



# SGMOP07D

## 3MHz, Low Noise, High Voltage, Precision Operational Amplifier

### GENERAL DESCRIPTION

The SGMOP07D is a single, low noise and low offset voltage operational amplifier. It is optimized for high voltage operation from 3.6V to 36V single supply or  $\pm 1.8V$  to  $\pm 18V$  dual supplies, while consuming only 0.9mA quiescent current.

The SGMOP07D is well suited in low noise systems. It exhibits a high gain-bandwidth product of 3MHz and a slew rate of  $4V/\mu s$ . The output swing is rail-to-rail with heavy loads. These specifications make the operational amplifier appropriate for various applications.

The SGMOP07D is available in a Green SOIC-8 package. It is specified over the extended  $-40^{\circ}C$  to  $+125^{\circ}C$  temperature range.

### FEATURES

- **Low Noise:**  $8.5nV/\sqrt{Hz}$  at 1kHz
- **Low Bias Current:**  $\pm 1nA$  (TYP)
- **High Open-Loop Gain:** 120dB at  $V_s = \pm 15V$
- **High PSRR:** 146dB
- **High Gain-Bandwidth Product:** 3MHz
- **Settling Time to 0.1% with 1V Step:**  $0.5\mu s$
- **Overload Recovery Time:**  $10\mu s$
- **Rail-to-Rail Output**
- **Support Single or Dual Power Supplies:**  
 $3.6V$  to  $36V$  or  $\pm 1.8V$  to  $\pm 18V$
- **Input Common Mode Voltage Range:**  
 $(-V_s) + 1.5V$  to  $(+V_s) - 2V$
- **Low Quiescent Current:** 0.9mA (TYP)
- **$-40^{\circ}C$  to  $+125^{\circ}C$  Operating Temperature Range**
- **Available in a Green SOIC-8 Package**

### APPLICATIONS

Sensors  
Audio  
Active Filters  
A/D Converters  
Communications  
Test Equipment  
Cellular and Cordless Phones  
Laptops and PDAs  
Photodiode Amplification

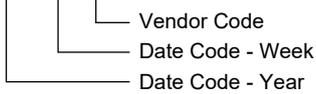
**PACKAGE/ORDERING INFORMATION**

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGMOP07D	SOIC-8	-40°C to +125°C	SGMOP07DXS8G/TR	OP07D XXXXX	Tape and Reel, 2500

**MARKING INFORMATION**

NOTE: XXXXX = Date Code and Vendor Code.

**XXXXX**



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

**ABSOLUTE MAXIMUM RATINGS**

- Supply Voltage, +V<sub>S</sub> to -V<sub>S</sub> ..... 40V
- Input Common Mode Voltage Range ..... (-V<sub>S</sub>) - 0.3V to (+V<sub>S</sub>) + 0.3V
- Junction Temperature ..... +150°C
- Storage Temperature Range ..... -65°C to +150°C
- Lead Temperature (Soldering, 10s) ..... +260°C
- ESD Susceptibility
- HBM ..... 2000V
- MM ..... 200V
- CDM ..... 1000V

**RECOMMENDED OPERATING CONDITIONS**

- Supply Voltage Range ..... 3.6V to 36V
- Operating Temperature Range ..... -40°C to +125°C

**OVERSTRESS CAUTION**

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

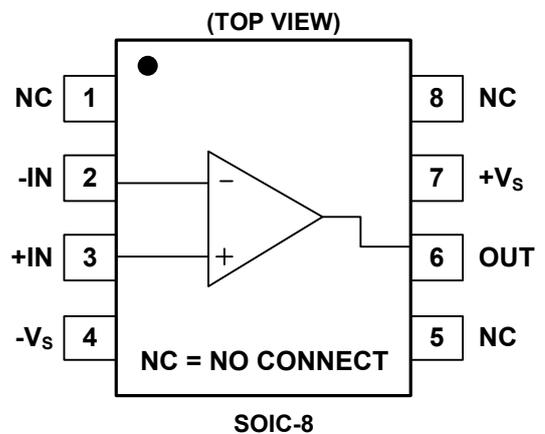
**ESD SENSITIVITY CAUTION**

This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

**DISCLAIMER**

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

**PIN CONFIGURATION**



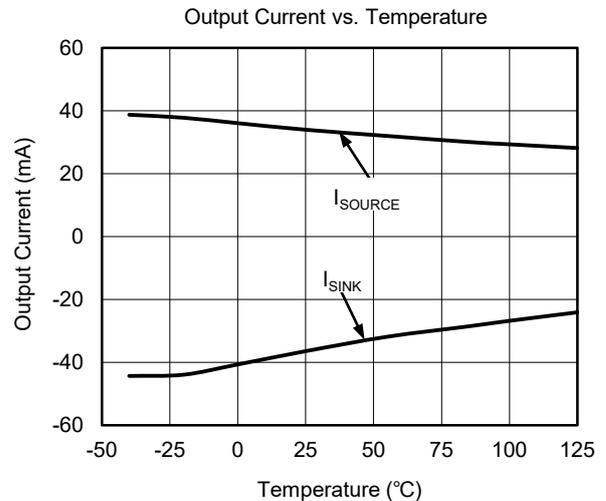
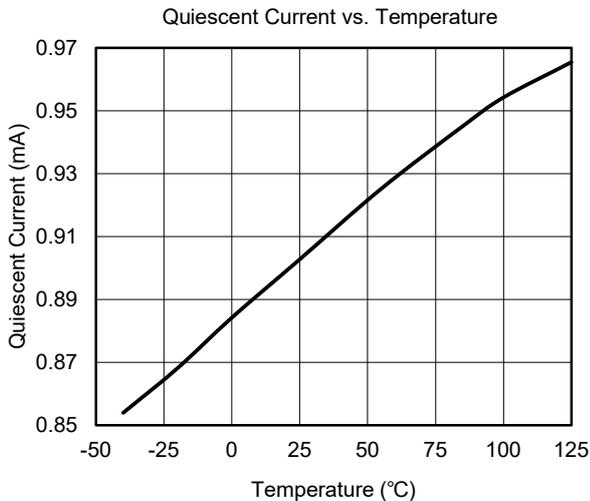
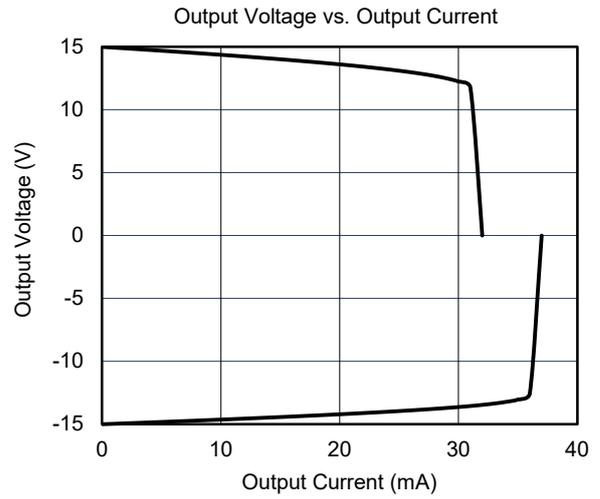
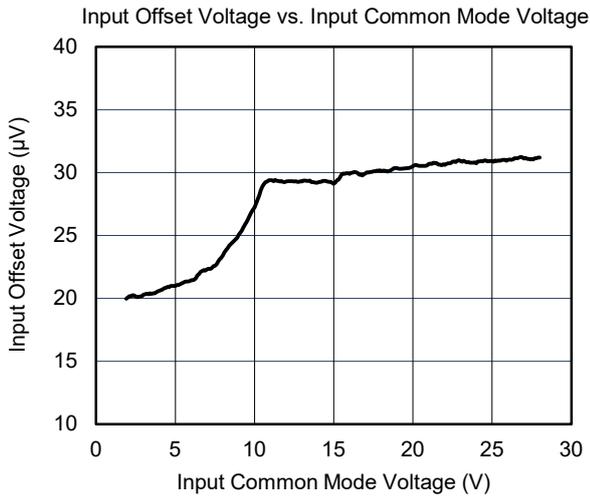
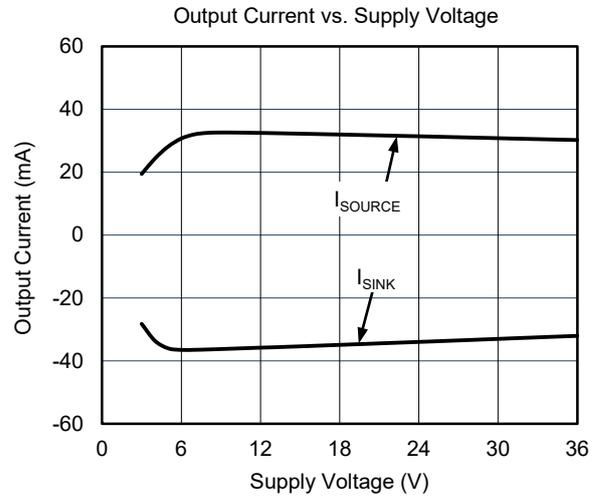
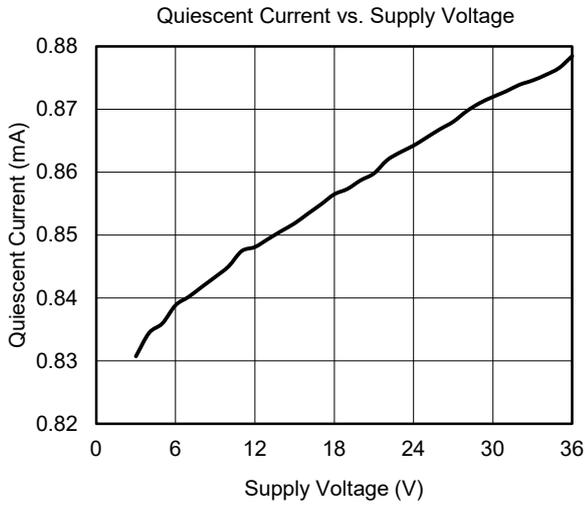
**ELECTRICAL CHARACTERISTICS**

( $V_S = \pm 5V$  to  $V_S = \pm 15V$ ,  $V_{CM} = 0V$ ,  $V_{OUT} = 0V$  and  $R_L$  connected to  $0V$ , Full =  $-40^\circ C$  to  $+125^\circ C$ , typical values are at  $T_A = +25^\circ C$ , unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	TEMP	MIN	TYP	MAX	UNITS
<b>Input Characteristics</b>							
Input Offset Voltage	$V_{OS}$		+25°C			200	μV
			Full			320	
Input Bias Current	$I_B$	$V_{CM} = V_S/2$	+25°C		±1	±14	nA
			Full			±52	
Input Offset Current	$I_{OS}$	$V_{CM} = V_S/2$	+25°C		±1	±15	nA
			Full			±28	
Input Common Mode Voltage Range	$V_{CM}$		Full	$(-V_S) + 1.5$		$(+V_S) - 2$	V
Common Mode Rejection Ratio	CMRR	$(-V_S) + 1.5V \leq V_{CM} \leq (+V_S) - 2V$	+25°C	120	140		dB
			Full	118			
Open-Loop Voltage Gain	$A_{OL}$	$V_S = \pm 5V, V_{OUT} = \pm 2.5V, R_L = 10k\Omega$	+25°C	115	135		dB
			Full	113			
		$V_S = \pm 15V, V_{OUT} = \pm 10V, R_L = 10k\Omega$	+25°C	117	126		
			Full	109			
		$V_S = \pm 5V, V_{OUT} = \pm 2.5V, R_L = 2k\Omega$	+25°C	105	112		
			Full	94			
		$V_S = \pm 15V, V_{OUT} = \pm 10V, R_L = 2k\Omega$	+25°C	112	120		
			Full	102			
Input Offset Voltage Drift	$\Delta V_{OS}/\Delta T$		Full		0.5		μV/°C
<b>Output Characteristics</b>							
Output Voltage Swing from Rail	$V_{OUT}$	$V_S = \pm 15V, R_L = 10k\Omega$	+25°C		90	175	mV
			Full			210	
		$V_S = \pm 15V, R_L = 2k\Omega$	+25°C		450	850	
			Full			1050	
Output Short-Circuit Current	$I_{SC}$		+25°C	±14	±32		mA
<b>Power Supply</b>							
Operating Voltage Range	$V_S$		Full	3.6		36	V
Quiescent Current/Amplifier	$I_Q$	$I_{OUT} = 0mA$	+25°C		0.9	1.2	mA
			Full			1.3	
Power Supply Rejection Ratio	PSRR	$V_S = 3V$ to $38V$	+25°C	125	146		dB
			Full	121			
<b>Dynamic Performance</b>							
Gain-Bandwidth Product	GBP	$V_{OUT} = 100mV_{P-P}, R_L = 2k\Omega, C_L = 10pF$	+25°C		3		MHz
Slew Rate	SR	$R_L = 2k\Omega$	+25°C		4		V/μs
Settling Time to 0.1%	$t_s$	$V_{IN} = 1V$ Step, $R_L = 2k\Omega, G = +1$	+25°C		0.5		μs
Overload Recovery Time		$R_L = 2k\Omega, V_{IN} \times G = V_S$	+25°C		10		μs
Phase Margin	$\phi_O$	$V_{OUT} = 100mV_{P-P}, R_L = 2k\Omega, C_L = 10pF$	+25°C		55		°
Total Harmonic Distortion + Noise	THD+N	$V_{IN} = 1V_{RMS}, G = +1, R_L = 2k\Omega, f = 1kHz$	+25°C		0.0008		%
<b>Noise</b>							
Input Voltage Noise		$f = 0.1Hz$ to $10Hz$	+25°C		300		nV <sub>P-P</sub>
Input Voltage Noise Density	$e_n$	$f = 1kHz$	+25°C		8.5		nV/ $\sqrt{Hz}$
Input Current Noise Density	$i_n$	$f = 1kHz$	+25°C		1.5		pA/ $\sqrt{Hz}$

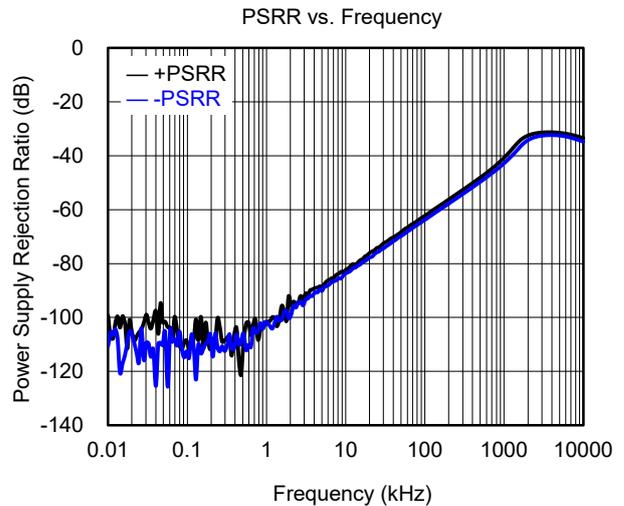
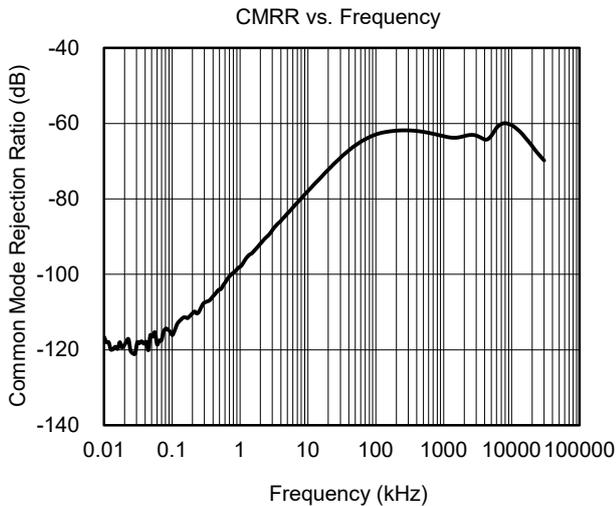
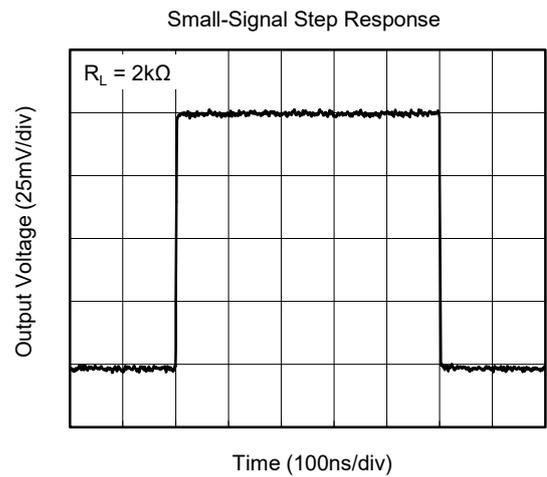
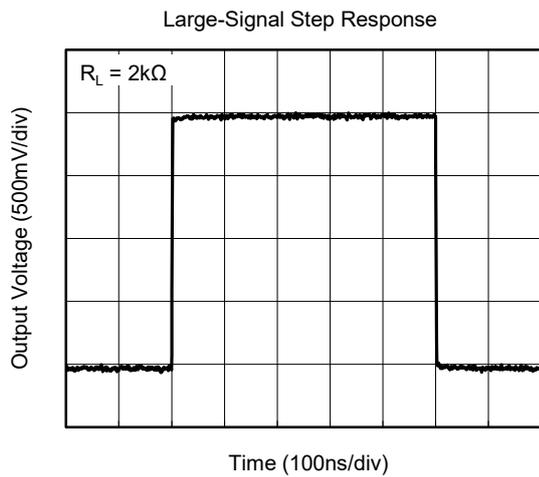
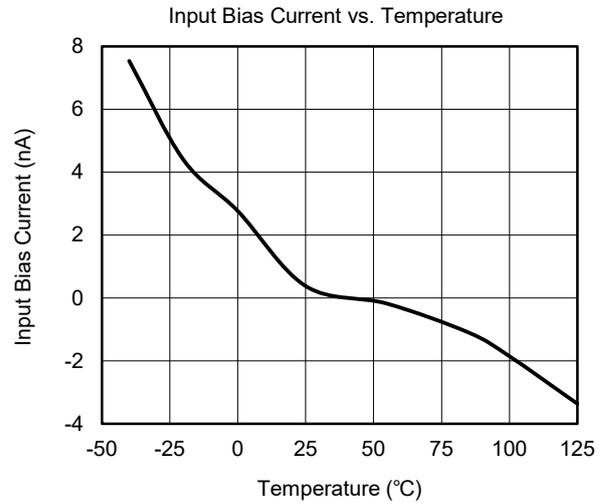
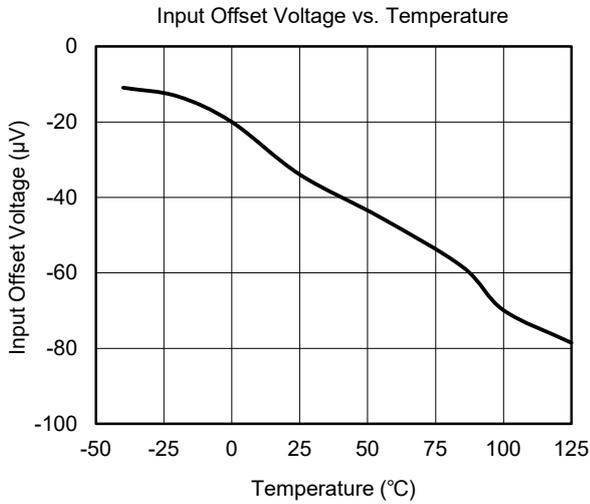
TYPICAL PERFORMANCE CHARACTERISTICS

At  $T_A = +25^\circ\text{C}$  and  $V_S = \pm 15\text{V}$ , unless otherwise noted.



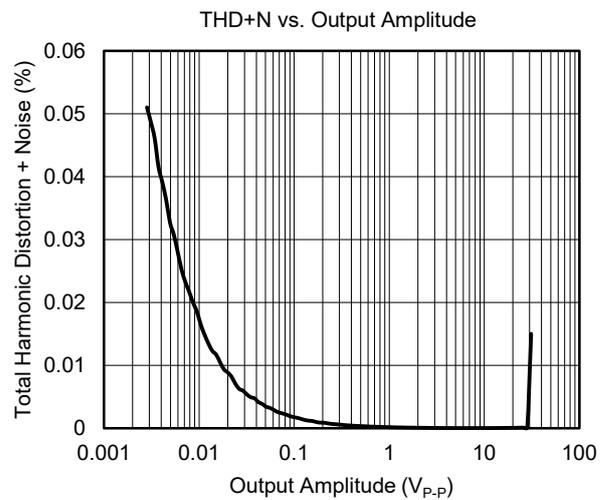
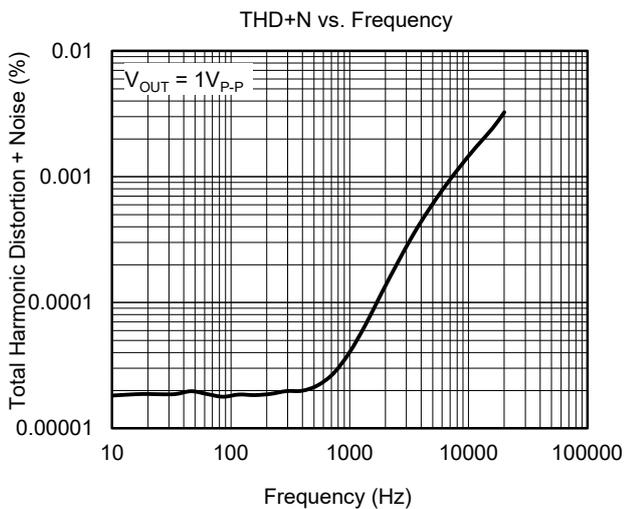
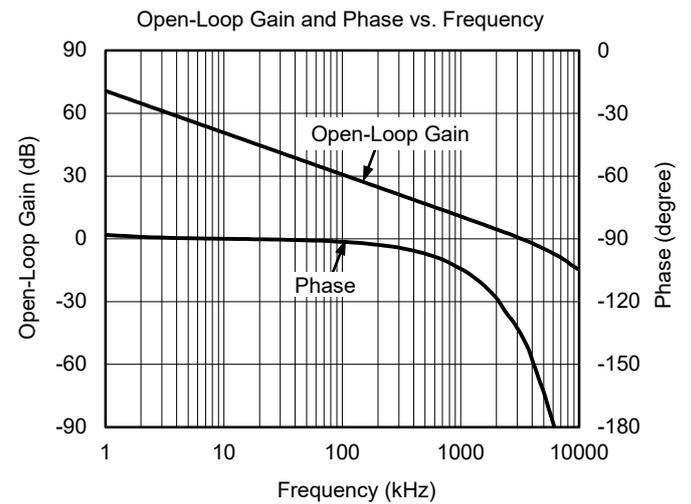
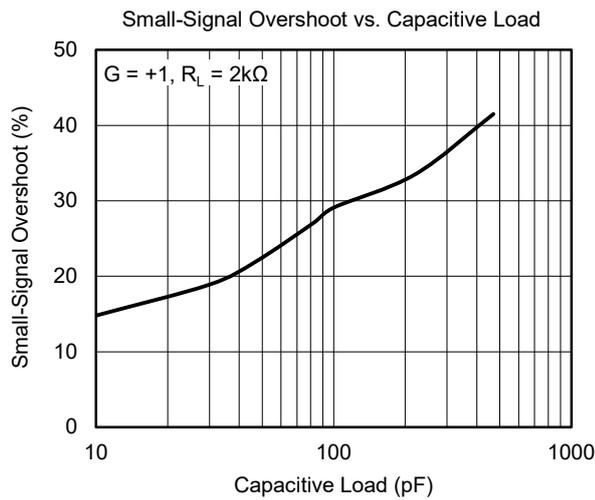
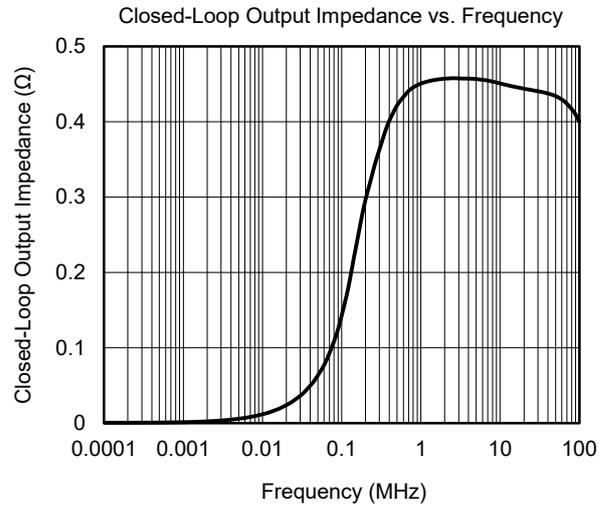
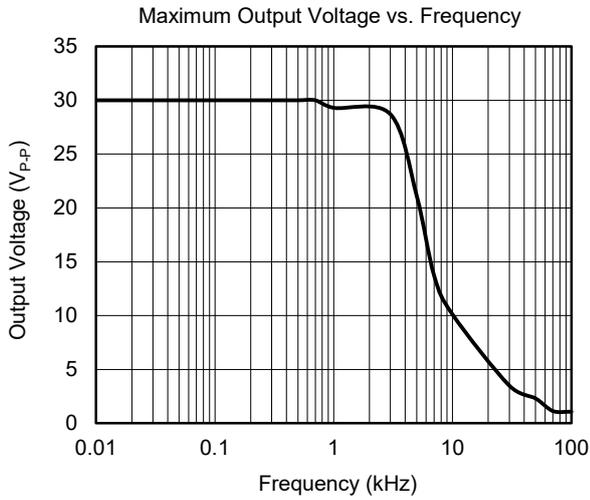
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

At  $T_A = +25^\circ\text{C}$  and  $V_S = \pm 15\text{V}$ , unless otherwise noted.



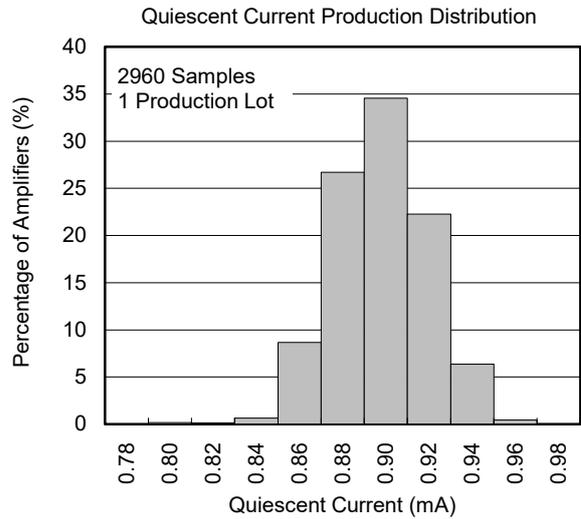
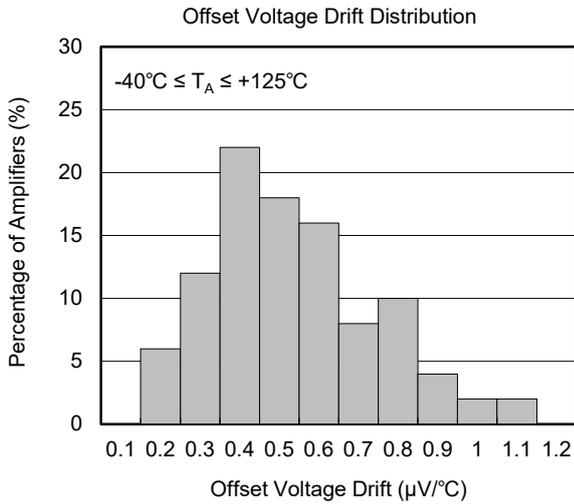
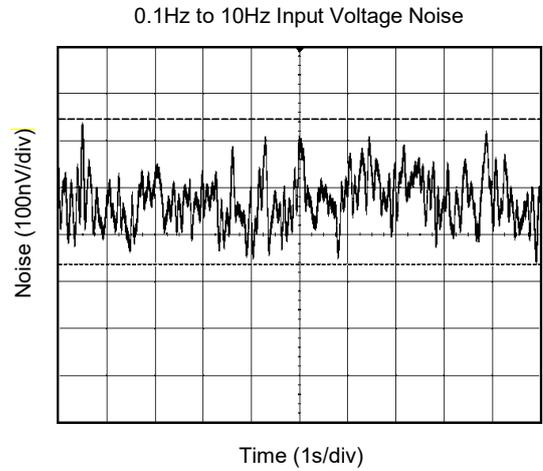
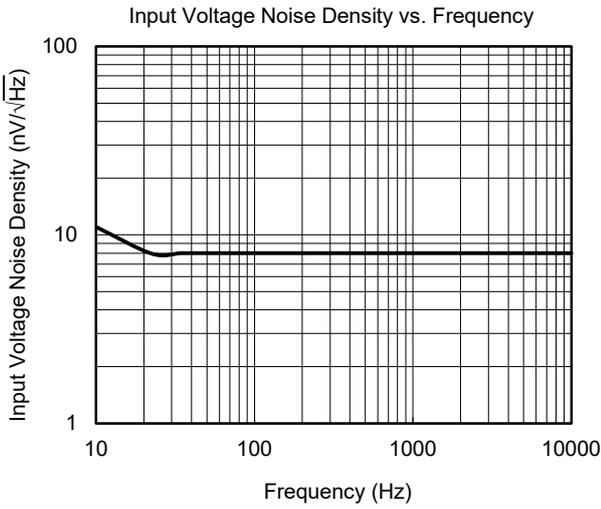
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

At  $T_A = +25^\circ\text{C}$  and  $V_S = \pm 15\text{V}$ , unless otherwise noted.



**TYPICAL PERFORMANCE CHARACTERISTICS (continued)**

At  $T_A = +25^\circ\text{C}$  and  $V_S = \pm 15\text{V}$ , unless otherwise noted.



**APPLICATION INFORMATION**

**Power Supply Decoupling and Layout**

A clean and low noise power supply is very important in amplifier circuit design, besides of input signal noise, the power supply is one of important source of noise to the amplifier through +V<sub>S</sub> and -V<sub>S</sub> pins. Power supply bypassing is an effective method to clear up the noise at power supply, and the low impedance path to ground of decoupling capacitor will bypass the noise to GND. In application, 10μF ceramic capacitor paralleled with 0.1μF or 0.01μF ceramic capacitor is used in Figure 1. The ceramic capacitors should be placed as close as possible to +V<sub>S</sub> and -V<sub>S</sub> power supply pins.

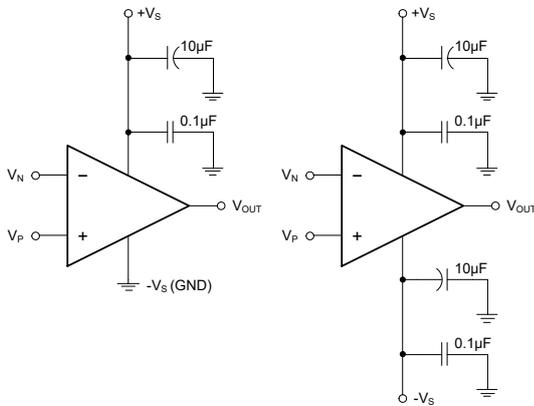


Figure 1. Amplifier Power Supply Bypassing

**Grounding**

In low speed application, one node grounding technique is the simplest and most effective method to eliminate the noise generated by grounding. In high speed application, the general method to eliminate noise is to use a complete ground plane technique, and the whole ground plane will help distribute heat and reduce EMI noise pickup.

**Reduce Input-to-Output Coupling**

To reduce the input-to-output coupling, the input traces must be placed as far away from the power supply or output traces as possible. The sensitive trace must not be placed in parallel with the noisy trace in same layer. They must be placed perpendicularly in different layers to reduce the crosstalk. These PCB layout techniques will help to reduce unwanted positive feedback and noise.

**Typical Application Circuits**

**Difference Amplifier**

The circuit in Figure 2 is a design example of classical difference amplifier. If  $R_4/R_3 = R_2/R_1$ , then  $V_{OUT} = (V_P - V_N) \times R_2/R_1 + V_{REF}$ .

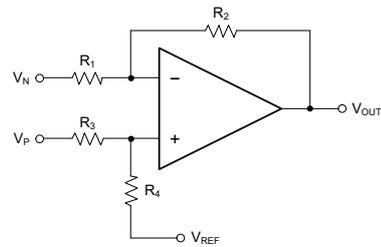


Figure 2. Difference Amplifier

**High Input Impedance Difference Amplifier**

The circuit in Figure 3 is a design example of high input impedance difference amplifier, the added amplifiers at the input are used to increase the input impedance and eliminate drawback of low input impedance in Figure 2.

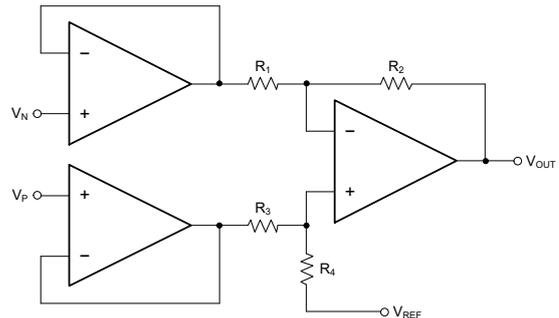


Figure 3. High Input Impedance Difference Amplifier

**Active Low-Pass Filter**

The circuit in Figure 4 is a design example of active low-pass filter, the DC gain is equal to  $-R_2/R_1$  and the -3dB corner frequency is equal to  $1/2\pi R_2 C$ . In this design, the filter bandwidth must be less than the bandwidth of the amplifier, the resistor values must be selected as low as possible to reduce ringing or oscillation generated by the parasitic parameters in PCB layout.

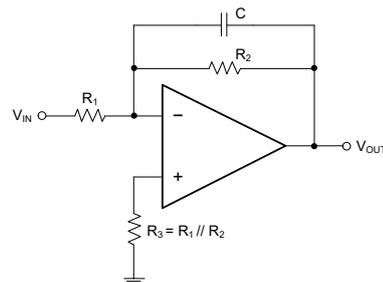


Figure 4. Active Low-Pass Filter

**REVISION HISTORY**

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

<b>MARCH 2023 – REV.A.1 to REV.A.2</b>	<b>Page</b>
Updated Typical Performance Characteristics section .....	5

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<b>AUGUST 2017 – REV.A to REV.A.1</b>	<b>Page</b>
Updated open-loop gain and phase vs. frequency .....	6

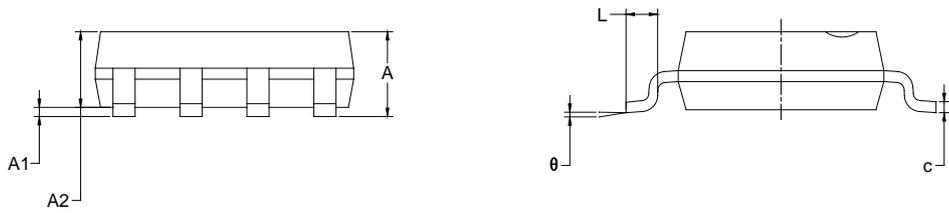
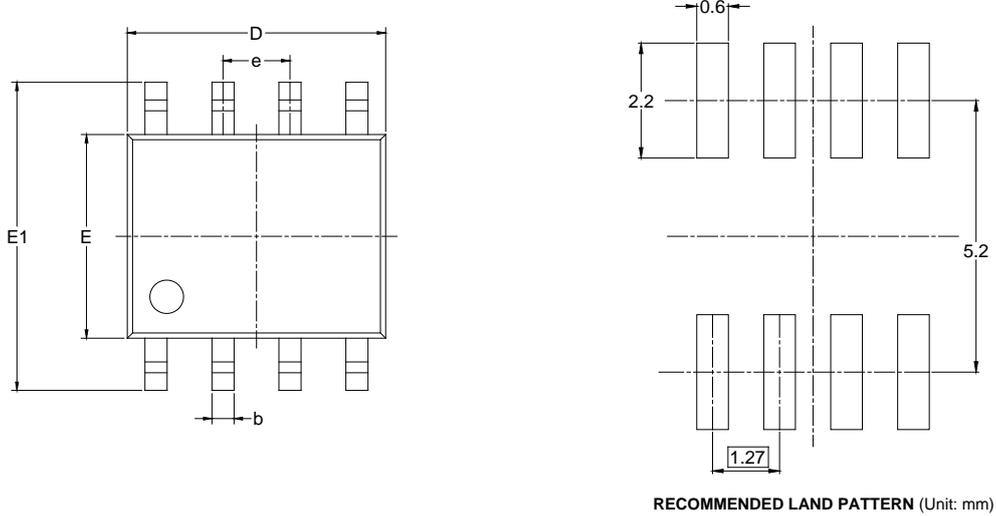
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<b>Changes from Original (AUGUST 2017) to REV.A</b>	<b>Page</b>
Changed from product preview to production data .....	All

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PACKAGE OUTLINE DIMENSIONS

SOIC-8

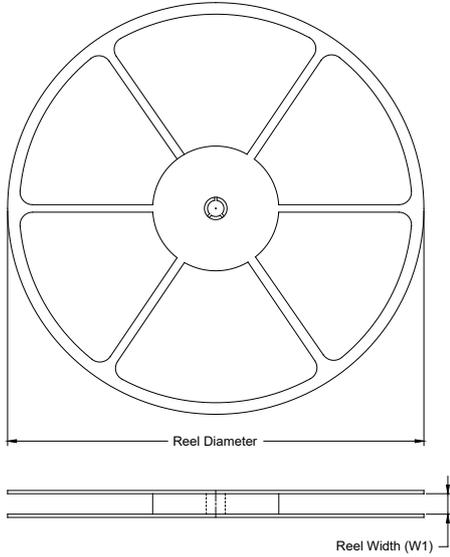


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.27 BSC		0.050 BSC	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

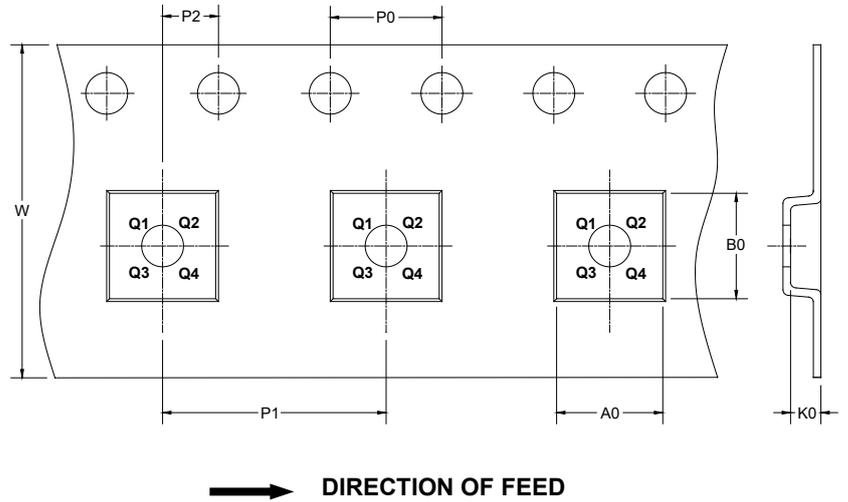
NOTES:  
 1. Body dimensions do not include mode flash or protrusion.  
 2. This drawing is subject to change without notice.

**TAPE AND REEL INFORMATION**

**REEL DIMENSIONS**



**TAPE DIMENSIONS**



NOTE: The picture is only for reference. Please make the object as the standard.

**KEY PARAMETER LIST OF TAPE AND REEL**

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
SOIC-8	13"	12.4	6.40	5.40	2.10	4.0	8.0	2.0	12.0	Q1

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# PACKAGE INFORMATION

## CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

## KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13"	386	280	370	5

DD0002