



# SGM621E

## Low Power, Low Noise, Rail-to-Rail Output, Instrumentation Amplifier

### GENERAL DESCRIPTION

The SGM621E is a high accuracy, high voltage instrumentation amplifier, which is designed to set any gain from 1 to 10000 with one external resistor. The device works well in battery-powered applications due to the low power consumption of 1.3mA typical quiescent current. The SGM621E provides SOIC-8 and MSOP-8 packages which are much smaller than discrete classical-three-OPAs circuits.

The SGM621E provides 140ppm (MAX) non-linearity and 55 $\mu$ V (MAX) low input offset voltage. The device also features low noise, low bias current and low power. The combination of these characteristics makes it a good choice for applications requiring excellent DC performance.

The SGM621E offers 6nV/ $\sqrt{\text{Hz}}$  low input voltage noise, 300fA/ $\sqrt{\text{Hz}}$  input current noise at 1kHz, and 0.4 $\mu$ V<sub>P-P</sub> in the 0.1Hz to 10Hz band. It is suitable for pre-amplifier applications. The 10 $\mu$ s settling time to 0.01% makes SGM621E appropriate for multiplexed applications.

The SGM621E is available in Green SOIC-8 and MSOP-8 packages. It is specified over the extended -40°C to +125°C temperature range.

### FEATURES

- **Single External Resistor Gain Set (Set Gain from 1 to 10000)**
- **Input Offset Voltage: 55 $\mu$ V (MAX)**
- **Input Bias Current: 15nA (TYP)**
- **Common Mode Rejection Ratio: 120dB (TYP) (G = 10)**
- **Input Voltage Noise: 6nV/ $\sqrt{\text{Hz}}$  at 1kHz**
- **0.1Hz to 10Hz Voltage Noise: 0.4 $\mu$ V<sub>P-P</sub> (G = 100)**
- **Bandwidth: 140kHz (G = 100)**
- **Settling Time to 0.01%: 10 $\mu$ s (G = 100)**
- **Rail-to-Rail Output**
- **Support Single or Dual Power Supplies: 4.6V to 36V or  $\pm$ 2.3V to  $\pm$ 18V**
- **Low Power Supply Current: 1.3mA (TYP)**
- **-40°C to +125°C Operating Temperature Range**
- **Available in Green SOIC-8 and MSOP-8 Packages**

### APPLICATIONS

Precision Current Measurement  
Pressure Measurement

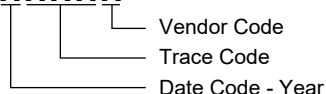
**PACKAGE/ORDERING INFORMATION**

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM621E	SOIC-8	-40°C to +125°C	SGM621EXS8G/TR	SGM 621EXS8 XXXXX	Tape and Reel, 4000
	MSOP-8	-40°C to +125°C	SGM621EXMS8G/TR	SGM621E XMS8 XXXXX	Tape and Reel, 4000

**MARKING INFORMATION**

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.

**XXXXX**



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

**ABSOLUTE MAXIMUM RATINGS**

Supply Voltage, +V <sub>S</sub> to -V <sub>S</sub> .....	40V
Input Common Mode Voltage .....	±V <sub>S</sub>
Package Thermal Resistance	
SOIC-8, θ <sub>JA</sub> .....	116.6°C/W
SOIC-8, θ <sub>JB</sub> .....	66.6°C/W
MSOP-8, θ <sub>JA</sub> .....	134.3°C/W
MSOP-8, θ <sub>JB</sub> .....	75.9°C/W
Junction Temperature .....	+150°C
Storage Temperature Range.....	-65°C to +150°C
Lead Temperature (Soldering, 10s) .....	+260°C
ESD Susceptibility <sup>(1) (2)</sup>	
HBM.....	±7000V
CDM .....	±1000V

NOTES:

1. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.
2. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

**RECOMMENDED OPERATING CONDITIONS**

Operating Temperature Range .....	-40°C to +125°C
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**OVERSTRESS CAUTION**

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

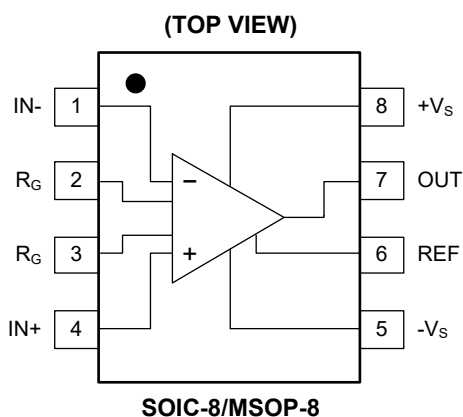
**ESD SENSITIVITY CAUTION**

This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

**DISCLAIMER**

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATIONS



PIN DESCRIPTION

PIN	NAME	FUNCTION
1	IN-	Inverting Input Pin.
2, 3	R <sub>G</sub>	Gain Setting Pin. The gain can be set by placing the resistor across R <sub>G</sub> . $G = 1 + (49.4k\Omega/R_G)$ .
4	IN+	Non-Inverting Input Pin.
5	-V <sub>S</sub>	Negative Power Supply Pin.
6	REF	Voltage Reference Pin. A voltage source with low impedance can be placed to supply this terminal in order to shift the output level.
7	OUT	Output Pin.
8	+V <sub>S</sub>	Positive Power Supply Pin.

**ELECTRICAL CHARACTERISTICS**

( $V_S = \pm 15V$ ,  $R_L = 2k\Omega$ , Full =  $-40^\circ C$  to  $+125^\circ C$ , typical values are at  $T_A = +25^\circ C$ , unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	TEMP	MIN	TYP	MAX	UNITS
<b>Gain (<math>G = 1 + (49.4k\Omega/R_G)</math>)</b>							
Gain Range				1		10000	
Gain Error <sup>(1)</sup>	GE	$V_{OUT} = -10V$ to $+10V$	G = 1	+25°C	0.01	0.05	%
				Full		0.1	
			G = 10	+25°C	0.05	0.2	
				Full		0.5	
			G = 100	+25°C	0.05	0.2	
				Full		0.5	
G = 1000	+25°C	0.05	0.2				
	Full		0.5				
Gain Temperature Coefficient			G = 1	Full	1		ppm/°C
			G > 1	Full	20		
Non-Linearity		$V_{OUT} = -10V$ to $+10V$	G = 1	+25°C	10	70	ppm
				Full		100	
			G = 10	+25°C	10	70	
				Full		100	
			G = 100	+25°C	10	70	
				Full		100	
G = 1000	+25°C	20	140				
	Full		170				
<b>Voltage Offset (Total RTI Error = <math>V_{OSI} + V_{OSO}/G</math>)</b>							
Input Offset Voltage	$V_{OSI}$	$V_S = \pm 5V$ to $\pm 15V$	+25°C		7	55	$\mu V$
			Full			150	
Input Offset Voltage Drift	$\Delta V_{OSI}/\Delta T$		Full		0.1		$\mu V/^\circ C$
Output Offset Voltage	$V_{OSO}$	$V_S = \pm 5V$ to $\pm 15V$	+25°C		80	600	$\mu V$
			Full			1200	
Output Offset Voltage Drift	$\Delta V_{OSO}/\Delta T$		Full		1.5		$\mu V/^\circ C$
Offset Referred to the Input vs. Power Supply	PSRR	$V_S = \pm 2.3V$ to $\pm 18V$	G = 1	+25°C	110	120	dB
				Full	100		
			G = 10	+25°C	125	130	
				Full	112		
			G = 100	+25°C	128	140	
				Full	125		
G = 1000	+25°C	128	140				
	Full	125					

NOTE: 1. Effects of external resistor  $R_G$  is not included.

**ELECTRICAL CHARACTERISTICS (continued)**(V<sub>S</sub> = ±15V, R<sub>L</sub> = 2kΩ, Full = -40°C to +125°C, typical values are at T<sub>A</sub> = +25°C, unless otherwise noted.)

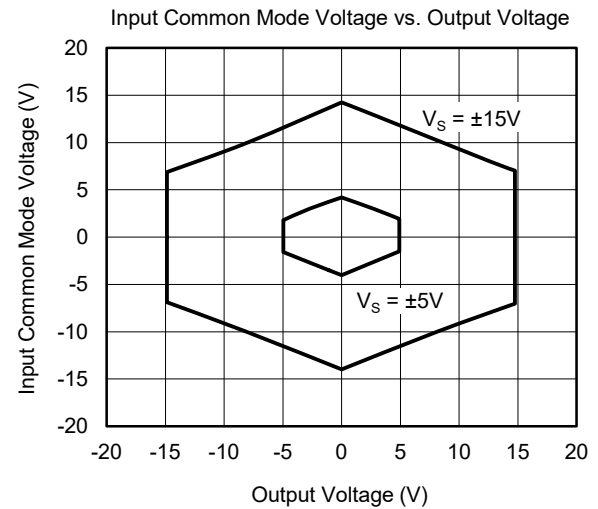
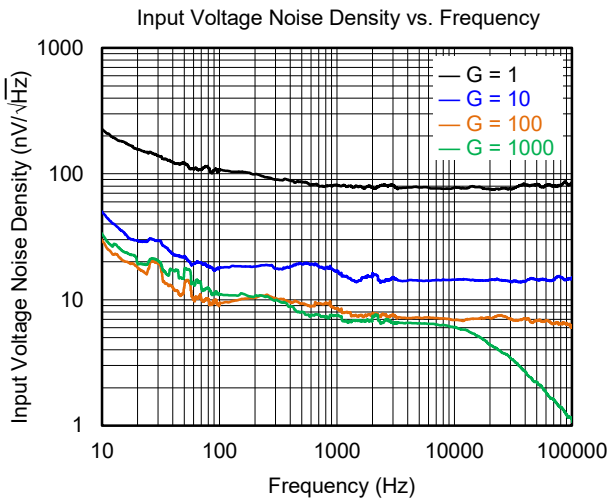
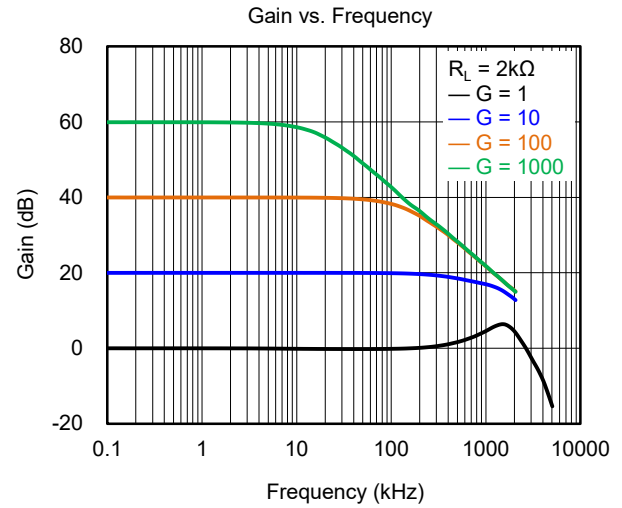
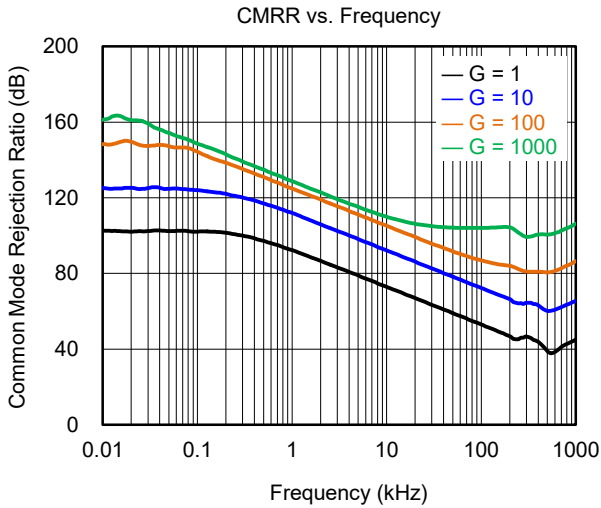
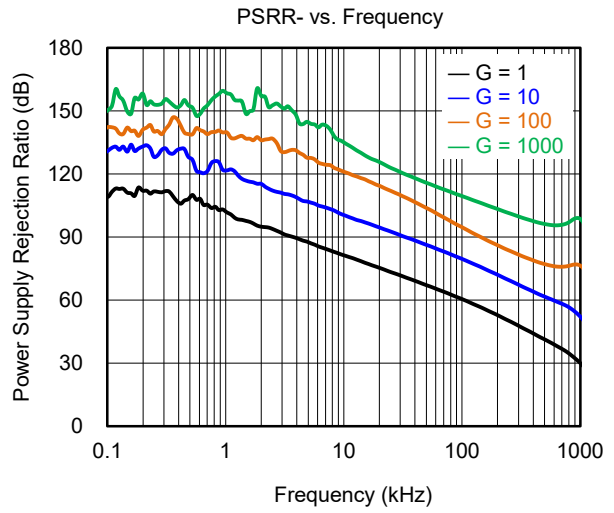
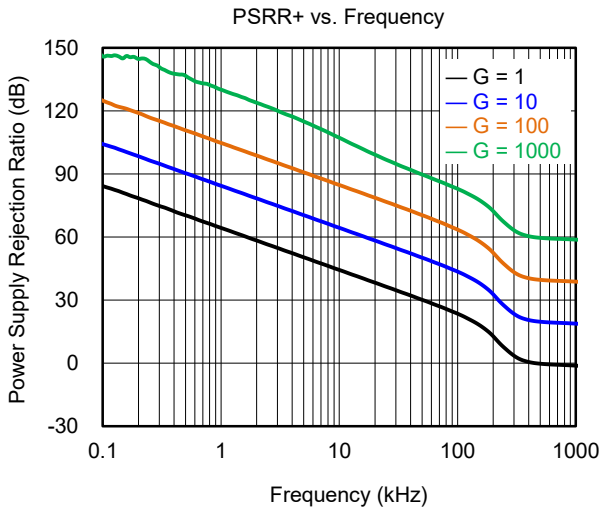
PARAMETER		SYMBOL	CONDITIONS	TEMP	MIN	TYP	MAX	UNITS
<b>Input Current</b>								
Input Bias Current	I <sub>B</sub>			+25°C		15	30	nA
				Full			50	
Average Temperature Coefficient of Input Bias Current		ΔI <sub>B</sub> /ΔT		Full		0.15		nA/°C
Input Offset Current	I <sub>OS</sub>			+25°C		5	18	nA
				Full			20	
Average Temperature Coefficient of Input Offset Current		ΔI <sub>OS</sub> /ΔT		Full		0.05		nA/°C
<b>Input</b>								
Input Impedance	Differential	Z <sub>DIFF</sub>		+25°C		10    4		GΩ    pF
	Common Mode	Z <sub>CM</sub>		+25°C		10    4		
Input Voltage Range			V <sub>S</sub> = ±2.3V to ±5V	+25°C	(-V <sub>S</sub> ) + 1.9		(+V <sub>S</sub> ) - 1.2	V
				Full	(-V <sub>S</sub> ) + 2.1		(+V <sub>S</sub> ) - 1.3	
			V <sub>S</sub> = ±5V to ±18V	+25°C	(-V <sub>S</sub> ) + 1.9		(+V <sub>S</sub> ) - 1.4	
				Full	(-V <sub>S</sub> ) + 2.1		(+V <sub>S</sub> ) - 1.4	
Common Mode Rejection Ratio with 1kΩ Source Imbalance	CMRR	V <sub>CM</sub> = -10V to +10V	G = 1	+25°C	80	100		dB
				Full	77			
			G = 10	+25°C	100	120		
				Full	92			
			G = 100	+25°C	105	130		
				Full	102			
			G = 1000	+25°C	105	130		
				Full	102			
<b>Reference Input</b>								
Reference Input Resistance		R <sub>REF</sub>		+25°C		18		kΩ
Reference Input Current	I <sub>REF</sub>	V <sub>IN+</sub> = V <sub>IN-</sub> = 0V, V <sub>REF</sub> = 0V		+25°C		30	45	μA
				Full			50	
<b>Output Characteristics</b>								
Output Voltage Swing	V <sub>OH</sub>	V <sub>S</sub> = ±18V		+25°C		310	450	mV
				Full			750	
	V <sub>OL</sub>	V <sub>S</sub> = ±18V		+25°C		150	220	
				Full			300	
Short-Circuit Current	I <sub>SC</sub>	V <sub>S</sub> = ±2.3V to ±18V, R <sub>L</sub> = 50Ω to V <sub>S</sub> /2		+25°C	12	24		mA
				Full	8			
<b>Power Supply</b>								
Quiescent Current	I <sub>Q</sub>	V <sub>S</sub> = ±2.3V to ±18V, I <sub>OUT</sub> = 0A		+25°C		1.3	1.8	mA
				Full			2.2	

**ELECTRICAL CHARACTERISTICS (continued)**(V<sub>S</sub> = ±15V, R<sub>L</sub> = 2kΩ, Full = -40°C to +125°C, typical values are at T<sub>A</sub> = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	TEMP	MIN	TYP	MAX	UNITS
<b>Dynamic Response</b>							
Small-Signal -3dB Bandwidth	BW		G = 1	+25°C		3900	kHz
			G = 10	+25°C		1000	
			G = 100	+25°C		140	
			G = 1000	+25°C		15	
Slew Rate	SR	V <sub>OUT</sub> = 1V <sub>P-P</sub> step	G = 1	+25°C		1.2	V/μs
Settling Time to 0.01%	t <sub>s</sub>	V <sub>OUT</sub> = 10V <sub>P-P</sub> step	G = 1 to 100	+25°C		10	μs
			G = 1000	+25°C		55	
<b>Noise</b>							
Input Voltage Noise Density	e <sub>ni</sub>	f = 1kHz		+25°C		6	nV/√Hz
Output Voltage Noise Density	e <sub>no</sub>	f = 1kHz		+25°C		80	nV/√Hz
0.1Hz to 10Hz Voltage Noise, RTI		f = 0.1Hz to 10Hz	G = 1	+25°C		6	μV <sub>P-P</sub>
			G = 10	+25°C		1	
			G = 100	+25°C		0.4	
			G = 1000	+25°C		0.4	
Input Current Noise Density, RTI	i <sub>n</sub>	f = 1kHz		+25°C		300	fA/√Hz
0.1Hz to 10Hz Current Noise, RTI		f = 0.1Hz to 10Hz		+25°C		15	pA <sub>P-P</sub>

TYPICAL PERFORMANCE CHARACTERISTICS

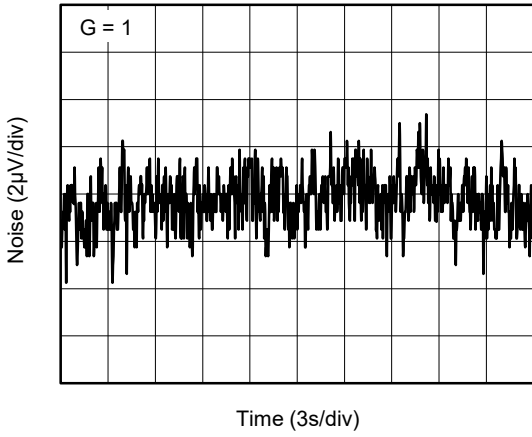
At  $T_A = +25^\circ\text{C}$ ,  $V_S = \pm 15\text{V}$ , unless otherwise noted.



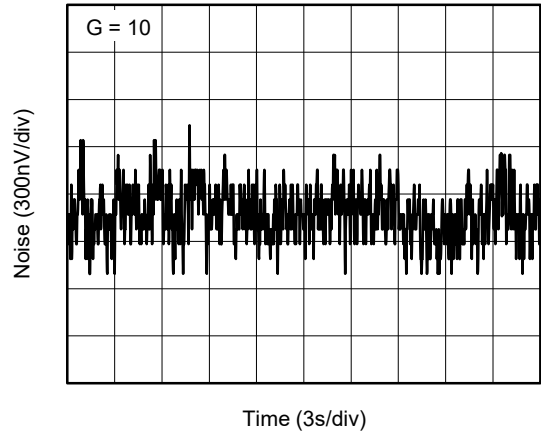
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

At  $T_A = +25^\circ\text{C}$ ,  $V_S = \pm 15\text{V}$ , unless otherwise noted.

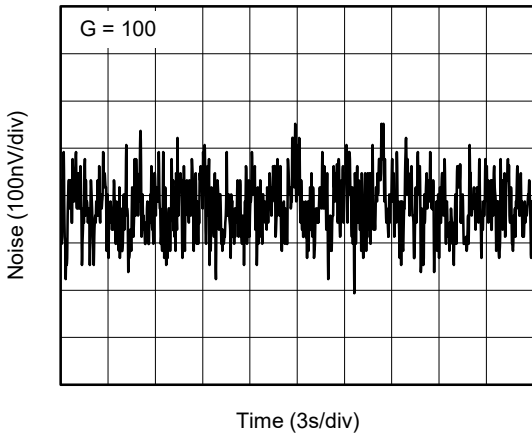
0.1Hz to 10Hz Input Voltage Noise



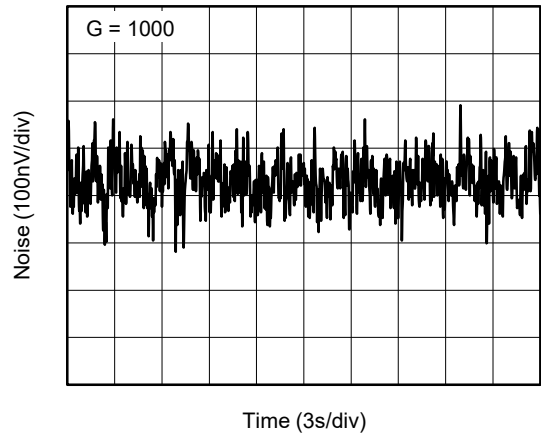
0.1Hz to 10Hz Input Voltage Noise



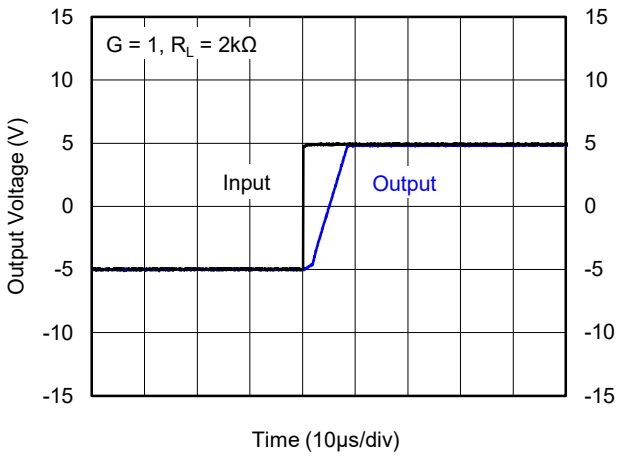
0.1Hz to 10Hz Input Voltage Noise



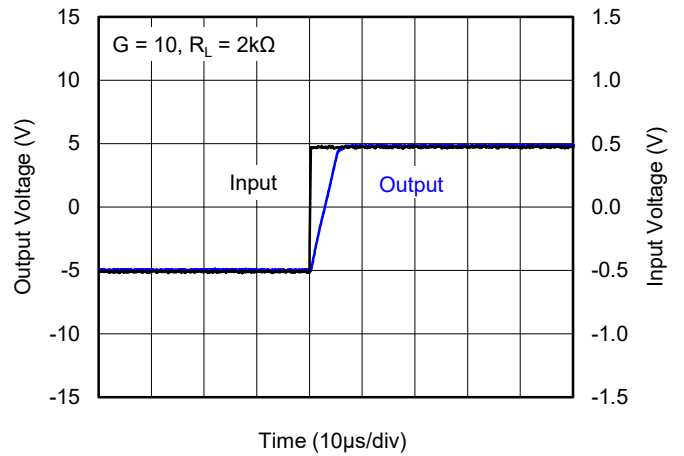
0.1Hz to 10Hz Input Voltage Noise



Settling Time

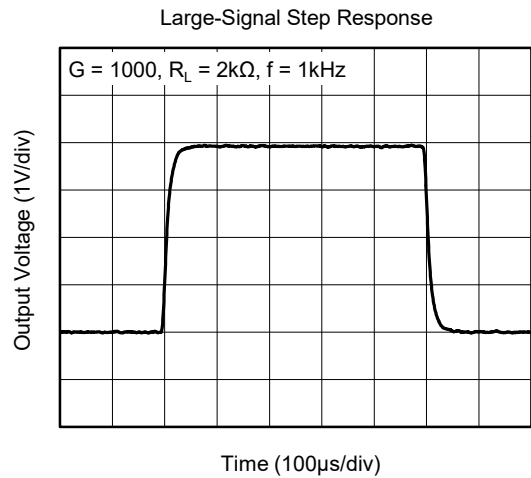
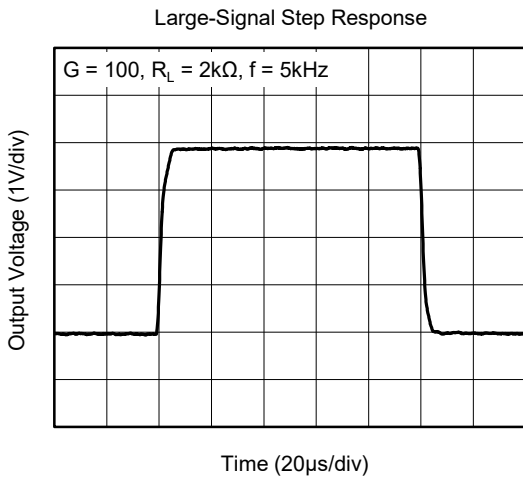
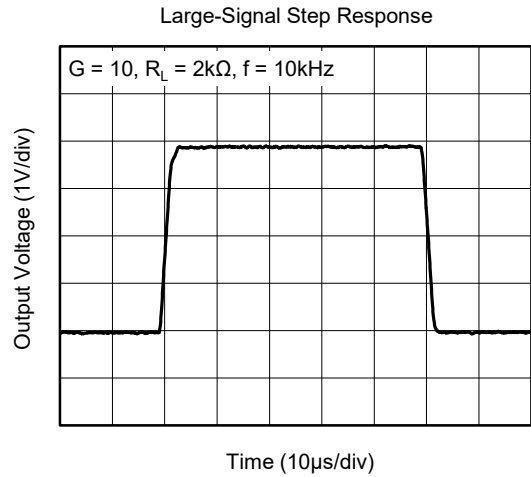
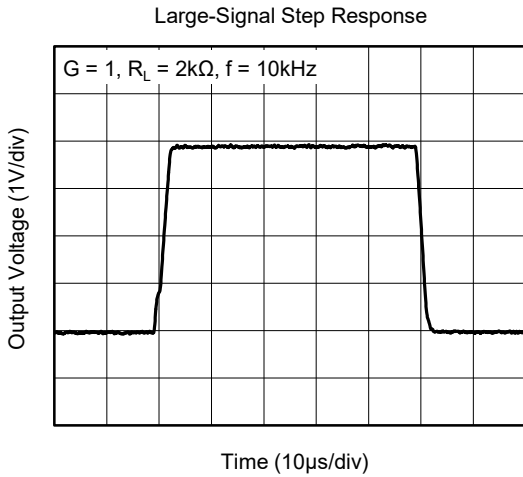
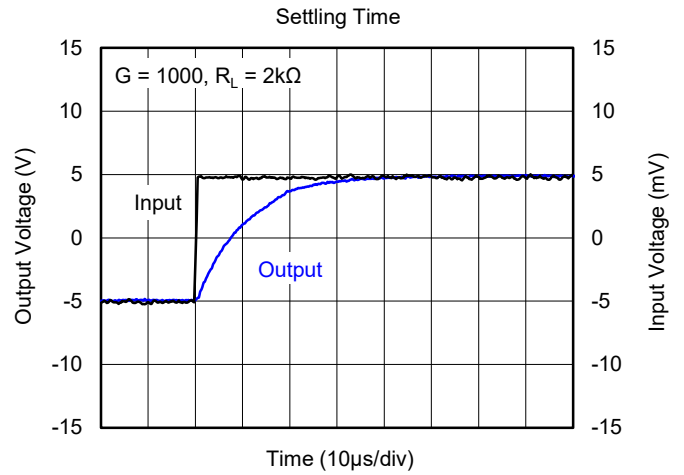
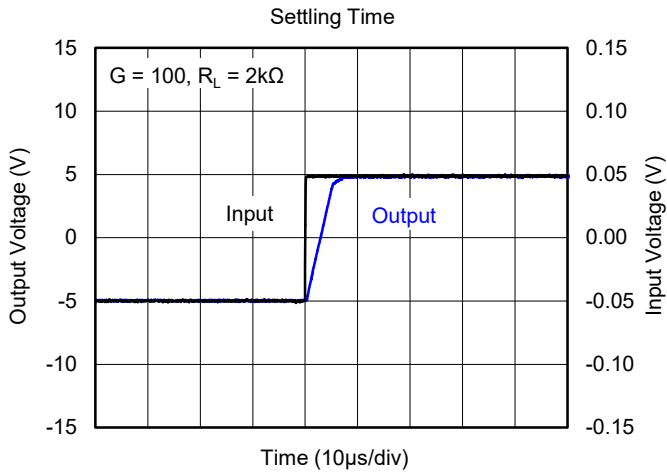


Settling Time



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

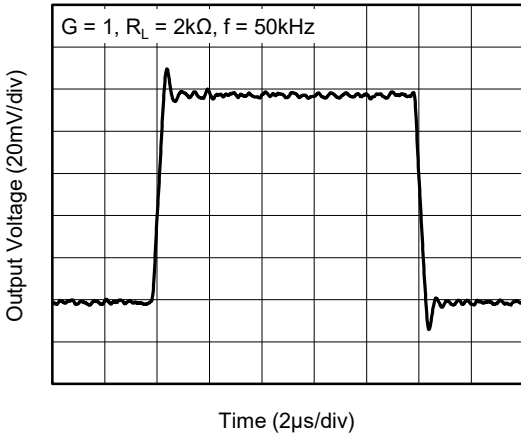
At  $T_A = +25^\circ\text{C}$ ,  $V_S = \pm 15\text{V}$ , unless otherwise noted.



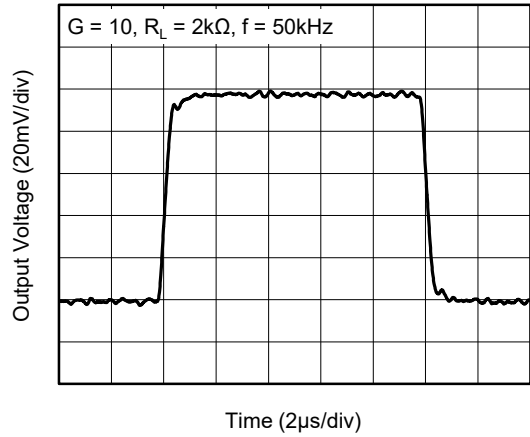
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

At  $T_A = +25^\circ\text{C}$ ,  $V_S = \pm 15\text{V}$ , unless otherwise noted.

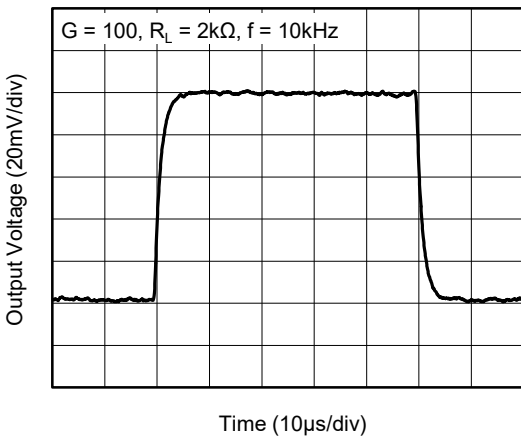
Small-Signal Step Response



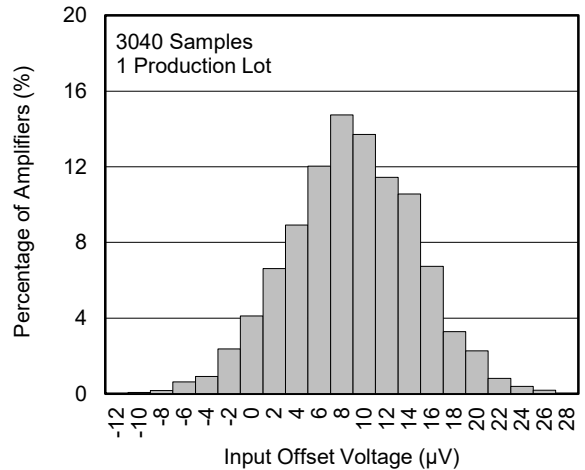
Small-Signal Step Response



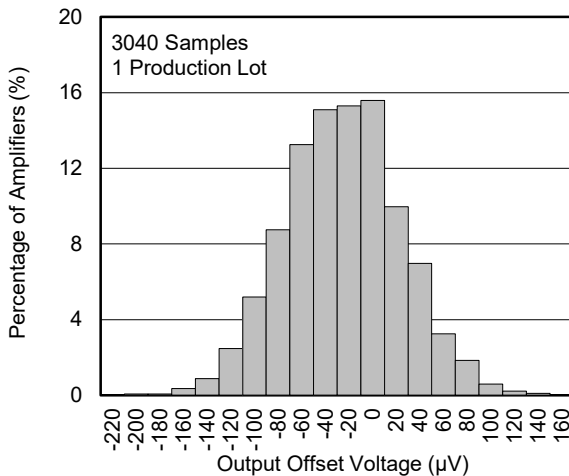
Small-Signal Step Response



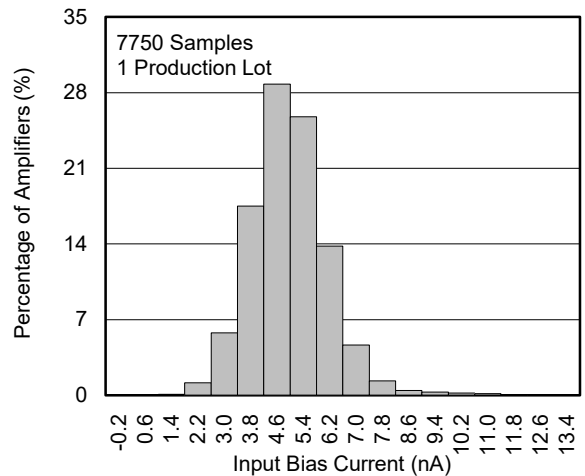
Input Offset Voltage Production Distribution



Output Offset Voltage Production Distribution



Input Bias Current Production Distribution



OPERATION THEORY

The SGM621E is modified with the classic three-op-amp and it is a holistic instrumentation amplifier.

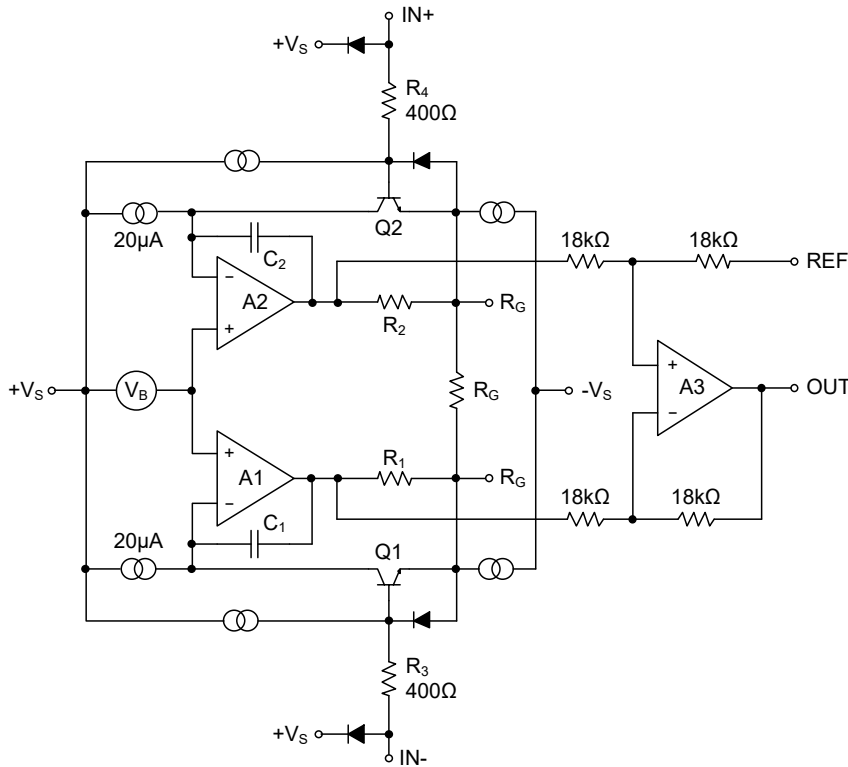


Figure 1. Simplified Schematic

The high precision input is provided by the two input transistor Q1 and Q2 (Figure 1) and this results in 10 × lower bias current of the input pins. The constant collector current of Q1 and Q2 is maintained by the two loops Q1-A1-R1 and Q2-A2-R2, so the input voltage is impressed across the gain setting resistor  $R_G$  of the amplifier. The differential gain from A1/A2 outputs can be expressed by  $G = 1 + (R_1+R_2)/R_G$ . The unity-gain subtractor (A3) can reject the common mode signal so that SGM621E produces a single-ended output with REF pin biased.

The transconductance of the pre-amplifier is determined by the resistance of  $R_G$ . The transconductance will increase gradually to that of the input transistors if the resistance of  $R_G$  is reduced for larger gains. The important benefits are shown below:

- ◆ Boosting the open-loop gain can also increase the programmed gain, so that the related error of gain is reduced.

- ◆ The gain-bandwidth product which is determined by the two capacitors  $C_1$ ,  $C_2$  and the transconductance of the pre-amplifier can increase with programmed gain, so that the frequency response is enhanced.

- ◆ Reducing the input voltage noise to  $6nV/\sqrt{Hz}$ , and it is determined by the base resistance and the collector current of the input.

The integrated resistors ( $R_1$  and  $R_2$ ) inside the SGM621E are set to 24.7kΩ, so that the gain can be programmed with the external resistor  $R_G$ .

The equation of gain is shown as below:

$$G = \frac{49.4k\Omega}{R_G} + 1$$

$$R_G = \frac{49.4k\Omega}{G - 1}$$



## SGM621E

### APPLICATION INFORMATION (continued)

#### Precision V-I Converter

It's easy to realize a precision current source (Figure 4) utilizing one SGM621E, another operational amplifier and two resistors. To obtain a better CMRR of SGM621E, a buffer should be placed between the REF pin and the OUT pin of the amplifier. The equation which is shown in Figure 4 illustrates the output current of the circuit.

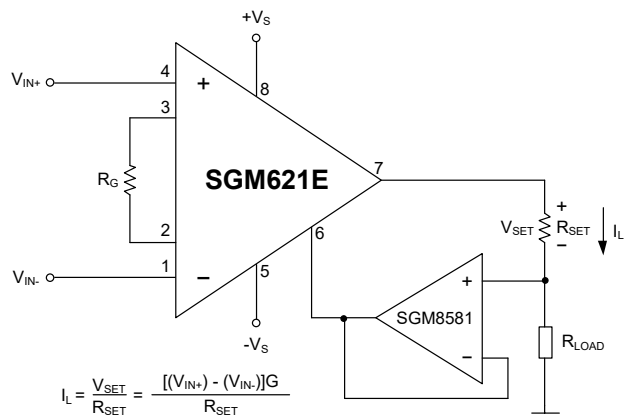


Figure 4. Precision Voltage-to-Current Converter

#### Input and Output Offset Voltage

Two main sources which are error of input and output result in the low errors of SGM621E. When referred to the input, the output error should be divided by the gain of the instrumentation amplifier. From the equations which are shown as below, the input error takes a leading position at large gains while the output error takes a leading position at small gains.

Total Error Referred to Input (RTI) = Input Error + (Output Error/G)

Total Error Referred to Output (RTO) = (Input Error × G) + Output Error

#### Terminal of Reference

Potential of the reference terminal defines the zero output voltage. It becomes extremely useful while the load is not tied to the precise ground of the rest of the system. The reference terminal provides one way to bias a precise voltage to the output, and the reference voltage should be in the range of 2V within the supply voltages. On top of these, to keep better CMRR, the parasitic resistor at this pin should be low.

#### Selection of Gain

The gain of the instrumentation amplifier is determined by the external resistor  $R_G$ . The accuracy of the external resistor  $R_G$  is important as it may influence the error of gain. It is recommended that selecting the resistor with 1% or 0.1% precision is a good choice. The following table shows the gain effect with the selection of 1% or 0.1% precision resistor. Also, leaving the pin 2 and pin 3 (the place of  $R_G$ ) open can make the gain of SGM621E equals to 1.

$$R_G = \frac{49.4k\Omega}{G - 1}$$

As mentioned before, the gain error can be minimized by equivalent parasitic resistor in series with  $R_G$ . Moreover, low TC of 1ppm/°C is required for the selection of  $R_G$  to avoid the gain drift of SGM621E.

Table 1. Different Values for Gain Resistor

1% STD Table Value of $R_G$ ( $\Omega$ )	Calculated Gain	0.1% STD Table Value of $R_G$ ( $\Omega$ )	Calculated Gain
49.9k	1.990	49.3k	2.002
12.4k	4.984	12.4k	4.984
5.49k	9.998	5.49k	9.998
2.61k	19.93	2.61k	19.93
1.00k	50.40	1.01k	49.91
499	100.0	499	100.0
249	199.4	249	199.4
100	495.0	98.8	501.0
49.9	991.0	49.3	1003.0

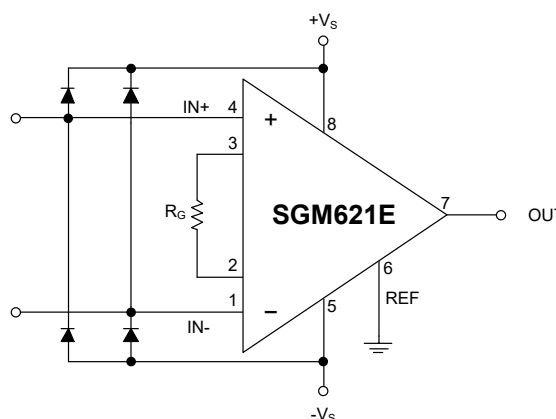


Figure 5. Diode for Protecting  $V_{IN}$  from Larger than  $V_S$

APPLICATION INFORMATION (continued)

RF Interference

One of the characteristics of instrumentation amplifier is rectifying the small signal which is out of the band. This kind of disturbance can be described as the small biased voltage. All of the high frequency components can be filtered by the R-C network which is placed in the input position of the instrumentation amplifier, as shown in Figure 6. The following equation shows the equation of filtering frequency for the differential and common mode part of the input signal.

$$\text{FilterFreq}_{\text{DIFF}} = \frac{1}{2\pi R(2C_D + C_C)}$$

$$\text{FilterFreq}_{\text{CM}} = \frac{1}{2\pi RC_C}$$

$C_D \geq 10C_C$  is required in the above equation.

The capacitor  $C_D$  influences the quality of the differential signal, while  $C_C$  influences the quality of the common mode signal. The common mode rejection ratio would be reduced if the  $R \times C_C$  is mismatched. To reduce this negative influence and obtain a good CMRR, it is recommended that the capacitance of  $C_D$  should be 10 times larger than  $C_C$ . To conclude, the larger the ratio of  $C_D:C_C$  is, the less negative influence to the circuit.

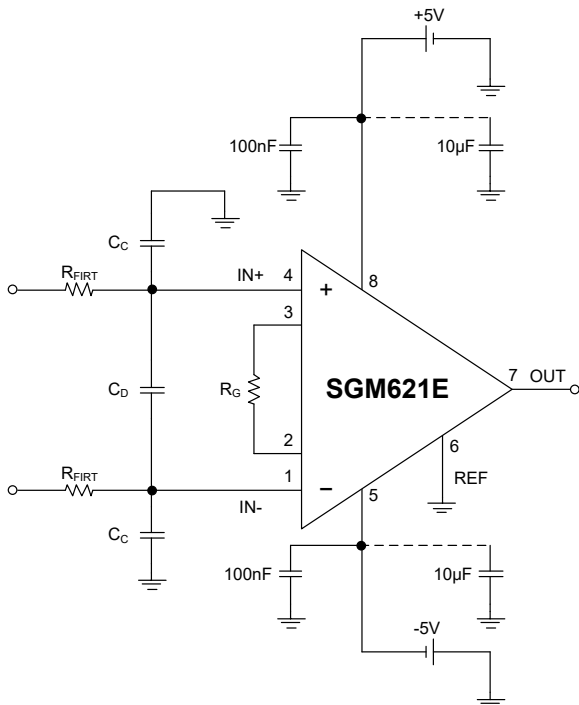


Figure 6. One Method to Reduce the Interference of RF

Common Mode Rejection

The common mode rejection ratio of the instrumentation amplifier is high as it can measure the differential signal between the two inputs when both IN+ and IN- increase or decrease equally. Also, this specification can be defined in the whole range of input voltage.

To obtain a best CMRR, it is recommended that the REF pin should be connected to a low impedance input and the difference of impedance between two inputs should be as small as possible. Also, using shielded cable can effectively reduce the noise of the circuit, and it should be driven properly for better value of CMRR. The following two figures (Figure 7 and Figure 8) illustrate the method to increase the CMRR for alternating circuit by bootstrapping the capacitance of the shielded cable, and this kind of method can also reduce the mismatching of capacitance at the inputs.

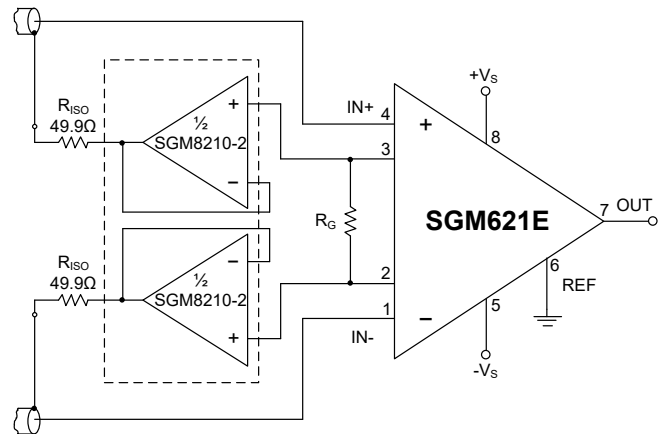


Figure 7. Differential Input Shield Driving

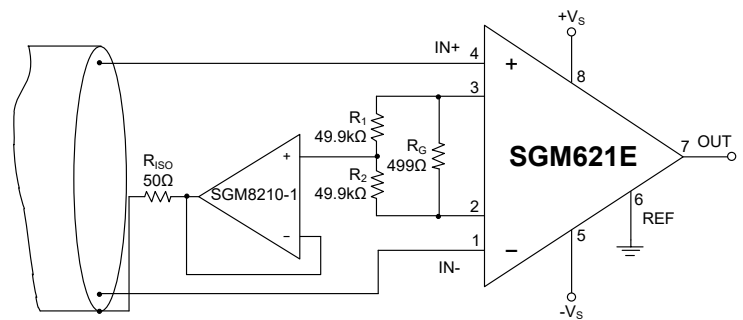


Figure 8. Common Mode Input Shield Driving

APPLICATION INFORMATION (continued)

Isolation of Grounding

For solving the problems of grounding, REF pin should be connected to the "local ground" as the output of the instrumentation amplifier is biased with  $V_{REF}$ .

Because of the noisy environment of the digital circuit, the component of data-acquisition such as Analog Digital Converter (ADC) has two pins which are AGND

and DGND. Also, the isolation can be made by using a single line or 0Ω resistor. However, each returns of ground should be separated so that the current flow from the sensitive point could be minimized. Also, the ground returns between analog and digital should be tied together with one point, which is shown in ADC part of Figure 9.

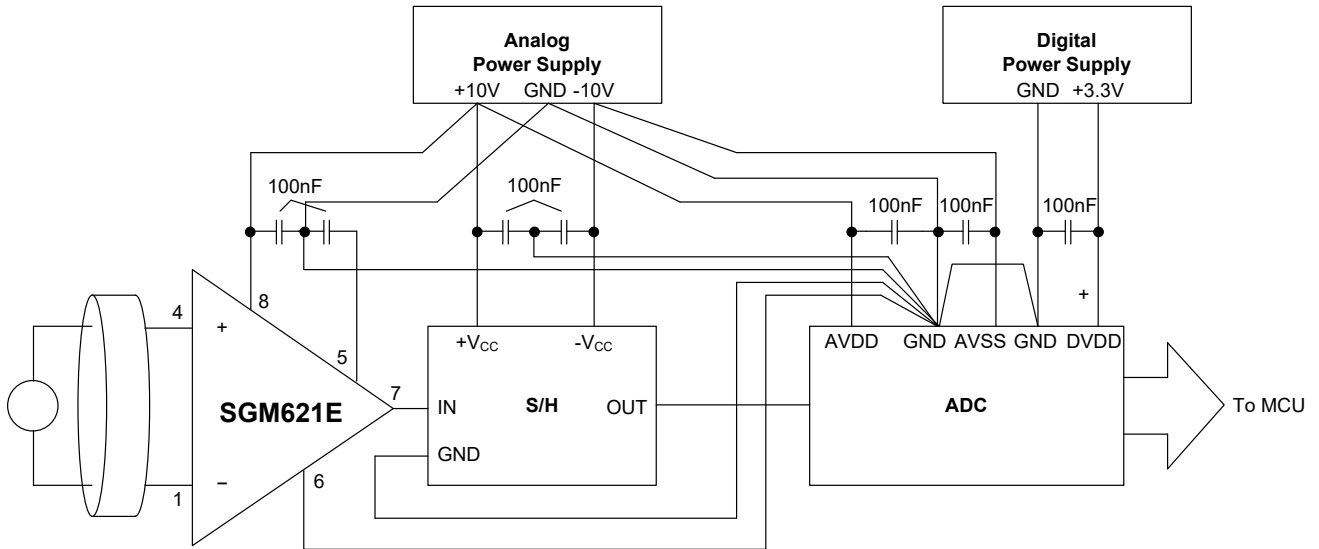


Figure 9. Isolation of Grounding

## SGM621E

### APPLICATION INFORMATION (continued)

#### Return of Grounding for $I_B$

The bias current ( $I_B$ ) at the inputs is needed for operating and biasing the transistor at the input stage of the instrumentation amplifier, so it is also necessary to design a ground return path for the bias current. For example, for operating the floating inputs of the amplifier (see Figure 10 ~ 12), such as AC-coupled transformer, there should be an electrical line between the input and the ground for ground return of bias current.

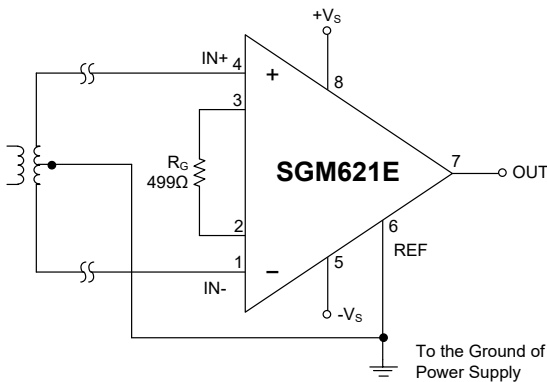


Figure 10. Return of Grounding for  $I_B$  with Transformer-Coupled Inputs

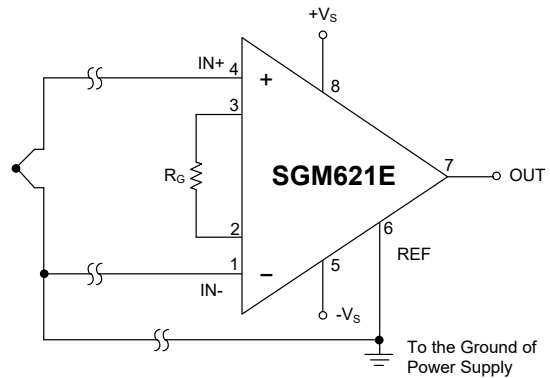


Figure 11. Return of Grounding for  $I_B$  with Thermocouple Inputs

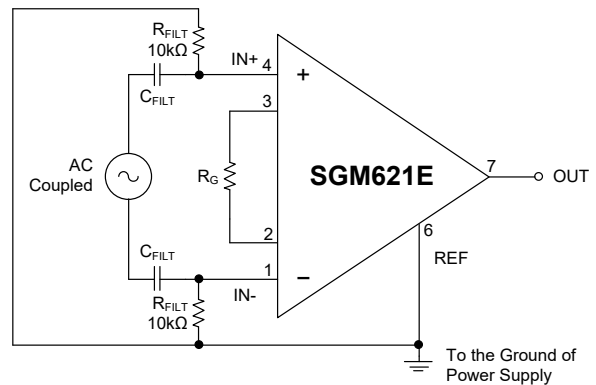


Figure 12. Return of Grounding for  $I_B$  with AC-Coupled Input

**REVISION HISTORY**

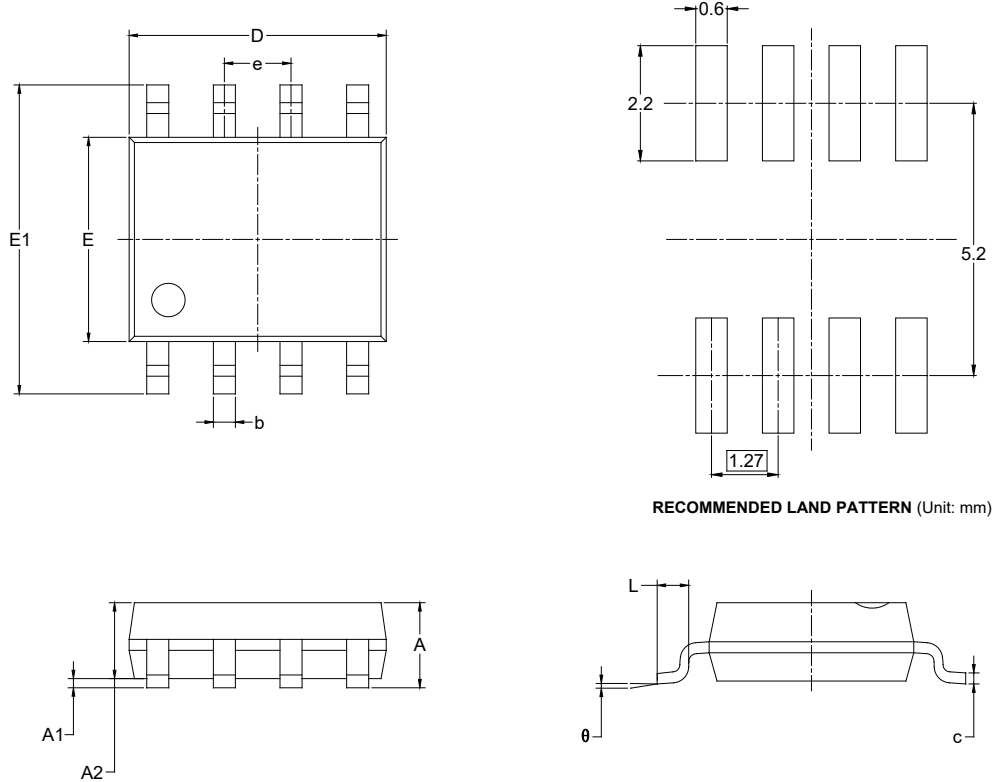
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

<b>Changes from Original to REV.A (APRIL 2026)</b>	<b>Page</b>
Changed from product preview to production data.....	All

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PACKAGE OUTLINE DIMENSIONS

SOIC-8



RECOMMENDED LAND PATTERN (Unit: mm)

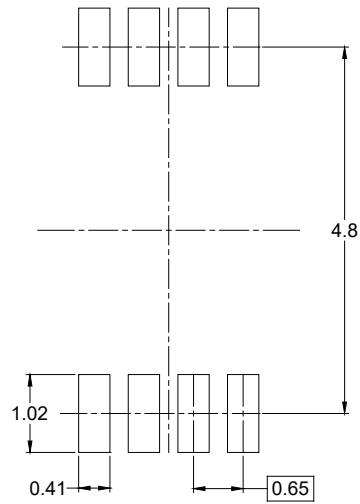
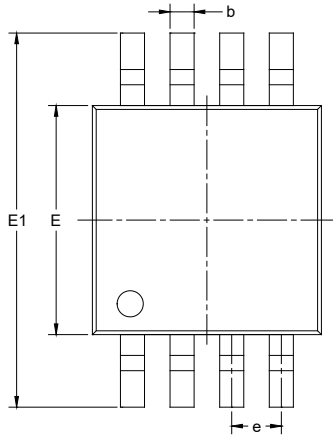
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.27 BSC		0.050 BSC	
L	0.400	1.270	0.016	0.050
$\theta$	0°	8°	0°	8°

NOTES:

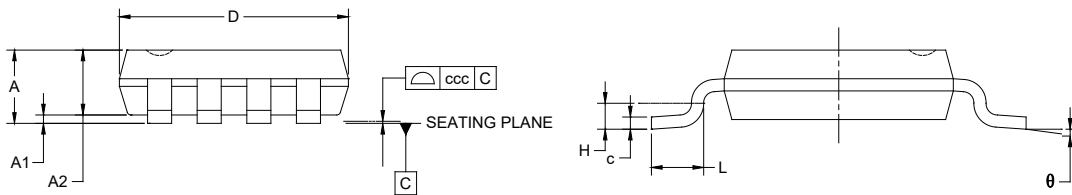
1. This drawing is subject to change without notice.
2. The dimensions do not include mold flashes, protrusions or gate burrs.
3. Reference JEDEC MS-012.

PACKAGE OUTLINE DIMENSIONS

MSOP-8



RECOMMENDED LAND PATTERN (Unit: mm)



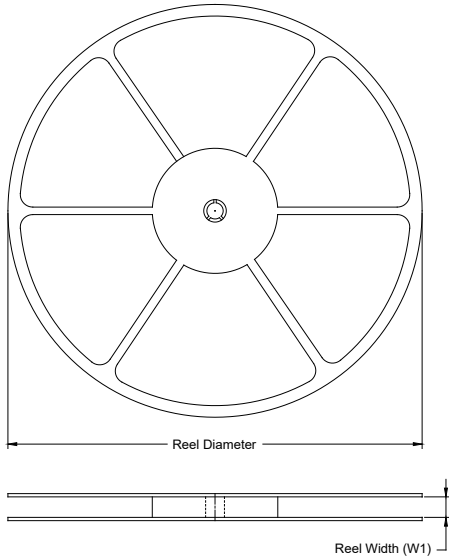
Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	-	-	1.100
A1	0.000	-	0.150
A2	0.750	-	0.950
b	0.220	-	0.380
c	0.080	-	0.230
D	2.800	-	3.200
E	2.800	-	3.200
E1	4.650	-	5.150
e	0.650 BSC		
L	0.400	-	0.800
H	0.250 TYP		
θ	0°	-	8°
ccc	0.100		

NOTES:

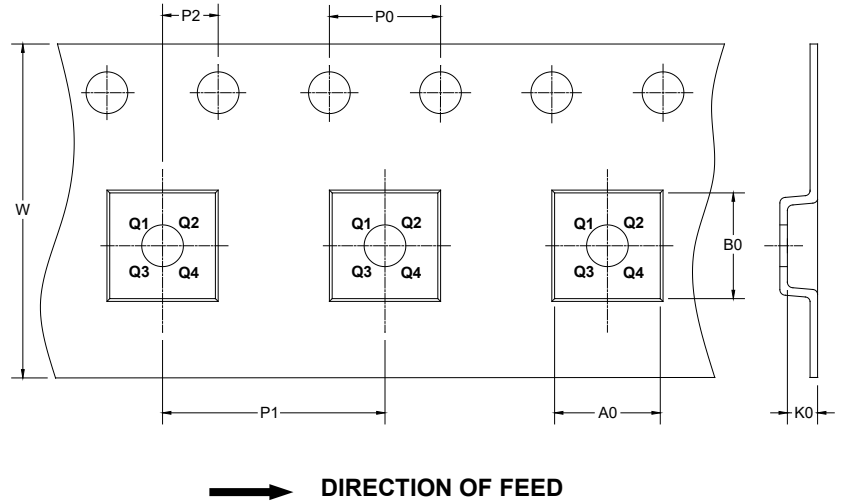
1. This drawing is subject to change without notice.
2. The dimensions do not include mold flashes, protrusions or gate burrs.
3. Reference JEDEC MO-187.

**TAPE AND REEL INFORMATION**

**REEL DIMENSIONS**



**TAPE DIMENSIONS**



NOTE: The picture is only for reference. Please make the object as the standard.

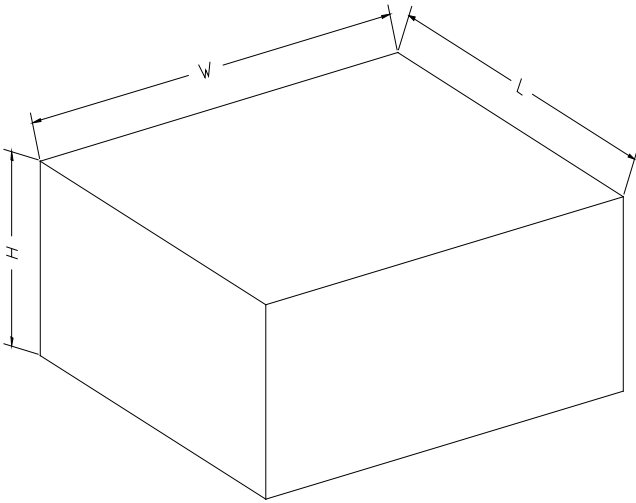
**KEY PARAMETER LIST OF TAPE AND REEL**

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
SOIC-8	13"	12.4	6.40	5.40	2.10	4.0	8.0	2.0	12.0	Q1
MSOP-8	13"	12.4	5.20	3.30	1.50	4.0	8.0	2.0	12.0	Q1

DD0001

# PACKAGE INFORMATION

## CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

## KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13"	386	280	370	5

DD0002