SGM41603A
I²C Controlled 10A Bidirectional Switched-Capacitor Converter

GENERAL DESCRIPTION

The SGM41603A is an efficient 2:1/1:2 bidirectional switched-capacitor converter with integrated power switches. It can deliver 10A in forward direction (2:1 voltage divider) and 5A in the reverse direction (1:2 voltage doubler). This device allows using a 2S Li+ power source as a 1S Li+ solution by inserting it between the 2S battery pack and 1S load input and save the existing 1S power architecture that is powered from the same battery. It can also function as a voltage doubler when V1X is connected to a 1S power supply.

This 2-channel high switching frequency (MAX 1.5MHz) and inductor-less topology allows low profile design with small footprint. The high switching frequency also reduces the size and quantity of the required capacitors. Safe operation is assured by over-voltage, under-voltage, over-current and thermal protections. Interference is also minimized by the built-in frequency dithering option. This device can achieve 99.3% efficiency which is among the highest in its class. Thermal management of such a low loss device is simple that makes it an ideal choice for industrial, consumer, and medical applications.

The I²C interface allows flexible parameter settings including OCP, OVLO, switching frequency thresholds and soft-start currents and durations. The SGM41603A is available in a tiny WLCSP-2.85×2.59-42B-A package.

APPLICATIONS

Smartphones, Tablets, Ultrabooks,
Chromebooks, DSLR and Mirrorless Cameras,
Power Banks, 2S Li+ Battery Applications,
Smartphone Direct Charging, Portable Printers,
Portable Gaming Devices, Two-Way Radios

FEATURES

- **Bidirectional Switched Capacitor Converter**
  - **Forward Direction 2:1 Conversion, Reverse Direction 1:2 Conversion**
  - **2-Channel Interleaved Operation (90° or 180°)**
  - **8 Integrated N-Type MOSFET Switches**
  - **10A Output Current Capability**
  - **99.3% Peak Efficiency**
- **Low I_Q Current: 50μA Forward Operating**
- **I²C Interface with Interrupt Signaling**
- **Adjustable Soft-Start Current and Timeout**
- **0.25MHz to 1.5MHz Adjustable Switching Frequency**
- **Low EMI with Switching Frequency Dithering**
- **Enable Input**
- **Out-of-Audio Option at Light Load**
- **Power Good Output**
- **Programmable V1X & V2X Over-Voltage Lockout**
- **Separate OCP Adjustment for Each Direction**
- **Thermal Alarm and Protection**
- **Available in a Green WLCSP-2.85×2.59-42B-A Package**

TYPICAL APPLICATION

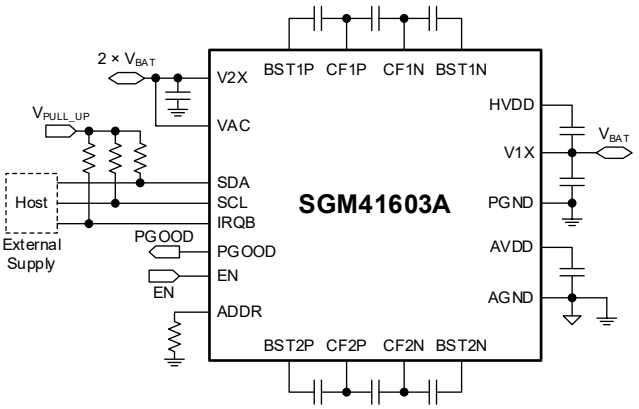


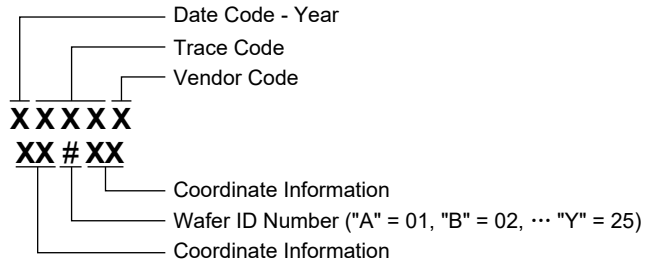
Figure 1. Typical Application Circuit

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM41603A	WLCSP-2.85×2.59-42B-A	-40℃ to +85℃	SGM41603AYG/TR	1EZ XXXXX XX#XX	Tape and Reel, 5000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code. XX#XX = Coordinate Information and Wafer ID Number.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

VAC to PGND ..... -0.3V to 28V
V2X to PGND ..... -0.3V to 16V
BSTxP to PGND ..... -0.3V to 16V
BSTxN to PGND ..... -0.3V to 8V
BSTxP to CFxP ..... -0.3V to 6V
BSTxN to CFxN ..... -0.3V to 6V
CFxP to PGND ..... -0.3V to (V_{V1X} + 6V)
CFxN to PGND ..... -0.3V to 6V
V1X to PGND ..... -0.3V to 6V
PGND to AGND ..... -0.3V to 0.3V
HVDD to AGND ..... -0.3V to (V_{V1X} + 6V)
AVDD to AGND ..... -0.3V to 6V
EN, ADDR to AGND ..... -0.3V to 16V
IRQB to AGND ..... -0.3V to 6V
SCL, SDA to AGND ..... -0.3V to 6V
PGOOD to AGND ..... -0.3V to 2.0V
V1X Continuous RMS Current (Forward Mode) 10A
V2X Continuous RMS Current (Reverse Mode) 5A
Package Thermal Resistance
WLCSP-2.85×2.59-42B-A, θ_{JA} ..... 38.7℃/W
WLCSP-2.85×2.59-42B-A, θ_{JB} ..... 6.3℃/W
WLCSP-2.85×2.59-42B-A, θ_{JC} ..... 14.6℃/W
Junction Temperature ..... +155℃
Storage Temperature Range ..... -65℃ to +155℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility (1) (2)
HBM ..... ±2000V
CDM ..... ±1000V

NOTES:

1. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.

2. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

RECOMMENDED OPERATING CONDITIONS

VAC ..... 22V (MAX)
V2X (Forward Mode) (3) ..... 4.1V to 11V
V1X (Reverse Mode) (4) ..... 2.7V to 5.5V
I_{V1X} (Forward Mode, Continuous) ..... 0A to 10A
I_{V2X} (Reverse Mode, Continuous) ..... 0A to 5A
(BST1P - CF1P), (BST1N - CF1N) ..... 0V to 5V
(CF1P - V1X), CF1N ..... 0V to 5.5V
(BST2P - CF2P), (BST2N - CF2N) ..... 0V to 5V
(CF2P - V1X), CF2N ..... 0V to 5.5V
AVDD, (HVDD - V1X) ..... 0V to 5V
EN ..... 0V to 12V
PGOOD ..... 0V to 1.8V
SDA, SCL, IRQB ..... 0V to 5V
Junction Temperature Range ..... -40℃ to +125℃

NOTES:

3. The V2X voltage must be higher than $V2X_{SW\_R}$ for switching, and the SGM41603A can switch down to 4.1V V2X voltage after starting switching.

4. The V1X voltage must be higher than $V1X_{SW\_R}$ for switching, and the SGM41603A can switch down to 2.7V V1X voltage after starting switching.

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

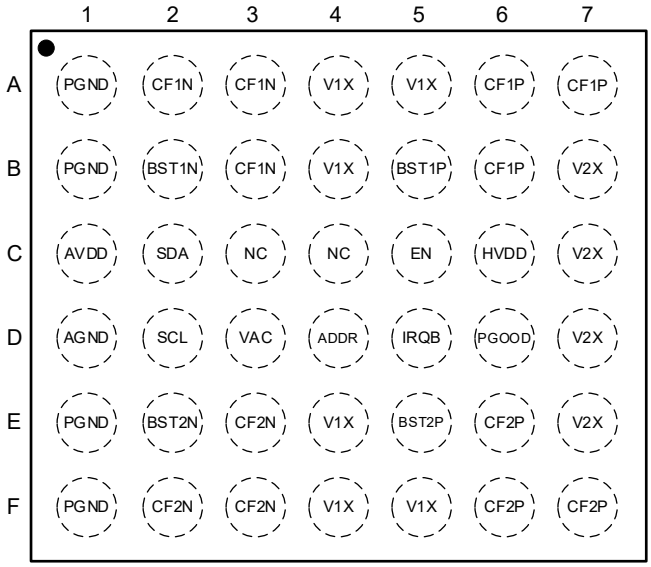
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

(TOP VIEW)



WLCSP-2.85×2.59-42B-A

PIN DESCRIPTION

PIN	NAME	TYPE (1)	FUNCTION
A1, B1, E1, F1	PGND	P	Power Ground.
A2, A3, B3	CF1N	P	Channel-1 Flying Capacitor Negative Node. Connect three parallel 22μF capacitors between CF1P and CF1N pins as close as possible to these pins.
A4, A5, B4, E4, F4, F5	V1X	P	Lower Voltage (1X) Power Port. It is an output in forward mode and an input in reverse mode. Two 10μF capacitors are recommended to be placed between V1X and PGND.
A6, A7, B6	CF1P	P	Channel-1 Flying Capacitor Positive Node. Connect three parallel 22μF capacitors between CF1P and CF1N pins as close as possible to these pins.
B2	BST1N	P	Bootstrap Capacitor Connection for Q_{CL1} Gate Driver Supply. Place a 47nF or larger ceramic capacitor between this pin and CF1N.
B5	BST1P	P	Bootstrap Capacitor Connection for Q_{CH1} Gate Driver Supply. Place a 47nF or larger ceramic capacitor between this pin and CF1P.
B7, C7, D7, E7	V2X	P	Higher Voltage (2X) Power Port. It is an input in forward mode and an output in reverse mode. Two 10μF capacitors are recommended to be placed between V2X and PGND.
C1	AVDD	AO	5V LDO Output. Decouple AVDD to AGND with at least 1μF high quality ceramic capacitor (X5R or better). Do not connect any external load to AVDD.
C2	SDA	DIO	I²C Interface Data Line. The SDA line is forced to release when the I²C timeout fault occurs.
C3, C4	NC	N/A	No Connection. Leave these pins floating and do not connect them together.
C5	EN	DI	Active High Device Enable Input.
C6	HVDD	AO	(V_{1X} + 5V) LDO Output. Decouple HVDD to V1X with at least 1μF high quality ceramic capacitor (X5R or better). Do not connect any external load to HVDD.
D1	AGND	P	Analog Ground.
D2	SCL	DI	I²C Interface Clock Line. The device I²C controller block is forced to reset when receiving 9 clock pulses on the SCL line.
D3	VAC	P	Power Supply for Internal Circuit and Fast Startup Enable Input in Forward Direction. When a voltage higher than $V_{VAC\_PRESENT\_R}$ is applied to this pin, the soft-discharge time (t_{SFT_DISCHG}) before forward-direction soft start will be skipped to shorten the startup period. If used in forward direction, it is recommended to connect this pin to V2X. If the function is not used or the chip is applied in reverse direction, short this pin to GND.
D4	ADDR	AIO	I²C Slave Address Setting Pin. This pin is used to assign the I²C address of the device during POR period. Place a 10kΩ or smaller resistor from ADDR to ground to set the I²C slave address to 0x69; Keep this pin floating can set the slave address to 0x68.
D5	IRQB	DO	Open-Drain Active Low Interrupt Output. A low on IRQB indicates a fault condition. The external pull-up resistor should be greater than 1kΩ.
D6	PGOOD	DO	Power Good Output.
E2	BST2N	P	Bootstrap Capacitor Connection for Q_{CL2} Gate Driver Supply. Place a 47nF or larger ceramic capacitor between this pin and CF2N.
E3, F2, F3	CF2N	P	Channel-2 Flying Capacitor Negative Node. Connect three parallel 22μF capacitors between CF2P and CF2N pins as close as possible to these pins.
E5	BST2P	P	Bootstrap Capacitor Connection for Q_{CH2} Gate Driver Supply. Place a 47nF or larger ceramic capacitor between this pin and CF2P.
E6, F6, F7	CF2P	P	Channel-2 Flying Capacitor Positive Node. Connect three parallel 22μF capacitors between CF2P and CF2N pins as close as possible to these pins.

NOTE:
1. P = Power, AO = Analog Output, AIO = Analog Input/Output, DI = Digital Input, DO = Digital Output, DIO = Digital Input/Output.

ELECTRICAL CHARACTERISTICS

(V_{V2X} = 7.6V, V_{V1X} = 3.8V, f_{SW} = 0.5MHz, T_J = -40℃ to +85℃, typical values are at T_J = +25℃, unless otherwise specified.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Global Input Supply						
Shutdown Supply Current	I_{SHDN_V2X}	EN = low, SCC_EN = 0, V_{V2X} = 8.4V		11		μA
	I_{SHDN_V1X}	EN = low, SCC_EN = 0, V_{V1X} = 4.2V		11		
Quiescent Current	I_{Q_V2X}	V_{V2X} = 8.4V, automatic mode		50		μA
	$I_{Q\_V2X\_OOA}$	V_{V2X} = 8.4V, Out-of-Audio mode		760		
	I_{Q_V1X}	V_{V1X} = 4.2V, automatic mode		100		μA
	$I_{Q\_V1X\_OOA}$	V_{V1X} = 4.2V, Out-of-Audio mode		1550		
V1X Leakage Current	I_{LK_V1X}	V_{V2X} = 4.2V, V1X_AD_EN = 0, EN = low		0.1		μA
Input Under-Voltage Lockout						
Under-Voltage Lockout Threshold	$V2X_{UVLO\_R}$	V_{V2X} rising		3.20	3.55	V
	$V2X_{UVLO\_F}$	V_{V2X} falling		2.90		
	$V1X_{UVLO\_R}$	V_{V1X} rising		2.77	2.97	
	$V1X_{UVLO\_F}$	V_{V1X} falling		2.47		
	VX_{UVLO_HYS}	V1X, V2X UVLO hysteresis		0.3		
Enable Inputs and Logic						
EN Deglitch Time	t_{EN_DEG}	Deglitch between V_{EN} rising over V_{IH} and starting soft-start action, when t_{EN_DEG} = 0.125ms (I²C programmable from 0.125ms to 64ms, default 0.125ms)		0.125		ms
Logic Input Low Level	V_{IL}	EN pin			0.4	V
Logic Input High Level	V_{IH}	EN pin	1.1			V
EN Pull-Down Resistance	R_{EN_PD}	Pulled down to AGND		1.5		MΩ
EN Input Leakage Current	I_{LK_EN}	EN pin connected to 3.3V, RPUPD_EN = 0		0.1		μA
IRQB Pin Output High Leakage	I_{LK_IRQB}	IRQB pin, V_{IRQB} = 5.5V		0.1		μA
Switched-Capacitor Converter						
Thresholds for Switching	$V2X_{SW\_R}$	Rising, when $V2X_{SW\_F}$ = 3.8V		4.0		V
	$V2X_{SW\_F}$	Falling, when $V2X_{SW\_F}$ = 3.8V (I²C programmable from 3.8V to 4.4V, 0.2V per step, default 3.8V)		3.8		
	$V1X_{SW\_R}$	Rising, when $V1X_{SW\_F}$ = 2.6V		2.8		
	$V1X_{SW\_F}$	Falling, when $V1X_{SW\_F}$ = 2.6V (I²C programmable from 2.6V to 2.7V, 0.1V per step, default 2.6V)		2.6		
	VX_{SW_HYS}	V1X, V2X switching threshold hysteresis		0.2		
Switching Stop Deglitch Time	$t_{SW\_F\_DEG}$	Deglitch time between the time of V_{V1X} or V_{V2X} falling below its switching threshold and stopping the switching action, when $t_{SW\_F\_DEG}$ = 108μs (I²C programmable from 0ms to 1ms, default 0ms)		108		μs
Input Operating Voltage Range	V_{V2X}		$V2X_{SW\_F}$		$V2X_{OVP\_R}$	V
	V_{V1X}		$V1X_{SW\_F}$		$V1X_{OVP\_R}$	
Forward Mode Soft-Start Current (all at V1X)	I_{SS_FWD}	V_{V1X} > 0.25V_{V2X} when I_{SS_FWD} = 145mA (I2C programmable from 145mA to 580mA, 145mA per step, default 145mA)		145		mA
Reverse Mode Soft-Start Current (all at V2X)	I_{SS_RVS}	V_{V2X} < $V2X_{VALID}$ when I_{SS_RVS} = 200mA (I²C programmable from 100mA to 250mA, default 100mA)		200		mA

ELECTRICAL CHARACTERISTICS (continued)

(V_{V2X} = 7.6V, V_{V1X} = 3.8V, f_{SW} = 0.5MHz, T_J = -40℃ to +85℃, typical values are at T_J = +25℃, unless otherwise specified.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Valid V2X Voltage During Soft-Start	$V2X_{VALID}$	V_{V2X} rising, threshold for reverse mode soft-start timeout		6		V
Light Load Efficiency	η_{LIGHT1_FWD}	I_{V1X} = 1mA, V_{V2X} = 7.4V		90.8		%
Light Load Efficiency	η_{LIGHT2_FWD}	I_{V1X} = 30mA, V_{V2X} = 7.4V		99.1		%
Light Load Efficiency	η_{LIGHT3_FWD}	I_{V1X} = 100mA, V_{V2X} = 7.4V		99.3		%
Light Load Efficiency	η_{LIGHT4_FWD}	I_{V1X} = 1A, V_{V2X} = 7.4V		99.1		%
Heavy Load Efficiency	η_{HEAVY_FWD}	I_{V1X} = 10A, V_{V2X} = 9V		96.4		%
Light Load Efficiency (Reverse)	η_{LIGHT1_RVS}	I_{V2X} = 1mA, V_{V1X} = 3.7V		94.3		%
Light Load Efficiency (Reverse)	η_{LIGHT2_RVS}	I_{V2X} = 0.1A, V_{V1X} = 3.7V		99.2		%
Light Load Efficiency (Reverse)	η_{LIGHT3_RVS}	I_{V2X} = 1A, V_{V1X} = 3.7V		98.8		%
Heavy Load Efficiency (Reverse)	η_{HEAVY_RVS}	I_{V2X} = 5A, V_{V1X} = 4.5V		96.3		%
R_{DSON} of Q_{CH1} and Q_{CH2}	R_{DS_QCH}	V_{V2X} = 7.6V, V_{V1X} = 3.8V, I_{V1X} = 0.5A		13		mΩ
R_{DSON} of Q_{DH1} and Q_{DH2}	R_{DS_QDH}	V_{V2X} = 7.6V, V_{V1X} = 3.8V, I_{V1X} = 0.5A		11		
R_{DSON} of Q_{CL1} and Q_{CL2}	R_{DS_QCL}	V_{V2X} = 7.6V, V_{V1X} = 3.8V, I_{V1X} = 0.5A		10		
R_{DSON} of Q_{DL1} and Q_{DL2}	R_{DS_QDL}	V_{V2X} = 7.6V, V_{V1X} = 3.8V, I_{V1X} = 0.5A		10		
Switching Frequency	f_{SW}	When f_{SW} = 500kHz (I^2C programmable from 250kHz to 1.5MHz, default 500kHz)	440	500	560	kHz
Switching Frequency Dither Rate	f_{SW_DTHR}	When f_{SW_DTHR} = 3% (I^2C programmable from 3% to 12% or OFF, default OFF)		±3		%
Active Discharge Resistance	R_{AD_V2X}	Active discharge is enabled, SCC is disabled		10		kΩ
	R_{AD_V1X}			1		
Protections						
Over-Voltage Protection Threshold	$V2X_{OVP\_R}$	Rising, when $V2X_{OVP\_R}$ = 8.7V (I^2C programmable from 8.3V to 11V, default 10.5V)	8.48	8.7	8.92	V
	$V2X_{OVP\_HYS}$	V2X OVP Hysteresis		0.2		
	$V1X_{OVP\_R}$	Rising, when $V1X_{OVP\_R}$ = 4.35V (I^2C programmable from 4.15V to 5.5V, default 5.3V)	4.3	4.35	4.4	
	$V1X_{OVP\_HYS}$	V1X OVP Hysteresis		0.1		
V1X OCP1 Threshold (Bidirectional)	I_{V1X_OCP1}	When I_{V1X_OCP1} = 16.5A (I^2C programmable from 13.2A to 20.9A, default 16.5A)		16.5		A
V1X OCP1 Accuracy	$I_{V1X\_OCP1\_ACC}$	In the entire I_{V1X_OCP1} range, T_J = +25℃	-12		12	%
OCP2 Offset	$V1X_{OCP2}$	When $V1X_{OCP2}$ = 340mV (I^2C programmable from 100mV to 660mV, default 340mV)		340		mV
	$V2X_{OCP2}$	When $V2X_{OCP2}$ = 580mV (I^2C programmable from 300mV to 860mV, 40mV per step, default 580mV)		580		
Thermal Alarms and Shutdown						
Thermal Alarm at +100℃	$T_{DIE\_ALM\_100}$	T_J rising, +15℃ hysteresis		100		℃
Thermal Alarm at +120℃	$T_{DIE\_ALM\_120}$	T_J rising, +15℃ hysteresis		120		℃
Thermal Shutdown Rising Threshold	$T_{DIE\_OTP\_R}$			155		℃
Thermal Shutdown Rising Threshold Hysteresis	$T_{DIE\_OTP\_HYS}$			15		℃

ELECTRICAL CHARACTERISTICS (continued)

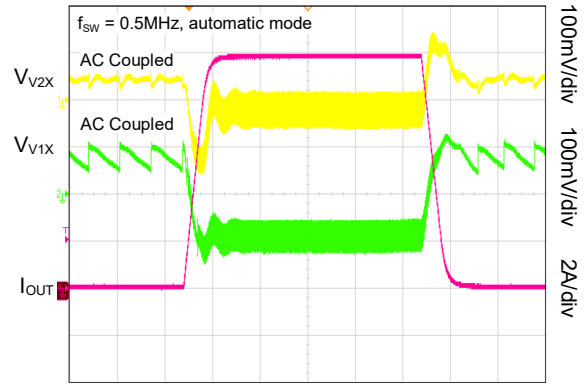
(V_{V2X} = 7.6V, V_{V1X} = 3.8V, f_{SW} = 0.5MHz, T_J = -40℃ to +85℃, typical values are at T_J = +25℃, unless otherwise specified.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SDA and SCL I/O Stage						
Input Logic Low Level	V_{IL_I2C}				0.36	V
Input Logic High Level	V_{IH_I2C}		0.92			V
SCL, SDA Logic Input Leakage Current	I_{IN_LK}	V_{SCL} = V_{SDA} = 1.8V	-1		1	μA
SCL, SDA Input Capacitance	C_{IN_I2C}			10		pF
Output Low Voltage (SDA only)	V_{OL_SDA}	Sinking 5mA			0.4	V
I²C Compatible Interface Timing for Standard, Fast, and Fast-Mode Plus Speeds						
Clock Frequency	f_{SCL}				1000	kHz
Hold Time (Repeated) START Condition	$t_{HD;STA}$		0.26			μs
CLK Low Period	t_{LOW}		0.5			μs
CLK High Period	t_{HIGH}		0.26			μs
Setup Time Repeated START Condition	$t_{SU;STA}$		0.26			μs
DATA Hold Time	$t_{HD:DAT}$		0			μs
DATA Valid Time	$t_{VD:DAT}$				0.45	μs
DATA Valid Acknowledge Time	$t_{VD:ACK}$				0.45	μs
DATA Setup time	$t_{SU;DAT}$		50			ns
Setup Time for STOP Condition	$t_{SU;STO}$		0.26			μs
Bus-Free Time Between STOP and START	t_{BUF}		0.5			μs
Pulse Width of Spikes that Must be Suppressed by the Input Filter	t_{SP}			50		ns
VAC Threshold						
VAC Present	$V_{VAC\_PRESENT}$	Rising threshold		3.75		V
		Hysteresis		100		mV
VAC UVLO	V_{VAC_UVLO}	Rising threshold		3.20	3.55	V
		Hysteresis		300		mV

TYPICAL PERFORMANCE CHARACTERISTICS

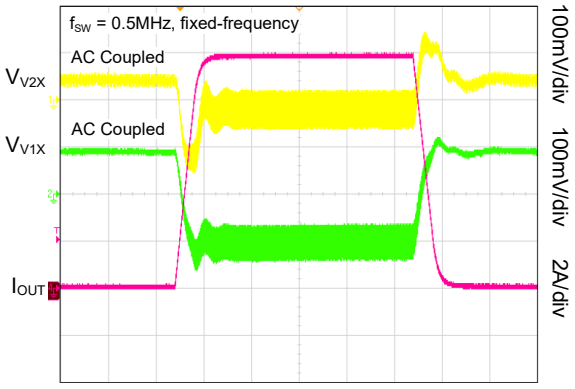
V_{V2X} = 7.6V, C_{FLY}/channel = 3 × 22μF, f_{SW} = 0.5MHz, unless otherwise specified.

10A Load Transient



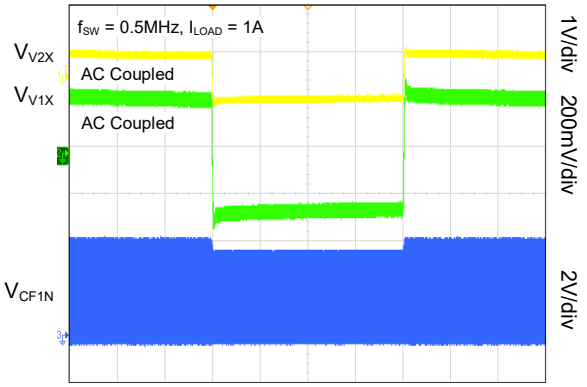
Time (100μs/div)

10A Load Transient



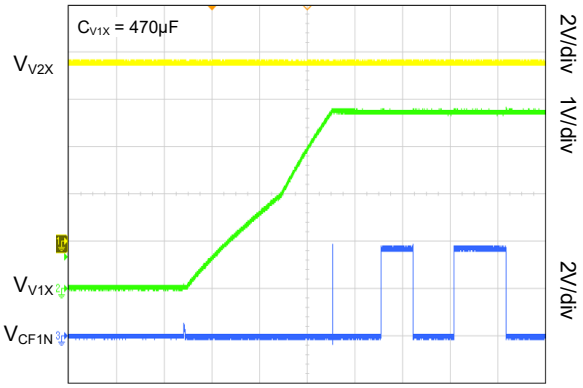
Time (100μs/div)

1V Line Transient



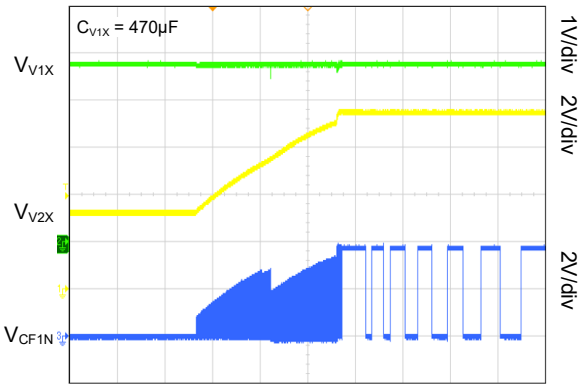
Time (2ms/div)

Soft-Start Waveform (Forward Mode)



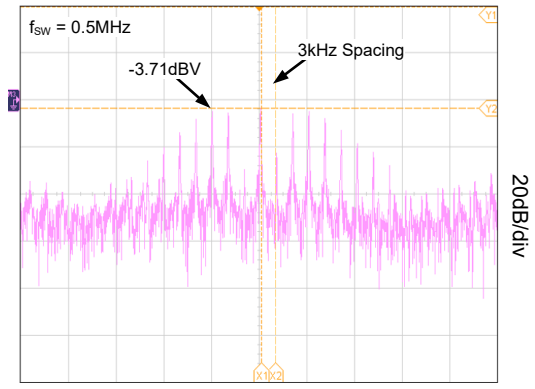
Time (5ms/div)

Soft-Start Waveform (Reverse Mode)



Time (5ms/div)

3% Dithering Frequency Spectrum

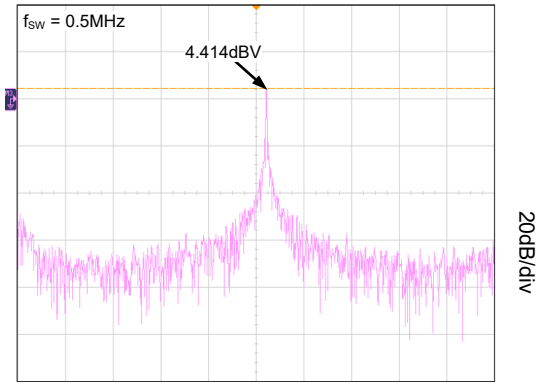


500kHz Center, 10kHz/div

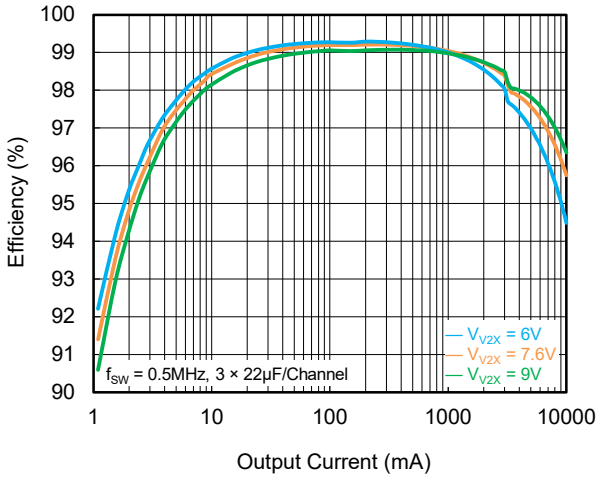
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

V_{V2X} = 7.6V, C_{FLY}/channel = 3 × 22μF, f_{SW} = 0.5MHz, unless otherwise specified.

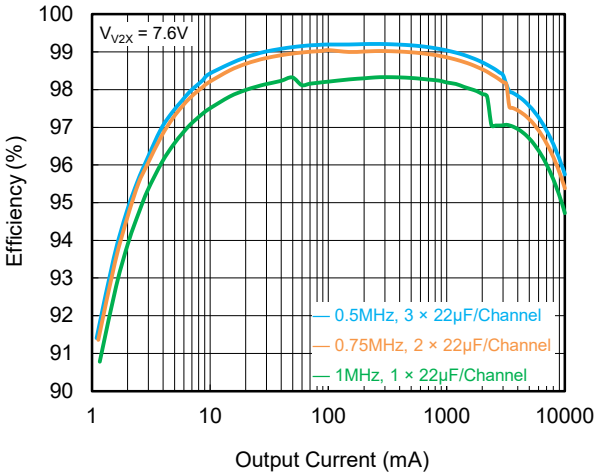
Dithering Disabled Frequency Spectrum



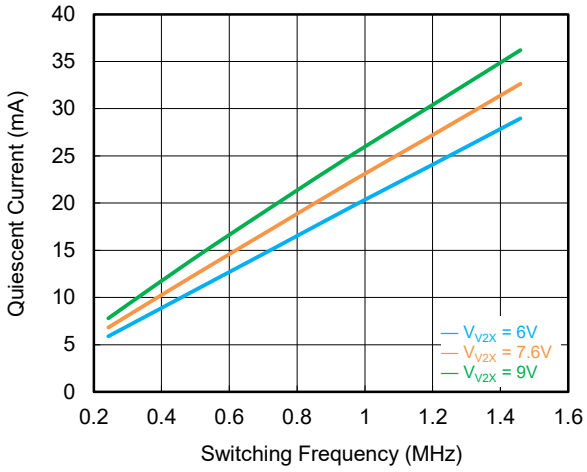
Automatic Mode Efficiency vs. Output Current



Automatic Mode Efficiency vs. Output Current



Fixed-Frequency Mode Quiescent Current vs. Switching Frequency



FUNCTIONAL BLOCK DIAGRAM

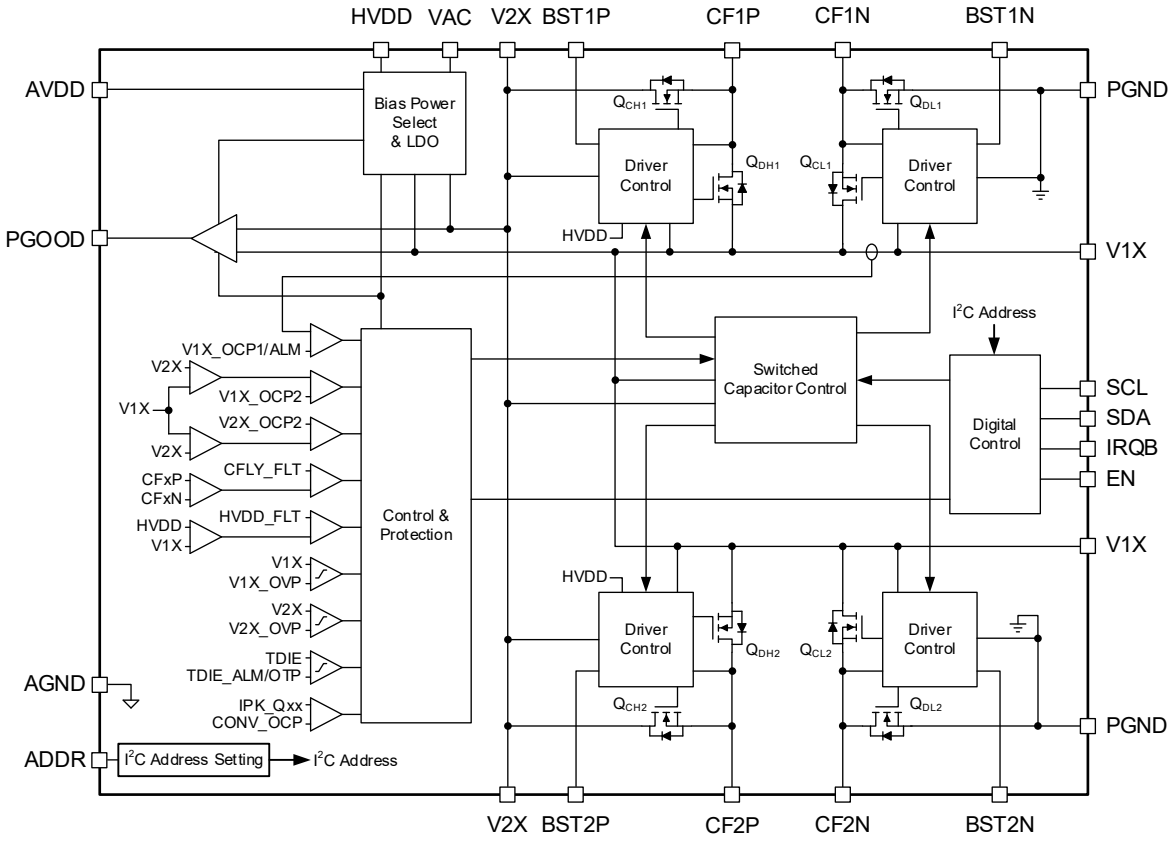


Figure 2. SGM41603A Block Diagram

I²C REGISTER ADDRESS MAP

All registers are 8-bit and individual bits are named from D[0] (LSB) to D[7] (MSB).

The device I²C Address is determined by the state of ADDR pin in the POR sequence, as described in I²C Slave Address Setting section.

FUNCTION	FLAG	MASK	STATUS	THRESHOLD SETTING	ENABLE	DEGLITCH
REG_RST	--	--	--	--	0x05[6]	--
WDT_TIMEOUT	0x12[3]	--	--	0x12[2:0]	0x12[2:0]	--
V2X_OVP	0x00[7]	0x01[7]	0x02[7]	0x08[7:3]	0x08[7:3]	--
V1X_OVP	0x00[6]	0x01[6]	0x02[6]	0x09[4:0]	0x09[4:0]	--
V1X_OC_ALM	0x00[5]	0x01[5]	0x02[5]	0x0A[7]	--	--
V1X_OCP	0x00[4]	0x01[4]	--	V1X_OCP1: 0x0A[2:0] V1X_OCP2: 0x0B[3:0]	V1X_OCP1: 0x07[7] V1X_OCP2: 0x0B[3:0]	V1X_OCP1: 0x0A[4:3] V1X_OCP2: 0x0C[7:6]
T_ALM1	0x00[3]	0x01[3]	0x02[3]	--	--	--
T_ALM2	0x00[2]	0x01[2]	0x02[2]	--	--	--
T_SHDN	0x00[1]	0x01[1]	0x02[1]	--	--	--
FSS_FLT	0x00[0]	0x01[0]	--	FWD_ISS: 0x0C[5:4] FWD_SS_TMO: 0x0C[2:0]	--	--
CONV_OCP_INT	0x03[3]	0x04[3]	--	--	--	--
V2X_VALID_INT	0x03[7]	0x04[7]	0x02[0]	--	--	--
CFLY_FLT	0x03[6]	0x04[6]	--	--	--	--
HVDD_FLT	0x03[5]	0x04[5]	--	--	--	--
SW_DIR_INT	0x03[4]	0x04[4]	0x02[4]	--	--	--
V2X_OCP	0x03[1]	0x04[1]	--	V2X_OCP2: 0x0B[7:4]	V2X_OCP2: 0x0B[7:4]	--
RSS_FLT	0x03[2]	0x04[2]	--	RVS_ISS: 0x0D[4:3] RVS_SS_TMO: 0x0D[2:1]	--	--
PWRON_INT	0x03[0]	--	--	--	--	--
RPUPD_EN	--	--	--	--	0x05[7]	--
EN_DEG	--	--	--	--	--	0x05[3:1]
SCC_EN	--	--	--	--	0x05[0]	--
PGOOD_DELAY	--	--	--	0x06[7]	--	--
SFT_DISCHG_T	--	--	--	0x06[5:4]	--	--
OOA_EN	--	--	--	--	0x06[3]	--
V2X_AD_EN	--	--	--	--	0x06[2]	--
V1X_AD_EN	--	--	--	--	0x06[1]	--
V2X_PDN_EN	--	--	--	--	0x0A[5]	--
V1X_PDN_EN	--	--	--	--	0x0A[6]	--
FIX_FREQ	--	--	--	--	0x06[0]	--
DTHR	--	--	--	0x07[5:4]	0x07[5:4]	--
FREQ	--	--	--	0x07[2:0]	--	--
V2X_SW_F	--	--	--	0x08[1:0]	--	0x09[6:5]
V1X_SW_F	--	--	--	0x09[7]	--	0x09[6:5]
DEEP_SKIP	--	--	--	0x0E[5:4]	--	--
RESTART_EN	--	--	--	--	0x0E[3]	--
WAIT_T	--	--	--	0x0E[1:0]	--	--
F2S_DROP	--	--	--	F2S_DROP: 0x0F[7:6] F2S_FWD_OFFSET: 0x15[2]	--	--
S2F_DROP	--	--	--	0x0F[5:4]	--	--
SAG_FWD	--	--	--	0x0F[3:2]	--	--
LO_V2X_SW	--	--	0x10[7]	--	--	--
OTP_VER	--	--	--	0x13[7:4]	--	--
CHIP_VER	--	--	--	0x13[3:0]	--	--
DEVICE_ID	--	--	--	0x14[7:0] (0x09)	--	--

REGISTER AND DATA

REG0x00: INT_SRC Register [reset = 0x00]

BITS	BIT NAME	RESET	TYPE	DESCRIPTION	RESET BY
D[7]	V2X_OVP_INT	0	RC	V2X_OVP Fault Flag Bit 0 = No V2X_OVP fault (default) 1 = V2X_OVP fault has occurred, or the V2X_OVP status bit is reset from '1' to '0' when the fault is cleared. Generates an interrupt on IRQB pin if unmasked. Read this bit to reset it to 0.	N/A
D[6]	V1X_OVP_INT	0	RC	V1X_OVP Fault Flag Bit 0 = No V1X_OVP fault (default) 1 = V1X_OVP fault has occurred, or the V1X_OVP status bit is reset from '1' to '0' when the fault is cleared. Generates an interrupt on IRQB pin if unmasked. Read this bit to reset it to 0.	N/A
D[5]	V1X_OC_ALM_INT	0	RC	V1X Over-Current Alarm Flag Bit (including forward mode and reverse mode) 0 = No V1X over-current alarm (default) 1 = V1X over-current alarm has occurred, or the V1X_OCP_ALM status bit has been reset from '1' to '0' when the alarm is cleared. Generates an interrupt on IRQB pin if unmasked. Read this bit to reset it to 0.	N/A
D[4]	V1X_OCP_INT	0	RC	V1X Over-Current Fault Flag Bit (including V1X_OCP1 and V1X_OCP2) 0 = No V1X over-current fault (default) 1 = V1X over-current fault has occurred. Generates an interrupt on IRQB pin if unmasked. Read this bit to reset it to 0.	N/A
D[3]	T_ALM1_INT	0	RC	T_{DIE} Over 100℃ Alarm Flag Bit 0 = No T_{DIE} over 100℃ alarm (default) 1 = T_{DIE} over 100℃ alarm has occurred, or the T_ALM1 status bit is reset from '1' to '0' when the alarm is cleared. Generates an interrupt on IRQB pin if unmasked. Read this bit to reset it to 0.	N/A
D[2]	T_ALM2_INT	0	RC	T_{DIE} Over 120℃ Alarm Flag Bit 0 = No T_{DIE} over 120℃ alarm (default) 1 = T_{DIE} over 120℃ alarm has occurred, or the T_ALM2 status bit is reset from '1' to '0' when the alarm is cleared. Generates an interrupt on IRQB pin if unmasked. Read this bit to reset it to 0.	N/A
D[1]	T_SHDN_INT	0	RC	T_{DIE} Thermal Shutdown Fault Flag Bit 0 = No T_{DIE} thermal shutdown fault (default) 1 = T_{DIE} thermal shutdown fault has occurred, or the T_SHDN status bit is reset from '1' to '0' when the fault is cleared. Generates an interrupt on IRQB pin if unmasked. Read this bit to reset it to 0.	N/A
D[0]	FSS_FLT_INT	0	RC	Forward Mode Soft-Start Fault Flag Bit 0 = No soft-start fault (default) 1 = Forward mode soft-start fault has occurred. Generates an interrupt on IRQB pin if unmasked. Read this bit to reset it to 0.	N/A

REGISTER AND DATA (continued)

REG0x01: INT_SRC_M Register [reset = 0x00]

BITS	BIT NAME	RESET	TYPE	DESCRIPTION	RESET BY
D[7]	V2X_OVP_M	0	R/W	Mask Bit for the V2X_OVP Fault Interrupt 0 = V2X_OVP fault interrupt can work (default) 1 = Mask V2X_OVP fault interrupt. V2X_OVP_INT bit sets after the fault occurs or is cleared, but no interrupt signal is sent on IRQB pin.	REG_RST or WDT
D[6]	V1X_OVP_M	0	R/W	Mask Bit for the V1X_OVP Fault Interrupt 0 = V1X_OVP fault interrupt can work (default) 1 = Mask V1X_OVP fault interrupt. V1X_OVP_INT bit sets after the fault occurs or is cleared, but no interrupt signal is sent on IRQB pin.	REG_RST or WDT
D[5]	V1X_OC_ALM_M	0	R/W	Mask Bit for the V1X Over-Current Alarm Interrupt 0 = V1X over-current alarm interrupt can work (default) 1 = Mask V1X over-current alarm interrupt. V1X_OC_ALM_INT bit sets after the alarm occurs or is cleared, but no interrupt signal is sent on IRQB pin.	REG_RST or WDT
D[4]	V1X_OCP_M	0	R/W	Mask Bit for the V1X Over-Current Fault Interrupt 0 = V1X over-current fault interrupt can work (default) 1 = Mask V1X over-current fault interrupt. V1X_OCP_INT bit sets after the fault, but no interrupt signal is sent on IRQB pin.	REG_RST or WDT
D[3]	T_ALM1_M	0	R/W	Mask Bit for the T_{DIE} Over 100℃ Alarm Interrupt 0 = T_{DIE} over 100℃ alarm interrupt can work (default) 1 = Mask T_{DIE} over 100℃ alarm interrupt. T_ALM1_INT bit sets after the alarm occurs or is cleared, but no interrupt signal is sent on IRQB pin.	REG_RST or WDT
D[2]	T_ALM2_M	0	R/W	Mask Bit for the T_{DIE} Over 120℃ Alarm Interrupt 0 = T_{DIE} over 120℃ alarm interrupt can work (default) 1 = Mask T_{DIE} over 120℃ alarm interrupt. T_ALM2_INT bit sets after the alarm occurs or is cleared, but no interrupt signal is sent on IRQB pin.	REG_RST or WDT
D[1]	T_SHDN_M	0	R/W	Mask Bit for the T_{DIE} Thermal Shutdown Fault Interrupt 0 = T_{DIE} thermal shutdown fault interrupt can work (default) 1 = Mask T_{DIE} thermal shutdown fault interrupt. T_SHDN_INT bit sets after the fault occurs or is cleared, but no interrupt signal is sent on IRQB pin.	REG_RST or WDT
D[0]	FSS_FLT_M	0	R/W	Mask Bit for the Forward Mode Soft-Start Fault Interrupt 0 = Soft-start fault interrupt can work (default) 1 = Mask forward mode soft-start fault interrupt. FSS_FLT_INT bit sets after the fault, but no interrupt signal is sent on IRQB pin.	REG_RST or WDT

REGISTER AND DATA (continued)

REG0x02: STATUS Register [reset = 0x00]

BITS	BIT NAME	RESET	TYPE	DESCRIPTION	RESET BY
D[7]	V2X_OVP	0	R	V2X_OVP Fault Status Bit 0 = No V2X_OVP fault (default) 1 = Device is in V2X_OVP fault status.	N/A
D[6]	V1X_OVP	0	R	V1X_OVP Fault Status Bit 0 = No V1X_OVP fault (default) 1 = Device is in V1X_OVP fault status.	N/A
D[5]	V1X_OC_ALM	0	R	Bidirectional V1X Over-Current Alarm Status Bit 0 = No V1X over-current alarm (default) 1 = Device is in V1X over-current alarm status.	N/A
D[4]	SW_DIR	0	R	SCC Switching Direction Status Bits 0 = Forward direction (default) 1 = Reverse direction	N/A
D[3]	T_ALM1	0	R	T_{DIE} Over 100℃ Alarm Status Bit 0 = No T_{DIE} over 100℃ alarm (default) 1 = Device is in T_{DIE} over 100℃ alarm status.	N/A
D[2]	T_ALM2	0	R	T_{DIE} Over 120℃ Alarm Status Bit 0 = No T_{DIE} over 120℃ alarm (default) 1 = Device is in T_{DIE} over 120℃ alarm status.	N/A
D[1]	T_SHDN	0	R	T_{DIE} Thermal Shutdown Fault Status Bit 0 = No T_{DIE} thermal shutdown fault (default) 1 = Device is in T_{DIE} thermal shutdown fault status.	N/A
D[0]	V2X_VALID	0	R	V_{V2X} above $V2X_{VALID}$ Threshold Status Bit 0 = V_{V2X} < $V2X_{VALID}$ (default) 1 = V_{V2X} > $V2X_{VALID}$.	N/A

REGISTER AND DATA (continued)

REG0x03: INT_SRC2 Register [reset = 0x00]

BITS	BIT NAME	RESET	TYPE	DESCRIPTION	RESET BY
D[7]	V2X_VALID_INT	0	RC	V2X_VALID Status Change Event Flag Bits 0 = No V2X_VALID status change event (default) 1 = V2X_VALID status change event has occurred. When the V2X_VALID status bit has changed, generates an interrupt on IRQB pin if unmasked. Read this bit to reset it to 0.	N/A
D[6]	CFLY_FLT_INT	0	RC	C_{FLY} Charging Fault Flag Bit 0 = No C_{FLY} charging fault (default) 1 = C_{FLY} charging fault has occurred. Generates an interrupt on IRQB pin. Read this bit to reset it to 0.	N/A
D[5]	HVDD_FLT_INT	0	RC	HVDD Charging Fault Flag Bit 0 = No HVDD charging fault (default) 1 = HVDD charging fault has occurred. Generates an interrupt on IRQB pin. Read this bit to reset it to 0.	N/A
D[4]	SW_DIR_INT	0	RC	SCC Switching Direction Transition Event Flag Bit 0 = No SCC switching direction transition event (default) 1 = SCC switching direction transition event has occurred. When the SW_DIR status bit is changed, generates an interrupt on IRQB pin if unmasked. Read this bit to reset it to 0.	N/A
D[3]	CONV_OCP_INT	0	RC	SCC Real-Time Converting Over-Current Event Flag Bit 0 = No SCC converting over-current event (default) 1 = SCC converting over-current event has occurred. When the CONV_OCP_INT status bit has changed, it generates an interrupt on IRQB pin if unmasked. Read this bit to reset it to 0.	N/A
D[2]	RSS_FLT_INT	0	RC	Reverse Mode Soft-Start Fault Flag Bit 0 = No reverse mode soft-start fault (default) 1 = Reverse mode soft-start fault has occurred. Generates an interrupt on IRQB pin if unmasked. Read this bit to reset it to 0.	N/A
D[1]	V2X_OCP_INT	0	RC	V2X Over-Current Fault Flag Bit (including V1X_OCP1 during reverse mode and V2X_OCP2) 0 = No V2X over-current fault (default) 1 = V2X over-current fault has occurred. Generates an interrupt on IRQB pin if unmasked. Read this bit to reset it to 0.	N/A
D[0]	PWRON_INT	0	RC	Device Power-on Event Flag Bit (V1X or V2X rising above its UVLO threshold and the chip is enabled; 2. VAC rising above its present threshold) 0 = No device power-on event (default) 1 = Device power-on event has occurred. Generates an interrupt on IRQB pin. Read this bit to reset it to 0.	N/A

REGISTER AND DATA (continued)

REG0x04: INT_SRC2_M Register [reset = 0x00]

BITS	BIT NAME	RESET	TYPE	DESCRIPTION	RESET BY
D[7]	V2X_VALID_M	0	R/W	Mask Bit for the V2X_VALID Status Change Event Interrupt 0 = V2X_VALID status change event interrupt can work (default) 1 = Mask V2X_VALID status change event interrupt. V2X_VALID_INT bit sets after the event occurs, but no interrupt signal is sent on IRQB pin.	REG_RST or WDT
D[6]	CFLY_FLT_M	0	R/W	Mask Bit for the C_{FLY} Charging Fault Interrupt 0 = C_{FLY} charging fault interrupt can work (default) 1 = Mask C_{FLY} charging fault interrupt. CFLY_FLT_INT bit sets after the fault occurs, but no interrupt signal is sent on IRQB pin.	REG_RST or WDT
D[5]	HVDD_FLT_M	0	R/W	Mask Bit for the HVDD Charging Fault Interrupt 0 = HVDD charging fault interrupt can work (default) 1 = Mask HVDD charging fault interrupt. HVDD_FLT_INT bit sets after the fault occurs, but no interrupt signal is sent on IRQB pin.	REG_RST or WDT
D[4]	SW_DIR_M	0	R/W	Mask Bit for the SCC Switching Direction Transition Event Interrupt 0 = SCC switching direction transition event interrupt can work (default) 1 = Mask SCC switching direction transition event interrupt. SW_DIR_INT bit sets after the event occurs, but no interrupt signal is sent on IRQB pin.	REG_RST or WDT
D[3]	CONV_OCP_INT_M	0	R/W	Mask Bit for the SCC Converting Over-Current Event Interrupt 0 = SCC converting over-current event interrupt can work (default). 1 = Mask SCC converting over-current event interrupt. CONV_OCP_INT bit sets after the event occurs, but no interrupt signal is sent on IRQB pin.	REG_RST or WDT
D[2]	RSS_FLT_M	0	R/W	Mask Bit for the Reverse Mode Soft-Start Fault Interrupt 0 = Reverse Mode soft-start fault interrupt can work (default) 1 = Mask reverse mode soft-start fault interrupt. RSS_FLT_INT bit sets after the fault, but no interrupt signal is sent on IRQB pin.	REG_RST or WDT
D[1]	V2X_OCP_M	0	R/W	Mask Bit for the V2X Over-Current Fault Interrupt 0 = V2X over-current fault interrupt can work (default) 1 = Mask V2X over-current fault interrupt. V2X_OCP_INT bit sets after the fault, but no interrupt signal is sent on IRQB pin.	REG_RST or WDT
D[0]	Reserved	0	R	Reserved	N/A

REG0x05: EN_CFG0 Register [reset = 0x80]

BITS	BIT NAME	RESET	TYPE	DESCRIPTION	RESET BY
D[7]	RPUPD_EN	1	R/W	Enable Bit of EN Pin Input Pull-Down Resistor Activation 0 = Disabled 1 = Enabled (default)	REG_RST or WDT
D[6]	REG_RST	0	R/W	Reset all the registers (this bit returns to 0 when the reset action is done) 0 = No Registers Reset (default) 1 = Reset Registers	REG_RST or WDT
D[5:4]	Reserved	00	R	Reserved	N/A
D[3:1]	EN_DEG[2:0]	000	R/W	Setting Bits of EN Pin Input High Deglitch Time 000 = 0.125ms 001 ~ 111: t_{EN_DEG} = 2 ^ (EN_DEG[2:0] - 1) × 1ms Default: 0x0, t_{EN_DEG} = 0.125ms	REG_RST or WDT
D[0]	SCC_EN	0	R/W	Switched Capacitor Converter Enable Bit 0 = Disabled (default) 1 = Enabled. If an HVDD or C_{FLY} charging fault occurs or reverse mode soft-start timeout, device returns to standby mode and this bit is automatically reset to 0.	REG_RST or WDT

REGISTER AND DATA (continued)

REG0x06: SCC_CFG1 Register [reset = 0x16]

BITS	BIT NAME	RESET	TYPE	DESCRIPTION	RESET BY
D[7]	PGOOD_DELAY	0	R/W	PGOOD Output Delay Time Bit after V1X or V2X Soft Starts Successfully 0 = 100ms (default) 1 = No delay	REG_RST or WDT
D[6]	Reserved	0	R	Reserved	N/A
D[5:4]	SFT_DISCHG_T[1:0]	01	R/W	Soft-Discharge Time (t_{SFT_DISCHG}) Setting Bits 00 = 50ms 01 = 100ms (default) 10 = 200ms 11 = 300ms	REG_RST or WDT
D[3]	OOA_EN	0	R/W	Skip Out-of-Audio (OOA) Mode Enable Bit 0 = Out-of-audio mode is disabled when converter is in Skip mode (default) 1 = Out-of-audio mode is enabled when converter is in Skip mode, and the pulse skipping frequency is maintained above 30kHz	REG_RST or WDT
D[2]	V2X_AD_EN	1	R/W	V2X Active Discharge Enable Bit 0 = Disabled 1 = Enabled (default)	REG_RST or WDT
D[1]	V1X_AD_EN	1	R/W	V1X Active Discharge Enable Bit 0 = Disabled 1 = Enabled (default)	REG_RST or WDT
D[0]	FIX_FREQ	0	R/W	Fixed-Frequency Operation Mode Enable Bit 0 = Disabled (default) 1 = Enabled	REG_RST or WDT

REG0x07: SCC_CFG2 Register [reset = 0x32]

BITS	BIT NAME	RESET	TYPE	DESCRIPTION	RESET BY
D[7]	V1X_OCP1_DIS	0	R/W	V1X OCP1 Function Disable Bit 0 = Enable (default) 1 = Disable	REG_RST or WDT
D[6]	Reserved	0	R	Reserved	N/A
D[5:4]	DTHR[1:0]	11	R/W	Setting Bits of Switching Frequency Dithering Enable and Ratio 00 = Dithering varies switching frequency between ±3% 01 = Dithering varies switching frequency between ±6% 10 = Dithering varies switching frequency between ±12% 11 = Dithering is OFF (default)	REG_RST or WDT
D[3]	PH_DEL	0	R/W	Setting Bit of Phase Delay Between Channel-1 and Channel-2 0 = 180 degree delay (default) 1 = 90 degree delay	REG_RST or WDT
D[2:0]	FREQ[2:0]	010	R/W	SCC Switching Frequency Setting Bits 000 = 250kHz 001 = 375kHz 010 = 500kHz (default) 011 = 625kHz 100 = 750kHz 101 = 1000kHz 110 = 1200kHz 111 = 1500kHz	REG_RST or WDT

REGISTER AND DATA (continued)

REG0x08: V2X_OVP_SW Register [reset = 0xB0]

BITS	BIT NAME	RESET	TYPE	DESCRIPTION	RESET BY
D[7:3]	V2X_OVP_R[4:0]	1 0110	R/W	V_{V2X} OVP Protection Rising Threshold Setting Bits 0 0000 ~ 0 1100: $V2X_{OVP\_R}$ = 8.3V + V2X_OVP_R[4:0] × 0.05V 0 1101 ~ 1 0010: $V2X_{OVP\_R}$ = 7.7V + V2X_OVP_R[4:0] × 0.10V 1 0011 ~ 1 1000: $V2X_{OVP\_R}$ = 5.0V + V2X_OVP_R[4:0] × 0.25V 1 1001 ~ 1 1110: $V2X_{OVP\_R}$ = 11V 1 1111 = V2X OVP Disabled Default: 0x16, $V2X_{OVP\_R}$ = 10.5V	REG_RST or WDT
D[2]	Reserved	0	R	Reserved	N/A
D[1:0]	V2X_SW_F[1:0]	00	R/W	Setting Bits of V_{V2X} Falling Threshold to Exit Switching 00 = 3.8V (default) 01 = 4V 10 = 4.2V 11 = 4.4V	REG_RST or WDT

REG0x09: V1X_OVP_SW Register [reset = 0x15]

BITS	BIT NAME	RESET	TYPE	DESCRIPTION	RESET BY
D[7]	V1X_SW_F	0	R/W	Setting Bit of V_{V1X} Falling Threshold to Exit Switching 0 = 2.6V (default) 1 = 2.7V	REG_RST or WDT
D[6:5]	SW_F_DEG[1:0]	00	R/W	Setting Bits of Deglitching Time for V_{V1X} or V_{V2X} to Exit Switching 00 = 0ms (default) 01 = 108μs 10 = 500μs 11 = 1ms	REG_RST or WDT
D[4:0]	V1X_OVP_R[4:0]	1 0101	R/W	V_{V1X} OVP Protection Rising Threshold Setting Bits 0 0000 ~ 0 1100: $V1X_{OVP\_R}$ = 4.15V + V1X_OVP_R[4:0] × 0.025V 0 1101 ~ 1 0111: $V1X_{OVP\_R}$ = 3.20V + V1X_OVP_R[4:0] × 0.1V 1 0111 ~ 1 1110: $V1X_{OVP\_R}$ = 5.5V 1 1111 = V1X OVP Disabled Default: 0x15, $V1X_{OVP\_R}$ = 5.3V	REG_RST or WDT

REG0x0A: OCP1 Register [reset = 0x93]

BITS	BIT NAME	RESET	TYPE	DESCRIPTION	RESET BY
D[7]	OCP_ALM_TH	1	R/W	V1X Over-Current Alarm Threshold Setting Bits 0 = 80% of I_{V1X_OCP1} 1 = 90% of I_{V1X_OCP1} (default)	REG_RST or WDT
D[6]	V1X_PDN_EN	0	R/W	V1X Pull-Down Resistor Enable Bit 0 = Pull-down disabled (default) 1 = Pull-down enabled. When enabled, the V1X is pulled down by 1kΩ R_{AD_V1X}.	REG_RST or WDT
D[5]	V2X_PDN_EN	0	R/W	V2X Pull-Down Resistor Enable Bit 0 = Pull-down disabled (default) 1 = Pull-down enabled. When enabled, the V2X is pulled down by 10kΩ R_{AD_V2X}.	REG_RST or WDT
D[4:3]	V1X_OCP1_DGL[1:0]	10	R/W	V1X OCP1 Protection Deglitch Time Setting Bits 00 = 3μs 01 = 200μs 10 = 1ms (default) 11 = 2ms	REG_RST or WDT
D[2:0]	V1X_OCP1[2:0]	011	R/W	Bidirectional V1X OCP1 Protection Threshold Setting Bits I_{V1X_OCP1} = 13.2A + V1X_OCP1[2:0] × 1.1A Default:0x3, I_{V1X_OCP1} = 16.5A	REG_RST or WDT

REGISTER AND DATA (continued)

REG0x0B: OCP2 Register [reset = 0x76]

BITS	BIT NAME	RESET	TYPE	DESCRIPTION	RESET BY
D[7:4]	V2X_OCP2[3:0]	0111	R/W	V2X OCP2 Protection Threshold Setting Bits 0000 ~ 1110: $V2X_{OCP2}$ = 300mV + V2X_OCP2[3:0] × 40mV 1111 = OFF Default: 0x7, $V2X_{OCP2}$ = 580mV Note: V2X OCP2 is triggered when $V_{V2X} < 2V_{V1X} - V2X_{OCP2}$ in reverse direction	REG_RST or WDT
D[3:0]	V1X_OCP2[3:0]	0110	R/W	V1X OCP2 Protection Threshold Setting Bits 0000 ~ 1110: $V1X_{OCP2}$ = 100mV + V1X_OCP2[3:0] × 40mV 1111 = OFF Default: 0x6, $V1X_{OCP2}$ = 340mV Note: V1X OCP2 is triggered when $V_{V1X} < V_{V2X}/2 - V1X_{OCP2}$ in forward direction	REG_RST or WDT

REG0x0C: FWD_SS_CFG Register [reset = 0x41]

BITS	BIT NAME	RESET	TYPE	DESCRIPTION	RESET BY
D[7:6]	OCP2_DGL[1:0]	01	R/W	OCP2 Protection Deglitch Time Setting Bits 00 = 0.1μs 01 = 0.8μs (default) 10 = 1.6μs 11 = 3.2μs	REG_RST or WDT
D[5:4]	FWD_ISS[1:0]	00	R/W	Forward Mode Soft-Start Current Setting Bits (total at V1X) 00 = 145mA (default) 01 = 290mA 10 = 435mA 11 = 580mA	REG_RST or WDT
D[3]	Reserved	0	R	Reserved	N/A
D[2:0]	FWD_SS_TMO[2:0]	001	R/W	Forward Mode Soft-Start Timeout Setting Bits t_{SS_FWD} = 62.5ms + FWD_SS_TMO[2:0] × 62.5ms Default: 0x1, t_{SS_FWD} = 125ms	REG_RST or WDT

REG0x0D: RVS_SS_CFG Register [reset = 0x06]

BITS	BIT NAME	RESET	TYPE	DESCRIPTION	RESET BY
D[7:5]	Reserved	000	R	Reserved	N/A
D[4:3]	RVS_ISS[1:0]	00	R/W	Reverse Mode Soft-Start Current Setting Bits (total at V2X) 00 = 100mA (default) 01 = 150mA 10 = 200mA 11 = 250mA	REG_RST or WDT
D[2:1]	RVS_SS_TMO[1:0]	11	R/W	Reverse Mode Soft-Start Timeout Setting Bits t_{SS_RVS} = 10min + RVS_SS_TMO[1:0] × 10min Default: 0x3, t_{SS_RVS} = 40min	REG_RST or WDT
D[0]	Reserved	0	R	Reserved	N/A

REGISTER AND DATA (continued)

REG0x0E: REQNFLT_CFG Register [reset = 0x1A]

BITS	BIT NAME	RESET	TYPE	DESCRIPTION	RESET BY
D[7:6]	Reserved	00	R	Reserved	N/A
D[5:4]	DEEP_SKIP[1:0]	01	R/W	Setting Bits of Deglitch Time for Entry to Deep Skip Mode 00 = 56μs 01 = 88μs (default) 10 = 120μs 11 = 152μs	REG_RST or WDT
D[3]	RESTART_EN	1	R/W	Enable Bit of Restart After Faults 0 = Disabled 1 = Enabled (default)	REG_RST or WDT
D[2]	Reserved	0	R	Reserved	N/A
D[1:0]	WAIT_T[1:0]	10	R/W	Setting Bits of Restart Wait Time after Faults 00 = 0.25sec 01 = 0.38sec 10 = 0.5sec (default) 11 = 0.75sec	REG_RST or WDT

REG0x0F: SKIP_CFG Register [reset = 0x40]

BITS	BIT NAME	RESET	TYPE	DESCRIPTION	RESET BY
D[7:6]	F2S_DROP[1:0]	01	R/W	Setting Bits of Threshold for Quitting Fixed f_{SW} Mode and Entering Skip Mode (In forward mode, device enters skip mode when V_{V1X} exceeds $V_{V2X}/2 - \Delta V_{F2S\_FWD}$ threshold, where ΔV_{F2S_FWD} = F2S_DROP[1:0] × 10mV + 40mV - F2S_FWD_OFFSET × 30mV) 00 = 10mV 01 = 20mV (default) 10 = 30mV 11 = 40mV	REG_RST or WDT
D[5:4]	S2F_DROP[1:0]	00	R/W	Setting Bits of Threshold for Quitting Skip Mode and Entering Fixed f_{SW} Mode (In forward mode, device enters fixed f_{SW} mode when V_{V1X} falls below the $V_{V2X}/2 - \Delta V_{S2F\_FWD}$ threshold, where ΔV_{S2F_FWD} = ΔV_{F2S_FWD} + S2F_DROP[1:0] × 5mV + 10mV) 00 = 10mV (default) 01 = 15mV 10 = 20mV 11 = 25mV	REG_RST or WDT
D[3:2]	SAG_FWD[1:0]	00	R/W	Setting Bits of Allowed Voltage Sag before Entering Fixed f_{SW} Mode (In forward operation skip mode) 00 = 5mV (default) 01 = 10mV 10 = 15mV 11 = 20mV	REG_RST or WDT
D[1:0]	Reserved	00	R/W	Reserved	N/A

REG0x10: MISC1 Register [reset = 0x00]

BITS	BIT NAME	RESET	TYPE	DESCRIPTION	RESET BY
D[7]	LO_V2X_SW_STATUS	0	R	Low V2X Switching (V_{V2X} < $V2X_{VALID}$) Status Bit 0 = Not in low V2X switching (default) 1 = Device is in low V2X switching	N/A
D[6:0]	Reserved	000 0000	R	Reserved	N/A

REG0x11: RESERVED [reset = 0x59]

BITS	BIT NAME	RESET	TYPE	DESCRIPTION	RESET BY
D[7:0]	Reserved	0101 1001	R	Reserved	N/A

REGISTER AND DATA (continued)

REG0x12: WDT_TIMEOUT Register [reset = 0x00]

BITS	BIT NAME	RESET	TYPE	DESCRIPTION	RESET BY
D[7:4]	Reserved	0000	R	Reserved	N/A
D[3]	WDT_TIMEOUT_INT	0	RC	Watchdog Timeout Event Flag Bit 0 = No Watchdog Timeout (default) 1 = Watchdog Timeout happens. Generates an interrupt on IRQB pin. Read this bit to reset it to 0 and start the watchdog timer if watchdog timer is enabled.	N/A
D[2:0]	WDT_TIMEOUT[2:0]	000	R/W	Watchdog Timer Setting Bits 000 = Disable watchdog timer (default) 001 = 0.5s 010 = 1s 011 = 2s 100 = 20s 101 = 40s 110 = 80s 111 = 160s Watchdog timeout event will reset all the registers except WDT_TIMEOUT[2:0] and status and flag bits to the default values. Any I²C read/write will reset the watchdog timer if not disabled.	REG_RST

REG0x13: CHIP_REV Register [reset = 0x00]

BITS	BIT NAME	RESET	TYPE	DESCRIPTION	RESET BY
D[7:4]	OTP_VER[3:0]	0000	R	OTP Receipt Version	N/A
D[3:0]	CHIP_VER[3:0]	0000	R	IC Version	N/A

REG0x14: DEVICE_ID Register [reset = 0x09]

BITS	BIT NAME	RESET	TYPE	DESCRIPTION	RESET BY
D[7:0]	DEVICE_ID[7:0]	0000 1001	R/W	Device ID 0000 1001 = SGM41603A	N/A

REG0x15: Debug Register [reset = 0x00]

BITS	BIT NAME	RESET	TYPE	DESCRIPTION	RESET BY
D[7:3]	Reserved	00000	R	Reserved	N/A
D[2]	F2S_FWD_OFFSET	0	R/W	Voltage Offset for Setting ΔV_{F2S_FWD} Threshold 0 = 30mV (default) 1 = 0mV ΔV_{F2S_FWD} = F2S_DROP[1:0] × 10mV + 40mV - F2S_FWD_OFFSET × 30mV	REG_RST or WDT
D[1:0]	Reserved	00	R	Reserved	N/A

TYPICAL APPLICATION CIRCUITS

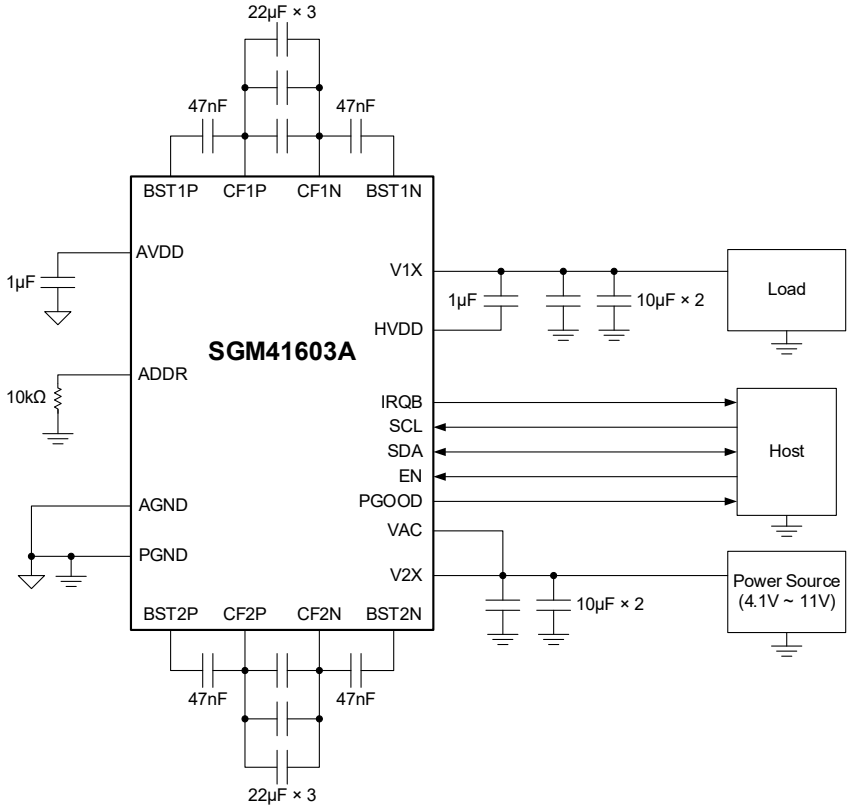


Figure 3. Typical Application Circuit 1

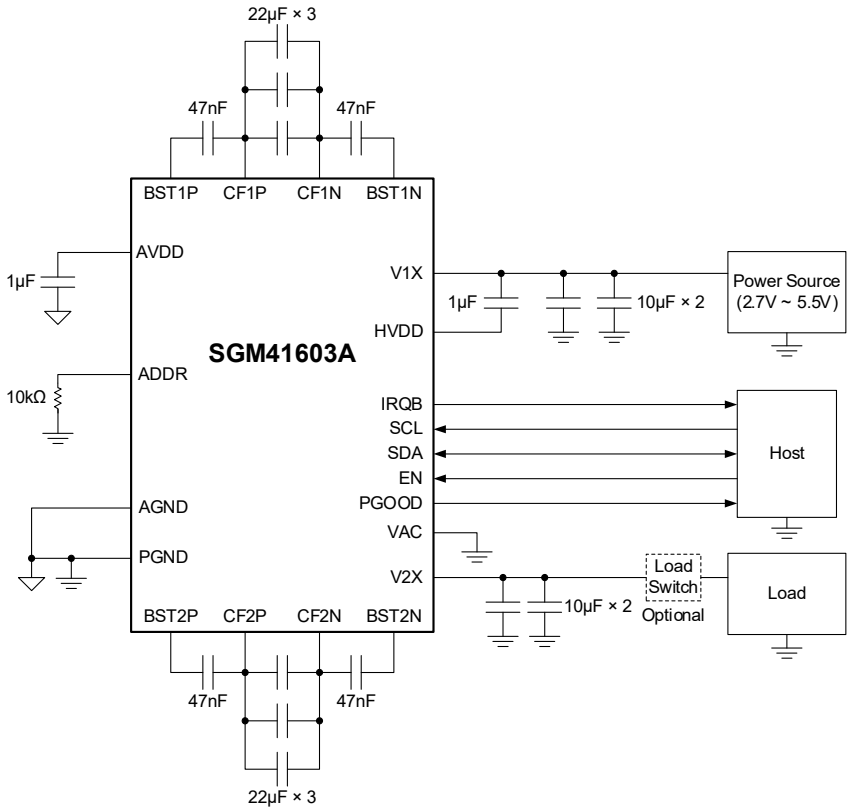


Figure 4. Typical Application Circuit 2

DETAILED DESCRIPTION

New electronic devices require more electric current and this demand is constantly increasing with every new generation of the equipment. Higher current requires larger batteries to keep the portable device running. Larger batteries in turn need higher charging currents to keep the charge time reasonably short. To reduce the charge current losses, it is preferred to have battery cells in series rather than in parallel, but the battery pack voltage will be higher. However, even for some low-voltage applications, it is beneficial to configure the batteries as 2-series (2S) cell and use an efficient 2-to-1 bidirectional voltage converter to interface the battery for powering the LV system. It is much faster to charge a 2S battery compared to a 2-parallel battery (2P) with the same current. To power the system the converter acts as a current-doubler and delivers double current to the system as if the source is 2P. The SGM41603A is an ultra-efficient switched-capacitor (inductor-less) converter with small solution size that perfectly fits such job. It can also function as a voltage doubler to power the high-voltage load when V1X is connected to a 1S power supply.

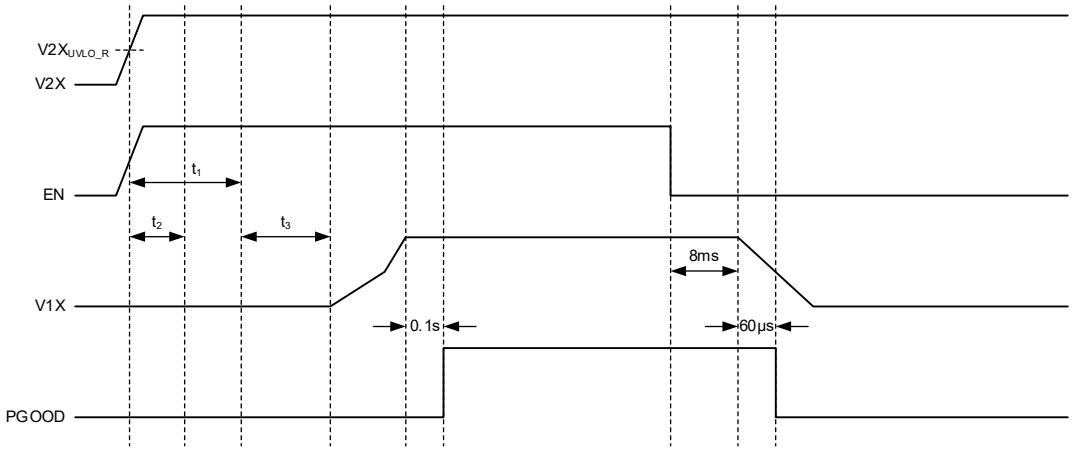
The Switched-Capacitor Converter (SCC)

A switched-capacitor converter uses capacitors as energy storage and transfer element for DC/DC conversion. Compared to converters that use inductors (like Buck converter), the SCC provides higher efficiency, smaller solution size and lower cost. The SGM41603A is a dual channel bidirectional 2:1/1:2 SCC with 10A output current capability in forward direction and 5A output current capability in reverse direction. In forward direction, half of the input voltage (1/2 × V_{V2X}) is generated on the output (V1X). In the reverse direction, the doubled input voltage (2 × V_{V1X}) is generated on the output (V2X) with 5A capability. The converter operates with a fixed 50% duty cycle and change between forward and reverse modes is automatic. To reduce the output voltage and current ripples, the converter is composed of two channels (90° or 180° selectable).

Enable Input (EN)

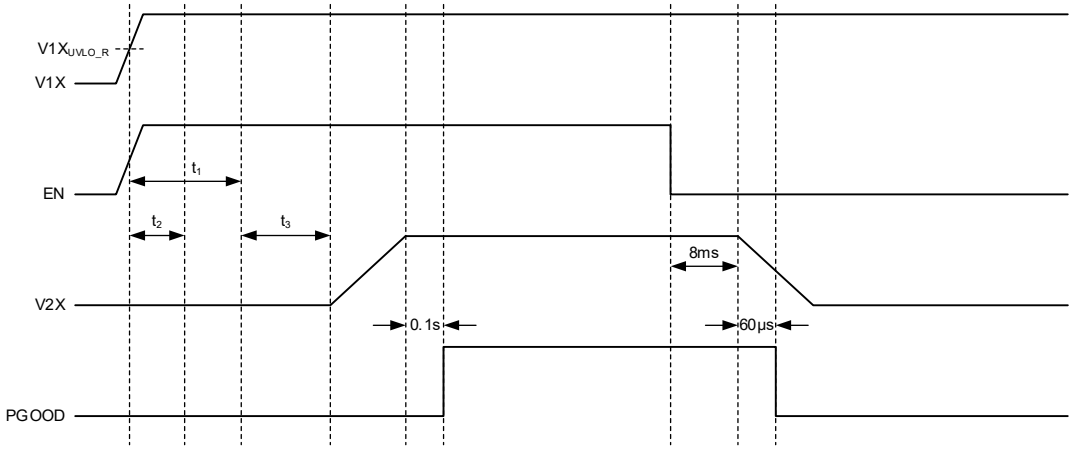
The EN pin is an active high enable input for the SGM41603A. When EN is pulled high and after the deglitch time (t_{EN_DEG}), first the soft discharge is activated for t_{SFT_DISCHG} and then the soft-start is initiated. The SCC full activation occurs only after a successful soft start. If EN is pulled low, the SCC turns off with 8ms (TYP) EN falling deglitch time. The t_{EN_DEG} deglitch time and t_{SFT_DISCHG} soft-discharge-time are I²C programmable. See Figure 5 for enable and soft-start timings in both directions. In this figure:

- t_1 is the EN deglitch time (EN_DEG[2:0] in REG0x05) and can be set from 0.125ms to 64ms (default 0.125ms).
- t_2 is the standby time which is 125μs (minimum time in STANDBY state).
- t_3 is the soft-discharge time (SFT_DISCHG_T[1:0] in REG0x06) that can be set from 50ms to 300ms (default 100ms).



a. Forward Direction

DETAILED DESCRIPTION (continued)



b. Reverse Direction

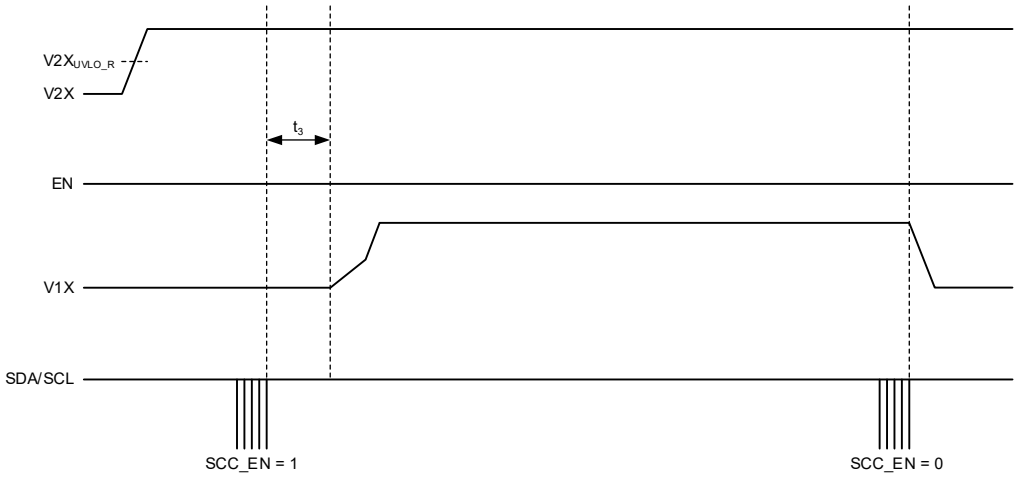
Figure 5. EN, Soft-Start and Power Good Timings (t_1: EN Deglitch Time; t_2: Standby Time; t_3: Soft Discharge Time)

Enable/Disable by I²C

Except enabling the device by EN pin, the host also can enable the device output by setting SCC_EN bit to 1 in REG0x05 when EN is low. The host can reset SCC_EN to 0, to disable the output (See Figure 6).

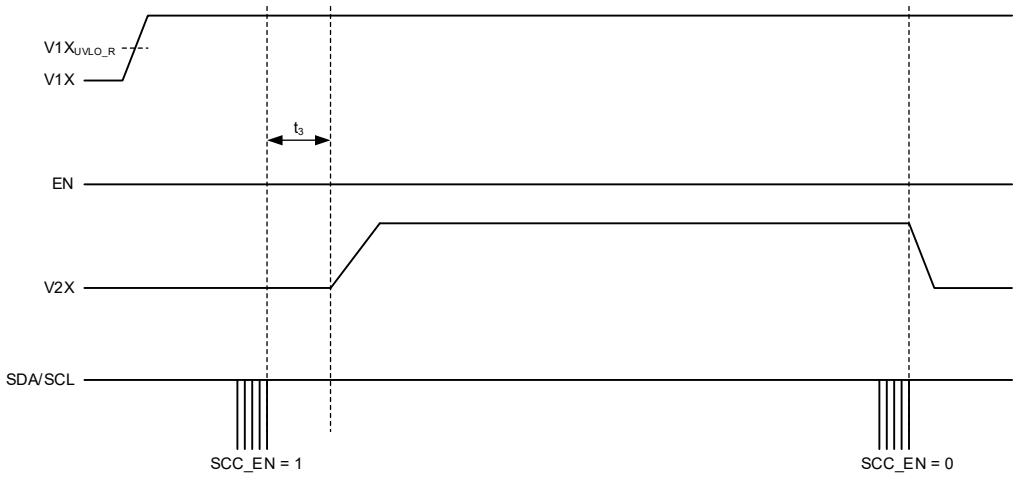
Startup and Soft-Start in Forward Direction

During the SGM41603A start up in forward direction, the flying capacitors (C_{FLY}) appear in parallel with the output (V1X) capacitor after the PoorSRC qualification timer expires (t_{SFT_DISCHG}). In normal operation, the capacitors are charged to a voltage near the final value (V_{V2X}/2) with a soft-start current that is I²C adjustable from 145mA to 580mA (setting by FWD_ISS[1:0] bits in REG0x0C). If within t_{SS_FWD} (forward mode soft-start time) and for 10 successive tries, the output does not reached near V_{V2X}/2 voltage, a FSS_FLT_INT (forward mode soft-start fault) interrupt will be generated and the device returns back to the STANDBY state. But if the soft start is successful, normal operation will begin. The t_{SS_FWD} soft-start time can be set by I²C.



a. Forward Direction

DETAILED DESCRIPTION (continued)



b. Reverse Direction

Figure 6. Enable Timing Waveform with I²C Command (t_3: Soft Discharge Time)

Startup and Soft-Start in Reverse Direction

During reverse direction start up, when the PoorSRC qualification timer expires (t_{SFT_DISCHG}) for V1X/V2X, and the following two conditions are met for V1X, then V2X charging will start with the I_{SS_RVS} current. It is noted that

1. V_{V1X} > ($V1X_{SW\_F}$ + VX_{SW_HYS}) and
2. V_{V1X} > (V_{V2X}/2 + 30mV)

When V2X voltage exceeds the $V2X_{VALID}$ threshold, V2X_VALID bit changes from 0 to 1, and an interrupt signal is sent on IRQB pin if unmasked. Finally, if V2X reaches to ($2V_{V1X}$ - $V2X_{OCP2}$ + 20mV) threshold, PGOOD output high after 0s or 100ms delay setting by PGOOD_DELAY bit, the converter starts full switching as a 1:2 SCC. If V2X voltage dose not reached $V2X_{VALID}$ within t_{SS_RVS} (reverse mode soft-start time), an RVS_FLT_INT (reverse mode soft-start fault) interrupt will be generated and the device returns back to the STANDBY state. The t_{SFT_DISCHG}, I_{SS_RVS}, t_{SS_RVS} parameters are I²C adjustable.

PGOOD

PGOOD is a push-pull power good indicator output with 200μA capability. When V1X is close to V2X/2 in forward soft-start, after 0s or 100ms delay setting by PGOOD_DELAY bit, PGOOD goes to high state (1.8V) and remains high while the converter is operating normally. An external RC filter (1kΩ, 10nF) should be connected to PGOOD if this pin is used.

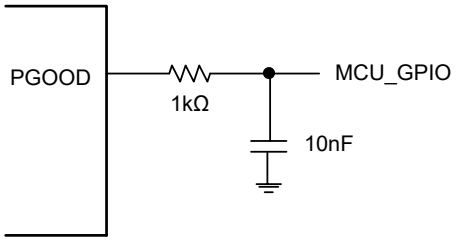


Figure 7. PGOOD Filter Example Circuit

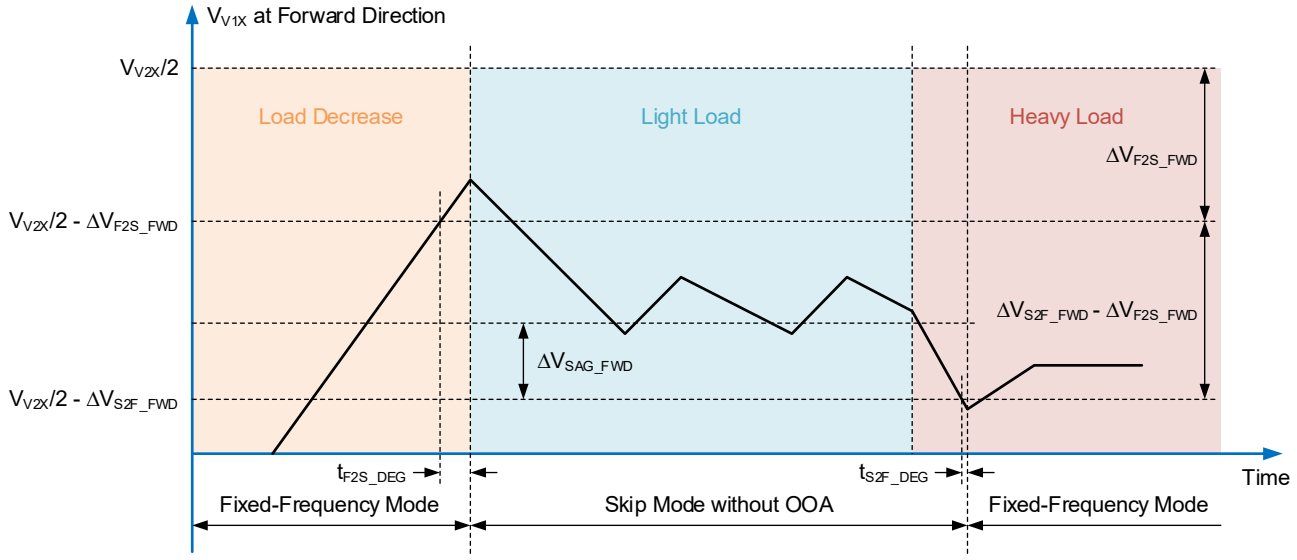
Skip Mode and Fixed-Frequency Mode

In normal operation, the converter operates with 50% duty cycle and the switching frequency is set by the SCC_CFG2 register (REG0x07).

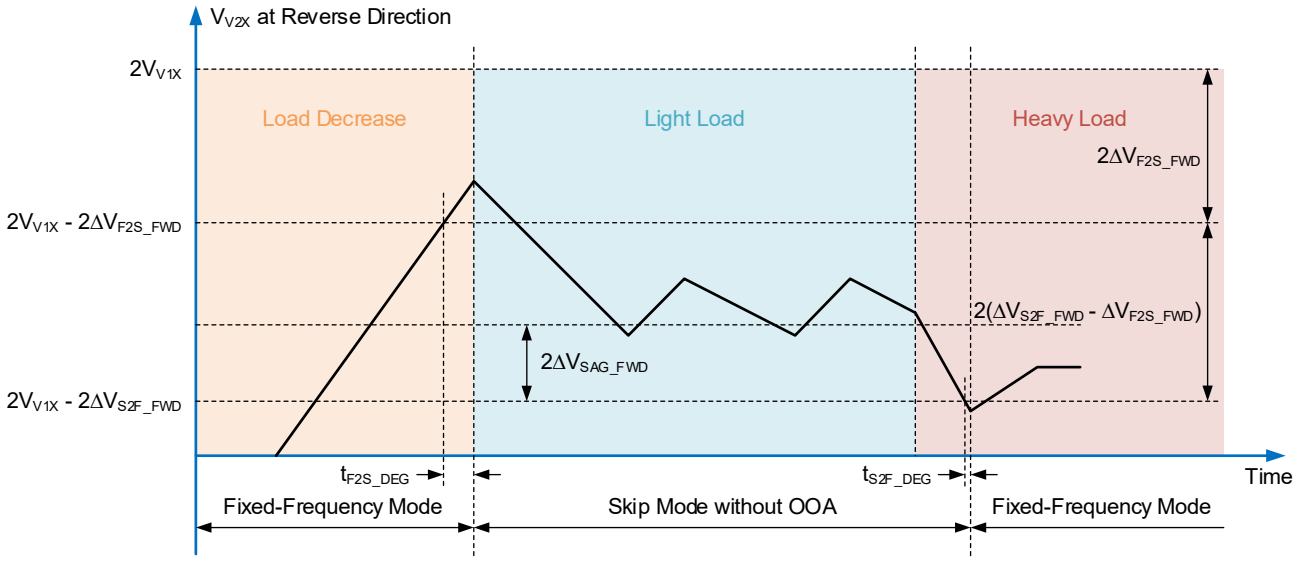
In the fixed-frequency mode, the converter generates unregulated outputs (V_{V2X}/2 at the V1X pin in forward mode or 2 × V_{V1X} at the V2X pin in reverse mode).

By setting the FIX_FREQ bit in REG0x06 to 0, the device is allowed for automatic entry to skip mode at light load. To keep the device in Fixed-Frequency mode and avoid skip mode, the FIX_FREQ bit must be set to 1. Figure 8 illustrates the skip mode operation. For example, when the V_{V1X} output exceeds the (V_{V2X}/2 - ΔV_{F2S_FWD}) threshold in forward mode, the device enters skip mode. It will return to Fixed-Frequency mode when V_{V1X} falls below the (V_{V2X}/2 - ΔV_{S2F_FWD}) threshold. Similar behavior occurs in reverse mode. The skip mode saves power at light loads and keeps the high efficiency over the entire load range, and in the same time maintains the V_{V1X} output near V_{V2X}/2.

DETAILED DESCRIPTION (continued)



a. Forward Direction



b. Reverse Direction

Figure 8. SGM41603A Skip Mode Operation

Out-of-Audio (OOA) Mode

When the SCC operates in skip mode, the skip frequency can fall in the audio range (20Hz to 20kHz). This can create audible noise in multilayer chip capacitor and the PCB. The SGM41603A offers an Out-of-Audio (OOA) Mode feature that if enabled, keeps the minimum skip frequency above 30kHz.

Operating details for the OOA mode during Skip interval is illustrated in Figure 9. During Skip mode, the maximum skip interval does not exceed t_{OOA} when OOA is enabled.

DETAILED DESCRIPTION (continued)

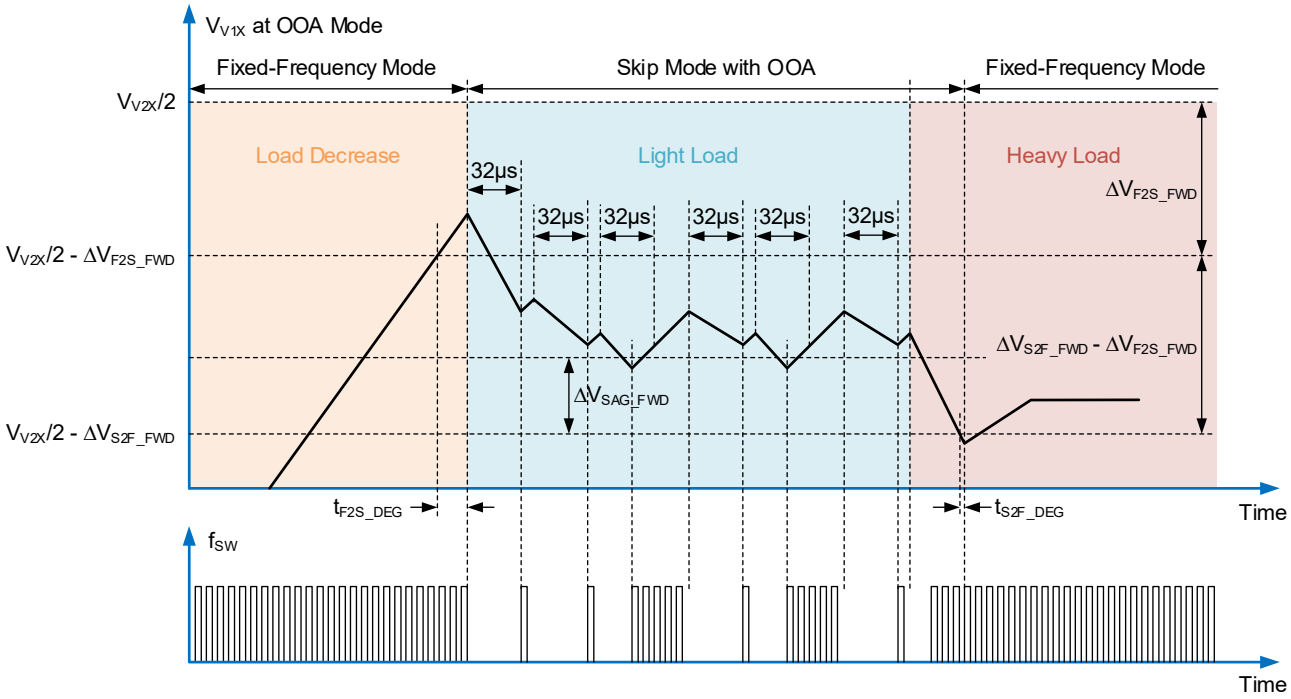


Figure 9. Skip Mode with Out-of-Audio (OOA) Operation at 500kHz

Under-Voltage Lockout (UVLO)

The SGM41603A will shut down if a UVLO event occurs in which V_{V2X} falls below $V2X_{UVLO\_F}$ and V_{V1X} falls below $V1X_{UVLO\_F}$ and V_{VAC} falls below V_{VAC_UVLO} falling threshold. It will not restart until one of the port voltages exceeds its UVLO threshold (V_{V2X} exceeds the $V2X_{UVLO\_R}$ threshold or V_{V1X} exceeds the $V1X_{UVLO\_R}$ threshold or V_{VAC} exceeds the V_{VAC_UVLO} rising threshold).

Frequency Dithering

The fixed switching frequency of the switching converter generates high peaks in EMI emission spectrum. By enabling the frequency dithering, this frequency is cyclically varied in a narrow band around the set frequency such that the emitted energy is distributed over a wider frequency range and the emission peaks are reduced. This feature is I²C configurable and can be disabled or set to 3%, 6% or 12% of the switching frequency in the whole synthesized switching frequency range (0.25MHz to 1.5MHz).

Over-Current Protections

The SGM41603A has two levels of over-current protection in forward direction. The V1X output current is monitored for I_{V1X_OCP1} over-current protection. For a faster short-circuit protection, the V1X and V2X are also sensed for drops ($V1X_{OCP2}$). The output is disabled if the V1X output current exceeds I_{V1X_OCP1} or if V_{V1X} falls below ($V_{V2X}/2$ - $V1X_{OCP2}$). I_{V1X_OCP1} can be set from 13.2A to 20.9A in 1.1A steps through I²C. $V1X_{OCP2}$ can be turned off or adjusted from 100mV to 660mV in 40mV steps.

In reverse direction, not only the V1X input current is monitored for detecting I_{V1X_OCP1} over-current, but also the V1X and the V2X are sensed for drops for faster short-circuit protection ($V2X_{OCP2}$). The output will disable if V_{V2X} falls below ($2V_{V1X}$ - $V2X_{OCP2}$). The $V2X_{OCP2}$ can be set from 300mV to 860mV in 40mV steps.

High Current Alarm (OCP_{ALM})

When V1X current (in or out) exceeds the OCP_{ALM} threshold (80% or 90% of the I_{V1X_OCP1}), the V1X_OC_ALM_INT interrupt bit and V1X_OC_ALM status bits are set. The OCP_{ALM} can be set to to 80% or 90% (default). The V1X_OC_ALM bit resets when the V1X current falls below OCP_{ALM_HYS} of the I_{V1X_OCP1}.

Over-Temperature Alarms and Fault

The die temperature (T_J) is monitored for thermal protection. If T_J exceeds +155℃ (T_{SHDN}), the device enters in the thermal shutdown state and the T_SHDN_INT interrupt bit is set. If T_J falls for around 15℃, the thermal shutdown will terminate and SCC can be enabled again.

Two additional alarming comparators that trip at +100℃ and +120 ℃ can set the T_ALM1 and T_ALM2 interrupts respectively.

DETAILED DESCRIPTION (continued)

Over-Voltage Lockout Protections for V2X and V1X

The SCC output will disable if an over voltage occurs on V1X or V2X. For V_{V2X} the $V2X_{OVP\_R}$ over voltage threshold is adjustable from 8.3V to 11V in REG0x08[7:3] with 10.5V default value. For V_{V1X} the $V1X_{OVP\_R}$ is adjustable from 4.15V to 5.5V in REG0x09[4:0] with 5.3V default value.

Converting Over-Current Protection

The CONV_OCP function monitors the converter switch operating current of power MOSFETs. If the Q_{CLx} or Q_{DLx} current reaches switch converting OCP threshold during forward or reverse mode, the CONV_OCP_INT bit is set to 1 and an interrupt is generated on IRQB pin, the operation is stopped and the chip returns to standby mode.

Auto Restart Features after Faults

Two after-fault auto restart feature are included in this device. Since the SGM41603A is usually the system power supply, in most applications it cannot be re-enabled externally after a fault (the auto restart feature is essential). After any fault, the switcher is off and if the active discharge is enabled, it will conduct an active discharge first. After that if all following conditions are valid:

(1) The fault condition is removed.
(2) EN is higher than V_{IH} or SCC_EN = 1.
(3) RESTART_EN bit is 1.
(4) At least one of the V1X or V2X voltages is above its switching start threshold ($V1X_{SW\_R}$ or $V2X_{SW\_R}$ respectively).

Then after a wait time (adjustable by WAIT_T[1:0] bits), the device initiates a soft start.

Note that if RESTART_EN is 0, the EN pin must be toggled to enable the output after a fault power down.

I²C Slave Address Setting

The ADDR pin is used to set the default I²C address during the POR procedure. By placing a 10kΩ or smaller resistor between ADDR and ground before power-up, the slave address is changed to 0x69 in the normal status. If ADDR is kept floating before power up, the slave address is 0x68.

I²C Interface

The SGM41603A acts as an I²C Slave Transmitter/Receiver at the following slave addresses:

Slave Address (7 bit) 1101 000 or 1101 001
Slave Address (Write) 0xD0 1101 0000 or 0xD2 1101 0010
Slave Address (Read) 0xD1 1101 0001 or 0xD3 1101 0011

I²C System Configuration

A “Transmitter” is a device on the I²C bus that generates a ″message″ on the bus and a “Receiver” is a device that receives that message from the bus. The “Master” is the device that controls the messaging, and a “Slave” is any device that is controlled by the ″Master″.

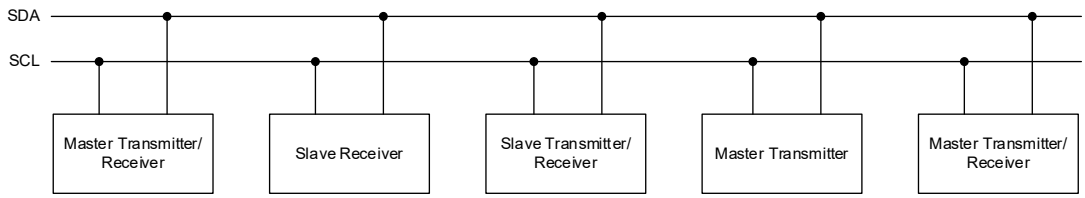


Figure 10. Configurations of the I²C Devices

DETAILED DESCRIPTION (continued)

Start and Stop Conditions

When the bus is free (idle), both SDA and SCL remain high. A START (S) condition is sent by master at the beginning of a transaction with a high-to-low transition on the SDA line while the SCL is high and all slaves will detect that. Similarly, one (or more) STOP (P) condition is sent by master with a low-to-high transition of the SDA line while the SCL is high to terminate the transaction and release the bus (See Figure 11). It is recommended to initiate the bus by sending a STOP condition after power-up. The master may not release the bus after a complete transaction with the slave and send a repeated START (Sr) to initiate a new data exchange with the slave.

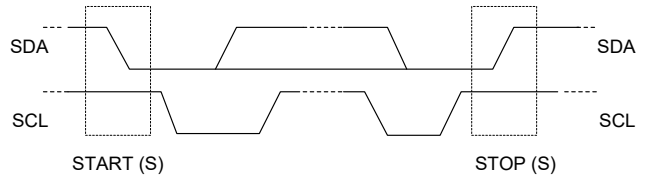


Figure 11. Placing the Start and Stop Conditions in the I²C Bus

Bit Transfer

With each clock pulse one data bit can be transferred as shown in Figure 12. The data on SDA line must remain stable (setup and hold times must be met) during the high time of the clock (SDA transitions during CLK high time are interpreted as a control signal).

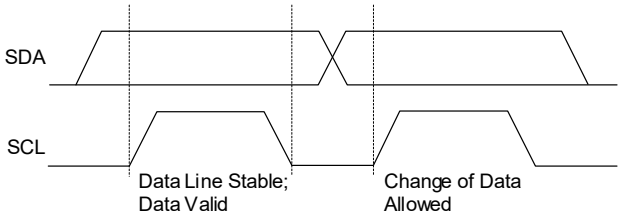


Figure 12. I²C Bit Transfer

I²C Data Format and Acknowledge

The data is transmitted one byte at a time. After detecting the START condition, the transmitter will send one byte (8-bit) of data, bit by bit starting from the Most Significant Bit (MSB). With each SCL pulse a new bit is placed on the SDA line. After sending the 8th bit, the transmitter releases the SDA line during the 9th SCL pulse in order to receive an acknowledge bit from the receiver. Therefore, a total of 9 bits is exchanged for each byte. The number of bytes in one transaction is not limited. After sending the ACK bit, if the receiver is busy and cannot transfer another byte of data, it can hold the SCL line low and keep the sender in wait state (clock stretching). When it is ready for another byte of data, it releases the clock line and the data transfer can continue with clocks generated by the master.

The 9th bit is the receiver response (slave or master) to show that the byte is received. Sending a low during the 9th clock cycle is interpreted as ACK. If the receiver responds a high or does not respond at all, the sender will receive a high for the 9th bit that is considered as Not ACK (= NCK). An NCK means that the receiver is not expecting more data. Therefore, the response of the receiver to the last byte in a transaction is an NCK. It can also show that there is a problem in the communication link (rare). After the 9th bit, a STOP or a Repeated START (Sr) should be sent by master. A master receiver must signal an end of data (NCK) to the transmitter on the last byte that has been clocked out of the slave. In this case, the transmitter must leave SDA high to enable the master to generate a STOP condition.

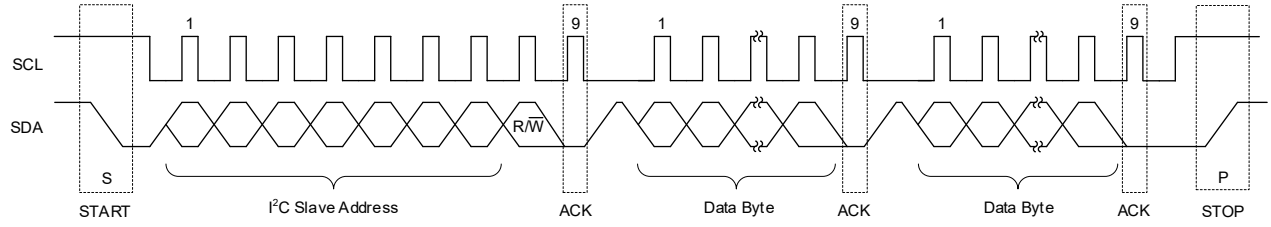


Figure 13. I²C Data Transfer and Acknowledge Bit

DETAILED DESCRIPTION (continued)

Master Transmits Protocol (Write Mode)

Figure 14 shows how the master writes to (R/$\overline{W}$ = 0) a slave register at a specific REGISTER ADDRESS, or group of register in the successive addresses.

Master Reads from Slave after Setting Register Address (Write Register Address and Read Data)

Figure 15 shows how master should read a specific register (it must first write the required register address).

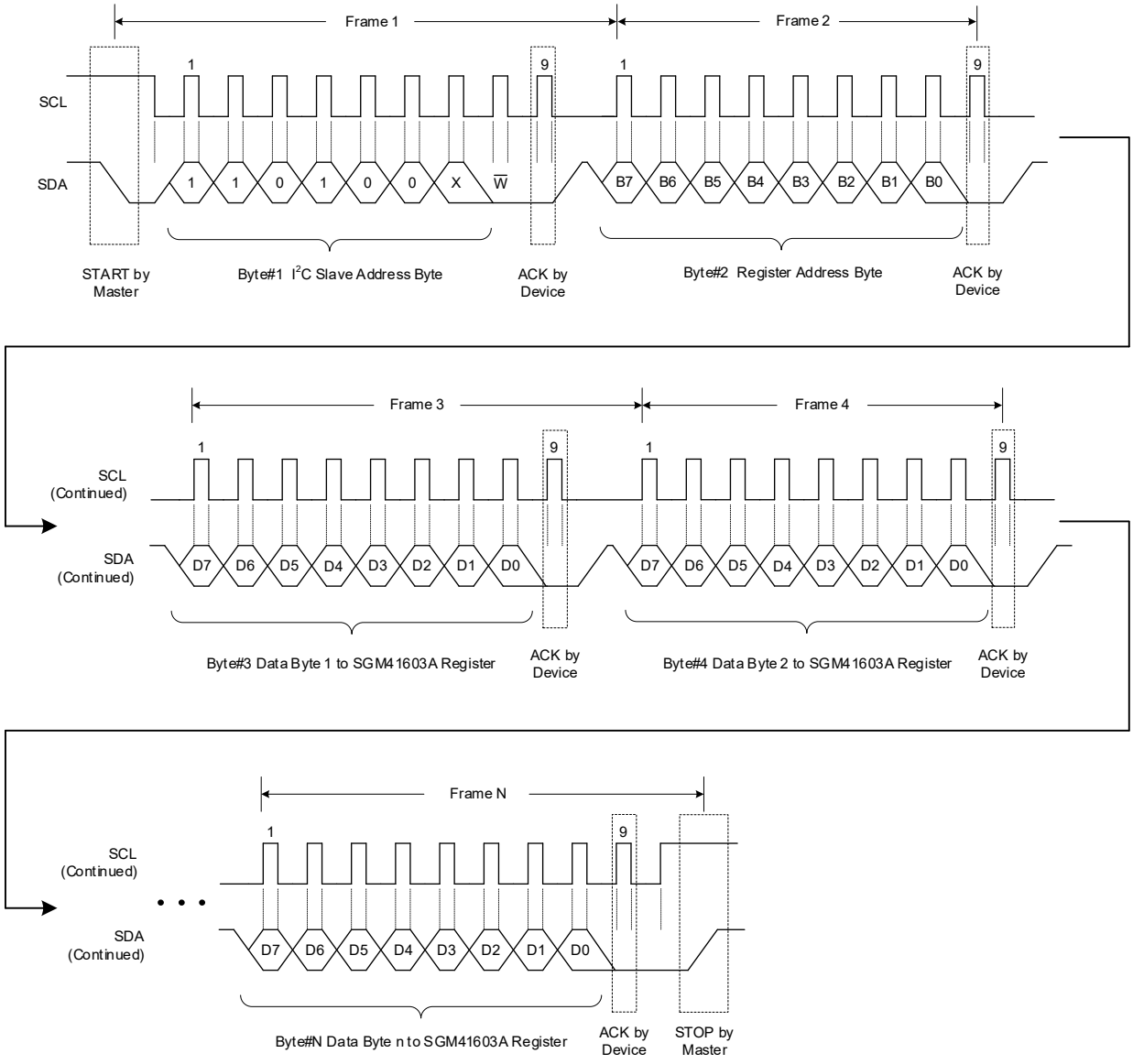


Figure 14. I²C Write Protocol Master Transmits

DETAILED DESCRIPTION (continued)

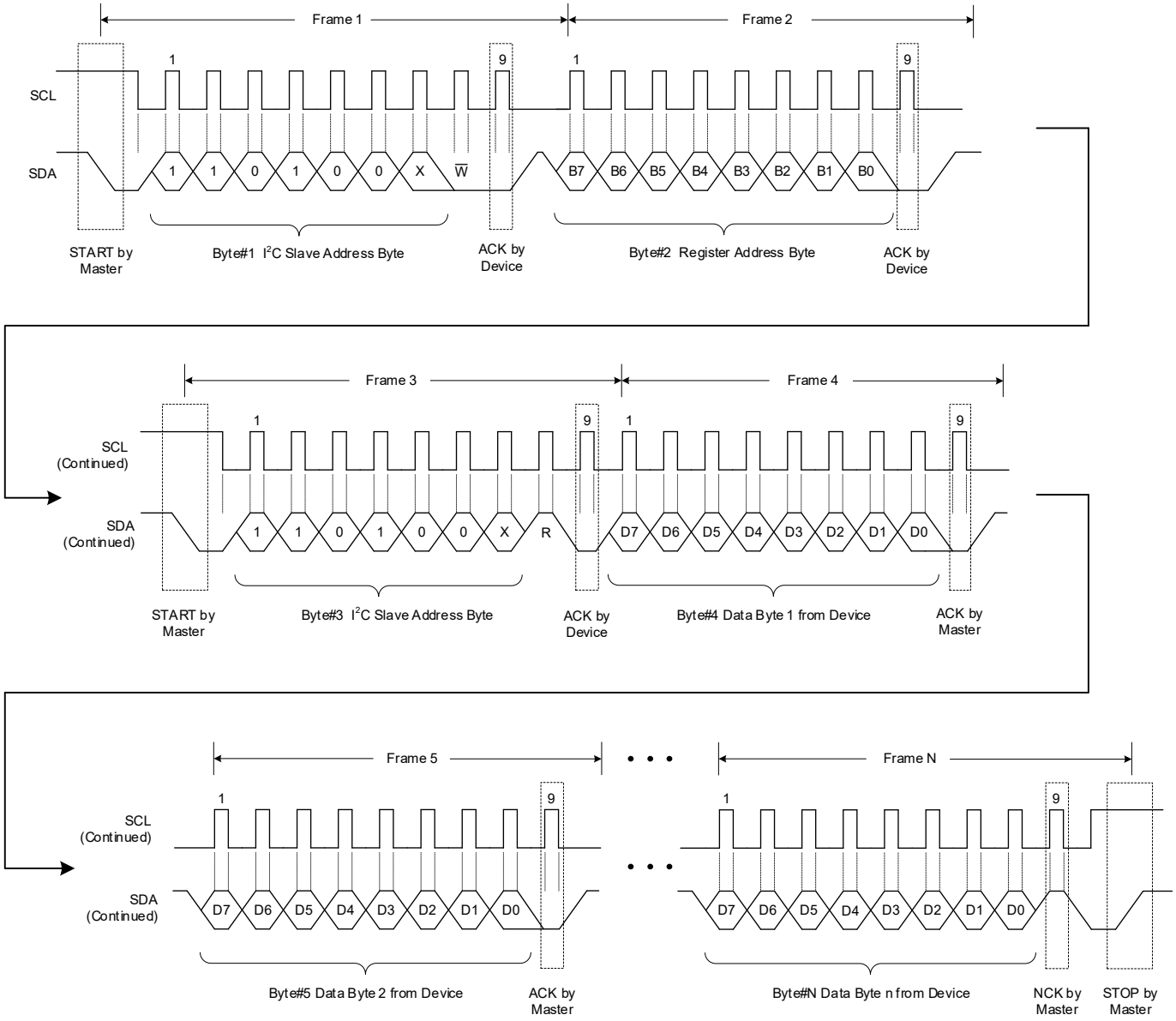


Figure 15. I²C Read Protocol (Master Reads after Setting Register Address)

DETAILED DESCRIPTION (continued)

Block Read: Master Reads Register Data without Setting Register Address (Read Mode)

The format given in Figure 16 can be used to read registers continuously starting from the first register address.

I²C Timeout

In I²C communication, some issues happen sometimes: 1) I²C device pulls SDA forever to ground due to ground noise or supply power noise. 2) SCL clock disappears sometimes because of host interrupt or power down. For SGM41603A, I²C circuit monitors the SCL and SDA line all the time once I²C interface is alive. When the low level is kept over than 25ms for SCL or SDA, I²C circuit will return to the idle state and release the SCL & SDA line unconditionally.

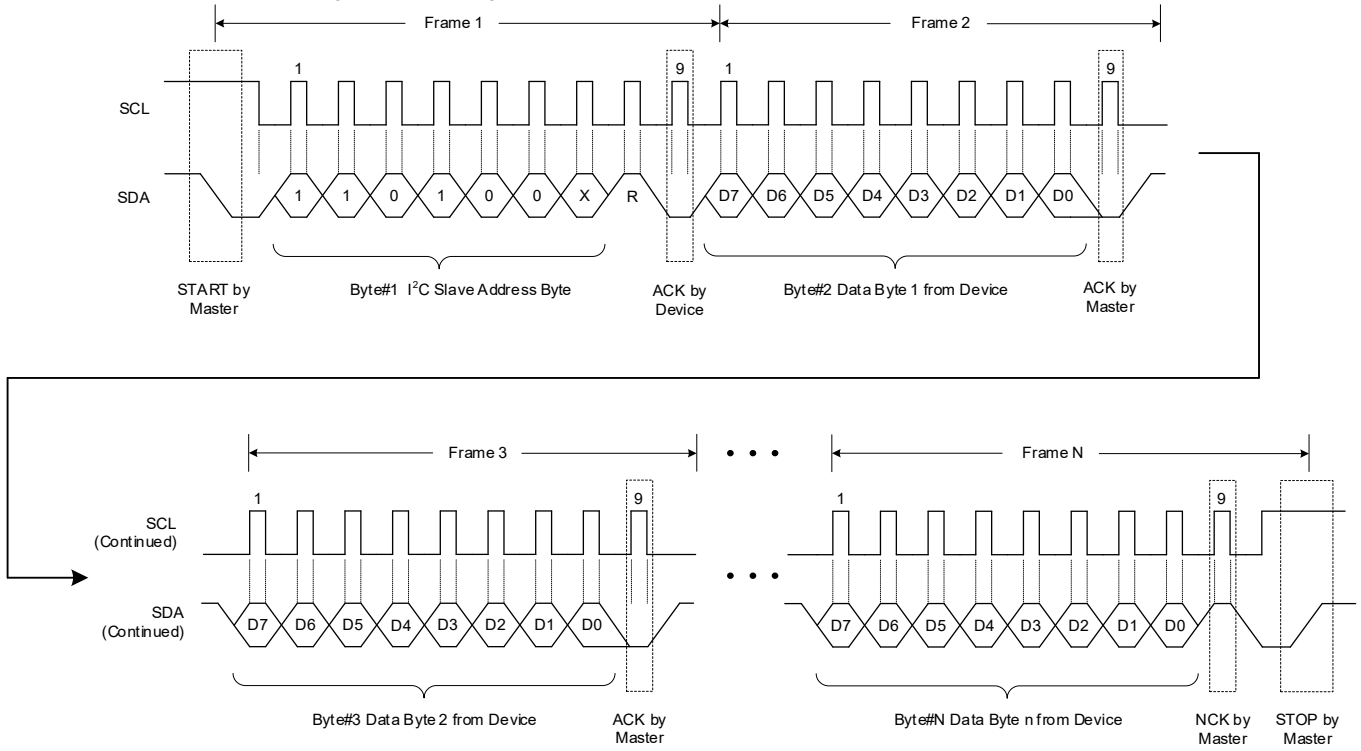


Figure 16. I²C Master Block Read Starting from the First Register

APPLICATION INFORMATION

Input Capacitor Selection (C_{V2X} or C_{V1X})

Two factors should be considered when choosing the input capacitor. One is that it must be chosen to support the maximum expected input surge voltage with adequate design margin. The other is that it is required to reduce peak currents drawn from the input source and reduce input noise.

The selection of C_{V2X} and C_{V1X} is determined by the effective series resistance (ESR) that is required to minimize voltage ripple and load step transients, as well as the amount of bulk capacitance that is necessary to ensure that the operation is stable. For most applications, ceramic capacitor which has total capacitance greater than 20μF with X5R or better grade can obtain stable performance.

A good design should consider the DC bias effect on a ceramic capacitor: as the applied voltage approaches the rated value, the capacitance value decreases. The X5R and X7R type capacitors should be the primary choices due to their stability versus both DC bias and temperature. For all ceramic capacitors, the DC bias effect is even more pronounced on smaller case sizes, so a good design will use the largest affordable case size. Also, it is advisable to select input capacitors with plenty of design margin in the voltage rating to accommodate the worst-case transient input voltage.

Flying Capacitor Selection (C_{FLY})

To select the capacitance of the flying capacitors, current rating and ESR are critical parameters. Moreover, these capacitors are biased to V1X voltage and their voltage rating should be high enough to avoid capacitance drop due to DC bias. The C_{FLY} is selected in a trade-off between efficiency and power density. Smaller C_{FLY} capacitance increases the output voltage/current ripples and reduces efficiency. A large C_{FLY} reduces the output ripples and improves efficiency. The C_{FLY} per channel can be calculated based on the equation below:

$$C_{FLY} = \frac{I_{V1X}}{4 f_{SW} V_{CFLY\_RPP}}$$

To start, set the voltage ripple to 2% of the output voltage:

$$C_{FLY} = \frac{I_{V1X}}{8\% f_{SW} V_{V1X}} \quad (1)$$

where

I_{V1X} is the V1X input/output current.

f_{SW} is the switching frequency.

V_{CFLY_RPP} is the peak-to-peak voltage ripple over C_{FLY}.

The switching frequency can be set using the FREQ[2:0] bits in REG0x07 (default value is 500kHz). A lower switching frequency improves efficiency at light load but will also increase voltage/current ripples.

Output Capacitor Design (C_{V2X} or C_{V1X})

The C_{V2X} or C_{V1X} output capacitor selection is similar to the C_{FLY} capacitor selection. More output capacitors result in smaller output voltage ripple. Because of the lower RMS current, the output capacitor value can be much less than the C_{FLY} capacitor, and can be calculated based on the equation below:

$$C_{V1X} = \frac{I_{V1X} t_{DEAD}}{0.5 V_{V1X\_RPP}} \quad (2)$$

$$C_{V2X} = \frac{I_{V2X} t_{DEAD}}{0.5 V_{V2X\_RPP}} \quad (3)$$

where

t_{DEAD} is the dead time between 2 phases (C_{FLY} charging phase: Q_{CHx} and Q_{CLx} turn on; C_{FLY} discharging phase: Q_{DHx} and Q_{DLx} turn on);

V_{V1X_RPP} is the peak-to-peak output voltage ripple which can be set as 2% of V_{V1X};

V_{V2X_RPP} is the peak-to-peak output voltage ripple which can be set as 2% of V_{V2X}.

Considered the bias voltage derating for the capacitors, as the C_{OUT} may be biased to the battery voltage, and this will affect their effective capacitance, two typical 10μF ceramic capacitors with X5R or better grade can be placed as close to the V2X or V1X pins as possible to obtain stable performance.

External Bootstrap Capacitors Selection (C_{BSTxP} and C_{BSTxN})

This bootstrap capacitors, C_{BSTxP} and C_{BSTxN}, provide the gate driver voltage for internal charging phase switching FETs Q_{CHx} and Q_{CLx}. A 47nF low ESR ceramic capacitor is recommended to be connected between the BSTxP pin and the CFxP pin, and between the BSTxN pin and the CFxN pin.

APPLICATION INFORMATION (continued)

PCB Layout Guidelines

For a stable and high-performance design the following guidelines are considered in the design of the PCB layout:

1. Avoid connectors as much as possible to minimize losses and hot spots.
2. Use short and wide traces for high current paths like V1X and V2X.
3. V1X and V2X pins must be bypassed to GND by ceramic capacitors placed as close as possible to these pins.
4. CFLY capacitors must be placed as close as possible to the device pins with minimal copper connection areas to reduce switching noise and EMI.
5. Use symmetrical power traces across the two channels as much as possible. For example, place the CF1P and CF1N symmetrically, and route V1X trace symmetrically on both channels.
6. Vias are inevitable for connection of the inner pins (under the device), especially for BST1P/N, BST2P/N, and HVDD. Use wide and short traces in the connecting layer to connect these pins and minimize the path length to the corresponding capacitors.
7. Use solid (filled) thermal vias for better heat dissipation.
8. Refer or decouple quiet signals to the AGND pin and power signals to the PGND pins (nearest pins).
9. Avoid interrupting or breaking the power planes by signal traces as much as possible.

The recommended layout is illustrated in Figure 17.

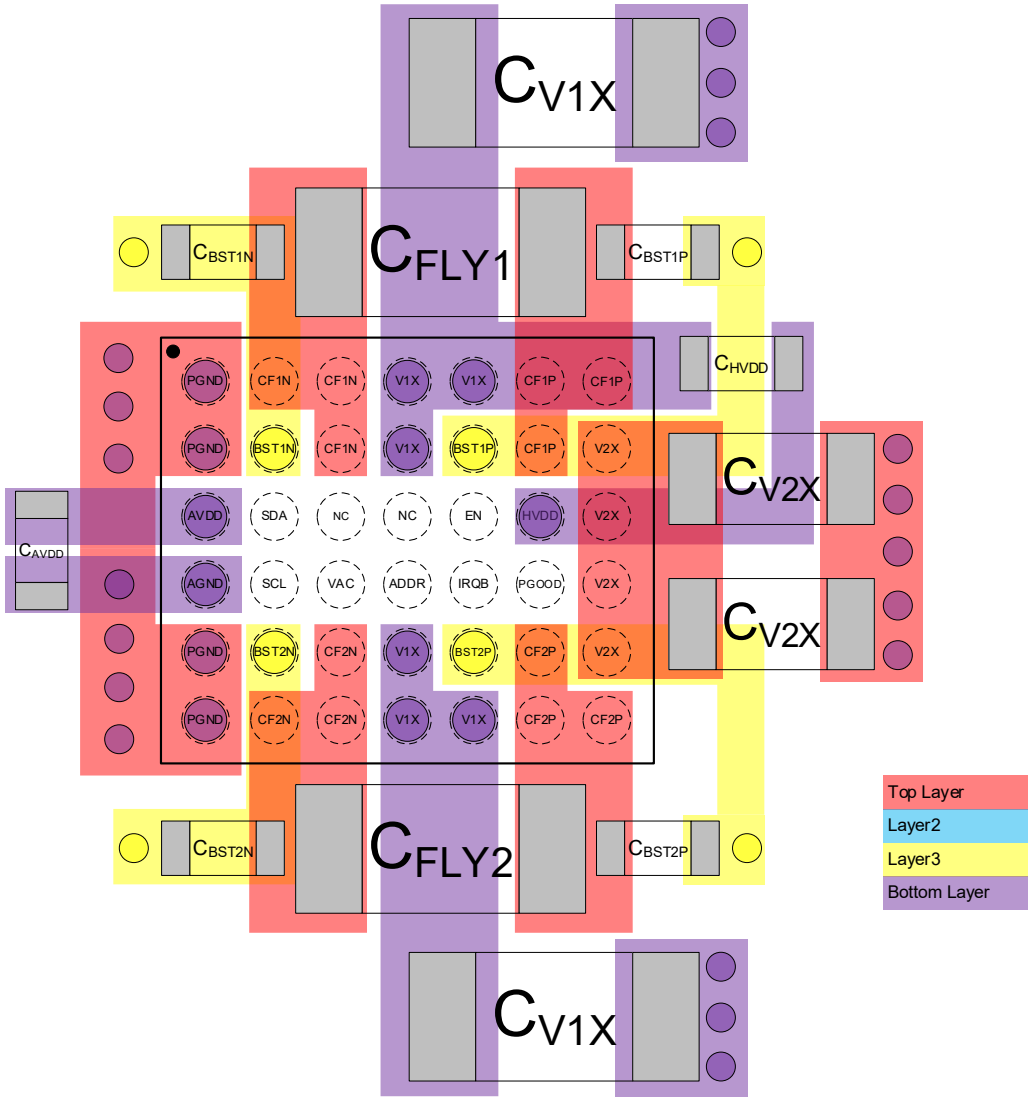


Figure 17. PCB Layout Reference

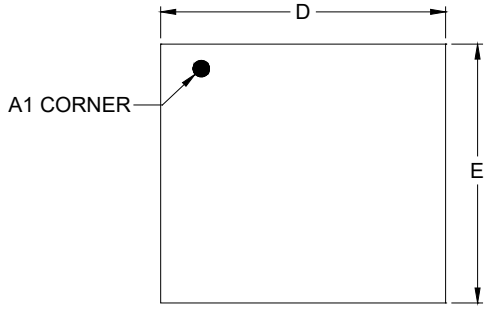
REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

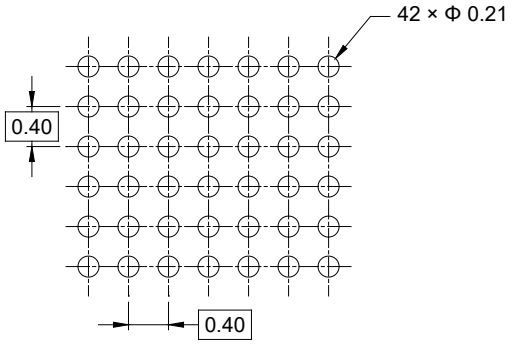
Changes from Original (MAY 2025) to REV.A	Page
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

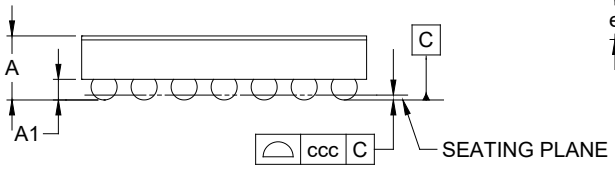
WLCSP-2.85×2.59-42B-A



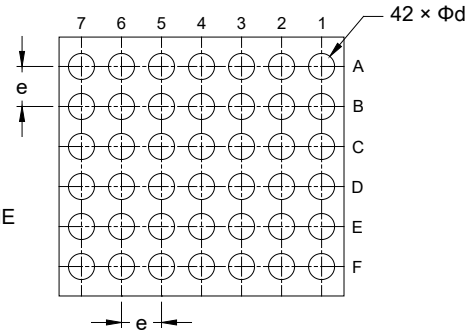
TOP VIEW



RECOMMENDED LAND PATTERN (Unit: mm)



SIDE VIEW



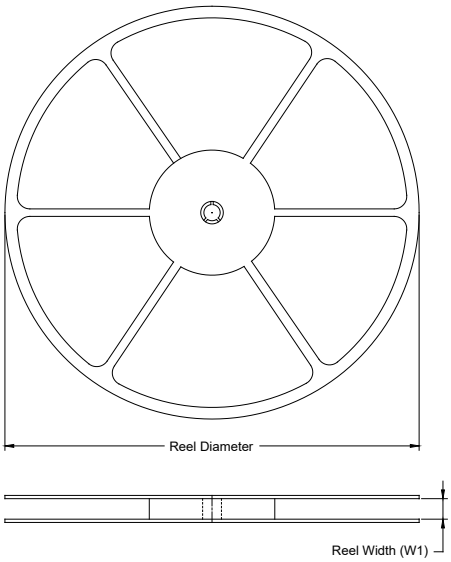
BOTTOM VIEW

Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	-	-	0.678
A1	0.186	-	0.226
D	2.818	-	2.878
E	2.558	-	2.618
d	0.230	-	0.290
e	0.400 BSC		
ccc	0.050		

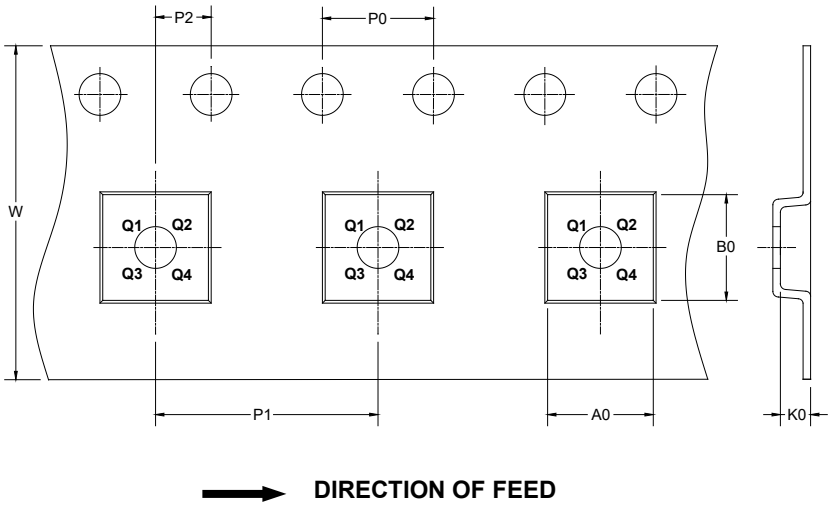
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



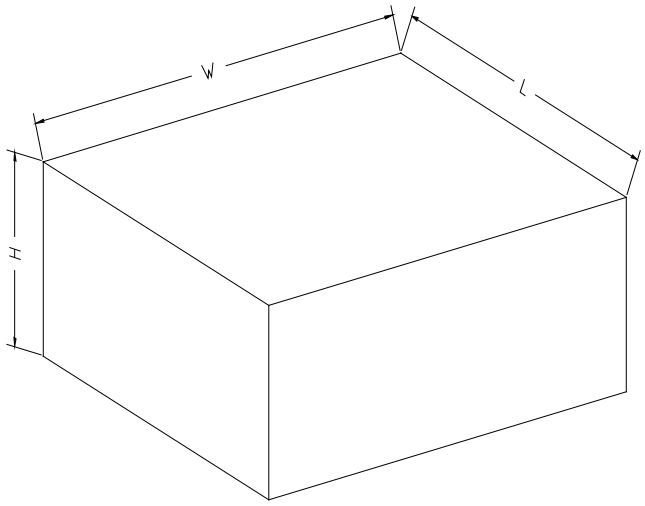
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
WLCSP-2.85×2.59-42B-A	13"	12.4	2.70	3.00	0.80	4.0	8.0	2.0	12.0	Q2

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002