SGM3842
Quad-Output 1A
AMOLED Display Power Supply

GENERAL DESCRIPTION

The SGM3842 is designed for powering AMOLED displays which requires V_{ELVDD}, V_{ELVSS}, V_{AVDD} and V_{DVDD}. The device integrates two Boost converters, VO1 for V_{ELVDD} and VO3 for V_{AVDD}, a dual-phase inverting Buck-Boost converter VO2 for V_{ELVSS} and a Buck converter VO4 for V_{DVDD}. Output voltages of all the four converters can be programmed in digital steps through the digital interface control pins (SWIRE1 & SWIRE2).

The SGM3842 is available in a Green WLCSP-2.5×2.9-42B package.

FEATURES

- **2.9V to 4.8V Input Supply Voltage Range**
- **Synchronous Boost Converter (ELVDD)**
  - **4.6V to 5.2V Output Voltage with 100mV Steps**
  - **4.6V Default Output Voltage**
  - **0.8% Accuracy at 4.6V**
  - **1A Output Current Capability**
  - **Output Voltage Sensing Pin for Path Loss Compensation (FB1)**
- **Synchronous Inverting Buck-Boost Converter (ELVSS)**
  - **-10V to -1.4V Output Voltage with 100mV Steps**
  - **-5.0V Default Output Voltage**
  - **1% Accuracy at -5V**
  - **1A Output Current Capability at -5.4V**
  - **660mA Output Current Capability at -9V**
- **Synchronous Boost Converter (AVDD)**
  - **5.5V to 8.0V Output Voltage with 100mV Steps**
  - **7.0V Default Output Voltage**
  - **0.7% Accuracy at 7.0V**
  - **150mA Output Current Capability**
- **Synchronous Buck Converter (DVDD)**
  - **0.8V to 1.5V Output Voltage with 25mV Steps**
  - **1.2V Default Output Voltage**
  - **1.1% Accuracy at 1.2V**
  - **300mA Output Current Capability**
- **V_{IN} and V_{OUT} Bi-Directional Isolation**
- **Short Circuit Protection (SCP)**
- **Overload Protection**
- **Thermal Shutdown**
- **V_{ELVSS} Start-Up Delay: 6ms**
- **Short Circuit and OLP Detection Time: 1.2ms**
- **Available in a Green WLCSP-2.5×2.9-42B Package**

APPLICATIONS

Smartphones & Tablets
Active Matrix OLED Displays

TYPICAL APPLICATION

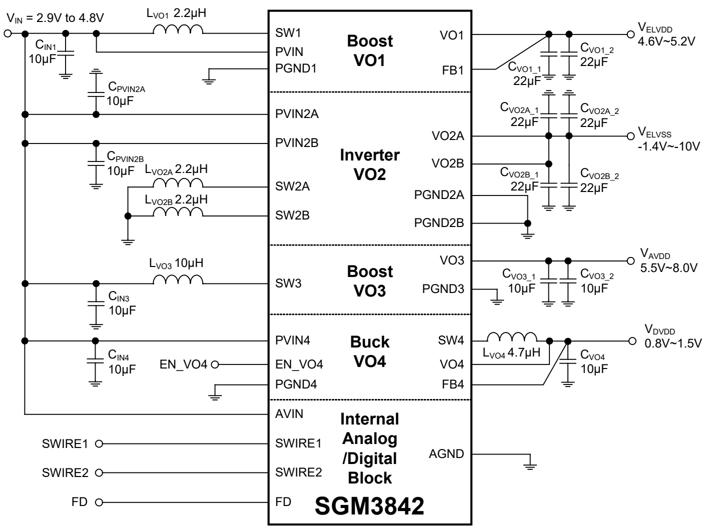


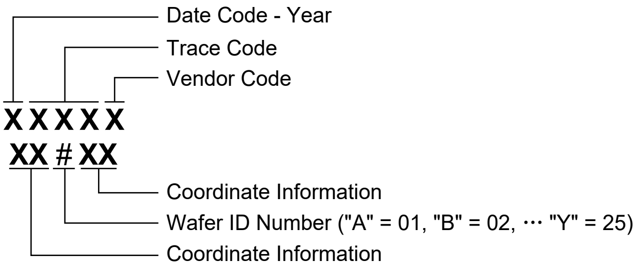
Figure 1. Typical Application Circuit

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM3842	WLCSP-2.5×2.9-42B	-40℃ to +85℃	SGM3842YG/TR	SGM 3842 XXXXX XX#XX	Tape and Reel, 5000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code. XX#XX = Coordinate Information and Wafer ID Number.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Voltage Range (with Respect to Ground Pin)
AVIN, PVIN, PVIN2A, PVIN2B, PVIN4, EN_VO4, SWIRE1, SWIRE2, FD, VO1, VO4, FB1, FB4 Voltages ...... -0.3V to 6V
SW1, SW4 Voltage .... -0.3V to 6V
SW1, SW4 Voltage (Transient: 10ns) .... -1V to 8V
SW3, VO3 Voltages... -0.3V to 10V
SW3 Voltage (Transient: 10ns)............................. -1V to 12V
VO2A, VO2B Voltages....................................... -12V to 0.3V
SW2A, SW2B Voltages .... -12V to 6V
SW2A, SW2B Voltage (Transient: 10ns)............... -14V to 8V
Package Thermal Resistance
WLCSP-2.5×2.9-42B, θ_{JA}....................................... 28℃/W
WLCSP-2.5×2.9-42B, θ_{JB}...................................... 7.3℃/W
WLCSP-2.5×2.9-42B, θ_{JC} .... 1.9℃/W
Junction Temperature...+150℃
Storage Temperature Range .... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ....+260℃
ESD Susceptibility
HBM...2000V
CDM 1000V

RECOMMENDED OPERATING CONDITIONS

Operating Ambient Temperature Range .... -40℃ to +85℃
Operating Junction Temperature Range ...... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

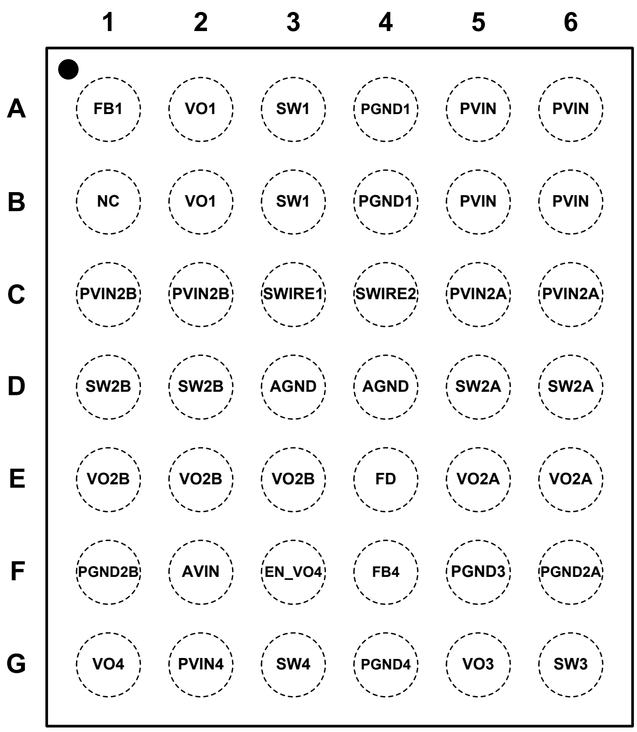
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

(TOP VIEW)



WLCSP-2.5×2.9-42B

PIN DESCRIPTION

PIN	NAME	TYPE	FUNCTION
A1	FB1	I	VO1 Boost Converter Output Sense Input.
A2, B2	VO1	P	VO1 Boost Converter Output.
A3, B3	SW1	P	VO1 Boost Converter Switching Node.
A4, B4	PGND1	G	VO1 Boost Converter Power Ground.
A5, A6 B5, B6	PVIN	P	Power Supply Input Pin.
B1	NC	—	No Connection.
C1, C2	PVIN2B	P	VO2 Inverting Buck-Boost Converter Phase B Power Supply Input Pin.
C3	SWIRE1	I	VO1/VO2 Converter Enable and Voltage Programming Pin.
C4	SWIRE2	I	VO3 Converter Enable and VO3/VO4 Voltage Programming Pin.
C5, C6	PVIN2A	P	VO2 Inverting Buck-Boost Converter Phase A Power Supply Input Pin.
D1, D2	SW2B	P	VO2 Inverting Buck-Boost Converter Phase B Switching Node.
D3, D4	AGND	G	Analog Ground Pin.

PIN DESCRIPTION (continued)

PIN	NAME	TYPE	FUNCTION
D5, D6	SW2A	P	VO2 Inverting Buck-Boost Converter Phase A Switching Node.
E1, E2, E3	VO2B	P	VO2 Inverting Buck-Boost Converter Phase B Output Pin.
E4	FD	I	Fast Discharge Enable Pin. FD = High: Enable Fast Discharge for VO1, VO2, VO3, and VO4. FD = Low: Disable Fast Discharge for VO1, VO2, VO3, and VO4.
E5, E6	VO2A	P	VO2 Inverting Buck-Boost Converter Phase A Output Pin.
F1	PGND2B	G	VO2 Inverting Buck-Boost Converter Phase B Power Ground Pin.
F2	AVIN	P	Analog Input Pin.
F3	EN_VO4	I	VO4 Buck Converter Enable Pin.
F4	FB4	I	VO4 Buck Converter Output Sense Input.
F5	PGND3	G	VO3 Boost Converter Power Ground Pin.
G4	PGND4	G	VO4 Buck Converter Power Ground Pin.
F6	PGND2A	G	VO2 Inverting Buck-Boost Converter Phase A Power Ground Pin.
G1	VO4	P	VO4 Buck Converter Output.
G2	PVIN4	P	VO4 Buck Converter Power Supply Input Pin.
G3	SW4	P	VO4 Buck Converter Switching Node.
G5	VO3	P	VO3 Boost Converter Output.
G6	SW3	P	VO3 Boost Converter Switching Node.

NOTE: I = input, P = power, G = ground.

ELECTRICAL CHARACTERISTICS

(At T_J = +25℃, V_{IN} = 3.7V, V_{SWIRE1} = V_{SWIRE2} = V_{EN_VO4} = V_{IN}, V_{VO1} = 4.6V, V_{VO2} = -5V, V_{VO3} = 7V, V_{VO4} = 1.2V, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Current and Thermal Protection							
Input Voltage Range	V_{IN}	T_J = -40℃ to +85℃		2.9		4.8	V
Shutdown Current into PVIN, AVIN	I_{SD}	V_{SWIRE1} = V_{SWIRE2} = V_{EN_VO4} = GND			0.6	1.0	μA
Quiescent Current into PVIN, AVIN	I_{QON}	V_{IN} = 3.7V, no load, V_{SWIRE1} = V_{SWIRE2} = V_{EN_VO4} = high			6.2		mA
Under-Voltage Lockout Threshold (AVIN)	V_{IT-}	V_{IN} falling			2.27		V
	V_{IT+}	V_{IN} rising			2.37	2.495	
Thermal Shutdown Temperature	T_{SD}	Junction temperature rising			145		℃
		Junction temperature falling			135		
Logic Signals (SWIRE1, SWIRE2, EN_VO4)							
Logic High Level Voltage	V_H	V_{IN} = 2.9V to 4.8V, T_J = -40℃ to +85℃		1.0			V
Logic Low Level Voltage	V_L	V_{IN} = 2.9V to 4.8V, T_J = -40℃ to +85℃				0.4	V
Pull-Down Resistor (SWIRE1, SWIRE2, EN_VO4)	R_{DOWN}				530		kΩ
Boost Converter (V_{VO1} = V_{ELVDD})							
Positive Output 1 Voltage	V_{VO1}	4.6V to 5.2V with 0.1V/step, default 4.6V, T_J = -40℃ to +85℃		4.6	4.6	5.2	V
Positive Output 1 Voltage Accuracy		V_{VO1} = 4.6V, no load, T_J = 25℃		-0.6		0.6	%
		V_{VO1} = 4.6V, no load, T_J = -40℃ to +85℃		-0.8		0.8	
SW1 MOSFET On-Resistance	$R_{DS(ON)11}$	I_{DS} = 200mA			60		mΩ
SW1 MOSFET Rectifier On-Resistance	$R_{DS(ON)12}$	I_{DS} = 200mA			145		
SW1 Switch Current Limit	I_{SW1}	Inductor valley current		1.86	2.45	3.00	A
SW1 Switching Frequency	f_{SW1}	I_{VO1} = 100mA		1.1	1.3	1.5	MHz
Output Current Capability	I_{VO1}	V_{IN} = 2.9V to 4.8V		1000			mA
Short Circuit Threshold in Operation	$V_{VO1(SCP)}$	Percentage of nominal V_{VO1}		63	76	88	%
Threshold of Output Sense with VO1	V_{TVO1}	V_{VO1} - V_{FB1} increasing			600		mV
Threshold of Output Sense with FB1	V_{TFB1}	V_{VO1} - V_{FB1} decreasing			440		mV
VO1 and FB1 Leakage, No Discharge	I_{LEAK_VO1}	V_{FD} = GND, V_{SWIRE1} = V_{SWIRE2} = GND			0.6	2	μA
Pull-Down Resistance of FB1	R_{FB1}				4		MΩ
VO1 Discharge Resistance	$R_{VO1(DCG)}$	V_{SWIRE1} = V_{SWIRE2} = GND, I_{VO1} = 20mA			57		Ω
VO1 Discharge Time	t_{DVO1}	V_{SWIRE1} = V_{SWIRE2} = GND			3		ms
Efficiency	$Eff_{VO1\text{-}VO2}$	V_{IN} = 3.7V, V_{VO1} = 4.6V, V_{VO2} = -4.0V, I_{VO1_VO2} = 100mA to 200mA			92.3		%
		V_{IN} = 3.7V, V_{VO1} = 4.6V, V_{VO2} = -7.4V, I_{VO1_VO2} = 300mA			90.7		
		V_{IN} = 3.7V, V_{VO1} = 4.6V, V_{VO2} = -9.0V, I_{VO1_VO2} = 450mA			89.2		
Line Transient	$VO1_{LINETRA}$	ΔV_{IN} = 0.5V, t_R = t_F = 10μs, I_{VO1} = 300mA	Undershoot		16		mV
			Overshoot		16		
Line Regulation	$VO1_{LINEREG}$	I_{VO1} = 100mA, V_{IN} = 2.9V to 4.8V			0.055		%/V
		No load, V_{IN} = 2.9V to 4.8V			0.06		
Output Voltage Ripple	$VO1_{RIPPLE}$	I_{VO1_VO2} = 0 to 1A			30		mV_{PP}
Load Transient	$VO1_{LOADTRA}$	ΔI_{VO1} = 10mA to 1A, t_R = t_F = 8ms	Undershoot		20		mV
			Overshoot		20		
		ΔI_{VO1} = 10mA to 600mA, t_R = t_F = 8ms	Undershoot		13		
			Overshoot		13		

ELECTRICAL CHARACTERISTICS (continued)

(At T_J = +25℃, V_{IN} = 3.7V, V_{SWIRE1} = V_{SWIRE2} = V_{EN_VO4} = V_{IN}, V_{VO1} = 4.6V, V_{VO2} = -5V, V_{VO3} = 7V, V_{VO4} = 1.2V, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Load Regulation	$VO1_{LOADREG}$	0mA ≤ I_{VO1} ≤ 1A, V_{IN} = 2.9V to 4.5V			6		mV
		0mA ≤ I_{VO1} ≤ 1A, V_{IN} = 4.5V to 4.8V			1		
Buck-Boost Converter (V_{VO2} = V_{ELVSS})							
Negative Output Voltage Range	V_{VO2}	-10V to -1.4V with 0.1V/step, default -5.0V, T_J = -40℃ to +85℃		-10	-5	-1.4	V
Negative Output Voltage Accuracy		V_{VO2} = -5V, no load, T_J = 25℃		-30		30	mV
		V_{VO2} = -5V, no load, T_J = -40℃ to +85℃		-50		50	
		V_{VO2} = -9V, no load, T_J = 25℃		-60		60	
		V_{VO2} = -9V, no load, T_J = -40℃ to +85℃		-100		100	
SW2 MOSFET On-Resistance-Phase A	$R_{DS(ON)A1}$	I_{DS} = 200mA			130		mΩ
SW2 MOSFET Rectifier On-Resistance-Phase A	$R_{DS(ON)A2}$	I_{DS} = 200mA			120		
SW2 MOSFET On-Resistance-Phase B	$R_{DS(ON)B1}$	I_{DS} = 200mA			130		mΩ
SW2 MOSFET Rectifier On-Resistance-Phase B	$R_{DS(ON)B2}$	I_{DS} = 200mA			120		
SW2 Switching Frequency	f_{SW2}	I_{VO2} = 100mA		1.0	1.2	1.4	MHz
Output Current Capability	I_{VO2}	V_{IN} = 2.9V to 4.8V, V_{VO2} = -5.4V		1000			mA
		V_{IN} = 2.9V to 4.8V, V_{VO2} = -9V		660			
SW2 Switch Current Limit-Phase A	I_{SW2A}	Inductor peak current		2.0	3.1	4.1	A
SW2 Switch Current Limit-Phase B	I_{SW2B}	Inductor peak current		2.0	3.1	4.1	A
Average Load Current Threshold with Dual-Phase	$I_{RMSA\&B}$	Load current rising			240		mA
Average Load Current Threshold with Phase A Only	I_{RMSA}	Load current falling			160		mA
Short Circuit Threshold in Operation	$V_{VO2(SCP)}$	Percentage of nominal V_{VO2}		58	71	83	%
VO2 Discharge Resistance	$R_{VO2(DCG)}$	V_{SWIRE1} = V_{SWIRE2} = GND, I_{VO2} = 20mA			160		Ω
VO2 Discharge Time	t_{DVO2}	V_{SWIRE1} = V_{SWIRE2} = GND			15		ms
VO2 Leakage, No Discharge	I_{LEAK_VO2}	V_{FD} = GND, V_{SWIRE1} = V_{SWIRE2} = GND			1	2	μA
Output Voltage Ripple	$VO2_{RIPPLE}$	I_{VO1_VO2} = 0 to 1A			20		mV_{PP}
Line Transient	$VO2_{LINETRA}$	$ΔV_{IN}$ = 0.5V, t_R = t_F = 10μs, I_{VO2} = 300mA	Undershoot		17		mV
			Overshoot		17		
Line Regulation	$VO2_{LINEREG}$	I_{VO2} = 100mA, V_{IN} = 2.9V to 4.8V			0.07		%/V
Load Transient	$VO2_{LOADTRA}$	$ΔI_{VO2}$ = 10mA to 1A, t_R = t_F = 8ms	Undershoot		30		mV
			Overshoot		30		
Load Regulation	$VO2_{LOADREG}$	0mA ≤ I_{VO2} ≤ 1A			0.2		%/A
Boost Converter (V_{VO3} = V_{AVDD})							
Positive Output 3 Voltage Range	V_{VO3}	5.5V to 8.0V with 0.1V/step, default 7V, T_J = -40℃ to +85℃		5.5	7.0	8.0	V
Positive Output 3 Voltage Accuracy		V_{VO3} = 7V, no load, T_J = -40℃ to +85℃		-0.7		0.7	%
SW3 MOSFET On-Resistance	$R_{DS(ON)31}$	I_{DS} = 200mA			470		mΩ
SW3 MOSFET Rectifier On-Resistance	$R_{DS(ON)32}$	I_{DS} = 200mA			550		
SW3 Switch Current Limit	I_{SW3}	Inductor peak current		0.71	1.05	1.38	A
SW3 Switching Frequency	f_{SW3}	I_{VO3} = 30mA		1.1	1.3	1.5	MHz
Output Current Capacity	I_{VO3}	V_{IN} = 2.9V to 4.8V		150			mA
Short Circuit Threshold in Operation	$V_{VO3(SCP)}$	Percentage of nominal V_{VO3}		81	87	93	%

ELECTRICAL CHARACTERISTICS (continued)

(At T_J = +25℃, V_{IN} = 3.7V, V_{SWIRE1} = V_{SWIRE2} = V_{EN_VO4} = V_{IN}, V_{VO1} = 4.6V, V_{VO2} = -5V, V_{VO3} = 7V, V_{VO4} = 1.2V, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
VO3 Leakage, No Discharge	I_{LEAK_VO3}	V_{FD} = GND, V_{SWIRE2} = GND			1.5	3	μA
VO3 Discharge Resistance	$R_{VO3(DCG)}$	V_{SWIRE2} = GND, I_{VO3} = 20mA			260		Ω
VO3 Discharge Time	t_{DVO3}	V_{SWIRE2} = GND			7		ms
Efficiency	Eff_{VO3}	V_{IN} = 3.7V, I_{VO3} = 5mA to 25mA			92.9		%
		V_{IN} = 3.7V, I_{VO3} = 25mA to 150mA			93.8		%
Output Voltage Ripple	$VO3_{RIPPLE}$	I_{VO3} = 0 to 150mA			25		mV_{PP}
Line Transient	$VO3_{LINETRA}$	ΔV_{IN} = 0.5V, t_R = t_F = 10μs, I_{VO3} = 30mA	Undershoot		18		mV
			Overshoot		18		
Line Regulation	$VO3_{LINEREG}$	I_{VO3} = 100mA, V_{IN} = 2.9V to 4.8V			0.025		%/V
Load Transient	$VO3_{LOADTRA}$	ΔI_{VO3} = 50mA, t_R = t_F = 10μs, V_{IN} = 3.8V	Undershoot		40		mV
			Overshoot		40		
Load Regulation	$VO3_{LOADREG}$	0mA ≤ I_{VO3} ≤ 150mA			0.25		%/A
Buck Converter (V_{VO4} = V_{DVDD})							
Positive Output 4 Voltage Range	V_{VO4}	0.8V to 1.5V with 25mV/step, default 1.2V, T_J = -40℃ to +85℃		0.8	1.2	1.5	V
Positive Output 4 Voltage Accuracy		V_{VO4} = 1.2V, no load, T_J = -40℃ to +85℃		-1.1		1.1	%
SW4 MOSFET On-Resistance	$R_{DS(ON)41}$	I_{DS} = 200mA			340		mΩ
SW4 MOSFET Rectifier On-Resistance	$R_{DS(ON)42}$	I_{DS} = 200mA			270		
SW4 Switch Current Limit	I_{SW4}	Inductor peak current		0.76	1.05	1.32	A
SW4 Switching Frequency	f_{SW4}	I_{VO4} = 30mA, PWM Mode		1.1	1.3	1.5	MHz
Output Current Capacity	I_{VO4}	V_{IN} = 2.9V to 4.8V, T_J = -40℃ to +85℃		300			mA
Short Circuit Threshold in Operation	$V_{VO4(SCP)}$	Percentage of nominal V_{VO4}		74	82	90	%
VO4 Leakage, No Discharge	I_{LEAK_VO4}	V_{FD} = GND, V_{SWIRE2} = GND			0.02	1	μA
VO4 Discharge Resistance	$R_{VO4(DCG)}$	V_{SWIRE2} = GND, I_{VO4} = 20mA			170		Ω
VO4 Discharge Time	t_{DVO4}	V_{SWIRE2} = GND			3		ms
Efficiency	Eff_{VO4}	V_{IN} = 3.7V, V_{VO4} = 1.2V, I_{VO4} = 60mA to 100mA			91.4		%
Output Voltage Ripple	$VO4_{RIPPLE}$	I_{VO4} = 300mA			4		mV_{PP}
Line Transient	$VO4_{LINETRA}$	ΔV_{IN} = 0.5V, t_R = t_F = 10μs, I_{VO4} = 200mA	Undershoot		3		mV
			Overshoot		3		
Line Regulation	$VO4_{LINEREG}$	I_{VO4} = 60mA to 100mA, V_{IN} = 2.9V to 4.8V			0.015		%/V
Load Transient	$VO4_{LOADTRA}$	ΔI_{VO4} = 300mA, t_R = t_F = 10μs, V_{IN} = 3.8V	Undershoot		45		mV
			Overshoot		45		
Load Regulation	$VO4_{LOADREG}$	0mA ≤ I_{VO4} ≤ 300mA			1		mV

TIMING REQUIREMENTS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Short Circuit Timer					
VO1 Short Circuit Detection Time in Start-Up	$t_{VO1(SCP)}$	2.10	2.76	3.50	ms
VO1 Short Circuit Detection Time in Operation		0.90	1.20	1.50	
VO2 Short Circuit Detection Time in Start-Up	$t_{VO2(SCP)}$	6.30	7.48	9.00	
VO2 Short Circuit Detection Time in Operation		0.90	1.20	1.50	
VO3 Short Circuit Detection Time in Start-Up	$t_{VO3(SCP)}$		3.7		
VO3 Short Circuit Detection Time in Operation		0.90	1.20	1.50	
VO4 Short Circuit Detection Time in Start-Up	$t_{VO4(SCP)}$		3.7		
VO4 Short Circuit Detection Time in Operation		0.90	1.20	1.50	
SWIRE1 & SWIRE2 Interface					
Initialization Time	t_{INIT}		400	490	μs
Shutdown Time Period	t_{OFF}	50	63	80	
Pulse High Level Time Period	t_{HIGH}	2	10	20	
Pulse Low Level Time Period	t_{LOW}	2	10	20	
Data Storage/Accept Time Period	t_{STORE}	50	63	80	
Power Sequence					
VO1 Start-Up Time	t_{SS1}		3.2		ms
VO2 Start-Up Time	t_{SS2}		2.6		
VO2 Start-Up Time Delay after VO1	t_{DELAY}		2.8		
VO3 Start-Up Time	t_{SS3}		1.8		
VO4 Start-Up Time	t_{SS4}		1.2		

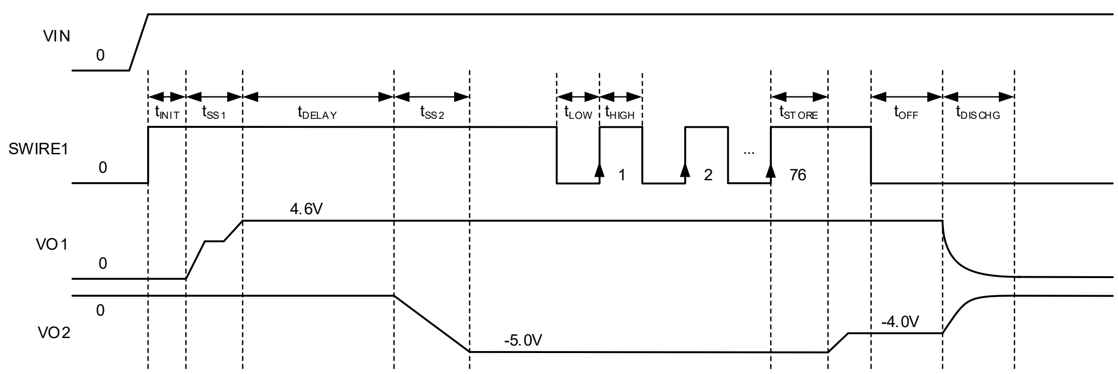


Figure 2. VO1/VO2 Timing Diagram

TIMING DIAGRAMS

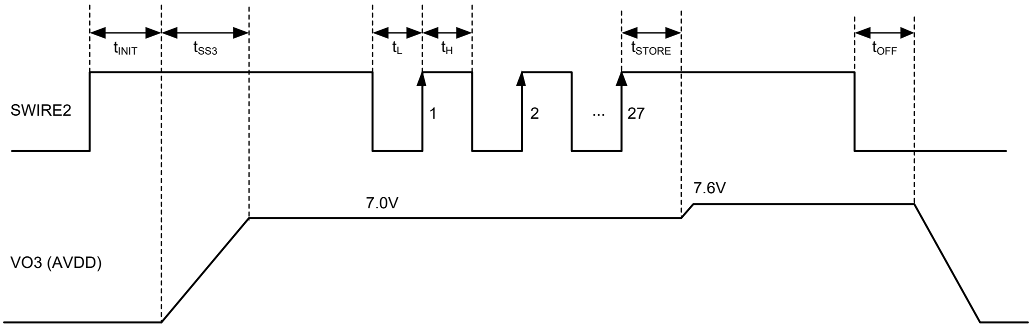


Figure 3. VO3 Timing Diagram

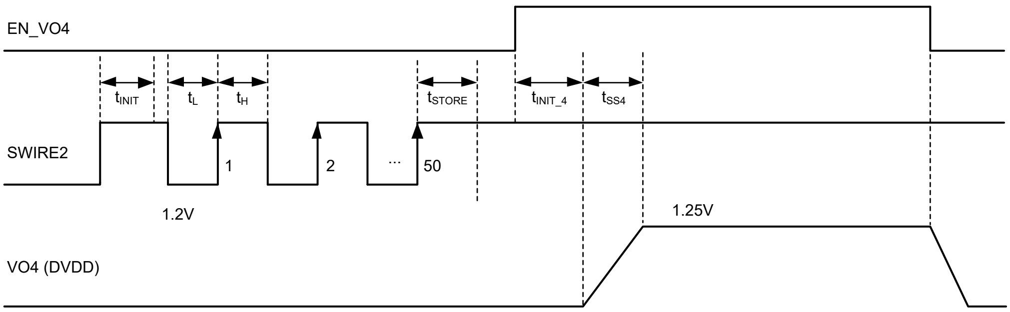


Figure 4. VO4 Timing Diagram 1

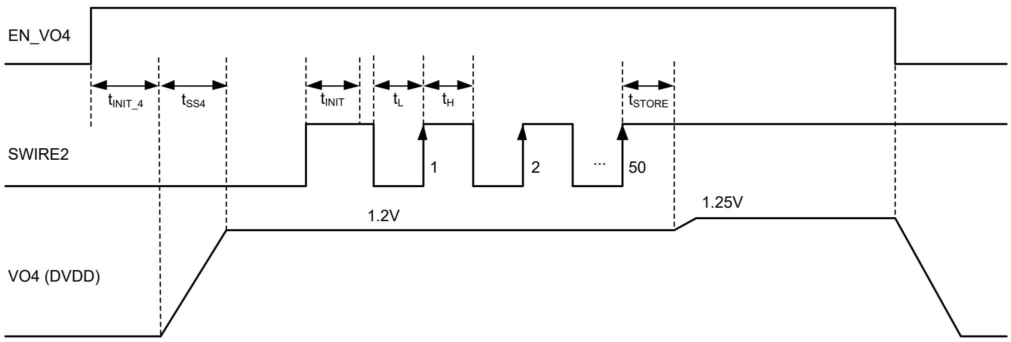
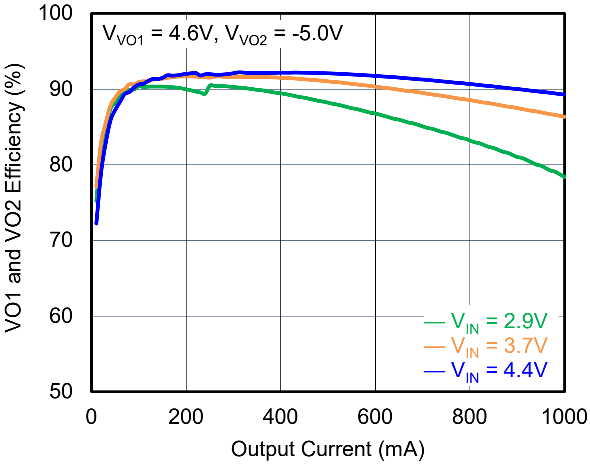


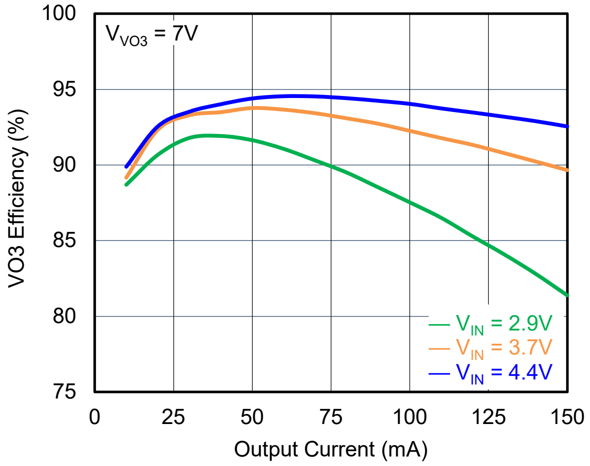
Figure 5. VO4 Timing Diagram 2

TYPICAL PERFORMANCE CHARACTERISTICS

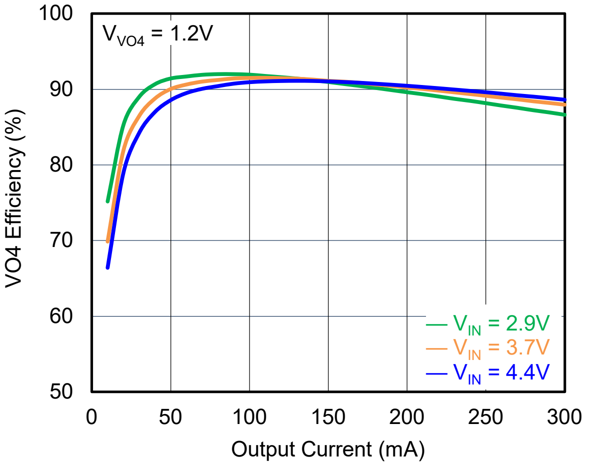
VO1 and VO2 Combined Efficiency vs. Output Current



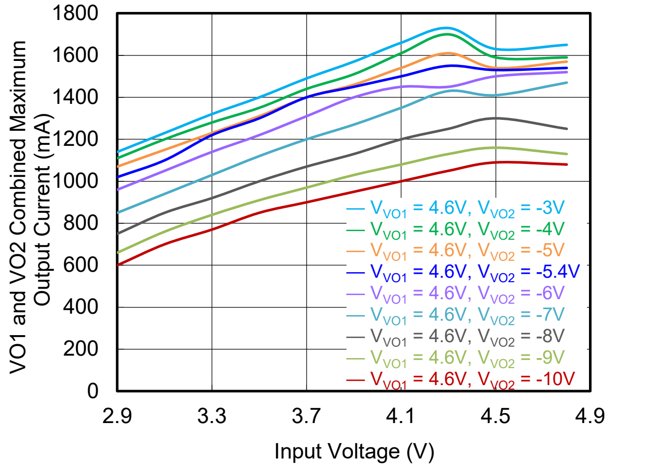
VO3 Efficiency vs. Output Current



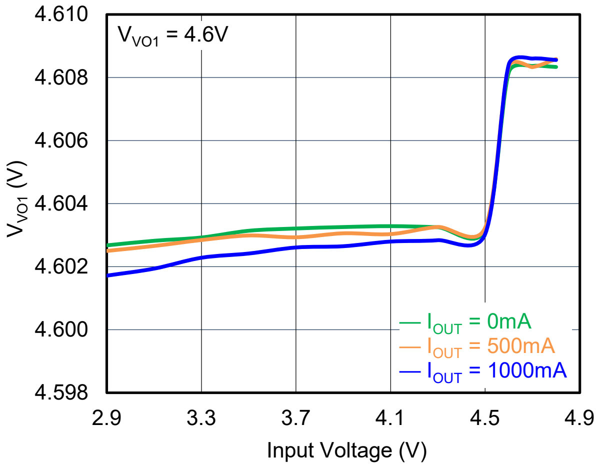
VO4 Efficiency vs. Output Current



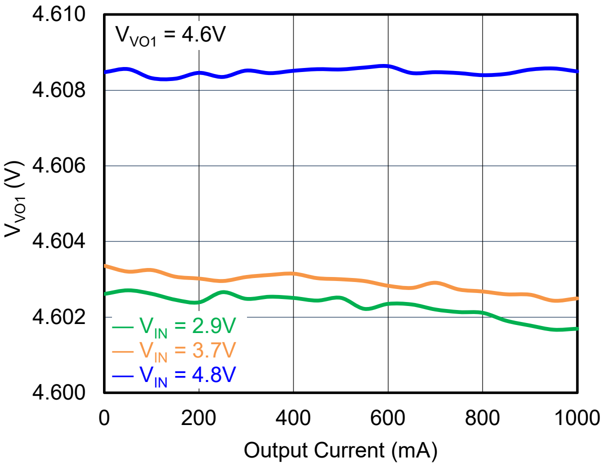
VO1 and VO2 Combined Maximum Output Current vs. Input Voltage



V_{VO1} Line Regulation

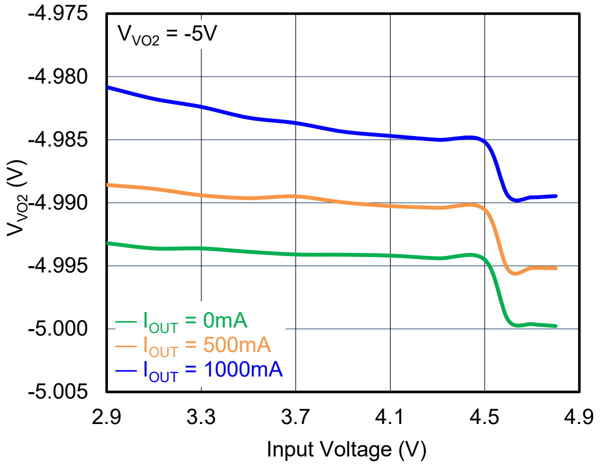


V_{VO1} Load Regulation

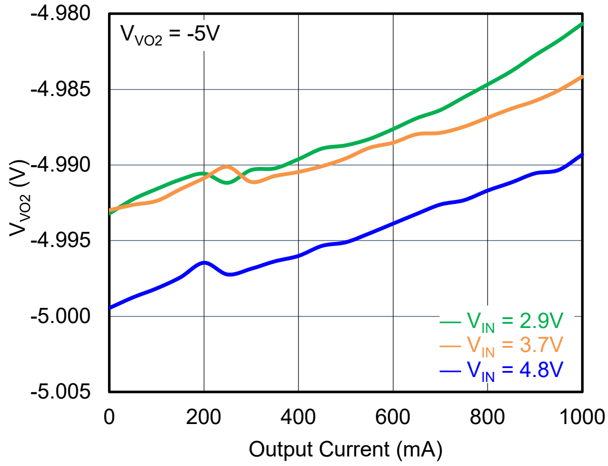


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

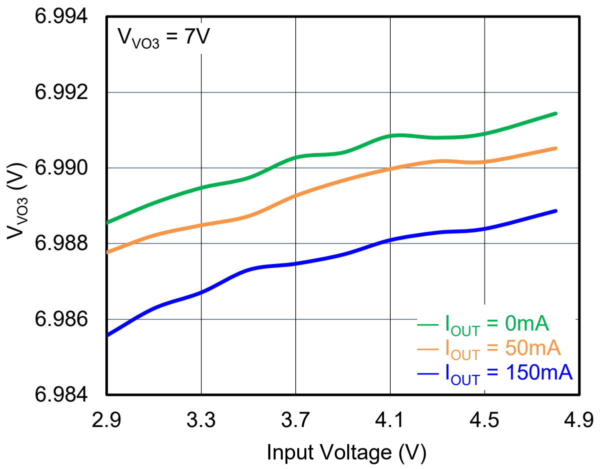
V_{VO2} Line Regulation



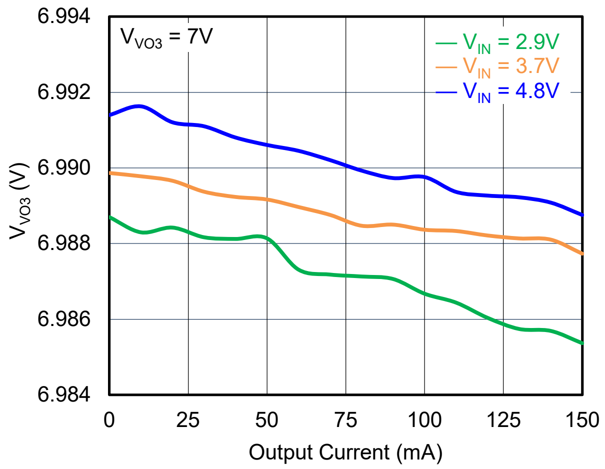
V_{VO2} Load Regulation



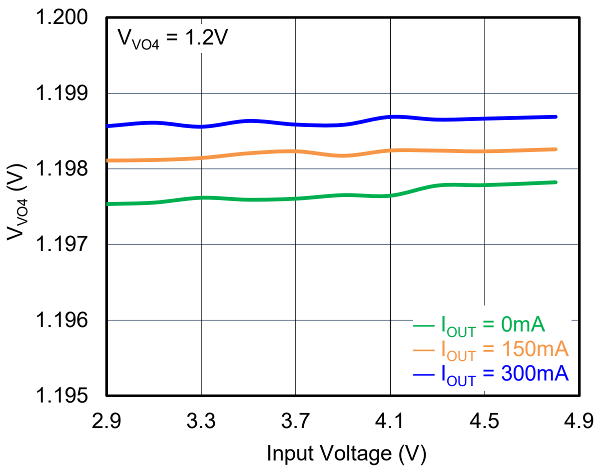
V_{VO3} Line Regulation



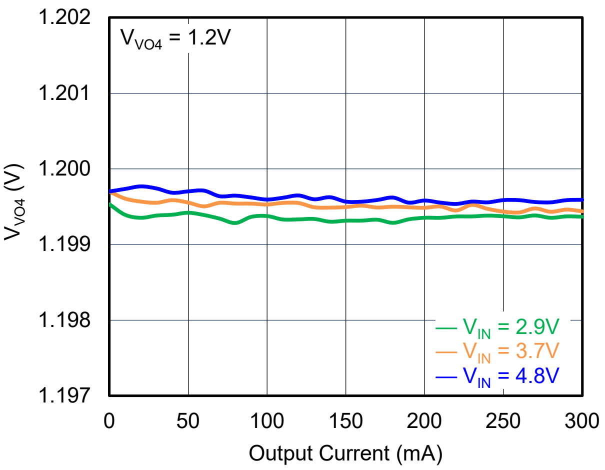
V_{VO3} Load Regulation



V_{VO4} Line Regulation

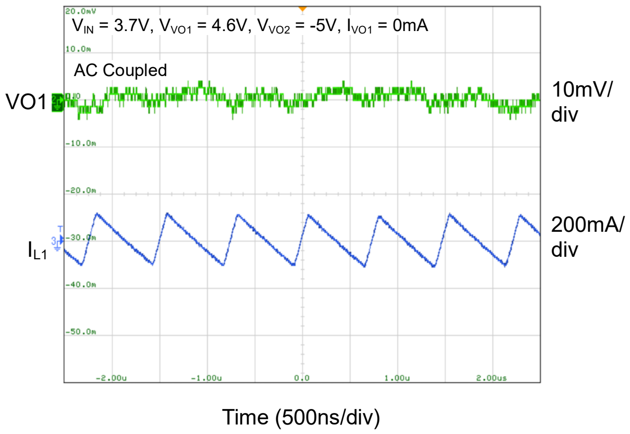


V_{VO4} Load Regulation

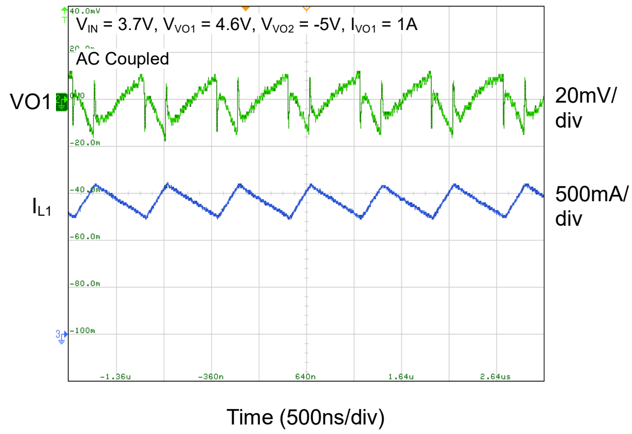


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

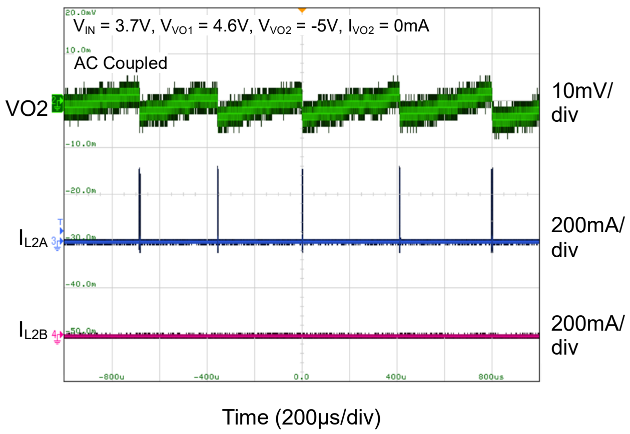
VO1 Output Voltage Ripple at No Load



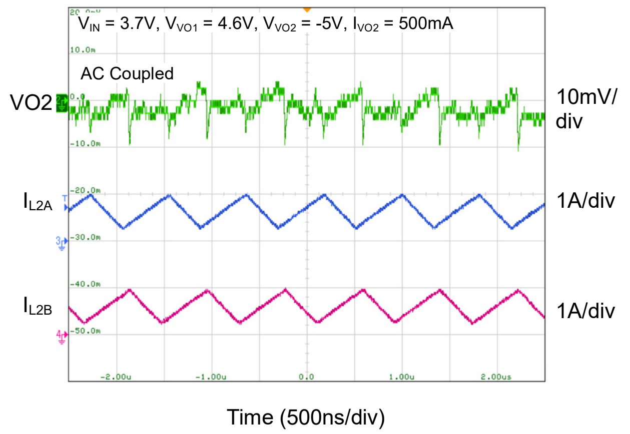
VO1 Output Voltage Ripple at Heavy Load



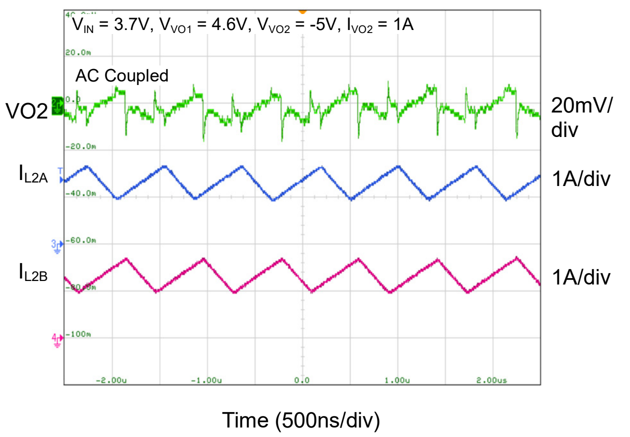
VO2 Output Voltage Ripple at No Load



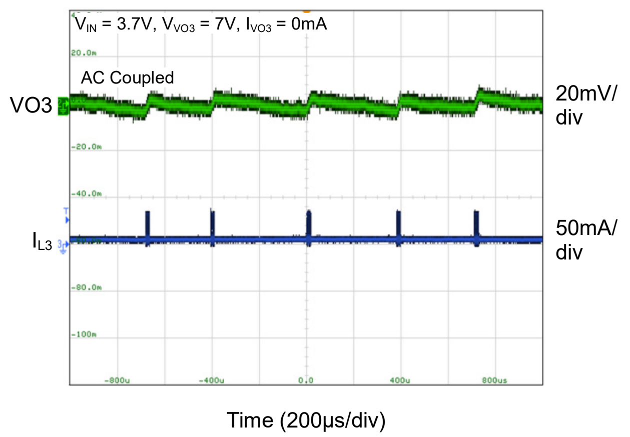
VO2 Output Voltage Ripple at Moderate Load



VO2 Output Voltage Ripple at Heavy Load

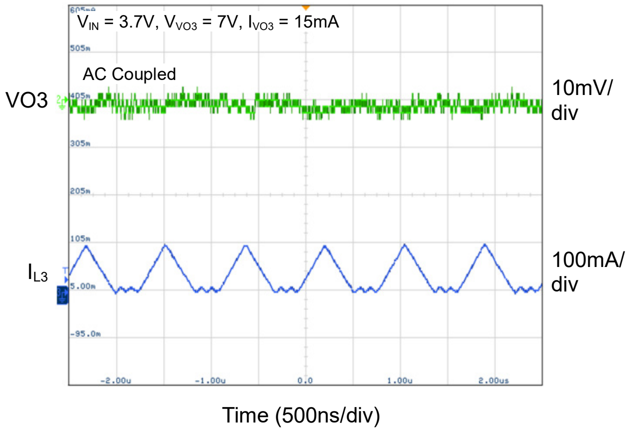


VO3 Output Voltage Ripple at No Load

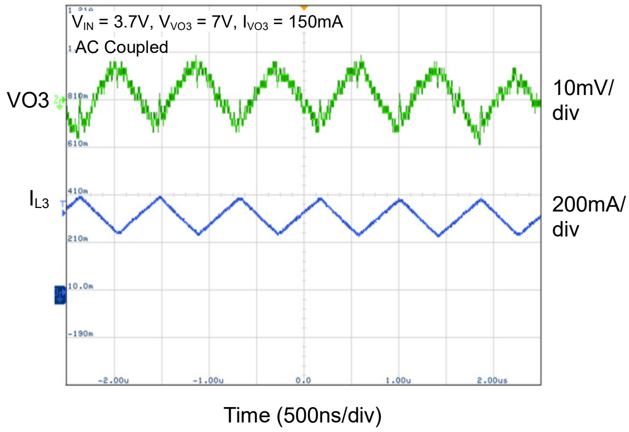


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

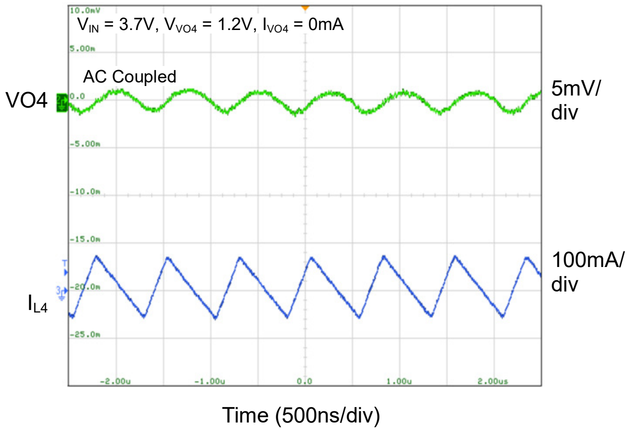
VO3 Output Voltage Ripple at Light Load



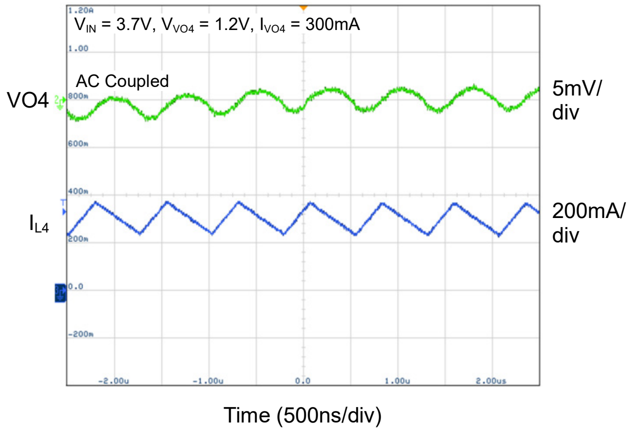
VO3 Output Voltage Ripple at Heavy Load



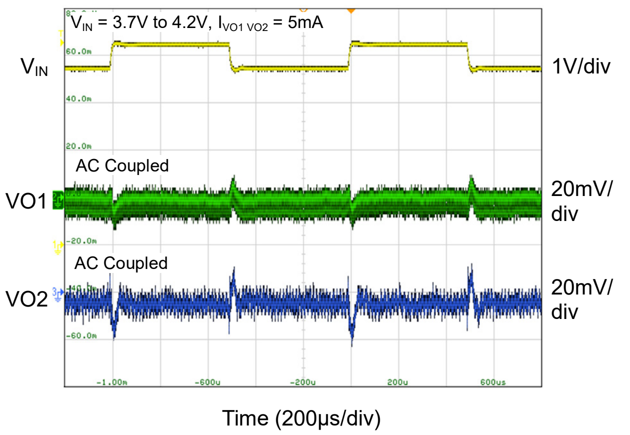
VO4 Output Voltage Ripple at No Load



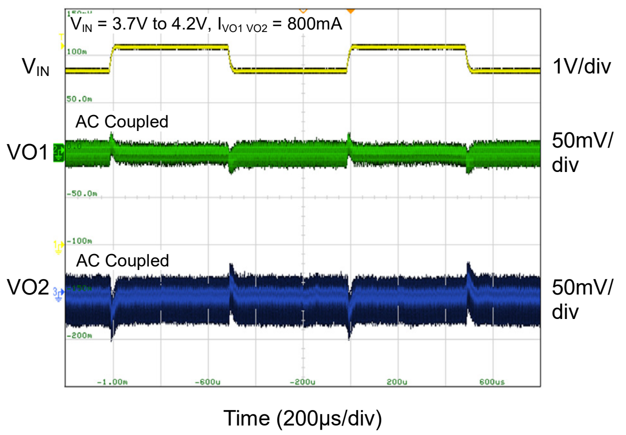
VO4 Output Voltage Ripple at Heavy Load



VO1 and VO2 Line Transient at Light Load

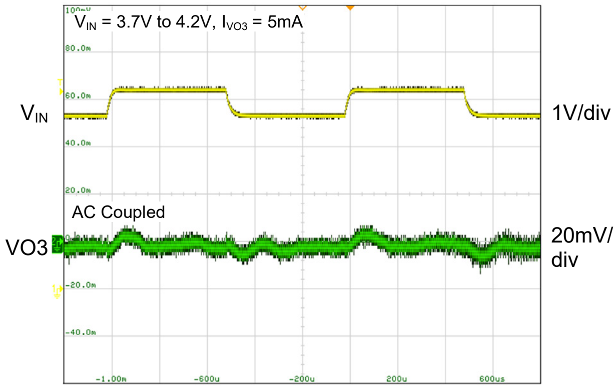


VO1 and VO2 Line Transient at Heavy Load



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

VO3 Line Transient at Light Load

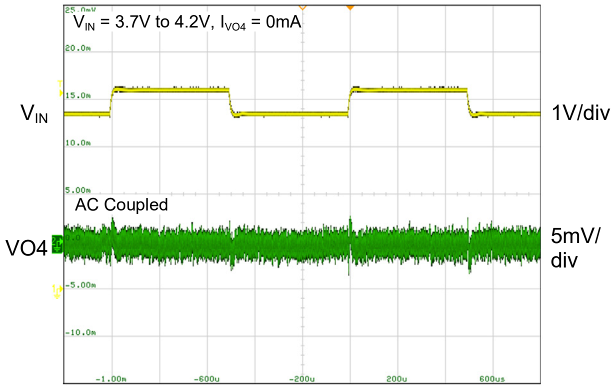


Time (200μs/div)

VO3 Line Transient at Heavy Load

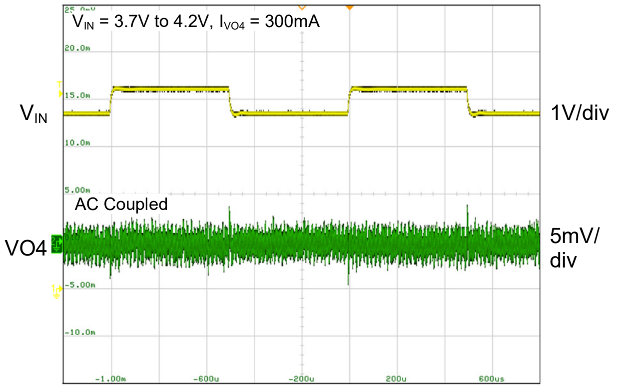
Time (200μs/div)

VO4 Line Transient at No Load



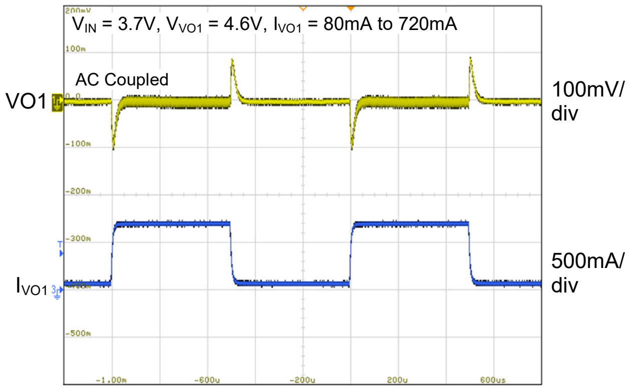
Time (200μs/div)

VO4 Line Transient at Heavy Load



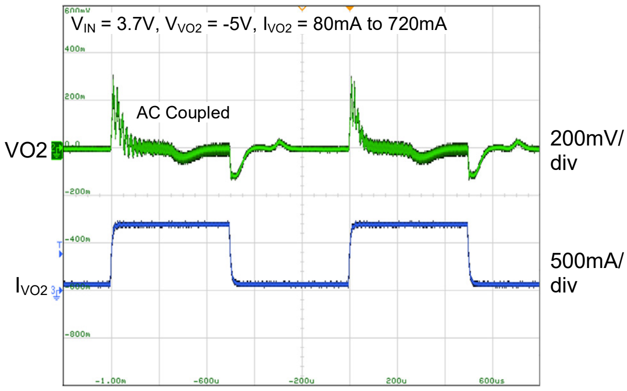
Time (200μs/div)

VO1 Load Transient



Time (200μs/div)

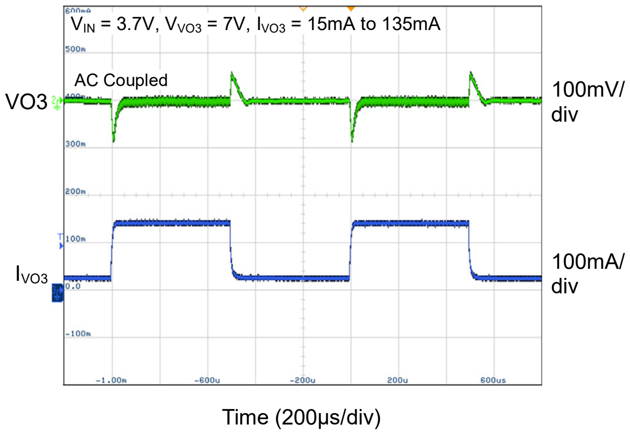
VO2 Load Transient



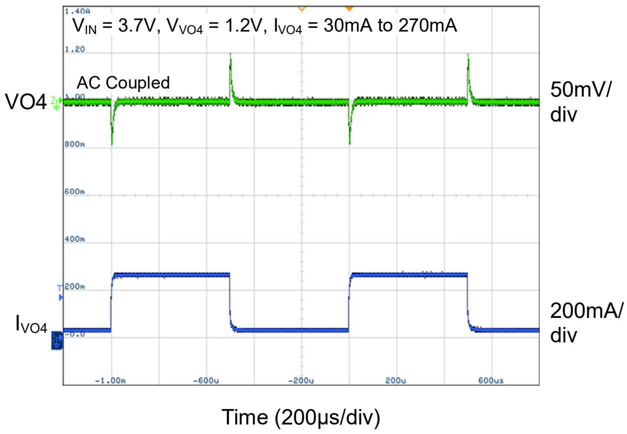
Time (200μs/div)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

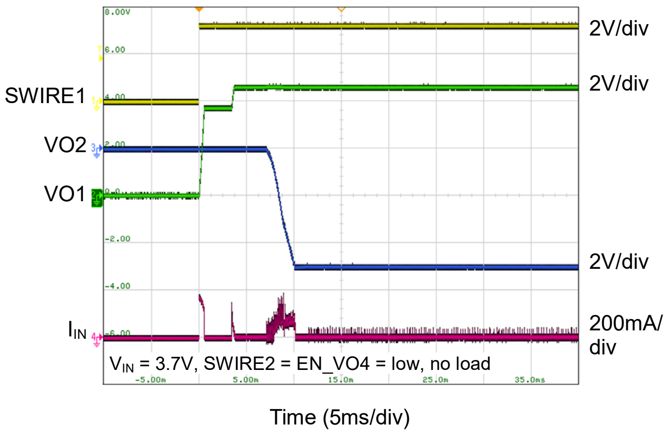
VO3 Load Transient



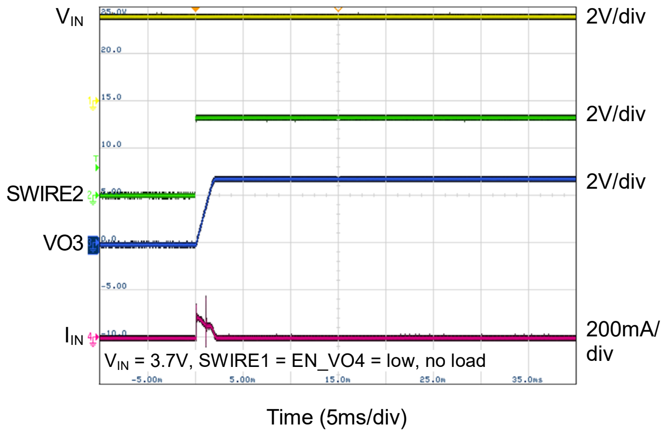
VO4 Load Transient



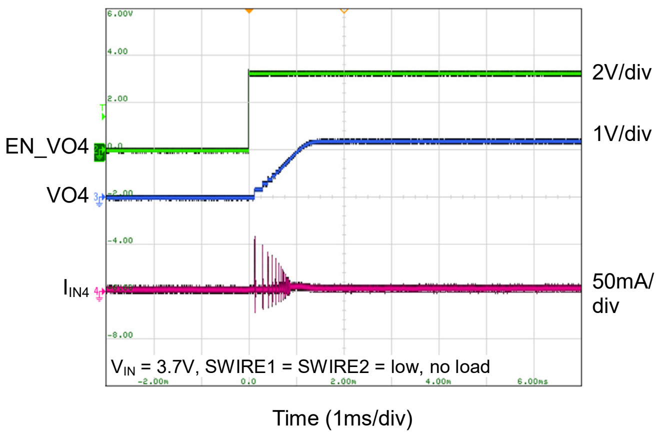
Start-Up Sequence



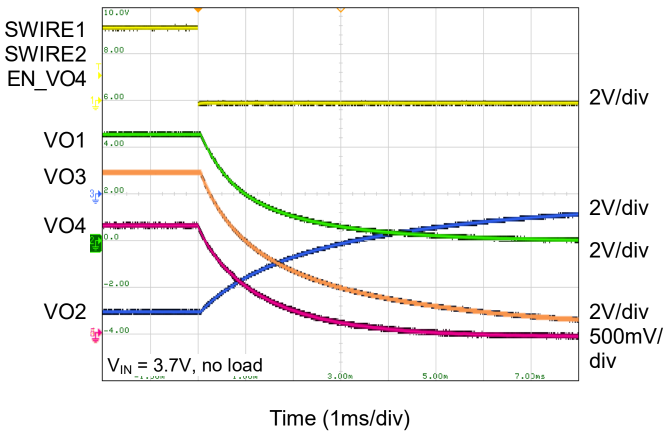
Start-Up Sequence



Start-Up Sequence



Shutdown Sequence Discharge = ON



FUNCTIONAL BLOCK DIAGRAM

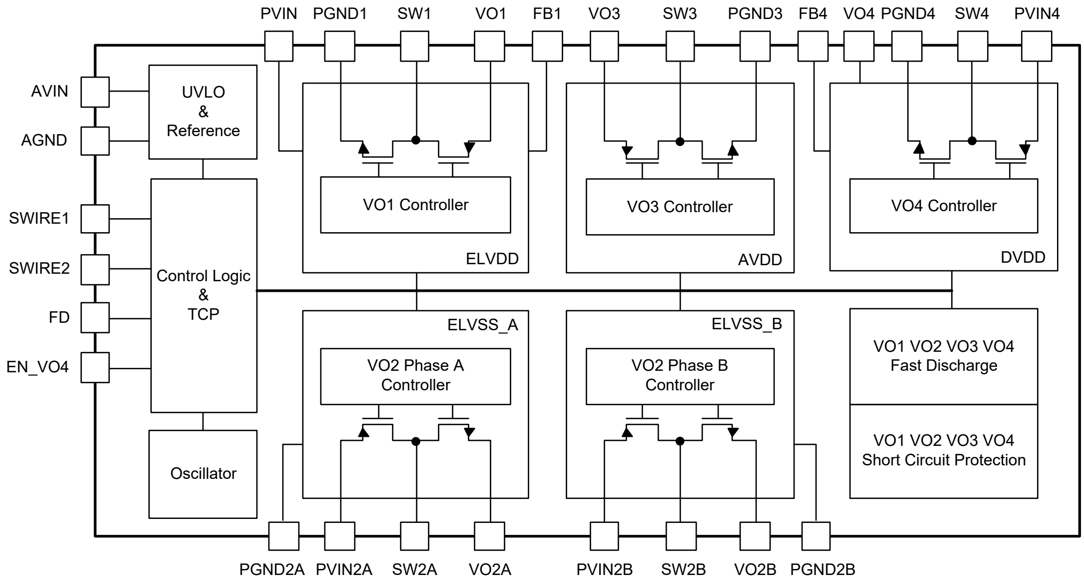


Figure 6. Functional Block Diagram

RECOMMENDED COMPONENT SELECTION

Table 1. Recommended Component Selection

Converter	Component	Value	Number	Electrical Spec	Part Number	Manufacturer
ELVDD	C_{IN1}	10µF	1	X5R, 6.3V, 0402	GRM155R60J106ME05	Murata
	C_{VO1_1} C_{VO1_2}	22µF	2	X5R, 6.3V, 0603	GRM188R60J226MEA0	Murata
	L_{VO1}	2.2µH	1	4A, 70mΩ, 322512	HMLQ32251B-2R2MS	Cyntec
ELVSS	C_{PVIN2A} C_{PVIN2B}	10µF	2	X5R, 6.3V, 0402	GRM155R60J106ME05	Murata
	C_{VO2A_1} C_{VO2A_2} C_{VO2B_1} C_{VO2B_2}	22µF	4	X5R, 16V, 0805	GRM219R61C226ME15	Murata
	L_{VO2A} L_{VO2B}	2.2µH	2	4A, 70mΩ, 322512	HMLQ32251B-2R2MS	Cyntec
AVDD	C_{IN3}	10µF	1	X5R, 6.3V, 0402	GRM155R60J106ME05	Murata
	C_{VO3_1} C_{VO3_2}	10µF	2	X5R, 16V, 0603	GRM188R61C106KAAL	Murata
	L_{VO3}	10µH	1	1.3A, 390mΩ, 252012	SDEM25201B-100MS	Cyntec
DVDD	C_{IN4}	10µF	1	X5R, 6.3V, 0402	GRM155R60J106ME05	Murata
	C_{VO4}	10µF	1	X5R, 6.3V, 0402	GRM155R60J106ME05	Murata
	L_{VO4}	4.7µH	1	2.5A, 94mΩ, 434312	HBLE041B-4R7MSA	Cyntec

DETAILED DESCRIPTION

Under-Voltage Lockout (UVLO)

The built-in under-voltage lockout function (UVLO) monitors the input voltage and disables the device when the input voltage is too low to operate.

Thermal Shutdown (TSD)

The device has a function of thermal shutdown, which prevents the device from damage due to overheating and excessive power dissipation. The device stops switching and shuts down all the outputs when the junction temperature exceeds +145℃ (TYP), and restarts with the same programmed voltages and sequences when the temperature decreases to +135℃ (TYP).

Boost Converter VO1 (ELVDD)

The Boost converter VO1 operates with a valley-current-mode topology and fixed 1.3MHz (TYP) frequency. The VO1 output voltage can be programmed between 4.6V and 5.2V (default 4.6V) with 100mV steps (see Table 2).

The output sense pin (FB1) is always connected to the positive pin of output capacitor for the highest output voltage accuracy. The wide hysteresis voltage makes the device suitable for large path loss applications. Additionally, the Boost converter can sense the output voltage with the VO1 pin, when the FB1 pin is floating or connected to ground or connected as close to the VO1 pin as possible.

The output of VO1 is fully isolated in shutdown mode.

Inverting Buck-Boost Converter VO2 (ELVSS)

The inverting Buck-Boost converter VO2 operates with a peak-current-mode topology and dual-phase fixed 1.2MHz (TYP) frequency. The VO2 output voltage can be programmed between -10V and -1.4V (default -5.0V) with 100mV steps (see Table 2).

When the load current exceeds 240mA, both phase A and phase B of the inverting Buck-Boost converter work. And only phase A works when the load current decreases to 160mA for reducing the switching loss.

The output of VO2 is fully isolated in shutdown mode.

Boost Converter VO3 (AVDD)

The Boost converter VO3 operates with a peak-current-mode topology and fixed 1.3MHz (TYP) frequency. The VO3 output voltage can be programmed between 5.5V and 8.0V (default 7.0V) with 100mV steps (see Table 2).

The output of VO3 is fully isolated in shutdown mode.

Buck Converter VO4 (DVDD)

The Buck converter VO4 operates with a peak-current-mode topology and fixed 1.3MHz (TYP) frequency. The VO4 output voltage can be programmed between 0.8V and 1.5V (default 1.2V) with 25mV steps (see Table 2).

The output of VO4 is fully isolated in shutdown mode.

Output Current Capacity

The device operates with an input voltage range of 2.9V to 4.8V. However, due to different input voltage and different output voltage, the output current capacity is quite different. A lower input voltage or a higher output voltage leads to a lower output current capacity.

Input Power Supply

The input power supply voltage is recommended between 2.9V and 4.8V. To achieve full performance, a stable and noise-free input source is needed. Once the distance between input source and SGM3842 is a bit long, additional capacitors are suggested to place as close to the device as possible. Please refer to the typical application circuit for the suggested input capacitance.

SGMICRO has patented circuits to solve the spike problem of V_{ELVDD} due to mode switching when the input voltage rises close to or higher than the programmed V_{ELVDD}.

Digital Interface (SWIRE1 & SWIRE2 Pins)

The positive output voltages V_{ELVDD}, V_{AVDD}, V_{DVDD} and the negative output voltage V_{ELVSS} can be programmed by the SWIRE1 and SWIRE2 digital interfaces with 100mV steps.

Figure 2 shows an example for SGM3842 programming V_{ELVSS} from -5.0V to -4.0V. The SWIRE1 and SWIRE2 pins can be used as standard enable pins for VO1, VO2 and VO3 if programming is not required.

DETAILED DESCRIPTION (continued)

The VO4 voltage can be preset by SWIRE2 and then it outputs when EN_VO4 is pulled high. In addition, the output voltage can be programmed when the EN_VO4 is already active.

The device starts with its default values (green marked values in Table 2) if enabled. The SWIRE interfaces count the rising edges to set the corresponding values as shown in Table 2. The device utilizes a volatile memory to store the settings.

Table 2. Programming Table

SWIRE1 Rising Edges	VO1 (V_{ELVDD})	SWIRE1 Rising Edges	VO2 (V_{ELVSS})	SWIRE1 Rising Edges	VO2 (V_{ELVSS})	SWIRE1 Rising Edges	VO2 (V_{ELVSS})	SWIRE2 Rising Edges	VO3 (V_{AVDD})	SWIRE2 Rising Edges	VO4 (V_{DVDD})
0/no pulse	4.6V	0/no pulse	-5.0V	59	-5.7V	93	-2.3V	0/no pulse	7V	0/no pulse	1.200V
1	5.2	26	-9.0V	60	-5.6V	94	-2.2V	1	Reserved	32	0.800V
2	5.1	27	-8.9V	61	-5.5V	95	-2.1V	2	Reserved	33	0.825V
3	5.0	28	-8.8V	62	-5.4V	96	-2.0V	3	Reserved	34	0.850V
4	4.9	29	-8.7V	63	-5.3V	97	-1.9V	4	Reserved	35	0.875V
5	4.8	30	-8.6V	64	-5.2V	98	-1.8V	5	Reserved	36	0.900V
6	4.7	31	-8.5V	65	-5.1V	99	-1.7V	6	5.5V	37	0.925V
7	4.6	32	-8.4V	66	-5.0V	100	-1.6V	7	5.6V	38	0.950V
8	Reserved	33	-8.3V	67	-4.9V	101	-1.5V	8	5.7V	39	0.975V
9	Reserved	34	-8.2V	68	-4.8V	102	-1.4V	9	5.8V	40	1.000V
10	Reserved	35	-8.1V	69	-4.7V	103	VO1/2 FD	10	5.9V	41	1.025V
11	Reserved	36	-8.0V	70	-4.6V	104	Reserved	11	6.0V	42	1.050V
12	Reserved	37	-7.9V	71	-4.5V	105	Reserved	12	6.1V	43	1.075V
13	Reserved	38	-7.8V	72	-4.4V	106	VO1/2 HiZ	13	6.2V	44	1.100V
14	Reserved	39	-7.7V	73	-4.3V	107	Leakage Protect Dis	14	6.3V	45	1.125V
15	Reserved	40	-7.6V	74	-4.2V	108	Leakage Protect EN	15	6.4V	46	1.150V
16	2 Phase	41	-7.5V	75	-4.1V	109	Reserved	16	6.5V	47	1.175V
17	Reserved	42	-7.4V	76	-4.0V	110	Reserved	17	6.6V	48	1.200V
18	Reserved	43	-7.3V	77	-3.9V	111	Reserved	18	6.7V	49	1.225V
19	Reserved	44	-7.2V	78	-3.8V	112	Reserved	19	6.8V	50	1.250V
20	Reserved	45	-7.1V	79	-3.7V	113	Reserved	20	6.9V	51	1.275V
21	Reserved	46	-7.0V	80	-3.6V	114	Reserved	21	7.0V	52	1.300V
22	Reserved	47	-6.9V	81	-3.5V	115	-10V	22	7.1V	53	1.325V
23	Reserved	48	-6.8V	82	-3.4V	116	-9.9V	23	7.2V	54	1.350V
24	Reserved	49	-6.7V	83	-3.3V	117	-9.8V	24	7.3V	55	1.375V
25	1 Phase	50	-6.6V	84	-3.2V	118	-9.7V	25	7.4V	56	1.400V
		51	-6.5V	85	-3.1V	119	-9.6V	26	7.5V	57	1.425V
		52	-6.4V	86	-3.0V	120	-9.5V	27	7.6V	58	1.450V
		53	-6.3V	87	-2.9V	121	-9.4V	28	7.7V	59	1.475V
		54	-6.2V	88	-2.8V	122	-9.3V	29	7.8V	60	1.500V
		55	-6.1V	89	-2.7V	123	-9.2V	30	7.9V	63	VO3 FD
		56	-6.0V	90	-2.6V	124	-9.1V	31	8.0V	64	VO3 HiZ
		57	-5.9V	91	-2.5V						
		58	-5.8V	92	-2.4V						

DETAILED DESCRIPTION (continued)

Soft-Start, Discharge, Start-Up and Timing Shutdown

The built-in soft-start function is adopted to limit the inrush current.

The output discharge function can be controlled by FD pin and SWIRE1/2 interface. See Table 3 to Table 5 for more details.

Toggling SWIRE1 high or with relevant pulses enables the VO1 Boost converter. VO1 starts with a 0.35A soft-start current limit until it rises to the programmed voltage. Then the full current limit is active (2.45A, TYP).

6ms after toggling SWIRE high, the VO2 converter starts switching phase A (VO2A) with a 0.7A current limit until the VO2 rises to the default voltage (-5V). Then the full current limit is active (3.1A per phase, TYP).

Toggling SWIRE2 high starts the VO3 Boost converter. Before VO3 rises to the default value (7.0V), it rises linearly for 1.8ms with a 0.35A current limit. Then the full current limit is active (1.05A, TYP).

Toggling EN_VO4 high starts the VO4 Buck converter. Before VO4 rises to the default value (1.2V), it rises linearly for 1.2ms with a 0.35A current limit. Then the full current limit is active (1.05A, TYP).

Table 3. VO2 Operation Mode Control

SWIRE1 Rising Edges	VO2 Load Setting (1->2 Converters)
0	240mA
16	Two Converters
25	One Converter

Table 4. VO1, VO2 Fast Discharge Mode Control and Leakage Current Protection Control

SWIRE1 Rising Edges	Discharging Mode (VO1&VO2)	SWIRE1 Rising Edges	Leakage Current Protection Setting
0/no pulse	FD = H: All Fast FD = L: All Hi-Z	0/no pulse	Disable
103	VO1: Fast VO2: Fast	107	Disable
104	Reserved	108	Enable
105	Reserved		
106	VO1: Hi-Z VO2: Hi-Z		

Table 5. VO3 Fast Discharge Mode Control

SWIRE2 Rising Edges	Discharging Mode (VO3)
0	FD = H: AVDD fast FD = L: AVDD Hi-Z
63	VO3: Fast
64	VO3: Hi-Z

Short Circuit and Overload Protection

The built-in short circuit protection (SCP) prevents the device from damage. If any of the four outputs (VO1, VO2, VO3 and VO4) is shorted to the ground or VO1 and VO2 are shorted together, the SGM3842 will trigger the function.

When a short or an overload occurs, all the four converters stop switching, the outputs are shut down and latched.

Only resetting the power supply or pulling SWIRE1, SWIRE2 and EN_VO4 low simultaneously for more than t_{OFF} can restart the device.

A SCP or overload occurs if any of the following events happens:

- V_{ELVDD} is not in regulation 2.76ms after V_{ELVDD} is enabled (SWIRE = high for longer than 2.76ms) then all converters shut down.
- V_{ELVSS} is not in regulation 7.48ms after V_{ELVSS} is enabled (SWIRE = high for longer than 13.5ms) then all converters shut down.
- V_{AVDD} protection is enabled when the soft-start is completed.
- V_{DVDD} protection is enabled when the soft-start is completed.
- V_{ELVDD} falls below 76% of the programmed output voltage longer than 1.2ms then all converters shut down.
- V_{ELVSS} rises above 71% of the programmed output voltage longer than 1.2ms then all converters shut down.
- V_{AVDD} falls below 87% of the programmed output voltage longer than 1.2ms then all converters shut down.
- V_{DVDD} falls below 82% of the programmed output voltage longer than 1.2ms then all converters shut down.

DETAILED DESCRIPTION (continued)

Device Reset

- Power resetting resets the device to default settings.
- Short circuit and overload protection reset all settings.
- Pulling SWIRE1 high to enable the V_{ELVDD} converter resets the output discharge. Then output discharge is controlled by FD pin.
- Pulling SWIRE1 low for t_{OFF} resets the leakage current protection function.
- Pulling SWIRE1 and SWIRE2 low for t_{OFF} then V_{ELVDD}, V_{ELVSS} and V_{AVDD} are reset to default values of 4.6V, -5.0V and 7.0V, respectively.
- Pulling SWIRE2 and EN_VO4 low at the same time for t_{OFF} then V_{DVDD} is reset to default value of 1.2V.
- Pulling SWIRE1, SWIRE2 and EN_VO4 low at the same time for t_{OFF} resets the SCP or overloading latch-up.

Layout Guideline

AMOLED displays are sensitive to the quality of power supplies. A good PCB layout is quite important to reduce the ripple and to enhance the line and load transients, as well as to achieve better noise, better EMI and loop stability. The recommended layout is illustrated in Figure 7.

It is recommended to follow the below PCB layout guidelines:

• A common ground plane between AGND and PGNDx can minimize ground shifts.
• Traces of switching nodes (SW1, SW2A, SW2B, SW3 and SW4) should be short and wide.
• Place input and output capacitors as close as possible to the related pins.
• Use short and wide traces to connect the input and output capacitors to the related pins.
• A common ground plane is between the ground pins of input capacitors and output capacitors.
• If the power IC has an exposed pad, connect AGND and PGNDx with the exposed pad.

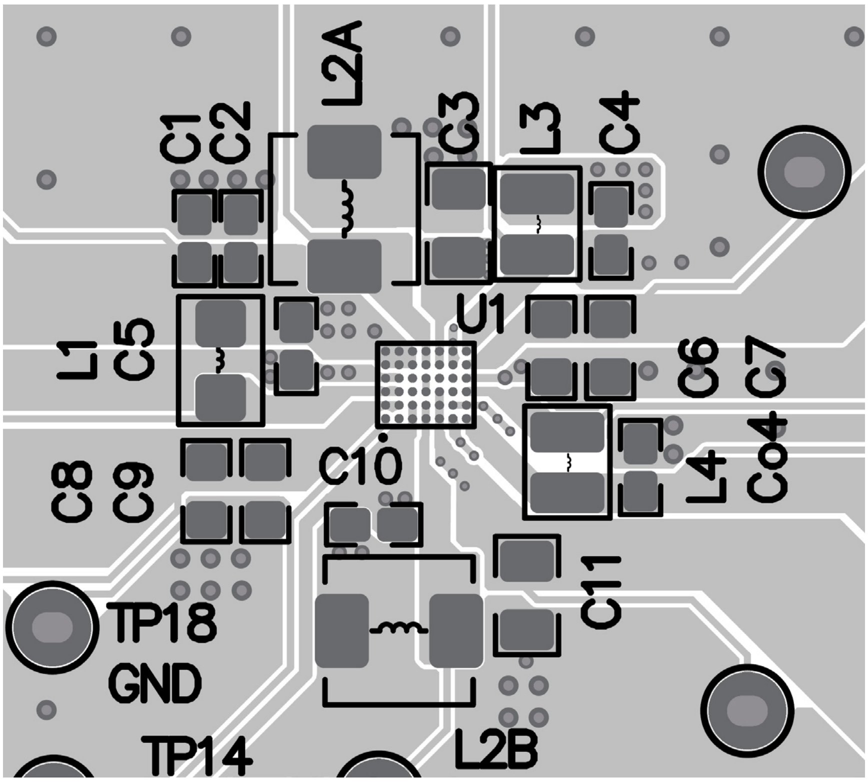


Figure 7. PCB Layout Reference

REVISION HISTORY

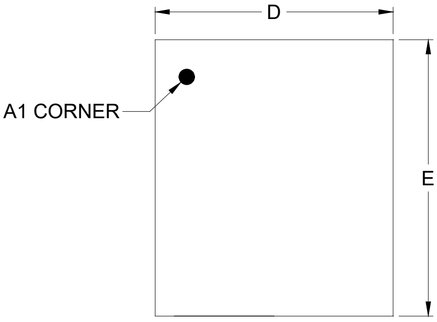
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

JANUARY 2025 – REV.A to REV.A.1	Page
Added θ_{JB} and θ_{JC}	2
Deleted V_{IT-} Minimum	5

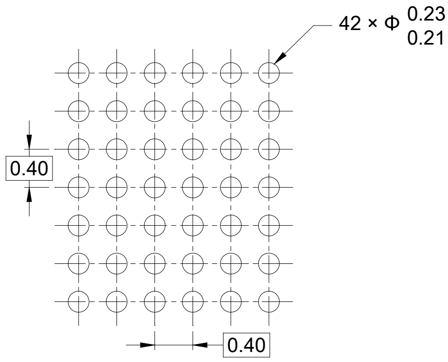
Changes from Original (OCTOBER 2023) to REV.A	Page
Corrected test condition of VO4 load transient from I_{VO3} to I_{VO4}	15
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

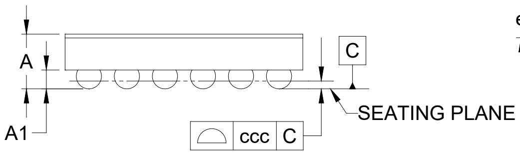
WLCSP-2.5×2.9-42B



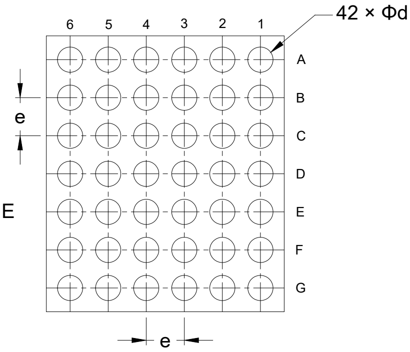
TOP VIEW



RECOMMENDED LAND PATTERN (Unit: mm)



SIDE VIEW



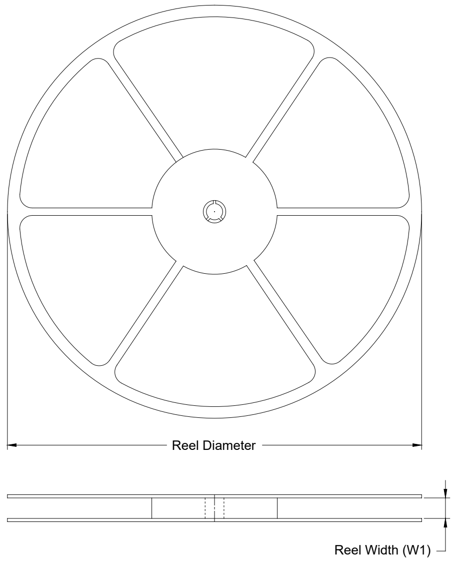
BOTTOM VIEW

Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	-	-	0.613
A1	0.178	-	0.218
D	2.470	-	2.530
E	2.870	-	2.930
d	0.235	-	0.295
e	0.400 BSC		
ccc	0.050		

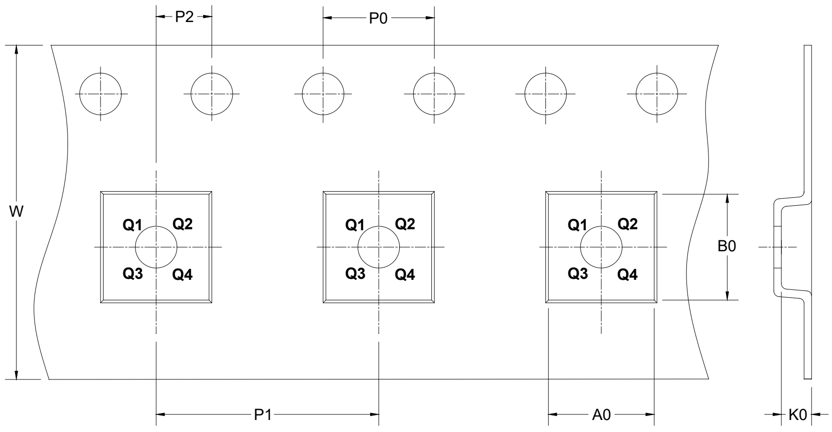
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



DIRECTION OF FEED

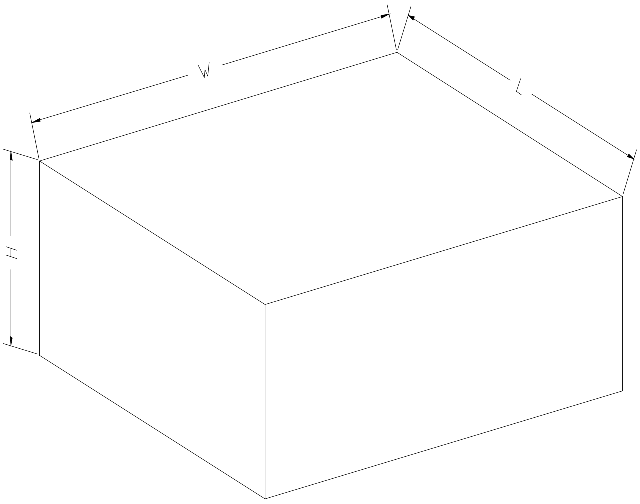
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
WLCSP-2.5×2.9-42B	13″	12.4	2.64	3.07	0.77	4.0	8.0	2.0	12.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002