SGM883
36V Voltage Detector with Internal Reference

GENERAL DESCRIPTION

The SGM883 is a 2.3V to 36V wide-supply voltage detector for under-voltage (UV) detection. It features a high-accuracy comparator with an internal reference voltage of 400mV and an open-drain reset outputs, capable of handling up to 36V.

If the IN voltage falls below the negative threshold, nRESET is pulled low. And if the IN voltage rises over the positive threshold, nRESET is pulled high.

To prevent false triggering and ensure stable output operation of the device, the comparator features built-in hysteresis for noise rejection.

The SGM883 is available in a Green SOT-23-6 package. It operates in the temperature range of -40℃ to +125℃.

TYPICAL APPLICATION

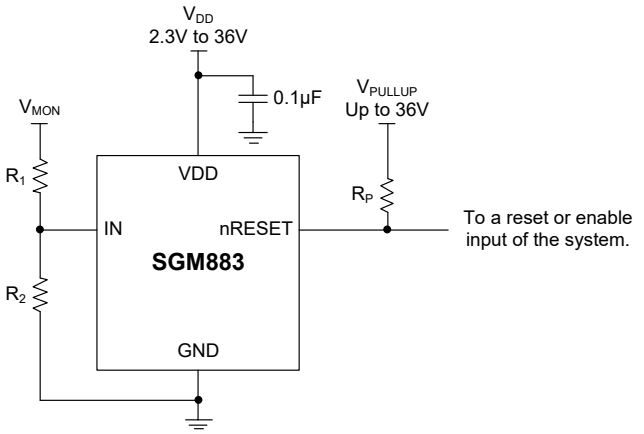


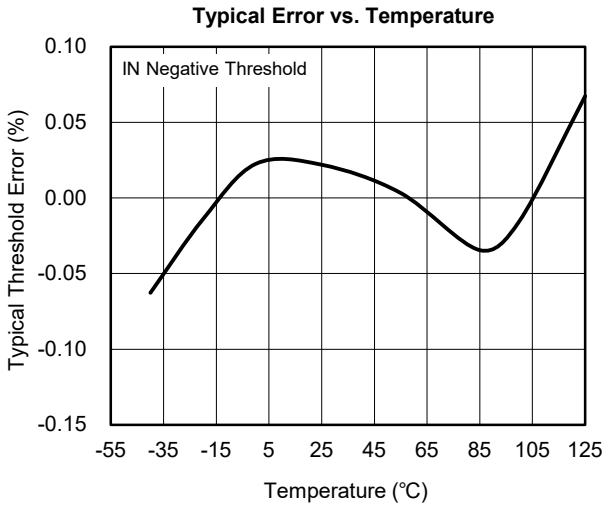
Figure 1. Typical Application Circuit

FEATURES

- **Wide Input Voltage Range: 2.3V to 36V**
- **Adjustable Threshold Down to 400mV**
- **Low Quiescent Current: 3.2μA (TYP)**
- **Low-to High Propagation Delay:**
  - **SGM883BA: 5.5μs**
  - **SGM883BB: 10ms**
  - **SGM883BC: 40ms**
  - **SGM883BD: 160ms**
  - **Accuracy: 15%**
- **High Threshold Accuracy**
  - **-40℃ to +125℃: 1.2%**
- **Internal Hysteresis: 27.5mV (TYP)**
- **Active-Low Open-Drain Reset Output for UV Detection**
- **Available in a Green SOT-23-6 Package**

APPLICATIONS

Industrial Control Systems
Embedded Computing Modules
DSP or Microcontroller
FPGA and ASIC Systems
Notebooks and Tablet Computers
Portable and Handheld Devices
Battery-Powered Products

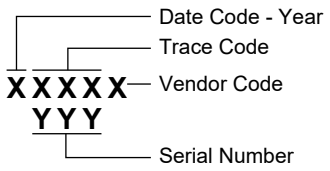


PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM883BA	SOT-23-6	-40℃ to +125℃	SGM883BAXN6G/TR	XXXXX 2FL	Tape and Reel, 3000
SGM883BB	SOT-23-6	-40℃ to +125℃	SGM883BBXN6G/TR	XXXXX 2FM	Tape and Reel, 3000
SGM883BC	SOT-23-6	-40℃ to +125℃	SGM883BCXN6G/TR	XXXXX 2FN	Tape and Reel, 3000
SGM883BD	SOT-23-6	-40℃ to +125℃	SGM883BDXN6G/TR	XXXXX 2FO	Tape and Reel, 3000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

VDD Voltage, V_{DD} ..... -0.3V to 45V
IN Voltage ..... -0.3V to 6.5V
nRESET Voltage ..... -0.3V to 40V
nRESET Current 20mA
Package Thermal Resistance
SOT-23-6, θ_{JA} ..... 147.2℃/W
SOT-23-6, θ_{JB} ..... 30.2℃/W
SOT-23-6, θ_{JC} ..... 80.3℃/W
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility (1) (2)
HBM ..... ±6000V
CDM ..... ±1000V

NOTES:

1. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.

2. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

RECOMMENDED OPERATING CONDITIONS

VDD Voltage, V_{DD} ..... 2.3V to 36V
IN Voltage ..... 0V to 5.5V
nRESET Voltage ..... 0V to 36V
nRESET Current ..... 0mA to 10mA
Operating Junction Temperature Range ..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

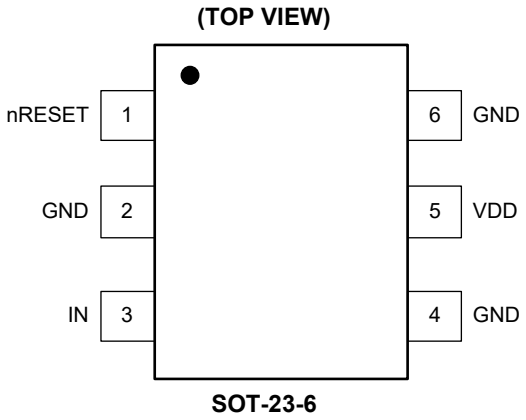
ESD SENSITIVITY CAUTION

This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION



PIN DESCRIPTION

PIN	NAME	TYPE	FUNCTION
1	nRESET	O	IN Comparator Open-Drain Output. If the IN voltage drops below V_{IT-}, nRESET is pulled low. And if the IN voltage rises over V_{IT+}, nRESET is pulled high.
2, 4, 6	GND	G	Ground. Connect all GND pins together.
3	IN	I	Comparator Input. Connect IN to the voltage being monitored via an external resistor divider. If the IN voltage drops below V_{IT-}, nRESET is pulled low.
5	VDD	I	2.3V to 36V Power Supply Voltage. Connect a 0.1μF ceramic capacitor between VDD and GND.

NOTE: I = input, O = output, G = ground.

ELECTRICAL CHARACTERISTICS

(V_{DD} = 2.3V to 36V, T_J = -40℃ to +125℃, R_P = 100kΩ, typical values are measured at V_{DD} = 12V and T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage Range	V_{DD}			2.3		36	V
Power-On Reset Voltage (1)	V_{POR}	V_{OL} ≤ 0.2V, pulled up to an external voltage rail of 36V				1.4	V
IN Pin Negative Input Threshold Voltage	V_{IT-}			395.2	400	404.8	mV
IN Pin Positive Input Threshold Voltage	V_{IT+}			421	427.5	434	mV
IN Pin Hysteresis Voltage (V_{HYS} = V_{IT+} - V_{IT-})	V_{HYS}			20	27.5	35	mV
Low-Level Output Voltage	V_{OL}	V_{DD} = 2.3V, I_{nRESET} = 3mA			40	100	mV
		V_{DD} = 5V, I_{nRESET} = 5mA			60	130	
Input Current at IN Pin	I_{IN}	0V ≤ V_{IN} ≤ 3V		-30	1	30	nA
Open-Drain Output Leakage Current	I_{D_LEAK}	V_{nRESET} = 36V			10	200	nA
Supply Current	I_{DD}				3.2	6.6	μA
Under-Voltage Lockout	UVLO	V_{DD} rising		1.7	2	2.3	V
High-to-Low Propagation Delay (2)	t_{PD_HL}	V_{DD} = 12V, ±200mV input overdrive, R_L = 100kΩ, V_{OH} = 0.9 × V_{DD}, V_{OL} = 250mV			5.3		μs
Low-to-High Propagation Delay (2)	t_{PD_LH}	V_{DD} = 12V, ±200mV input overdrive, V_{OH} = 0.9 × V_{DD}, V_{OL} = 250mV	SGM883BA		5.5		μs
			SGM883BB	8.5	10	11.5	ms
			SGM883BC	34	40	46	
			SGM883BD	136	160	184	
Startup Delay (3)	t_{D_START}	V_{DD} = 5V			740		μs
Output Rise Time	t_R	V_{DD} = 12V, C_L ≤ 10pF, V_O = (0.1 to 0.9) × V_{DD}			5		μs
Output Fall Time	t_F	V_{DD} = 12V, C_L ≤ 10pF, V_O = (0.9 to 0.1) × V_{DD}			0.08		μs

NOTES:

1. V_{POR} represents the minimum VDD voltage to ensure a controlled output condition.
2. High-to-low and low-to-high refers to the transition at nRESET pin.
3. During power-on, V_{DD} must exceed UVLO for at least t_{D_START} to finish the startup procedure.

Timing Diagram

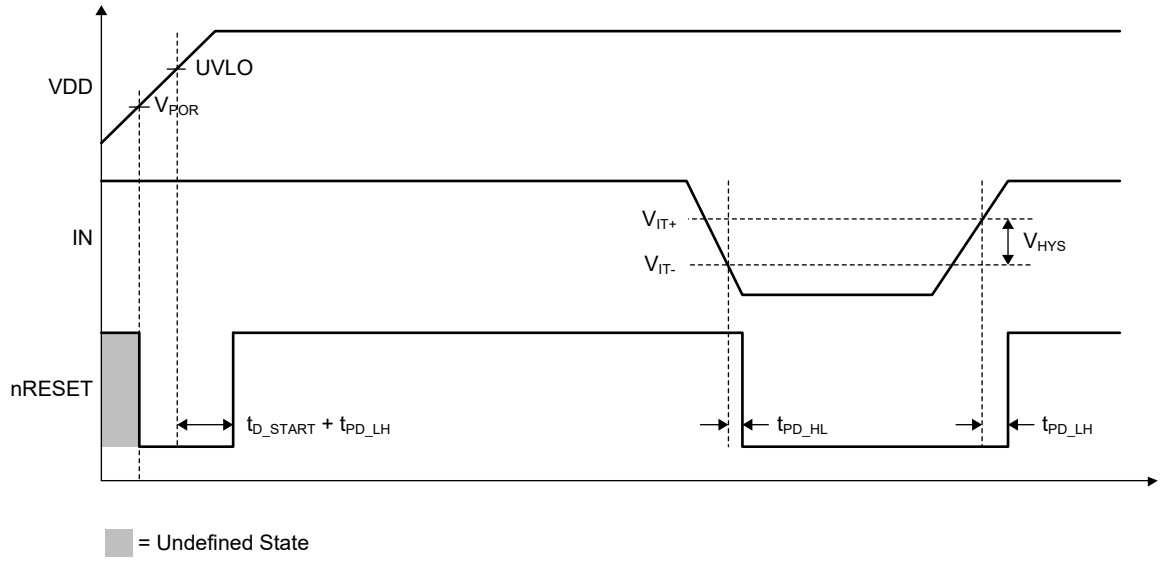
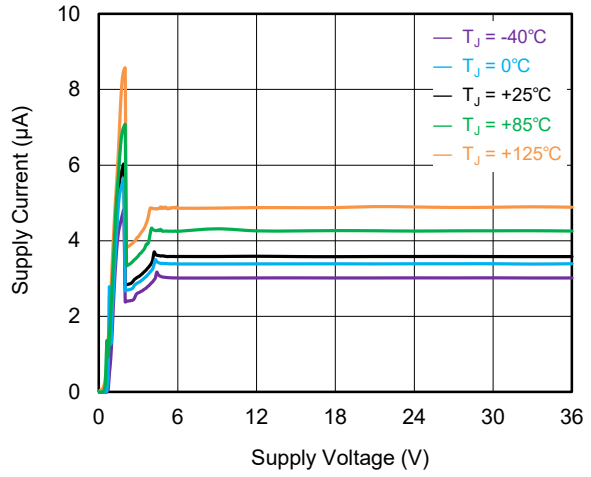


Figure 2. Timing Diagram

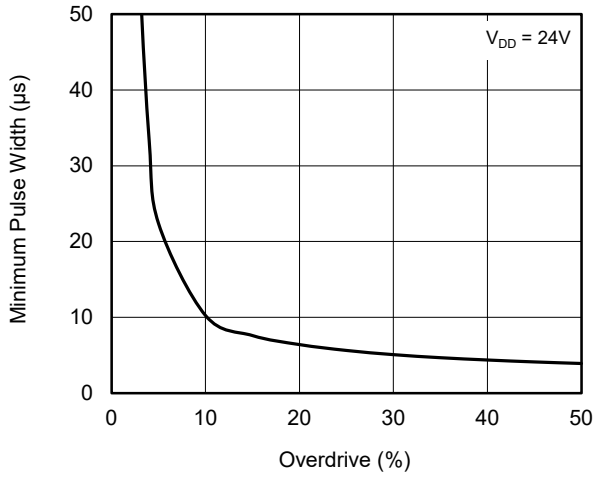
TYPICAL PERFORMANCE CHARACTERISTICS

T_J = +25℃ and V_{DD} = 12V, unless otherwise noted.

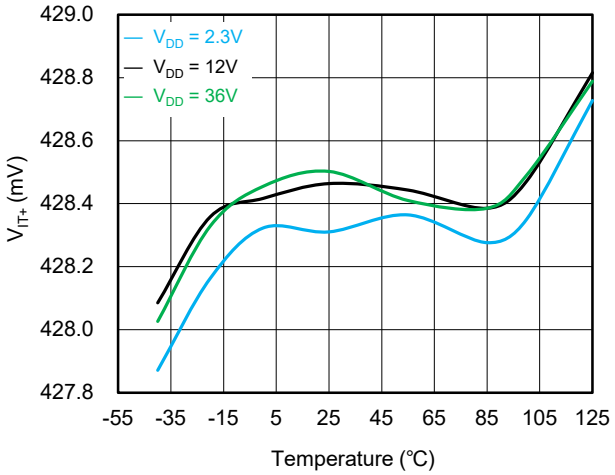
Supply Current vs. Supply Voltage



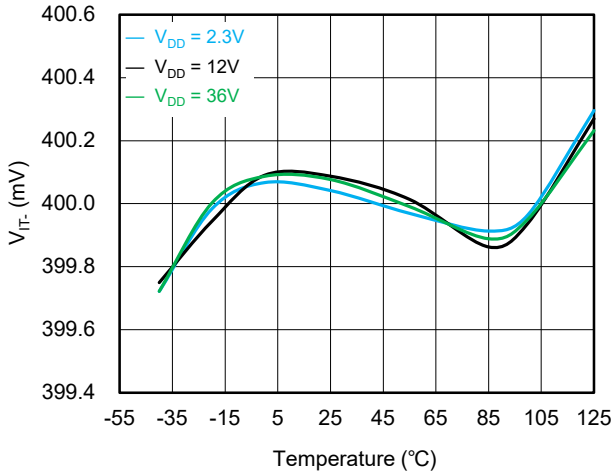
Minimum Pulse Duration vs. Threshold Overdrive Voltage (1)



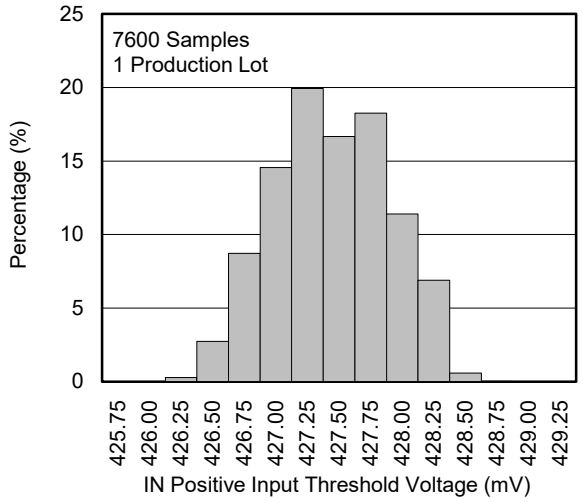
IN Positive Input Threshold Voltage (V_{IT+}) vs. Temperature



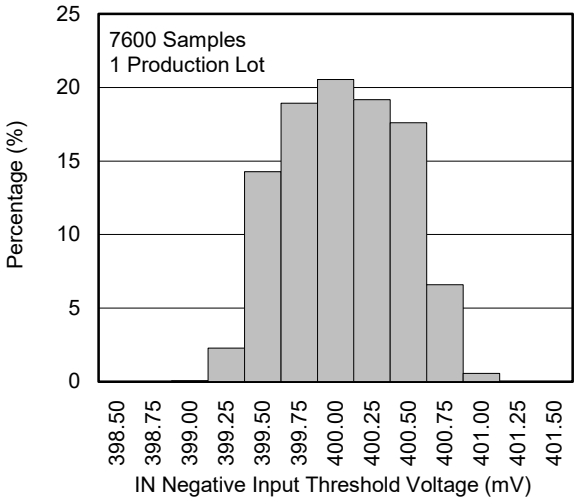
IN Negative Input Threshold Voltage (V_{IT-}) vs. Temperature



IN Positive Input Threshold Voltage (V_{IT+}) Distribution



IN Negative Input Threshold Voltage (V_{IT-}) Distribution

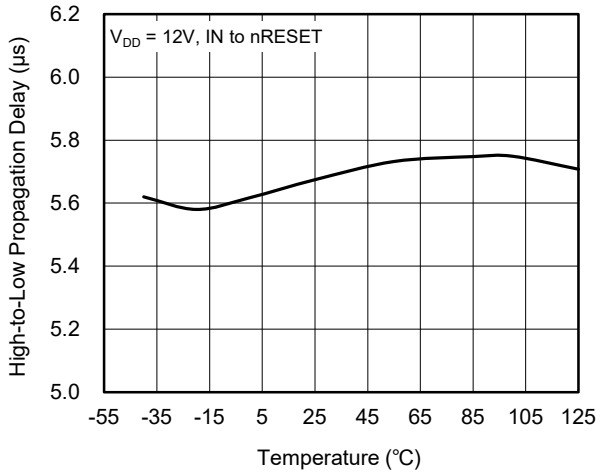


NOTE: 1. Minimum pulse duration required to trigger output high-to-low transition. IN = negative spike below V_{IT-}.

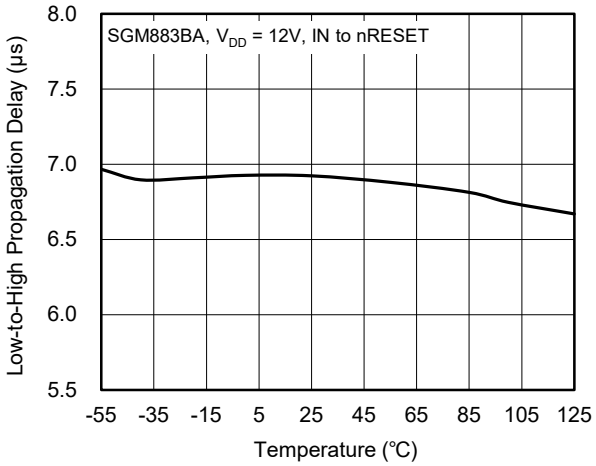
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_J = +25℃ and V_{DD} = 12V, unless otherwise noted.

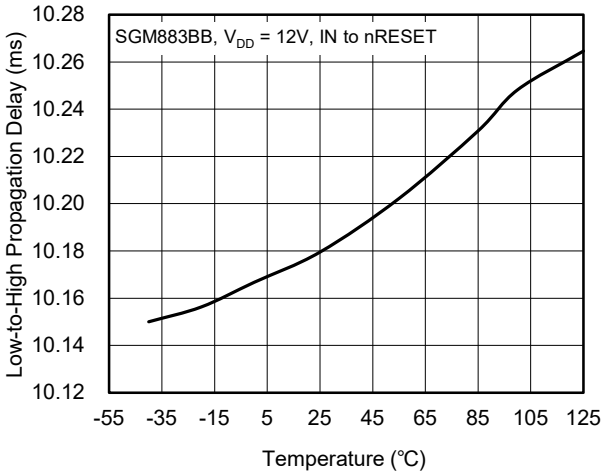
High-to-Low Propagation Delay vs. Temperature



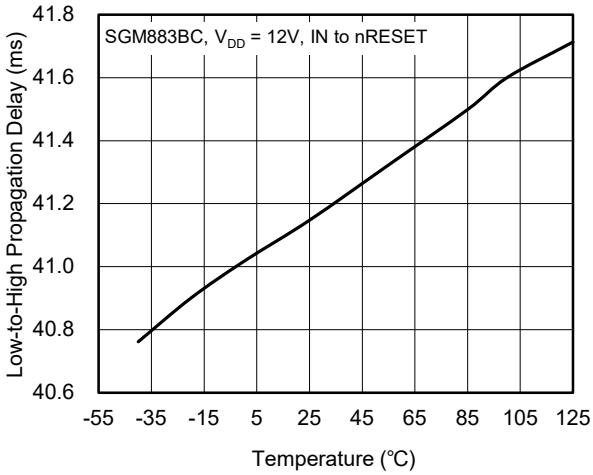
Low-to-High Propagation Delay vs. Temperature



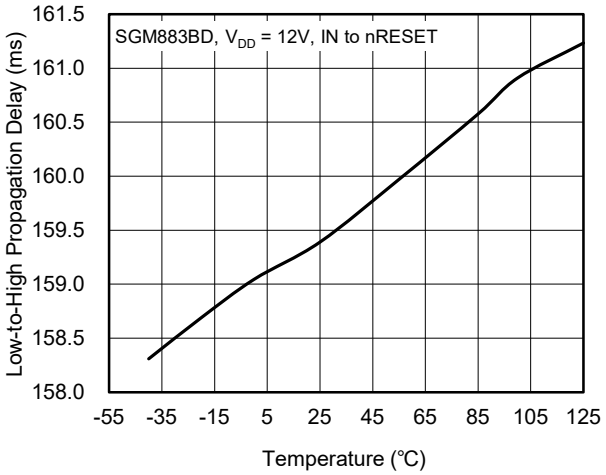
Low-to-High Propagation Delay vs. Temperature



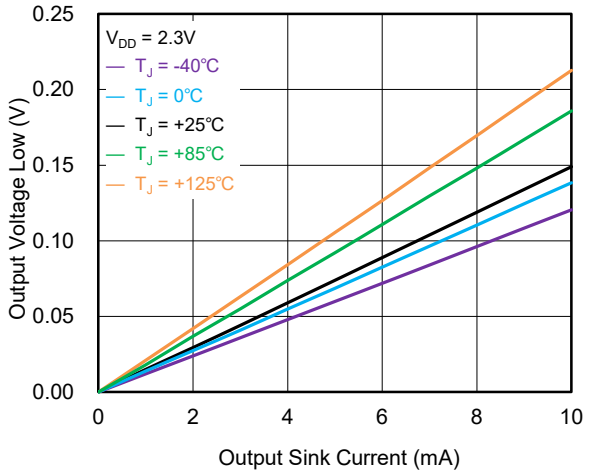
Low-to-High Propagation Delay vs. Temperature



Low-to-High Propagation Delay vs. Temperature



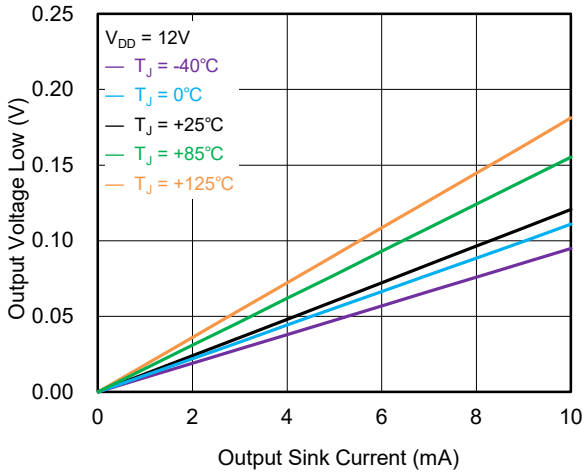
Output Voltage Low vs. Output Sink Current



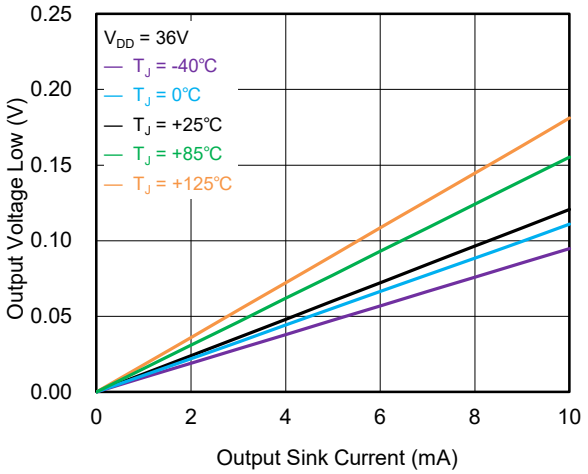
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_J = +25℃ and V_{DD} = 12V, unless otherwise noted.

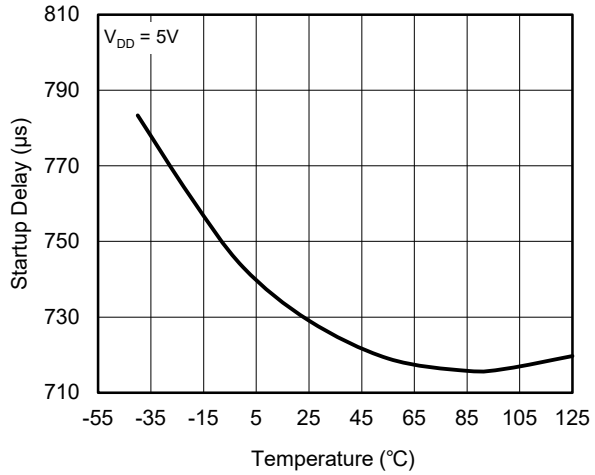
Output Voltage Low vs. Output Sink Current



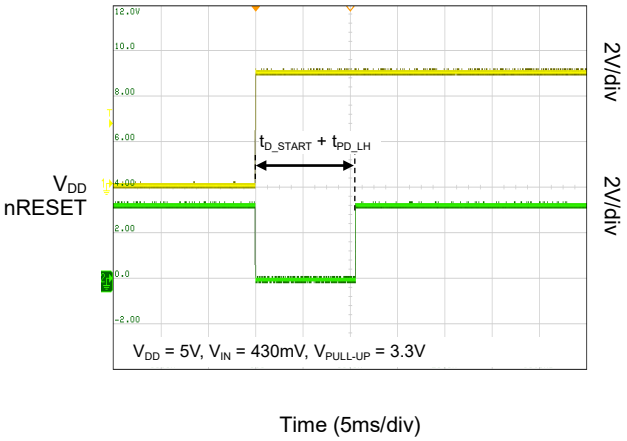
Output Voltage Low vs. Output Sink Current



Startup Delay vs. Temperature



Startup Delay (SGM883BB)



FUNCTIONAL BLOCK DIAGRAM

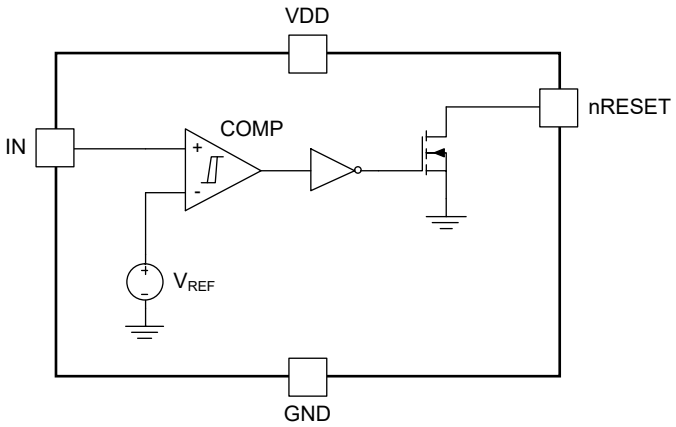


Figure 3. Block Diagram

DETAILED DESCRIPTION

Overview

The SGM883 is a 2.3V to 36V wide-supply voltage detector for under-voltage (UV) detection. It features a high-accuracy comparator with an internal reference voltage of 400mV and an open-drain reset output, capable of handling up to 36V and can sink up to 10mA.

Use an external resistor divider network to set the IN pin to sense voltage greater than 0.4V. The input allows the use of high-value resistors in the divider without sacrificing measurement accuracy for the low leakage current. To implement a voltage detection function, connect the input pin through a two-resistor network (see the Voltage Detector Considerations section). In this configuration, the SGM883 triggers its output signals when the monitored voltage falls below the negative input threshold voltage. The relationship between input states and output behavior is summarized in Table 1. The device supports wide range of threshold voltages, making it suitable for various system requirements.

Table 1. Truth Table

Condition	Output	Status
IN > V_{IT+}	nRESET high	Output high impedance
IN < V_{IT-}	nRESET low	Output asserted

Feature Description

Input (IN)

The SGM883 integrates a high-accuracy comparator with built-in hysteresis, providing noise immunity and ensuring stable operation. The comparator has one external input and the other internal input connected to the internal reference. The IN falling threshold is designed and trimmed to match the reference voltage of 400mV. It is recommended to add a 1nF to 10nF bypass capacitor at the comparator (IN) input for noisy applications, as it helps to reduce susceptibility to transient voltage fluctuations in the monitored signal.

The comparator drives its output (nRESET) to a logic low state when the IN voltage drops below the V_{IT-} threshold. nRESET returns to a high-impedance condition once IN exceeds the V_{IT+} level. The timing relationship between thresholds and output is illustrated in Figure 2.

The IN has internal clamp. When IN monitors high-voltage rail via resistor divider as Figure 1, if R_2 is open-circuited, the clamp circuit has limited protection for the IN pin. The protection is limited as IN = 6.5V, the current flows through IN is about 300μA. So considering the monitored voltage and the connecting resistor, the clamp is valid when open-circuit event happens and the current through the resistor is smaller than 300μA, as $(V_{MON} - 6.5)/R_1 < 300μA$.

Otherwise, the internal clamp protection is invalid and IN may be damaged if the voltage at the IN pin is higher than the absolute voltage.

Output (nRESET)

The reset output pin is designed to be used as reset input or enable input for typical applications like a micro-processor (μP), a DC/DC converter or a low dropout linear regulator (LDO).

The nRESET pin is an open-drain output. There must be a pull-up resistor to pull up the nRESET high when the output enters a high-impedance state. Connect the pull-up resistor to appropriate voltage rail, ensuring the output can interface with other devices at correct voltage levels. The output of SGM883 supports pull-up voltage up to 36V, regardless of the device's supply voltage. To maintain proper voltage levels, carefully consider the value of pull-up resistor. The value is determined by V_{OL}, output capacitive loading, and output leakage current (I_{D_LEAK}), all of which are specified in the Electrical Characteristics table.

Output assertion and high-impedance transitions follow the behavior described in Table 1 and the Input (IN) section. The dynamic relationship between threshold crossings and output states is depicted in the timing diagram of Figure 2.

Device Functional Modes

V_{DD} is below V_{POR} ($V_{DD} < V_{POR}$)

When V_{DD} is below V_{POR}, the nRESET is in a high-impedance state.

Under-Voltage Lockout ($V_{POR} \leq V_{DD} < UVLO$)

When $V_{POR} \leq V_{DD} < UVLO$, the nRESET signal is asserted to logic low regardless of the IN signal.

Normal Operation ($V_{DD} \geq UVLO$)

When V_{DD} is above or equal to UVLO, the nRESET signal is determined by IN, as shown in Table 1.

APPLICATION INFORMATION

Application Information

The SGM883 operates as a precision voltage detector in various systems. The monitored voltage (V_{MON}), supply voltage (V_{DD}), and output pull-up rail can be powered independently or interconnected, offering flexible design options. The subsequent sections provide a detailed explanation of how to configure the connection schemes.

Voltage Detector Considerations

By using a resistor divider network, the SGM883 forms a voltage detector circuit (see Figure 4 and Figure 5). With a resistor divider network, the input pin can monitor any system voltage exceeding 400mV.

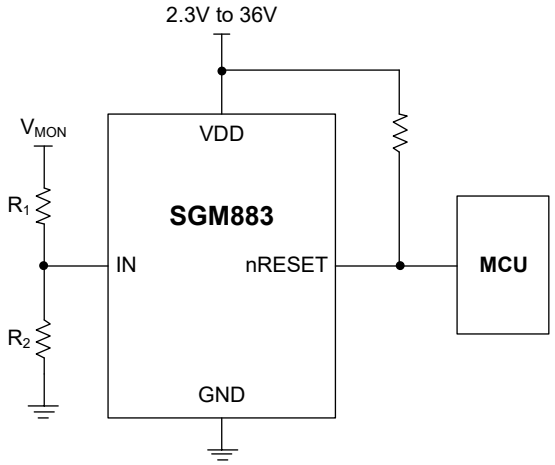


Figure 4. Voltage Detector Block Diagram

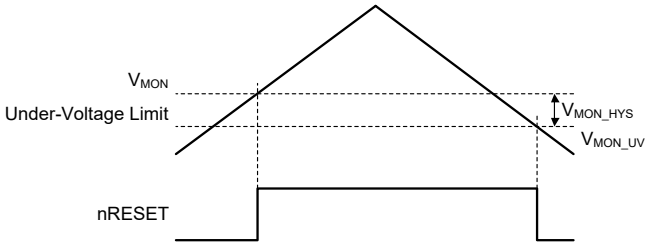


Figure 5. Voltage Detector Timing Diagram

The SGM883 identifies under-voltage condition with maximum accuracy. If the monitored voltage falls below V_{MON_UV}, the voltage required to pull nRESET high is V_{MON_UV} + V_{MON_HYS}.

Use Equations 1 to 2 to calculate resistor divider values.

$$R_{TOTAL} = R_1 + R_2 \quad (1)$$

Select an R_{TOTAL} value such that the current flowing through the divider is roughly 100 times higher than the input current at the IN pin. High-value resistors reduce current consumption, but input bias current will compromise V_{IT} accuracy when the current through the resistors is too low.

Calculate R_2 through Equation 2:

$$R_2 = \frac{R_{TOTAL}}{V_{MON\_UV}} \times V_{IT-} \quad (2)$$

V_{MON_UV} refers to the target voltage corresponding to the occurrence of under-voltage.

Input and Output Configurations

The examples of different input/output configurations are shown in Figure 6 to Figure 8.

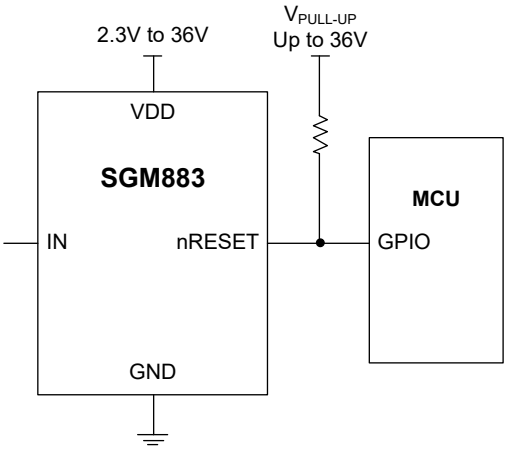


Figure 6. Interfacing to Voltages Other than V_{DD}

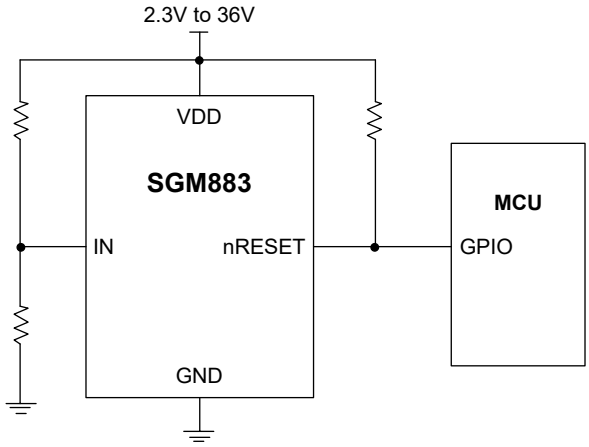
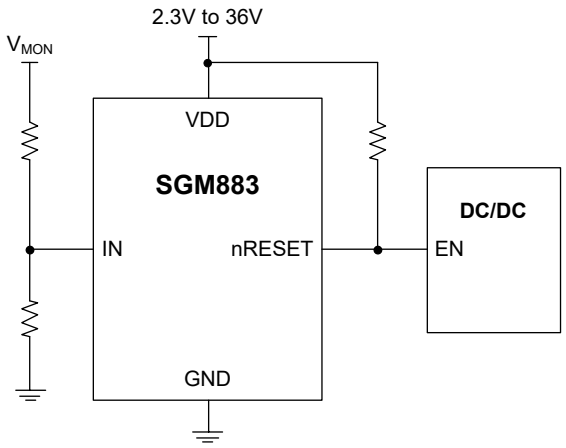


Figure 7. Monitoring the Same Voltage as V_{DD}

APPLICATION INFORMATION (continued)



NOTE: Users can monitor the voltage higher than V_{DD_MAX} by connecting an external resistor divider.

Figure 8. Monitoring a Voltage Other than V_{DD}

Immunity to Input Pin Voltage Transients

The SGM883 can suppress short voltage transient spikes on its input pin. Sensitivity to such transients depends on both transient duration and amplitude. Refer to the Minimum Pulse Duration vs. Threshold Overdrive Voltage curve in Typical Performance Characteristics for details.

Power Supply Recommendations

The VDD pin of the SGM883 has an absolute maximum voltage rating of 45V, with a recommended operating range up to 36V. In applications where the supply is subject to large transients exceeding 40V or the slew rate is greater than 1V/μs, additional protection is recommended. A series RC filter, consisting of a 100Ω resistor and a 0.1μF capacitor, should be installed between the power supply and VDD pin to suppress high-frequency disturbances, as shown in Figure 9.

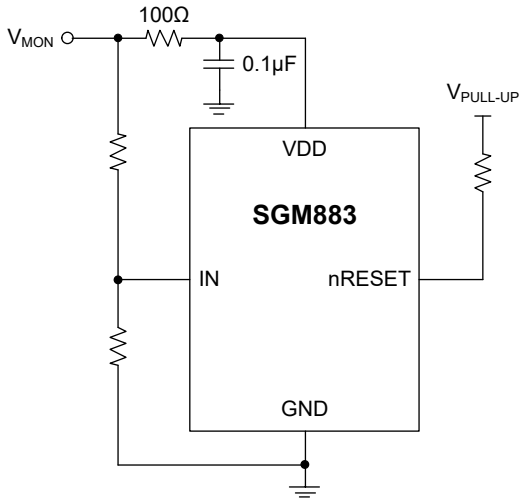


Figure 9. Filtering High-Frequency Disturbances on VDD by Using an RC Filter

Layout Guidelines

Place the external resistors network close to the device to mitigate noise effect.

Place the VDD capacitor as close to the VDD pin as possible.

Keep the VDD traces short to avoid LC resonance from the decoupling capacitor and parasitic inductance of the trace. If long traces are unavoidable, refer to Figure 9 for a VDD filtering example.

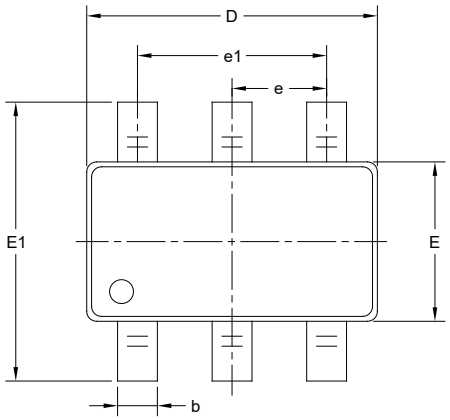
REVISION HISTORY

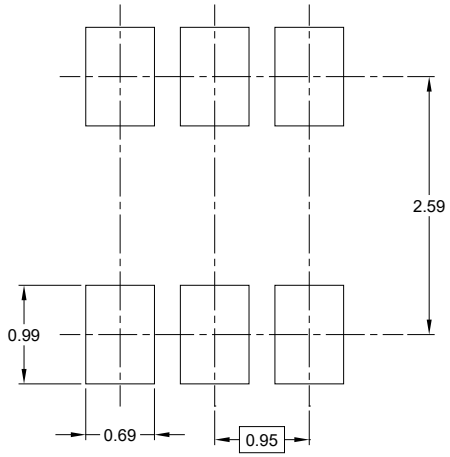
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original to REV.A (DECEMBER 2025)	Page
Changed from product preview to production data	All

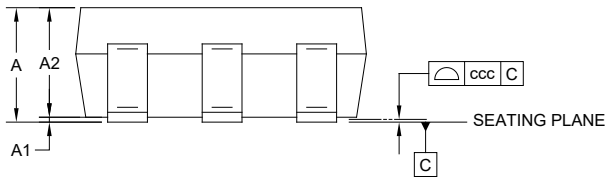
PACKAGE OUTLINE DIMENSIONS

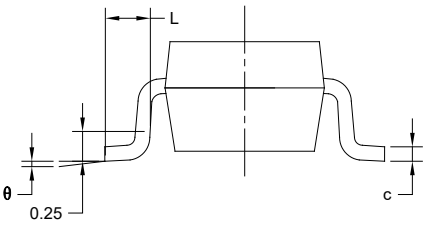
SOT-23-6





RECOMMENDED LAND PATTERN (Unit: mm)



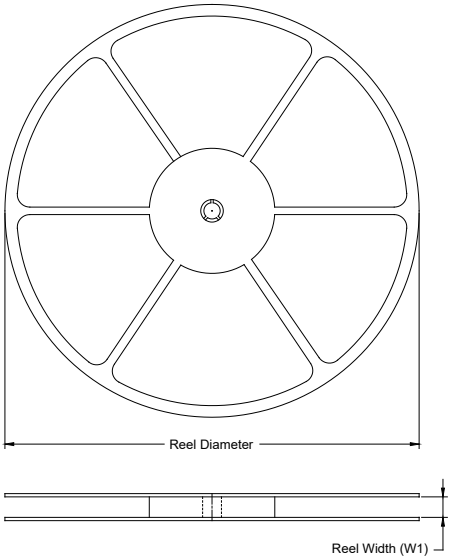


Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	-	-	1.450
A1	0.000	-	0.150
A2	0.900	-	1.300
b	0.300	-	0.500
c	0.080	-	0.220
D	2.750	-	3.050
E	1.450	-	1.750
E1	2.600	-	3.000
e	0.950 BSC		
e1	1.900 BSC		
L	0.300	-	0.600
θ	0°	-	8°
ccc	0.100		

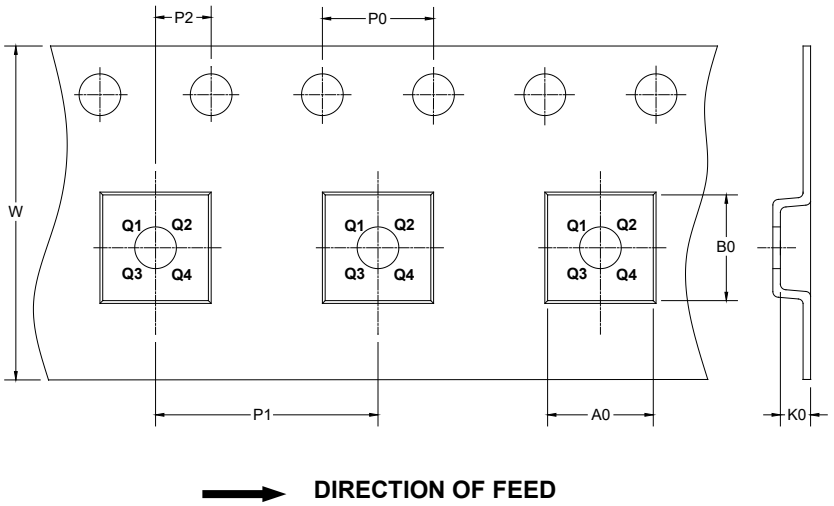
NOTES:
1. This drawing is subject to change without notice.
2. The dimensions do not include mold flashes, protrusions or gate burrs.
3. Reference JEDEC MO-178.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



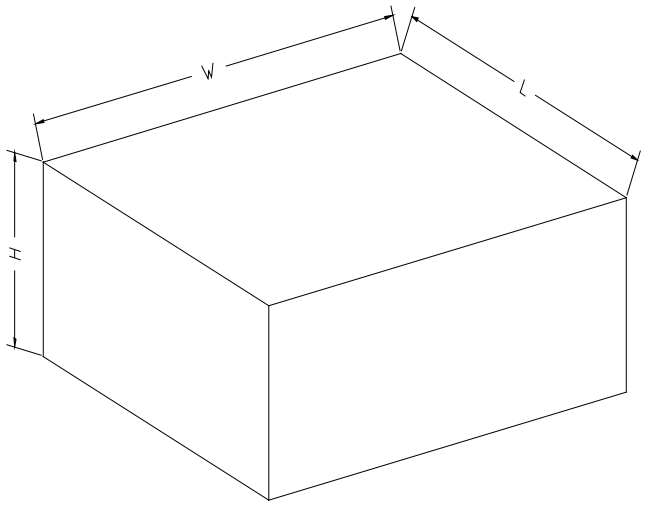
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
SOT-23-6	7″	9.5	3.23	3.17	1.37	4.0	4.0	2.0	8.0	Q3

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18

DD0002