SGM90516
16 Channels, 12-Bit Analog Monitor and Controller with Multichannel ADC, Bipolar DACs, Temperature Sensor and GPIO Ports

GENERAL DESCRIPTION

The SGM90516 is a high integrated analog front end, which includes 16 monotonic 12-bit DACs, a 21-input 12-bit SAR ADC, a temperature sensor and an on-chip reference.

The chip also has 8-channel general purpose inputs and outputs (GPIOs). These pins are configurable for ADC inputs or GPIOs.

The chip is operated by a 4-wire SPI-compatible interface.

The SGM90516 is available in a Green TQFP-10×10-64L (Exposed Pad) package. It is specified from -40℃ to +125℃.

APPLICATIONS

Active Antenna System mMIMO
Distributed Antenna Systems
Macro Remote Radio Unit
Radar
Outdoor Backhaul Unit
Data Acquisition Systems

FEATURES

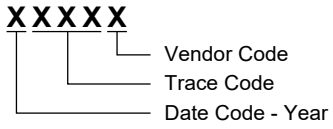
- **16 Monotonic 12-Bit DACs**
  - **Programmable Voltage Ranges: -10V to 0V, -5V to 0V, 0V to 5V, and 0V to 10V**
  - **High Current Output: up to ±15mA**
  - **Supports Auto-Range Detector**
  - **Configurable Clamp Voltage**
- **12-Bit SAR ADC**
  - **16 Bipolar Input Channels: -12.5V to +12.5V**
  - **5 Unipolar Input Channels: 0V to 5V**
  - **Supports Programmable Out-of-Range Alarms**
- **Internal 2.5V Reference**
- **Internal Temperature Sensor**
  - **-40℃ to +125℃ Operation**
  - **±6℃ Accuracy**
- **8 General Purpose Input/Output Ports (GPIOs)**
- **4-Wire SPI-Compatible Serial Interface**
  - **Supports 1.8V to 5.25V Operation**
- **-40℃ to +125℃ Operating Temperature Range**
- **Available in a Green TQFP-10×10-64L (Exposed Pad) Package**

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM90516	TQFP-10×10-64L (Exposed Pad)	-40℃ to +125℃	SGM90516XTFF64G/TR	05Q XTFF64 XXXXX	Tape and Reel, 1000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Voltage Range (with Respect to GND)
- V_{AVDD} ..... -0.3V to 6V
- V_{DVDD} ..... -0.3V to 6V
- V_{IOVDD} ..... -0.3V to 6V
- V_{AVCC} ..... -0.3V to 18V
- V_{AVSSA} ..... -13V to 0.3V
- V_{AVSSB}, V_{AVSSC}, V_{AVSSD} to V_{AVSSA} ..... -0.3V to 13V
- V_{AVCC} to V_{AVSSB}, V_{AVSSC}, or V_{AVSSD} ..... -0.3V to 26V
- V_{AVCC} to V_{AVSSA} ..... -0.3V to 26V

DGND to AGND ..... -0.3V to 0.3V

Pin Voltage Range (with Respect to GND)
- ADC_[0-15] Analog Inputs ..... -13V to 13V
- LV_ADC[16-20] Analog Inputs ..... -0.3V to V_{AVDD} + 0.3V
- DAC_A[0-3] Outputs ..... V_{AVSSA} - 0.3V to V_{AVCC} + 0.3V
- DAC_B[4-7] Outputs ..... V_{AVSSB} - 0.3V to V_{AVCC} + 0.3V
- DAC_C[8-11] Outputs ..... V_{AVSSC} - 0.3V to V_{AVCC} + 0.3V
- DAC_D[12-15] Outputs ..... V_{AVSSD} - 0.3V to V_{AVCC} + 0.3V
- REF_CMP ..... -0.3V to V_{AVDD} + 0.3V
- nCS, SCLK, SDI and nRESET ..... -0.3V to V_{IOVDD} + 0.3V
- SDO ..... -0.3V to V_{IOVDD} + 0.3V
- GPIO[0-7] ..... -0.3V to V_{IOVDD} + 0.3V

ADC_[0-15] Analog Input Current ..... -10mA to 10mA

LV_ADC[16-20] Analog Input Current ..... -10mA to 10mA

GPIO[0-7] Sinking Current 5mA

Package Thermal Resistance

TQFP-10×10-64L (Exposed Pad), θ_{JA} ..... 23℃/W

Junction Temperature ..... +150℃

Storage Temperature Range ..... -65℃ to +150℃

Lead Temperature (Soldering, 10s) ..... +260℃

ESD Susceptibility

HBM 2000V

CDM 500V

RECOMMENDED OPERATING CONDITIONS

V_{AVDD} ..... 4.7V to 5.5V

V_{DVDD} (1) ..... 4.7V to 5.5V

V_{IOVDD} (2) ..... 1.8V to 5.25V

V_{AVCC} ..... 4.7V to 12.5V

V_{AVSSA} ..... -12.5V to 0V

V_{AVSSB}, V_{AVSSC}, V_{AVSSD} ..... V_{AVSSA} to 0V

Specified Operating Temperature Range ..... -40℃ to +105℃

Operating Temperature Range ..... -40℃ to +125℃

NOTES:

1. The supply voltage potential of the DVDD pin must be equal to that of the AVDD pin.
2. The supply voltage potential of the IOVDD pin must not be higher than that of the DVDD pin.

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

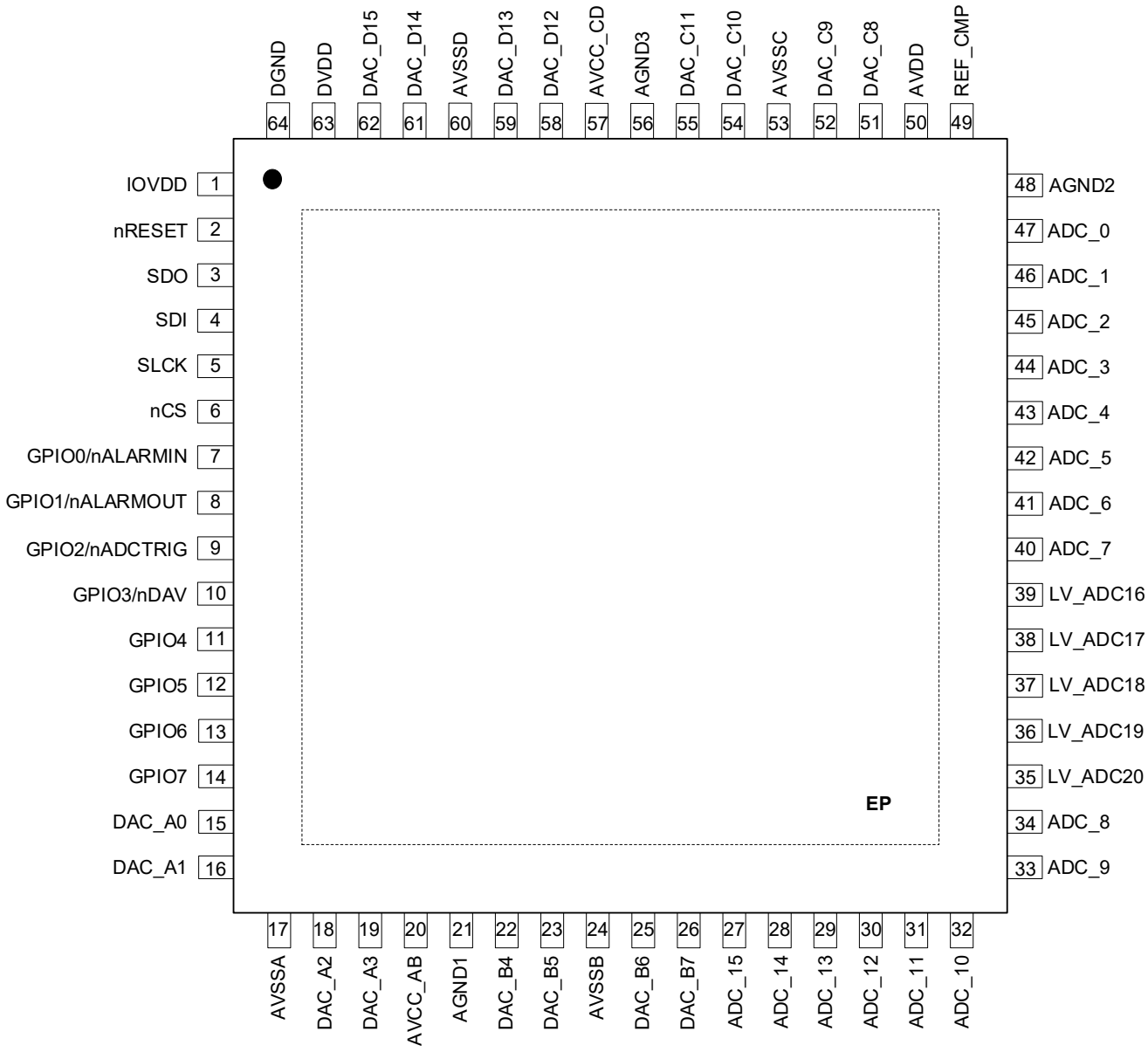
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

(TOP VIEW)



TQFP-10×10-64L (Exposed Pad)

PIN DESCRIPTION

PIN	NAME	I/O	FUNCTION
1	IOVDD	I	Digital Interface Input/Output Power Supply. It can be operated from 1.8V to 5.25V. The supply voltage potential of the IOVDD pin must not be higher than that of the DVDD pin.
2	nRESET	I	Hardware Reset Input Pin. It is active low.
3	SDO	O	Serial Data Output Pin. When nCS pin is pulled high, SDO is in high-impedance. When nCS pin is low, the data is shifted out by this pin at each falling edge of the SCLK.
4	SDI	I	Serial Data Input Pin. Data is shifted in at each rising edged of the SCLK.
5	SCLK	I	Serial Interface Clock Pin.
6	nCS	I	Chip Select Pin. This pin also works as the data frame synchronization signal. It is active low.
7	GPIO0/nALARMIN	I/O	General Purpose Digital Input/Output Pin0 (default). It is a bidirectional pin which has an internal 60kΩ resistor pulled up to IOVDD. This pin can be alternatively configured as nALARMIN input pin, which is an active low input signal. This pin can be floated if it is not used.
8	GPIO1/nALARMOUT	I/O	General Purpose Digital Input/Output Pin1 (default). It is a bidirectional pin which has an internal 60kΩ resistor pulled up to IOVDD. This pin can be alternatively configured as nALARMOUT output pin, which is an open-drain output. If there is an alarm event is generated, it outputs low. This pin can be floated if it is not used.
9	GPIO2/nADCTRIG	I/O	General Purpose Digital Input/Output Pin2 (default). It is a bidirectional pin which has an internal 60kΩ resistor pulled up to IOVDD. This pin can be alternatively configured as nADCTRIG input pin, which is an active low input signal. The falling edge of nADCTRIG starts ADC sampling and conversion. This pin can be floated if it is not used.
10	GPIO3/nDAV	I/O	General Purpose Digital Input/Output Pin3 (default). It is a bidirectional pin which has an internal 60kΩ resistor pulled up to IOVDD. This pin can be alternatively configured as nDAV output pin, which is an active low signal that indicates data are available. When the device is in direct mode, the nDAV goes low if the conversion ends. When the device is in auto mode, it will generate a 1μs pulse on nDAV pin if a conversion cycle is completed. When it is in deactivated state, nDAV pin remains high. This pin can be floated if it is not used.
11	GPIO4	I/O	General Purpose Digital Input/Output Pins. These pins are bidirectional pins which each have an internal 60kΩ resistor pulled up to IOVDD. If they are not used, these pins can be floated.
12	GPIO5	I/O	
13	GPIO6	I/O	
14	GPIO7	I/O	
15	DAC_A0	O	DAC Group A. All DACs in group A have the same output range and clamp voltage. When one of the DACs works in a negative range, the others must also be in a negative range.
16	DAC_A1	O	
17	AVSSA	I	This pin is the negative power supply of DAC group A. It sets the power-on-reset and clamp voltage potential of the DAC group A.
18	DAC_A2	O	DAC Group A. All DACs in group A have the same output range and clamp voltage. When one of the DACs works in a negative range, the others must also be in a negative range.
19	DAC_A3	O	
20	AVCC_AB	I	This pin is the positive analog power of DAC group A and group B. Care should be taken that AVCC_AB and AVCC_CD must have the same voltage potential (AVCC).

PIN DESCRIPTION (continued)

PIN	NAME	I/O	FUNCTION
21	AGND1	I	Analog Ground. This pin is the ground of the analog circuits of the chip. AGND1, AGND2 and AGND3 must be connected to same reference point (AGND).
22	DAC_B4	O	DAC Group B. All DACs in group B have the same output range and clamp voltage. When one of the DACs works in a negative range, the others must also be in a negative range.
23	DAC_B5	O	
24	AVSSB	I	This pin is the negative power supply of DAC group B. It sets the power-on-reset and clamp voltage potential of the DAC group B.
25	DAC_B6	O	DAC Group B. All DACs in group B have the same output range and clamp voltage. When one of the DACs works in a negative range, the others must also be in a negative range.
26	DAC_B7	O	
27	ADC_15	I	Bipolar Analog Inputs. The input voltage range is between -12.5V and 12.5V.
28	ADC_14	I	
29	ADC_13	I	
30	ADC_12	I	
31	ADC_11	I	Bipolar Analog Inputs. The input voltage range is between -12.5V and 12.5V.
32	ADC_10	I	
33	ADC_9	I	
34	ADC_8	I	
35	LV_ADC20	I	General Purpose Analog Inputs. The input voltage is between 0 and 2 × V_{REF}.
36	LV_ADC19	I	
37	LV_ADC18	I	
38	LV_ADC17	I	
39	LV_ADC16	I	
40	ADC_7	I	Bipolar Analog Inputs. The input voltage range is between -12.5V and 12.5V.
41	ADC_6	I	
42	ADC_5	I	
43	ADC_4	I	
44	ADC_3	I	Bipolar Analog Inputs. The input voltage range is between -12.5V and 12.5V.
45	ADC_2	I	
46	ADC_1	I	
47	ADC_0	I	

PIN DESCRIPTION (continued)

PIN	NAME	I/O	FUNCTION
48	AGND2	I	Analog Ground. This pin is the ground of the analog circuits of the chip. AGND1, AGND2 and AGND3 must be connected to same reference point (AGND).
49	REF_CMP	O	Internal Reference Decoupling Pin. Connect it with a 4.7μF capacitor to AGND2 pin. Be noted that it will take about 5ms for the REF_CMP voltage fully settling after the ADC_REF_BUFF bit (which is D[4] in ADC configuration register) is enabled from a previous disabled status and at same time at least one ADC channel is selected in ADC MUX configuration registers (which is set by registers 0x13 to 0x15). Before the REF_CMP voltage fully settles, any ADC conversion result is untrusted, and any ADC conversion operation is not recommended. The REF_CMP voltage settling time depends on the decoupling capacitor. The REF_CMP voltage settling time is a setting time when the internal reference source charges to the external decoupling capacitor. The REF_CMP voltage does not need a settling time when the ADC_REF_BUFF bit is enabled from a previous enabled status and any ADC channels that are selected by ADC MUX configuration registers are re-configured. For all the upping explanations, assume that the internal reference is already enabled by setting PREF bit (which is configured in register 0xB4).
50	AVDD	I	Analog Supply Voltage (4.7V to 5.5V). The voltages of AVDD and DVDD pins must be same.
51	DAC_C8	O	DAC Group C. All DACs in group C have the same output range and clamp voltage. When one of the DACs works in a negative range, the others must also be in a negative range.
52	DAC_C9	O	
53	AVSSC	I	This pin is the negative power supply of DAC group C. It sets the power-on-reset and clamp voltage potential of the DAC group C.
54	DAC_C10	O	DAC Group C. All DACs in group C have the same output range and clamp voltage. When one of the DACs works in a negative range, the others must also be in a negative range.
55	DAC_C11	O	
56	AGND3	I	Analog Ground. This pin is the ground of the analog circuits of the chip. AGND1, AGND2 and AGND3 must be connected to same reference point (AGND).
57	AVCC_CD	I	This pin is the positive analog power of DAC group C and group D. Care should be taken that AVCC_AB and AVCC_CD must have the same voltage potential (AVCC).
58	DAC_D12	O	DAC Group D. All DACs in group D have the same output range and clamp voltage. When one of the DACs works in a negative range, the others must also be in a negative range.
59	DAC_D13	O	
60	AVSSD	I	This pin is the negative power supply of DAC group D. It sets the power-on-reset and clamp voltage potential of the DAC group D.
61	DAC_D14	O	DAC Group D. All DACs in group D have the same output range and clamp voltage. When one of the DACs works in a negative range, the others must also be in a negative range.
62	DAC_D15	O	
63	DVDD	I	Digital Supply Voltage (4.7V to 5.5V). The voltages of AVDD and DVDD pins must be same.
64	DGND	I	Digital Ground. This pin is the ground of the digital circuits of the chip.
Exposed Pad	EP	I	Exposed Pad. It should be connected to the same potential as the AVSSA pin or left open.

NOTE: I = input, O = output, I/O = input and output.

ELECTRICAL CHARACTERISTICS

DAC

(V_{AVDD} = V_{DVDD} = 4.7V to 5.5V, V_{AVCC} = 12V, V_{IOVDD} = 1.8V to 5.25V, AGND = DGND = 0V, V_{AVSSA} = V_{AVSSB} = V_{AVSSC} = V_{AVSSD} = -12V (for DAC groups in negative range) or 0V (for DAC groups in positive ranges), DAC output range = 0V to 10V for all groups, no load on the DACs, T_A = -40℃ to +105℃, typical values are at T_A = +25℃, the following electrical ratings apply to all specifications in this datasheet, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
DAC DC Accuracy						
Resolution			12			Bits
Relative Accuracy (INL)	0V to 10V and -10V to 0V ranges (measured codes 020h and FE0h)		-3.2	-0.3/1.2	5.5	LSB
	0V to 5V and -5V to 0V ranges (measured codes 020h and FE0h)		-3.5	-0.3/1.2	5.5	
Differential Nonlinearity (DNL)	Specified monotonic. 0V to 10V and -10V to 0V ranges (measured codes 020h and FE0h)		-0.99	±0.3	0.99	LSB
	Specified monotonic. 0V to 5V and -5V to 0V ranges (measured codes 020h and FE0h)		-0.99	±0.3	0.99	
Total Unadjusted Error (1) (TUE)	T_A = +25℃	0V to 10V range	-144	-8.9/2.3	90	mV
		-10V to 0V range	-117	-1.2/9.5	156	
		0V to 5V range	-77	-6.9/5.1	74	
		-5V to 0V range	-62	-2.4/10.0	99	
Offset Error	0V to 10V range (measured codes 020h and FE0h)		-72	2.4	74	mV
	0V to 5V range (measured codes 020h and FE0h)		-75	4	80	
Zero-Code Error	T_A = +25℃	Code 000h, -10V to 0V range	-137	20	174	mV
		Code 000h, -5V to 0V range	-85	10	107	
Gain Error (1)	0V to 10V range (measured codes 020h and FE0h)		-1.75	-0.20	1.30	%FSR
	-10V to 0V range (measured codes 020h and FE0h)		-1.70	-0.20	1.30	
	0V to 5V range (measured codes 020h and FE0h)		-1.70	-0.20	1.35	
	-5V to 0V range (measured codes 020h and FE0h)		-1.70	-0.20	1.35	
Offset Temperature Coefficient	0V to 10V range			1		ppm/℃
	0V to 5V range			1.5		
Zero-Code Temperature Coefficient	-10V to 0V range			2		ppm/℃
	-5V to 0V range			2		
Gain Temperature Coefficient (1)	0V to 10V range			1		ppm/℃
	-10V to 0V range			1.5		
	0V to 5V range			3		
	-5V to 0V range			3		

NOTE:

1. The contribution of internal reference is not included.

ELECTRICAL CHARACTERISTICS (continued)

DAC (continued)

(V_{AVDD} = V_{DVDD} = 4.7V to 5.5V, V_{AVCC} = 12V, V_{IOVDD} = 1.8V to 5.25V, AGND = DGND = 0V, V_{AVSSA} = V_{AVSSB} = V_{AVSSC} = V_{AVSSD} = -12V (for DAC groups in negative range) or 0V (for DAC groups in positive ranges), DAC output range = 0V to 10V for all groups, no load on the DACs, T_A = -40℃ to +105℃, typical values are at T_A = +25℃, the following electrical ratings apply to all specifications in this datasheet, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
DAC Output Characteristics					
Full-Scale Output Voltage Range (2)	DAC_RANGEn[2:0] = 100	-10		0	V
	DAC_RANGEn[2:0] = 101	-5		0	
	DAC_RANGEn[2:0] = 110	0		10	
	DAC_RANGEn[2:0] = 111	0		5	
Output Voltage Settling Time	Transition: Code 400h to C00h to within ½ LSB, R_L = 2kΩ, C_L = 200pF. 0V to 10V and -10V to 0 V ranges		5		μs
	Transition: Code 400h to C00h to within ½ LSB, R_L = 2kΩ, C_L = 200pF. 0V to 5V and -5V to 0V ranges		5		
Slew Rate	Transition: Code 400h to C00h, 10% to 90%, R_L = 2kΩ, C_L = 200pF. 0V to 10V and -10V to 0V ranges		4		V/μs
	Transition: Code 400h to C00h, 10% to 90%, R_L = 2kΩ, C_L = 200pF. 0V to 5V and -5V to 0V ranges		4		
Short Circuit Current	Full-scale current shorted to the DAC group AVSS or AVCC voltage		±45		mA
Load Current (3)	Source or sink with 1V headroom from the DAC group AVCC or AVSS voltage, voltage drop < 25mV	±15			mA
	Source or sink with 300mV headroom from the DAC group AVCC or AVSS voltage, voltage drop < 25mV	±10			
Maximum Capacitive Load (4)	R_L = ∞, the capability of load of cap directly	0		10	nF
DC Output Impedance	Code set to 800h, ±15mA		0.2		Ω
Power-On Overshoot	V_{AVCC} = 12V, V_{AVSSA} = V_{AVSSB} = V_{AVSSC} = V_{AVSSD} = 0V to -12V, 2ms ramp		30		mV
Glitch Energy	Transition: Code 7FFh to 800h; 800h to 7FFh		1		nV-s
Output Noise	1kHz, code 800h, includes internal reference noise		1000		$nV/\sqrt{Hz}$
	Integrated noise from 0.1Hz to 10Hz, code 800h, includes internal reference noise		100		μV_{PP}
Clamp Outputs					
Clamp Output Voltage (5)	DAC output range: 0V to 10V, AVSS = AGND		0		V
	DAC output range: 0V to 5V, AVSS = AGND		0		
	DAC output range: -10V to 0V, V_{AVSS} = -12V		V_{AVSS}		
	DAC output range: -5V to 0V, V_{AVSS} = -6V		V_{AVSS}		
Clamp Output Impedance			80		Ω

NOTES:

2. The output voltage range of each DAC must be within the positive power supply rail AVCC pin (AVCC_AB or AVCC_CD) and the negative power supply rail AVSS pin (AVSSA, AVSSB, AVSSC or AVSSD).

3. Make sure that the thermal condition of the chip is within restricted if all channels are loaded simultaneously.

4. To be sampled with limited samples, not guaranteed by production testing.

5. Tested under the condition that DAC output is floated.

ELECTRICAL CHARACTERISTICS (continued)

ADC and Temperature Sensor

(V_{AVDD} = V_{DVDD} = 4.7V to 5.5V, V_{AVCC} = 12V, V_{IOVDD} = 1.8V to 5.25V, AGND = DGND = 0V, V_{AVSSA} = V_{AVSSB} = V_{AVSSC} = V_{AVSSD} = -12V (for DAC groups in negative range) or 0V (for DAC groups in positive ranges), DAC output range = 0V to 10V for all groups, no load on the DACs, T_A = -40℃ to +105℃, typical values are at T_A = +25℃, the following electrical ratings apply to all specifications in this datasheet, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Resolution			12			Bits
Integral Nonlinearity	Unipolar input channels		-1.7	±0.5	2.2	LSB
	Bipolar input channels		-1.5	±0.5	1.5	
Differential Nonlinearity	Specified monotonic. All input channels		-0.99	±0.5	0.99	LSB
Unipolar Analog Inputs: LV_ADC16 to LV_ADC20						
Absolute Input Voltage Range			AGND - 0.2		V_{AVDD} + 0.2	V
Full Scale Input Range	V_{REF} measured at REF_CMP pin		0		2 × V_{REF}	V
Input Capacitance				15		pF
DC Input Leakage Current	Unselected ADC input		-10		10	μA
Offset Error			-3	-0.7	1.5	LSB
Offset Error Match				±0.2		LSB
Gain Error (1)			-3	0.6	4	LSB
Gain Error Match				±0.3		LSB
Update Time	Single unipolar input, temperature sensor disabled			12.5		μs
Bipolar Analog Inputs: ADC_0 to ADC_15						
Absolute Input Voltage Range			-13		13	V
Full Scale Input Range			-12.5		12.5	V
Input Resistance				120		kΩ
Offset Error			-7.5	0.45	9.2	LSB
Gain Error (1)			-28	-8.3	11	LSB
Update Time	Single bipolar input, temperature sensor disabled			26		μs
Temperature Sensor						
Operating Range			-40		125	℃
Accuracy	V_{AVDD} = 5V			±2	±6	℃
Resolution	LSB size			0.25		℃
Update Time	All ADC input channels disabled			258		μs
ADC Update Time						
Internal Oscillator Frequency			3.7	4	4.4	MHz
ADC Update Time	All 21 ADC inputs enabled, temperature sensor disabled			465		μs
	All 21 ADC inputs enabled, temperature sensor enabled			720		μs
Internal Reference						
Initial Accuracy	T_A = +25℃	After aging	2.49	2.5	2.51	V
		Before aging	2.497	2.5	2.503	
Reference Temperature Coefficient				5		ppm/℃

ELECTRICAL CHARACTERISTICS (continued)

General

(V_{AVDD} = V_{DVDD} = 4.7V to 5.5V, V_{AVCC} = 12V, V_{IOVDD} = 1.8V to 5.25V, AGND = DGND = 0V, V_{AVSSA} = V_{AVSSB} = V_{AVSSC} = V_{AVSSD} = -12V (for DAC groups in negative range) or 0V (for DAC groups in positive ranges), DAC output range = 0V to 10V for all groups, no load on the DACs, T_A = -40℃ to +105℃, typical values are at T_A = +25℃, the following electrical ratings apply to all specifications in this datasheet, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
AVSS Detector					
AVSS Threshold Detector (V_{AVSSTH})		-3.5		-1.5	V
Digital Logic: GPIO					
High-Level Input Voltage	V_{IOVDD} = 1.8V to 5.25V	0.75 × V_{IOVDD}			V
Low-Level Input Voltage	V_{IOVDD} = 1.8V			0.45	V
	V_{IOVDD} = 2.7V to 5.25V			0.3 × V_{IOVDD}	
Low-Level Output Voltage	V_{IOVDD} = 1.8V, I_{LOAD} = -2mA			0.4	V
	V_{IOVDD} = 5.25V, I_{LOAD} = -5mA			0.4	
Input Impedance	To IOVDD		60		kΩ
Digital Logic: All Except GPIO					
High-Level Input Voltage	V_{IOVDD} = 1.8V to 5.25V	0.75 × V_{IOVDD}			V
Low-Level Input Voltage	V_{IOVDD} = 1.8V			0.45	V
	V_{IOVDD} = 2.7V to 5.25V			0.3 × V_{IOVDD}	V
High-Level Output Voltage	I_{LOAD} = -1mA	V_{IOVDD} - 0.4			V
Low-Level Output Voltage	I_{LOAD} = 1mA			0.4	V
High Impedance Leakage		-5		5	μA
High Impedance Output Capacitance			5		pF
Power Requirements					
AVDD Supply Current (I_{AVDD})	No DAC load, all DACs at 800h code and ADC at the fastest auto conversion rate		3.9	6	mA
AVCC Supply Current (I_{AVCC})			2.3	5	
AVSS Supply Current (I_{AVSS})		-5	-2.5		
DVDD Supply Current (I_{DVDD})			1.4	3	
IOVDD Supply Current (I_{IODD})			10	20	μA
Power Consumption			100		mW
AVDD Supply Current (I_{AVDD})	Power-down mode		0.04	0.1	mA
AVCC Supply Current (I_{AVCC})			0.3	1	
AVSS Supply Current (I_{AVSS})		-1	-0.6		
DVDD Supply Current (I_{DVDD})			0.12	0.2	
IOVDD Supply Current (I_{IODD})			10	18	μA
Power Consumption			20		mW

TIMING REQUIREMENTS

(V_{AVDD} = V_{DVDD} = 4.7V to 5.5V, V_{AVCC} = 12V, V_{AVSSA} = -12V, AGND = DGND = V_{AVSSB} = V_{AVSSC} = V_{AVSSD} = 0V, DAC output range = 0V to 10V for all groups, no load on the DACs, T_A = -40℃ to +105℃, typical values are at T_A = +25℃, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Serial Interface (1)					
SCLK Frequency (f_{SCLK})	V_{IOVDD} = 1.8V to 2.7V			20	MHz
	V_{IOVDD} = 2.7V to 5.25V			20	
SCLK Period (2) (t_1)	V_{IOVDD} = 1.8V to 2.7V	50			ns
	V_{IOVDD} = 2.7V to 5.25V	50			
SCLK Pulse Width High (2) (t_2)	V_{IOVDD} = 1.8V to 2.7V	23			ns
	V_{IOVDD} = 2.7V to 5.25V	23			
SCLK Pulse Width Low (2) (t_3)	V_{IOVDD} = 1.8V to 2.7V	23			ns
	V_{IOVDD} = 2.7V to 5.25V	23			
SDI Setup (2) (t_4)	V_{IOVDD} = 1.8V to 2.7V	10			ns
	V_{IOVDD} = 2.7V to 5.25V	10			
SDI Hold (2) (t_5)	V_{IOVDD} = 1.8V to 2.7V	10			ns
	V_{IOVDD} = 2.7V to 5.25V	10			
SDO Driven to Tri-State (3) (4) (t_6)	V_{IOVDD} = 1.8V to 2.7V	0		15	ns
	V_{IOVDD} = 2.7V to 5.25V	0		12	
SDO Tri-State to Driven (3) (4) (t_7)	V_{IOVDD} = 1.8V to 2.7V	0		23	ns
	V_{IOVDD} = 2.7V to 5.25V	0		15	
SDO Output Delay (3) (4) (t_8)	V_{IOVDD} = 1.8V to 2.7V	0		23	ns
	V_{IOVDD} = 2.7V to 5.25V	0		15	
nCS Setup (2) (t_9)	V_{IOVDD} = 1.8V to 2.7V	6			ns
	V_{IOVDD} = 2.7V to 5.25V	6			
nCS Hold (2) (t_{10})	V_{IOVDD} = 1.8V to 2.7V	20			ns
	V_{IOVDD} = 2.7V to 5.25V	20			
Inter-Access Gap (2) (t_{11})	V_{IOVDD} = 1.8V to 2.7V	10			ns
	V_{IOVDD} = 2.7V to 5.25V	10			
Digital Logic					
Reset Delay; Delay-to-Normal Operation from Reset			2	5	μs
Power-Down Recovery Time				500	μs
Clamp Shutdown Delay			5		μs
Convert Pulse Width		20			ns
Reset Pulse Width		40			ns
ADC WAIT State (5); the Wait Time from when the ADC Enters the IDLE State		2			μs

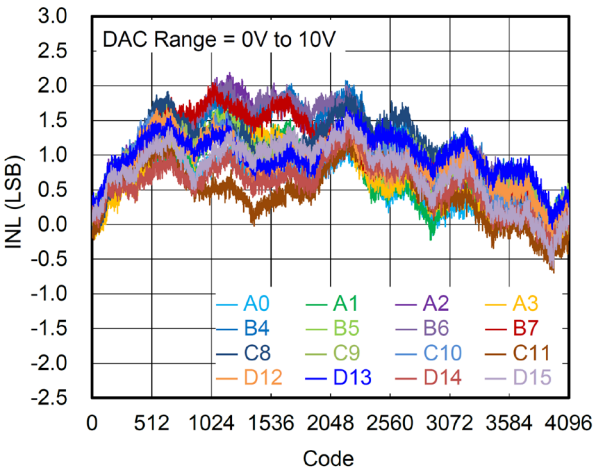
NOTES:

1. Specified by design and tested with limited samples. Not guaranteed by production testing.
2. See Figure 1 and Figure 2.
3. SDO timing specifications when SDO is loaded with 10pF capacitor.
4. See Figure 2.
5. Specified by design and tested with limited samples. Not guaranteed by production testing. Refer to the ADC Sequencing section for more detailed information.

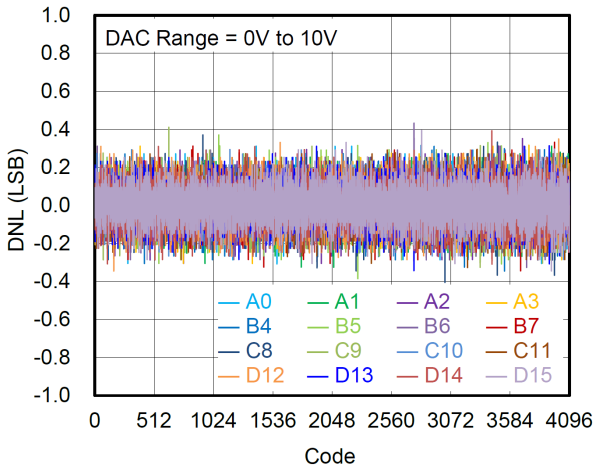
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = +25℃, unless otherwise noted.

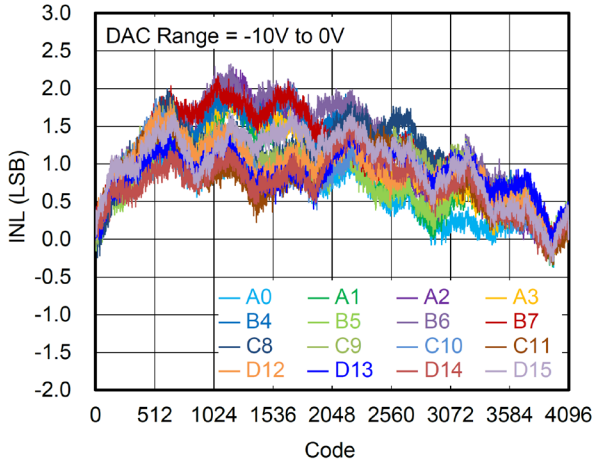
DAC Linearity Error vs. Code



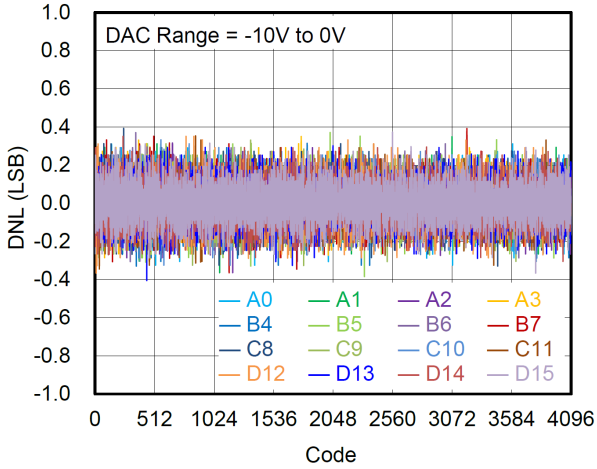
DAC Differential Linearity Error vs. Code



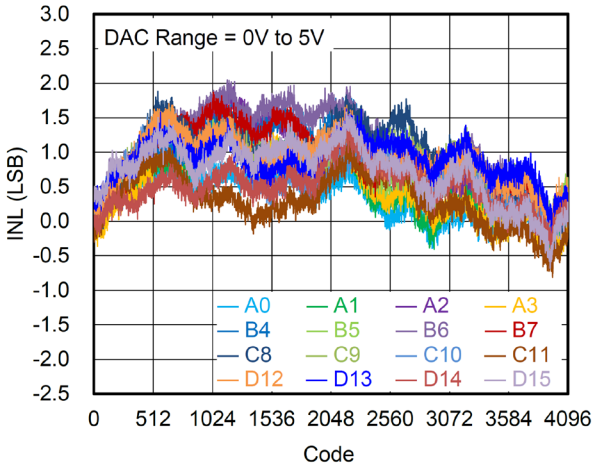
DAC Linearity Error vs. Code



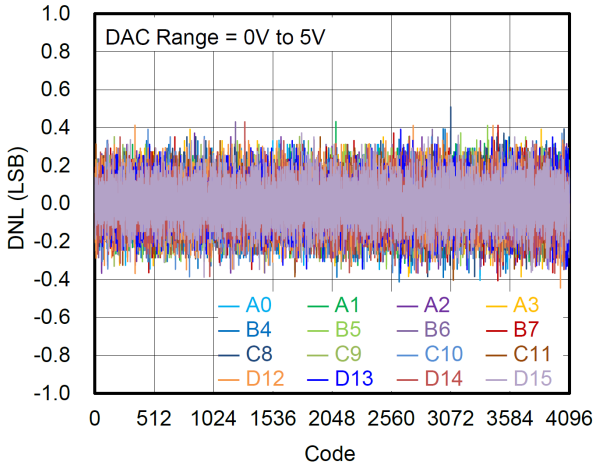
DAC Differential Linearity Error vs. Code



DAC Linearity Error vs. Code



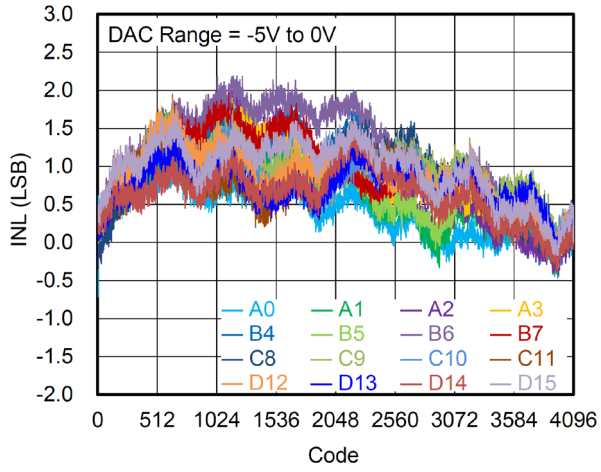
DAC Differential Linearity Error vs. Code



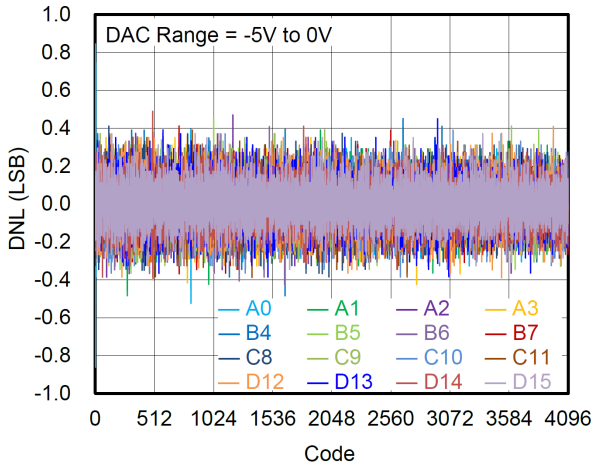
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, unless otherwise noted.

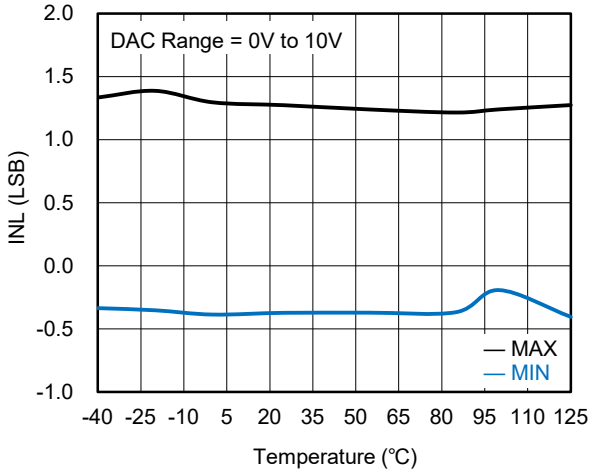
DAC Linearity Error vs. Code



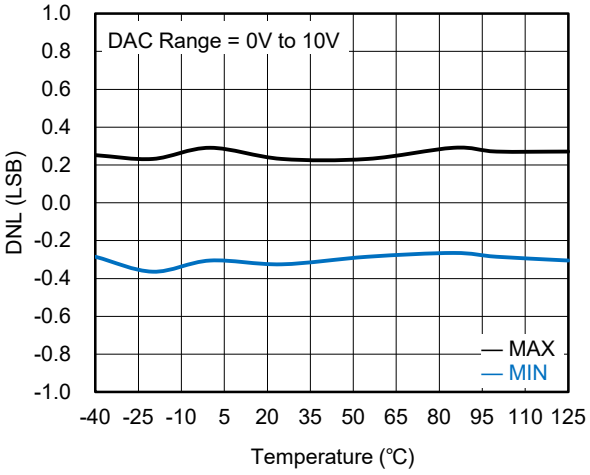
DAC Differential Linearity Error vs. Code



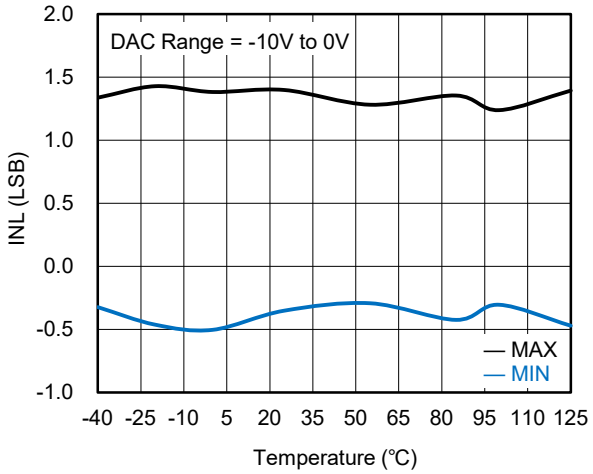
DAC Linearity Error vs. Temperature



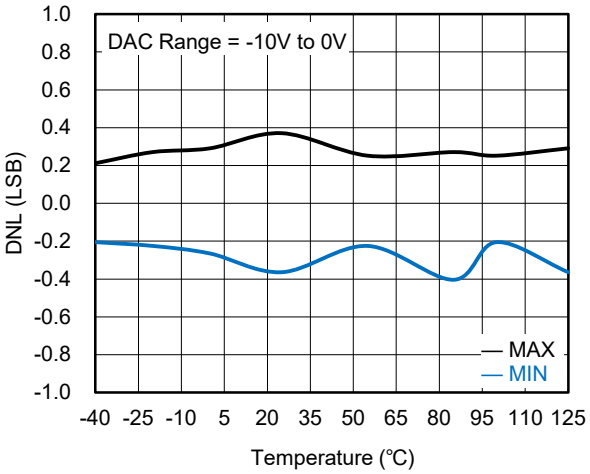
DAC Differential Linearity Error vs. Temperature



DAC Linearity Error vs. Temperature



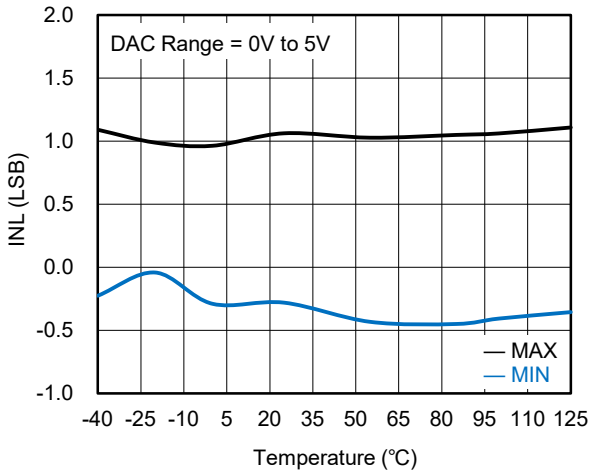
DAC Differential Linearity Error vs. Temperature



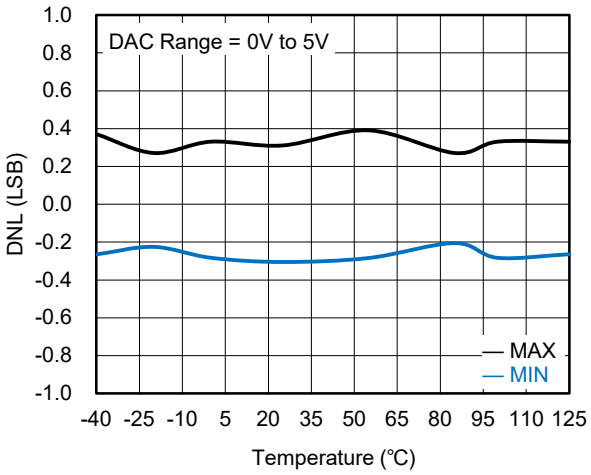
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, unless otherwise noted.

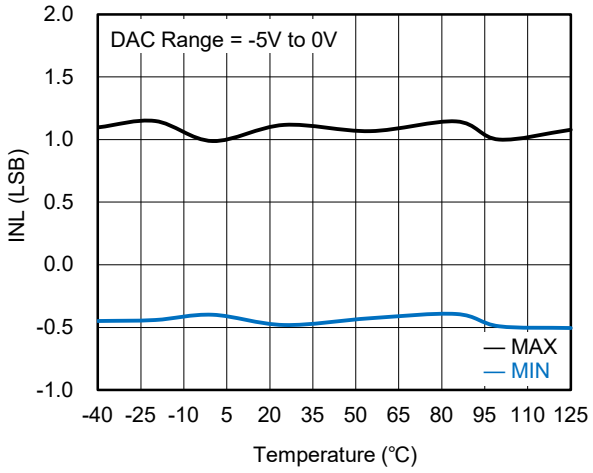
DAC Linearity Error vs. Temperature



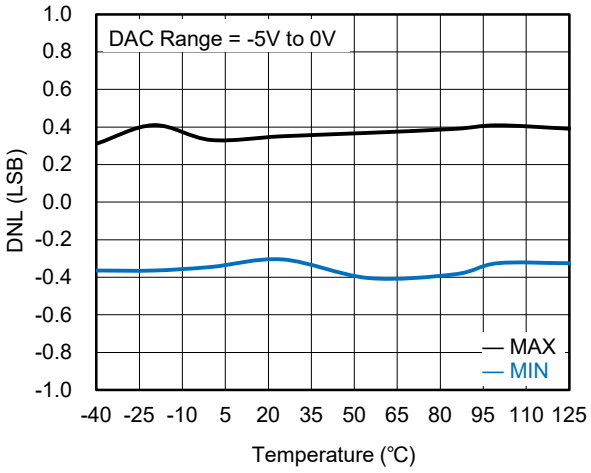
DAC Differential Linearity Error vs. Temperature



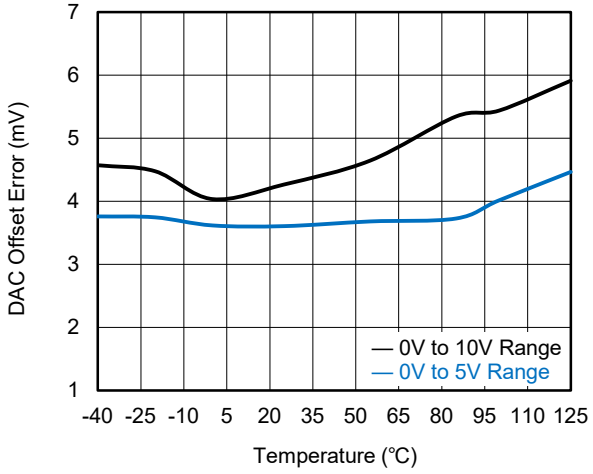
DAC Linearity Error vs. Temperature



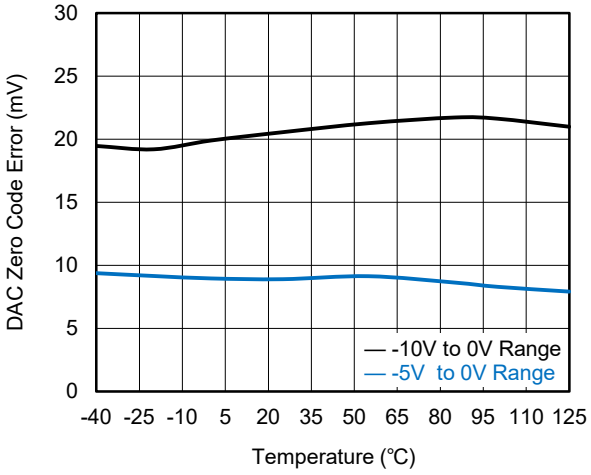
DAC Differential Linearity Error vs. Temperature



DAC Offset Error vs. Temperature



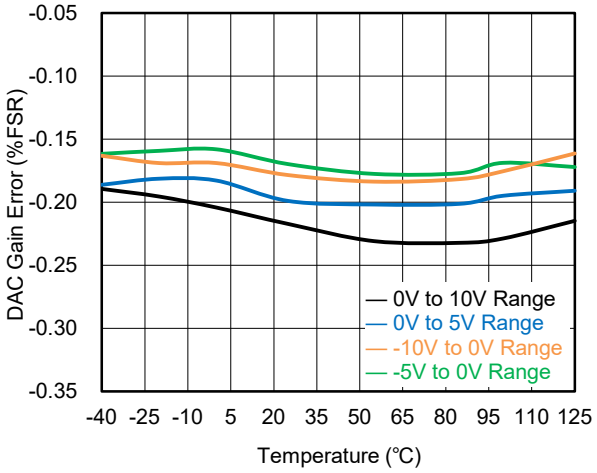
DAC Zero Code Error vs. Temperature



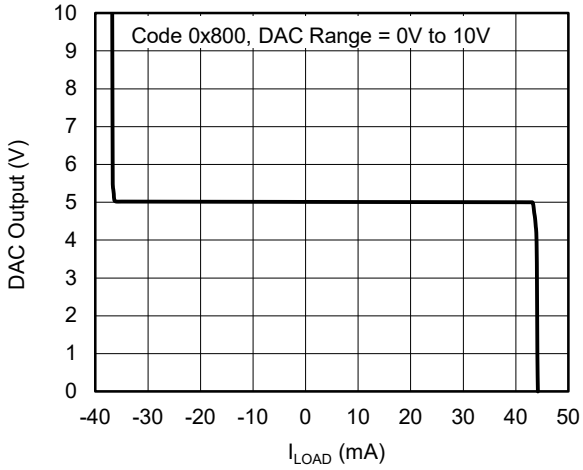
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, unless otherwise noted.

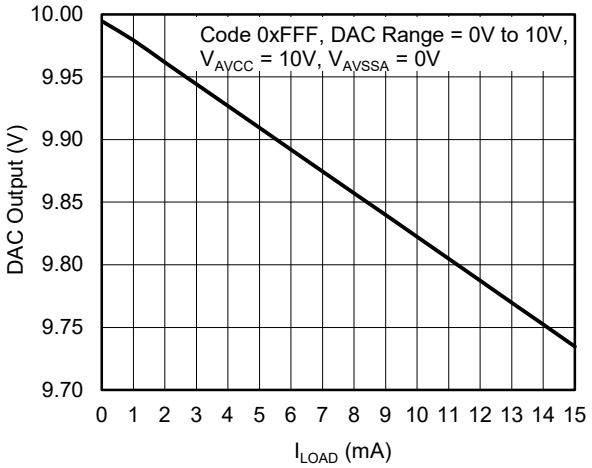
DAC Gain Error vs. Temperature



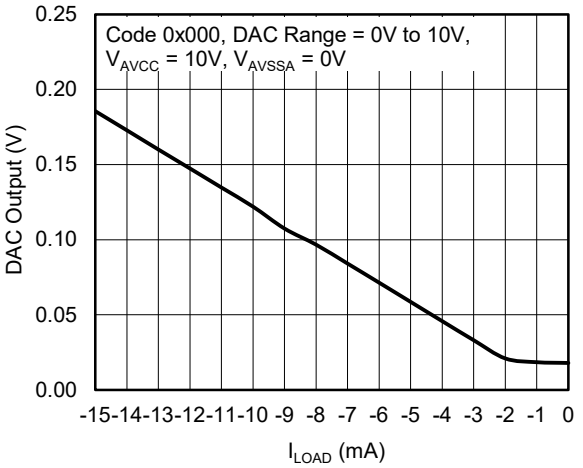
DAC Output Voltage vs. Load Current



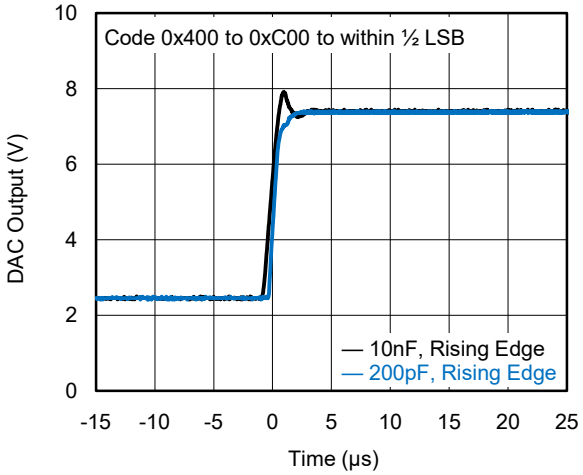
DAC Source Current



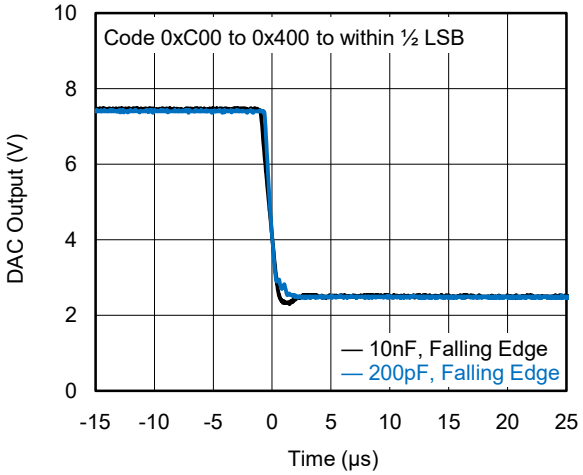
DAC Sink Current



DAC Settling Time



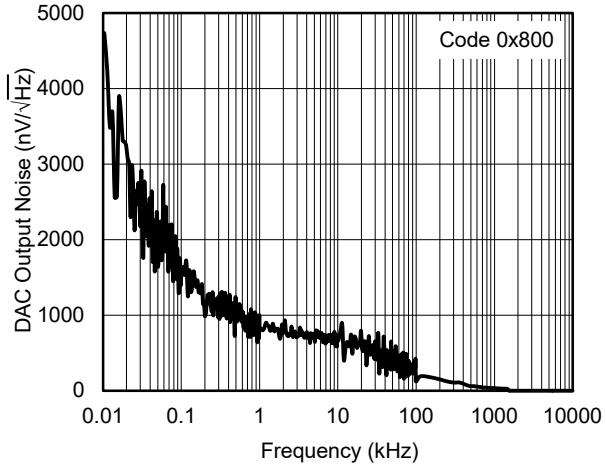
DAC Settling Time



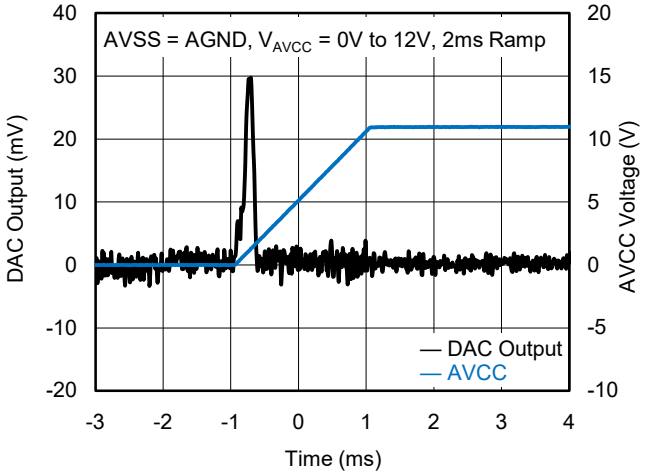
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, unless otherwise noted.

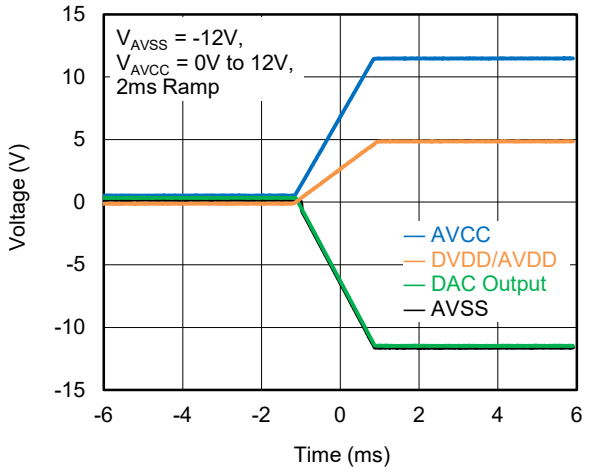
DAC Output Noise vs. Frequency



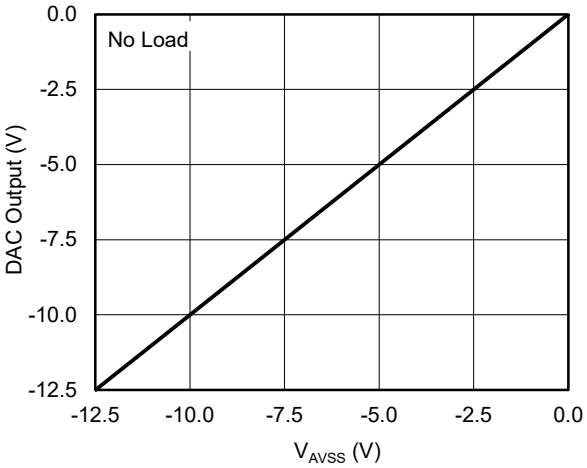
DAC Power On Overshoot, Single Supply



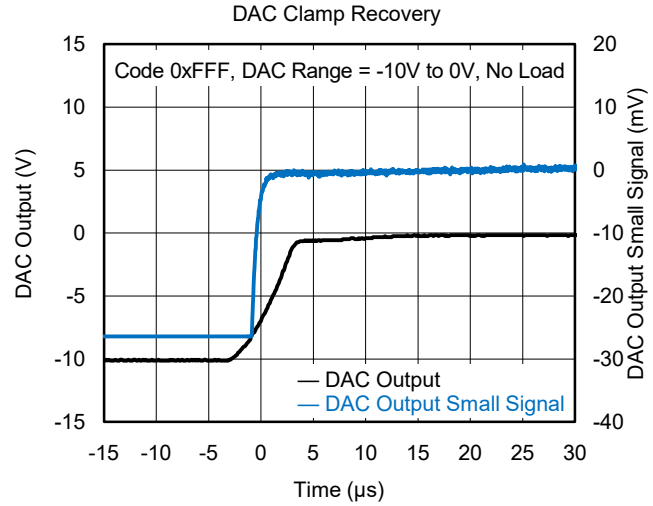
DAC Power On Overshoot, Dual Supply



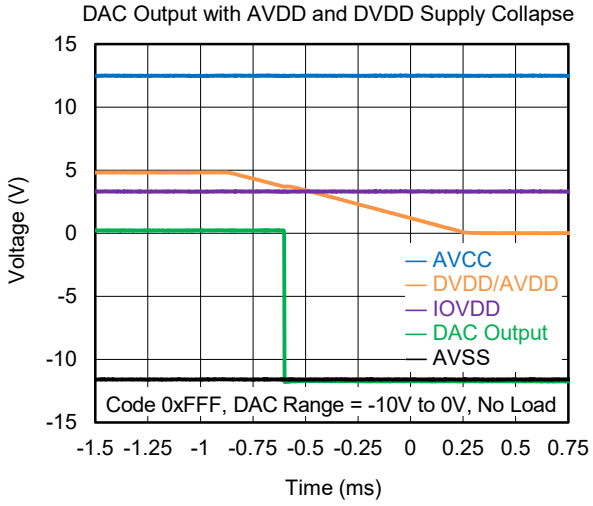
DAC Clamp Output vs. AVSS Voltage



DAC Clamp Recovery



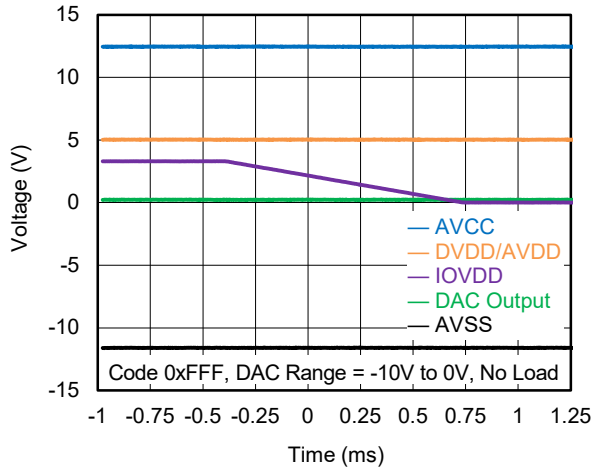
DAC Output with AVDD and DVDD Supply Collapse



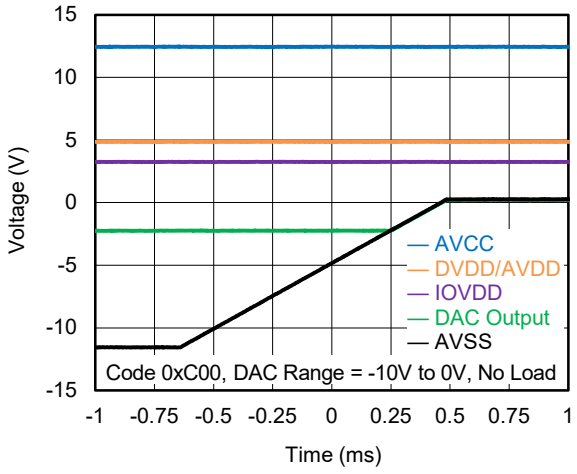
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, unless otherwise noted.

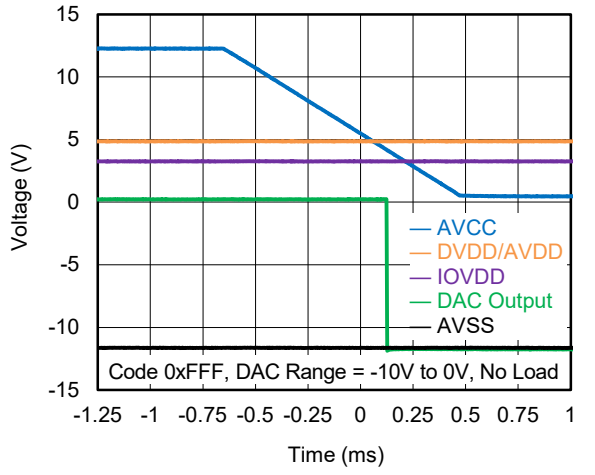
DAC Output with IOVDD Supply Collapse



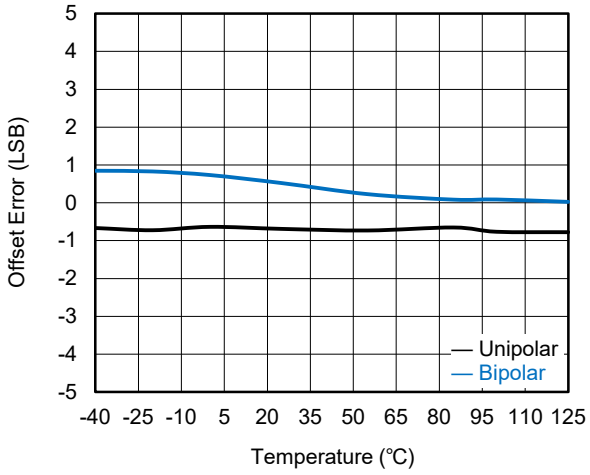
DAC Output with AVSS Supply Collapse



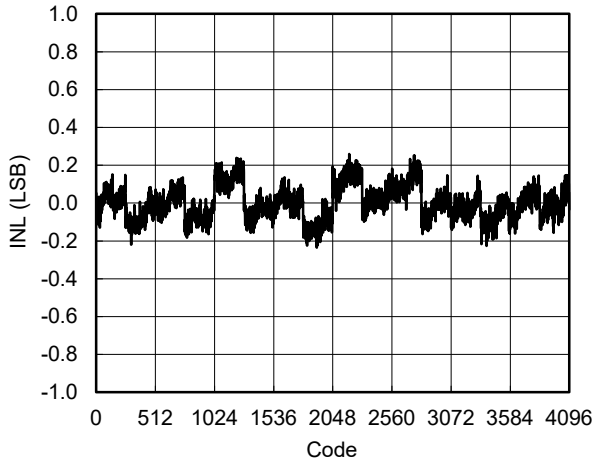
DAC Output with AVCC Supply Collapse



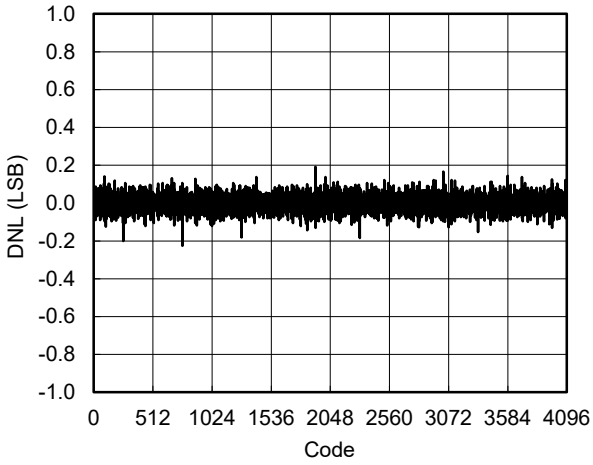
ADC Offset Error vs. Temperature



ADC Linearity Error vs. Code (Unipolar Input)



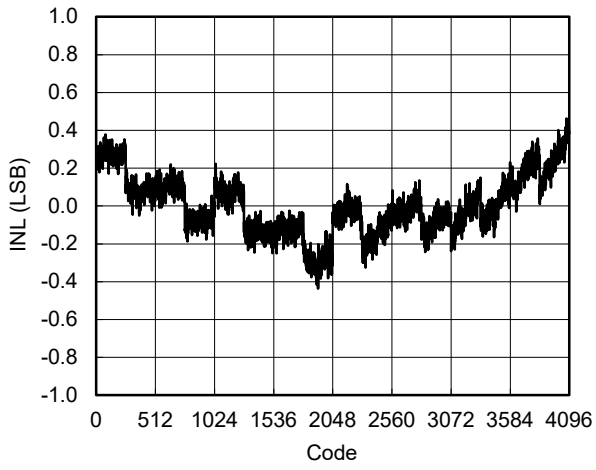
ADC Differential Linearity Error vs. Code (Unipolar Input)



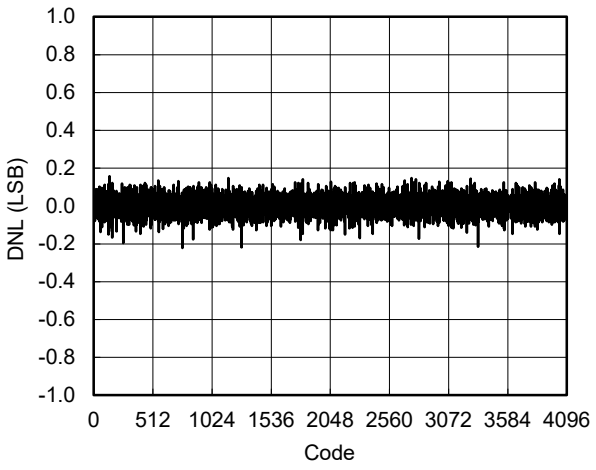
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, unless otherwise noted.

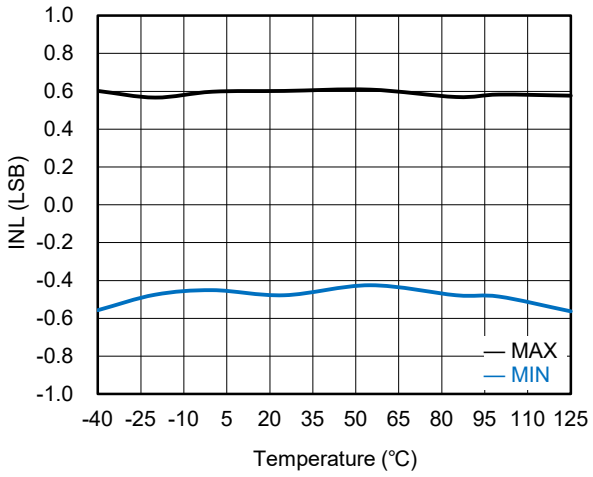
ADC Linearity Error vs. Code (Bipolar Input)



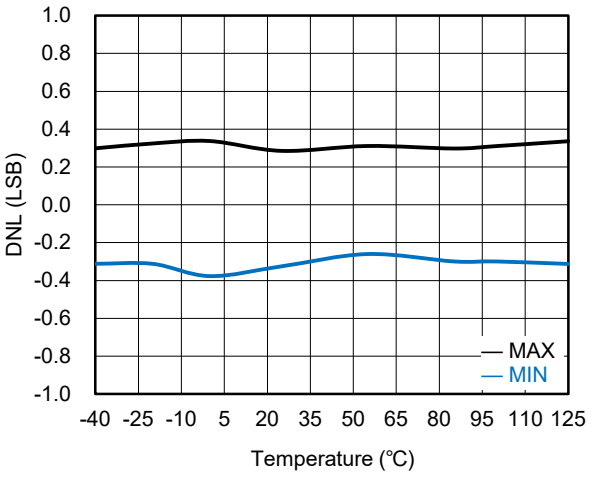
ADC Differential Linearity Error vs. Code (Bipolar Input)



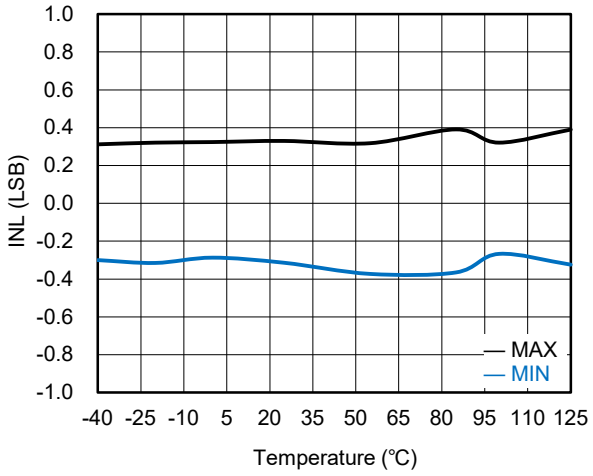
ADC Linearity Error vs. Temperature (Unipolar Input)



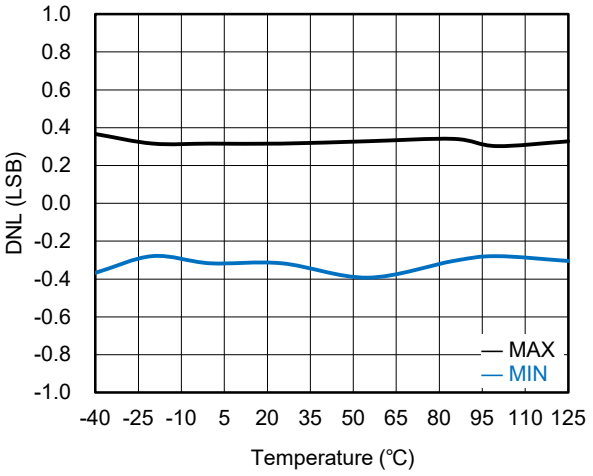
ADC Differential Linearity Error vs. Temperature (Unipolar Input)



ADC Linearity Error vs. Temperature (Bipolar Input)



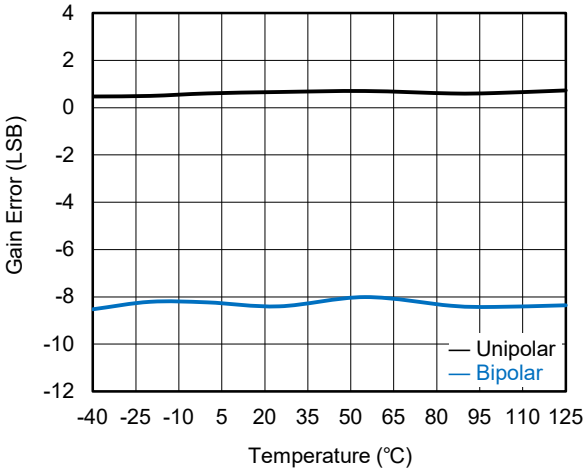
ADC Differential Linearity Error vs. Temperature (Bipolar Input)



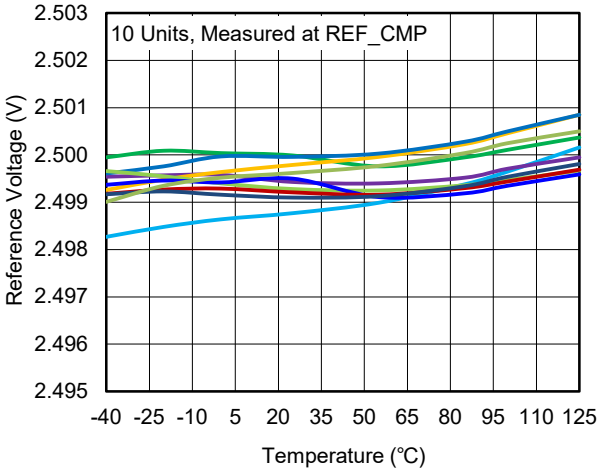
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, unless otherwise noted.

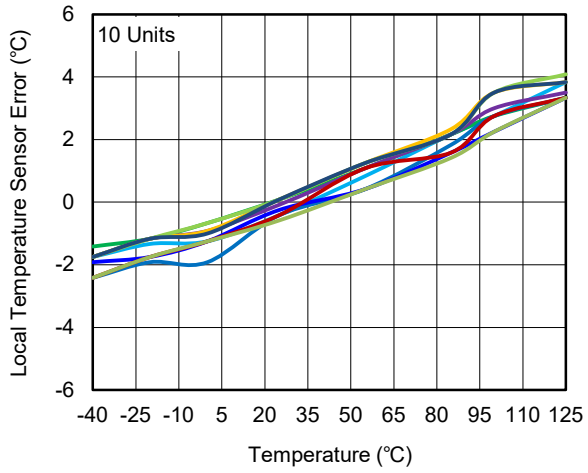
ADC Gain Error vs. Temperature



Reference Voltage vs. Temperature



Temperature Sensor Error vs. Temperature



TIMING DIAGRAMS

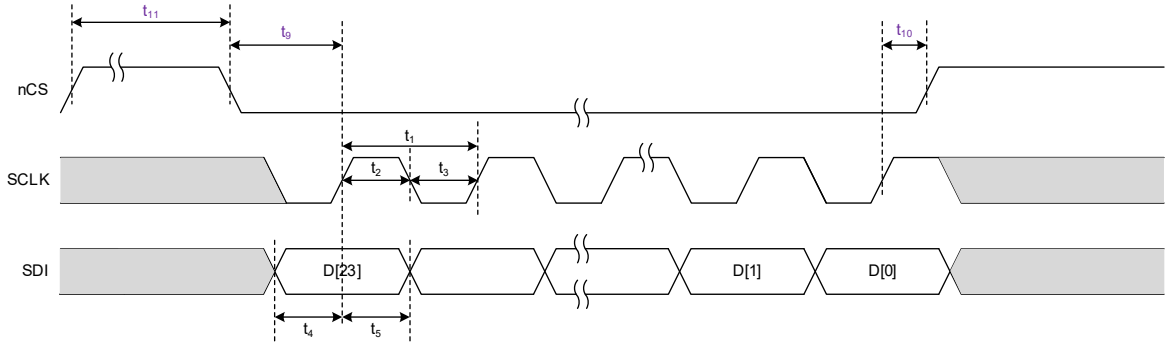


Figure 1. Serial Interface Write Timing Diagram

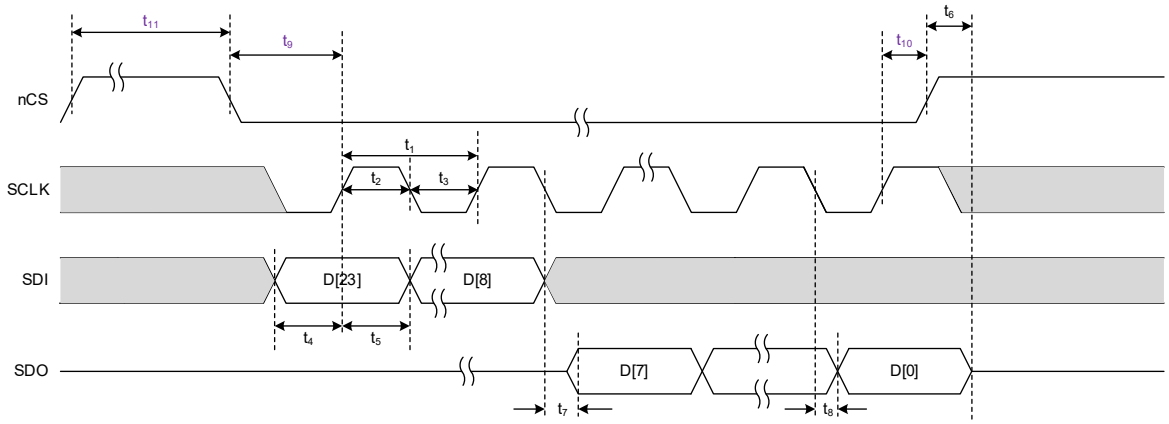


Figure 2. Serial Interface Read Timing Diagram

FUNCTIONAL BLOCK DIAGRAM

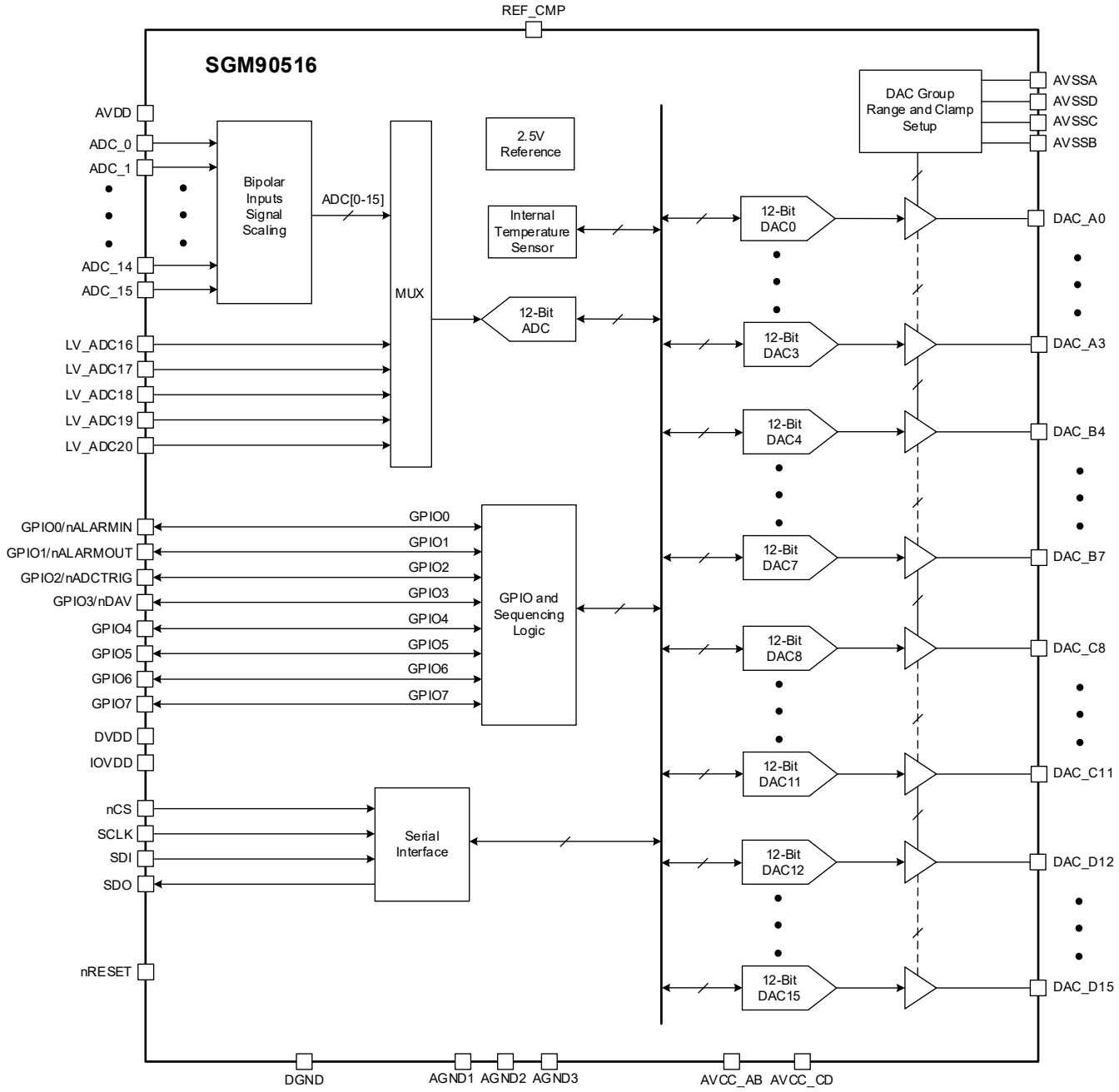


Figure 3. Functional Block Diagram

DETAILED DESCRIPTION

The SGM90516 is a high integrated analog front end which is specified for power amplifier monitoring system in communication application. The SGM90516 consists of the following components, 16-channel 12-bit DACs, 16-channel bipolar high voltage inputs and 5-channel unipolar low voltage inputs and one on-chip temperature sensor, and these analog inputs share one 12-bit ADC core through multiplexer, on-chip 2.5V reference.

The SGM90516 supports 4-wire SPI interface. The interface is powered from 1.8V to 5.25V.

Digital-to-Analog Converters (DACs)

The SGM90516 has 16-channel 12 bits DACs which are operated with on-chip internal reference. Each DAC has separate string DAC network and output buffer.

DAC Output Range and Clamp Configuration

The SGM90516 has 4 groups of DAC outputs. Each DAC group has separate output range and clamp voltage. These settings can be re-configured in registers by software. After system power on or a reset, all DAC setting registers and data registers are reset to default values. The internal auto-range detector circuits will detect the value of the power supply of the AVSS, and compare with AVSSTH threshold, then set the DAC outputs range and clamp DAC outputs to the corresponding AVSS value automatically.

Auto-Range Detection

After system power on or a reset event, the internal auto-range detector circuits will detect the value of the power supply of the AVSS, and compare with AVSSTH threshold. If V_{AVSS} is lower than V_{AVSSTH}, the DACs output range will be set between -10V and 0V. If V_{AVSS} is higher than V_{AVSSTH}, the DACs output range will be set between 0V and 5V. At the same time, the DAC outputs will be clamped to the corresponding AVSS value automatically. The output range auto detected result is stored in general status register (REG0x72).

Besides of a system power on or a reset event, the auto-range detector can also be triggered by a writing operation to the power-down 0 and power-down 1 registers (REG0xB2 and REG0xB3), or a writing operation to the device configuration register (REG0x02).

The output range of each DAC group can be re-configured by software through the DAC range 0 and DAC range 1 registers (REG0x1E and REG0x1F). The available voltage ranges are -10V to 0V, -5V to 0V, 0V to 5V, and 0V to 10V.

NOTES:
The recommended connections of AVSS are:
1. If output range is positive, connect it to AGND, and then the clamp voltage is 0V.
2. If the output range is negative, connect it to the negative power supply rail, and then the clamp voltage depends on the negative power supply rail.

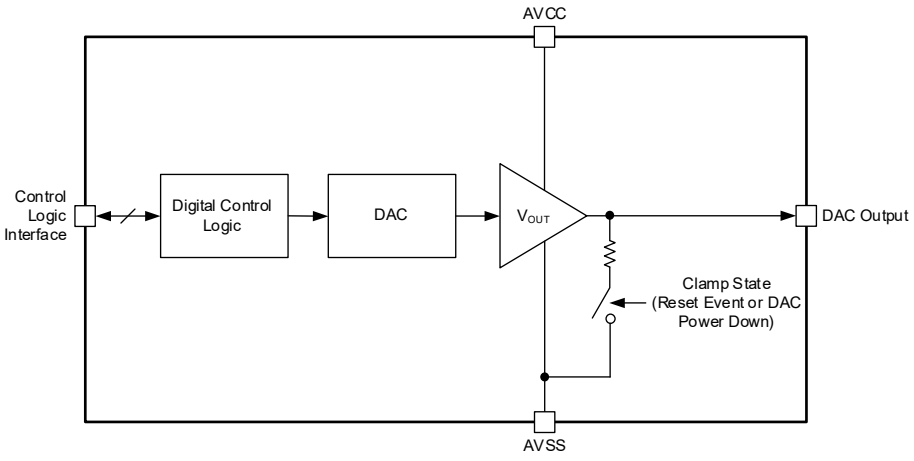


Figure 4. DAC Block Diagram

DETAILED DESCRIPTION (continued)

The DAC output range of each DAC group is restricted by the power supply rail of AVCC and AVSS.

Table 1. Recommended DAC Group Configuration

DAC Group	DAC	Auto-Range and Clamp Voltage Selection (AVSS)	AVSSA = AGND		$V_{AVSSA} = V_{NEG}$	
			Output Voltage Range	Clamp Voltage Connection	Output Voltage Range	Clamp Voltage Connection
A	DAC_A0	AVSSA	0V to 5V or 0V to 10V	AGND	-5V to 0V or -10V to 0V	V_{NEG}
	DAC_A1					
	DAC_A2					
	DAC_A3					
B	DAC_B4	AVSSB	0V to 5V or 0V to 10V	AGND	-5V to 0V or -10V to 0V	$V_{NEG} \le V_{AVSSB} \le -5V$
	DAC_B5					
	DAC_B6				0V to 5V or 0V to 10V	AGND
	DAC_B7					
C	DAC_C8	AVSSC	0V to 5V or 0V to 10V	AGND	-5V to 0V or -10V to 0V	$V_{NEG} \le V_{AVSSC} \le -5V$
	DAC_C9					
	DAC_C10				0V to 5V or 0V to 10V	AGND
	DAC_C11					
D	DAC_D12	AVSSD	0V to 5V or 0V to 10V	AGND	-5V to 0V or -10V to 0V	$V_{NEG} \le V_{AVSSD} \le -5V$
	DAC_D13					
	DAC_D14				0V to 5V or 0V to 10V	AGND
	DAC_D15					

DAC Register Structure

The DAC operation data format is straight binary. See Table 2 for details.

DAC has two sets of registers, DAC buffer registers and DAC active registers. The data from the host controller is firstly written to and stored in DAC buffer registers. And then issuing an update command to the update register (REG0x0F), the DAC active registers are updated and DAC outputs change to new voltage accordingly.

Both DAC buffer registers and DAC active registers can be read by host controllers. The readback selection is set by the READBACK bit in the configuration register (REG0x01[5]).

Table 2. DAC Data Format

Digital Code (Binary)	DAC Output Voltage (V)			
	0V to 5V Range	0V to 10V Range	-5V to 0V Range	-10V to 0V Range
0000 0000 0000	0	0	-5	-10
0000 0000 0001	0.00122	0.00244	-4.99878	-9.99756
1000 0000 0000	2.5	5	-2.5	-5
1111 1111 1110	4.99756	9.99512	-0.00244	-0.00488
1111 1111 1111	4.99878	9.99756	-0.00122	-0.00244

DETAILED DESCRIPTION (continued)

DAC Clear Operation

Each DAC can go into a clear state that can be triggered by hardware and software. Once a DAC is in clear state, it outputs a zero-code voltage that is in accordance with the configured operating range. In clear state, DAC buffer and active registers will hold the data before a clear event is informed. Moreover, reading back a DAC active register returns zero-code, while reading back a buffer register returns to the same values as before.

When the chip is in clear state, the DAC buffer register and active register can be updated by writing operation. Once the DAC exits the clear state, the DAC output is updated with setting.

The DAC clear registers (REG0xB0 and REG0xB1) are used to configure clearing operation to each DAC separately. The DACs can go into clear state by many alarm events such as a special nALARMIN-controlled clear mechanism. To enable this function, the alarm event must be set as DAC clear sources in the DAC clear source registers (REG0x1A and REG0x1B). And it must be specified which DACs are going to be cleared in the DAC clear enable registers (REG0x18 and REG0x19). See details in the programmable out-of-range alarms section.

If an alarm event happens, the corresponding bit is set in the alarm status registers, and all the corresponding DACs enter a clear state. Once the alarm bit is cleared and there are no other alarm events triggered, the DAC exits clear state and updates output by DAC active register.

Analog-to-Digital Converter (ADC)

The SGM90516 has a 12-bit SAR ADC, which can be configured with 21-channel inputs and an internal analog temperature sensor through a multiplexer. The ADC is driven by internal oscillator.

The ADC works with an internal 2.5V reference and the input range is from 0V to 2 × V_{REF}. The high voltage bipolar inputs are scaled into this range by a resistor network.

Analog Inputs

The ADC input equivalent circuit for the external analog-input pins is shown in Figure 5. All switches are open when the ADC is in the IDLE state.

To get the specified performance, an external driving amplifier is recommended before each ADC input.

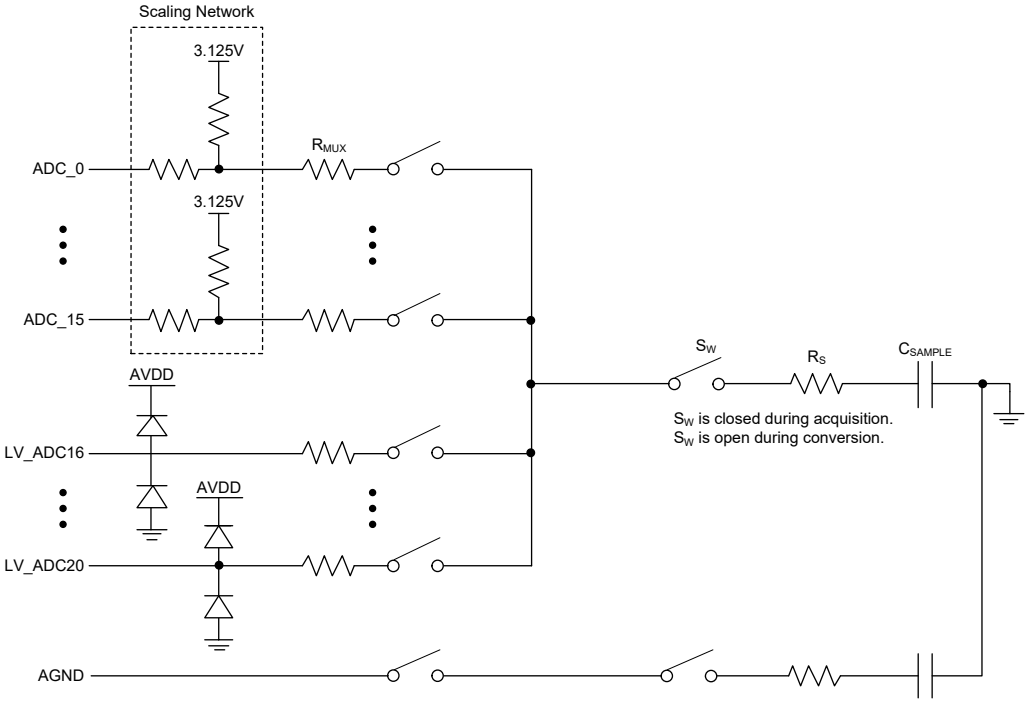


Figure 5. ADC External Input Equivalent Circuit

DETAILED DESCRIPTION (continued)

Bipolar Analog Inputs

The SGM90516 supports 16-channel high voltage bipolar inputs. The available input range is between -12.5V and 12.5V. The input voltage scales ADC input range (which is 0V to 5V) through a 120kΩ resistor network.

The input voltage is given by Equation 1.

$$\text{Voltage} = 5\left(\frac{\text{CODE}\times 5}{4096} - 2.5\right) \quad (1)$$

Unipolar Analog Inputs

The SGM90516 supports 5-channel low voltage unipolar inputs. The available input range is 0V to 5V.

Therefore, the input voltage is given by:

$$\text{Voltage} = \frac{\text{CODE}\times 5}{4096} \quad (2)$$

ADC Sequencing

The SGM90516 ADC has two conversion modes, direct mode and auto mode (ADC configuration register REG0x10). After reset, the direct mode is set by default. In both modes, the ADC channels are selected by ADC MUX configuration 0/1/2 registers (REG0x13 to REG0x15).

In direct mode, if an ADC trigger signal (software or hardware) is issued, all selected channels are converted in sequence, and then ADC goes to IDLE state. The ADC remains in IDLE state until a new trigger signal is issued.

In auto mode, the conversion cycle is triggered by an ADC trigger signal (software or hardware). All selected channels will be converted in sequence. When a cycle is completed, a new cycle will be started automatically. It will not stop until a second trigger signal occurs.

In both operating modes, the ADC associated registers which include ADC configuration register (REG0x10), false alarm configuration register (REG0x11), ADC MUX configuration 0/1/2 register (REG0x13 to REG0x15), threshold registers (REG0x80 to REG0x97), and hysteresis registers (REG0xA0 to REG0xA5) must be updated in ADC IDLE state. After any register is updated, the host controller must wait at least 2μs before sending a new ADC trigger signal.

ADC Synchronization

The ADC trigger signal can be set by software (ICONV bit in the ADC trigger register, REG0xC0[0]) or hardware (GPIO2/nADCTRIG pin). To use nADCTRIG, it is necessary to configure in GPIO configuration register accordingly (REG0x12). Once the pin is configured, a trigger signal is active on the falling edge of GPIO2/nADCTRIG pin.

In auto mode, to update the ADC data registers, there is no need for synchronization between the SGM90516 and the host controller. Only issuing an ADC_UPDATE command (in the register update register, REG0x0F), all ADC data registers are updated with the latest available data. The ADC_UPDATE bit will reset automatically. To read all ADC data out, the register reading sequence needs to be followed.

In direct mode, the ADC data registers and temperature data register should be read out when the ADC is in IDLE state. The ADC provides an indicator signal to report ADC status. The indicator signal can be set by hardware (GPIO3/nDAV pin which must be configured in GPIO configuration register, REG0x12) or software (DAVF bit in the general status register, REG0x72[0]). Failure to meet the synchronization requirements may result in data read faults.

DETAILED DESCRIPTION (continued)

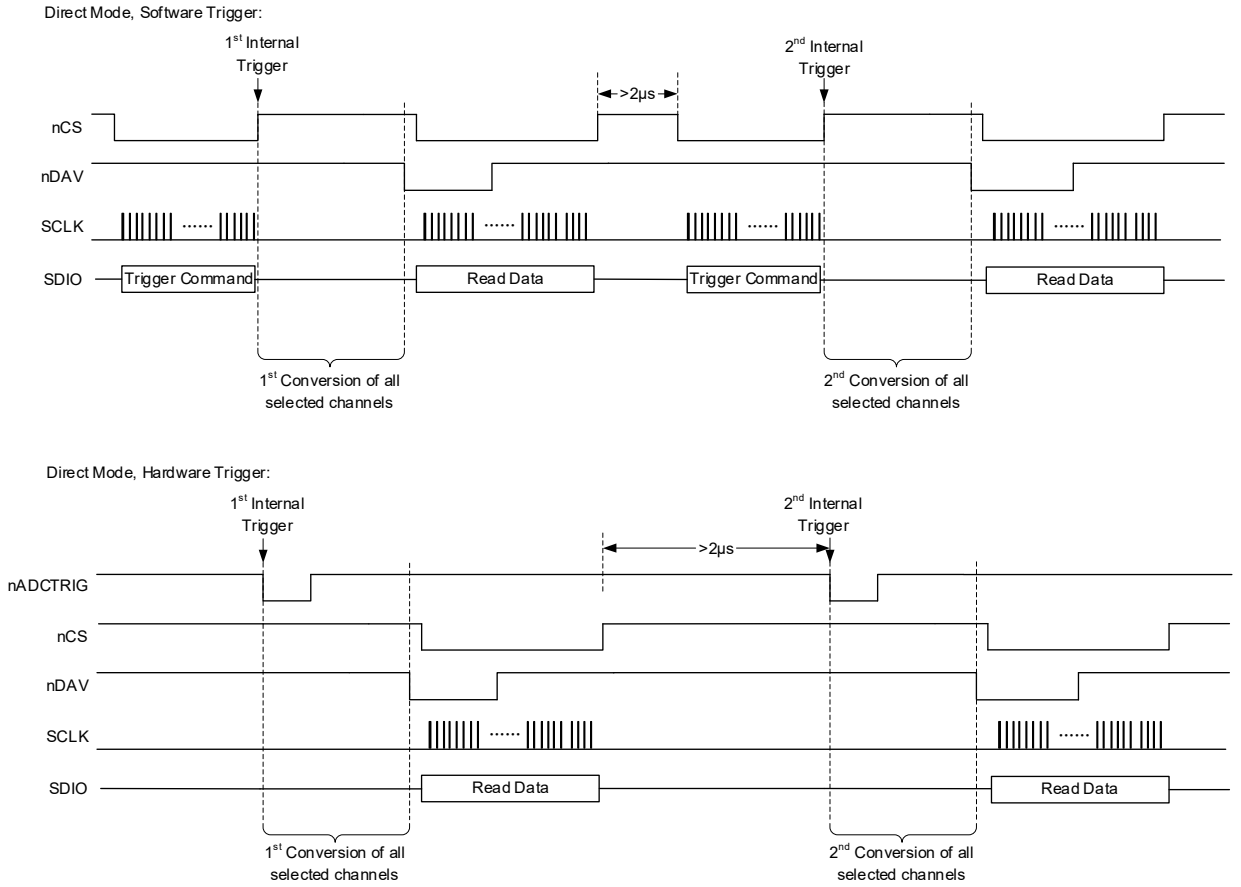


Figure 6. ADC Direct-Mode Trigger Synchronization

Programmable Out-of-Range Alarms

The SGM90516 can continuously monitor kinds of inputs and give out alarms. The alarm sources include the ADC high and low limit, the temperature high and low limit, reference voltage and an external input signal (nALARMIN alarm).

If any limit is exceeded (configured in corresponding threshold registers, REG0x80 to REG0x97), the corresponding bit is set in the alarm status 0/1 registers (REG0x70 and REG0x71). Simultaneously the GALR bit in the general status register (REG0x72[1]) is set. A simple schematic is shown in Figure 7.

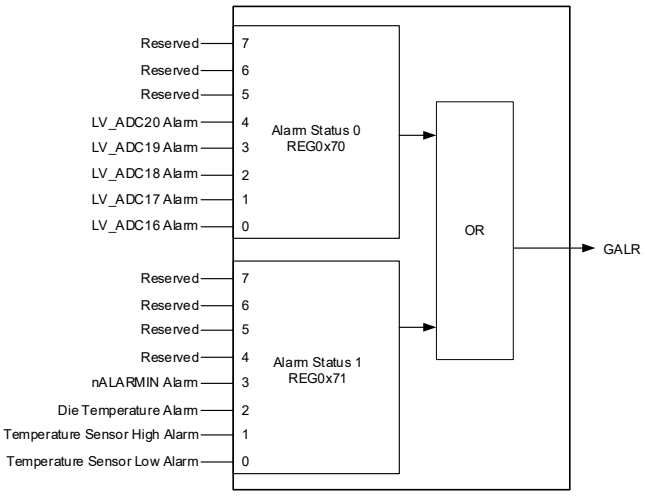


Figure 7. Alarm Status Register

DETAILED DESCRIPTION (continued)

Except that the nALARMIN alarm is always unlatched, all the others can be latched or dis-latched by setting the ALARM_LATCH_DIS bit in ALARMOUT source 1 register (REG0x1D[4]). Once the ALARM_LATCH_DIS bit is enabled, the alarm bits in the alarm status registers can be cleared by software (reading the alarm status registers). If the exceeding alarm limit condition is still fulfilled, the alarm bit will be set again.

When the ALARM_LATCH_DIS is not enabled, the alarm bits are not latched. Once the exceeding alarm limit condition is unfulfilled, the alarm bits will be cleared automatically.

All the alarm sources can be used to drive the nALARMOUT pin. The nALARMOUT pin function is configured in the GPIO configuration register (REG0x12). Any alarm event used to activate the nALARMOUT pin must be enabled in the ALARMOUT source registers (REG0x1C and REG0x1D). Even if an alarm source is not enabled in the ALARMOUT source registers and an out-of-limit occurs, the status register corresponding bit is still set.

Out-of-Range Alarms of Unipolar Inputs

The SGM90516 has 5 unipolar ADC inputs. Each ADC input has an out-of-range detection function. If an out-of-range event occurs, the corresponding alarm bit in the alarm status 0 register (REG0x70) is set to '1'. The ADC upper threshold registers and the ADC lower threshold registers (REG0x80 to REG0x93) define the upper and lower limitation of the ADC inputs.

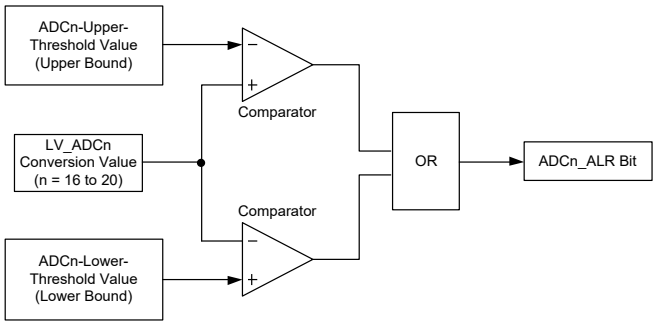


Figure 8. Unipolar Input Out-of-Range Alarms

Out-of-Range Alarms of Local Temperature Sensor

The SGM90516 has an internal temperature sensor out-of-range detection block. The LT upper threshold register and the LT lower threshold register (REG0x94 to REG0x97) set the upper limitation and the lower limitation separately. If the temperature exceeds the limitations, a high temperature alarm (LT_HIGH_ALR bit) or a low temperature alarm (LT_LOW_ALR bit) in the alarm status 1 register (REG0x71) is set accordingly.

Besides the programmable threshold temperature alarm function, the temperature sensor detection block also features a die thermal-alarm function. If the die temperature exceeds +150℃, the die thermal alarm flag (THERM_ALR bit) is set to '1'.

To enable the internal temperature sensor monitoring function, the TEMP_CH bit must be set in ADC MUX Configuration 2 Register (REG0x15).

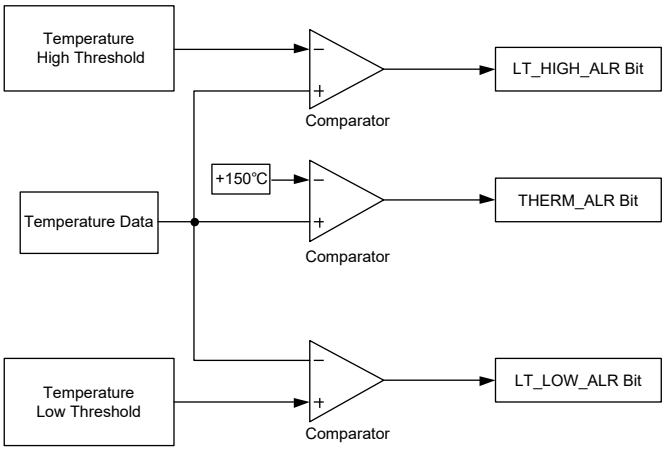


Figure 9. Internal Temperature Out-of-Range Alarms

nALARMIN Alarm

The SGM90516 supports external alarm signal input, which needs to configure nALARMIN pin in GPIO configuration register (REG0x12). Once it is configured as nALARMIN input, this pin input is active low.

DETAILED DESCRIPTION (continued)

Hysteresis

The ADC out-of-range detection block and internal temperature sensor out-of-range detection block can be functioned with a hysteresis window feature. The ADC and temperature hysteresis windows are set by the ADCn hysteresis registers (REG0xA0 to REG0xA4) and LT hysteresis register (REG0xA5).

The LT hysteresis is programmed between 0 LSB and 32 LSB for the unipolar inputs alarms. The available range for the internal temperature-sensor alarms hysteresis is 0℃ to 8℃ with 0.25℃ resolution. The die thermal alarm hysteresis is fixed at 8℃.

False-Alarm Protection

Ensure that a false is triggered by a true alarm event, not by a random wrong action. A false alarm factor N can be used to monitor the times of consecutive conversions of input signals which are out of normal range. If the out-of-range time is equal to or greater than N, then an alarm event is issued. The false alarm factor N is available for the unipolar inputs and local temperature sensor. It can be configured in the false alarm configuration register (REG0x11).

Internal Temperature Sensor

The SGM90516 has an internal on-chip temperature sensor which is used to monitor the chip die temperature. The available detecting range is -40℃ to +125℃.

The temperature sensor output can be sampled by ADC in a lower sampling speed than the other analog input channels. ADC can be in auto mode or direct mode. The temperature sensor input is configured in ADC MUX configuration 2 register (REG0x15).

The temperature sensor features 0.25℃ resolution in the operating temperature range. The temperature date is 12-bit two's complement format.

Table 3. Temperature Sensor Data Format

Temperature (℃)	Digital Code
-40	1111 0110 0000
-25	1111 1001 1100
-10	1111 1101 1000
-0.25	1111 1111 1111
0	0000 0000 0000
0.25	0000 0000 0001
10	0000 0010 1000
25	0000 0110 0100
50	0000 1100 1000
75	0001 0010 1100
100	0001 1001 0000
105	0001 1010 0100
125	0001 1111 0100

According to whether the temperature data is positive or negative, use Equation 3 or Equation 4 to calculate the temperature.

$$\text{Positive Temperature (℃)} = \frac{\text{ADC\_CODE}}{4} \quad (3)$$

$$\text{Negative Temperature (℃)} = \frac{4096 - \text{ADC\_CODE}}{4} \quad (4)$$

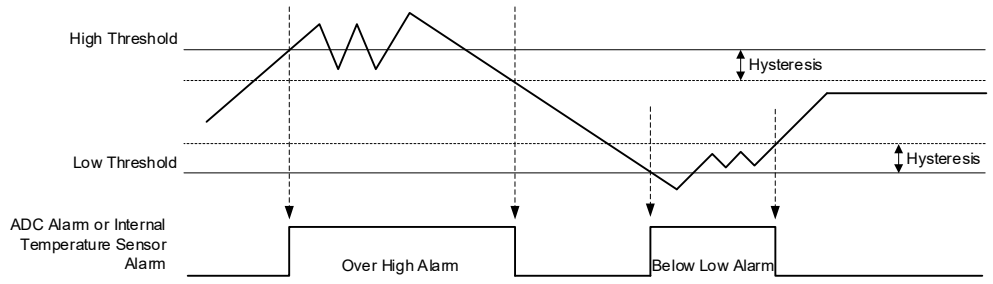


Figure 10. Device Hysteresis

DETAILED DESCRIPTION (continued)

Internal Reference

The SGM90516 has an on-chip 2.5V reference which can be used for ADC and DACs. A 4.7μF decoupling capacitor is needed between the REF_CMP and the AGND2 pins.

The internal output buffer for the reference is OFF by default. It can be enabled in ADC configuration register (REG0x10). This buffer is not intended to drive any external circuitry.

The internal reference typically takes about 5ms to fully settle at 25℃. This set-up time varies across temperature. Thus, temperature conditions shall be considered during system level design.

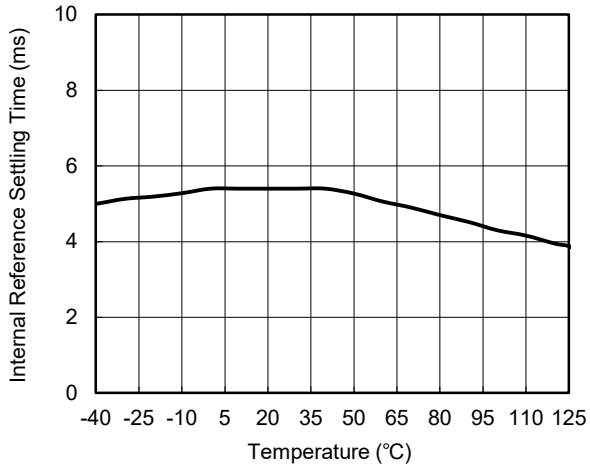


Figure 11. Internal Reference Settling Time vs. Temperature

General Purpose I/Os

The SGM90516 has eight GPIO pins. Each pin has an internal 60kΩ pull-up resistor to the IOVDD. The GPIO[0:3] pins are multi-function pins, which can be set as GPIO pins or interrupt signals (configuration register is REG0x12). The GPIO[4:7] pins are dedicated GPIOs.

If any of the GPIOs is used as an output, the setting of the corresponding GPIO bit in the GPIO register (REG0x7A) determines the output logic state. If the GPIO is set as an input, the corresponding bit in the GPIO register must be set to '1', and the input value is acquired by reading the corresponding bit in the GPIO register.

After a power on or any reset event, all GPIO bits are reset to '1', and the GPIOs each are connected to IOVDD by a 60kΩ pull-up resistor by default. If unused, GPIO pins can be left open.

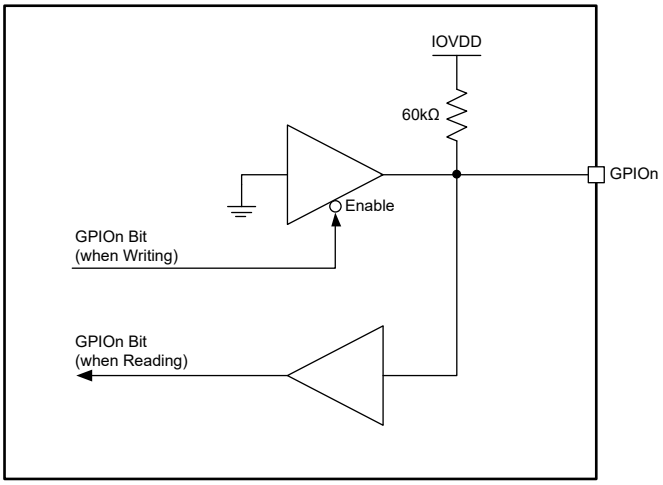


Figure 12. SGM90516 GPIO Pin

Table 4. Dual Functionality GPIO Pins

Pin	Default Pin Name	Alternative Pin Name	Alternative Functionality
7	GPIO0	nALARMIN	DAC Clear Control Signal
8	GPIO1	nALARMOUT	Global Alarm Output
9	GPIO2	nADCTRIG	External ADC Conversion Trigger
10	GPIO3	nDAV	ADC Data Available Indicator

DETAILED DESCRIPTION (continued)

Device Functional Modes

The DACs of SGM90516 are divided into four groups. Each group has separate output range and clamp voltage. These DAC groups can work in the following three modes:

- All-positive DAC range mode
- All-negative DAC range mode
- Mixed DAC range mode

All-Positive DAC Range Mode

In all positive modes, all four DAC groups are set to positive 0V to 5V range or 0V to 10V range. The outputs of all DACs are limited below AVCC voltage (AVCC = AVCC_AB = AVCC_CD). In this mode, if one of four DAC groups operates with 0V to 10V voltage range, the AVCC must be powered with 10V. Only all four DAC groups are set to 0V to 5V range, AVCC voltage can be set to 5V.

The output voltages of all DAC groups must be higher than the reference voltage of AVSS pins (AVSSA, AVSSB, AVSSC, and AVSSD). In this mode, all reference pins are tied together and connected to AGND.

After power on or a reset event, the internal auto-range detector circuits will detect the value of the power supply of the AVSS, and compare with AVSSTH threshold, then set the DAC outputs range and clamp DAC outputs to the corresponding AVSS value automatically. In all-positive DAC range mode, all DAC groups will be reset to default 0V to 5V range. Each DAC group output range can be re-configured by software in DAC range registers (REG0x1E and REG0x1F).

As in all-positive DAC range mode, the AVSS pins are tied to 0V, and the clamp voltage is 0V. Changing the DAC output range does not change the clamp voltage.

Table 5. Typical Configuration in All-Positive DAC Range Mode

Pin	Notes	Typical Connection
AVDD		5V
DVDD	The power supply voltage of DVDD must be equal to that of AVDD.	5V
IOVDD	The supply voltage potential of the IOVDD pin must not be higher than that of the DVDD pin.	1.8V to 5V
AVCC_AB, AVCC_CD	AVCC_AB and AVCC_CD must have the same voltage potential (AVCC). AVCC determines the maximum output rail of all the 16 DACs.	V_{AVCC} ≥ 5V, V_{AVCC} ≥ 10V
AVSSA		AGND
AVSSB, AVSSC, AVSSD		AGND
Exposed Pad		AGND

All-Negative DAC Range Mode

In all negative modes, all four DAC groups are set to negative -5V to 0V range or -10V to 0V range. The minimum DAC output voltage of each group must be higher than the voltage of the corresponding AVSS (AVSSA, AVSSB, AVSSC and AVSSD). It is not necessary for all AVSS pins to share same voltage potential. Each AVSS pin can be set to its desired operating range.

In all negative modes, all DAC outputs voltage is lower than 0V. The AVCC voltage (AVCC, AVCC_AB, AVCC_CD) still must be compatible with the device operating voltage range of 4.7V to 5V. A suggested operating condition can be that AVCC, AVDD and DVDD share a common supply potential.

After power on or a reset event, the internal auto-range detector circuits will detect the value of the power supply of the AVSS, and compare with AVSSTH threshold, then set the DAC outputs range and clamp DAC outputs to the corresponding AVSS value automatically. In all-negative range mode, all voltages of AVSS pins must be lower than V_{AVSSTH}. In this condition, all four DAC groups are reset to -10V to 0V range in default. Each DAC group output range can be re-configured by software in DAC range registers (REG0x1E and REG0x1F).

DETAILED DESCRIPTION (continued)

Table 6. Typical Configuration of All-Negative DAC Range Mode

Pin	Notes	Typical Connection
AVDD		5V
DVDD	The power supply voltage of DVDD must be equal to that of AVDD.	5V
IOVDD	The supply voltage potential of the IOVDD pin must not be higher than that of the DVDD pin.	1.8V to 5V
AVCC_AB, AVCC_CD	AVCC_AB and AVCC_CD must have the same voltage potential (AVCC). AVCC determines the maximum output rail of all the 16 DACs.	5V
AVSSA	AVSSA potential must be lowest in the device. AVSSA is the negative power supply rail of DAC group A.	$V_{AVSSA} \leq -5V$ $V_{AVSSA} \leq -10V$
AVSSB, AVSSC, AVSSD	AVSSn is the according negative power supply rail of DAC group n (n = B, C, D).	$V_{AVSSA} \leq V_{AVSSn} \leq -5V$ $V_{AVSSA} \leq V_{AVSSn} \leq -10V$
Exposed Pad		AVSSA or Floating

Mixed DAC Range Mode

In the mixed range mode, each DAC group output range can be a positive range (0V to 5V or 0V to 10V) or a negative range (-5V to 0V or -10V to 0V).

All DACs output is limited below AVCC voltage (AVCC = AVCC_AB = AVCC_CD). If one DAC group is in the 0V to 10V range, the others DAC groups supply voltage must be greater than or equal to 10V. If all DAC groups work in 0V to 5V range, the AVCC voltage can be 5V.

The minimum DAC output voltage of each group must be higher than the voltage of the corresponding AVSS (AVSSA, AVSSB, AVSSC and AVSSD). The AVSS pin of each is not necessary to be connected to the same voltage potential. It can be tied to the desired DAC operating negative supply rail.

After power on or a reset event, the internal auto-range detector circuits will detect the value of the power supply of the AVSS, and compare with AVSSTH threshold, then set the DAC outputs range and clamp DAC outputs to the corresponding AVSS value automatically. If V_{AVSS} is lower than V_{AVSSTH}, the DACs output will be set to -10V to 0V range. If V_{AVSS} is higher than V_{AVSSTH}, the DACs output will be set to 0V to 5V range. Simultaneously the DAC outputs will be clamped to the corresponding AVSS value automatically.

The output range can be reset by software after initialization.

Table 7. Typical Configuration of Mixed DAC Range Mode

Pin	Notes	Typical Connection	
AVDD		5V	
DVDD	The power supply voltage of DVDD must be equal to that of AVDD.	5V	
IOVDD	The supply voltage potential of the IOVDD pin must not be higher than that of the DVDD pin.	1.8V to 5V	
AVCC_AB, AVCC_CD	AVCC_AB and AVCC_CD must have the same voltage potential (AVCC). AVCC determines the maximum output rail of all the 16 DACs.	$V_{AVCC} \geq 5V$ $V_{AVCC} \geq 10V$	
AVSSA	AVSSA potential must be lowest in the device. AVSSA is the negative power supply rail of DAC group A.	$V_{AVSSA} \leq -5V$ $V_{AVSSA} \leq -10V$	
AVSSB, AVSSC, AVSSD	AVSSn is the according negative power supply rail of DAC group n (n = B, C, D).	Negative Range	$V_{AVSSA} \leq V_{AVSSn} \leq -5V$ $V_{AVSSA} \leq V_{AVSSn} \leq -10V$
		Positive Range	AGND
Exposed Pad		AVSSA or Floating	

DETAILED DESCRIPTION (continued)

Programming

The SGM90516 interface is a 4-wire SPI compatible interface.

The operation frame is restricted in N+2 bytes, where N represents the number of data bytes to be accessed. In MSB-first mode, the first bit of the frame is W/R (write/read) acknowledge bit. When it is '0', it sets a write operation. When it is '1', it sets a read operation. The next 15 bits are the register address, which means 32768 addressable registers. The remaining bits are data. In a write operation, the data is shifted in on the rising edge of SCLK. In a read operation, the data is shifted out on the falling edge of SCLK. Note that, in writing operation, if the clocks are not an even multiple of 8 clocks, the writing is invalid.

The access protocol used by the interface is illustrated in Figure 13 and Figure 14.

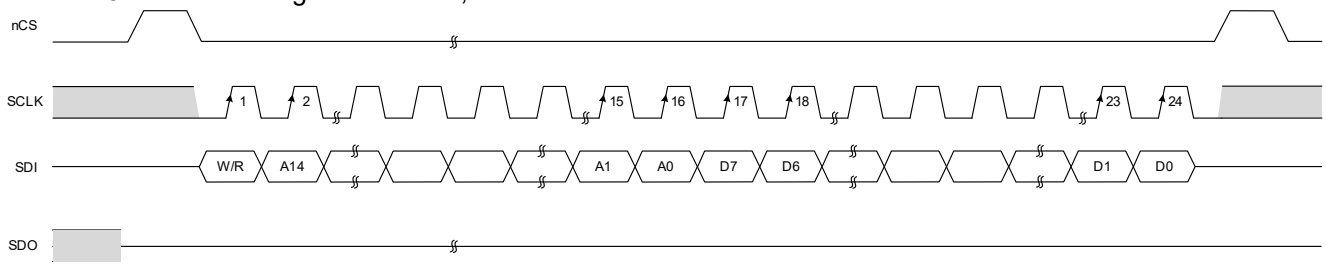


Figure 13. Serial Interface Write Bus Cycle

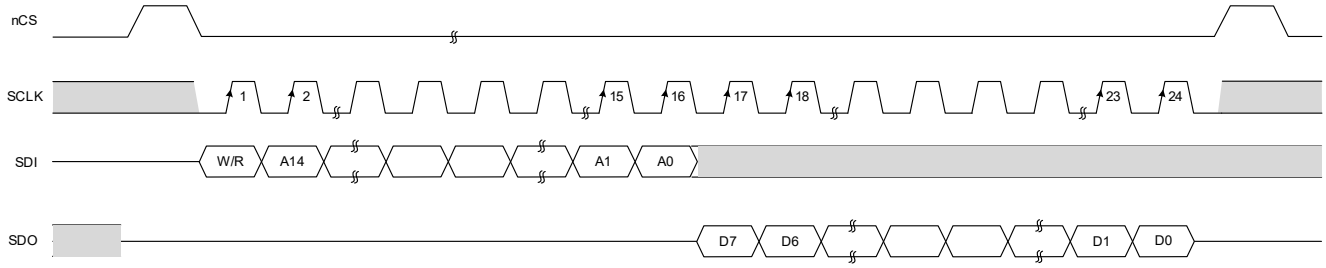


Figure 14. Serial Interface Read Bus Cycle

Streaming Mode Operation

In stream mode, multiple bytes of data can be written or read in one frame operation. In this mode, a single byte or multiple bytes are accessed, which is configured in interface configuration 1 register (REG0x01). And the data to be accessed in increased address sequence or decreased address sequence is configured by ADDR_ASCEND bit in interface configuration 0 register (REG0x00[5]).

In stream mode, when the address is increased, if the address 0x7FFF is reached, the next address will loop back to 0x0000. When the address is decreased, if the address is 0x0000 is reached, the next address will loop back to 0x7FFF. Note that when in continuous operations, as 0x0001 is the configuration register address, writing to this register may change the configuration of the serial interface.

The access protocol used in streaming mode is illustrated in Figure 15 and Figure 16.

DETAILED DESCRIPTION (continued)

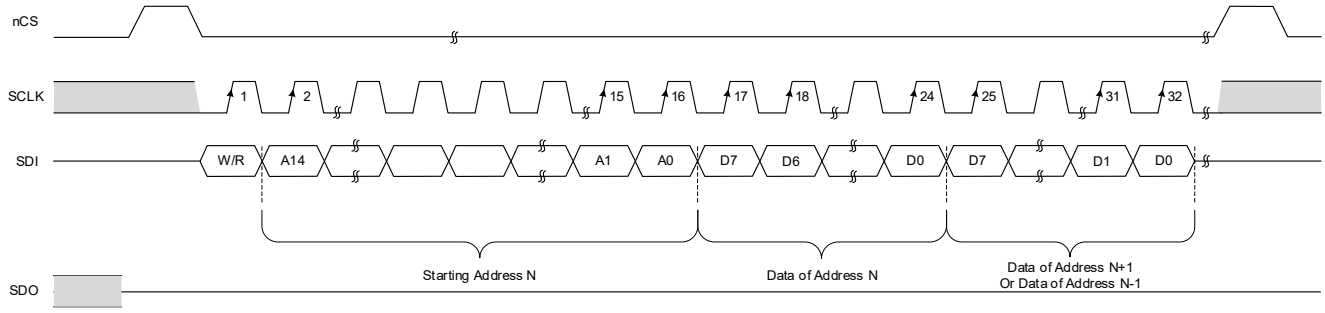


Figure 15. Serial Interface Streaming Write Example

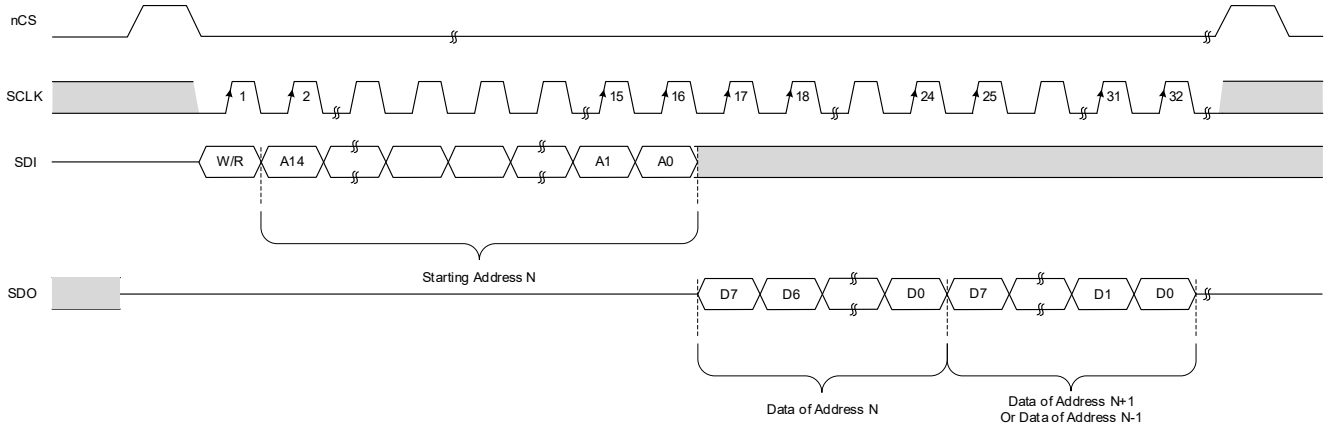


Figure 16. Serial Interface Streaming Read Example

REGISTER MAPS

All registers are 8-bit and individual bits are named from D[0] (LSB) to D[7] (MSB).

Bit Types:
R: Read only
R/W: Read/Write

Table 8. Register Map

ADDRESS	REGISTER NAME	TYPE	DEFAULT
0x00	Interface Configuration 0	R/W	0x30
0x01	Interface Configuration 1	R/W	0x00
0x02	Device Configuration	R/W	0x03
0x03	Device Type	R	0x08
0x04	Device ID (Low Byte)	R	0x36
0x05	Device ID (High Byte)	R	0x0C
0x06	Version ID	R	0x00
0x07 - 0x0B	Reserved	—	—
0x0C	Vendor ID (Low Byte)	R	0x51
0x0D	Vendor ID (High Byte)	R	0x04
0x0E	Reserved	—	—
0x0F	Register Update	R/W	0x00
0x10	ADC Configuration	R/W	0x00
0x11	False Alarm Configuration	R/W	0x70
0x12	GPIO Configuration	R/W	0x00
0x13	ADC MUX Configuration 0	R/W	0x00
0x14	ADC MUX Configuration 1	R/W	0x00
0x15	ADC MUX Configuration 2	R/W	0x00
0x16	Reserved	—	—
0x17	Reserved	—	—
0x18	DAC Clear Enable 0	R/W	0x00
0x19	DAC Clear Enable 1	R/W	0x00
0x1A	DAC Clear Source 0	R/W	0x00
0x1B	DAC Clear Source 1	R/W	0x00
0x1C	ALARMOUT Source 0	R/W	0x00
0x1D	ALARMOUT Source 1	R/W	0x00
0x1E	DAC Range 0	R/W	0xXX
0x1F	DAC Range 1	R/W	0xXX
0x20	ADC0_Data (Low Byte)	R	0x00
0x21	ADC0_Data (High Byte)	R	0x00
0x22	ADC1_Data (Low Byte)	R	0x00
0x23	ADC1_Data (High Byte)	R	0x00
0x24	ADC2_Data (Low Byte)	R	0x00
0x25	ADC2_Data (High Byte)	R	0x00
0x26	ADC3_Data (Low Byte)	R	0x00
0x27	ADC3_Data (High Byte)	R	0x00

REGISTER MAPS (continued)

ADDRESS	REGISTER NAME	TYPE	DEFAULT
0x28	ADC4_Data (Low Byte)	R	0x00
0x29	ADC4_Data (High Byte)	R	0x00
0x2A	ADC5_Data (Low Byte)	R	0x00
0x2B	ADC5_Data (High Byte)	R	0x00
0x2C	ADC6_Data (Low Byte)	R	0x00
0x2D	ADC6_Data (High Byte)	R	0x00
0x2E	ADC7_Data (Low Byte)	R	0x00
0x2F	ADC7_Data (High Byte)	R	0x00
0x30	ADC8_Data (Low Byte)	R	0x00
0x31	ADC8_Data (High Byte)	R	0x00
0x32	ADC9_Data (Low Byte)	R	0x00
0x33	ADC9-Data (High Byte)	R	0x00
0x34	ADC10_Data (Low Byte)	R	0x00
0x35	ADC10_Data (High Byte)	R	0x00
0x36	ADC11_Data (Low Byte)	R	0x00
0x37	ADC11_Data (High Byte)	R	0x00
0x38	ADC12_Data (Low Byte)	R	0x00
0x39	ADC12_Data (High Byte)	R	0x00
0x3A	ADC13_Data (Low Byte)	R	0x00
0x3B	ADC13_Data (High Byte)	R	0x00
0x3C	ADC14_Data (Low Byte)	R	0x00
0x3D	ADC14_Data (High Byte)	R	0x00
0x3E	ADC15_Data (Low Byte)	R	0x00
0x3F	ADC15_Data (High Byte)	R	0x00
0x40	ADC16_Data (Low Byte)	R	0x00
0x41	ADC16_Data (High Byte)	R	0x00
0x42	ADC17_Data (Low Byte)	R	0x00
0x43	ADC17_Data (High Byte)	R	0x00
0x44	ADC18_Data (Low Byte)	R	0x00
0x45	ADC18_Data (High Byte)	R	0x00
0x46	ADC19_Data (Low Byte)	R	0x00
0x47	ADC19_Data (High Byte)	R	0x00
0x48	ADC20_Data (Low Byte)	R	0x00
0x49	ADC20_Data (High Byte)	R	0x00
0x4A	Temperature Data (Low Byte)	R	0x00
0x4B	Temperature Data (High Byte)	R	0x00
0x4C - 0x4F	Reserved	—	—
0x50	DACA0_Data (Low Byte)	R/W	0x00
0x51	DACA0_Data (High Byte)	R/W	0x00
0x52	DACA1_Data (Low Byte)	R/W	0x00
0x53	DACA1_Data (High Byte)	R/W	0x00

REGISTER MAPS (continued)

ADDRESS	REGISTER NAME	TYPE	DEFAULT
0x54	DACA2_Data (Low Byte)	R/W	0x00
0x55	DACA2_Data (High Byte)	R/W	0x00
0x56	DACA3_Data (Low Byte)	R/W	0x00
0x57	DACA3_Data (High Byte)	R/W	0x00
0x58	DACB4_Data (Low Byte)	R/W	0x00
0x59	DACB4_Data (High Byte)	R/W	0x00
0x5A	DACB5_Data (Low Byte)	R/W	0x00
0x5B	DACB5_Data (High Byte)	R/W	0x00
0x5C	DACB6_Data (Low Byte)	R/W	0x00
0x5D	DACB6_Data (High Byte)	R/W	0x00
0x5E	DACB7_Data (Low Byte)	R/W	0x00
0x5F	DACB7_Data (High Byte)	R/W	0x00
0x60	DACC8_Data (Low Byte)	R/W	0x00
0x61	DACC8_Data (High Byte)	R/W	0x00
0x62	DACC9_Data (Low Byte)	R/W	0x00
0x63	DACC9_Data (High Byte)	R/W	0x00
0x64	DACC10_Data (Low Byte)	R/W	0x00
0x65	DACC10_Data (High Byte)	R/W	0x00
0x66	DACC11_Data (Low Byte)	R/W	0x00
0x67	DACC11_Data (High Byte)	R/W	0x00
0x68	DACD12_Data (Low Byte)	R/W	0x00
0x69	DACD12_Data (High Byte)	R/W	0x00
0x6A	DACD13_Data (Low Byte)	R/W	0x00
0x6B	DACD13_Data (High Byte)	R/W	0x00
0x6C	DACD14_Data (Low Byte)	R/W	0x00
0x6D	DACD14_Data (High Byte)	R/W	0x00
0x6E	DACD15_Data (Low Byte)	R/W	0x00
0x6F	DACD15_Data (High Byte)	R/W	0x00
0x70	Alarm Status 0	R	0x00
0x71	Alarm Status 1	R	0x00
0x72	General Status	R	0x0C
0x73 - 0x79	Reserved	—	—
0x7A	GPIO	R/W	0xFF
0x7B - 0x7F	Reserved	—	—
0x80	ADC16 Upper Threshold (Low Byte)	R/W	0xFF
0x81	ADC16 Upper Threshold (High Byte)	R/W	0x0F
0x82	ADC16 Lower Threshold (Low Byte)	R/W	0x00
0x83	ADC16 Lower Threshold (High Byte)	R/W	0x00
0x84	ADC17 Upper Threshold (Low Byte)	R/W	0xFF
0x85	ADC17 Upper Threshold (High Byte)	R/W	0x0F
0x86	ADC17 Lower Threshold (Low Byte)	R/W	0x00

REGISTER MAPS (continued)

ADDRESS	REGISTER NAME	TYPE	DEFAULT
0x87	ADC17 Lower Threshold (High Byte)	R/W	0x00
0x88	ADC18 Upper Threshold (Low Byte)	R/W	0xFF
0x89	ADC18 Upper Threshold (High Byte)	R/W	0x0F
0x8A	ADC18 Lower Threshold (Low Byte)	R/W	0x00
0x8B	ADC18 Lower Threshold (High Byte)	R/W	0x00
0x8C	ADC19 Upper Threshold (Low Byte)	R/W	0xFF
0x8D	ADC19 Upper Threshold (High Byte)	R/W	0x0F
0x8E	ADC19 Lower Threshold (Low Byte)	R/W	0x00
0x8F	ADC19 Lower Threshold (High Byte)	R/W	0x00
0x90	ADC20 Upper Threshold (Low Byte)	R/W	0xFF
0x91	ADC20 Upper Threshold (High Byte)	R/W	0x0F
0x92	ADC20 Lower Threshold (Low Byte)	R/W	0x00
0x93	ADC20 Lower Threshold (High Byte)	R/W	0x00
0x94	LT Upper Threshold (Low Byte)	R/W	0xFF
0x95	LT Upper Threshold (High Byte)	R/W	0x07
0x96	LT Lower Threshold (Low Byte)	R/W	0x00
0x97	LT Lower Threshold (High Byte)	R/W	0x08
0x98 - 0x9F	Reserved	—	—
0xA0	ADC16 Hysteresis	R/W	0x08
0xA1	ADC17 Hysteresis	R/W	0x08
0xA2	ADC18 Hysteresis	R/W	0x08
0xA3	ADC19 Hysteresis	R/W	0x08
0xA4	ADC20 Hysteresis	R/W	0x08
0xA5	LT Hysteresis	R/W	0x08
0xA6 - 0xAF	Reserved	—	—
0xB0	DAC Clear 0	R/W	0x00
0xB1	DAC Clear 1	R/W	0x00
0xB2	Power-Down 0	R/W	0x00
0xB3	Power-Down 1	R/W	0x00
0xB4	Power-Down 2	R/W	0x00
0xB5 - 0xBF	Reserved	—	—
0xC0	ADC Trigger	R/W	0x00

REGISTER MAPS (continued)

REG0x00: Interface Configuration 0 Register [reset = 0x30]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	SOFT_RESET	0	R/W	Soft Reset (Self-Clearing) 0 = No action 1 = Reset - Resets all registers except for REG0x00, REG0x01
D[6]	Reserved	0	R/W	Reserved
D[5]	ADDR_ASCEND	1	R/W	Address Ascend 0 = Descend - Address is decreased while streaming operation. (Address wrap from 0x0000 to 0x7FFF) 1 = Ascend - Address is increased while streaming operation. (Address wrap from 0x7FFF to 0x0000)
D[4]	Reserved	1	R/W	Reserved
D[3:0]	Reserved	0000	R/W	Reserved

REG0x01: Interface Configuration 1 Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	SINGLE_INSTR	0	R/W	Single Instruction Enable 0 = Streaming mode (default) 1 = Single instruction
D[6]	Reserved	0	R/W	Reserved
D[5]	READBACK	0	R/W	Read Back 0 = DAC read back from active registers (default) 1 = DAC read back from buffer registers
D[4:0]	Reserved	00000	R/W	Reserved

REG0x02: Device Configuration Register [reset = 0x03]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:2]	Reserved	000000	R/W	Reserved
D[1:0]	POWER_MODE[1:0]	11	R/W	Mode: 00 = Normal operation - full power and full performance 11 = Power Down - lowest power, only SPI active. One time overwrite of the power-down registers (REG0xB2 and REG0xB3)

REG0x03: Device Type Register [reset = 0x08]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:4]	Reserved	0000	R	Reserved
D[3:0]	DEVICE_TYPE[3:0]	1000	R	It identifies the device.

REG0x04: Device ID (Low Byte) Register [reset = 0x36]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:0]	DEVICE_ID[7:0]	00110110	R	Device ID. Low Byte

REG0x05: Device ID (High Byte) Register [reset = 0x0C]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:0]	DEVICE_ID[15:8]	00001100	R	Device ID. High Byte

REG0x06: Version ID Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:0]	VERSION_ID[7:0]	00000000	R	SGM90516 Version ID. Subject to change

REGISTER MAPS (continued)

REG0x0C: Vendor ID (Low Byte) Register [reset = 0x51]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:0]	VENDOR_ID[7:0]	01010001	R	Vendor ID. Low Byte

REG0x0D: Vendor ID (High Byte) Register [reset = 0x04]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:0]	VENDOR_ID[15:8]	00000100	R	Vendor ID. High Byte

REG0x0F: Register Update Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:5]	Reserved	000	R/W	Reserved
D[4]	ADC_UPDATE	0	R/W	When it is enabled by setting it to '1', the chip updates the latest ADC and temperature conversion data to the ADC and temperature data registers. This function is used when running ADC in auto mode.
D[3:1]	Reserved	000	R/W	Reserved
D[0]	DAC_UPDATE	0	R/W	DAC Update (Self-Clearing) 0 = Disabled 1 = Enabled - DAC data is transferred from DAC buffer registers to DAC active registers by the chip. (DAC registers only)

REG0x10: ADC Configuration Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	CMODE	0	R/W	ADC Conversion Mode Bit. This bit is used for selecting the ADC conversion mode. 0 = Direct mode. If there is a trigger signal, all selected channels are converted in sequence, and then ADC goes to IDLE state. The ADC waits in IDLE state until a new trigger signal is issued. 1 = Auto mode. If there is a trigger signal, all selected channels will be converted in sequence. When a cycle is completed, a new cycle will be started automatically. It will not stop until a second trigger signal occurs. In this mode, ADC_UPDATE bit (REG0x0F[4]) must be set to update the latest conversion result to the ADC Data Registers.
D[6:5]	CONV_RATE[1:0]	00	R/W	ADC Conversion Rate. See Table 9 for configuration details.
D[4]	ADC_REF_BUFF (1)	0	R/W	ADC Reference Buffer Bit. After the device is powered up, it must be set to '1' to enable the internal reference buffer. 0 = disabled 1 = enabled
D[3:1]	Reserved	000	R/W	Reserved
D[0]	TMPSR_CHOP	0	R/W	Temp Sensor Buffer Offset Polarity. Averaging temp sensor output for higher accuracy is possible by toggling this bit. 0 = positive buffer offset 1 = negative buffer offset

NOTE:

1. Be noted that it will take about 5ms for the REF_CMP voltage fully settling after the ADC_REF_BUFF bit (which is D[4] in ADC configuration register) is enabled from a previous disabled status and at same time at least one ADC channel is selected in ADC MUX configuration registers (which is set by registers 0x13 to 0x15). Before the REF_CMP voltage fully settles, any ADC conversion result is untrusted, and any ADC conversion operation is not recommended. The REF_CMP voltage settling time depends on the decoupling capacitor. The REF_CMP voltage settling time is a setting time when the internal reference source charges to the external decoupling capacitor. The REF_CMP voltage does not need a settling time when the ADC_REF_BUFF bit is enabled from a previous enabled status and any ADC channels that are selected by ADC MUX configuration registers are re-configured. For all the upping explanations, assume that the internal reference is already enabled by setting PREF bit (which is configured in register 0xB4).

REGISTER MAPS (continued)

Table 9. CONV-RATE[1:0] Bit Configuration

CONV-RATE[1:0]	Unipolar Channel Sample Time (μs)		Bipolar Channel Sample Time (μs)	
	Direct Mode	Auto Mode (1)	Direct Mode	Auto Mode (1)
00	13.9	11.5	36.9	34.5
01	25.4	23	36.9	34.5
10	36.9	34.5	36.9	34.5
11	71.4	69	71.4	69

NOTE:
1. For auto mode, the first sample time needs additional 1.4μs, and the following sample time will be compliant with Table 9.

REG0x11: False Alarm Configuration Register [reset = 0x70]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:5]	CH_FALR_CT[2:0]	011	R/W	False Alarm Protection Counters for ADC Channels. It sets how many times of false sample results need to be countered before an alarm is triggered. See Table 10 for configuration details.
D[4:3]	TEMP_FALR_CT[1:0]	10	R/W	False Alarm Protection Counters for Temperature Sensor. It sets how many times of false temperature sample results need to be countered before an alarm is triggered. See Table 11 for configuration details.
D[2:0]	Reserved	000	R/W	Reserved

Table 10. CH_FALR_CT[2:0] Bit Configuration

CH_FALR_CT[2:0]	N Consecutive Samples before Alarm is Set
000	1
001	4
010	8
011	16
100	32
101	64
110	128
111	256

Table 11. TEMP_FALR_CT[1:0] Bit Configuration

TEMP_FALR_CT[1:0]	N Consecutive Samples before Alarm is Set
00	1
01	2
10	4
11	8

REGISTER MAPS (continued)

REG0x12: GPIO Configuration Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:5]	Reserved	000	R/W	Reserved
D[4]	Reserved	0	R/W	Reserved
D[3]	EN_DAV	0	R/W	nDAV Pin Enable 0 = GPIO3 operation (default) 1 = nDAV operation
D[2]	EN_ADCTRIG	0	R/W	nADCTRIG Pin Enable 0 = GPIO2 operation (default) 1 = nADCTRIG operation
D[1]	EN_ALARMOUT	0	R/W	nALARMOUT Pin Enable 0 = GPIO1 operation (default) 1 = nALARMOUT operation
D[0]	EN_ALARMIN	0	R/W	nALARMIN Pin Enable 0 = GPIO0 operation (default) 1 = nALARMIN operation

REG0x13: ADC MUX Configuration 0 Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	ADC7_EN	0	R/W	When this bit is set to '1', the corresponding ADC input channel ADC_n is accessed in an ADC conversion cycle. When this bit is set to '0', the corresponding ADC input channel ADC_n is ignored in an ADC conversion cycle.
D[6]	ADC6_EN	0	R/W	
D[5]	ADC5_EN	0	R/W	
D[4]	ADC4_EN	0	R/W	
D[3]	ADC3_EN	0	R/W	
D[2]	ADC2_EN	0	R/W	
D[1]	ADC1_EN	0	R/W	
D[0]	ADC0_EN	0	R/W	

REG0x14: ADC MUX Configuration 1 Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	ADC15_EN	0	R/W	When this bit is set to '1', the corresponding ADC input channel ADC_n is accessed in an ADC conversion cycle. When this bit is set to '0', the corresponding ADC input channel ADC_n is ignored in an ADC conversion cycle.
D[6]	ADC14_EN	0	R/W	
D[5]	ADC13_EN	0	R/W	
D[4]	ADC12_EN	0	R/W	
D[3]	ADC11_EN	0	R/W	
D[2]	ADC10_EN	0	R/W	
D[1]	ADC9_EN	0	R/W	
D[0]	ADC8_EN	0	R/W	

REGISTER MAPS (continued)

REG0x15: ADC MUX Configuration 2 Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:6]	Reserved	00	R/W	Reserved
D[5]	TEMP_CH	0	R/W	If it is set to ‘1’, the internal temperature sensor is accessed for ADC conversion. If it is set to ‘0’, the internal temperature sensor is ignored for ADC conversion.
D[4]	ADC20_EN	0	R/W	When this bit is set to '1', the corresponding ADC input channel ADC_n is accessed in an ADC conversion cycle. When this bit is set to '0', the corresponding ADC input channel ADC_n is ignored in an ADC conversion cycle.
D[3]	ADC19_EN	0	R/W	
D[2]	ADC18_EN	0	R/W	
D[1]	ADC17_EN	0	R/W	
D[0]	ADC16_EN	0	R/W	

REG0x18: DAC Clear Enable 0 Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	CLREN_B7	0	R/W	0 = DAC_n state is not affected by a clear event. 1 = DAC_n passively enters into a clear state with a clear event. When this bit is set to '1', the corresponding DAC channel will go into clear state when a clear event is detected as configured in the DAC clear source registers.
D[6]	CLREN_B6	0	R/W	
D[5]	CLREN_B5	0	R/W	
D[4]	CLREN_B4	0	R/W	
D[3]	CLREN_A3	0	R/W	
D[2]	CLREN_A2	0	R/W	
D[1]	CLREN_A1	0	R/W	
D[0]	CLREN_A0	0	R/W	

REG0x19: DAC Clear Enable 1 Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	CLREN_D15	0	R/W	0 = DAC_n state is not affected by a clear event. 1 = DAC_n passively enters into a clear state with a clear event. When this bit is set to '1', the corresponding DAC channel will go into clear state when a clear event is detected as configured in the DAC clear source registers.
D[6]	CLREN_D14	0	R/W	
D[5]	CLREN_D13	0	R/W	
D[4]	CLREN_D12	0	R/W	
D[3]	CLREN_C11	0	R/W	
D[2]	CLREN_C10	0	R/W	
D[1]	CLREN_C9	0	R/W	
D[0]	CLREN_C8	0	R/W	

REG0x1A: DAC Clear Source 0 Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:5]	Reserved	000	R/W	Reserved
D[4]	ADC20_ALR_CLR	0	R/W	When this bit is set to '1', the corresponding alarm will be one of sources to force DACs into a clear state. It forces DACs into a clear state ignoring DACs in any operation mode (active, auto or manual). At the same time, in order to bring DAC_n into clear mode, make sure that DAC_n is enabled in the DAC clear enable registers.
D[3]	ADC19_ALR_CLR	0	R/W	
D[2]	ADC18_ALR_CLR	0	R/W	
D[1]	ADC17_ALR_CLR	0	R/W	
D[0]	ADC16_ALR_CLR	0	R/W	

REGISTER MAPS (continued)

REG0x1B: DAC Clear Source 1 Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:4]	Reserved	0000	R/W	Reserved
D[3]	ALARMIN_ALR	0	R/W	When this bit is set to '1', the corresponding alarm will be one of sources to force DACs into a clear state. It forces DACs into a clear state ignoring DACs in any operation mode (active, auto or manual). At the same time, in order to bring DAC_n into clear mode, make sure that DAC_n is enabled in the DAC clear enable registers.
D[2]	THERM_ALR	0	R/W	
D[1]	LT_HIGH_ALR	0	R/W	
D[0]	LT_LOW_ALR	0	R/W	

REG0x1C: ALARMOUT Source 0 Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:5]	Reserved	000	R/W	Reserved
D[4]	ADC20_ALR_OUT	0	R/W	When this bit is set to '1', the corresponding alarm will be one of sources to activate the nALARMOUT pin. The nALARMOUT pin must be enabled in GPIO configuration register at the same time.
D[3]	ADC19_ALR_OUT	0	R/W	
D[2]	ADC18_ALR_OUT	0	R/W	
D[1]	ADC17_ALR_OUT	0	R/W	
D[0]	ADC16_ALR_OUT	0	R/W	

REG0x1D: ALARMOUT Source 1 Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:5]	Reserved	000	R/W	Reserved
D[4]	ALARM_LATCH_DIS	0	R/W	Alarm Latch Enable/Disable Bit 0 = Alarm bits latch enabled. When an alarm bit is set to '1', the bit only can be cleared by reading the alarm register. Before reading, the alarm bit is not cleared even if the alarm condition disappears. And if the alarm condition is not disappeared, the bit will be set again. 1 = Alarm bits are not latched. An alarm bit is set to '1', if an alarm limit is exceeded. And the alarm bit is cleared automatically if the alarm trigger condition disappeared.
D[3]	ALRIN_ALR_OUT	0	R/W	When this bit is set to '1', the corresponding alarm will be one of sources to activate the nALARMOUT pin. The nALARMOUT pin must be enabled in GPIO configuration register at the same time.
D[2]	THERM_ALR_OUT	0	R/W	
D[1]	LT_HIGH_ALR_OUT	0	R/W	
D[0]	LT_LOW_ALR_OUT	0	R/W	

REG0x1E: DAC Range 0 Register [reset = 0xXX]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	Reserved	0	R/W	Reserved
D[6:4]	DAC_RANGEB[2:0]	0xx	R/W	DAC Group B Output Voltage Range Selection. It overrides output voltage range that is set by the auto-range detection circuit. The auto-range is set when the chip is reset by a reset event. See Table 12 for configuration details.
D[3]	Reserved	0	R/W	Reserved
D[2:0]	DAC_RANGEA[2:0]	0xx	R/W	DAC Group A Output Voltage Range Selection. It overrides output voltage range that is set by the auto-range detection circuit. The auto-range is set when the chip is reset by a reset event. See Table 12 for configuration details.

REGISTER MAPS (continued)

REG0x1F: DAC Range 1 Register [reset = 0xXX]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	Reserved	0	R/W	Reserved
D[6:4]	DAC_RANGED[2:0]	0xx	R/W	DAC Group D Output Voltage Range Selection. It overrides output voltage range that is set by the auto-range detection circuit. The auto-range is set when the chip is reset by a reset event. See Table 12 for configuration details.
D[3]	Reserved	0	R/W	Reserved
D[2:0]	DAC_RANGEC[2:0]	0xx	R/W	DAC Group C Output Voltage Range Selection. It overrides output voltage range that is set by the auto-range detection circuit. The auto-range is set when the chip is reset by a reset event. See Table 12 for configuration details.

Table 12. DAC_RANGEn[2:0] Bit Configuration

DAC_RANGEn[2:0] (n = A, B, C, D)	DAC Group n Output Voltage Range
000 ~ 011	Range Set by Auto-Range Detection Circuit
100	-10V to 0V
101	-5V to 0V
110	0V to 10V
111	0V to 5V

REG0x20 ~ REG0x48: ADCn_Data (Low Byte) Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:0]	ADCn_DATA[7:0]	00000000	R	It stores the low byte of 12-bit ADC_n conversion results. The data is in straight binary format for both unipolar and bipolar input channels.

REG0x21 ~ REG0x49: ADCn_Data (High Byte) Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:4]	Reserved	0000	R	Reserved
D[3:0]	ADCn_DATA[11:8]	0000	R	It stores the high 4 bits of 12-bit ADC_n conversion results. The data is in straight binary format for both unipolar and bipolar input channels.

REG0x4A: Temperature Data (Low Byte) Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:0]	TEMP_DATA[7:0]	00000000	R	It stores low byte of the temperature sensor data. The data is in two's complement format.

REG0x4B: Temperature Data (High Byte) Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:4]	Reserved	0000	R	Reserved
D[3:0]	TEMP_DATA[11:8]	0000	R	It stores the high 4 bits of the temperature sensor data. The data is in two's complement format.

REG0x50 ~ REG0x6E: DACn_Data (Low Byte) Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:0]	DACn_DATA[7:0]	00000000	R/W	It stores low byte of the 12-bit data to be loaded to the DAC_n. The data is in straight binary format. All DAC ranges have the same data format.

REGISTER MAPS (continued)

REG0x51 ~ REG0x6F: DACn_Data (High Byte) Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:4]	Reserved	0000	R/W	Reserved
D[3:0]	DACn_DATA[11:8]	0000	R/W	It stores the high 4 bits of the 12-bit data to be loaded to the DAC_n. The data is in straight binary format. All DAC ranges have the same data format.

The SGM90516 device continuously monitors all general purpose analog inputs and local temperature sensor in normal operation.

REG0x70: Alarm Status 0 Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:5]	Reserved	000	R	Reserved
D[4]	ADC20_ALR	0	R	1 = ADC20 exceeds the restricted range defined by the corresponding threshold registers. 0 = ADC20 is within the specified range.
D[3]	ADC19_ALR	0	R	1 = ADC19 exceeds the restricted range defined by the corresponding threshold registers. 0 = ADC19 is within the specified range.
D[2]	ADC18_ALR	0	R	1 = ADC18 exceeds the restricted range defined by the corresponding threshold registers. 0 = ADC18 is within the specified range.
D[1]	ADC17_ALR	0	R	1 = ADC17 exceeds the restricted range defined by the corresponding threshold registers. 0 = ADC17 is within the specified range.
D[0]	ADC16_ALR	0	R	1 = ADC16 exceeds the restricted range defined by the corresponding threshold registers. 0 = ADC16 is within the specified range.

REG0x71: Alarm Status 1 Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:4]	Reserved	0000	R	Reserved
D[3]	ALARMIN_ALR	0	R	1 = nALARMIN pin is enabled and input is logic high.
D[2]	THERM_ALR	0	R	Thermal Alarm Flag. If the internal temperature sensor is enabled and the die temperature is equal to or greater than +150℃, this bit will be set to '1'. This alarm has 8℃ hysteresis. If the internal temperature sensor is not enabled, this bit is always '0'.
D[1]	LT_HIGH_ALR	0	R	If the temperature sensor exceeds the upper threshold, this bit will be set to '1'.
D[0]	LT_LOW_ALR	0	R	If the temperature sensor exceeds the lower threshold, this bit will be set to '1'.

REGISTER MAPS (continued)

REG0x72: General Status Register [reset = 0x0C]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	AVSSD	—	R	It is a status indicator bit of AVSS of auto-range detection output for DAC group D. If V_{AVSSD} < V_{AVSSTH}, this bit is set to '1' (default automatically setting output range is -10V to 0V by auto-range detection function). If V_{AVSSD} > V_{AVSSTH}, this bit is set to '0' (default automatically setting output range is 0V to 5V by auto-range detection function).
D[6]	AVSSC	—	R	It is a status indicator bit of AVSS of auto-range detection output for DAC group C. If V_{AVSSC} < V_{AVSSTH}, this bit is set to '1' (default automatically setting output range is -10V to 0V by auto-range detection function). If V_{AVSSC} > V_{AVSSTH}, this bit is set to '0' (default automatically setting output range is 0V to 5V by auto-range detection function).
D[5]	AVSSB	—	R	It is a status indicator bit of AVSS of auto-range detection output for DAC group B. If V_{AVSSB} < V_{AVSSTH}, this bit is set to '1' (default automatically setting output range is -10V to 0V by auto-range detection function). If V_{AVSSB} > V_{AVSSTH}, this bit is set to '0' (default automatically setting output range is 0V to 5V by auto-range detection function).
D[4]	AVSSA	—	R	It is a status indicator bit of AVSS of auto-range detection output for DAC group A. If V_{AVSSA} < V_{AVSSTH}, this bit is set to '1' (default automatically setting output range is -10V to 0V by auto-range detection function). If V_{AVSSA} > V_{AVSSTH}, this bit is set to '0' (default automatically setting output range is 0V to 5V by auto-range detection function).
D[3]	ADC_IDLE	1	R	ADC Idle Indicate Bit. Auto mode: default value is '1'. If ADC is triggered and keeps running, the bit turns to '0' and remains '0'. If ADC is stopped, it goes to '1' again. Direct mode: default value is '1'. If ADC is triggered and keeps running, the bit turns to '0' and remains '0'. If direct mode conversion is completed, it goes to '1' again.
D[2]	Reserved	1	R	Reserved
D[1]	GALR	0	R	Global Alarm Bit. Any of the alarm bits setting will cause this bit to be set to '1'. Once this bit is set, it will remain '1' until a reading operation to the alarm status register.
D[0]	DAVF	0	R	ADC Data Available Flag Bit. It is useful in direct mode only and keeps '0' in auto mode. 0 = ADC is converting 1 = ADC conversion is completed and ADC data is ready

REG0x7A: GPIO Register [reset = 0xFF]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	GPIO_7	1	R/W	When the GPIOn pin is used as output, writing '1' will set the pin to high impedance. Writing '0' will set the pin to logic low. Whether the GPIOn pin is used as output or input, a read operation will get the status of the GPIOn pin. Each GPIOn pin has 60kΩ input impedance to IOVDD.
D[6]	GPIO_6	1	R/W	
D[5]	GPIO_5	1	R/W	
D[4]	GPIO_4	1	R/W	
D[3]	GPIO_3	1	R/W	
D[2]	GPIO_2	1	R/W	
D[1]	GPIO_1	1	R/W	
D[0]	GPIO_0	1	R/W	

REGISTER MAPS (continued)

The unipolar ADC input channels (LV_ADC16 to LV_ADC20) and internal temperature sensor have out-of-range alarm function. The upper-thresh registers set the upper limitations, and the lower-thresh registers set the lower limitations. If the ADC results or the temperature data exceeds the limitations, the corresponding ADCn_ALR bit will be set to '1' (in the alarm status 0 register). The ADC threshold values are set in straight binary format and the temperature threshold are set in two's complement format.

REG0x80 ~ REG0x90: ADCn Upper Threshold (Low Byte) Register [reset = 0xFF]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:0]	THRUn[7:0]	11111111	R/W	It sets the low byte of 12-bit upper threshold for the ADCn channel. It is in straight binary format.

REG0x81 ~ REG0x91: ADCn Upper Threshold (High Byte) Register [reset = 0x0F]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:4]	Reserved	0000	R/W	Reserved
D[3:0]	THRUn[11:8]	1111	R/W	It sets high 4 bits of 12-bit upper threshold for the ADCn channel. It is in straight binary format.

REG0x82 ~ REG0x92: ADCn Lower Threshold (Low Byte) Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:0]	THRLn[7:0]	00000000	R/W	It sets the low byte of 12-bit lower threshold for the ADCn channel. It is in straight binary format.

REG0x83 ~ REG0x93: ADCn Lower Threshold (High Byte) Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:4]	Reserved	0000	R/W	Reserved
D[3:0]	THRLn[11:8]	0000	R/W	It sets high 4 bits of 12-bit lower threshold for the ADCn channel. It is in straight binary format.

REG0x94: LT Upper Threshold (Low Byte) Register [reset = 0xFF]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:0]	THRU_LT[7:0]	11111111	R/W	It sets the low byte of 12-bit upper threshold for the local temperature sensor. It is in two's complement format.

REG0x95: LT Upper Threshold (High Byte) Register [reset = 0x07]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:4]	Reserved	0000	R/W	Reserved
D[3:0]	THRU_LT[11:8]	0111	R/W	It sets high 4 bits of 12-bit upper threshold for the local temperature sensor. It is in two's complement format.

REG0x96: LT Lower Threshold (Low Byte) Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:0]	THRL_LT[7:0]	00000000	R/W	It sets the low byte of 12-bit lower threshold for the local temperature sensor. It is in two's complement format.

REG0x97: LT Lower Threshold (High Byte) Register [reset = 0x08]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:4]	Reserved	0000	R/W	Reserved.
D[3:0]	THRL_LT[11:8]	1000	R/W	It sets high 4 bits of 12-bit lower threshold for the local temperature sensor. It is in two's complement format.

REGISTER MAPS (continued)

The hysteresis registers define the hysteresis in the out-of-range alarms.

REG0xA0 ~ REG0xA4: ADCn Hysteresis Register [reset = 0x08]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	Reserved	0	R/W	Reserved
D[6:0]	HYSTn[6:0]	0001000	R/W	Hysteresis of General Purpose ADC_n with 1 LSB Resolution

REG0xA5: LT Hysteresis Register [reset = 0x08]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:5]	Reserved	000	R/W	Reserved
D[4:0]	HYST_LT[4:0]	01000	R/W	Hysteresis of Local Temperature Sensor with 0.25℃ Resolution. The range is 0℃ to 8℃.

REG0xB0: DAC Clear 0 Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	CLR_B7	0	R/W	This register is used to force the corresponding DAC_n into a clear state. If CLR_n = 1, DAC_n is forced into a clear state. If CLR_n = 0, DAC_n is restored to normal operation.
D[6]	CLR_B6	0	R/W	
D[5]	CLR_B5	0	R/W	
D[4]	CLR_B4	0	R/W	
D[3]	CLR_A3	0	R/W	
D[2]	CLR_A2	0	R/W	
D[1]	CLR_A1	0	R/W	
D[0]	CLR_A0	0	R/W	

REG0xB1: DAC Clear 1 Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	CLR_D15	0	R/W	This register is used to force the corresponding DAC_n into a clear state. If CLR_n = 1, DAC_n is forced into a clear state. If CLR_n = 0, DAC_n is restored to normal operation.
D[6]	CLR_D14	0	R/W	
D[5]	CLR_D13	0	R/W	
D[4]	CLR_D12	0	R/W	
D[3]	CLR_C11	0	R/W	
D[2]	CLR_C10	0	R/W	
D[1]	CLR_C9	0	R/W	
D[0]	CLR_C8	0	R/W	

REGISTER MAPS (continued)

REG0xB2: Power-Down 0 Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	PDAC_B7	0	R/W	Setting the bit to '1' to enable the corresponding DAC channel function. 1 = DAC_n is powered up. 0 = DAC_n is powered down. After power-on or reset, these bits are all set to 0 by default and all the DACs enter power-down mode.
D[6]	PDAC_B6	0	R/W	
D[5]	PDAC_B5	0	R/W	
D[4]	PDAC_B4	0	R/W	
D[3]	PDAC_A3	0	R/W	
D[2]	PDAC_A2	0	R/W	
D[1]	PDAC_A1	0	R/W	
D[0]	PDAC_A0	0	R/W	

REG0xB3: Power-Down 1 Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	PDAC_D15	0	R/W	Setting the bit to '1' to enable the corresponding DAC channel function. 1 = DAC_n is powered up. 0 = DAC_n is powered down. After power-on or reset, these bits are all set to 0 by default and all the DACs enter power-down mode.
D[6]	PDAC_D14	0	R/W	
D[5]	PDAC_D13	0	R/W	
D[4]	PDAC_D12	0	R/W	
D[3]	PDAC_C11	0	R/W	
D[2]	PDAC_C10	0	R/W	
D[1]	PDAC_C9	0	R/W	
D[0]	PDAC_C8	0	R/W	

REG0xB4: Power-Down 2 Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:2]	Reserved	000000	R/W	Reserved
D[1]	PREF	0	R/W	Setting PREF and PADC bits to '1' to enable the corresponding ADC and internal reference functions, respectively. 1 = internal REF or ADC is powered up. 0 = internal REF or ADC is powered down. After power-on or reset, these bits are all set to 0 by default, and the internal reference and the ADC enter power-down mode.
D[0]	PADC	0	R/W	

REG0xC0: ADC Trigger Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:1]	Reserved	0000000	R/W	Reserved
D[0]	ICONV	0	R/W	Internal ADC Conversion Trigger Bit Set it to '1' to trigger an ADC conversion start. Once the ADC conversion starts, the bit is set to '0' automatically.

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DECEMBER 2024 – REV.A.2 to REV.A.3	Page
Updated pinout pin 20 from DAC_AB to AVCC_AB	3

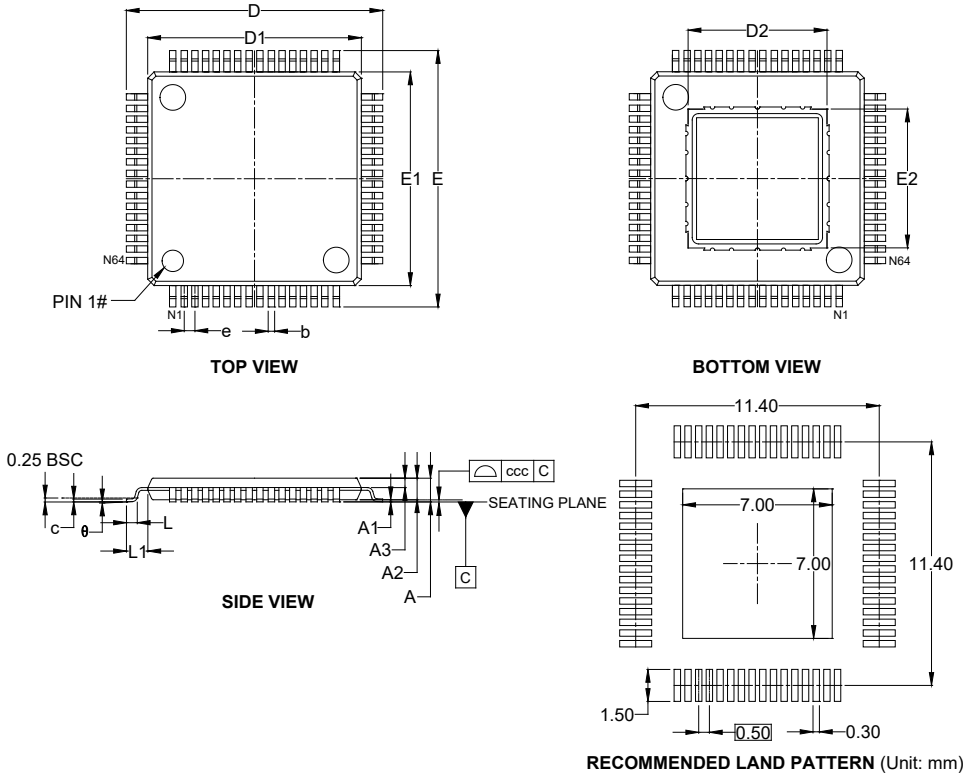
JANUARY 2024 – REV.A.1 to REV.A.2	Page
Changed Package Outline Dimensions section	51

NOVEMBER 2023 – REV.A to REV.A.1	Page
Changed Electrical Characteristics section	9

Changes from Original (JUNE 2023) to REV.A	Page
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

TQFP-10×10-64L (Exposed Pad)

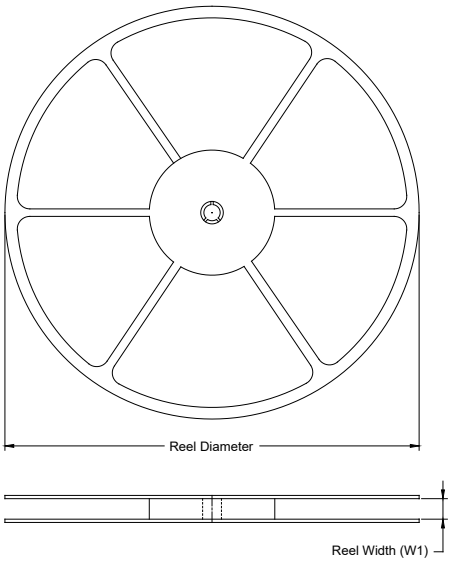


Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	-	-	1.200
A1	0.050	-	0.150
A2		1.000 REF	
A3	0.390	-	0.490
b	0.170	-	0.270
c	0.090	-	0.180
D	11.800	-	12.200
D1	9.900	-	10.100
D2	5.900	-	6.800
E	11.800	-	12.200
E1	9.900	-	10.100
E2	5.900	-	6.800
e		0.500 BSC	
L	0.450	-	0.750
L1		1.000 REF	
θ	0°	-	7°
ccc		0.080	

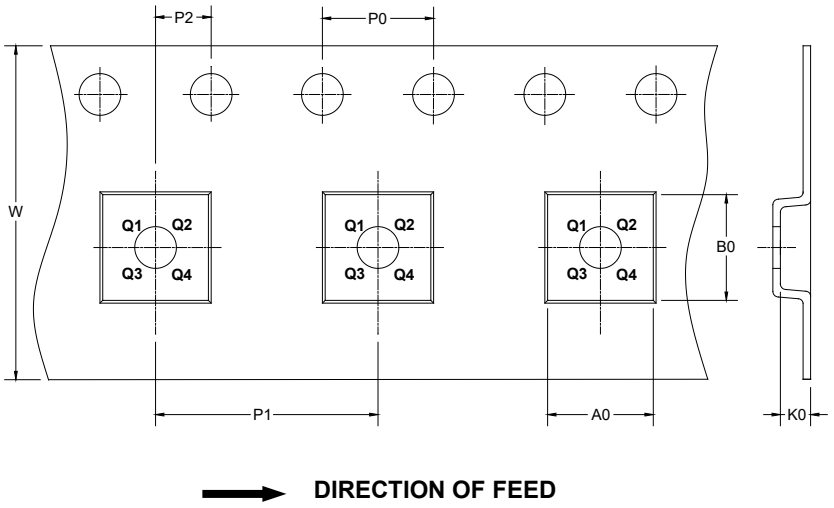
NOTES:
1. This drawing is subject to change without notice.
2. The dimensions do not include mold flashes, protrusions or gate burrs.
3. Reference JEDEC MS-026.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



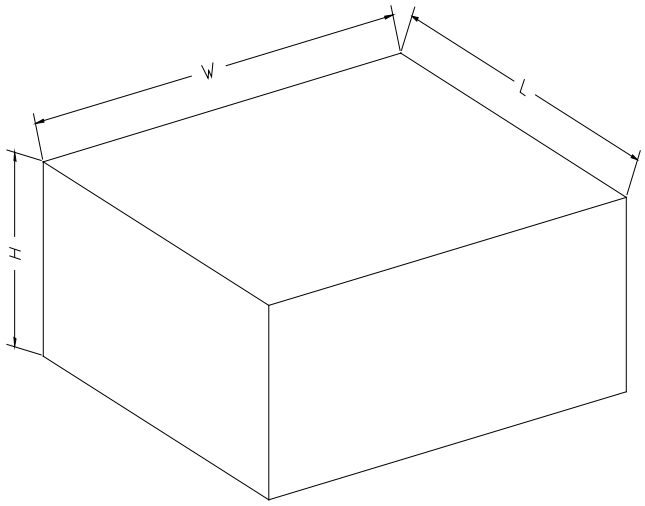
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TQFP-10×10-64L (Exposed Pad)	13"	24.4	12.70	12.70	1.70	4.0	16.0	2.0	24.0	Q2

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002