74AHC595

8-Bit Serial-In/Serial-Out or Parallel-Out Shift Register with Output Latches

GENERAL DESCRIPTION

The 74AHC595 is a high-speed Si-gate CMOS device. The device is an 8-bit serial-in/serial-out or parallel-out shift register with output latches.

This device features a serial input and a serial standard output for cascading. All of the 8 shift register stages have the asynchronous reset function when active low. When $\overline{\mathrm{OE}}$ is held low, the data in storage register will appear at the outputs. When $\overline{\mathrm{OE}}$ is held high, all outputs except Q7S are in high-impedance state.

Both the shift register and storage register have separate clocks. The shift register clock (SHCP) is positive-edge triggered. Data is shifted on the positive-going transitions of the SHCP. The storage register clock (STCP) is also positive-edge triggered. The data in each register is transferred to the storage register on a positive-going transition of the STCP.

The 74AHC595 is available in Green TSSOP-16 and SOIC-16 packages. It operates over a temperature range of -40℃ to +125℃.

FEATURES

- **Wide Operating Voltage Range: 2.0V to 5.5V**
- **Inputs Accept Voltages Higher than the Supply Voltage**
- **All Inputs with Schmitt-Trigger Actions**
- **Balanced Propagation Delays**
- **Operate with CMOS Input Level**
- **-40℃ to +125℃ Operating Temperature Range**
- **Available in Green TSSOP-16 and SOIC-16 Packages**

APPLICATIONS

Remote Control Holding Registers

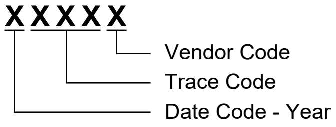
Serial-to-Parallel Data Conversion

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
74AHC595	TSSOP-16	-40℃ to +125℃	74AHC595XTS16G/TR	74AHC595 XTS16 XXXXX	Tape and Reel, 4000
	SOIC-16	-40℃ to +125℃	74AHC595XS16G/TR	74AHC595XS16 XXXXX	Tape and Reel, 2500

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS (1)

Supply Voltage Range, V_{CC}	-0.5V to 7V
Input Voltage Range, V_I	-0.5V to 7V
Input Clamp Current, I_{IK} (2) (V_I < -0.5V)	-20mA
Output Clamp Current, I_{OK} (2) (V_O < -0.5V or V_O > V_{CC} + 0.5V)	±20mA
Output Current, I_O (V_O = -0.5V to V_{CC} + 0.5V)	±25mA
Supply Current, I_{CC}	75mA
Ground Current, I_{GND}	-75mA
Junction Temperature (3)	+150℃
Storage Temperature Range	-65℃ to +150℃
Lead Temperature (Soldering, 10s)	+260℃
ESD Susceptibility	
HBM	3000V
CDM	1000V

RECOMMENDED OPERATING CONDITIONS

Supply Voltage Range, V_{CC}	2.0V to 5.5V
Input Voltage Range, V_I	0V to 5.5V
Output Voltage Range, V_O	0V to V_{CC}
Input Transition Rise or Fall Rate, Δt/ΔV	
V_{CC} = 3.0V to 3.6V	100ns/V (MAX)
V_{CC} = 4.5V to 5.5V	20ns/V (MAX)
Operating Temperature Range	-40℃ to +125℃

OVERSTRESS CAUTION

1. Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

2. The input and output voltage ratings may be exceeded if the input and output clamp current ratings are observed.

3. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability.

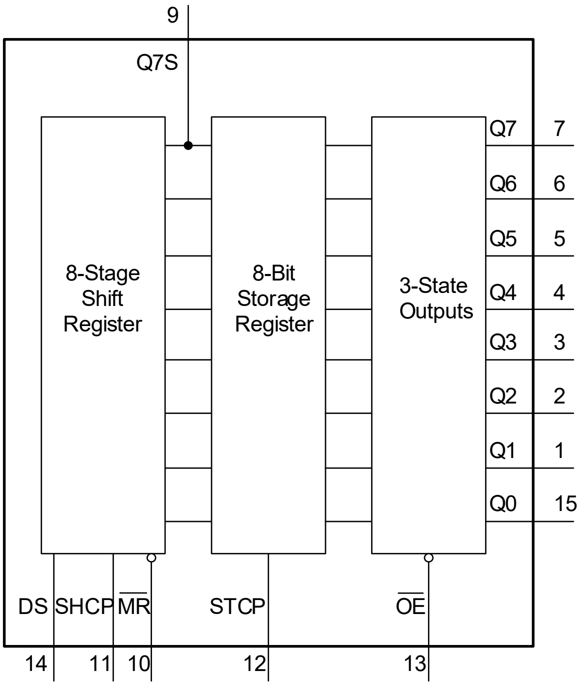
ESD SENSITIVITY CAUTION

This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

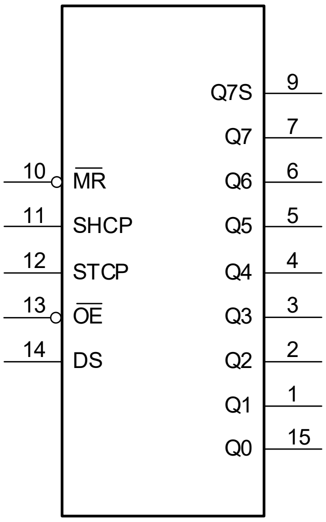
DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

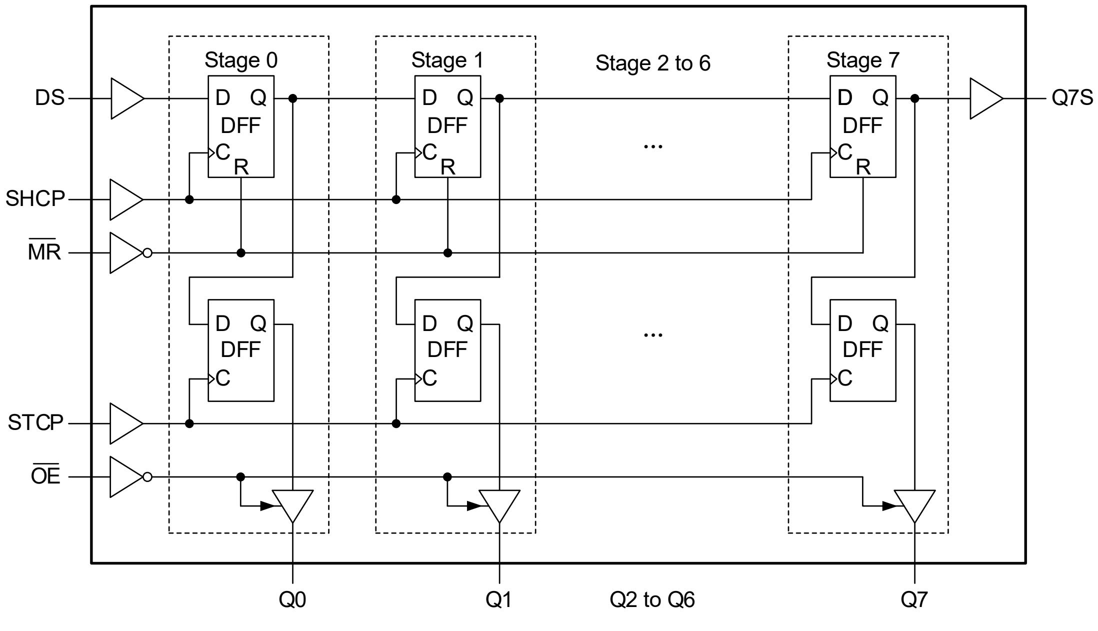
FUNCTIONAL DIAGRAM



LOGIC SYMBOL



LOGIC DIAGRAM



FUNCTION TABLE

CONTROL INPUTS				INPUT	OUTPUTS		FUNCTION
SHCP	**STCP**	**$\overline{OE}$**	**$\overline{MR}$**	**DS**	**Q7S**	**Qn**	
X	*X*	L	L	*X*	L	NC	A low-level on $\overline{MR}$ only affects the shift register.
X	↑	L	L	*X*	L	L	Empty shift register loaded into storage register.
X	*X*	H	L	*X*	L	Z	Shift register clear, parallel outputs in high-impedance off-state.
↑	*X*	L	H	H	Q6S	NC	Logic high-level shifted into shift register Stage 0. Contents of all shift register stages shifted through, e.g. previous state of Stage 6 (internal Q6S) appears on the serial output (Q7S).
X	↑	L	H	*X*	NC	QnS	Contents of shift register stages (internal QnS) are transferred to the storage register and parallel output stages.
↑	↑	L	H	*X*	Q6S	QnS	Contents of shift register shifted through, previous contents of the shift register are transferred to the storage register and parallel output stages.

H = High Voltage Level

L = Low Voltage Level

↑ = Low-to-High Clock Transition

Z = High-Impedance State

NC = No Change

X = Don't Care

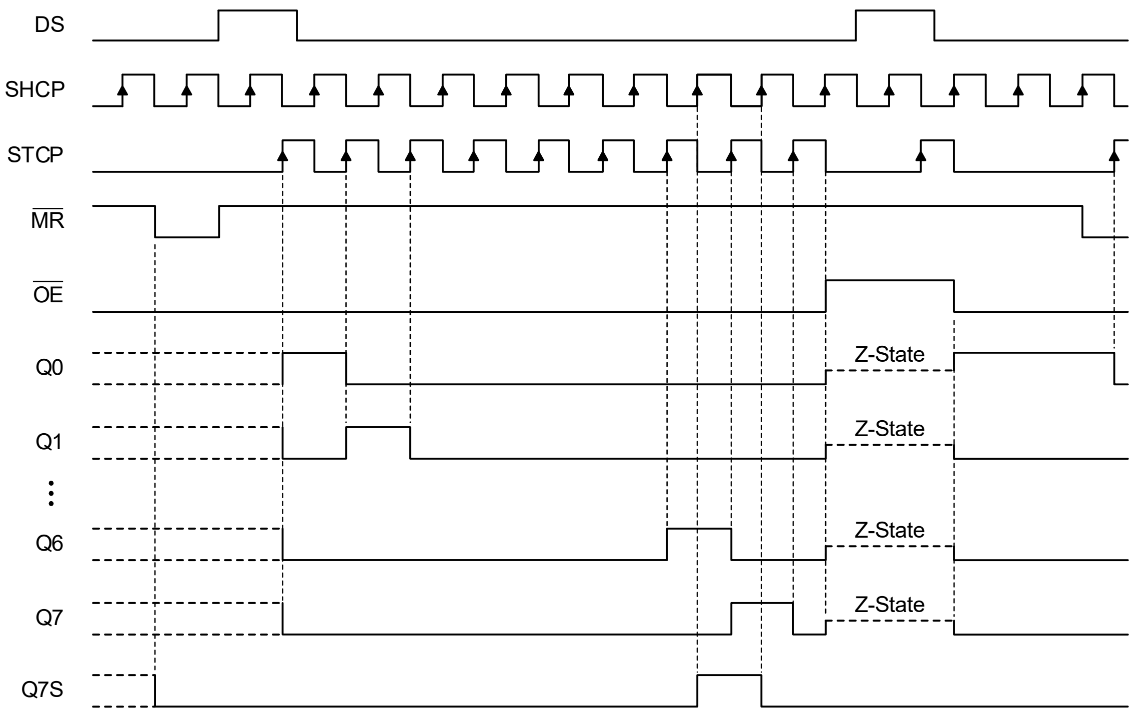
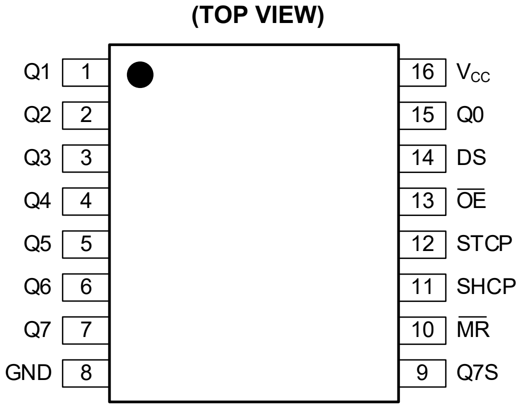


Figure 1. Timing Diagram

PIN CONFIGURATIONS



TSSOP-16/SOIC-16

PIN DESCRIPTION

PIN	NAME	FUNCTION
15, 1, 2, 3, 4, 5, 6, 7	Q0, Q1, Q2, Q3, Q4, Q5, Q6, Q7	Parallel Data Outputs.
8	GND	Ground.
9	Q7S	Serial Data Output.
10	$\overline{\text{MR}}$	Master Reset (Active-Low).
11	SHCP	Shift Register Clock Input.
12	STCP	Storage Register Clock Input.
13	$\overline{\text{OE}}$	Output Enable Input (Active-Low).
14	DS	Serial Data Input.
16	V_{CC}	Supply Voltage.

ELECTRICAL CHARACTERISTICS

(Full = -40℃ to +125℃, all typical values are measured at T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		TEMP	MIN	TYP	MAX	UNITS
High-Level Input Voltage	V_{IH}	V_{CC} = 2.0V		Full	1.5			V
		V_{CC} = 3.0V		Full	2.1			
		V_{CC} = 5.5V		Full	3.85			
Low-Level Input Voltage	V_{IL}	V_{CC} = 2.0V		Full			0.5	V
		V_{CC} = 3.0V		Full			0.9	
		V_{CC} = 5.5V		Full			1.65	
High-Level Output Voltage	V_{OH}	$V_I = V_{IH}$ or V_{IL}	V_{CC} = 2.0V to 4.5V, I_O = -50μA	Full	V_{CC} - 0.1	V_{CC} - 0.005		V
			V_{CC} = 3.0V, I_O = -4.0mA	Full	2.4	2.8		
			V_{CC} = 4.5V, I_O = -8.0mA	Full	3.7	4.2		
Low-Level Output Voltage	V_{OL}	$V_I = V_{IH}$ or V_{IL}	V_{CC} = 2.0V to 4.5V, I_O = 50μA	Full		0.005	0.1	V
			V_{CC} = 3.0V, I_O = 4.0mA	Full		0.2	0.55	
			V_{CC} = 4.5V, I_O = 8.0mA	Full		0.3	0.55	
Input Leakage Current	I_I	V_{CC} = 0V to 5.5V, V_I = 5.5V or GND		+25℃		±0.1	±1	μA
				Full			±2	
Off-State Output Current	I_{OZ}	V_{CC} = 5.5V, $V_I = V_{IH}$ or V_{IL}, $V_O = V_{CC}$ or GND		+25℃		±0.1	±1	μA
				Full			±10	
Supply Current	I_{CC}	V_{CC} = 5.5V, $V_I = V_{CC}$ or GND, I_O = 0A		+25℃		0.1	2	μA
				Full			20	
Input Capacitance	C_I			+25℃		6		pF

DYNAMIC CHARACTERISTICS

(See Figure 2 for test circuit. Full = -40℃ to +125℃, all typical values are measured at T_A = +25℃, V_{CC} = 3.3V and 5.0V respectively, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS			TEMP	MIN [1]	TYP	MAX [1]	UNITS
Propagation Delay	t_{PD}	SHCP to Q7S [2], see Figure 3	V_{CC} = 3.0V to 3.6V	C_L = 15pF	Full	0.5	8	16.5	ns
				C_L = 50pF	Full	0.5	10	20	
			V_{CC} = 4.5V to 5.5V	C_L = 15pF	Full	0.5	6	11.5	
				C_L = 50pF	Full	0.5	8	13.5	
		STCP to Qn [2], see Figure 4	V_{CC} = 3.0V to 3.6V	C_L = 15pF	Full	0.5	8	14.5	
				C_L = 50pF	Full	0.5	10.5	19	
			V_{CC} = 4.5V to 5.5V	C_L = 15pF	Full	0.5	6	10.5	
				C_L = 50pF	Full	0.5	8	12.5	
		$\overline{MR}$ to Q7S [3], see Figure 6	V_{CC} = 3.0V to 3.6V	C_L = 15pF	Full	0.5	6.5	14	
				C_L = 50pF	Full	0.5	8	17.5	
			V_{CC} = 4.5V to 5.5V	C_L = 15pF	Full	0.5	5	9.5	
				C_L = 50pF	Full	0.5	6	11.5	
Enable Time [4]	t_{EN}	$\overline{OE}$ to Qn, see Figure 7	V_{CC} = 3.0V to 3.6V	C_L = 15pF	Full	0.5	7	14.5	ns
				C_L = 50pF	Full	0.5	9	18	
			V_{CC} = 4.5V to 5.5V	C_L = 15pF	Full	0.5	5.5	11	
				C_L = 50pF	Full	0.5	7	13	
Disable Time [5]	t_{DIS}	$\overline{OE}$ to Qn, see Figure 7	V_{CC} = 3.0V to 3.6V	C_L = 15pF	Full	0.5	7	14	ns
				C_L = 50pF	Full	0.5	12	18.5	
			V_{CC} = 4.5V to 5.5V	C_L = 15pF	Full	0.5	7	12.5	
				C_L = 50pF	Full	0.5	8	14	
Maximum Frequency	f_{MAX}	SHCP or STCP, see Figure 3 and Figure 4	V_{CC} = 3.0V to 3.6V		Full	80	165		MHz
			V_{CC} = 4.5V to 5.5V		Full	110	165		
Pulse Width	t_W	SHCP high or low, see Figure 3	V_{CC} = 3.0V to 3.6V		Full	5			ns
			V_{CC} = 4.5V to 5.5V		Full	5			
		STCP high or low, see Figure 4	V_{CC} = 3.0V to 3.6V		Full	5			
			V_{CC} = 4.5V to 5.5V		Full	5			
		$\overline{MR}$ Low, see Figure 6	V_{CC} = 3.0V to 3.6V		Full	5			
			V_{CC} = 4.5V to 5.5V		Full	5			

NOTES:

1. Specified by design and characterization, not production tested.
2. t_{PD} is the same as t_{PHL} and t_{PLH}.
3. t_{PD} is the same as t_{PHL} only.
4. t_{EN} is the same as t_{PZL} and t_{PZH}.
5. t_{DIS} is the same as t_{PLZ} and t_{PHZ}.

DYNAMIC CHARACTERISTICS (continued)

(See Figure 2 for test circuit. Full = -40℃ to +125℃, all typical values are measured at T_A = +25℃, V_{CC} = 3.3V and 5.0V respectively, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		TEMP	MIN [1]	TYP	MAX [1]	UNITS
Setup Time	t_{SU}	DS to SHCP, see Figure 5	V_{CC} = 3.0V to 3.6V	Full	3.5			ns
			V_{CC} = 4.5V to 5.5V	Full	3			
		SHCP to STCP, see Figure 4	V_{CC} = 3.0V to 3.6V	Full	8			
			V_{CC} = 4.5V to 5.5V	Full	5			
Hold Time	t_H	DS to SHCP, see Figure 5	V_{CC} = 3.0V to 3.6V	Full	2.5			ns
			V_{CC} = 4.5V to 5.5V	Full	2			
Recovery Time	t_{REC}	$\overline{MR}$ to SHCP, see Figure 6	V_{CC} = 3.0V to 3.6V	Full	3			ns
			V_{CC} = 4.5V to 5.5V	Full	2.5			
Power Dissipation Capacitance [2] [3]	C_{PD}	f_i = 1MHz, V_I = GND to V_{CC}		+25℃		180		pF

NOTES:

1. Specified by design and characterization, not production tested.

2. C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma(C_L \times V_{CC}^2 \times f_o)$

   where:

   f_i = Input frequency in MHz.

   f_o = Output frequency in MHz.

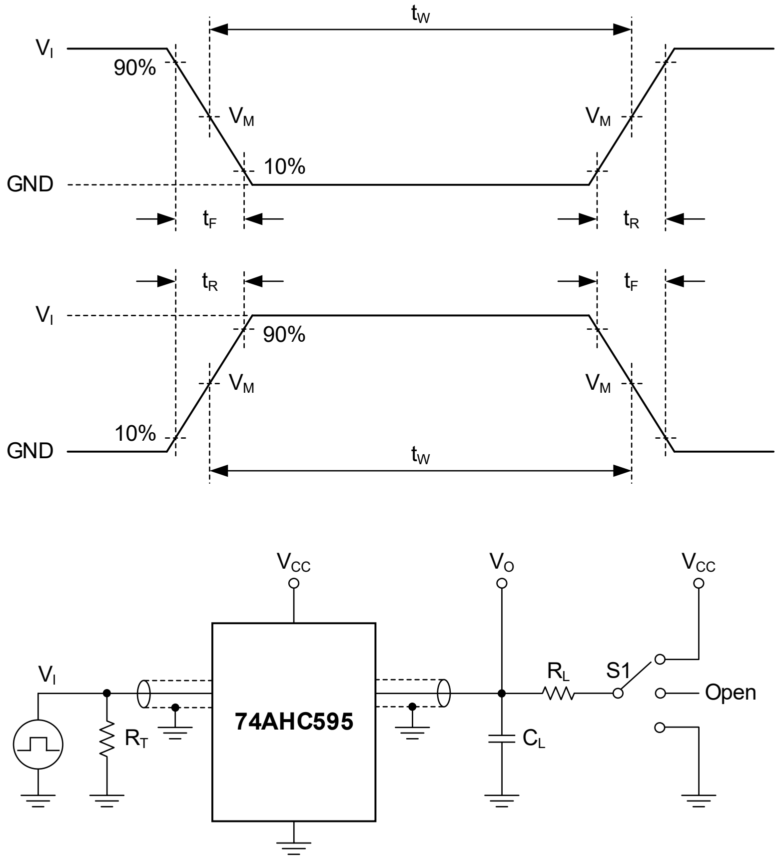
   C_L = Output load capacitance in pF.

   V_{CC} = Supply voltage in Volts.

   $\Sigma(C_L \times V_{CC}^2 \times f_o)$ = Sum of outputs.

3. All 9 outputs switching.

TEST CIRCUIT



Test conditions are given in Table 1.

Definitions test circuit:

R_L: Load resistance.

C_L: Load capacitance (includes jig and probe).

R_T: Termination resistance (equals to output impedance Z_O of the pulse generator).

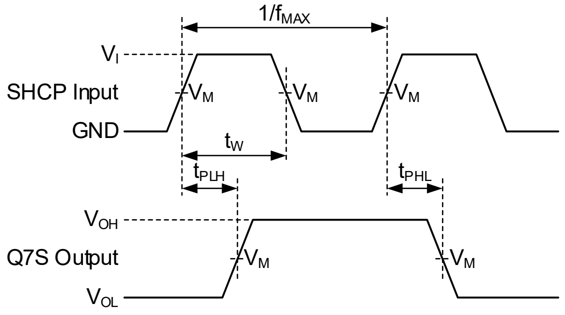
S1: Test selection switch.

Figure 2. Test Circuit for Measuring Switching Times

Table 1. Test Conditions

SUPPLY VOLTAGE	INPUT		LOAD		S1 POSITION		
V_{CC}	V_I	t_R, t_F	C_L	R_L	t_{PHL}, t_{PLH}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
2.0V to 5.5V	V_{CC}	≤ 3.0ns	15pF, 50pF	1kΩ	Open	GND	V_{CC}

WAVEFORMS

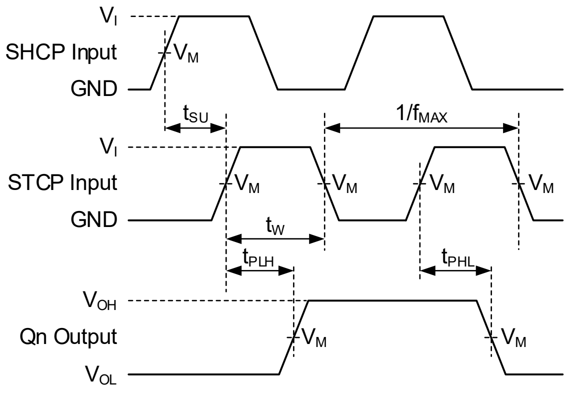


Test conditions are given in Table 1.

Measurement points are given in Table 2.

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Figure 3. Shift Register Clock Input to Output Propagation Delay Times, Pulse Width and Maximum Frequency

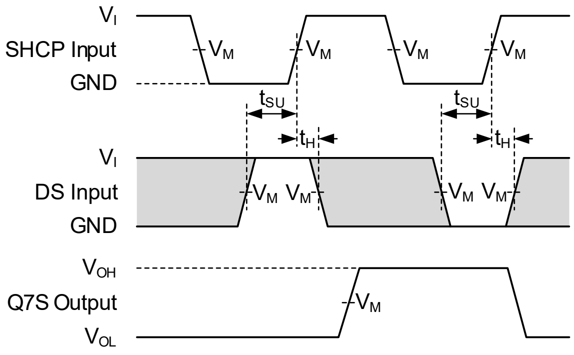


Test conditions are given in Table 1.

Measurement points are given in Table 2.

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Figure 4. Storage Register Clock Input to Output Propagation Delay Times, Shift Register Clock to Storage Register Clock Setup Time, Pulse Width and Maximum Frequency



Test conditions are given in Table 1.

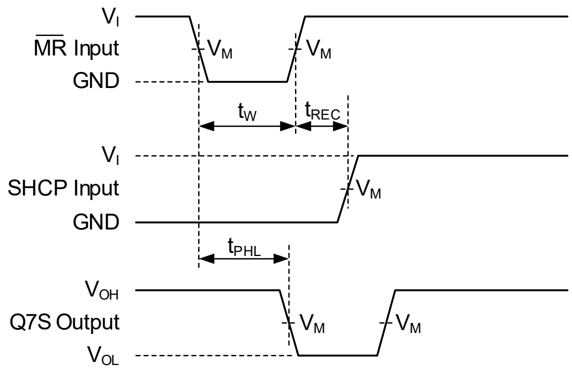
Measurement points are given in Table 2.

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

The shaded areas refer to when the input is allowed to change for predictable output performance.

Figure 5. Data Setup and Hold Times

WAVEFORMS (continued)

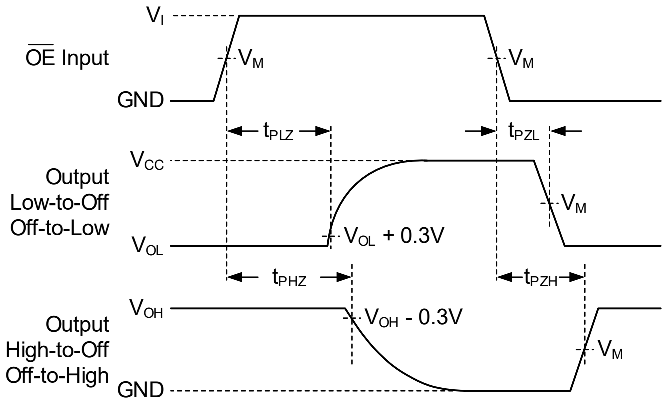


Test conditions are given in Table 1.

Measurement points are given in Table 2.

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Figure 6. Master Reset to Output Propagation Delay Times, Pulse Width and Recovery Time



Test conditions are given in Table 1.

Measurement points are given in Table 2.

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Figure 7. Enable and Disable Times

Table 2. Measurement Points

SUPPLY VOLTAGE	INPUT	OUTPUT
V_{CC}	V_M [1]	V_M
2.0V to 5.5V	0.5 × V_{CC}	0.5 × V_{CC}

NOTE:

1. The measurement points should be V_{IH} or V_{IL} when the input rising or falling time exceeds 3.0ns.

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

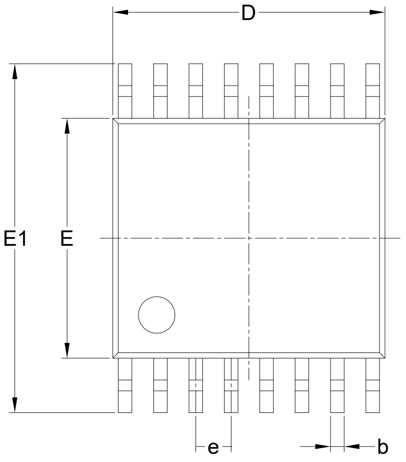
MARCH 2026 – REV.A.1 to REV.A.2	Page
Updated General Description section	1
Updated Logic Diagram section	4
Updated Package Outline Dimensions section	14

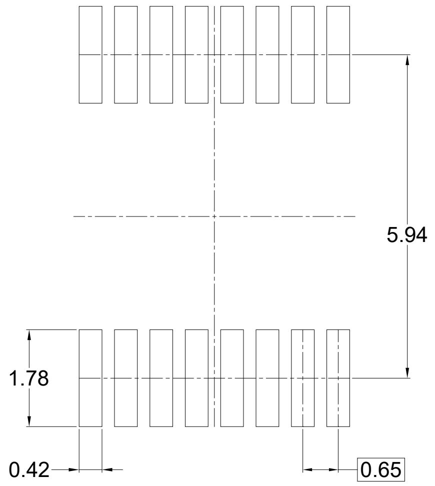
SEPTEMBER 2022 – REV.A to REV.A.1	Page
Updated Electrical Characteristics section	6
Updated Dynamic Characteristics section	7
Added SOIC-16 package	All

Changes from Original (SEPTEMBER 2021) to REV.A	Page
Changed from product preview to production data	All

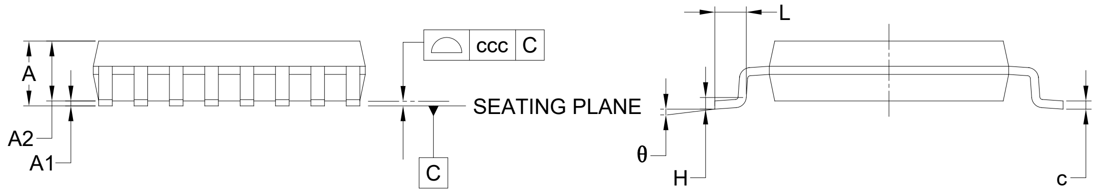
PACKAGE OUTLINE DIMENSIONS

TSSOP-16





RECOMMENDED LAND PATTERN (Unit: mm)

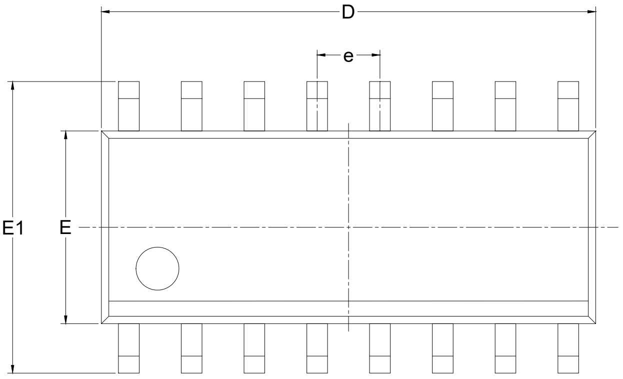


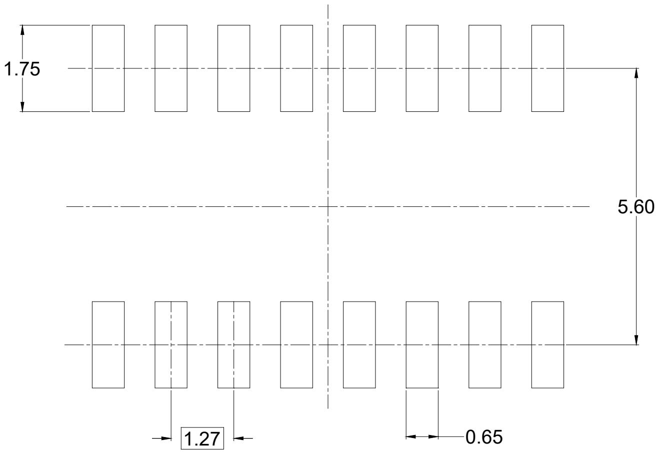
Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	-	-	1.200
A1	0.050	-	0.150
A2	0.800	-	1.050
b	0.190	-	0.300
c	0.090	-	0.200
D	4.860	-	5.100
E	4.300	-	4.500
E1	6.200	-	6.600
e	0.650 BSC		
L	0.450	-	0.750
H	0.250 TYP		
θ	0°	-	8°
ccc	0.100		

NOTES:
1. This drawing is subject to change without notice.
2. The dimensions do not include mold flashes, protrusions or gate burrs.
3. Reference JEDEC MO-153.

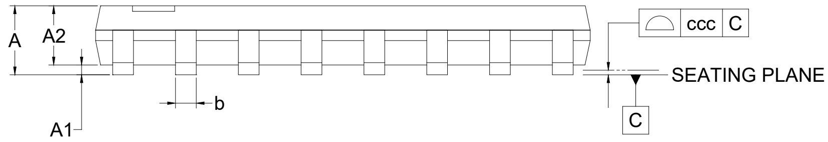
PACKAGE OUTLINE DIMENSIONS

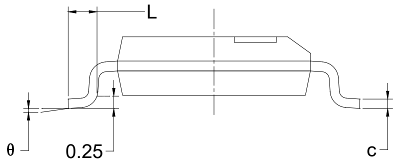
SOIC-16





RECOMMENDED LAND PATTERN (Unit: mm)



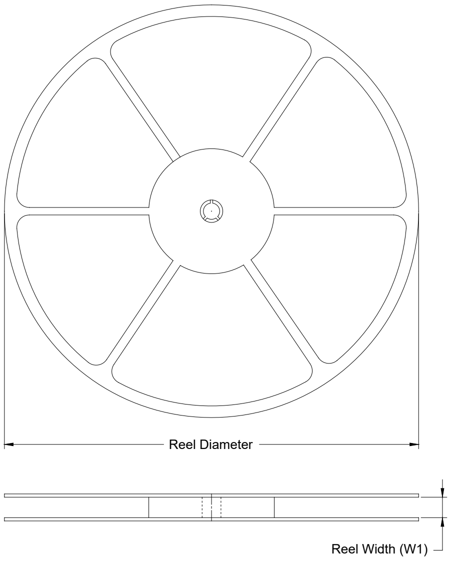


Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	-	-	1.750
A1	0.100	-	0.250
A2	1.250	-	1.550
b	0.310	-	0.510
c	0.100	-	0.250
D	9.800	-	10.200
E	3.800	-	4.000
E1	5.800	-	6.200
e	1.270 BSC		
L	0.400	-	1.270
θ	0°	-	8°
ccc	0.100		

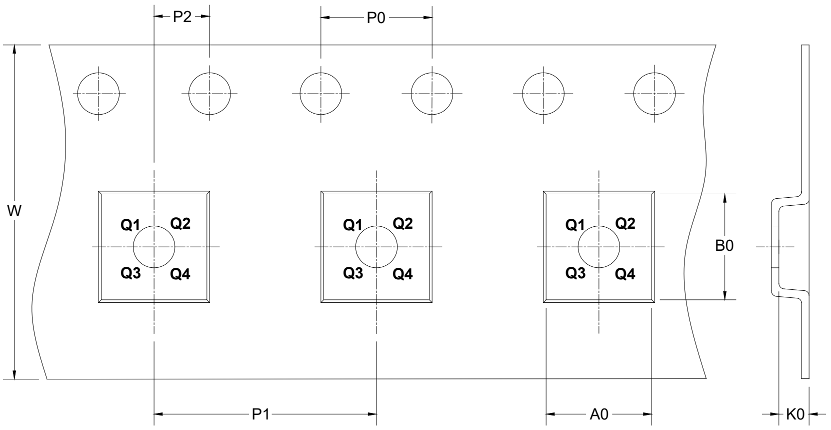
NOTES:
1. This drawing is subject to change without notice.
2. The dimensions do not include mold flashes, protrusions or gate burrs.
3. Reference JEDEC MS-012.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



DIRECTION OF FEED

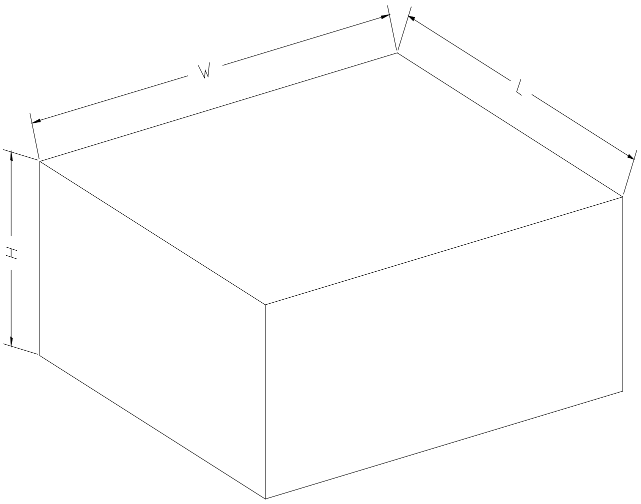
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TSSOP-16	13″	12.4	6.90	5.60	1.50	4.0	8.0	2.0	12.0	Q1
SOIC-16	13″	16.4	6.50	10.30	2.10	4.0	8.0	2.0	16.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

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