SGM41551

I²C Controlled, 3.52A, Maximum 16V Input, Charger with NVDC Power Path Management and OTG Output

FEATURES

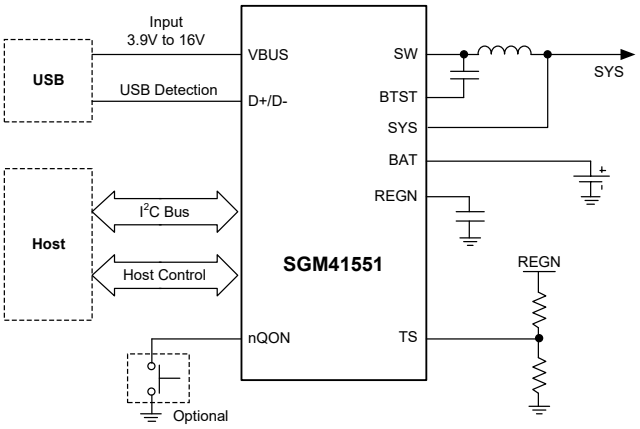
- High Efficiency, 1.5MHz, Synchronous Buck Charger
  - > 90% Charge Efficiency down to 120mA Output Current from 5V Input
  - Adjustable Charge Termination Current from 10mA to 1240mA
  - Flexible JEITA Profile to Support Safe Charging of Device
- Ship Mode, Wake-Up and Full System Reset Capability by Battery FET Control
  - Low to 0.1μA Battery Leakage Current in Shutdown Mode
  - Low to 0.9μA Battery Leakage Current in Ship Mode
  - Low to 1.8μA Quiescent Current in Battery Only Mode
- USB On-The-Go (OTG) Support (Boost Mode)
  - Boost Converter with up to 2A Output
  - Boost Mode Operation Supporting 3.84V to 9.6V Output
  - Boost Efficiency of > 90% down to 100mA OTG Current
- Single Input for USB or High Voltage Adaptors
  - 3.9V to 16V Operating Input Voltage Range
  - 26V Absolute Maximum Input Voltage Rating
  - Maximum Power Tracking by Programmable Input Voltage Limit (VINDPM) with Selectable Offset
  - VINDPM Tracking of Battery Voltage
- High Battery Discharge Efficiency with 18mΩ BATFET
- Narrow Voltage DC (NVDC) Power Path Management
  - Instant-On with No or Highly Depleted Battery
  - Ideal Diode Operation in Battery Supplement Mode
- Flexible Autonomous and I²C Operation Modes for Optimal System Performance
- Integrated 12-Bit High Accuracy ADC for Monitoring of Key System Parameter
  - Input or Output Current from VBUS Pin
  - Charge or Discharge Current from BAT Pin
  - Voltage of VBUS Pin
  - Voltage of PMID Pin
  - Voltage of Battery Pin
  - Voltage of SYS Pin
  - Voltage in Percentage of Bias Reference of TS Pin
  - Die Temperature
- High Accuracy
  - ±0.5% Charge Voltage Regulation (10mV/Step)
  - ±4.8% Charge Current Regulation at 1.04A
  - ±5% Input Current Regulation at 500mA
- Safety
  - Battery Temperature Sensing (Charge/Boost Modes)
  - Thermal Regulation and Thermal Shutdown
  - Input Under-Voltage Lockout (UVLO)
  - Input Over-Voltage Protection

APPLICATIONS

Smart Phones, EPOS

Portable Internet Devices and Accessory

SIMPLIFIED SCHEMATIC



GENERAL DESCRIPTION

The SGM41551 is a battery charger and system power path management device with integrated converter and power switches for using with single-cell Li-Ion or Li-polymer batteries. This highly integrated 3.52A device is capable of fast charging and supports a wide input voltage range suitable for smart phones, tablets and portable systems. I^2C programming makes it a very flexible powering and charger design solution.

The device includes four main power switches: input reverse blocking FET (RBFET, Q1), high-side switching FET for Buck or Boost mode (HSFET, Q2), low-side switching FET for Buck or Boost mode (LSFET, Q3) and battery FET that controls the interconnection of the system and battery (BATFET, Q4). The bootstrap diode for the high-side gate driving is also integrated. The internal power path has a very low impedance that reduces the charging time and maximizes the battery discharge efficiency. Moreover, the input voltage and current regulations provide maximum charging power delivery to the battery with various types of input sources.

A wide range of input sources are supported, including standard USB hosts, charging ports and USB compliant high voltage adaptors. The default input current limit is automatically selected based on the built-in USB interface. This limit is determined by the detection circuit in the system (e.g. USB PHY). The SGM41551 is USB 2.0 and USB 3.0 power specifications compliant with input current and voltage regulation. It also meets USB On-The-Go (OTG) power rating specification and is capable of boosting the battery voltage to supply on VBUS with 2A current limit.

The system voltage is regulated slightly above the battery voltage by the power path management circuit and is kept above the programmable minimum system voltage (3.52V by default). Therefore, system power is maintained even if the battery is completely depleted or removed. Dynamic power management (DPM) feature is also included that automatically reduces the charge current if the input current or voltage limit is reached. If the system load continues to increase after reduction of charge current down to zero, the power path management provides the deficit from battery by discharging battery to the system until the system power demand is fulfilled. This is called supplement mode, which prevents the input source from overloading.

Starting and termination of a charging cycle can be accomplished without software control. The sensed battery voltage is used to decide for starting phase of charging in one of the four phases of charging cycle: trickle charge, pre-conditioning, constant current or constant voltage. When the charge current falls below a preset limit and the battery voltage is above recharge threshold, the charger function will automatically terminate and end the charging cycle. If the voltage of a charged battery falls below the recharge threshold, the charger begins another charging cycle.

Several safety features are provided in the SGM41551 such as over-voltage and over-current protections, battery temperature monitoring, charging safety timing, thermal shutdown and input UVLO. TS pin is connected to an NTC thermistor for battery temperature monitoring and protection in both charge and Boost modes according to JEITA profile. This device also features thermal regulation in which the charge current is reduced, if the junction temperature exceeds 60℃ or 120℃ (selectable).

Charging status is reported by the STAT output and fault/status bits. A negative pulse is sent to the nINT output pin as soon as a fault occurs to notify the host. BATFET reset control is provided by nQON pin to exit ship mode or for a full system reset.

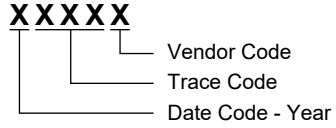
The SGM41551 is available in a Green TQFN-3×2.5-18L package.

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM41551	TQFN-3×2.5-18L	-40℃ to +85℃	SGM41551YTUV18G/TR	SGM19M XXXXX	Tape and Reel, 3000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Voltage Range (with Respect to GND)
- VBUS (Converter Not Switching) ..... -2V to 26V
- PMID (Converter Not Switching) ..... -0.3V to 26V
- BAT, SYS (Converter Not Switching) ..... -0.3V to 6V
- SW ..... -2V (50ns) to 21V
- BTST (When Converter Switching) ..... -0.3V to 27V
- D+, D-, nPG, TS ..... -0.3V to 6V
- nCE, STAT, SDA, SCL, nINT, REGN, nQON .... -0.3V to 6V

Output Sink Current
- STAT, nINT, nPG ..... 6mA (MAX)

Differential Voltage Range
- BTST-SW ..... -0.3V to 6V
- PMID-VBUS ..... -0.3V to 6V
- SYS-BAT ..... -0.3V to 6V

Package Thermal Resistance
- TQFN-3×2.5-18L, θ_{JA} ..... 53.4℃/W
- TQFN-3×2.5-18L, θ_{JB} ..... 3.8℃/W
- TQFN-3×2.5-18L, θ_{JC} ..... 34.3℃/W

Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility (1) (2)
HBM ..... ±3000V
CDM ..... ±1000V

NOTES:

1. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.
2. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

RECOMMENDED OPERATING CONDITIONS

Input Voltage Range, V_{VBUS} ..... 3.9V to 16V
Input Current (VBUS), I_{IN} ..... 3.2A (MAX)
Output DC Current (SW), I_{SWOP} ..... 3.5A (MAX)
Battery Voltage, V_{BATOP} ..... 4.8V (MAX)
Fast Charging Current, I_{CHGOP} ..... 3.52A (MAX)
RMS Discharging Current (Continuous), I_{BATOP} ..... 6A (MAX)
Peak Discharging Current (Up to 50ms) ..... 10A (MAX)
Maximum REGN Current (Up to 50ms) ..... 20mA (MAX)
Operating Junction Temperature Range ..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

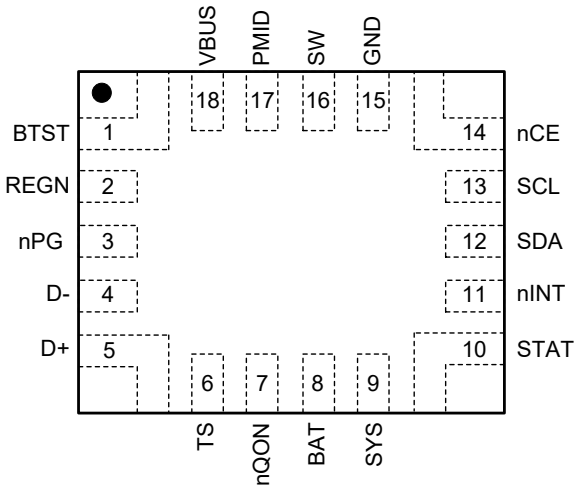
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

(TOP VIEW)



TQFN-3×2.5-18L

PIN DESCRIPTION

PIN	NAME	TYPE	FUNCTION
1	BTST	P	High-side Driver Positive Supply. It is internally connected to the bootstrap diode cathode. Use a 47nF ceramic capacitor from SW pin to BTST pin.
2	REGN	P	LDO Output that Powers LSFET Driver and Internal Circuits. Internally, the REGN pin is connected to the anode of the bootstrap diode. Place a 1μF (10V rating) ceramic capacitor between REGN pin and GND. It is recommended to place the capacitor close to the REGN pin. The REGN LDO output is used for biasing the external TS pin thermistor in SGM41551.
3	nPG	DO	Open-Drain Active Low Input Power Good Indicator. Use a 10kΩ pull-up to the logic high rail. A low state indicates a good input (V_{VBUS_UVLOZ} < V_{VBUS} < V_{VBUS_OV}, V_{VBUS} is above sleep mode threshold, and V_{VBUS} > V_{BAD_SRC} when I_{BAD_SRC} = 10mA).
4	D-	AIO	Negative USB Data Line. D+/D- based USB device protocol detection.
5	D+	AIO	Positive USB Data Line. D+/D- based USB device protocol detection.
6	TS	AI	Temperature Sense Input Pin. Connect to the battery NTC thermistor that is grounded on the other side. To program operating temperature window, it can be biased by a resistor-divider between REGN and GND. Charge suspends if TS voltage goes out of the programmed range. It is recommended to use a 103AT-2 type thermistor. If NTC or TS pin function is not needed, use a 10kΩ/10kΩ pair for the resistor-divider.
7	nQON	DI	BATFET On/Off Control Input. Use an internal pull-up to a small voltage for maintaining the default high logic (whenever a source or battery is available). In the ship mode, the BATFET is off. To exit ship mode and turn BATFET on, a logic low pulse with a duration of t_{SM_EXIT} (0.94s TYP) can be applied to nQON. When VBUS source is not connected, a logic low pulse with a duration of t_{QON_RST} (9.4s TYP) resets the system power (SYS) by turning BATFET off for t_{BATFET_RST} (300ms TYP) and then goes back to provide a full power reset for system. The nQON pin can be left floating if its function is not used.
8	BAT	P	Battery Positive Terminal Pin. Use a 10μF capacitor between BAT and GND pins close to the device. SYS and BAT pins are internally connected by BATFET with current sensing capability.
9	SYS	P	Connection Point to Converter Output. SYS is connected to the converter LC filter output that powers the system. BAT to SYS internal current (power from battery to system) is sensed. Connect 2 × 10μF capacitors between SYS pin and GND close to the device.

PIN DESCRIPTION (continued)

PIN	NAME	TYPE	FUNCTION
10	STAT	DO	Open-Drain Charge Status Output. Use a 10kΩ pull-up to the logic high rail (or an LED + a resistor). The STAT pin acts as follows: During charge: low (LED ON). Charge completed or charger in sleep mode: high (LED OFF). Charge suspended (in response to a fault): 1Hz, 50% duty cycle pulses (LED BLINKS). The function can be disabled via STAT_DIS = 1.
11	nINT	DO	Open-Drain Interrupt Output Pin. Use a 10kΩ pull-up to the logic high rail. The nINT pin is active low and sends a negative 256μs pulse to inform host about a new charger status update or a fault.
12	SDA	DIO	I²C Data Signal. Use a 10kΩ pull-up to the logic high rail.
13	SCL	DI	I²C Clock Signal. Use a 10kΩ pull-up to the logic high rail.
14	nCE	DI	Charge Enable Input Pin (Active Low). Battery charging is enabled when EN_CHG bit is 1 and nCE pin is pulled low. Do not leave nCE pin floating.
15	GND	—	Ground Pin of the Device.
16	SW	P	Switching Node Output. Connect SW pin to the output inductor. Connect a 47nF bootstrap capacitor from SW pin to BTST pin.
17	PMID	P	PMID Pin. PMID is the actual higher voltage port of converter (Buck or Boost) and is connected to the drain of the reverse blocking MOSFET (RBFET) and the drain of HSFET. Connect a 10μF ceramic capacitor from PMID pin to GND. It is the proper point for decoupling of high frequency switching currents.
18	VBUS	P	Charger Input (V_{IN}). The internal N-channel reverse blocking MOSFET (RBFET) is connected between VBUS and PMID pins. Place a 1μF ceramic capacitor from VBUS pin to GND close to the device.

NOTE: AI = analog input, AO = analog output, AIO = analog input and output, DI = digital input, DO = digital output, DIO = digital input and output, P = power.

ELECTRICAL CHARACTERISTICS

(V_{VBUS_UVLOZ} < V_{VBUS} < V_{VBUS_OV}, T_J = -40℃ to +85℃, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Quiescent Currents							
Quiescent Battery Current (BAT, SYS, SW) when the Charger is in the Battery Only Mode	I_{Q_BAT}	V_{BAT} = 4V, No VBUS, BATFET is enabled, I²C enabled, ADC disabled, system is powered by battery			1.8	3.2	μA
	$I_{Q\_BAT\_ADC}$	V_{BAT} = 4V, No VBUS, BATFET is enabled, I²C enabled, ADC enabled, system is powered by battery			1340		
Quiescent Battery Current (BAT) when the Charger is in Shutdown Mode	$I_{Q\_BAT\_SD}$	V_{BAT} = 4V, No VBUS, BATFET is disabled, I²C disabled, in shutdown mode, ADC disabled			0.1	0.35	μA
Quiescent Battery Current (BAT) when the Charger is in Ship Mode	$I_{Q\_BAT\_SHIP}$	V_{BAT} = 4V, No VBUS, BATFET is disabled, I²C enabled, in ship mode, ADC disabled			0.9	1.7	μA
Input Supply Current (VBUS) in Buck Mode	I_{VBUS_HIZ}	V_{VBUS} = 5V, V_{BAT} = 3.5V, HIZ mode, ADC disabled			5.2	10	μA
		V_{VBUS} = 15V, V_{BAT} = 3.5V, HIZ mode, ADC disabled			22.5	35	
	I_{VBUS}	V_{BAT} = 5V, V_{BAT} = 4V, I_{SYS} = 0A, charge disabled, converter switching, PSM enabled			2.2		mA
Quiescent Battery Current (BAT, SYS, SW) in Boost OTG Mode	I_{Q_OTG}	V_{BAT} = 4.2V, V_{VBUS} = 5V, OTG mode enabled, converter switching, I_{VBUS} = 0A, TS float, TS_IGNORE = 1			2.6		mA
BAT Pin and VBUS Pin Power-Up							
VBUS Operating Range	V_{VBUS_OP}	V_{VBUS} rising		3.9		16	V
VBUS Falling to Turn Off I²C, Turn Off REGN (No Battery)	V_{VBUS_UVLO}	V_{VBUS} falling		2.78	3.15	3.5	V
VBUS Rising to Turn On I²C, Turn On REGN (No Battery)	V_{VBUS_UVLOZ}	V_{VBUS} rising		3	3.33	3.66	V
VBUS Over-Voltage Rising Threshold	$V_{VBUS\_OV\_RISE}$	V_{VBUS} rising	VBUS_OVP[1:0] = 11	6.3	6.5	6.7	V
			VBUS_OVP[1:0] = 10	10.27	10.5	10.73	
			VBUS_OVP[1:0] = 01	13.75	14	14.25	
			VBUS_OVP[1:0] = 00	18.2	18.5	18.8	
VBUS Over-Voltage Falling Threshold	$V_{VBUS\_OV\_FALL}$	V_{VBUS} falling	VBUS_OVP[1:0] = 11	5.8	6	6.2	V
			VBUS_OVP[1:0] = 10	9.27	9.5	9.73	
			VBUS_OVP[1:0] = 01	12.75	13	13.25	
			VBUS_OVP[1:0] = 00	17.2	17.5	17.8	
Sleep Mode Falling Threshold	V_{SLEEP}	V_{VBUS} - V_{BAT}, V_{VBUS} falling, initial accuracy		10	80	150	mV
Sleep Mode Rising Threshold	V_{SLEEPZ}	V_{VBUS} - V_{BAT}, V_{VBUS} rising, initial accuracy		150	240	330	mV
BAT Voltage to Turn On I²C, Turn On BATFET, No VBUS	V_{BAT_UVLOZ}	V_{BAT} rising		2.1	2.35	2.6	V
BAT Voltage to Turn Off I²C, Turn Off BATFET, No VBUS	V_{BAT_UVLO}	V_{BAT} falling	VBAT_UVLO = 0	1.9	2.15	2.4	V
			VBAT_UVLO = 1	1.76	2	2.22	
BAT Voltage Rising Threshold to Enable OTG Mode (1)	V_{BAT_OTG}	V_{BAT} rising	VBAT_OTG_MIN = 0	2.88	3	3.1	V
			VBAT_OTG_MIN = 1	2.48	2.6	2.7	
BAT Voltage Falling Threshold to Disable OTG Mode	V_{BAT_OTGZ}	V_{BAT} falling	VBAT_OTG_MIN = 0	2.7	2.8	2.9	V
			VBAT_OTG_MIN = 1	2.3	2.4	2.5	
Bad Adaptor Detection Threshold	V_{BAD_SRC}	V_{VBUS} falling		3.52	3.67	3.82	V
Bad Adaptor Detection Current Source	I_{BAD_SRC}	VBUS_SINK_DIS = 0			10		mA

NOTE:

1. The SGM41551 can enter OTG mode when V_{BAT} > V_{BAT_OTG} and V_{REGN} > $V_{REGN\_OK\_RISE}$.

ELECTRICAL CHARACTERISTICS (continued)

(V_{VBUS_UVLOZ} < V_{VBUS} < V_{VBUS_OV}, T_J = -40℃ to +85℃, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Power Path Management							
System Regulation Voltage	V_{SYS}	I_{SYS} = 0A, V_{BAT} > V_{SYSMIN}, charge disabled, offset above V_{BAT}			50		mV
		I_{SYS} = 0A, V_{BAT} < V_{SYSMIN}, charge disabled, offset above V_{SYSMIN}			250		
VSYSMIN Register Range	V_{SYSMIN_RNG}			2.56		3.84	V
VSYSMIN Register Step Size	$V_{SYSMIN\_REG\_STEP}$				80		mV
Minimum DC System Voltage Output	$V_{SYSMIN\_REG\_ACC}$	I_{SYS} = 0A, V_{BAT} < V_{SYSMIN} = 3.52V, charge disabled		3.52	3.77		V
System Short Falling Threshold	V_{SYS_SHORT}				1.7		V
System Short Rising Threshold	V_{SYS_SHORTZ}				2		V
Battery Charger							
Charge Voltage Program Range	$V_{BAT\_REG\_RANGE}$			3.5		4.8	V
Charge Voltage Step	$V_{BAT\_REG\_STEP}$				10		mV
Charge Voltage Setting Accuracy	$V_{BAT\_REG\_ACC}$	VREG[8:0] = 4.2V	T_J = +25℃	-0.3		0.3	%
			T_J = -40℃ to +85℃	-0.5		0.5	
Charge Current Regulation Range	$I_{CHG\_REG\_RANGE}$			0.04		3.52	A
Charge Current Regulation Step	$I_{CHG\_REG\_STEP}$				40		mA
Charge Current Regulation Accuracy	$I_{CHG\_REG\_ACC}$	V_{BAT} = 3.2V	ICHG[6:0] = 320mA	-15		16	%
			ICHG[6:0] = 1040mA	-8		8	
			ICHG[6:0] = 1760mA	-5		5	
		V_{BAT} = 4.0V	ICHG[6:0] = 320mA	-7		7.5	
			ICHG[6:0] = 1040mA	-4.8		4.8	
			ICHG[6:0] = 1760mA	-5		5	
Pre-Charge Current Range	I_{PRECHG_RANGE}			20		620	mA
Pre-Charge Current Step	I_{PRECHG_STEP}				20		mA
Pre-Charge Current	I_{PRECHG}	V_{BAT} = 2.5V	IPRECHG[5:0] = 100mA	75	100	128	mA
			IPRECHG[5:0] = 200mA	155	200	245	
			IPRECHG[5:0] = 500mA	430	500	570	
Termination Current Regulation Setting	I_{TERM_RANGE}			10		620	mA
Termination Current Step	I_{TERM_STEP}				10		mA
Termination Current	I_{TERM}	ITERM[6:0] = 20mA		9	20	36	mA
		ITERM[6:0] = 100mA		78	100	130	
		ITERM[6:0] = 300mA		260	300	340	
Battery Low Falling Threshold	$V_{BATLOWV\_FALL}$	Change from fast charging to pre-charge (BATLOWV = 1)		2.69	2.82	2.95	V
Battery Low Rising Threshold	$V_{BATLOWV\_RISE}$	Change from pre-charge to fast charging (BATLOWV = 1)		2.9	3	3.1	V
Battery Short Voltage	V_{SHORT}	V_{BAT} falling	VBAT_UVLO = 0		2.05		V
			VBAT_UVLO = 1		1.85		
	V_{SHORTZ}	V_{BAT} rising			2.25		
Battery Short Current	I_{SHORT}	V_{BAT} < V_{SHORTZ}	ITRICKLE = 0	7	18	29	mA
			ITRICKLE = 1	55	80	105	
Recharge Threshold below V_{BAT_REG}	V_{RECHG}	V_{BAT} falling	VRECHG = 0		100		mV
			VRECHG = 1		200		

ELECTRICAL CHARACTERISTICS (continued)

(V_{VBUS_UVLOZ} < V_{VBUS} < V_{VBUS_OV}, T_J = -40℃ to +85℃, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Battery Charger							
PMID Discharge Load Current	I_{PMID_LOAD}			13	27		mA
Battery Discharge Load Current	I_{BAT_LOAD}			10	22		mA
System Discharge Load Current	I_{SYS_LOAD}			13	22		mA
BATFET							
BATFET MOSFET On-Resistance	R_{ON_BATFET}	Measured from BAT pin to SYS pin			18	31	mΩ
Battery Protections							
Battery Over-Voltage Rising Threshold	V_{BAT_OVP}	As percentage of V_{BAT_REG}		102.7	104	105.1	%
Battery Over-Voltage Falling Threshold	V_{BAT_OVPZ}	As percentage of V_{BAT_REG}		100.7	102	103.5	%
Battery Discharging Peak Current Rising Threshold	I_{BAT_PK}	IBAT_PK[1:0] = 00		1.5			A
		IBAT_PK[1:0] = 01		3			
		IBAT_PK[1:0] = 10		6			
		IBAT_PK[1:0] = 11		12			
Input Voltage and Current Regulation (DPM: Dynamic Power Management)							
Input Voltage Regulation Limit	V_{INDPM_RANGE}			3.8		16.8	V
Input Voltage Regulation Step	V_{INDPM_STEP}				40		mV
Input Voltage Regulation Accuracy	V_{INDPM_ACC}	VINDPM[8:0] = 4.6V		-1.5		1.5	%
		VINDPM[8:0] = 8V		-1.5		1.5	
		VINDPM[8:0] = 16V		-1.5		1.5	
Input Voltage Regulation Limit Tracking V_{BAT}	$V_{INDPM\_BAT\_TRACK}$	V_{BAT} = 4.1V, VINDPM[8:0] = 4V, VINDPM_BAT_TRACK = 1		4.12	4.3	4.44	V
Input Current Regulation Limit	I_{INDPM_RANGE}			0.1		3.2	A
Input Current Regulation Step	I_{INDPM_STEP}				20		mA
Input Current Regulation	I_{INDPM}	V_{VBUS} = 5V	IINDPM[7:0] = 500mA	450	475	500	mA
			IINDPM[7:0] = 900mA	805	855	900	
			IINDPM[7:0] = 1500mA	1350	1425	1500	
D+/D- Detection							
D+/D- Voltage Source (600mV)	$V_{D+D-\_0p6V\_SRC}$	1mA load on D+/D-		550	600	650	mV
Leakage Current into D+/D-	I_{D+D-_LKG}	HIZ mode		-1		1	μA
D+/D- Comparator Threshold for Non-Standard Adaptor	V_{D+D-_2p8}			2.6		2.85	V
	V_{D+D-_2p0}			1.875		2.125	
Thermal Regulation and Thermal Shutdown							
Junction Temperature Regulation Threshold	$T_{JUNCTION\_REG}$	Temperature increasing	TREG = 1		120		℃
			TREG = 0		60		
Thermal Shutdown Rising Temperature	T_{SHUT}	Temperature increasing			140		℃
Thermal Shutdown Hysteresis	T_{SHUT_HYS}	Temperature decreasing by T_{SHUT_HYS}			30		℃

ELECTRICAL CHARACTERISTICS (continued)

(V_{VBUS_UVLOZ} < V_{VBUS} < V_{VBUS_OV}, T_J = -40℃ to +85℃, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Thermistor Comparators (Charge Mode)						
TS Pin Rising Voltage Threshold for TH1 Comparator to Transition from TS_COOL to TS_COLD, Charge Suspended above This Voltage	V_{TS_COLD}	As percentage to TS pin bias reference (-5℃ w/ 103AT), TS_TH1_TH2_TH3[2:0] = 100, 101, 110	75.1	75.6	76.1	%
		As percentage to TS pin bias reference (0℃ w/ 103AT), fixed JEITA threshold or TS_TH1_TH2_TH3[2:0] = 000, 001, 010, 011, 111	72.9	73.4	73.9	
TS Pin Falling Voltage Threshold for TH1 Comparator to Transition from TS_COLD to TS_COOL, TS_COOL Charge Settings Resume below This Voltage	V_{TS_COLDZ}	As percentage to TS pin bias reference (-2.5℃ w/ 103AT), TS_TH1_TH2_TH3[2:0] = 100, 101, 110	73.9	74.4	74.9	%
		As percentage to TS pin bias reference (2.5℃ w/ 103AT), fixed JEITA threshold or TS_TH1_TH2_TH3[2:0] = 000, 001, 010, 011, 111	71.8	72.3	72.8	
TS Pin Rising Voltage Threshold for TH2 Comparator to Transition from TS_PRECOOL to TS_COOL, TS_COOL Charging Settings Used above This Voltage	V_{TS_COOL}	As percentage to TS pin bias reference (5℃ w/ 103AT), TS_ISET_COOL[1:0] = 00 or TS_TH1_TH2_TH3[2:0] = 000, 100	70.6	71.1	71.6	%
		As percentage to TS pin bias reference (10℃ w/ 103AT), TS_ISET_COOL[1:0] = 01 or TS_TH1_TH2_TH3[2:0] = 001, 101, 110, 111	68	68.5	69	
		As percentage to TS pin bias reference (15℃ w/ 103AT), TS_ISET_COOL[1:0] = 10 or TS_TH1_TH2_TH3[2:0] = 010	65	65.5	66	
		As percentage to TS pin bias reference (20℃ w/ 103AT), TS_ISET_COOL[1:0] = 11 or TS_TH1_TH2_TH3[2:0] = 011	62	62.5	63	
TS Pin Falling Voltage Threshold for TH2 Comparator to Transition from TS_COOL to TS_PRECOOL, TS_PRECOOL Charging Settings Resume below This Voltage	V_{TS_COOLZ}	As percentage to TS pin bias reference (7.5℃ w/ 103AT), TS_ISET_COOL[1:0] = 00 or TS_TH1_TH2_TH3[2:0] = 000, 100	69.3	69.8	70.3	%
		As percentage to TS pin bias reference (12.5℃ w/ 103AT), TS_ISET_COOL[1:0] = 01 or TS_TH1_TH2_TH3[2:0] = 001, 101, 110, 111	66.5	67	67.5	
		As percentage to TS pin bias reference (17.5℃ w/ 103AT), TS_ISET_COOL[1:0] = 10 or TS_TH1_TH2_TH3[2:0] = 010	63.6	64.1	64.6	
		As percentage to TS pin bias reference (22.5℃ w/ 103AT), TS_ISET_COOL[1:0] = 11 or TS_TH1_TH2_TH3[2:0] = 011	60.5	61	61.5	
TS Pin Rising Voltage Threshold for TH3 Comparator to Transition from TS_NORMAL to TS_PRECOOL, TS_PRECOOL Charge Settings Used above This Voltage	$V_{TS\_PRECOOL}$	As percentage to TS pin bias reference (15℃ w/ 103AT), TS_TH1_TH2_TH3[2:0] = 000, 001, 100, 101	65	65.5	66	%
		As percentage to TS pin bias reference (20℃ w/ 103AT), TS_TH1_TH2_TH3[2:0] = 010, 011, 110, 111	62	62.5	63	
TS Pin Falling Voltage Threshold for TH3 Comparator To Transition from TS_PRECOOL to TS_NORMAL, Normal Charging Resumes below This Voltage	$V_{TS\_PRECOOLZ}$	As percentage to TS pin bias reference (17.5℃ w/ 103AT), TS_TH1_TH2_TH3[2:0] = 000, 001, 100, 101	63.6	64.1	64.6	%
		As percentage to TS pin bias reference (22.5℃ w/ 103AT), TS_TH1_TH2_TH3[2:0] = 010, 011, 110, 111	60.5	61	61.5	
TS Pin Falling Voltage Threshold for TH4 Comparator to Transition from TS_NORMAL to TS_PREWARM, TS_PREWARM Charging Settings Used below This Voltage	$V_{TS\_PREWARM}$	As percentage to TS pin bias reference (35℃ w/ 103AT), TS_TH4_TH5_TH6[2:0] = 000, 001, 010, 100, 101	51.3	52	52.7	%
		As Percentage to TS pin bias reference (40℃ w/ 103AT), TS_TH4_TH5_TH6[2:0] = 011, 110, 111	47.7	48.4	49.1	
TS Pin Rising Voltage Threshold for TH4 Comparator to Transition from TS_PREWARM to TS_NORMAL, Normal Charging Resumes above This Voltage	$V_{TS\_PREWARMZ}$	As percentage to TS pin bias reference (32.5℃ w/ 103AT), TS_TH4_TH5_TH6[2:0] = 000, 001, 010, 100, 101	53.2	53.9	54.6	%
		As percentage to TS pin bias reference (37.5℃ w/ 103AT), TS_TH4_TH5_TH6[2:0] = 011, 110, 111	49	49.7	50.4	

ELECTRICAL CHARACTERISTICS (continued)

(V_{VBUS_UVLOZ} < V_{VBUS} < V_{VBUS_OV}, T_J = -40℃ to +85℃, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
TS Pin Falling Voltage Threshold for TH5 Comparator to Transition from TS_PREWARM to TS_WARM, TS_WARM Charging Settings Used below This Voltage	V_{TS_WARM}	As percentage to TS pin bias reference (40℃ w/ 103AT), TS_ISET_WARM[1:0] = 00 or TS_TH4_TH5_TH6[2:0] = 000, 100	47.7	48.4	49.1	%
		As percentage to TS pin bias reference (45℃ w/ 103AT), TS_ISET_WARM[1:0] = 01 or TS_TH4_TH5_TH6[2:0] = 001, 101, 110	44.1	44.8	45.5	
		As percentage to TS pin bias reference (50℃ w/ 103AT), TS_ISET_WARM[1:0] = 10 or TS_TH4_TH5_TH6[2:0] = 010, 111	40.5	41.2	41.9	
		As percentage to TS pin bias reference (55℃ w/ 103AT), TS_ISET_WARM[1:0] = 11 or TS_TH4_TH5_TH6[2:0] = 011	37	37.7	38.4	
TS Pin Rising Voltage Threshold for TH5 Comparator to Transition from TS_WARM to TS_PREWARM, TS_PREWARM Charging Settings Resume above This Voltage	V_{TS_WARMZ}	As percentage to TS pin bias reference (37.5℃ w/ 103AT), TS_ISET_WARM[1:0] = 00 or TS_TH4_TH5_TH6[2:0] = 000, 100	49	49.7	50.4	%
		As percentage to TS pin bias reference (42.5℃ w/ 103AT), TS_ISET_WARM[1:0] = 01 or TS_TH4_TH5_TH6[2:0] = 001, 101, 110	45.4	46.1	46.8	
		As percentage to TS pin bias reference (47.5℃ w/ 103AT), TS_ISET_WARM[1:0] = 10 or TS_TH4_TH5_TH6[2:0] = 010, 111	41.8	42.5	43.2	
		As percentage to TS pin bias reference (52.5℃ w/ 103AT), TS_ISET_WARM[1:0] = 11 or TS_TH4_TH5_TH6[2:0] = 011	38.4	39.1	39.8	
TS Pin Falling Voltage Threshold for TH6 Comparator to Transition from TS_WARM to TS_HOT, Charging is Suspended below This Voltage	V_{TS_HOT}	As Percentage to TS pin bias reference (50℃ w/ 103AT), TS_TH4_TH5_TH6[2:0] = 100 or 101	40.5	41.2	41.9	%
		As percentage to TS pin bias reference (60℃ w/ 103AT), fixed JEITA threshold or TS_TH4_TH5_TH6[2:0] = 000, 001, 010, 011, 110 or 111	33.7	34.4	35.1	
TS Pin Rising Voltage Threshold for TH6 Comparator to Transition from TS_HOT to TS_WARM, TS_WARM Charging Settings Resume above This Voltage	V_{TS_HOTZ}	As percentage to TS pin bias reference (47.5℃ w/ 103AT), TS_TH4_TH5_TH6[2:0] = 100 or 101	41.8	42.5	43.2	%
		As percentage to TS pin bias reference (57.5℃ w/ 103AT), fixed JEITA threshold or TS_TH4_TH5_TH6[2:0] = 000, 001, 010, 011, 110 or 111	35.1	35.8	36.5	
Thermistor Comparators (OTG Mode)						
TS Pin Rising Voltage Threshold to Transition from TS_OTG_NORMAL to TS_OTG_COLD, OTG Suspended above This Voltage	$V_{TS\_OTG\_COLD}$	As percentage to TS pin bias reference (-20℃ w/ 103AT), TS_TH_OTG_COLD = 0	79.6	80.1	80.6	%
		As percentage to TS pin bias reference (-10℃ w/ 103AT), TS_TH_OTG_COLD = 1	76.7	77.2	77.7	
TS Pin Falling Voltage Threshold to Transition from TS_OTG_COLD to TS_OTG_NORMAL, OTG Resumes below This Voltage	$V_{TS\_OTG\_COLDZ}$	As percentage to TS pin bias reference (-15℃ w/ 103AT), TS_TH_OTG_COLD = 0	78.3	78.8	79.3	%
		As percentage to TS pin bias reference (-5℃ w/ 103AT), TS_TH_OTG_COLD = 1	75.1	75.6	76.1	
TS Pin Falling Voltage Threshold to Transition from TS_OTG_NORMAL to TS_OTG_HOT, OTG Suspended below This Voltage	$V_{TS\_OTG\_HOT}$	As percentage to TS pin bias reference (55℃ w/ 103AT), TS_TH_OTG_HOT[1:0] = 00	36.9	37.6	38.3	%
		As percentage to TS pin bias reference (60℃ w/ 103AT), TS_TH_OTG_HOT[1:0] = 01	33.6	34.3	35	
		As percentage to TS pin bias reference (65℃ w/ 103AT), TS_TH_OTG_HOT[1:0] = 10	30.5	31.2	31.9	
TS Pin Rising Voltage Threshold to Transition from TS_OTG_HOT to TS_OTG_NORMAL, OTG Resumes above This Threshold	$V_{TS\_OTG\_HOTZ}$	As percentage to TS pin bias reference (52.5℃ w/ 103AT), TS_TH_OTG_HOT[1:0] = 00	38.3	39.0	39.7	%
		As percentage to TS pin bias reference (57.5℃ w/ 103AT), TS_TH_OTG_HOT[1:0] = 01	35	35.7	36.4	
		As percentage to TS pin bias reference (62.5℃ w/ 103AT), TS_TH_OTG_HOT[1:0] = 10	31.7	32.5	33.2	

ELECTRICAL CHARACTERISTICS (continued)

(V_{VBUS_UVLOZ} < V_{VBUS} < V_{VBUS_OV}, T_J = -40℃ to +85℃, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
PWM						
PWM Switching Frequency	f_{SW}	Oscillator frequency	1.34	1.5	1.66	MHz
MOSFET Turn-On Resistance						
Top Reverse Blocking MOSFET On-Resistance between VBUS and PMID - Q1	R_{ON_RBFET}			24	36	mΩ
Top Switching MOSFET On-Resistance between PMID and SW - Q2	R_{ON_HSFET}			56	80	mΩ
Bottom Switching MOSFET On-Resistance between SW and GND - Q3	R_{ON_LSFET}			60	90	mΩ
OTG Mode Converter						
Typical OTG Mode Voltage Regulation Range	V_{OTG_RANGE}		3.84		9.6	V
Typical OTG Mode Voltage Regulation Step	V_{OTG_STEP}			80		mV
OTG Mode Voltage Regulation Accuracy	V_{OTG_ACC}	I_{VBUS} = 0A, VOTG[6:0] = 9.04V	-2		2	%
		I_{VBUS} = 0A, VOTG[6:0] = 5.04V	-2.5		2.5	
Typical OTG Mode Current Regulation Range	I_{OTG_RANGE}		0.1		2.0	A
Typical OTG Mode Current Regulation Step	I_{OTG_STEP}			20		mA
OTG Mode Current Regulation	I_{OTG}	IOTG[7:0] = 0.5A	445	525	615	mA
		IOTG[7:0] = 1.5A	1465	1575	1705	
		IOTG[7:0] = 1.8A	1750	1890	2040	
OTG Mode Under-Voltage Falling Threshold at PMID	V_{OTG_UVP}			3.2		V
OTG Mode Over-Voltage Rising Threshold at VBUS	$V_{OTG\_VBUS\_OVP}$	OTG_OVP = 0	10.25	10.55	10.85	V
		OTG_OVP = 1	5.75	6	6.25	
REGN LDO						
REGN LDO Output Voltage	V_{REGN}	V_{VBUS} = 5V, I_{REGN} = 20mA	4.35	4.6		V
		V_{VBUS} = 9V, I_{REGN} = 20mA	4.43	5	5.53	V
REGN Not Good Falling Threshold	V_{REGNZ_OK}	Forward mode		2.75		V
		OTG mode		1.85		
REGN LDO Current Limit	I_{REGN_LIM}	V_{VBUS} = 5V, V_{REGN} = 4.3V	28			mA
ADC Measurement Accuracy and Performance						
Conversion Time, Each Measurement	t_{ADC_CONV}	ADC_SAMPLE[1:0] = 00		24		ms
		ADC_SAMPLE[1:0] = 01		12		
		ADC_SAMPLE[1:0] = 10		6		
		ADC_SAMPLE[1:0] = 11		3		
Effective Resolution	ADC_{RES}	ADC_SAMPLE[1:0] = 00	11	12		bits
		ADC_SAMPLE[1:0] = 01	10	11		
		ADC_SAMPLE[1:0] = 10	9	10		
		ADC_SAMPLE[1:0] = 11	8	9		

ELECTRICAL CHARACTERISTICS (continued)

(V_{VBUS_UVLOZ} < V_{VBUS} < V_{VBUS_OV}, T_J = -40℃ to +85℃, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER		SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ADC Measurement Range and LSB							
ADC Bus Current Reading (both Forward and OTG)		IBUS_ADC	Range	-4		4	A
			LSB		2		mA
ADC VBUS Voltage Reading		VBUS_ADC	Range	0		20	V
			LSB		4		mV
ADC PMID Voltage Reading		VPMID_ADC	Range	0		20	V
			LSB		4		mV
ADC BAT Voltage Reading		VBAT_ADC	Range	0		5.6	V
			LSB		2		mV
ADC SYS Voltage Reading		VSYS_ADC	Range	0		5.6	V
			LSB		2		mV
ADC BAT Current Reading		IBAT_ADC	Range	-7.5		4	A
			LSB		4		mA
ADC TS Voltage Reading		TS_ADC	Range as a percent of REGN (-40℃ to +85℃ for 103AT)	0		98.567	%
ADC TS Voltage Reading			LSB		0.09635		%
ADC Die Temperature Reading		TDIE_ADC	Range	-40		150	℃
			LSB		0.5		℃
I²C Interface (SCL, SDA)							
Input High Threshold Level, SDA and SCL		V_{IH}		0.78			V
Input Low Threshold Level, SDA and SCL		V_{IL}				0.4	V
Output Low Threshold Level		V_{OL_SDA}	Sink current = 5mA, 1.2V VDD			0.2	V
High-Level Leakage Current		I_{BIAS}	Pull up rail 1.2V			1	μA
Capacitive Load for Each Bus Line		C_{BUS}				400	pF
Logic Output Pin (nINT, nPG, STAT)							
Output Low Threshold Level		V_{OL}	Sink current = 5mA			0.2	V
High-Level Leakage Current		I_{OUT_BIAS}	Pull up rail 1.2V			1	μA
Logic Input Pin (nCE, nQON)							
Input Low Threshold	nCE	V_{IL}				0.4	V
Input High Threshold		V_{IH}		0.78			V
High-Level Leakage Current		$I_{IN\_BIAS\_CE}$	Pull up rail 1.2V			1	μA
Input Low Threshold	nQON	V_{IL}				0.4	V
Input High Threshold		V_{IH}		1.22			V
Internal nQON Pull-Up		V_{QON}	Battery only mode		V_{BAT} - 0.7		V
			V_{VBUS} = 9V		4.3		
			V_{VBUS} = 5V		4.3		
Internal nQON Pull-Up Resistance		R_{QON}			250		kΩ

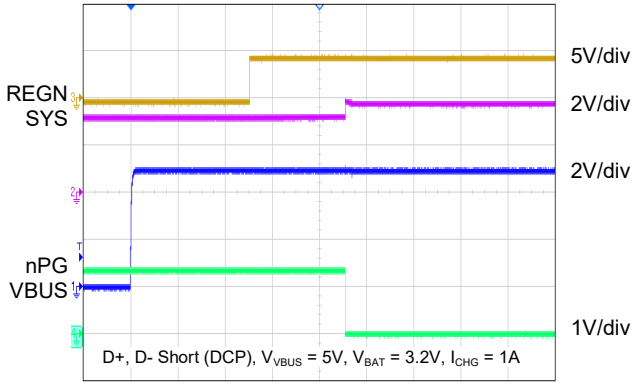
TIMING REQUIREMENTS

(V_{VBUS_UVLOZ} < V_{VBUS} < V_{VBUS_OV}, T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{VBUS}/V_{BAT} Power-Up						
VBUS_OVP Propagation Delay to Stop Converter, VBUS Rising (No Deglitch)	$t_{VBUS\_OVP\_PROP}$			130		ns
VBUS OVP Deglitch Time to Set VBUS_FAULT_STAT and VBUS_FAULT_FLAG	t_{VBUS_OVP}			112		μs
Wait Window for Bad Adaptor Detection	t_{BAD_SRC}			30		ms
Bad Adaptor Detection Retry Wait Time	t_{BAD_RETRY}			2		s
Battery Charger						
Deglitch Time for Charge Termination	t_{TERM_DGL}	ITERM_TIMER = 0		230		ms
Deglitch Time for Recharge	t_{RECHG_DGL}	V_{BAT} falling		22.5		ms
Charge Safety Timer in Trickle Charge	t_{SAFETY_TRKCHG}		0.96	1.12	1.3	h
Charge Safety Timer in Pre-Charge	t_{SAFETY_PRECHG}	PRECHG_TMR = 0	1.79	2	2.28	h
		PRECHG_TMR = 1	0.4	0.52	0.65	
Typical Charge Safety Timer Range	t_{SAFETY}	CHG_TMR = 0	11.4	12.5	13.7	h
		CHG_TMR = 1	21.8	23.8	26	
Typical Top-Off Timer Range	t_{TOP_OFF}	TOPOFF_TMR[1:0] = 01	14.4	16.2	18.3	min
		TOPOFF_TMR[1:0] = 10	30	34	38	
		TOPOFF_TMR[1:0] = 11	47	52	57	
BATFET Control						
Time after Writing to BATFET_CTRL before BATFET Turned Off for Ship Mode or Shutdown	t_{BATFET_DLY}	BATFET_DLY = 1		10		s
		BATFET_DLY = 0		20		ms
nQON Low Time to Reset BATFET	t_{QON_RST}		5.6	9.4	13.8	s
BATFET Off Time during Full System Reset	t_{BATFET_RST}	No VBUS, battery only		300		ms
Wait Delay for Exiting Ship Mode	t_{SM_EXIT}	SM_EXIT = 1	0.5	0.94	1.4	s
		SM_EXIT = 0		120		ms
Digital Clock and Watchdog Timer						
Watchdog Reset Time	t_{WDT}	EN_HIZ = 0, WATCHDOG[1:0] = 11	146	160		s
	t_{LP_WDT}	EN_HIZ = 1, WATCHDOG[1:0] = 11	89	160		
I²C Interface						
SCL Clock Frequency	f_{SCL}				1	MHz

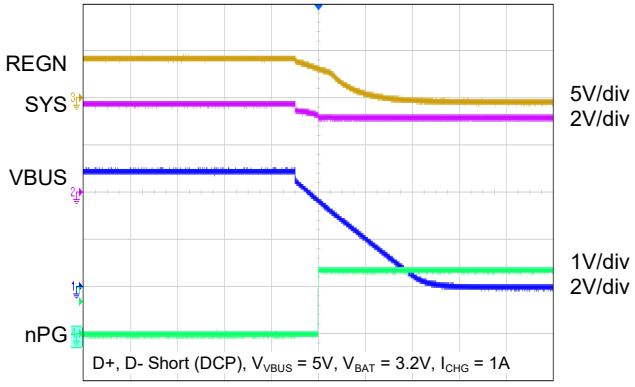
TYPICAL PERFORMANCE CHARACTERISTICS

Power-Up with Charge Enable



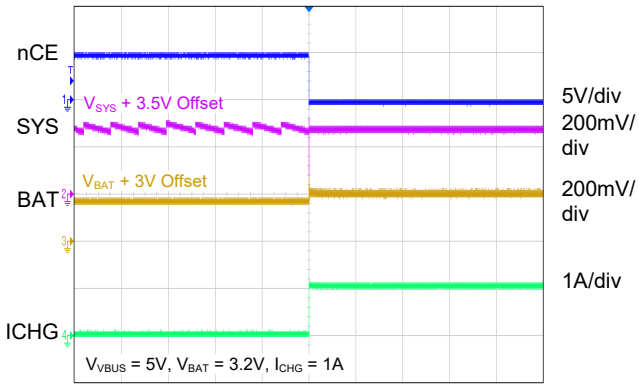
Time (100ms/div)

Power-Down



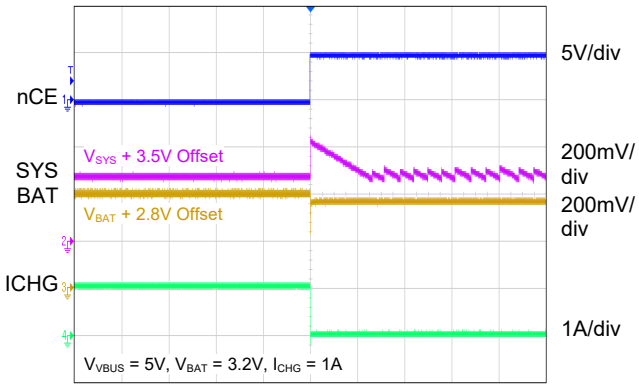
Time (20ms/div)

Charge Enable



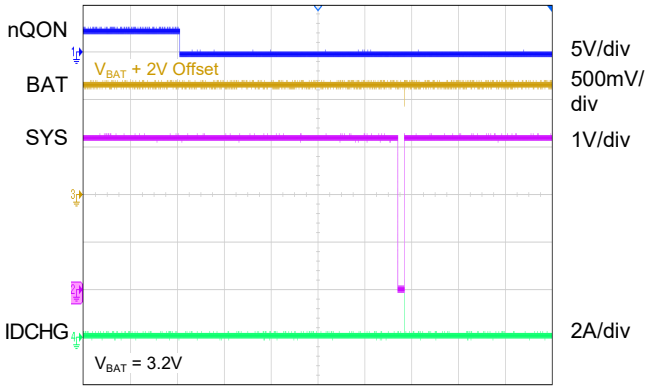
Time (10ms/div)

Charge Disable



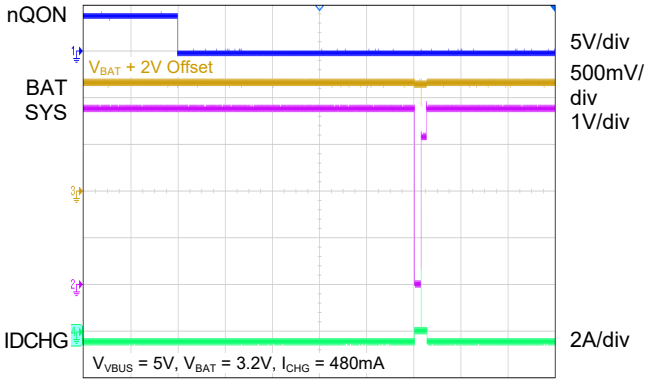
Time (20ms/div)

System Reset by nQON without VBUS Present



Time (2s/div)

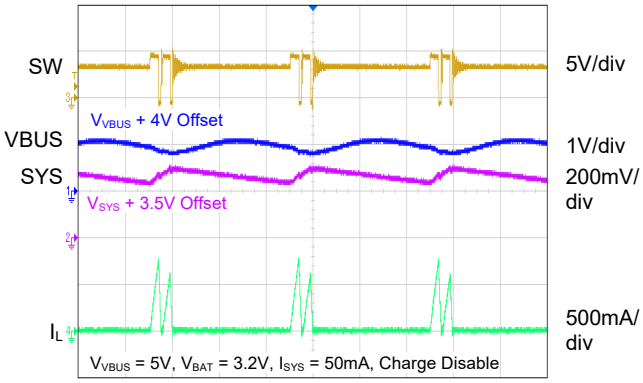
System Reset by nQON with VBUS Present



Time (2s/div)

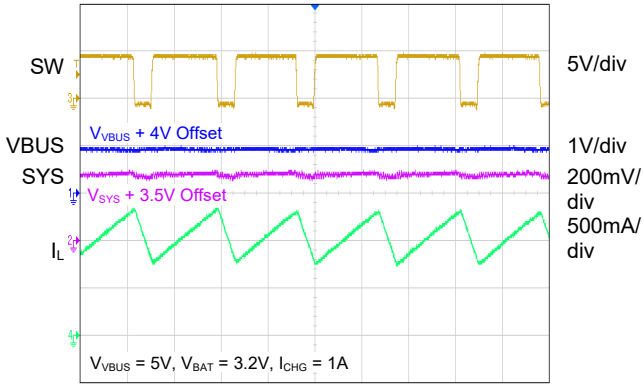
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

PSM Switching in Buck Mode



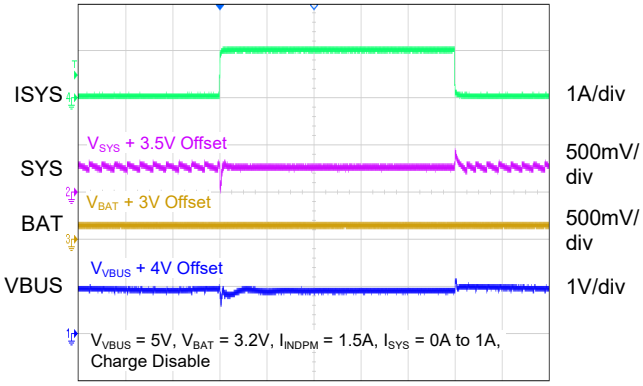
Time (4μs/div)

PWM Switching in Buck Mode



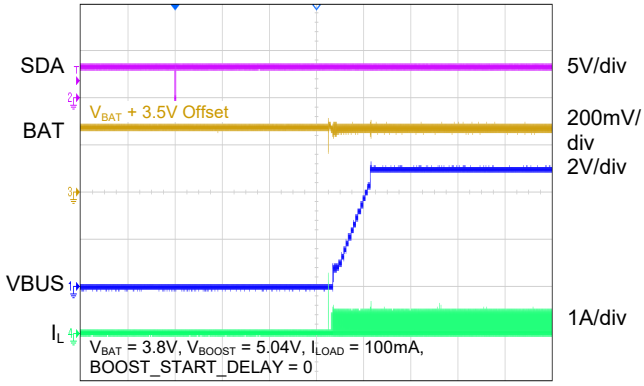
Time (400ns/div)

System Load Transient



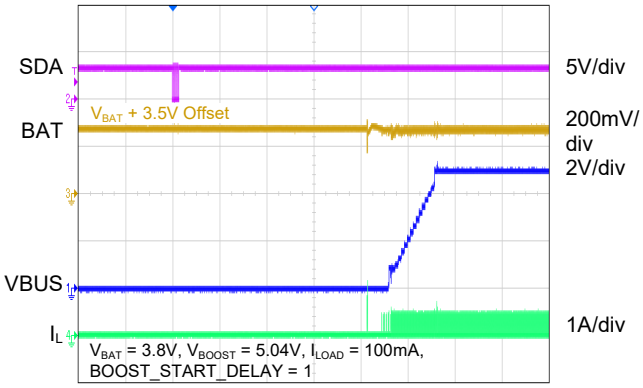
Time (200μs/div)

Boost Mode Power-Up



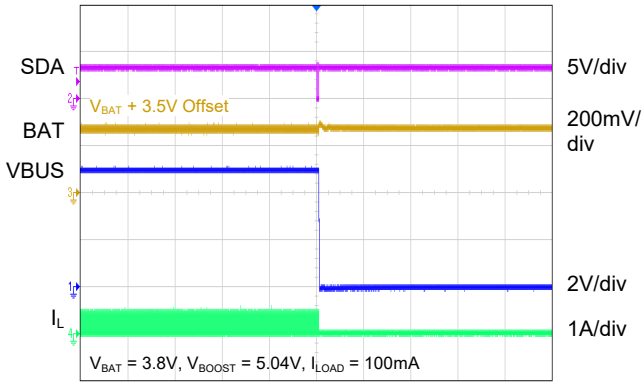
Time (10ms/div)

Boost Mode Power-Up



Time (2ms/div)

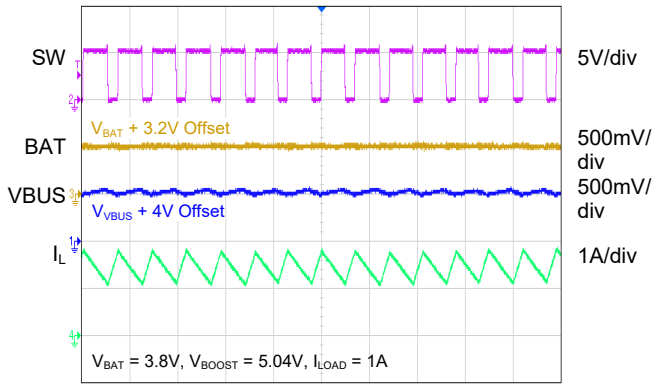
Boost Mode Power-Down



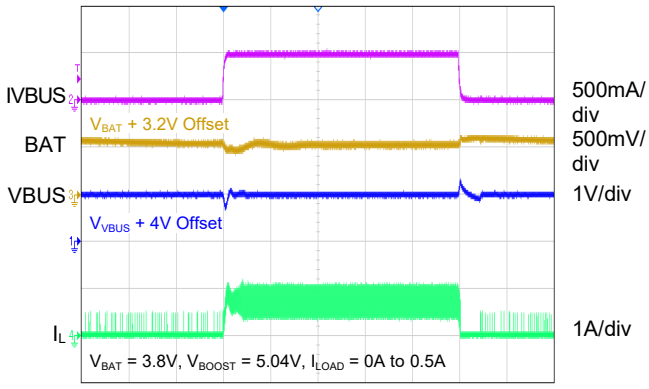
Time (5ms/div)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

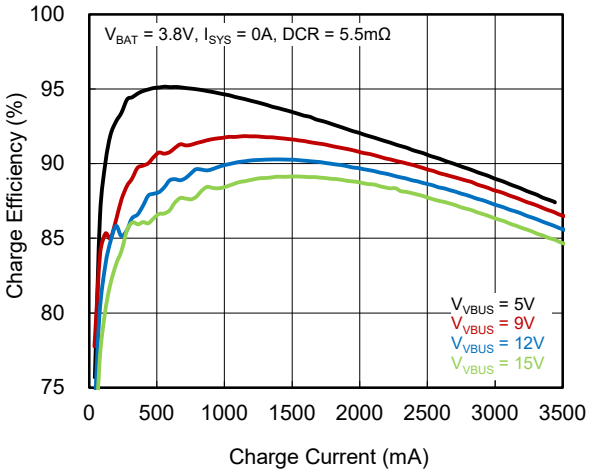
PWM Switching in Boost Mode



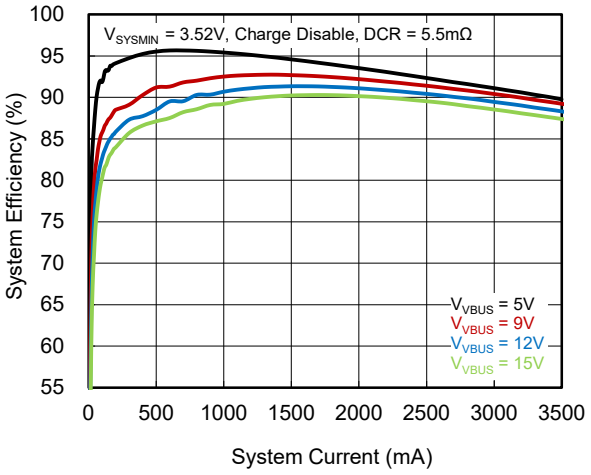
Boost Mode Load Transient



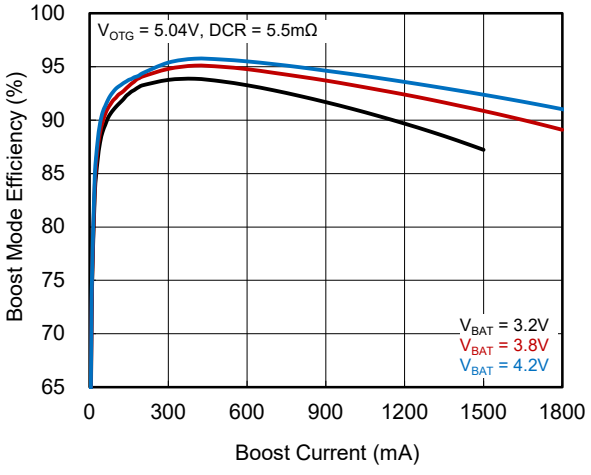
Charge Efficiency vs. Charge Current



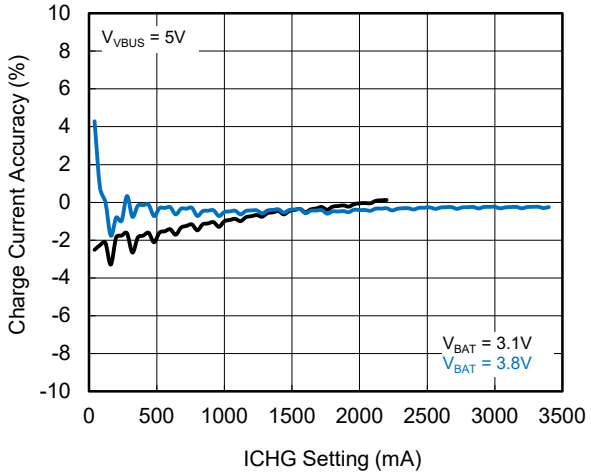
System Efficiency vs. System Current



Boost Mode Efficiency vs. Boost Current

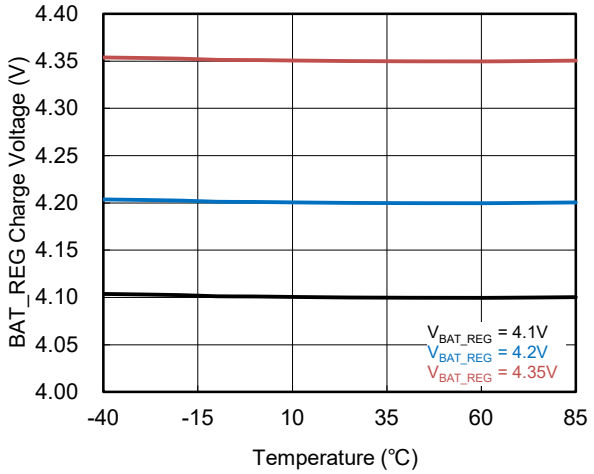


Charge Current Accuracy vs. ICHG Setting

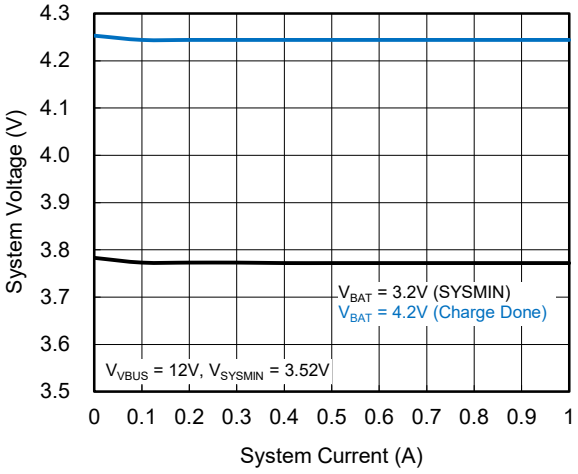


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

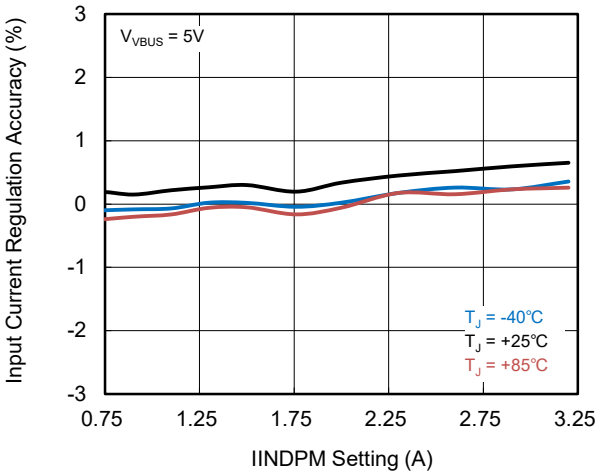
BAT_REG Charge Voltage vs. Temperature



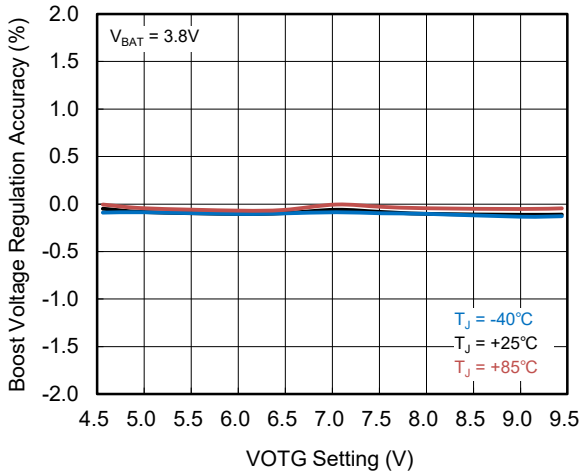
System Load Regulation for SYSMIN and after Charge Done



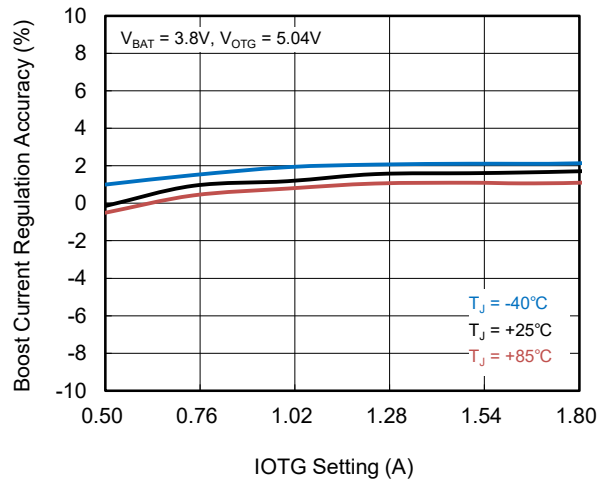
Input Current Regulation Accuracy vs. IINDPM Setting



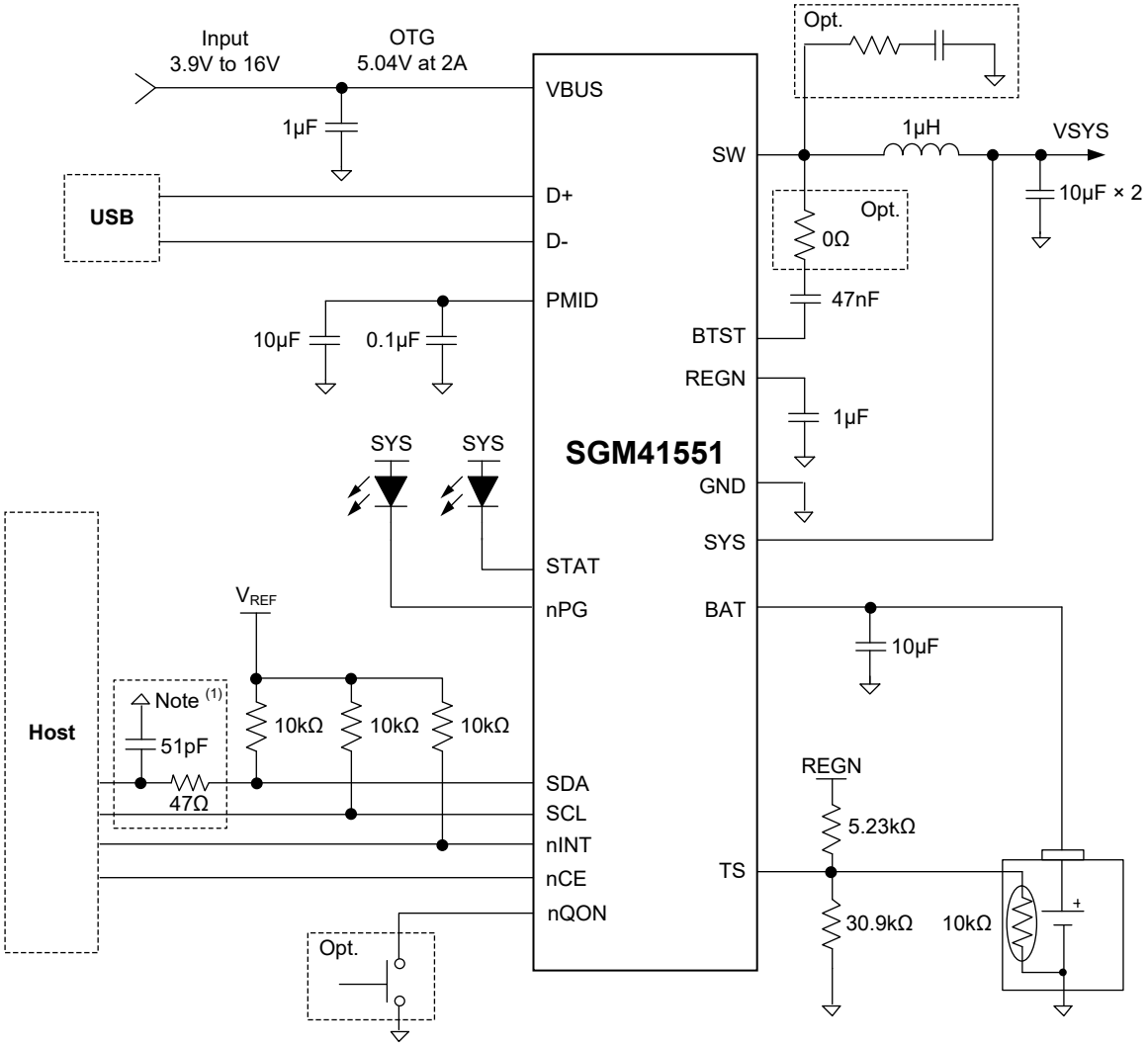
Boost Voltage Regulation vs. VOTG Setting



Boost Current Regulation Accuracy vs. IOTG Setting



TYPICAL APPLICATION CIRCUIT



NOTE:

1. This section is recommended to be added.

Figure 1. Typical Application Circuit

FUNCTIONAL BLOCK DIAGRAM

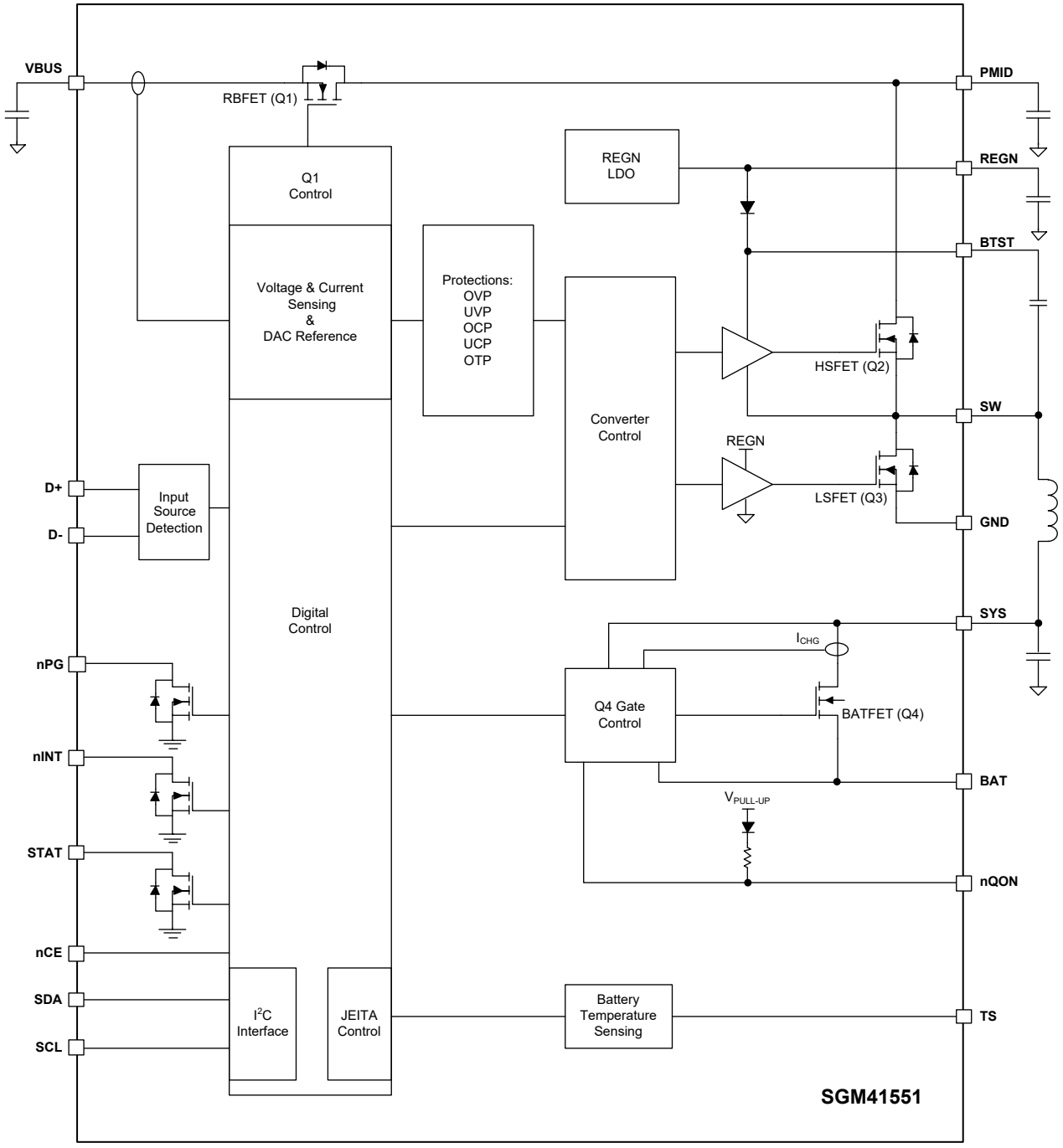


Figure 2. Block Diagram

DETAILED DESCRIPTION

The SGM41551 is a power management and charger device for applications such as cell phones and tablets that use high capacity single-cell Li-Ion or Li-polymer batteries. The SGM41551 can accommodate a wide range of input sources including USB, wall adaptor and car chargers. It is optimized for 5V input (USB voltage) but is capable of operating with input voltages from 3.9V to 16V. It also supports JEITA profile for battery charging safety at high or low temperatures. Automatic power path selection to power the system (SYS) from the input source (VBUS), battery (BAT) or both is another feature of the device. Battery charge current is programmable and can reach a maximum of 3.52A (charge). In the Boost mode, the battery voltage is boosted to power the VBUS pin (2A MAX) when it is a power receiving node (USB OTG) that is typically regulated to 5.04V.

The device may operate in several different modes:

In HIZ mode, the reverse blocking FET (Q1), internal REGN LDO, converter switches and some other parts of the internal circuit remain off to save the battery while it supplies DC power to the system through BATFET.

In the sleep mode, the switching is stopped. The charger goes to the sleep mode when the input source voltage (V_{VBUS}) is not high enough for charging the battery. In other words, V_{VBUS} is smaller than V_{BAT} + V_{SLEEP} (where V_{SLEEP} is a small threshold) and Buck converter is not able to charge, even at its maximum duty cycle. The Boost may also go to the sleep mode if similar issue happens in the reverse direction (when V_{VBUS} is almost equal to or smaller than V_{BAT}).

In supplement mode, the input source power is not enough to supply system demanded power and the battery assists by discharging to the system in parallel and providing the deficit.

Power-On Reset (POR)

The internal circuit of the device is powered from the greater voltage between V_{VBUS} and V_{BAT}. When the voltage of the selected source goes above its UVLO level (V_{VBUS} > V_{VBUS_UVLOZ} or V_{BAT} > V_{BAT_UVLOZ}), a POR happens and activates the sleep comparator, battery depletion comparator and BATFET driver. Upon activation, the I²C interface will also be ready for communication and all registers reset to their default values.

Power-Up from Battery Only (No Input Source)

When only the battery is presented as a source and its voltage is above depletion threshold (V_{BAT_UVLOZ}), the BATFET turns on and connects the battery to the system. The quiescent current is minimum because the REGN LDO remains off. Conduction losses are also low due to small R_{DSON} of BATFET. Low losses help to extend the battery run time.

Power-Up Process from the Input Power Source

Upon connection of an input source (VBUS), its voltage sensed from VBUS pin is checked to turn on the internal REGN LDO regulator and the bias circuits (whether the battery is present or not). The input current limit is determined and set before the Buck converter is started. The sequences of actions when VBUS as input source is powered up are:

1. REGN LDO power-up.
2. Poor power source detection (qualification).
3. Input power source type detection. (Based on D+/D- input. It is used to set the default input current limit (IINDPM[7:0]).)
4. Setting of the input voltage limit threshold (VINDPM threshold).
5. DC/DC converter power-up.

Details of the power-up steps are explained in the following sections.

DETAILED DESCRIPTION (continued)

REGN LDO Power-Up

The REGN low dropout regulator powers the internal bias circuits, HSFET and LSFET gate drivers and TS rail (thermistor pin). The STAT pin can also be pulled up to REGN. The REGN enables when the following 2 conditions are satisfied and remain valid for a 220ms delay time, otherwise the device stays in high-impedance mode (HIZ) with REGN LDO off.

1. V_{VBUS} > V_{VBUS_UVLOZ}.
2. V_{VBUS} > V_{BAT} + V_{SLEEPZ} (in Buck mode) or V_{VBUS} < V_{BAT} + V_{SLEEP} (in Boost mode).

In HIZ state, the quiescent current drawn from VBUS is very small (I_{VBUS_HIZ}). System is only powered by the battery in HIZ mode.

Poor Power Source Detection (Qualification)

When REGN LDO is powered, the input source (adaptor) is checked for its type and current capacity. To start the Buck converter, the input (VBUS) must meet the following conditions:

1. V_{VBUS} < V_{VBUS_OV}.
2. V_{VBUS} > V_{VBUS_MIN} during t_{BAD_SRC} test period (30ms TYP) in which the I_{BAD_SRC} (10mA TYP) current is pulled from VBUS.

Once these conditions are satisfied, the SGM41551 will proceed to the input source type detection.

If a power source is detected (V_{VBUS} drops below V_{BAD_SRC} during pulling I_{BAD_SRC}) as poor, the SGM41551 waits for t_{BAD_RETRY} and then repeat the poor source qualification routine. The chip automatically sets EN_HIZ =1 and goes to HIZ mode after 7 consecutive failures. The VBUS_STAT[2:0] register bits remain at 000 (not powered from VBUS) and there is no change to VBUS_FLAG.

Input Power Source Type Detection

If the REGN LDO is powered, the adaptor is detected as a good source, and EN_AUTO_INDET bit is set to 1 (POR default), the SGM41551 runs input source detection through D+/D- lines to identify input sources (CDP/SDP/DCP) based on USB Battery Charging Specification 1.2 (BC1.2) and other non-standard adaptors. If DCP is detected, the SGM41551 runs HVDCP detection as long as either EN_9V or EN_12V bit is set to 1. The detection algorithm runs automatically each time if VBUS is plugged in, updating the IINDPM[7:0] register according to Table 2. If the EN_AUTO_INDET bit is set to 0, the detection algorithm will not run and IINDPM remains unchanged. The I²C host can force the detection algorithm to run and update IINDPM register by setting FORCE_INDET bit to 1.

As shown in Figure 3, the standard adaptor that follows USB BC1.2 is able to pass data contact detection (DCD) within 500ms. After the 500ms data contact detection (DCD) timer is expired, a non-standard adaptor detection is automatically applied to configure the input current limit.

The primary detection is used to recognize if input adaptor is SDP. The secondary detection is used to identify the charging port is CDP or DCP.

Some registers and pins are also updated as detailed below:

1. Input current limit register (the value in the IINDPM[7:0]) is changed to set current limit.
2. VBUS_STAT[2:0] register is updated to indicate adaptor input source types.

The input current is always limited by the IINDPM[7:0] register and the limit can be updated by the host if needed.

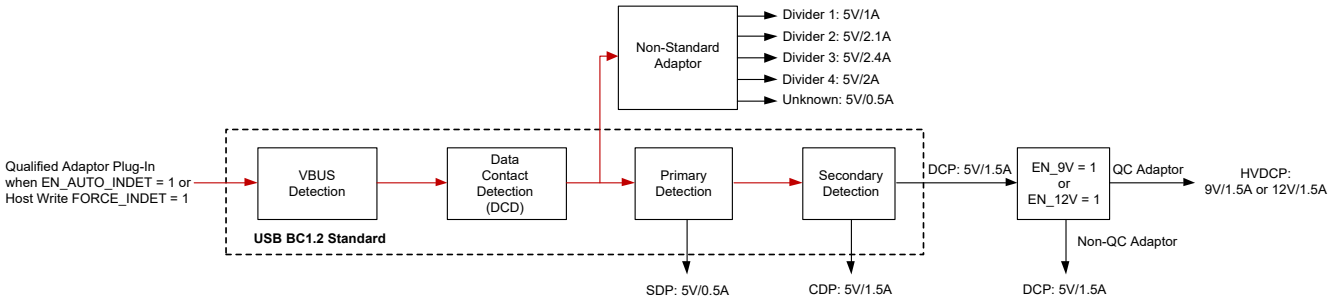


Figure 3. D+/D- Based USB BC1.2 Detection Flow

DETAILED DESCRIPTION (continued)

Input Current Limit by D+/D- Detection

If DCP is detected (VBUS_STAT[2:0] = 011) and EN_DCP_BIAS bit is set to 1, the SGM41551 turns on $V_{D+D-\_0p6V\_SRC}$ on D+ pin. Configuring EN_DCP_BIAS bit to 0 when VBUS_STAT[2:0] = 011 disables the $V_{D+D-\_0p6V\_SRC}$ on D+ pin, and configuring EN_DCP_BIAS bit to 1 when VBUS_STAT[2:0] = 011 enables the $V_{D+D-\_0p6V\_SRC}$ on D+ pin. The EN_HIZ bit has higher priority than EN_DCP_BIAS.

The SGM41551 provides a non-standard detection to identify vendor specific adaptors according to the dividers on the D+/D- pins. Internal comparators of the SGM41551 detect the voltage that applied on D+/D- pin and determine the input current limit based on Table 1.

Setting of the Input Voltage Limit Threshold (VINDPM Threshold)

A wide voltage range (3.8V to 16.8V) is supported for the input voltage limit setting in VINDPM[8:0]. 4.6V is the default for USB.

The device supports dynamic tracking of the battery voltage (VINDPM). The VINDPM_BAT_TRACK bit can be used to enable tracking (0 to disable tracking) and set the tracking offset value. When the tracking is enabled, the input voltage limit will be set to the larger value between the VINDPM[8:0] and V_{BAT} + $V_{INDPM\_BAT\_TRACK}$. The VINDPM_BAT_TRACK tracking offset can be set to 200mV typically.

DC/DC Converter Power-Up

The 1.5MHz switching converter composed of LSFET and HSFET is enabled, which can start switching when the input current limit is set. Converter is initiated with a soft-start when the system voltage is ramped up. Meanwhile, the peak of inductor current is limited to about 1.2A when the system rail is not above V_{SYS_SHORT}.

The BATFET remains on to charge the battery if the battery charging function is enabled, otherwise BATFET turns off.

When converter operates for battery charging, it acts as an efficient, fixed frequency synchronous Buck converter regardless of the input/output voltages and currents. However, it is capable of switching to PSM mode at light load when charging is disabled or when the detected battery voltage is less than minimum system voltage setting. The PSM operation can be enabled or prevented in Buck mode by using the PSM_FWD_DIS bit.

Table 1. Non-Standard Adaptor Detection

Non-Standard Adaptor	D+ Threshold	D- Threshold	Input Current Limit (A)
Divider 1	V_{D+} within V_{D+D-_2p0}	V_{D-} within V_{D+D-_2p8}	1
Divider 2	V_{D+} within V_{D+D-_2p8}	V_{D-} within V_{D+D-_2p0}	2.1
Divider 3	V_{D+} within V_{D+D-_2p8}	V_{D-} within V_{D+D-_2p8}	2.4
Divider 4	V_{D+} within V_{D+D-_1p2}	V_{D-} within V_{D+D-_1p2}	2

Table 2. Input Current Limit Setting from D+/D- Detection

D+/D- Detection	Input Current Limit (I_{INDPM})	VBUS_STAT[2:0]
USB SDP (USB500)	500mA	001
USB CDP	1.5A	010
USB DCP	1.5A	011
Divider 1	1A	101
Divider 2	2.1A	101
Divider 3	2.4A	101
Divider 4	2A	101
HVDCP	1.5A	110
Unknown 5V Adaptor 1	500mA	100

DETAILED DESCRIPTION (continued)

Boost Mode

The SGM41551 supports USB On-The-Go. When a load device is connected to the USB port, the converter can operate as a step-up synchronous converter (Boost mode) with 1.5MHz switching frequency to supply power from the battery to that load. The USB OTG output current limit requirement is achieved by programming. However, the Boost converter can deliver 2A to the output (maximum limit). Converter will be set to Boost mode if about 30ms or 15ms (setting by BOOST_START_DELAY bit) is passed from enabling this mode (EN_OTG bit = 1) and the following conditions are satisfied:

1. $V_{BAT} > V_{BAT\_OTG}$.
2. $V_{VBUS} < V_{BAT} + V_{SLEEP}$ (in sleep mode).
3. Acceptable voltage range at TS pin ($V_{TS\_OTG\_HOT} < V_{TS} < V_{TS\_OTG\_COLD}$).
4. Target voltage of Boost mode (setting by VOTG[6:0] bits) is 200mV greater than battery voltage.

The output voltage is set to V_{VBUS} = 5.04V and is maintained as long as V_{BAT} is above V_{BAT_OTG}. The output current can reach up to the programmed value by IOTG[7:0] bits. The VBUS_STAT[2:0] status register bits are set to 111 in Boost mode (OTG).

Host Mode and Default Mode Operation with Watchdog Timer

After a power-on reset, the device starts in default mode (standalone) with all registers reset as default. If the watchdog timer is expired, the device will also enter default mode with WD_STAT bit set to high. When the host is in sleep mode or there is no host, the device stays in the default mode in which the SGM41551 operates like an autonomous charger. The WD_STAT bit becomes 1 when the charger is in default mode, and becomes 0 when the charger is in host mode. In default mode, the WD_FLAG bit is set to 1, and an nINT pulse is generated to alert the host if WD_MASK = 0. For the first time read, the WD_FLAG bit is set to 1 and then becomes 0 for subsequent reads.

Most of the flexibility features of the SGM41551 become available in the host mode when the device is controlled by a host with I²C. By setting the WD_RST bit to 1, the charger mode changes from default mode to host mode. In this mode, the WD_STAT bit is low and all device parameters can be programmed by the host. To prevent the device watchdog from resetting that results in going back to default mode, the host must disable the watchdog timer by setting WATCHDOG[1:0] = 00, or it must consistently reset the watchdog timer before expiry by writing 1 to WD_RST bit to prevent WD_STAT bit from being set. Every time a 1 is written to the WD_RST bit, the watchdog timer will restart counting. Therefore, it should be reset again before overflow (expiry) to keep the device in the host mode. The device will return to default mode if the watchdog timer expires (WD_STAT bit = 1), and the ICHG value is divided in half and a number of other registers are reset to their default values as shown in the RESET BY column of the register tables in Register Maps section.

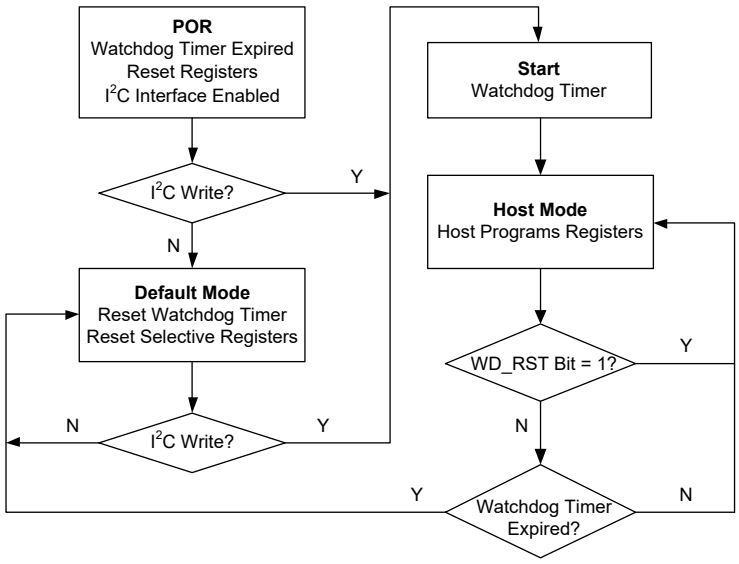


Figure 4. Watchdog Timer Flow Chart

DETAILED DESCRIPTION (continued)

Battery Charging Management

The SGM41551 is designed for charging single-cell Li-Ion or Li-poly batteries with a charge current up to 3.52A (MAX). The battery connection switch (BATFET) is in the charge or discharge current path and features low on-resistance (18mΩ TYP) to allow high efficiency and low voltage drop.

Charging Cycle in Autonomous Mode

Charging is enabled if EN_CHG = 1 and nCE pin is pulled low. In default mode, the SGM41551 runs a charge cycle with the default parameters itemized in Table 3. At any moment, the host can control the charging operations by writing the registers.

Start a New Charging Cycle

If the converter can start switching and all the following conditions are satisfied, a new charge cycle starts:

• NTC temperature fault is not asserted (TS pin).
• Safety timer fault is not asserted.
• BATFET is not forced off. (BATFET_CTRL[1:0] = 00).
• Charging enabled (2 conditions: EN_CHG bit = 1 and nCE pin is low).
• Battery voltage is below the programmed full charge level (V_{BAT_REG}).

A new charge cycle starts automatically if the battery voltage falls below the recharge threshold level (V_{BAT_REG} - 100mV or V_{BAT_REG} - 200mV configured by VRECHG bit). Also, if the charge cycle is completed, a new charging cycle can be initiated by toggling of the nCE pin or EN_CHG bit.

Normally, a charge cycle terminates when the charge voltage is above the recharge threshold level and the charging current falls below the termination threshold if the device is not in thermal regulation or dynamic power management (DPM) mode.

Charge Status Report

The STAT is an open-drain output pin that reports the status of charge and can drive an LED for indication: a low indicates that charging is in progress, a high shows that charging is completed or disabled and alternating low/high (blinking) show a charging fault. The STAT may be disabled (keep the open-drain switch off) by setting STAT_DIS = 1.

The CHG_STAT[1:0] status register reports the present charging phase and status by two bits: 00 = charging disabled or charge terminated, 01 = CC mode (trickle charge, pre-charge or fast charge), 10 = CV mode (taper charge) and 11 = top-off timer active charging.

Battery Charging Profile

The SGM41551 features a full battery charging profile with five phases. In the beginning of the cycle, the battery voltage (V_{BAT}) is tested, and appropriate current and voltage regulation levels are selected as shown in Table 4. Depending on the detected status of the battery, the proper phase is selected to start or for continuation of the charging cycle. The phases are trickle charge (V_{BAT} < 2.25V), pre-charge and fast-charge (constant current and constant voltage).

Note that in the DPM or thermal regulation modes, normal charging functions are temporarily modified: The charge current will be less than the value in the register. The termination is disabled, and the charging safety timer is slowed down by counting at half clock rate.

Table 3. Charging Parameter Default Setting

Part Number	VREG[8:0]	ITRICKLE	IPRECHG[5:0]	ICHG[6:0]	ITERM[6:0]	VRECHG	TOPOFF_TMR[1:0]
SGM41551	4.2V	18mA	100mA	1040mA	60mA	100mV	Disabled

Table 4. Charging Current Setting Based on V_{BAT}

V_{BAT} Voltage	Selected Charging Current	Default Value in the Register	CHG_STAT[1:0]
< 2.25V	I_{SHORT}	18mA	01
2.25V to 3V	I_{PRECHG}	100mA	01
> 3V	I_{CHG}	1.04A	01 or 10

DETAILED DESCRIPTION (continued)

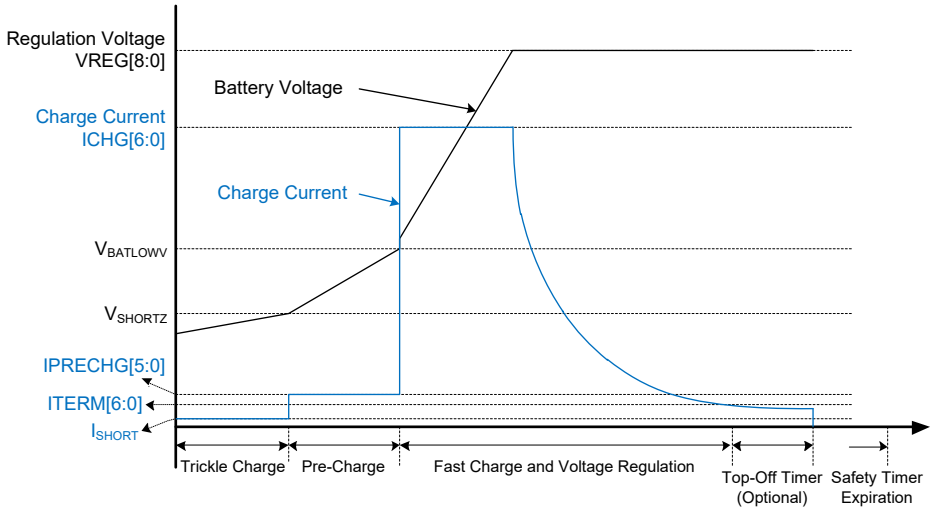


Figure 5. Battery Charging Profile

Charge Termination

A charge cycle is terminated when the battery voltage is higher than the recharge threshold and the charge current falls below the programmed termination current. Unless there is a high power demand for system and it needs to operate in supplement mode, the BATFET turns off at the end of the charge cycle. Even after termination, the Buck converter operates continuously to supply the system.

If the charger is regulating input current, input voltage or junction temperature instead of charge current, termination will be temporarily prevented. The EN_TERM bit is termination control bit and can be set to 0 to disable termination before it happens.

At low termination currents (60mA TYP), the offset in the internal comparator may give rise to a higher (+10mA to +20mA) actual termination current. A delay in termination can be added (optional) as a compensation for comparator offset using a programmable top-off timer. During the delay, constant voltage charge phase continues and gives the falling charge current a chance to drop closer to the programmed value. The top-off delay timer has the same restrictions of the safety timer. As an example, under some conditions, if the safety timer is suspended, the top-off timer will also be suspended or if the safety timer is slowed down, the top-off timer will also be slowed down. Refer to Safety Timer section for the list of conditions. The CHG_STAT[1:0] bits can be read to find status of the termination.

Any of the following events resets the top-off timer:

1. Disable to enable transition of nCE (charge enable).
2. A low to high change in the status of termination.
3. Set REG_RST bit to 1.

The setting of the top-off timer is applied at the time of termination detection and unless a new charge cycle is started, modifying the top-off timer parameters after termination has no effect. When entering top-off timer segment, the CHG_FLAG bit is set to 1, and it is set again if the top-off timer expires.

Temperature Qualification

The charging current and voltage of the battery must be limited when battery is cold or hot. A thermistor input for battery temperature monitoring is included in the device that can protect the battery based on JEITA guidelines.

The TS pin is used to receive the battery temperature, and it is able to be ignored by the charger once TS_IGNORE = 1. If the TS pin input is ignored, the charger will consider the battery temperature to always be valid for charging and OTG modes, and TS_STAT[2:0] bits always report to 000. If TS_IGNORE bit is configured to 1, the TS pin is able to be left floating.

When TS_IGNORE bit is set to 0, the charger changes the charging profile based on the feedback information from TS pin. The TS_STAT[2:0] bits will be updated, if the battery temperature crosses from one temperature range to another, and the charger will also set the flag bit to show it enters a new temperature range. If TS_MASK bit is set to 0, any change to TS_STAT[2:0] bits will generate an nINT pulse including a transition to TS_NORMAL.

DETAILED DESCRIPTION (continued)

Advanced Temperature Profile in Charge Mode

The JEITA guideline was released on April 20, 2007 to improve the safety of charging for Li-Ion batteries. The guideline highlights the importance that avoids high charge current and high charge voltage operation at certain low and high temperature ranges of battery. With the continuous evolution of battery technology, the manufacturers have released wider temperature safety specifications compare with the JEITA standard. The SGM41551 provides a highly flexible temperature-based charging profile, which can meet these advanced specifications as well as remain backwards compatible with the initial JEITA standard. The programmability for charger behavior under different battery temperature regions is shown in Figure 6.

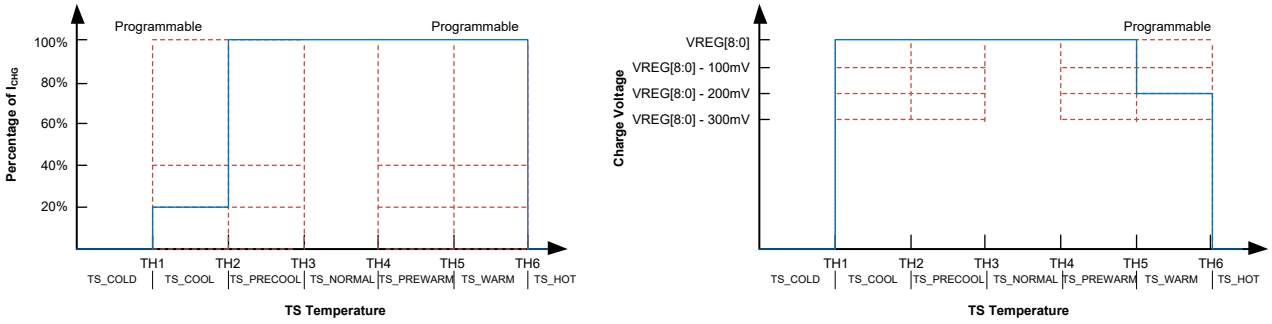


Figure 6. Current and Voltage Settings Based on TS Pin

TS Pin Thermistor Configuration

The typical resistor network for sensing battery temperature is given as shown below.

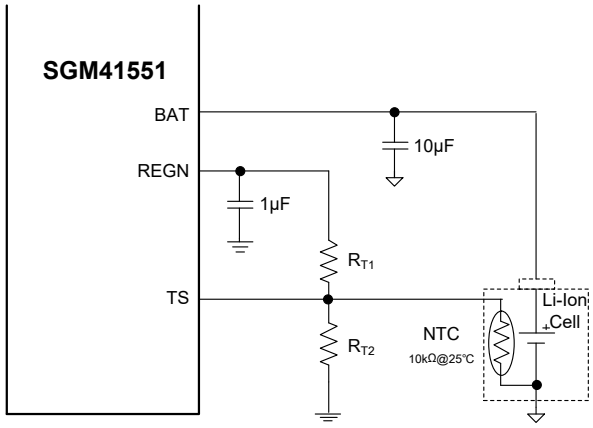


Figure 7. Battery Thermistor Connection and Bias Network

The value of R_{T1} and R_{T2} are determined by the resistance of the thermistor at 0℃ and 60℃ (R_{THCOLD} and R_{THHOT}) and the corresponding voltage thresholds V_{T1} (voltage of TS pin at 0℃) and V_{T4} (Voltage of TS pin at 60℃). For the most accurate thermistor curve matching, it is recommended to use the rising threshold for V_{TS_COLD} at 0℃ and the falling threshold for V_{TS_HOT} at 60℃, regardless of the real configuration for TS_TH1_TH2_TH3[2:0] and TS_TH4_TH5_TH6[2:0] registers.

$$R_{T2} = \frac{R_{THCOLD} \times R_{THHOT} \times \left(\frac{1}{V_{T1}} - \frac{1}{V_{T4}}\right)}{R_{THHOT} \times \left(\frac{1}{V_{T4}} - 1\right) - R_{THCOLD} \times \left(\frac{1}{V_{T1}} - 1\right)} \quad (1)$$

$$R_{T1} = \frac{\left(\frac{1}{V_{T1}} - 1\right)}{\left(\frac{1}{R_{T2}}\right) + \left(\frac{1}{R_{THCOLD}}\right)} \quad (2)$$

For a 103AT-2 type thermistor, its R_{THCOLD} = 27.28kΩ and R_{THHOT} = 3.02kΩ, the calculation results are: R_{T1} = 5.25kΩ and R_{T2} = 30.83kΩ. The standard value of R_{T1} is 5.23kΩ and that of R_{T2} is 30.9kΩ.

DETAILED DESCRIPTION (continued)

Boost Mode Temperature Monitoring (Battery Discharge)

The device is capable of monitoring the battery temperature for safety during the Boost mode. The battery temperature must remain within the TS_TH_OTG_COLD to TS_TH_OTG_HOT[1:0] register settings. If a 103AT NTC thermistor with 5.23kΩ R_{T1} and 30.9kΩ R_{T2} is used, the default value of TS_TH_OTG_COLD register is -10℃, and the default value of TS_TH_OTG_HOT[1:0] register is 60℃. The OTG mode will suspended with REGN remaining turning on once the temperature is outside of range. In addition, the VBUS_STAT[2:0] bits are set to 000, TS_STAT[2:0] bits are set to 001 (TS_OTG_COLD) or 010 (TS_OTG_HOT), and the TS_FLAG bit is set to 1. The Boost mode will restart and TS_STAT[2:0] bits return to 000 (TS_NORMAL), if the battery temperature returns to normal temperature range.

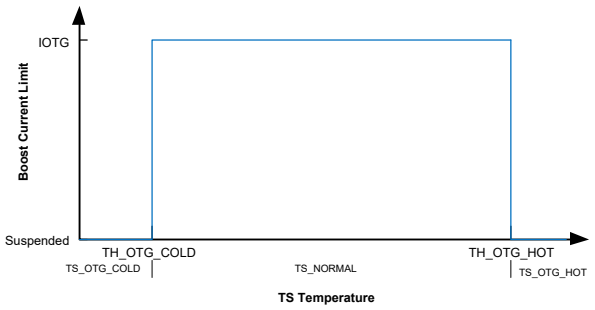


Figure 8. Temperature Sense Threshold of TS Pin Thermistor in Boost Mode

JEITA Charge Rate Scaling

The charge current fold backs of TS_ISET_COOL[1:0], TS_ISET_PRECOOL[1:0], TS_ISET_PREWARM[1:0] and TS_ISET_WARM[1:0] registers are based on a 1C charging rate.

Configure TS_ISET_COOL[1:0] = 01 to make I_{CHG_COOL} = 20% ICHG at 1C charging rate. In order to convert the charging fold back, the host must set the CHG_RATE[1:0] register according to the C rate of battery.

When TS_ISET_COOL[1:0], TS_ISET_PRECOOL[1:0], TS_ISET_PREWARM[1:0] or TS_ISET_WARM[1:0] is set to either 00 (suspended) or 11 (unchanged), the setting of CHG_RATE[1:0] register has no effect. Table 5 shows the summary about ICHG.

Safety Timer

To avoid abnormal battery conditions resulting in prolonged charge cycles, the SGM41551 has three types built-in safety timer to stop charging in such conditions. The host is able to configure the fast charge safety timer and pre-charge safety timer through CHG_TMR and PRECHG_TMR registers, and the trickle charge timer is a fixed 1.12 hour. This feature is optional and can be disabled by clearing EN_SAFETY_TMRS bit. The EN_SAFETY_TMRS bit can be set to 1 anytime, whatever the charger is in any charging stage. Once EN_SAFETY_TMRS = 1 and the corresponding charging stage is active, the safety timer starts to count immediately.

When any safety timer is expired, the SAFETY_TMR_STAT and SAFETY_TMR_FLAG bits will be set to 1. If EN_TMR2X bit is set to 1, events that input DPM, JEITA cool or thermal regulation will cause the charging safety timer to count at half-clock rate. If charger is suspended by faults, these safety timers are also suspended, regardless of the value of the EN_TMR2X bit. Charging resumes and the safety timer also resumes from where it stopped, when the fault disappears.

The charging safety timer and the charging termination are able to be disabled at the same time. With this configuration, the charging will run continuously until it is disabled by the host.

Table 5. ICHG Fold Back Value

TS_ISET_COOL[1:0], TS_ISET_PRECOOL[1:0], TS_ISET_PREWARM[1:0] or TS_ISET_WARM[1:0]	CHG_RATE[1:0]	Fold-Back Current as Percentage of ICHG
00	Any	0% (Suspended)
01 (20%)	00 (1C)	20%
	01 (2C)	10%
	10 (4C)	5%
	11 (6C)	3.3%
10 (40%)	00 (1C)	40%
	01 (2C)	20%
	10 (4C)	10%
	11 (6C)	6.6%
11	Any	100%

DETAILED DESCRIPTION (continued)

Integrated 12-Bit ADC

The SGM41551 features an integrated high accuracy 12-bit ADC to monitor various key system parameters. Table 6 shows the battery monitor operation modes.

To enable the function of ADC, the control bit EN_ADC must be set to 1. The ADC is automatically disabled after POR to conserve power. The ADC is allowed to operate only when either V_{VBUS} > V_{VBUS_UVLOZ} or V_{BAT} > 3V is satisfied.

In ADC one-shot mode, the ADC_DONE_STAT, ADC_DONE_FLAG bits are set to 1 and the EN_ADC bit is set to 0 when an ADC conversion is complete.

The ADC_DONE_STAT and ADC_DONE_FLAG bits are meaningless and remain at 0 under ADC continuous conversion mode, and the EN_ADC bit will never clear until the host disables the ADC by configuring it to 0.

When the EN_CHG bit is 0, the IBAT_ADC register resets to zero, so the IBAT_ADC register can be read correctly in charge disable mode only EN_CHG = 1 and nCE pin is pulled high.

BATFET Control for System Power Reset and Ship Mode

The SGM41551 provides an integrated, low resistance, bidirectional blocking BATFET that can be turned off to eliminate leakage current from the battery to the system. Configure BATFET_CTRL[1:0] bits to enter shutdown mode, ship mode and system power reset. Table 7 shows the BATFET control modes.

Table 6. Battery Monitor Operation Modes

Parameter	Enable Bit	ADC Register	Modes of Operation			
			Charge Mode	Boost Mode	Disable Charge Mode	Battery Only Mode
Input/Output Current (I_{VBUS})	REG0x27[7]	REG0x28	Yes (Input Current)	Yes (Output Current)	Yes (Input Current)	NA
Battery Current (I_{BAT})	REG0x27[6]	REG0x2A	Yes	Yes (Discharge Current)	Yes (Discharge Current)	Yes (Discharge Current)
VBUS Voltage (V_{VBUS})	REG0x27[5]	REG0x2C	Yes	Yes	Yes	NA
Battery Voltage (V_{BAT})	REG0x27[4]	REG0x30	Yes	Yes	Yes	Yes
System Voltage (V_{SYS})	REG0x27[3]	REG0x32	Yes	Yes	Yes	Yes
TS Voltage Percentage (TS)	REG0x27[2]	REG0x34	Yes	Yes	Yes	Yes
Die Temperature (T_{DIE})	REG0x27[1]	REG0x36	Yes	Yes	Yes	Yes
PMID Voltage (V_{PMID})	REG0x27[0]	REG0x2E	Yes	Yes	Yes	Yes

Table 7. BATFET Control Modes

Mode	BATFET	I²C	Entry, Without Adaptor	Entry, With Adaptor, BATFET_CTRL_WVBUS = 0	Entry, With Adaptor, BATFET_CTRL_WVBUS = 1	Exit
Normal	On	Active	N/A	N/A	N/A	N/A
Ship Mode	Off	Active	Setting BATFET_CTRL[1:0] = 10 to turn off BATFET after BATFET_DLY and then the charger enters ship mode.	Setting BATFET_CTRL[1:0] = 10 has no immediate effect when adaptor is plugged in. If the adaptor is removed, the charger turns off BATFET and enters ship mode after BATFET_DLY.	Setting BATFET_CTRL[1:0] = 10 to turn off BATFET after BATFET_DLY.	Pull low nQON pin or adaptor is plugged in or write BATFET_CTRL[1:0] = 00
System Reset	On->Off->On	Active	Setting BATFET_CTRL[1:0] = 11 to initiate system voltage reset after BATFET_DLY. Or pulling nQON pin low for t_{QON_RST} can also initiates immediate reset without BATFET_DLY. Or setting WD_BATFET_RST = 1 to initiate system reset after watchdog timer expired.	Setting BATFET_CTRL[1:0] = 11 has no effect. Pulling nQON pin low for t_{QON_RST} is also ignored. Setting WD_BATFET_RST = 1 has no effect.	Setting BATFET_CTRL[1:0] = 11 to initiate system reset after BATFET_DLY. Or pulling nQON pin low for t_{QON_RST} to initiate immediate reset without BATFET_DLY. Or setting WD_BATFET_RST = 1 to initiate system reset after watchdog timer expired. The charger is placed in HIZ mode during system reset and exits HIZ mode once the system reset completes except for the way of BATFET_CTRL (EN_HIZ is set to 1 after system reset completes).	N/A
Shutdown Mode	Off	Off	Setting BATFET_CTRL[1:0] = 01 to turn off BATFET after BATFET_DLY and the charger enters shutdown mode.	Setting BATFET_CTRL[1:0] = 01 has no effect when the adaptor is plugged in, regardless of the value of BATFET_CTRL_WVBUS register, and the BATFET_CTRL[1:0] bits are automatically reset to 00.		Adaptor is plugged in

DETAILED DESCRIPTION (continued)

Shutdown Mode

To minimize battery leakage current, the host can shut down SGM41551 by configuring the register BATFET_CTRL[1:0] as 01 to enter shutdown mode. In this mode, the BATFET is turned off to avoid that the battery powers the system, the I²C function is disabled and the charger is totally shut down. The SGM41551 can only exit shutdown mode after plugging in an adaptor. When the adaptor is present, the SGM41551 will start running with all register settings reset to POR default.

When the host configures BATFET_CTRL[1:0] as 01, the BATFET turns off after 20ms or 10s delay according to the value of BATFET_DLY register. The charger can only enter shutdown mode when V_{VBUS} < V_{VBUS_UVLO}, regardless of the configuration of BATFET_CTRL_WVBUS setting, which is ignored for shutdown mode entry. If the host sets BATFET_CTRL[1:0] = 01 when V_{VBUS} > V_{VBUS_UVLOZ}, the request is ignored and the BATFET_CTRL[1:0] bits are automatically reset to 00.

The nQON pin has no effect for shutdown mode. The internal pull-up on the nQON pin is automatically disabled when charger enters shutdown to reduce leakage current through this pin.

Ship Mode

The host is able to place SGM41551 into ship mode by writing BATFET_CTRL[1:0] bits to 10. In this mode, the BATFET is turned off to avoid that the battery powers the system, and the I²C function is not disabled. The ship mode has slightly higher quiescent current compare with shutdown mode. The SGM41551 can exit ship mode by below three methods:

1. Hold the nQON pin low for t_{SM_EXIT} (based on SM_EXIT register setting).

2. V_{VBUS} > V_{VBUS_UVLOZ} (adaptor is plugged in).

3. Clear BATFET_CTRL[1:0] bits by using host and I²C.

If the SGM41551 exits from ship mode, the BATFET_CTRL[1:0] register is automatically reset to POR value.

When the BATFET_CTRL_WVBUS bit is configured to 0 and V_{VBUS} > V_{VBUS_UVLO} (adaptor is plugged in), writing BATFET_CTRL[1:0] bits to 10 has no immediate effect. If the adaptor is plugged out when BATFET_CTRL[1:0] = 10, the SGM41551 will enter ship mode after t_{BATFET_DLY} configured by BATFET_DLY register or when the adaptor is removed, whichever comes later.

When the BATFET_CTRL_WVBUS bit is configured to 1 and V_{VBUS} > V_{VBUS_UVLO} (adaptor is plugged in), writing the BATFET_CTRL[1:0] bits to 10 turns off the BATFET after t_{BATFET_DLY}. The Buck converter keeps running when the adaptor is present to supply system power. If the adaptor is plugged out when BATFET_CTRL[1:0] = 10, the SGM41551 will enter ship mode after t_{BATFET_DLY} configured by BATFET_DLY register or when the adaptor is removed, whichever comes later.

System Power Reset

The BATFET works as load switch between battery and system when the Buck converter is not running. The systems are able to be power reset by changing the conduction state of BATFET from on to off. Host can initiate a system power reset by:

1. Set BATFET_CTRL_WVBUS bit to 1 and pull nQON pin low for t_{QON_RST}.

2. Set BATFET_CTRL_WVBUS bit to 1 and the BATFET_CTRL[1:0] bits to 11.

3. Set BATFET_CTRL_WVBUS bit to 1 and WD_BATFET_RST bit to 1 and watchdog timer expired.

4. Set BATFET_CTRL_WVBUS bit to 0 and pull nQON pin low for t_{QON_RST} when V_{VBUS} < V_{VBUS_UVLO} (adaptor is plugged out).

5. Set BATFET_CTRL_WVBUS bit to 0 and the BATFET_CTRL[1:0] bits to 11 when V_{VBUS} < V_{VBUS_UVLO} (adaptor is plugged out).

6. Set BATFET_CTRL_WVBUS bit to 0 and WD_BATFET_RST bit to 1 and watchdog timer expired when V_{VBUS} < V_{VBUS_UVLO} (adaptor is plugged out).

When BATFET_CTRL_WVBUS bit is configured to 1, the system enters power reset proceeds if either BATFET_CTRL[1:0] bits are written to 11 or nQON pin is pulled low for t_{QON_RST} or watchdog timer expired when WD_BATFET_RST bit is 1, whatever the adaptor is present or not. When write BATFET_CTRL[1:0] bits to 11 to enable power reset, there is a delay configured by BATFET_DLY register before starting the system power reset. If nQON pin is pulled low, the system power resets after the t_{QON_RST} completes, regardless of the setting of BATFET_DLY register. If WD_BATFET_RST bit is 1, the system power resets after watchdog timer expired.

The system power reset is able to be started from the battery only mode, OTG mode or the forward charging mode with adaptor plug-in. If the system power is reset during the charger works in OTG mode, the OTG mode is automatically disabled by configuring EN_OTG bit as 0.

DETAILED DESCRIPTION (continued)

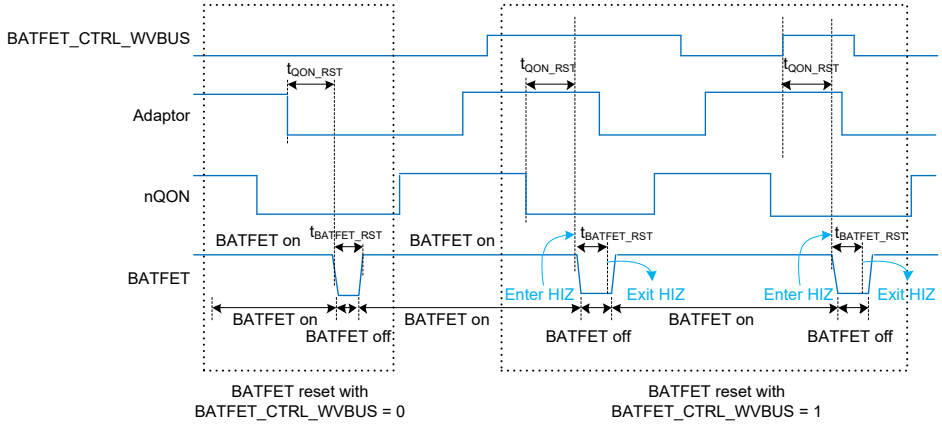


Figure 9. Timing of Enabling and Resetting BATFET by nQON Pin

Status Outputs Pins (nPG, STAT and nINT)

Power Good Indication (nPG Pin)

When a good input source is connected to VBUS and input type is detected, the nPG pin goes low. A good input source is detected if all following conditions on V_{VBUS} are satisfied and input type detection is completed:

- V_{VBUS} is in the operating range: $V_{VBUS\_UVLOZ} < V_{VBUS} < V_{VBUS\_OV}$.
- Device is not in sleep mode: $V_{VBUS} > V_{BAT} + V_{SLEEPZ}$.
- Input source is not poor: $V_{VBUS} > V_{BAD\_SRC\_RISE}$ when I_{BAD_SRC} (10mA TYP) loading is applied. (Poor source detection.)
- Completed input source type detection when EN_AUTO_INDET bit is 1 and this condition is ignored when EN_AUTO_INDET bit is 0.

Charge Status (STAT Pin)

Charging state is indicated with the open-drain STAT pin as explained in Table 8. This pin is able to drive an LED (see Figure 1). The functionality of the STAT pin is disabled if the STAT_DIS bit is set to 1.

Table 8. STAT Pin Function

Charging State	STAT Indicator
Charging battery (or recharge)	Low (LED ON)
Charging completed	High (LED OFF)
Charging is disabled or in sleep mode	High (LED OFF)
Charge is suspended due to input over-voltage, TS fault, timer faults or battery/system over-voltage or Boost mode is suspended (TS fault)	1Hz Blinking

nINT Interrupt Output Pin

When a new update occurs in the charger states, a 256μs negative pulse is sent through the nINT pin to interrupt the host. The host may not continuously monitor the charger device and by receiving the interrupt, it can react and check the charger situation on time. After receiving the nINT pulse, the host could read the flag registers through I²C to check which event causes the nINT, and read the corresponding status registers of charger to check the current state for each flagged event. Once flag bits are set to 1, they remains latched at 1 until these bits are read by the host, and then automatically clear to 0. Unlike flag bits, the status bit always represents the current state of the system, and updates whenever there is a change to status.

All of the interrupt events are able be masked off by configuring mask registers to prevent the generation of nINT pulses when they occur. Interrupt events always cause the corresponding flag bit set to 1, regardless of the configuration of mask register.

Protection Features

Monitoring of Voltage and Current

During the converter operation, the input, system and battery voltage and current are constantly monitored to assure safe operation of the device in both Buck and Boost modes, as described below. Any fault status reports in REG0x1F and fault flag reports in REG0x22. An nINT pulse is sent if REG0x25 is not unmasked.

Buck Mode Voltage and Current Monitoring

1. Input Over-Voltage Protection (VBUS OVP)

Converter switching will stop as soon as VBUS voltage exceeds V_{VBUS_OV} over-voltage limit that is programmable by VBUS_OVP[1:0] in REG0x21. It is selectable among 6.5V, 10.5V, 14V and 18.5V (default) for USB or 5V, 9V or 12V adaptors respectively.

Each time VBUS exceeds the OVP limit, the VBUS_FAULT_FLAG is set to 1 and an nINT pulse is sent if the VBUS_FAULT_MASK = 0. As long as the over-voltage persists, the VBUS_FAULT_STAT bit is set to 1. The VBUS_FAULT_STAT bit will be cleared to 0 if the voltage comes back below limit (and a hysteresis threshold). Charger resumes its normal operation when the voltage comes back below OVP limit.

DETAILED DESCRIPTION (continued)

2. System Over-Voltage Protection (SYS OVP)

During a system load transient, the device clamps the system voltage to protect the system components from over-voltage. The SYSOVP over-voltage limit threshold is 350mV + V_{SYS_REG} (system regulation voltage + 350mV). Once a SYS OVP occurs, switching stops to clamp any overshoot and a 22mA sink current is applied to SYS to pull the voltage down. The SYS_FAULT_STAT is set to 1. An nINT pulse is sent if SYS_FAULT_MASK = 0 and SYS_FAULT_FLAG is set to 1.

Boost Mode Voltage and Current Monitoring

In Boost mode, the RBFET (reverse blocking) and LSFET (low-side switch) FET currents and VBUS voltage are monitored for protection.

1. Soft-Start on VBUS

Boost mode begins with a soft-start to prevent large inrush currents when it is enabled.

2. Output Short/Over-Current Protection for VBUS (VBUS SCP/OCP)

Short-circuit and over-current protection are provided for VBUS output in Boost mode. To accept different types of load connected to VBUS and OTG adaptation, an accurate constant current regulation control is implemented for Boost mode. In case of a short-circuit on VBUS pin, or VBUS or PMID under-voltage because of over-current, the Q1 turns off and retries 7 times (Hiccup). If short is not removed after retries, the OTG will be disabled by clearing EN_OTG bit. Also, an nINT pulse is sent if OTG_FAULT_MASK = 0 and the OTG_FAULT_FLAG bit is set to 1.

3. Output Over-Voltage Protection for VBUS (VBUS OVP)

In Boost mode, converter stops switching and exits Boost mode (by clearing EN_OTG bit) if VBUS voltage rises above regulation and exceeds the $V_{OTG\_VBUS\_OVP}$ over-voltage limit (10.55V TYP, setting by OTG_OVP bit). An nINT pulse is sent if OTG_FAULT_MASK = 0 and the OTG_FAULT_FLAG bit is set to 1.

Thermal Regulation and Shutdown

Buck Mode Thermal Protections

Internal junction temperature (T_J) is always monitored to avoid overheating. A limit of +120℃ is considered for maximum IC surface temperature in Buck mode and if T_J intends to exceed this level, the device reduces the charge current to keep maximum temperature limited to +120℃ (thermal regulation mode) and sets the TREG_STAT bit to 1. An nINT pulse is sent if TREG_MASK = 0 and the TREG_FLAG bit is set to 1.

As expected, the actual charging current is usually lower than programmed value during thermal regulation. Therefore, the safety timer runs at half clock rate and charge termination is disabled during thermal regulation. The thermal regulation temperature is programmable from +60℃ to +120℃ by TREG bit.

If the junction temperature exceeds T_{SHUT} (+140℃), thermal shutdown protection arises in which the converter is turned off, TSHUT_STAT bit is set to 1. An nINT pulse is sent if TSHUT_MASK = 0 and the TSHUT_FLAG is set to 1.

When the device recovers and T_J falls below the hysteresis band of T_{SHUT_HYS} (30℃ under T_{SHUT}), the converter resumes automatically.

Boost Mode Thermal Protections

Similar to Buck mode, T_J is monitored in Boost mode for thermal shutdown protection. If junction temperature exceeds T_{SHUT} (+140℃), the Boost mode will be disabled (EN_OTG bit clears). If T_J falls below the hysteresis band of T_{SHUT_HYS} (30℃ under T_{SHUT}), the Boost can recover again by re-enabling EN_OTG bit by host.

Battery Protections

Battery Over-Voltage Protection (BAT OVP)

The over-voltage limit for the battery is 4% above the battery regulation voltage (V_{BAT_REG}). In case of a BATOVP, charging stops right away, the BAT_FAULT_STAT bit is set to 1. An nINT pulse is sent if BAT_FAULT_MASK = 0 and the BAT_FAULT_FLAG is set to 1.

Battery Over-Discharge Protection

If battery discharges too much and V_{BAT} falls below the depletion level (V_{BAT_UVLO}), the device turns off BATFET to protect battery. This protection is latched and is not recovered until an input source is connected to the VBUS pin. In such condition, the battery will start charging with the small I_{SHORT} current (18mA TYP) first as long as $V_{BAT} < V_{SHORTZ}$. When battery voltage is increased and $V_{SHORTZ} < V_{BAT} < V_{BATLOW\_RISE}$, the charge current will increase to the pre-charge current level programmed in the IPRECHG[5:0] register.

Battery Over-Current Protection for System (BAT OCP)

The BATFET will latch off, if its current limit is exceeded due to a short or large overload on the system (I_{BAT} > IBAT_PK[1:0] with BATOCP_DEG[1:0]). An nINT pulse is sent if BAT_FAULT_MASK = 0 and the BAT_FAULT_FLAG is set to 1. To reset this latch off and enable BATFET, the "Exit Ship Mode" procedure must be followed.

DETAILED DESCRIPTION (continued)

I²C Serial Interface and Data Communication

Standard I²C interface is used to program SGM41551 parameters and get status reports. I²C is the well-known 2-wire serial communication interface that can connect one (or more) master device(s) to some slave devices for two-way communication. The bus lines are named serial data (SDA) and serial clock (SCL). The device that initiates a data transfer is a master. A master generates the SCL signal. Slave devices have unique addresses to identify. A master is typically a micro controller or a digital signal processor.

The SGM41551 operates as a slave device that address is 0x6B. It has 55 registers, numbered from REG0x02 to REG0x38. A register read beyond REG0x38 returns 0xFF.

Physical Layer

The standard I²C interface of SGM41551 supports standard mode and fast mode communication speeds. The frequency of standard mode is up to 100kbits/s, while the fast mode is up to 400kbits/s. Bus lines are pulled high by weak current source or pull-up resistors and in logic high state with no clocking when the bus is free. The SDA pin is open-drain.

I²C Data Communication

START and STOP Conditions

A transaction is started by taking control of the bus by master if the bus is free. The transaction is terminated by releasing the bus when the data transfer job is done as shown in Figure 10. All transactions are started by the master which applies a START condition on the bus lines to take over the bus and exchange data. At the end, the master terminates the transaction by applying one (or more) STOP condition. START condition is generated by master when SCL is high and a high to low transition on the SDA. Similarly, a STOP is defined when SCL is high and SDA goes from low to high. START and STOP are always generated by a master. After a START and before a STOP, the bus is considered busy.

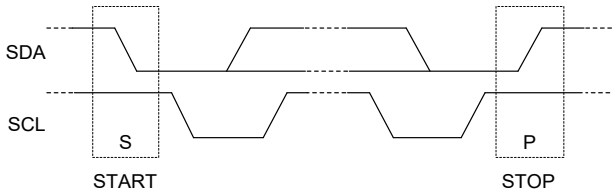


Figure 10. I²C Bus in START and STOP Conditions

Data Bit Transmission and Validity

The data bit (high or low) must remain stable on the SDA line during the high period of the clock. The state of the SDA can only change when the clock (SCL) is low. For each data bit transmission, one clock pulse is generated by master. Bit transfer in I²C is shown in Figure 11.

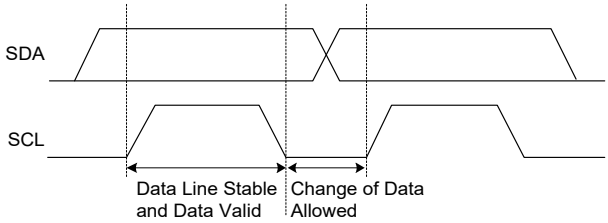


Figure 11. I²C Bus Bit Transfer

Byte Format

Data is transmitted in 8-bit packets (one byte at a time). The number of bytes in one transaction is not limited. In each packet, the 8 bits are sent successively with the Most Significant Bit (MSB) first. An acknowledge (or not-acknowledge) bit must come after the 8 data bits. This bit informs the transmitter whether the receiver is ready to proceed for the next byte or not. Figure 12 shows the byte transfer process with I²C interface.

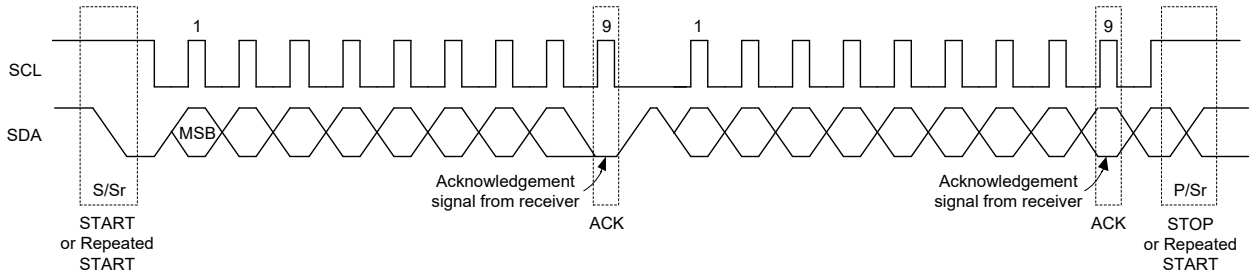


Figure 12. Byte Transfer Process

DETAILED DESCRIPTION (continued)

Acknowledge (ACK) and Not Acknowledge (NCK)

After transmission of each byte by transmitter, an acknowledge bit is replied by the receiver as the ninth bit. With the acknowledge bit, the receiver informs the transmitter that the byte is received, and another byte is expected or can be sent (ACK) or it is not expected (NCK = not ACK). Clock (SCL) is always generated by master, including the acknowledge clock pulse, no matter who is acting as transmitter or receiver. SDA line is released for receiver control during the acknowledge clock pulse. And the receiver can pull the SDA line low as ACK (reply a 0 bit) or let it be high as NCK during the SCL high pulse. After that, the master can either apply a STOP (P) condition to end the transaction or send a new START (S) condition to start a new transfer (called repeated start). For example, when master wants to read a register in slave, one start is needed to send the slave address and register address, and then, without a STOP condition, another start is sent by master to initiate the receiving transaction from slave. Master then sends the STOP condition and releases the bus.

Data Direction Bit and Addressing Slaves

The first byte sent by master after the START is always the target slave address (7 bits) and an eighth data-direction bit (R/$\overline{W}$). R/$\overline{W}$ bit is 0 for a WRITE transaction and 1 for READ (when master is asking for data). Data direction is the same for all next bytes of the transaction. To reverse it, a new START or repeated START condition must be sent by master (STOP will end the transaction). Usually the second byte is a WRITE sending the register address that is supposed to be accessed in the next byte(s). The data transfer transaction is shown in Figure 13.

WRITE: If the master wants to write in the register, the third byte can be written directly as shown in Figure 14 for a single write data transfer. After receiving the ACK, master may issue a STOP condition to end the transaction or send the next register data, which will be written to the next address in a slave as multi-write. A STOP is needed after sending the last data.

READ: If the master wants to read a single register (Figure 15), it sends a new START condition along with device address with R/$\overline{W}$ bit = 1. After ACK is received, master reads the SDA line to receive the content of the register. Master replies with NCK to inform slave that no more data is needed (single read) or it can send an ACK to request for sending the next register content (multi-read). This can continue until an NCK is sent by master. A STOP must be sent by master in any case to end the transaction.

Data Transactions with Multi-Read or Multi-Write

Multi-read and multi-write are supported by SGM41551, as explained in Figure 16 and Figure 17. In the multi-write, every new data byte sent by master is written to the next register of the device. A STOP is sent whenever master is done with writing into device registers.

In a multi-read transaction, after receiving the first register data (its address is already written to the slave), the master replies with an ACK to ask the slave to send the next register data. This can continue as much as it is needed by master. Master sends back an NCK after the last received byte and issues a STOP condition.

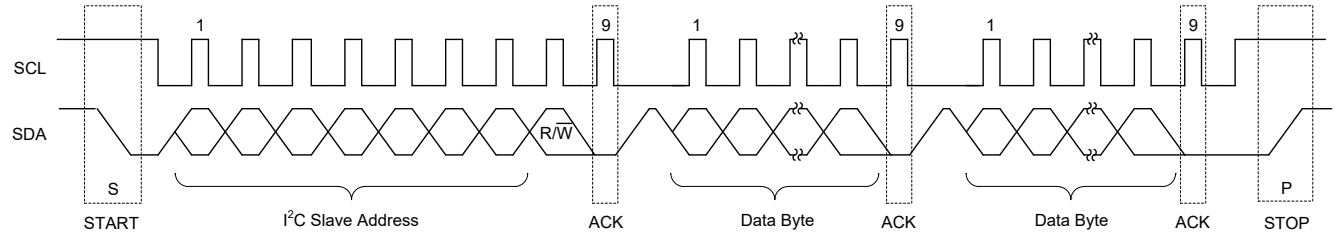


Figure 13. Data Transfer Transaction

DETAILED DESCRIPTION (continued)

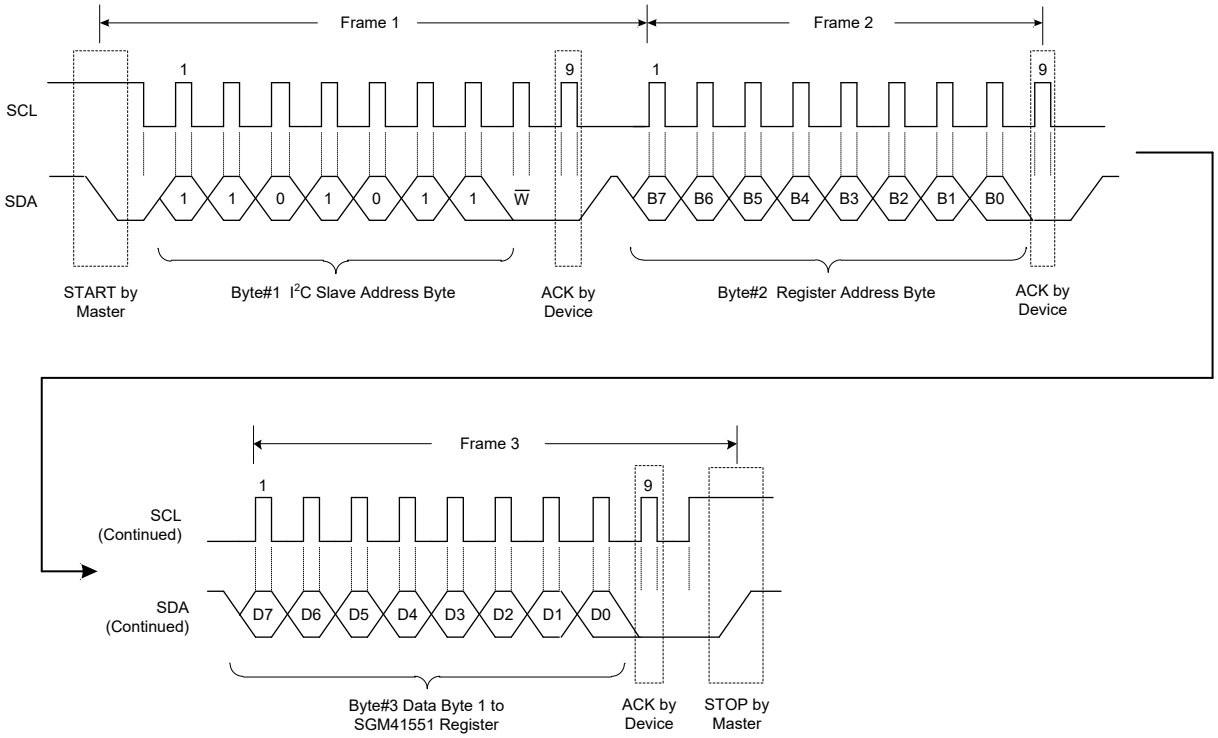


Figure 14. A Single Write Transaction

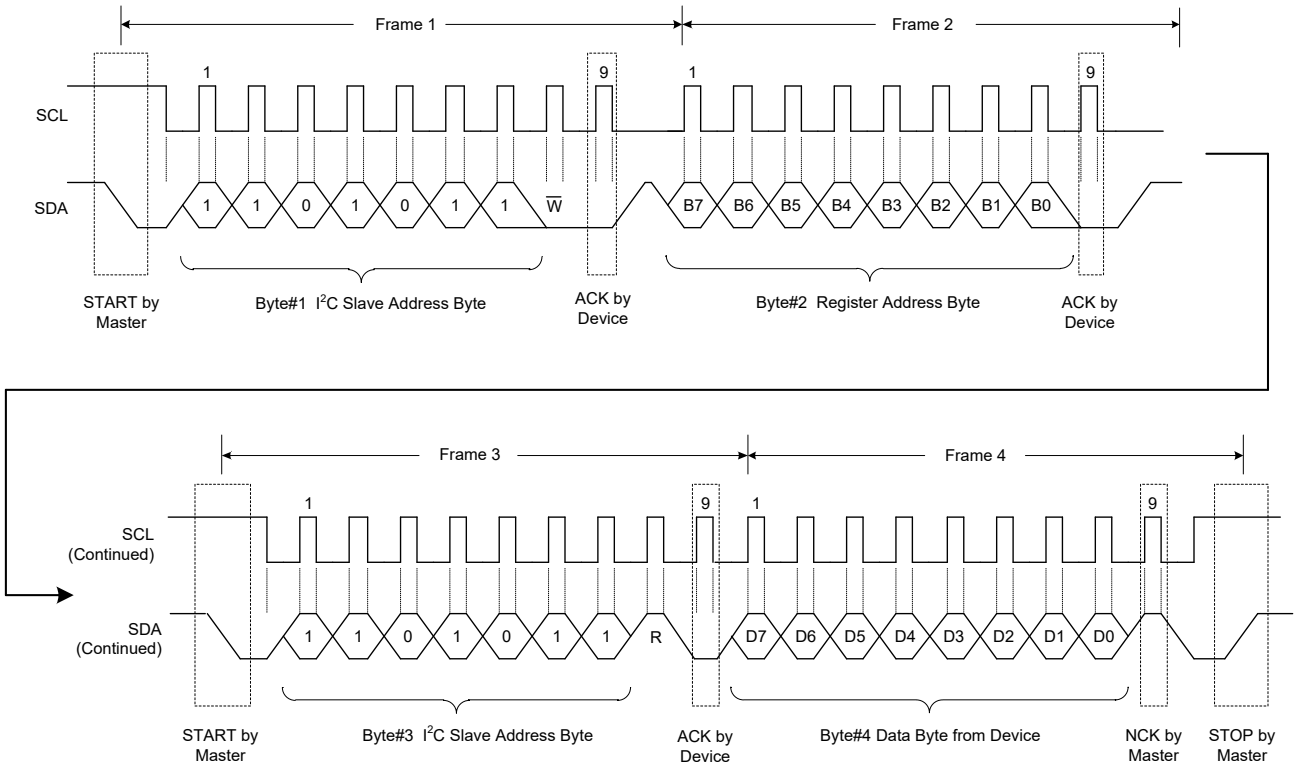


Figure 15. A Single Read Transaction

DETAILED DESCRIPTION (continued)

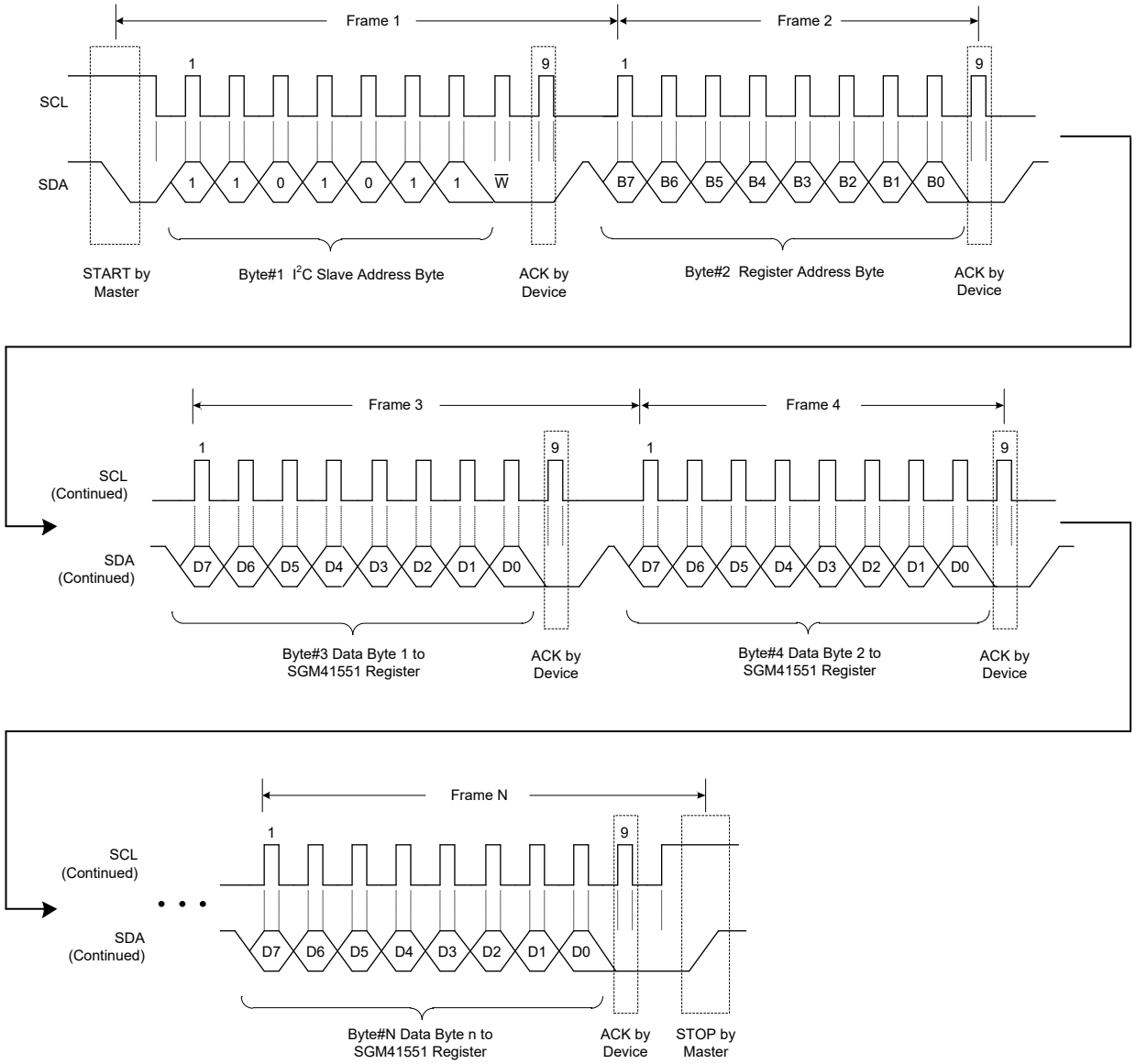


Figure 16. A Multi-Write Transaction

DETAILED DESCRIPTION (continued)

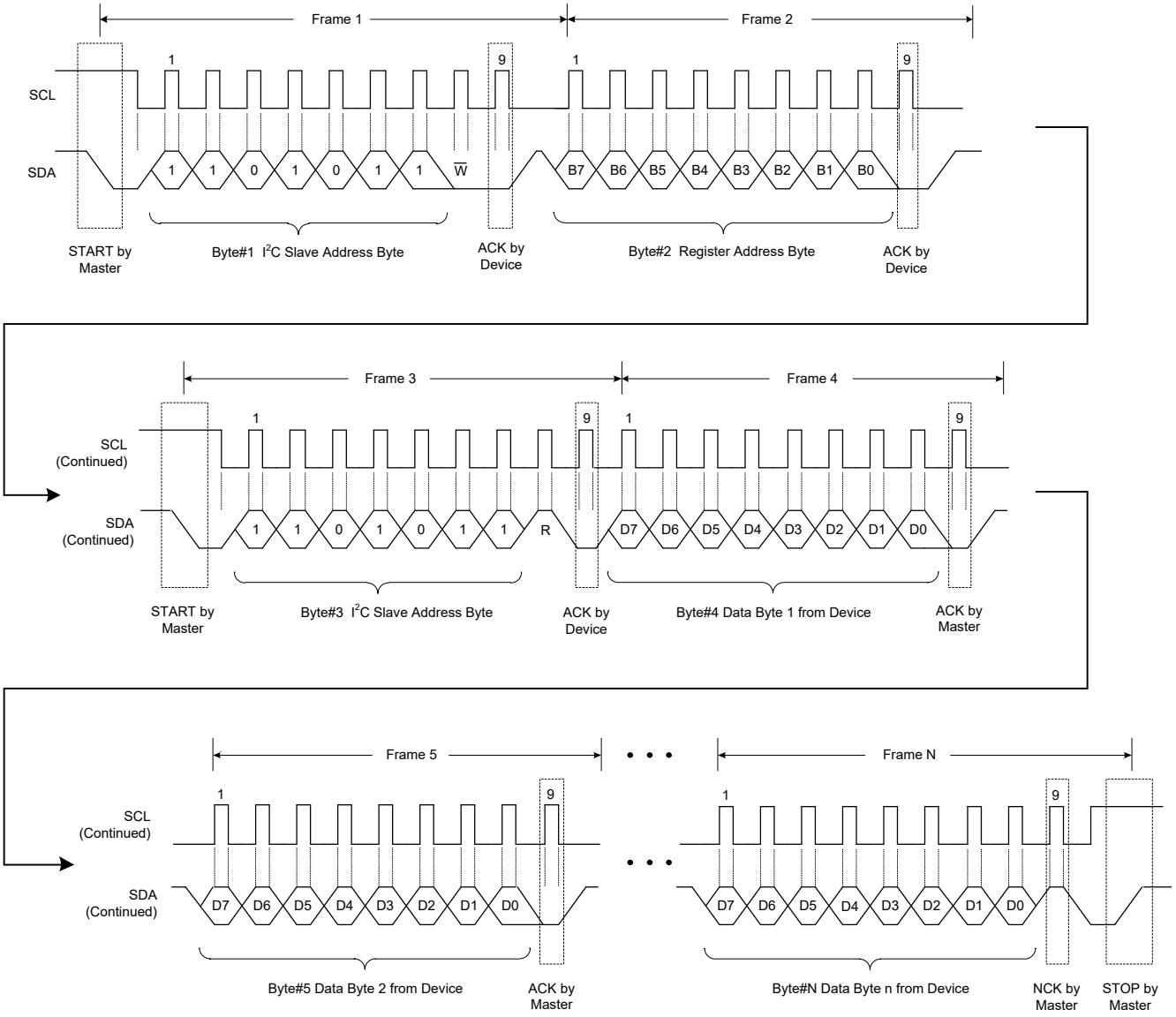


Figure 17. A Multi-Read Transaction

REGISTER MAPS

The SGM41551 has 8-bit and 16-bit registers. For 16-bit register writes, the SGM41551 uses little-endian byte order within a single I²C transaction, starting from the register address that holds the least significant byte (LSB).

I²C Register Address Map

FUNCTION	STAT	FLAG	MASK	THRESHOLD SETTING	ENABLE	DEGLITCH
D+/D- Detection	0x1E[2:0]	0x21[0]	0x24[0]	—	0x15[6] & 0x15[5]	—
HVDCP Detection	0x1E[2:0]	0x21[0]	0x24[0]	0x19[3] & 0x19[2]	—	—
Enable 600mV Bias on D+ Pin at DCP	—	—	—	—	0x15[4]	—
EN_CHG	0x1E[4:3]	0x21[3]	0x24[3]	—	0x16[5]	—
Trickle Charge Current	0x1E[4:3]	0x21[3]	0x24[3]	0x14[5]	—	—
Pre-Charge Current	0x1E[4:3]	0x21[3]	0x24[3]	0x10[8:3] & 0x21[6]	—	—
Fast Charge Current	0x1E[4:3]	0x21[3]	0x24[3]	0x02[11:5]	—	—
Termination Current	0x1E[4:3]	0x21[3]	0x24[3]	0x12[8:2] & 0x21[7]	0x14[2]	0x1E[7]
Termination Delay	0x1E[4:3]	0x21[3]	0x24[3]	0x14[4:3]	0x14[4:3]	
Input Current Limit	0x1D[3]	0x20[3]	0x23[3]	0x06[11:4]	—	—
Input Voltage Limit	0x1D[2]	0x20[2]	0x23[2]	0x08[13:5] & 0x14[1]	—	—
Charge Voltage	0x1E[4:3]	0x21[3]	0x24[3]	0x04[11:3]	—	—
Minimal System Voltage	0x1D[4]	0x20[4]	0x23[4]	0x0E[11:6]	—	—
Pre-Charge to Fast Charge Threshold	—	—	—	0x04[0]	—	—
VBAT_UVLO	—	—	—	0x19[5]	—	0x21[4]
Battery Recharge Threshold	—	—	—	0x14[0]	—	—
EN_OTG	0x1E[2:0]	—	—	0x19[4]	0x18[6]	—
OTG Mode Current Limit	0x1D[3]	0x20[3]	0x23[3]	0x0A[11:4]	—	—
OTG Mode Voltage	—	—	—	0x0C[12:6]	—	—
Boost Mode Startup Delay	—	—	—	0x0E[14]	—	—
Switch Frequency/Capability	—	—	—	0x17[5:4]/0x17[3:2]	—	—
EN_HIZ	—	—	—	—	0x16[4]	—
PSM_FWD_DIS	—	—	—	—	0x18[4]	—
Enable Half Clock Rate Safety Timer	—	—	—	—	0x15[3]	—
Charge Safety Timer	0x1D[1]	0x20[1]	0x23[1]	0x15[1] & 0x15[0]	0x15[2]	—
WATCHDOG	0x1D[0]	0x20[0]	0x23[0]	0x16[1:0]	0x16[1:0]	—
Watchdog Timer Reset	—	—	—	—	0x16[2]	—
Registers Reset	—	—	—	—	0x17[7]	—
System Reset	—	—	—	0x18[1:0] & 0x18[2]	0x04[2] (& 0x18[3] if VBUS present) 0x04[1] (& 0x18[3] if VBUS present)	—
Exit Ship Mode Delay	—	—	—	0x18[7]	—	—
BATFET Control	—	—	—	0x18[1:0] & 0x18[2]	—	—
RBFET/BATFET R_{DSON}	—	—	—	0x14[7]/0x14[6]	—	—
STAT_DIS	—	—	—	—	0x15[7]	—
Enable VBUS Pull-Down	—	—	—	—	0x24[7]	—
VBUS_SINK_DIS	—	—	—	—	0x24[1]	—
Enable Battery Discharge during BAT OVP	—	—	—	—	0x16[7]	—
Force BAT/PMID Discharge	—	—	—	0x16[6]/0x16[3]	—	—
JEITA	0x1F[2:0]	0x22[0]	0x25[0]	0x19[1:0] & 0x1A to 0x1C	0x1A[7]	—
ADC	0x1D[6]	0x20[6]	0x23[6]	0x26[6:2]	0x26[7] & 0x27	—
Thermal Regulation	0x1D[5]	0x20[5]	0x23[5]	0x17[6]	—	—
Thermal Shutdown	0x1F[3]	0x22[3]	0x25[3]	—	—	—
VBUS_FAULT	0x1F[7]	0x22[7]	0x25[7]	0x21[2:1]	—	—
BAT_FAULT	0x1F[6]	0x22[6]	0x25[6]	0x17[1:0] & 0x19[7:6]	—	—
SYS_FAULT	0x1F[5]	0x22[5]	0x25[5]	—	—	—
OTG_FAULT	0x1F[4]	0x22[4]	0x25[4]	0x21[5]	—	—
Part Information	—	—	—	0x38[5:0]	—	—

REGISTER MAPS (continued)

I²C Slave Address of SGM41551: 0b1101 011 + W/R

Bit Types:

R/W: Read/Write bit(s)

R: Read only bit(s)

RC: Read clears the bit

R/WC: Read/Write. Writing a '1' clears the bit. Writing a '0' has no effect.

n: Parameter code formed by the bits as an unsigned binary number.

REG0x02: Charge Current Limit Register [Reset = 0x0340]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[15:12]	Reserved	0000	R	Reserved	N/A
D[11:5]	ICHG[6:0]	001 1010	R/W	Charge Current Regulation Limit I_{CHG} = 40n (mA) Offset: 0mA Bit Step: 40mA Range: 40mA (000 0001) - 3520mA (101 1000) Default: 1040mA (001 1010) Note: ICHG[6:3] is in REG0x03[3:0], and ICHG[2:0] is in REG0x02[7:5]. Values below 0x01 = 40mA are clamped to 0x01 = 40mA and above 0x58 = 3520mA are clamped to 0x58 = 3520mA. When Q4_FULLON = 1, this register has a minimum value of 80mA. When the watchdog timer is expired, ICHG is set to 1/2 its previous value (rounded down).	REG_RST
D[4:0]	Reserved	0 0000	R/W	Reserved	REG_RST or Watchdog

REG0x04: Charge Voltage Limit Register [Reset = 0x0D23]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[15:12]	Reserved	0000	R/W	Reserved	REG_RST or Watchdog
D[11:3]	VREG[8:0]	1 1010 0100	R/W	Battery Voltage Regulation Limit V_{BAT_REG} = 10n (mV) Offset: 0mV Bit Step: 10mV Range: 3500mV (1 0101 1110) - 4800mV (1 1110 0000) Default: 4200mV (1 1010 0100) Note: VREG[8:5] is in REG0x05[3:0], and VREG[4:0] is in REG0x04[7:3]. Values below 0x015E = 3500mV are clamped to 0x015E = 3500mV and above 0x01E0 = 4800mV are clamped to 0x01E0 = 4800mV.	REG_RST
D[2]	WD_BATFET_RST	0	R/W	Watchdog Timer Expired Allows BATFET Off for System Power Reset 0 = Disable BATFET reset (default) 1 = Enable BATFET reset	REG_RST
D[1]	nQON_BATFET_RST	1	R/W	nQON Pulled Down for t_{QON_RST} Allows BATFET Off for System Power Reset 0 = Disable BATFET reset 1 = Enable BATFET reset (default)	REG_RST or Watchdog
D[0]	BATLOWV	1	R/W	Battery Pre-Charge to Fast Charge Threshold 0 = 2.8V 1 = 3V (default)	REG_RST

REGISTER MAPS (continued)

REG0x06: Input Current Limit Register [Reset = 0x0A00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[15:12]	Reserved	0000	R/W	Reserved	REG_RST or Watchdog
D[11:4]	IINDPM[7:0]	1010 0000	R/W	Input Current Regulation Limit I_{INDPM} = 20n (mA) Offset: 0mA Bit Step: 20mA Range: 100mA (0000 0101) - 3200mA (1010 0000) Default: 3200mA (1010 0000) Note: IINDPM[7:4] is in REG0x07[3:0], and IINDPM[3:0] is in REG0x06[7:4]. Values below 0x05 = 100mA are clamped to 0x05 = 100mA and above 0xA0 = 3200mA are clamped to 0xA0 = 3200mA. IINDPM[7:0] bits are changed automatically after the input source type detection is completed. USB SDP = 500mA USB CDP = 1.5A USB DCP = 1.5A HVDCP = 1.5A Unknown Adaptor = 500mA Non-Standard Adaptor = 1A/2A/2.1A/2.4A	REG_RST or Adaptor Removal
D[3:0]	Reserved	0000	R	Reserved	N/A

REG0x08: Input Voltage Limit Register [Reset = 0x0E60]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[15:14]	Reserved	00	R/W	Reserved	REG_RST or Watchdog
D[13:5]	VINDPM[8:0]	0 0111 0011	R/W	Absolute Input Voltage Regulation Limit V_{INDPM} = 40n (mV) Offset: 0mV Bit Step: 40mV Range: 3800mV (0 0101 1111) - 16800mV (1 1010 0100) Default: 4600mV (0 0111 0011) Note: VINDPM[8:3] is in REG0x09[5:0], and VINDPM[2:0] is in REG0x08[7:5]. Values below 0x005F = 3800mV are clamped to 0x005F = 3800mV and above 0x01A4 = 16800mV are clamped to 0x01A4 = 16800mV.	REG_RST
D[4:0]	Reserved	0 0000	R	Reserved	N/A

REG0x0A: IOTG Regulation Register [Reset = 0x0320]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[15:12]	Reserved	0000	R/W	Reserved	REG_RST or Watchdog
D[11:4]	IOTG[7:0]	0011 0010	R/W	OTG Mode Current Regulation Limit I_{OTG} = 20n (mA) Offset: 0mA Bit Step: 20mA Range: 100mA (0000 0101) - 2000mA (0110 0100) Default: 1000mA (0011 0010) Note: IOTG[7:4] is in REG0x0B[3:0], and IOTG[3:0] is in REG0x0A[7:4]. Values below 0x05 = 100mA are clamped to 0x05 = 100mA and above 0x64 = 2000mA are clamped by inductor current.	REG_RST or Watchdog
D[3:0]	Reserved	0000	R	Reserved	N/A

REGISTER MAPS (continued)

REG0x0C: VOTG Regulation Register [Reset = 0x0FC0]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[15:13]	Reserved	000	R/W	Reserved	REG_RST or Watchdog
D[12:6]	VOTG[6:0]	011 1111	R/W	OTG Mode Regulation Voltage V_{OTG} = 80n (mV) Offset: 0mV Bit Step: 80mV Range: 3840mV (011 0000) - 9600mV (111 1000) Default: 5040mV (011 1111) Note: VOTG[6:2] is in REG0x0D[4:0], and VOTG[1:0] is in REG0x0C[7:6]. Values below 0x30 = 3840mV are clamped to 0x30 = 3840mV and above 0x78 = 9600mV are clamped to 0x78 = 9600mV.	REG_RST
D[5:0]	Reserved	00 0000	R	Reserved	N/A

REG0x0E: Minimal System Voltage Register [Reset = 0x0B00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[15]	Reserved	0	R/W	Reserved	REG_RST or Watchdog
D[14]	BOOST_START_DELAY	0	R/W	Boost Mode Startup Delay Setting Bit 0 = Disable Boost mode delay time shortening function (default) 1 = Shorten the Boost mode startup time by no more than 15ms.	REG_RST or Watchdog
D[13:12]	Reserved	00	R/W	Reserved	REG_RST or Watchdog
D[11:6]	VSYSMIN[5:0]	10 1100	R/W	Minimal System Voltage V_{SYSMIN} = 80n (mV) Offset: 0mV Bit Step: 80mV Range: 2560mV (10 0000) - 3840mV (11 0000) Default: 3520mV (10 1100) Note: VSYSMIN[5:2] is in REG0x0F[3:0], and VSYSMIN[1:0] is in REG0x0E[7:6]. Values below 0x20 = 2560mV are clamped to 0x20 = 2560mV and above 0x30 = 3840mV are clamped to 0x30 = 3840mV.	REG_RST
D[5:0]	Reserved	00 0000	R	Reserved	N/A

REG0x10: Pre-Charge Control Register [Reset = 0x0050]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[15:9]	Reserved	000 0000	R	Reserved	N/A
D[8:3]	IPRECHG[5:0]	00 1010	R/W	Pre-Charge Current Regulation Limit I_{PRECHG} = 10n (mA) n is even Offset: 0mA Bit Step: 20mA Range: 20mA (00 0010) - 620mA (11 1110) Default: 100mA (00 1010) Note: IPRECHG[5] is in REG0x11[0], and IPRECHG[4:0] is in REG0x10[7:3]. Values below 0x02 = 20mA are clamped to 0x02 = 20mA and above 0x3E = 620mA are clamped to 0x3E = 620mA. When Q4_FULLON = 1, this register has a minimum value of 80mA.	REG_RST
D[2:0]	Reserved	000	R	Reserved	N/A

REGISTER MAPS (continued)

REG0x12: Termination Control Register [Reset = 0x0030]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[15:9]	Reserved	000 0000	R	Reserved	N/A
D[8:2]	ITERM[6:0]	000 1100	R/W	Termination Current Threshold I_{TERM} = 5n (mA) n is even Offset: 0mA Bit Step: 10mA Range: 10mA (000 0010) - 620mA (111 1100) Default: 60mA (000 1100) Note: ITERM[6] is in REG0x13[0], and ITERM[5:0] is in REG0x12[7:2]. Values below 0x02 = 10mA are clamped to 0x02 = 10mA and above 0x7C = 620mA are clamped to 0x7C = 620mA. When Q4_FULLON = 1, this register has a minimum value of 120mA.	REG_RST
D[1:0]	Reserved	00	R	Reserved	N/A

REG0x14: Charge Control 0 Register [Reset = 0x06]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	Q1_FULLON	0	R/W	RBFET R_{DSON} Setting 0 = RBFET R_{DSON} is always 24mΩ (default) 1 = RBFET R_{DSON} determined by IINDPM setting Forces RBFET (Q1) into low resistance state (24mΩ), regardless of IINDPM setting.	N/A
D[6]	Q4_FULLON	0	R/W	BATFET R_{DSON} Setting 0 = BATFET R_{DSON} determined by charge current (default) 1 = BATFET R_{DSON} is always 18mΩ Forces BATFET (Q4) into low resistance state (18mΩ), regardless of ICHG setting. (Only applies when V_{BAT} > V_{SYSMIN}. Otherwise BATFET operates in linear mode.)	N/A
D[5]	ITRICKLE	0	R/W	Trickle Charging Current Setting 0 = 18mA (default) 1 = 80mA	REG_RST
D[4:3]	TOPOFF_TMR[1:0]	00	R/W	Top-Off Timer Control 00 = Disabled (default) 01 = 16.2min 10 = 34min 11 = 52min	REG_RST
D[2]	EN_TERM	1	R/W	Enable Charging Termination 0 = Disable 1 = Enable (default)	REG_RST or Watchdog
D[1]	VINDPM_BAT_TRACK	1	R/W	Set VINDPM to Track BAT Voltage 0 = Disable function (VINDPM set by register) 1 = V_{BAT} + 200mV (default) Actual VINDPM is higher value of the setting of VINDPM register and V_{BAT} + $V_{INDPM\_BAT\_TRACK}$ if this bit is set to 1.	REG_RST
D[0]	VRECHG	0	R/W	Battery Recharge Threshold Offset (Below VREG[8:0]) 0 = 100mV (default) 1 = 200mV	REG_RST

REGISTER MAPS (continued)

REG0x15: Charge Timer Control Register [Reset = 0x5C]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	STAT_DIS	0	R/W	Disable the STAT Pin Output 0 = Enable (default) 1 = Disable	REG_RST
D[6]	EN_AUTO_INDET	1	R/W	Automatic D+/D- Detection Enable 0 = Disable D+/D- detection when VBUS is plugged in 1 = Enable D+/D- detection when VBUS is plugged in (default)	REG_RST or Watchdog
D[5]	FORCE_INDET	0	R/WC	Force D+/D- Detection 0 = Do not force D+/D- detection (default) 1 = Force D+/D- algorithm, when D+/D- detection is done, this bit is reset to 0	REG_RST or Watchdog
D[4]	EN_DCP_BIAS	1	R/W	Enable 600mV Bias on D+ Pin whenever DCP is Detected by BC1.2 Detection Algorithm (VBUS_STAT[2:0] = 011) 0 = Disable 600mV bias on D+ pin 1 = Enable 600mV bias on D+ pin if DCP detected (default)	REG_RST or Watchdog
D[3]	EN_TMR2X	1	R/W	Enable Half Clock Rate Safety Timer 0 = Disable 1 = Safety timer slows down during DPM, JEITA cool, or thermal regulation (default) Slow down by a factor of 2.	REG_RST
D[2]	EN_SAFETY_TMRS	1	R/W	Enable Fast Charge, Pre-Charge and Trickle Charge Timers 0 = Disable 1 = Enable (default)	REG_RST or Watchdog
D[1]	PRECHG_TMR	0	R/W	Pre-Charge Safety Timer Setting 0 = 2h (default) 1 = 0.52h	REG_RST
D[0]	CHG_TMR	0	R/W	Fast Charge Safety Timer Setting 0 = 12.5h (default) 1 = 23.8h	REG_RST

REG0x16: Charger Control 1 Register [Reset = 0xA1]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	EN_AUTO_IBAT	1	R/W	Enable the Auto Battery Discharging during the BAT OVP 0 = Disable a discharging current on BAT during BAT OVP 1 = Enable a discharging current on BAT during BAT OVP (default)	REG_RST
D[6]	FORCE_BAT_DCHG	0	R/W	Force a Battery Discharging Current (~30mA) 0 = Do not force a discharging current on BAT (default) 1 = Force a discharging current on BAT	REG_RST or Watchdog
D[5]	EN_CHG	1	R/W	Enable Battery Charging 0 = Charge disable 1 = Charge enable (default) Charge is enabled when EN_CHG bit is 1 and nCE pin is pulled low.	REG_RST or Watchdog
D[4]	EN_HIZ	0	R/W	Enable HIZ Mode 0 = Disable (default) 1 = Enable	REG_RST or Watchdog or Adaptor Plug-In
D[3]	FORCE_PMID_DCHG	0	R/W	Force a PMID Discharge Current (~30mA) 0 = Do not force a discharging current on PMID (default) 1 = Force a discharging current on PMID	REG_RST or Watchdog
D[2]	WD_RST	0	R/WC	I²C Watchdog Timer Reset 0 = Normal (default) 1 = Reset (this bit goes back to 0 after timer reset)	REG_RST
D[1:0]	WATCHDOG[1:0]	01	R/W	Watchdog Timer Setting 00 = Disable 01 = 40s (default) 10 = 80s 11 = 160s	REG_RST

REGISTER MAPS (continued)

REG0x17: Charger Control 2 Register [Reset = 0x4C]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	REG_RST	0	R/WC	Reset Registers to Default Values 0 = Not reset (default) 1 = Reset. Value resets to 0 after reset completes.	REG_RST
D[6]	TREG	1	R/W	Thermal Regulation Thresholds 0 = 60℃ 1 = 120℃ (default)	REG_RST
D[5:4]	SET_CONV_FREQ[1:0]	00	R/W	Adjust Switching Frequency of the Converter 00 or 11 = Nominal, 1.5MHz (default) 01 = -10%, 1.35MHz 10 = +10%, 1.65MHz	REG_RST
D[3:2]	SET_CONV_STRN[1:0]	11	R/W	Configure Driver Capability of the High-side and Low-side to Adjust Efficiency Versus EMI 00 = Weak 01 = Normal 10 = Reserved 11 = Strong (default)	REG_RST
D[1:0]	BATOCP_DEG[1:0]	00	R/W	BATFET Over-Current Protection Deglitch Time 00 = 128μs (default) 01 = 256μs 10 = 1ms 11 = 2ms	REG_RST

REG0x18: Charger Control 3 Register [Reset = 0x84]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	SM_EXIT	1	R/W	Wait Delay for Exiting Ship Mode Setting 0 = 120ms 1 = 0.94s (default)	REG_RST
D[6]	EN_OTG	0	R/W	OTG Mode Control 0 = OTG disable (default) 1 = OTG enable	REG_RST or Watchdog
D[5]	Reserved	0	R/W	Reserved.	REG_RST
D[4]	PSM_FWD_DIS	0	R/W	Disable PSM in Forward Buck Mode 0 = Enable (default) 1 = Disable	REG_RST
D[3]	BATFET_CTRL_WVBUS	0	R/W	Enable BATFET Off or System Power Reset When Adaptor Presents 0 = Disable (default) 1 = Enable	N/A
D[2]	BATFET_DLY	1	R/W	Select Delay Time that Added to the Taking Action of BATFET_CTRL[1:0] Bits 0 = Add 20ms delay time 1 = Add 10s delay time (default)	REG_RST
D[1:0]	BATFET_CTRL[1:0]	00	R/W	BATFET Control Force the device enters different working modes. 00 = Normal (default) 01 = Shutdown mode 10 = Ship mode 11 = System power reset	REG_RST

REGISTER MAPS (continued)

REG0x19: Charger Control 4 Register [Reset = 0xC0]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:6]	IBAT_PK[1:0]	11	R/W	Battery Discharging Peak Current Protection Threshold Setting 00 = 1.5A 01 = 3A 10 = 6A 11 = 12A (default)	REG_RST
D[5]	VBAT_UVLO	0	R/W	Select the V_{BAT_UVLO} (Falling) Threshold and V_{SHORT} (Falling) Threshold 0 = V_{BAT_UVLO} 2.15V, V_{SHORT} 2.05V (default) 1 = V_{BAT_UVLO} 2V, V_{SHORT} 1.85V	REG_RST
D[4]	VBAT_OTG_MIN	0	R/W	Select the Minimal Battery Voltage to Start the OTG Mode 0 = 3V rising/2.8V falling (default) 1 = 2.6V rising/2.4V falling	REG_RST
D[3]	EN_9V	0	R/W	Enable 9V HVDCP Adaptor Detection 0 = Disabled (default) 1 = Enabled After the input power source type detection completed, the EN_9V bit is ignored.	REG_RST
D[2]	EN_12V	0	R/W	Enable 12V HVDCP Adaptor Detection 0 = Disabled (default) 1 = Enabled The EN_12V bit has a higher priority than EN_9V bit. After the input power source type detection completed, the EN_12V bit is ignored.	REG_RST or Watchdog
D[1:0]	CHG_RATE[1:0]	00	R/W	The charge rate definition is used for the fast charge stage in TS_COOL, PRECOOL, PREWARM and WARM. Refer to Table 5. 00 = 1C (default) 01 = 2C 10 = 4C 11 = 6C The charging current fold back value equals the setting value of ICHG times the ratio of fold back, and then is divided by the charge rate that configured by these bits.	REG_RST

REG0x1A: NTC Control 0 Register [Reset = 0x3D]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	TS_IGNORE	0	R/W	Ignore JEITA Function 0 = Not ignore (default) 1 = Ignore If this bit is set to 1, the charger considers the battery temperature is always ok to allow charge and OTG modes, and the TS_STAT[2:0] bits report to 000.	REG_RST or Watchdog
D[6:5]	TS_TH_OTG_HOT[1:0]	01	R/W	TS_HOT Temperature Setting for OTG Mode 00 = 55℃ 01 = 60℃ (default) 10 = 65℃ 11 = Disable	REG_RST
D[4]	TS_TH_OTG_COLD	1	R/W	TS_COLD Temperature Setting for OTG Mode 0 = -20℃ 1 = -10℃ (default)	REG_RST
D[3:2]	TS_ISET_WARM[1:0]	11	R/W	TS_WARM Charge Current Setting 00 = Charge suspend 01 = Set I_{CHG} to 20% 10 = Set I_{CHG} to 40% 11 = I_{CHG} unchanged (default)	REG_RST
D[1:0]	TS_ISET_COOL[1:0]	01	R/W	TS_COOL Charge Current Setting 00 = Charge suspend 01 = Set I_{CHG} to 20% (default) 10 = Set I_{CHG} to 40% 11 = I_{CHG} unchanged	REG_RST

REGISTER MAPS (continued)

REG0x1B: NTC Control 1 Register [Reset = 0x25]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:5]	TS_TH1_TH2_TH3[2:0]	001	R/W	TH1 (TS_COLD), TH2 (TS_COOL) and TH3 (TS_PRECOOL) Temperature Setting 000 = TH1 is 0℃, TH2 is 5℃, TH3 is 15℃ 001 = TH1 is 0℃, TH2 is 10℃, TH3 is 15℃ (default) 010 = TH1 is 0℃, TH2 is 15℃, TH3 is 20℃ 011 = TH1 is 0℃, TH2 is 20℃, TH3 20℃ 100 = TH1 is -5℃, TH2 is 5℃, TH3 is 15℃ 101 = TH1 is -5℃, TH2 is 10℃, TH3 is 15℃ 110 = TH1 is -5℃, TH2 is 10℃, TH3 is 20℃ 111 = TH1 is 0℃, TH2 is 10℃, TH3 is 20℃	REG_RST
D[4:2]	TS_TH4_TH5_TH6[2:0]	001	R/W	TH4 (TS_PREWARM), TH5 (TS_WARM) and TH6 (TS_HOT) Temperature Setting 000 = TH4 is 35℃, TH5 is 40℃, TH6 is 60℃ 001 = TH4 is 35℃, TH5 is 45℃, TH6 is 60℃ (default) 010 = TH4 is 35℃, TH5 is 50℃, TH6 is 60℃ 011 = TH4 is 40℃, TH5 is 55℃, TH6 is 60℃ 100 = TH4 is 35℃, TH5 is 40℃, TH6 is 50℃ 101 = TH4 is 35℃, TH5 is 45℃, TH6 is 50℃ 110 = TH4 is 40℃, TH5 is 45℃, TH6 is 60℃ 111 = TH4 is 40℃, TH5 is 50℃, TH6 is 60℃	REG_RST
D[1:0]	TS_VSET_WARM[1:0]	01	R/W	TS_WARM Charge Voltage Setting 00 = Set charge voltage to VREG[8:0] - 300mV 01 = Set charge voltage to VREG[8:0] - 200mV (default) 10 = Set charge voltage to VREG[8:0] - 100mV 11 = Set charge voltage to VREG[8:0]	REG_RST

REG0x1C: NTC Control 2 Register [Reset = 0x3F]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	Reserved	0	R	Reserved	N/A
D[6]	TS_VSET_COOLx	0	R/W	TS_COOL and TS_PRECOOL Charge Voltage Setting 0 = VREG[8:0] unchanged (default) 1 = TS_VSET_COOL matches TS_VSET_WARM, TS_VSET_PRECOOL matches TS_VSET_PREWARM	REG_RST
D[5:4]	TS_VSET_PREWARM[1:0]	11	R/W	TS_PREWARM Charge Voltage Setting 00 = Set charge voltage to VREG[8:0] - 300mV 01 = Set charge voltage to VREG[8:0] - 200mV 10 = Set charge voltage to VREG[8:0] - 100mV 11 = Set charge voltage to VREG[8:0] (default)	REG_RST
D[3:2]	TS_ISET_PREWARM[1:0]	11	R/W	TS_PREWARM Charge Current Setting 00 = Charge Suspend 01 = Set I_{CHG} to 20% 10 = Set I_{CHG} to 40% 11 = I_{CHG} unchanged (default)	REG_RST
D[1:0]	TS_ISET_PRECOOL[1:0]	11	R/W	TS_PRECOOL Charge Current Setting 00 = Charge Suspend 01 = Set I_{CHG} to 20% 10 = Set I_{CHG} to 40% 11 = I_{CHG} unchanged (default)	REG_RST

REGISTER MAPS (continued)

REG0x1D: Charge Status 0 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	Reserved	0	R	Reserved	N/A
D[6]	ADC_DONE_STAT	0	R	ADC Conversion Done Status (in One-Shot Mode Only) Bit 0 = Conversion not done (default) 1 = In conversion done Always reads 0 in continuous mode.	N/A
D[5]	TREG_STAT	0	R	IC Thermal Regulation Status Bit 0 = Not in IC thermal regulation (default) 1 = In thermal regulation	N/A
D[4]	VSYS_STAT	0	R	VSYS Regulation Status (Forward Mode) Bit 0 = Not in VSYSMIN regulation (V_{BAT} > V_{SYSMIN}) (default) 1 = In VSYSMIN regulation (V_{BAT} < V_{SYSMIN})	N/A
D[3]	IINDPM_STAT	0	R	IINDPM or IOTG Regulation Status Bit 0 = Not in IINDPM or IOTG regulation (default) 1 = In IINDPM or IOTG regulation In forward mode, indicates that device enters IINDPM regulation loop. In OTG mode, indicates that device enters IOTG regulation loop.	N/A
D[2]	VINDPM_STAT	0	R	VINDPM Regulation Status Bit 0 = Not in VINDPM regulation (default) 1 = In VINDPM regulation	N/A
D[1]	SAFETY_TMR_STAT	0	R	Fast Charge, Trickle Charge and Pre-Charge Timer Expired Status Bit 0 = Normal (default) 1 = In safety timer expired	N/A
D[0]	WD_STAT	0	R	I²C Watchdog Timer Expired Status Bit 0 = Normal (default) 1 = In WD timer expired	N/A

REG0x1E: Charge Status 1 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	ITERM_TIMER	0	R/W	ITERM Deglitch Timer Setting Bit 0 = 230ms (default) 1 = 16ms	REG_RST or Watchdog
D[6:5]	Reserved	00	R/W	Reserved	REG_RST or Watchdog
D[4:3]	CHG_STAT[1:0]	00	R	Charge Status Bits 00 = Not charging or charge terminated (default) 01 = Trickle charge, pre-charge or fast charge (CC mode) 10 = Taper charge (CV mode) 11 = Top-off timer active charging	N/A
D[2:0]	VBUS_STAT[2:0]	000	R	VBUS Status Bits 000 = No qualified adaptor, or EN_AUTO_INDET = 0 (default) 001 = USB SDP adaptor (500mA) 010 = USB CDP adaptor (1.5A) 011 = USB DCP adaptor (1.5A) 100 = Unknown adaptor (500mA) 101 = Non-standard adaptor (1A/2A/2.1A/2.4A) 110 = HVDCP adaptor (1.5A) 111 = In OTG mode	N/A

REGISTER MAPS (continued)

REG0x1F: FAULT Status 0 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	VBUS_FAULT_STAT	0	R	VBUS OVP or Sleep except for OTG Mode Status Bit 0 = Normal (default) 1 = In VBUS OVP or sleep except for OTG mode	N/A
D[6]	BAT_FAULT_STAT	0	R	BAT OCP or OVP Status Bit 0 = Normal (default) 1 = In BAT OCP or OVP	N/A
D[5]	SYS_FAULT_STAT	0	R	SYS SCP or OVP Status Bit 0 = Normal (default) 1 = In SYS SCP or OVP	N/A
D[4]	OTG_FAULT_STAT	0	R	VBUS OVP or UVP, or PMID UVP, or BAT UVP during OTG Status Bit 0 = Normal (default) 1 = In VBUS OVP or UVP, or PMID UVP, or BAT UVP during OTG	N/A
D[3]	TSHUT_STAT	0	R	IC Temperature Shutdown Status Bit 0 = Normal (default) 1 = In thermal shutdown	N/A
D[2:0]	TS_STAT[2:0]	000	R	TS Status Bits Based on Battery NTC Temperature Measurement 000 = NORMAL (default) 001 = COLD 010 = HOT 011 = COOL (Buck mode only) 100 = WARM (Buck mode only) 101 = PRECOOL (Buck mode only) 110 = PREWARM (Buck mode only) 111 = Reserved	N/A

REGISTER MAPS (continued)

REG0x20: Charger Flag 0 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	Reserved	0	R	Reserved	N/A
D[6]	ADC_DONE_FLAG	0	RC	ADC Conversion Done Event Flag Bit(Only in One-Shot Mode) In one-shot conversion mode, this bit is set to 1 after ADC conversion of all enabled channels is completed. 0 = No ADC conversion done event (default) 1 = ADC conversion done event (the rising edge of ADC_DONE_STAT bit) has occurred. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0	N/A
D[5]	TREG_FLAG	0	RC	IC Thermal Regulation Event Flag Bit 0 = No IC thermal regulation event (default) 1 = IC thermal regulation event (the rising edge of TREG_STAT bit) has occurred. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0	N/A
D[4]	VSYS_FLAG	0	RC	VSYSMIN Regulation Status Change Event Flag Bit 0 = No VSYSMIN regulation status change event (default) 1 = VSYSMIN regulation status change event (VSYS_STAT bit) has occurred. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0	N/A
D[3]	IINDPM_FLAG	0	RC	IINDPM or IOTG Regulation Event Flag Bit 0 = No IINDPM or IOTG regulation event (default) 1 = IINDPM or IOTG regulation event (the rising edge of IINDPM_STAT bit) has occurred. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0	N/A
D[2]	VINDPM_FLAG	0	RC	VINDPM Regulation Event Flag Bit 0 = No VINDPM regulation event (default) 1 = VINDPM regulation event (the rising edge of VINDPM_STAT bit) has occurred. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0	N/A
D[1]	SAFETY_TMR_FLAG	0	RC	Fast Charge, Trickle Charge and Pre-Charge Timer Expires Event Flag Bit 0 = No fast charge, trickle charge and pre-charge timer expires event (default) 1 = Fast charge, trickle charge and pre-charge timer expires event (the rising edge of SAFETY_TMR_STAT bit) has occurred. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0	N/A
D[0]	WD_FLAG	0	RC	I²C Watchdog Timer Expires Event Flag Bit 0 = No I²C watchdog timer expires event (default) 1 = I²C watchdog timer expires event (the rising edge of WD_STAT bit) has occurred. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0	N/A

REGISTER MAPS (continued)

REG0x21: Charger Flag 1 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	Termination Current Range	0	R/W	ITERM Range Select in Charge Mode 0 = ITERM[6:0] (default) 1 = ITERM[6:0] × 2	REG_RST
D[6]	Pre-Charge Current Range	0	R/W	Pre-Charge Range Select in Charge Mode 0 = IPRECHG[5:0] (default) 1 = IPRECHG[5:0] × 2	REG_RST
D[5]	OTG_OVP	0	R/W	Boost Over-Voltage Threshold on VBUS Voltage Sense 0 = 10.55V (default) 1 = 6V	REG_RST
D[4]	DEPLETION_DEG	0	R/W	Battery Depletion Falling Edge Deglitch Time 0 = No deglitch time (default) 1 = 64ms	REG_RST
D[3]	CHG_FLAG	0	RC	Charge Status Change Event Flag Bit 0 = No charge status change event (default) 1 = Charge status change event (CHG_STAT[1:0] bits) has occurred. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0	N/A
D[2:1]	VBUS_OVP[1:0]	00	R/W	VBUS Over-Voltage Protection Threshold Setting 00 = 18.5V (default) 01 = 14V 10 = 10.5V 11 = 6.5V	REG_RST
D[0]	VBUS_FLAG	0	RC	VBUS Status Change Event Flag Bit 0 = No VBUS status change event (default) 1 = VBUS status change event (VBUS_STAT[2:0] bits) has occurred. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0	N/A

REGISTER MAPS (continued)

REG0x22: FAULT Flag 0 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	VBUS_FAULT_FLAG	0	RC	VBUS OVP or Sleep except for OTG Mode Fault Flag Bit 0 = No VBUS OVP or sleep except for OTG mode fault (default) 1 = VBUS OVP or sleep except for OTG mode fault (the rising edge of VBUS_FAULT_STAT bit) has occurred. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0	N/A
D[6]	BAT_FAULT_FLAG	0	RC	BAT OCP or OVP Fault Flag Bit 0 = No BAT OCP or OVP fault (default) 1 = BAT OCP or OVP fault (the rising edge of BAT_FAULT_STAT bit) has occurred. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0	N/A
D[5]	SYS_FAULT_FLAG	0	RC	SYS SCP or OVP Fault Flag Bit 0 = No SYS SCP or OVP fault (default) 1 = SYS SCP or OVP fault (the rising edge of SYS_FAULT_STAT bit) has occurred. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0	N/A
D[4]	OTG_FAULT_FLAG	0	RC	VBUS OVP or UVP, or PMID UVP, or BAT UVP during OTG Fault Flag Bit 0 = No VBUS OVP or UVP, or PMID UVP, or BAT UVP during OTG fault (default) 1 = VBUS OVP or UVP, or PMID UVP, or BAT UVP fault (the rising edge of OTG_FAULT_STAT bit) has occurred. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0	N/A
D[3]	TSHUT_FLAG	0	RC	IC Thermal Shutdown Fault Flag Bit 0 = No IC thermal shutdown fault (default) 1 = IC thermal shutdown fault (the rising edge of TSHUT_STAT bit) has occurred. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0	N/A
D[2:1]	Reserved	00	R	Reserved	N/A
D[0]	TS_FLAG	0	RC	TS Status Change Event Flag Bit 0 = No TS status change event (default) 1 = TS status change event (TS_STAT[2:0] bits) has occurred. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0	N/A

REGISTER MAPS (continued)

REG0x23: Charger Mask 0 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	Reserved	0	R/W	Reserved	N/A
D[6]	ADC_DONE_MASK	0	R/W	Mask ADC Conversion Done Event Interrupt (Only in One-Shot Mode) 0 = ADC conversion done event interrupt can work (default) 1 = Mask ADC conversion done event interrupt. The ADC_DONE_FLAG bit is set after the event, but the interrupt signal is not generated	REG_RST
D[5]	TREG_MASK	0	R/W	Mask IC Thermal Regulation Event Interrupt 0 = IC thermal regulation event interrupt can work (default) 1 = Mask IC thermal regulation event interrupt. The TREG_FLAG bit is set after the event, but the interrupt signal is not generated	REG_RST
D[4]	VSYS_MASK	0	R/W	Mask VSYSMIN Regulation Event Interrupt 0 = VSYSMIN regulation event interrupt can work (default) 1 = Mask VSYSMIN regulation event interrupt. The VSYS_FLAG bit is set after the event, but the interrupt signal is not generated	REG_RST
D[3]	IINDPM_MASK	0	R/W	Mask IINDPM or IOTG Regulation Event Interrupt 0 = IINDPM or IOTG regulation event interrupt can work (default) 1 = Mask IINDPM or IOTG regulation event interrupt. The IINDPM_FLAG bit is set after the event, but the interrupt signal is not generated	REG_RST
D[2]	VINDPM_MASK	0	R/W	Mask VINDPM Regulation Event Interrupt 0 = VINDPM regulation event interrupt can work (default) 1 = Mask VINDPM regulation event interrupt. The VINDPM_FLAG bit is set after the event, but the interrupt signal is not generated	REG_RST
D[1]	SAFETY_TMR_MASK	0	R/W	Mask Fast Charge, Trickle Charge and Pre-Charge Timer Expired Event Interrupt 0 = Fast charge, trickle charge or pre-charge timer expired event Interrupt can work (default) 1 = Mask Fast charge, trickle charge or pre-charge timer expired event Interrupt. The SAFETY_TMR_FLAG bit is set after the event, but the interrupt signal is not generated	REG_RST
D[0]	WD_MASK	0	R/W	Mask I²C Watchdog Timer Expired Event Interrupt 0 = I²C watchdog timer expired event interrupt can work (default) 1 = Mask I²C watchdog timer expired event interrupt. The WD_FLAG bit is set after the event, but the interrupt signal is not generated	REG_RST

REGISTER MAPS (continued)

REG0x24: Charger Mask 1 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	EN_VBUS_PD	0	R/W	Enable the VBUS 2kΩ Pull-Down Resistor 0 = Disable the VBUS pull-down resistor (default) 1 = Enable the VBUS pull-down resistor	REG_RST
D[6:4]	Reserved	000	R/W	Reserved	REG_RST
D[3]	CHG_MASK	0	R/W	Mask Charge Status Change Event Interrupt 0 = Charge status change event interrupt can work (default) 1 = Mask Charge status change event interrupt. The CHG_FLAG bit is set after the event, but the interrupt signal is not generated	REG_RST
D[2]	Reserved	0	R/W	Reserved	REG_RST
D[1]	VBUS_SINK_DIS	0	R/W	Disable the VBUS Sink during Poor Power Source Detection 0 = Enable the 10mA VBUS sink with 30ms (default) 1 = Disable the VBUS sink	REG_RST
D[0]	VBUS_MASK	0	R/W	Mask VBUS Status Change Event Interrupt 0 = VBUS status change event interrupt can work (default) 1 = Mask VBUS status change event interrupt. The VBUS_FLAG bit is set after the event, but the interrupt signal is not generated	REG_RST

REG0x25: FAULT Mask 0 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	VBUS_FAULT_MASK	0	R/W	Mask VBUS OVP or Sleep Fault Interrupt 0 = VBUS OVP or sleep fault interrupt can work (default) 1 = Mask VBUS OVP or sleep fault interrupt. The VBUS_FAULT_FLAG bit is set after the event, but the interrupt signal is not generated	REG_RST
D[6]	BAT_FAULT_MASK	0	R/W	Mask BAT OCP or BAT OVP Fault Interrupt 0 = BAT OCP or OVP fault interrupt can work (default) 1 = Mask BAT OCP or OVP fault interrupt. The BAT_FAULT_FLAG bit is set after the event, but the interrupt signal is not generated.	REG_RST
D[5]	SYS_FAULT_MASK	0	R/W	Mask SYS SCP or OVP Fault Interrupt 0 = SYS SCP or OVP fault interrupt can work (default) 1 = Mask SYS SCP or OVP fault interrupt. The SYS_FAULT_FLAG bit is set after the event, but the interrupt signal is not generated	REG_RST
D[4]	OTG_FAULT_MASK	0	R/W	Mask VBUS OVP or UVP, or PMID UVP, or BAT UVP during OTG Fault Interrupt 0 = VBUS OVP or UVP, or PMID UVP, or BAT UVP during OTG fault interrupt can work (default) 1 = Mask VBUS OVP or UVP, or PMID UVP, or BAT UVP during OTG fault interrupt. The OTG_FAULT_FLAG bit is set after the event, but the interrupt signal is not generated	REG_RST
D[3]	TSHUT_MASK	0	R/W	Mask IC Thermal Shutdown Fault Interrupt 0 = IC thermal shutdown fault interrupt can work (default) 1 = Mask IC thermal shutdown fault interrupt. The TSHUT_FLAG bit is set after the event, but the interrupt signal is not generated	REG_RST
D[2:1]	Reserved	00	R	Reserved	N/A
D[0]	TS_MASK	0	R/W	Mask TS Status Change Event Interrupt 0 = TS status change event interrupt can work (default) 1 = Mask TS status change event interrupt. The TS_FLAG bit is set after the event, but the interrupt signal is not generated	REG_RST

REGISTER MAPS (continued)

REG0x26: ADC Control Register [Reset = 0x30]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	EN_ADC	0	R/W	ADC Control 0 = Disable (default) 1 = Enable The bit stays '1' during ADC conversion when ADC_RATE = 0. The bit resets to '0' after ADC conversion has done when ADC_RATE = 1. If all ADC are disabled (REG0x27), the EN_ADC bit will be cleared. All registers of ADC report are set to all 0 after POR, then always remain the last measurement result, and never clear.	REG_RST or Watchdog
D[6]	ADC_RATE	0	R/W	ADC Conversion Mode Control 0 = Continuous conversion (default) 1 = One-shot conversion	REG_RST
D[5:4]	ADC_SAMPLE[1:0]	11	R/W	ADC Sample Speed 00 = 12-bit effective resolution 01 = 11-bit effective resolution 10 = 10-bit effective resolution 11 = 9-bit effective resolution (default)	REG_RST
D[3]	ADC_AVG	0	R/W	ADC Average Control 0 = Single value (default) 1 = Running average	REG_RST
D[2]	ADC_AVG_INIT	0	R/W	ADC Average Initial Value Control 0 = Start average using the existing register value (default) 1 = Start average using a new ADC conversion	REG_RST
D[1:0]	Reserved	00	R	Reserved	N/A

REG0x27: ADC Function Disable 0 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	IBUS_ADC_DIS	0	R/W	IBUS ADC Control 0 = Enable (default) 1 = Disable	REG_RST
D[6]	IBAT_ADC_DIS	0	R/W	IBAT ADC Control 0 = Enable (default) 1 = Disable	REG_RST
D[5]	VBUS_ADC_DIS	0	R/W	VBUS ADC Control 0 = Enable (default) 1 = Disable	REG_RST
D[4]	VBAT_ADC_DIS	0	R/W	VBAT ADC Control 0 = Enable (default) 1 = Disable	REG_RST
D[3]	VSYS_ADC_DIS	0	R/W	VSYS ADC Control 0 = Enable (default) 1 = Disable	REG_RST
D[2]	TS_ADC_DIS	0	R/W	TS ADC Control 0 = Enable (default) 1 = Disable	REG_RST
D[1]	TDIE_ADC_DIS	0	R/W	TDIE ADC Control 0 = Enable (default) 1 = Disable	REG_RST
D[0]	VPMID_ADC_DIS	0	R/W	VPMID ADC Control 0 = Enable (default) 1 = Disable	REG_RST

REGISTER MAPS (continued)

REG0x28: IBUS_ADC Register [Reset = 0x0000]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[15:1]	IBUS_ADC[14:0]	000 0000 0000 0000	R	IBUS ADC Reading I_{BUS_ADC} = ±2n (mA) Offset: 0mA Bit step: 2mA Range: -4000mA (111 1000 0011 0000) - 4000mA (000 0111 1101 0000) The most significant bit represents the sign bit. IBUS ADC reports positive value when the current flows from VBUS to PMID, and reports negative value when the current flow from PMID to VBUS.	N/A
D[0]	Reserved	0	R	Reserved	N/A

REG0x2A: IBAT_ADC Register [Reset = 0x0000]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[15:2]	IBAT_ADC[13:0]	00 0000 0000 0000	R	IBAT ADC Reading I_{BAT_ADC} = ±4n (mA) Offset: 0mA Bit step: 4mA Range: -7500mA (11 1000 1010 1101) - 4000mA (00 0011 1110 1000) The most significant bit represents the sign bit. The IBAT ADC reports positive value when charging, and report negative value when discharging. The IBAT ADC resets to zero when EN_CHG bit is 0.	N/A
D[1:0]	Reserved	00	R	Reserved	N/A

REG0x2C: VBUS_ADC Register [Reset = 0x0000]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[15]	Reserved	0	R	Reserved	N/A
D[14:2]	VBUS_ADC[12:0]	0 0000 0000 0000	R	VBUS ADC Reading V_{BUS_ADC} = 4n (mV) Offset: 0mV Bit Step: 4mV Range: 0mV (0 0000 0000 0000) - 20000mV (1 0011 1000 1000)	N/A
D[1:0]	Reserved	00	R	Reserved	N/A

REG0x2E: VPMID_ADC Register [Reset = 0x0000]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[15]	Reserved	0	R	Reserved	N/A
D[14:2]	VPMID_ADC[12:0]	0 0000 0000 0000	R	VPMID ADC Reading V_{PMID_ADC} = 4n (mV) Offset: 0mV Bit Step: 4mV Range: 0mV (0 0000 0000 0000) - 20000mV (1 0011 1000 1000)	N/A
D[1:0]	Reserved	00	R	Reserved	N/A

REGISTER MAPS (continued)

REG0x30: VBAT_ADC Register [Reset = 0x0000]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[15:13]	Reserved	000	R	Reserved	N/A
D[12:1]	VBAT_ADC[11:0]	0000 0000 0000	R	VBAT ADC Reading V_{BAT_ADC} = 2n (mV) Offset: 0mV Bit Step: 2mV Range: 0mV (0000 0000 0000) - 5600mV (1010 1111 0000)	N/A
D[0]	Reserved	0	R	Reserved	N/A

REG0x32: VSYS_ADC Register [Reset = 0x0000]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[15:13]	Reserved	000	R	Reserved	N/A
D[12:1]	VSYS_ADC[11:0]	0000 0000 0000	R	VSYS ADC Reading V_{SYS_ADC} = 2n (mV) Offset: 0mV Bit Step: 2mV Range: 0mV (0000 0000 0000) - 5600mV (1010 1111 0000)	N/A
D[0]	Reserved	0	R	Reserved	N/A

REG0x34: TS_ADC Register [Reset = 0x0000]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[15:12]	Reserved	0000	R	Reserved	N/A
D[11:0]	TS_ADC[11:0]	0000 0000 0000	R	The percentage of TS voltage compared to bias reference. TS_ADC = 0.09635n (%) Offset: 0% Bit Step: 0.09635% Range: 0% (0000 0000 0000) - 98.567% (0011 1111 1111)	N/A

REG0x36: TDIE_ADC Register [Reset = 0x0000]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[15:12]	Reserved	0000	R	Reserved	N/A
D[11:0]	TDIE_ADC[11:0]	0000 0000 0000	R	TDIE ADC Reading T_{DIE_ADC} = 0.5n (℃) Offset: 0℃ Bit Step: 0.5℃ Range: -40℃ (1111 1011 0000) - 150℃ (0001 0010 1100) The most significant bit represents the sign bit.	N/A

REG0x38: Part Information Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:6]	Reserved	00	R	Reserved	N/A
D[5:3]	PN[2:0]	000	R	Device Part Number 000 = SGM41551	N/A
D[2:0]	DEV_REV[2:0]	000	R	Revision	N/A

APPLICATION INFORMATION

The SGM41551 is typically used as a charger with power path management in smart phones, tablets and other portable devices. In the design, it comes along with a host controller (a processor with I²C interface) and a single-cell Li-Ion or Li-polymer battery.

Detailed Design Procedure

Inductor Design

Small energy storage elements (inductor and capacitor) can be used due to the high frequency (1.5MHz) switching converter used in the SGM41551. Inductor should tolerate currents higher than the maximum charge current (I_{CHG}) plus half the inductor peak to peak ripple current (ΔI) without saturation:

$$I_{SAT} > I_{CHG} + \frac{\Delta I}{2} \quad (3)$$

The inductor ripple current is determined by the input voltage (V_{VBUS}), duty cycle ($D = V_{BAT}/V_{VBUS}$), switching frequency (f_S = 1.5MHz) and the inductance (L). In CCM:

$$\Delta I = \frac{V_{VBUS} \times D \times (1-D)}{f_S \times L} \quad (4)$$

Inductor ripple current is maximum when D ≈ 0.5. In the practical designs, inductor peak to peak current ripple is selected in a range from 20% to 40% of the maximum DC current $\Delta I = (0.2 \sim 0.4) \times I_{CHG}$ for a good trade-off between inductor size and efficiency. Selecting higher ripple allows choosing of smaller inductance.

For each application, V_{VBUS} and I_{CHG} are known, so L can be calculated from (4) and current rating of the inductor can be selected from (3). Choose an inductor that has small DCR and core losses at 1.5MHz to have high efficiency and cool operation at full load.

Input Capacitor Design

Select low ESR ceramic input capacitor (X7R or X5R) with sufficient voltage and RMS ripple current rating for decoupling of the input switching ripple current (I_{CIN}). The RMS ripple current in the worst case is around the $I_{CHG}/2$ when D ≈ 0.5. If the converter does not operate at D ≈ 50%, the worst case capacitor RMS current can be estimated from (5) in which D is the closest operating duty cycle to 0.5.

$$I_{CIN} = I_{CHG} \times \sqrt{D \times (1-D)} \quad (5)$$

For SGM41551, place C_{IN} across PMID and GND pins close to the chip. Voltage rating of the capacitor must be at least 25% higher than the normal input voltage to minimize voltage derating. For a 13.5V input voltage, the preferred rating is 25V or higher.

A C_{IN} ≥ 10μF is suggested.

Output Capacitor Design

The output capacitance (on the system) must have enough RMS (ripple) current rating to carry the inductor switching ripple and provide enough energy for system transient current demands. I_{COUT} (C_{OUT} RMS current) can be calculated by:

$$I_{COUT} = \frac{I_{RIPPLE}}{2 \times \sqrt{3}} \approx 0.29 \times I_{RIPPLE} \quad (6)$$

And the output voltage ripple can be calculated by:

$$\Delta V_O = \frac{V_{OUT}}{8LC_{OUT}f_S^2}\left(1 - \frac{V_{OUT}}{V_{VBUS}}\right) \quad (7)$$

Increasing L or C_{OUT} (the LC filter) can reduce the ripple. The internal loop compensation of the device is optimized for > 20μF ceramic output capacitor. 10V, X7R (or X5R) ceramic capacitors are recommended for the output.

Input Power Supply Considerations

To power the system from the SGM41551, either an input power source with a voltage range from 3.9V to 16V and at least 100mA current rating should power VBUS, or a single-cell Li-Ion battery with voltage higher than V_{BAT_UVLOZ} should be connected to BAT pin of the device. The input source must have enough current rating to allow maximum power delivery through charger (Buck converter) to the system.

Layout Guidelines

The switching node (SW) creates very high frequency noises, which are several times higher than f_{SW} (1.5MHz) due to sharp rise and fall times of the voltage and current in the switches. To reduce the ringing issues and noise generation, it is important to design a proper layout for minimizing the current path impedance and loop area. The reference layout is shown in Figure 18.

1. Place the input capacitor between PMID and GND pins as close as possible to the chip with the shortest copper connections (avoid vias). Choose the smallest capacitor size.

APPLICATION INFORMATION (continued)

2. Connect one pin of the inductor as close as possible to the SW pin of the device and minimize the copper area connected to the SW node to reduce capacitive coupling from SW area to nearby signal traces. This decreases the noise induced through parasitic stray capacitances and displacement currents to other conductors. SW connection should be wide enough to carry the charging current. Keep other signals and traces away from SW if possible.

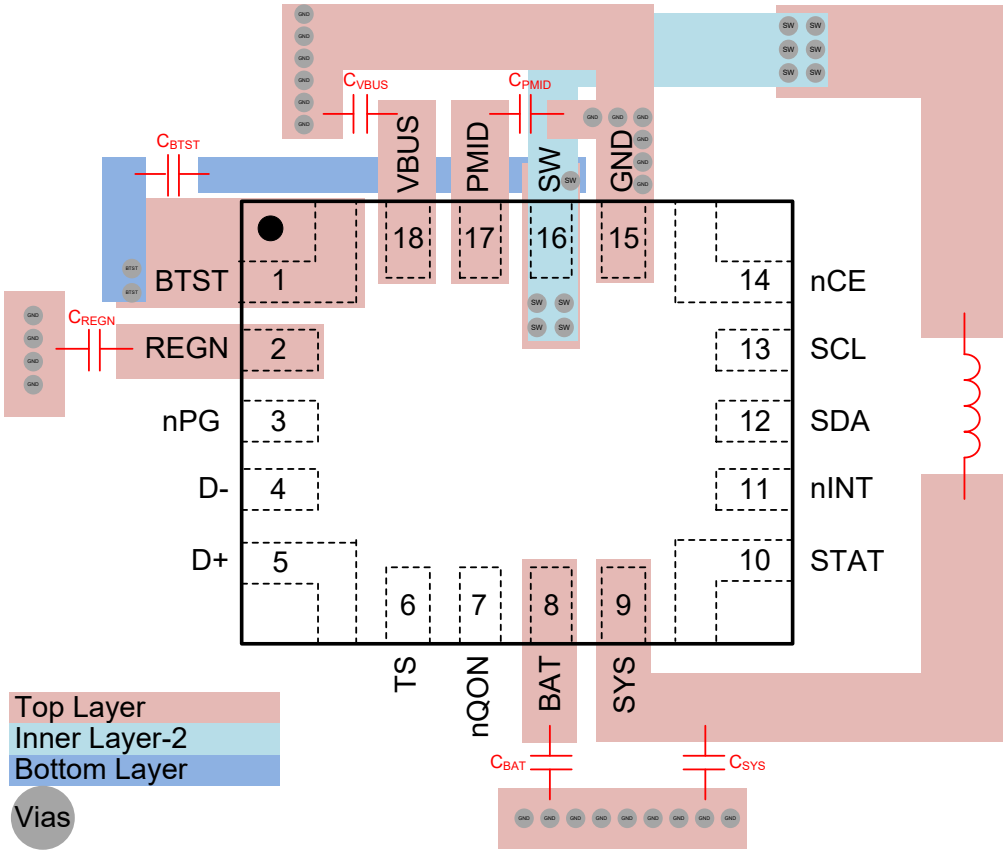
3. Place output capacitor GND pin as close as possible to the GND pin of the device and the GND pin of input capacitor C_{IN}. It is better to avoid using vias for these connections and keep the high frequency current paths short enough and on the same layer. A GND copper layer under the component layer helps to reduce noise emissions. Pay attention to the DC current and AC current paths in the layout and keep them short and decoupled as much as possible.

4. For analog signals, it is better to use a separate analog ground (AGND) branched only at one point from GND pin. To avoid high current flow through the AGND path, it should be connected to GND only at one point (preferably the GND pin).

5. Place decoupling capacitors close to the IC pins with the shortest copper connections.

6. Solder the exposed thermal pad of the package to the PCB ground planes. Ensure that there are enough thermal vias directly under the IC, connecting to the ground plane on the other layers for better heat dissipation and cooling of the device.

7. Select proper sizes for the vias and ensure enough copper is available to carry the current for the given current path. Vias usually have some considerable parasitic inductance and resistance.



NOTES:

1. The layout example is actually a board with 4 layers. The inner layer-1 is a GND copper layer and not shown in the figure.

2. Only the critical circuit path layout is shown for reference, and other heat dissipation planes and vias are not shown in the figure. For more detailed information, please refer to the SGM41551 evaluation kit on www.sg-micro.com.

Figure 18. Reference Layout

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

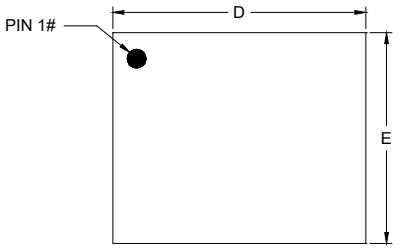
APRIL 2026 – REV.A.1 to REV.A.2	Page
Updated Detailed Description section	27, 29
Updated Register Maps section	40, 41, 53

FEBRUARY 2026 – REV.A to REV.A.1	Page
Updated Electrical Characteristics section	8
Updated Register Maps section	37, 55

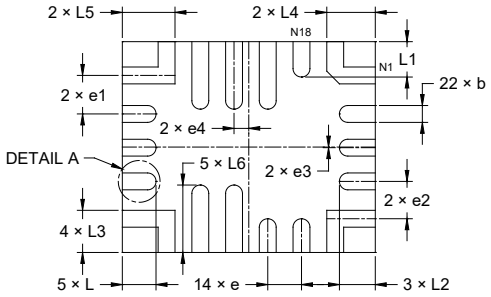
Changes from Original to REV.A (DECEMBER 2025)	Page
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

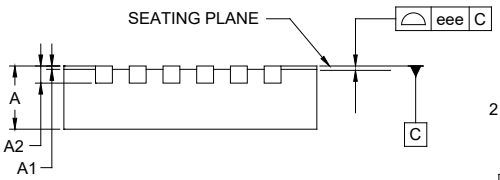
TQFN-3×2.5-18L



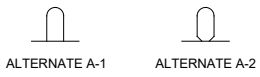
TOP VIEW



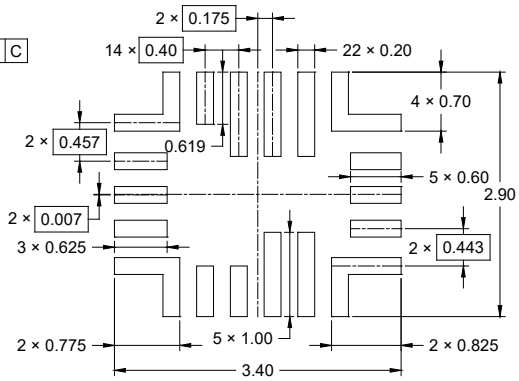
BOTTOM VIEW



SIDE VIEW



DETAIL A
ALTERNATE TERMINAL CONSTRUCTION



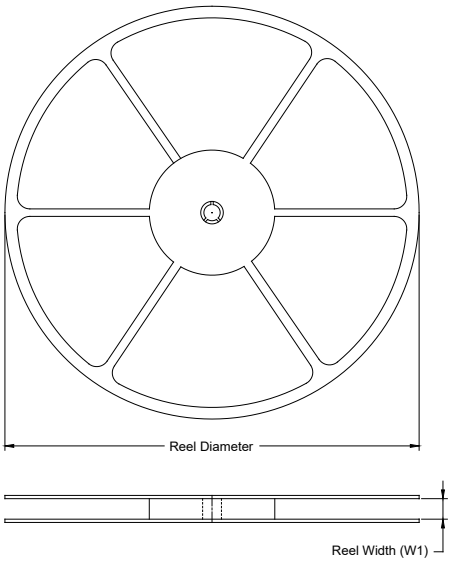
RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	0.700	-	0.800
A1	0.000	-	0.050
A2		0.203 REF	
b	0.150	-	0.250
D	2.900	-	3.100
E	2.400	-	2.600
e		0.400 BSC	
e1		0.457 BSC	
e2		0.443 BSC	
e3		0.007 BSC	
e4		0.175 BSC	
L	0.300	-	0.500
L1	0.319	-	0.519
L2	0.325	-	0.525
L3	0.400	-	0.600
L4	0.475	-	0.675
L5	0.525	-	0.725
L6	0.700	-	0.900
eee		0.080	

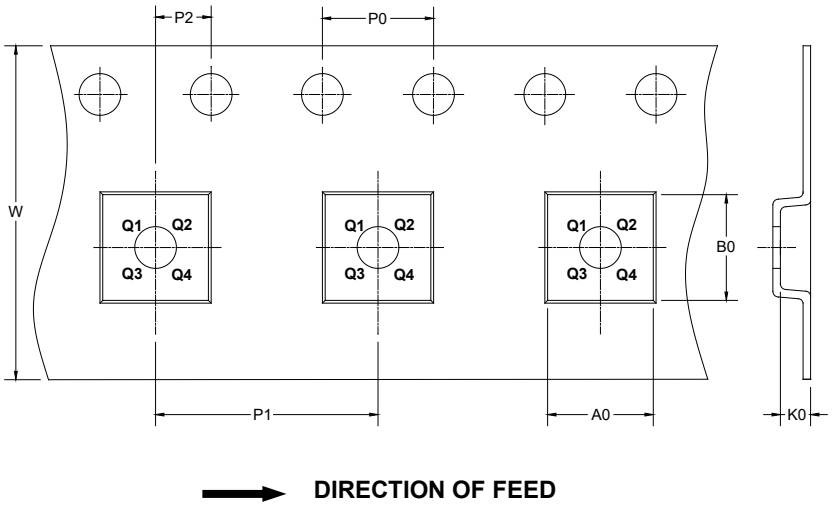
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



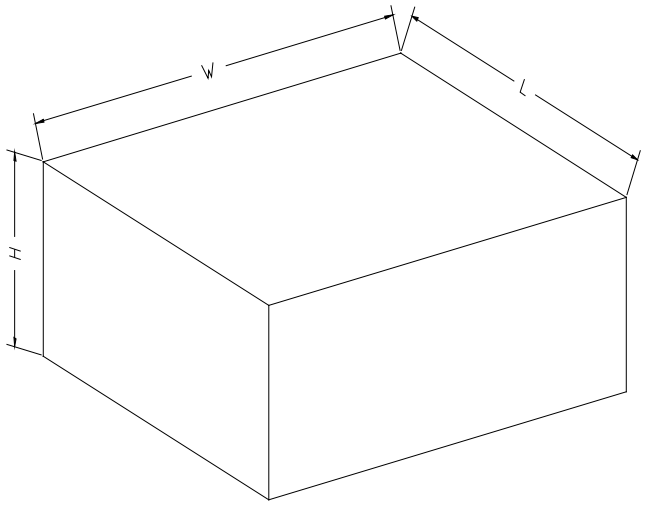
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TQFN-3×2.5-18L	7″	12.4	2.75	3.25	1.00	4.0	4.0	2.0	12.0	Q2

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18

DD0002