TDT5111

I²C and I3C Serial Interface Temperature Sensors Compatible with JEDEC JESD302-1A for DDR5

GENERAL DESCRIPTION

The TDT5111 (TS5) devices incorporate high accuracy thermal sensing capability which is controlled and read over two-wire bus. The TS5 device operates from a 1.8V nominal power supply (VDDSPD) and a 1.0V nominal power supply (VDDIO). The TS5 device is compatible with JEDEC JESD302-1A standard and is intended to operate up to 12.5MHz on a 1.0V I3C Basic bus or up to 1MHz on a 1.0V to 3.3V I²C bus. The TS5 device is intended to interface to I²C or I3C Basic bus which has multiple devices on a shared bus, and must be uniquely addressed with fixed addressing on the same bus. All TS5 devices respond to specific pre-defined device select codes on the two-wire bus.

The TS5 is an important component of the DDR5 server DIMMs. The current mainstream DIMMs are expected to be equipped with two TS5 chips per DIMM.

The TDT5111 is available in a Green WLCSP-0.81×1.31-6B package.

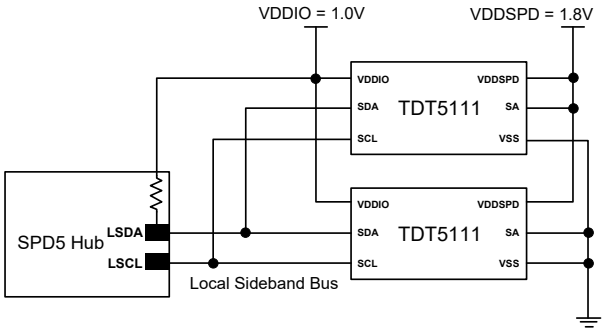
FEATURES

- **TS5 Device, JEDEC JESD302-1A Compliant**
- **Two-wire Programmable I²C or I3C Basic Bus Serial Interface**
- **Up to 12.5MHz Transfer Rate**
- **Power Supply: 1.8V VDDSPD, 1.0V VDDIO**
- **Supports 1.0V, 1.1V and 1.2V Push Pull I/O Levels**
- **Supports 1.0V, 1.1V, 1.2V, 1.8V, 2.5V and 3.3V Open Drain I/O Levels**
- **Integrated Temperature Sensor: 0.5℃ Accuracy with 0.25℃ Resolution**
- **Packet Error Check (PEC) Function**
- **Parity Error Check Function**
- **Bus Reset Function**
- **Two Unique Addresses Selected by SA Pin**
- **In Band Interrupt (IBI)**
- **Operating Temperature Range: -40℃ to +125℃**
- **Available in a Green WLCSP-0.81×1.31-6B Package**

APPLICATIONS

DDR5 DIMM Modules
PC, Server Platforms
Industrial Temperature Monitors

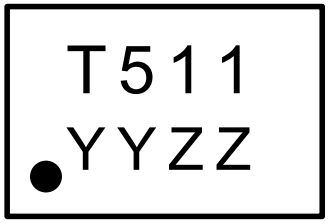
SIMPLIFIED SCHEMATIC



PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
TDT5111	WLCSP-0.81×1.31-6B	-40℃ to +125℃	TDT5111-C6LPTR	T511 YYZZ	Tape and Reel, 4000

PACKAGE MARKING INFORMATION



T511: TDT5111-C6LP

YYZZ: Date Code, YY = year, ZZ = week

Example: 2416 = year 2024, week 16

Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{DDIO} ..... -0.5V to 2.1V
Supply voltage, V_{DDSPD} ..... -0.5V to 2.1V
Voltage on SA Pin, V_{HSA} ..... -0.5V to 2.1V
Voltage on SCL, SDA Pins $V_{SCL, SDA}$ ..... -0.5V to 3.6V
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility (1) (2)
HBM ..... ±2000V
CDM ..... ±1000V

NOTES:

1. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.

2. For charged device model (CDM), all pins comply with per JEDEC specification JESD22-C101 specifications.

RECOMMENDED OPERATING CONDITIONS

Input Supply Voltage (1), V_{DDSPD} ..... 1.8V (TYP)
Input Supply Voltage (1), V_{DDSPD} ..... 1.7V to 1.98V
Input Supply Voltage (2), V_{DDIO} ..... 1.0V (TYP)
Input Supply Voltage (2), V_{DDIO} ..... 0.95V to 1.05V
Operating Ambient Temperature Range ..... -40℃ to +125℃

NOTES:

1. For DDR5 DIMM application, the DDR5 PMIC VOUT_1.8V setting should be selected such that absolute MIN and MAX values for SPD Hub specification are not violated.

2. For DDR5 DIMM application, the DDR5 PMIC VOUT_1.0V setting should be selected such that absolute MIN and MAX values for SPD Hub specification are not violated.

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

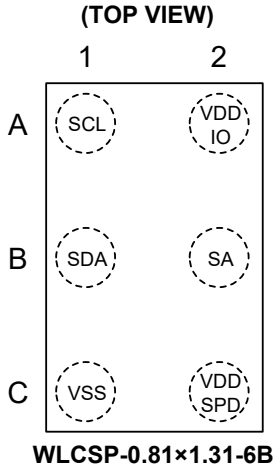
ESD SENSITIVITY CAUTION

This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION



WLCSP-0.81×1.31-6B

PIN DESCRIPTION

PIN	NAME	TYPE	FUNCTION
C2	VDDSPD	P	1.8V Input Power Supply. Connect minimum of 1.0μF capacitor to VSS.
C1	VSS	G	GND
A1	SCL	I	I^2C/I3C Basic Input Clock
B1	SDA	I/O	I^2C/I3C Basic Data
B2	SA	I	I^2C/I3C Basic Address Pin. This pin is tied to either VSS or VDDSPD to establish the 4-bit LID.
A2	VDDIO	P	1.0V Input Power Supply. Connect minimum of 1.0μF capacitor to VSS.

NOTE: I = input, O = output, I/O = input/output, P = power, G = ground.

ELECTRICAL CHARACTERISTICS

Table 1. AC Measurement Conditions (1)

PARAMETER	SYMBOL	MIN	MAX	UNITS
Load Capacitance	C_L	40		pF
Input Rise And Fall Times - Open Drain			120	ns
Input Rise And Fall Times - Push Pull			5	ns
Input Signal Swing Levels		0.2 to 0.8		V
Input Levels For Timing Reference		0.3 to 0.7		V

NOTE:

1. This AC measurement condition (Table 1 and Figure 1) is only for the test purpose in lab.

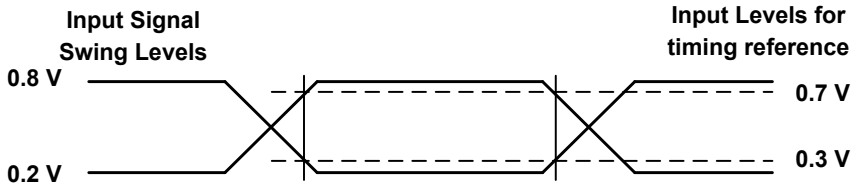


Figure 1. AC Measurement Waveform

Table 2. Input Parameters

PARAMETER (1) (2)	SYMBOL	CONDITIONS	MIN	MAX	UNITS
Input Capacitance (SDA, SCL)	C_{IN}	-	-	4	pF
Pulse width of spikes which must be suppressed by the input filter in I²C mode	t_{SP}	Single glitch, f ≤ 100kHz	-	-	ns
		Single glitch, f > 100kHz	0	50	ns

NOTES:

1. T_A = +25℃, f = 400kHz.
2. Verified by design and characterization, not necessarily tested on all devices.

Table 3. Output R_{ON} Specification

PARAMETER (1)	SYMBOL	MIN	MAX	UNITS
SDA Output Pull-Up and Pull-Down Driver Impedance	R_{ON}	40	100	Ω

NOTE:

1. Pull-Down $R_{ON} = V_{OUT}/I_{OUT}$; Pull-Up $R_{ON} = (V_{DDIO} - V_{OUT})/I_{OUT}$.

ELECTRICAL CHARACTERISTICS (continued)

DC Characteristics

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
Input Leakage Current	I_{LI}			± 5	μA
Output Leakage Current	I_{LO}			± 5	μA
Supply Current, Read Operation (1)	I_{DDR}	V_{DDSPD} = 1.8V, f_C = 12.5MHz		2	mA
Supply Current, Write Operation (1)	I_{DDW}	V_{DDSPD} = 1.8V, f_C = 12.5MHz		3	mA
Input Low Voltage	V_{IL}		-0.35	0.3	V
Input High Voltage	V_{IH}		0.7	3.6	V
Output Low Voltage	V_{OL}	3 mA sink current		0.3	V
Output High Voltage	V_{OH}	3 mA source current	0.75		V
Output Low Current (SDA)	I_{OL}	V_{OL} = 0.3V	-3		mA
Output High Current (SDA)	I_{OH}	V_{OH} = V_{DDIO} - 0.3V		-3	mA
Rising Output Slew Rate (SDA) (2)	Slew_Rate		0.1	1.0	V/ns
Falling Output Slew Rate (SDA) (2)			0.1	1.0	V/ns
Power On Reset Threshold	V_{PON}	Monotonic rise between V_{PON} and V_{DDSPD_MIN} without ringback	1.6		V
Power Off Threshold for Warm Power On Cycle	V_{POFF}	No ringback above V_{POFF}		0.3	V

NOTES:

1. Thermal sensor is active.
2. Output slew rate is guaranteed by design and / or characterization. The output slew rate reference load is shown in Figure 5 and Figure 6 shows the timing measurement points. For slew rate measurements, the V_{OH} level shown in Figure 6 is a function of R_{ON} value; V_{OH} = {1.0 / (R_{ON} + 50)} * 50.

AC Characteristics

PARAMETER	SYMBOL	I²C MODE – OPEN DRAIN		I3C Basic – Push-Pull (1)		UNITS
		MIN	MAX	MIN	MAX	
Clock Frequency	f_{SCL}	0.01	1	0	12.5	MHz
Clock Pulse Width High Time	t_{HIGH}	260		35		ns
Clock Pulse Width Low Time	t_{LOW}	500		35		ns
Detect Clock Low Timeout	$t_{TIMEOUT}$	10	50	10	50	ms
SDA Rise Time (2) (3)	t_R		120		5	ns
SDA Fall Time (2) (3)	t_F		120		5	ns
Data In Setup Time (2)	$t_{SU:DAT}$	50		8		ns
Data In Hold Time (2)	$t_{HD:DI}$	0		3		ns
Start Condition Setup Time (2)	$t_{SU:STA}$	260		12		ns
Start Condition Hold Time (2)	$t_{HD:STA}$	260		30		ns
Stop Condition Setup Time (2)	$t_{SU:STO}$	260		12		ns
Time between Stop Condition and next Start Condition (2) (4)	t_{BUF}	500		500		ns
Warm Power Cycle Off Time	t_{POFF}	1		1		ms
Time from Valid 1.8V Supply to Sense SA Pin for LID Code Assignment	t_{SENSE_SA}		5		5	ms
Time from Power On to First Command	t_{INIT}	10		10		ms
Bus Available Time (No Edges Seen on SDA and SCL)	t_{AVAL}			1		μs
Time to Issue IBI after an Event is Detected when Bus is Available	t_{IBI_ISSUE}				15	μs

ELECTRICAL CHARACTERISTICS (continued)

PARAMETER	SYMBOL	I²C MODE – OPEN DRAIN		I3C Basic – Push-Pull (1)		UNITS
		MIN	MAX	MIN	MAX	
Time from Clear Register Status to any I3C Operation with Start Condition to Avoid IBI Generation; PEC Disabled	$t_{CLR_I3C_CMD_DELAY}$			2.5		µs
Time from Clear Register Status to any I3C Operation with Start Condition to Avoid IBI Generation; PEC Enabled				15		µs
SCL Falling Clock In to HSDA Data Out Hold Time (5)	$t_{HD:DAT}$	0.5	350	N/A	N/A	ns
SCL Falling Clock In to HSDA Valid Data Out Time (6)	t_{DOUT}	N/A	N/A	0.5	12	ns
SCL Rising Clock In to SDA Output Off (7)	t_{DOFFT}	N/A	N/A	0.5	12	ns
SCL Rising Clock In to Controller SDA Output Off (8)	t_{DOFFC}	N/A	N/A	0.5	t_{HIGH}	ns
SCL Rising Clock In to Controller Driving SDA Signal Low (9)	$t_{CL_R_DAT_F}$	N/A	N/A	40		ns
DEVCTRL CCC Followed by DEVCTRL CCC or Register Read/Write Command Delay (10) (11) (12)	$t_{DEVCTRLCCC_DELAY_PEC_DIS}$	3		3		µs
Register Write Command Followed by Register Read Command Delay in PEC Enabled Mode (13) (14) (15)	$t_{WR_RD_DELAY_PEC_EN}$	N/A	N/A	8		µs
SETHID CCC or SETAASA CCC to any other CCC or Read/Write Command Delay	$t_{I2C_CCC_UPDATE_DELAY}$	2.5				µs
RSTDAA CCC or ENEC CCC or DISEC CCC to any other CCC or Read/Write Command Delay	$t_{I3C_CCC_UPDATE_DELAY}$			2.5		µs
Any CCC to RSTDAA CCC Delay	t_{CCC_DELAY}	N/A	N/A	2.5		µs

NOTES:

1. I3C mode with Open Drain operation follows timing values as shown in *I²C Mode - Open Drain* column.
2. See Figure 2 for input timing parameter definition.
3. See Figure 7 for voltage threshold definition for rise and fall times.
4. If PEC is enabled, $t_{WR_RD_DELAY_PEC_EN}$ timing parameter also applies.
5. See Figure 4 for output timing parameter definition.
6. The TS5 device must be in configured in I3C Basic mode to guarantee t_{DOUT} value. See Figure 3 for output timing parameter definition. See Figure 5 for output timing parameter measurement reference load.
7. The TS5 device must be configured in I3C Basic mode to guarantee t_{DOFFT} value. See Figure 10. See Figure 5 for output timing parameter measurement reference load. Also refer to MIPI Alliance Specification for *I3C Basic Version 1.0-19 July 2018, section 5.1.2.3.2, Transition from Address ACK to Mandatory Byte during IBI*.
8. The TS5 device must be configured in I3C Basic mode. The Host guarantees t_{DOFFC} value. See Figure 11. See Figure 5 for output timing parameter measurement reference load.
9. See Figure 14.
10. From Stop condition of DEVCTRL CCC to Start condition for Register Read or Register Write Command Data Packet delay.
11. The TS5 device may send ACK or NACK if Host does not satisfy $t_{DEVCTRLCCC_DELAY_PEC_DIS}$ timing parameter.
12. This timing parameter restriction is only applicable when PEC function is disabled in TS5. If PEC is enabled, this timing parameter does not apply.
13. From Stop condition for Register Write Command Data Packet to Start condition for Register Read Command Data Packet delay.
14. This timing parameter restriction is only applicable when PEC function is enabled in TS5. If PEC is disabled, this timing parameter does not apply.
15. The TS5 device may send ACK or NACK if Host does not satisfy $t_{WR_RD_DELAY_PEC_EN}$ timing parameter.

Temperature Sensor Performance

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
Temperature Sensor Accuracy (Active Range)	T_{ACC}	+75℃ ≤ T_A ≤ +95℃	-	±0.5	±1.0	℃
Temperature Sensor Accuracy (Monitor Range)		+40℃ ≤ T_A ≤ +125℃	-	±1.0	±2.0	℃
Temperature Sensor Accuracy (Industrial Temperature Range)		-40℃ ≤ T_A ≤ +125℃	-	±2.0	±3.0	℃
Temperature Sensor Resolution	R_{TS}			0.25		℃
Conversion Time	t_{CONV}	Assumes 0.25 ℃ accuracy			68	ms
Hysteresis between temperature events	T_{HYST}		1	-	-	℃

AC TIMING DEFINITION

I²C or I3C Basic Bus Timing

The TS5 device follows the I²C or I3C Basic bus timing requirements. The Figure 2 and Figure 3 show the timing diagram for Data Bus Input and Data Output parameters.

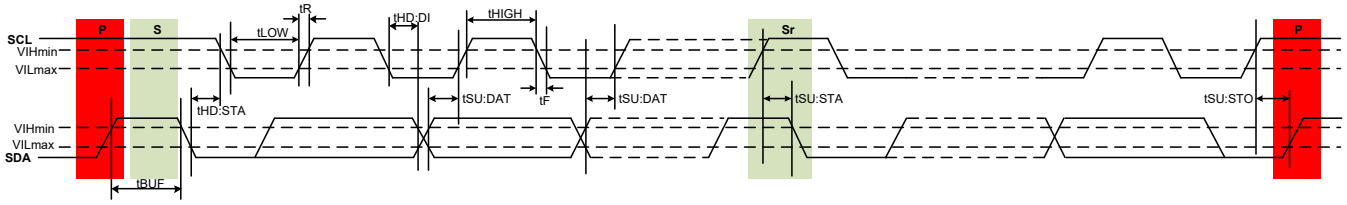


Figure 2. I²C or I3C Basic Bus AC Input Timing Parameter Definition

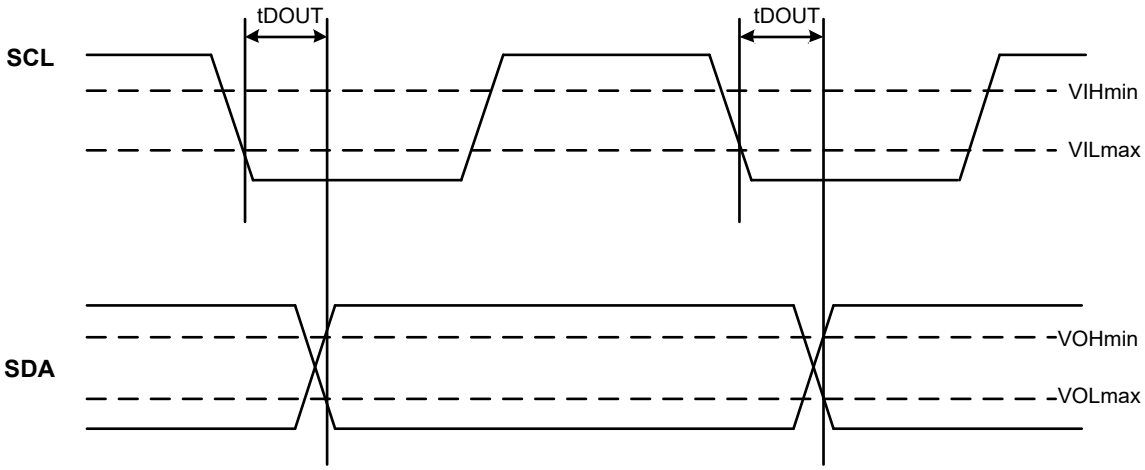


Figure 3. I3C Basic Bus AC Data Output Timing Parameter Definition

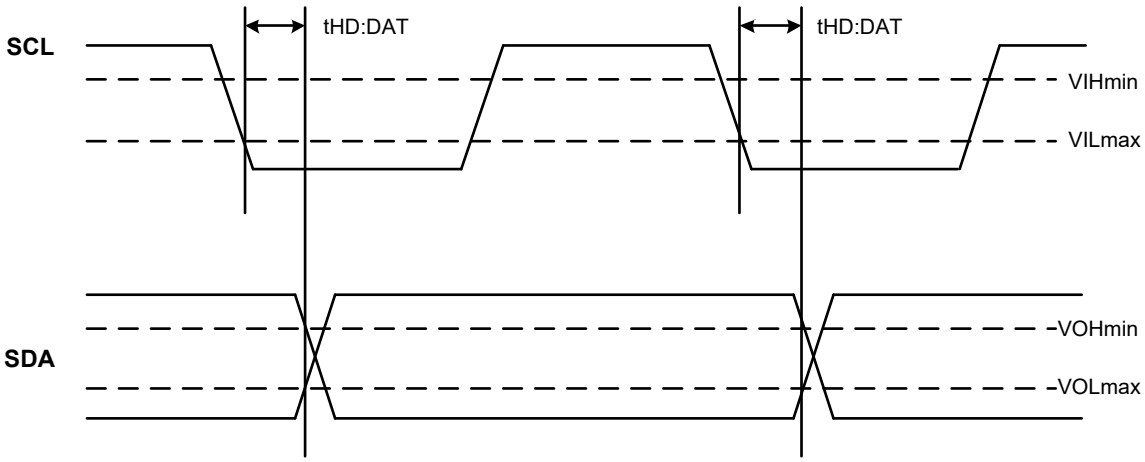


Figure 4. I²C Bus AC Data Output Timing Parameter Definition

AC TIMING DEFINITION (continued)

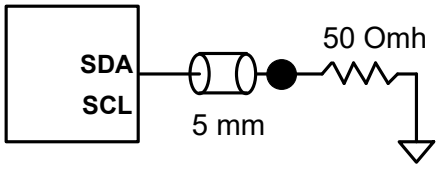


Figure 5. Output Slew Rate and Output Timing Reference Load

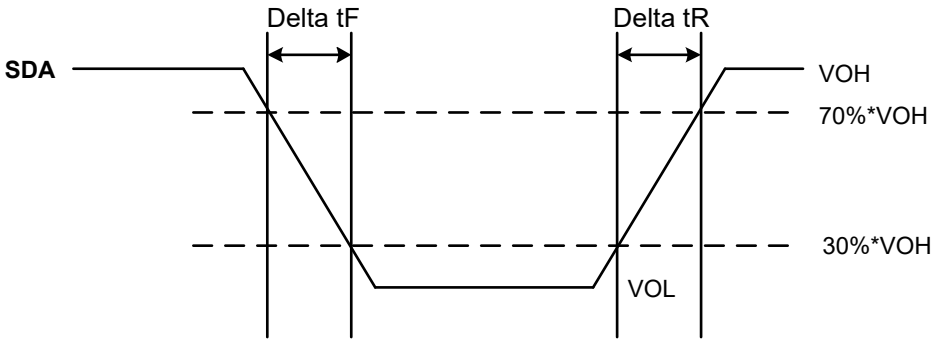


Figure 6. Output Slew Rate Measurement Points

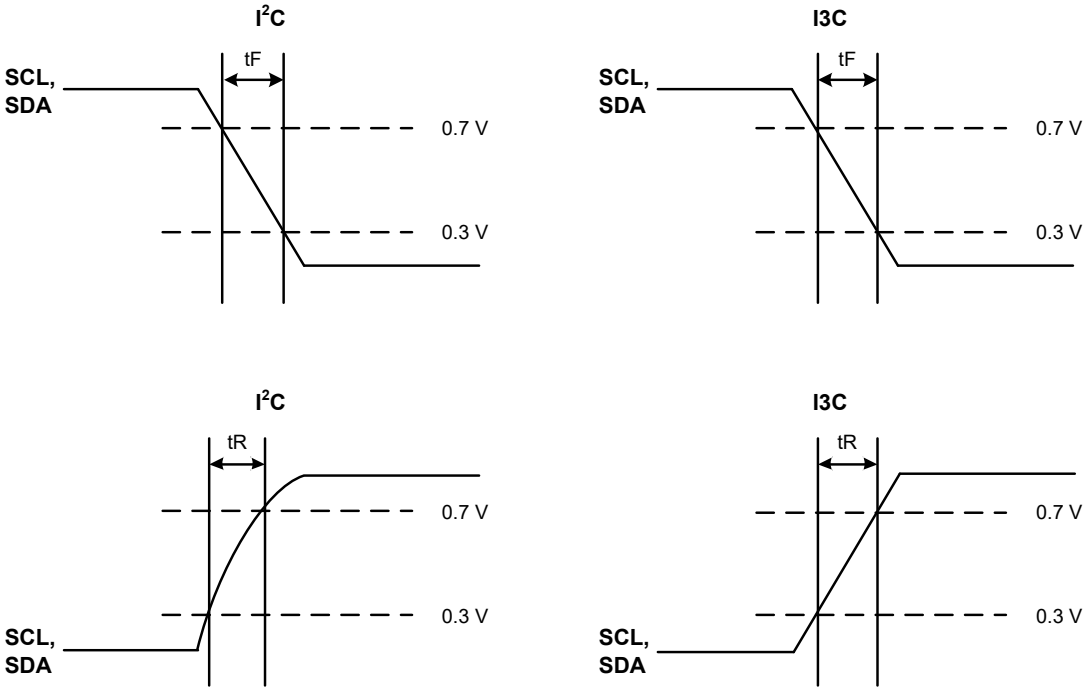


Figure 7. Rise and Fall Timing Parameter Definition

DETAILED DESCRIPTION

Device Power Up

The TS5 device has one VDDSPD supply input and one VDDIO supply input.

In order to prevent inadvertent operations during power up, a Power-On Reset (POR) circuit is included. On cold power on, VDDSPD input supply must rise monotonically between V_{PON} and V_{DDSPD_MIN} without ringback to ensure proper startup.

The TS5 device uses VDDIO supply for its I/O levels and it must reach $V_{DDIO(MIN)}$ to ensure proper operation of I²C or I3C Basic bus interface.

Once the VDDSPD and VDDIO supplies are valid and stable, the TS5 device shall:

1. Once VDDSPD supply is valid and stable, within t_{SENSE_SA} time, sense its SA pin to automatically configure the LID code based on what is detected on SA pin.
2. Enable I²C interface within t_{INIT} time and be ready to receive the command from the Host. The TS5 device is ready for operation after t_{INIT} time.

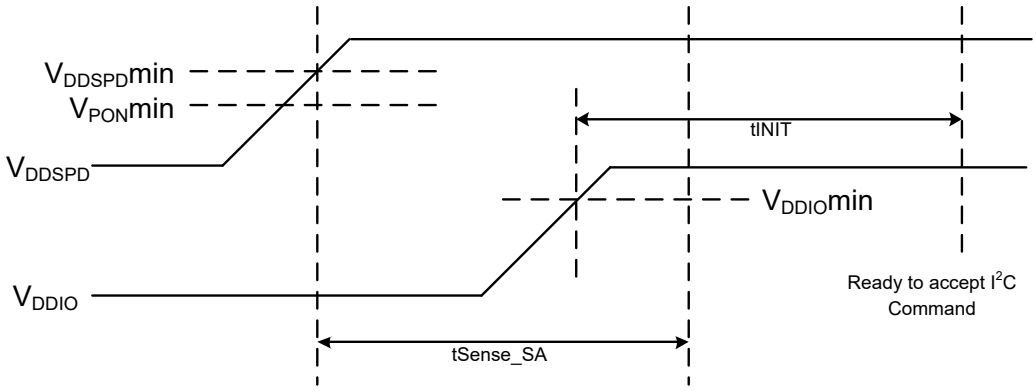


Figure 8. Device Power-Up Sequence

Device Reset and Initialization

At power down (phase during which VDDSPD input supply decreases continuously), as soon as VDDSPD input supply drops below the V_{DDSPD_MIN}, the TS5 device does not guarantee the operation.

On warm power cycling, the VDDSPD and VDDIO input supplies must remain below V_{POFF} for t_{POFF} and must meet cold power on reset timing when restoring the power.

Bus Clear

The TS5 device supports the following described Bus Clear feature in I²C mode only. Any attempt by Host to perform I²C Bus Clear on a Target device in I3C mode may result in an active drive bus contention on the SDA data line.

There may be abnormal circumstances when the Host abruptly stops clocking SCL while the Target device is in the middle of outputting data for read operation. For this type of events, the SDA data line may appear as stuck low as the device is expecting to receive more clock pulses from the Host. Eventually when the Host has control of the SCL clock, the Host may optionally clear the device that is stuck low on the SDA data line by sending continuous 18 clock pulses without driving the SDA data line followed by Stop operation. The device floats the SDA line within 18 clock pulses and returns to the Idle state. The device is ready for normal new transaction with Start condition.

DETAILED DESCRIPTION (continued)

Bus Reset

To prevent a malfunctioning device from locking up the I²C bus or I3C Basic bus, a bus reset mechanism is defined. It uses a timeout mechanism on SCL as shown in Figure 9 to force a device bus reset. All devices on an I²C or I3C Basic bus reset simultaneously. Bus reset operation works in the same way regardless of whether the device is operating in I²C or I3C Basic mode.

To guarantee the device resets I²C bus or I3C Basic bus, the HSCL clock input Low time has to be greater than or equal to $t_{TIMEOUT(MAX)}$.

The TS5 device does not reset I²C bus or I3C Basic bus if the SCL clock input Low time is less than $t_{TIMEOUT(MIN)}$.

If the SCL clock input Low time is between $t_{TIMEOUT(MIN)}$ and $t_{TIMEOUT(MAX)}$, the TS5 device does not guarantee and it may or may not reset the I²C bus or I3C Basic bus.

When RESET, the TS5 device takes the following actions:

1. Interface and any pending command or transactions are cleared.
2. All internal register values are preserved unless noted otherwise in item # 3 below.
3. Device returns to I²C mode of operation; MR7[3:1] resets to ‘111’; MR18[7:5] resets to ‘000’; MR27[4] resets to ‘0’; MR52[1:0] resets to ‘00’.
4. Device does not re-sample SA pin.
5. Device floats the SDA pin such that it gets pulled High by external/other device pull-up.
6. Device treats bus resets as Stop operation.

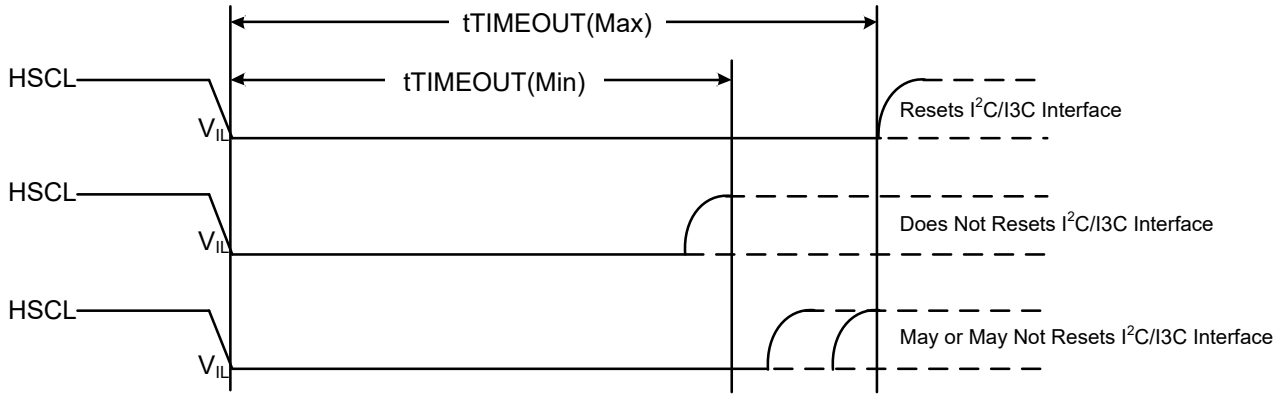


Figure 9. I²C or I3C Basic Bus Reset - TS5 Device

I/O OPERATION

At power on, by default, the TS5 device comes up in legacy I²C mode of operation with Open Drain I/O for its interface. The maximum speed is limited to 1MHz and supported I/O voltage levels are from 1.0V to 3.3V for Grade A.

After power on, the Host may put the TS5 device in I3C mode of operation. In I3C Basic mode of operation, the maximum speed is limited to 12.5MHz and supported I/O voltage levels are from 1.0V to 1.2V.

In I3C Basic mode, the Host may drive the SCL clock input of the TS5 device using either push-pull output driver or using the open-drain output driver. It is expected that for all DDR5 DIMM family environment, the Host may always drive the SCL clock input using a push-pull output driver.

To support in band interrupt, the TS5 device supports dynamic switching between Open Drain mode and Push Pull mode on its SDA bus for various events. The Table 4 below describes the different mode of operation by the TS5 device for each cycle.

Table 4. TS5 Device Dynamic I/O Operation Mode Switching

FEATURES	OPEN DRAIN MODE	PUSH PULL MODE
Start + Device Select Code	Yes	No
Start + 7'h7E IBI Header Byte	Yes	No
Repeat Start + Device Select Code	No	Yes
Repeat Start + 7'h7E Header Byte	No	Yes
CCC Bytes (i.e after 7'h7E+W = 0+ACK)	No	Yes
Stop	No	Yes
ACK/NACK Responses	Yes	No
Command, Block Address, Address Operation	No	Yes
Interrupt Request by Target + Device Select Code	Yes	No
IBI Payload	No	Yes
Write Data, T-bit sequence	No	Yes
Read Data, T-bit sequence	No	Yes
PEC, T-bit sequence	No	Yes

DEVICE INTERFACE - PROTOCOL

I²C and I3C Basic Operation

At power on, by default, the TS5 device comes up in I²C mode of operation. Following applies in I²C mode:

1. The maximum operation speed is limited to 1MHz.
2. In-band interrupts are not supported.
3. Bus reset is supported.
4. Parity check is not supported except for supported CCCs.
5. Packet Error check is not supported.

The TS5 device shall operate in the I²C mode until put into I3C Basic mode via command.

The Host may put the TS5 device in I3C Basic mode by issuing SETAASA CCC.

Following applies in I3C mode:

1. The maximum operation speed is up to 12.5MHz.
2. In-band interrupts are supported.
3. Bus reset is supported.
4. Parity check is always enabled by default.
5. Packet error check is supported and by default is disabled.

Serial Address of the TS5 Device

The 7-bit serial address of the TS5 device applies to both I²C and I3C Basic mode of operation identically.

The TS5 device 4-bit binary value is 0010b or 0110b depending on sample status of SA pin on power up.

The TS5 device samples the status of the SA pin on power up. The sampled status of the SA pin is used to select one of the two possible unique LID code for the device. The selected LID code either 0010b or 0110b is merged with a 3-bit HID code MR7[3:1] to establish the 7-bit address code for the device.

With the default setting in MR7[3:1] = '111'; if the SA pin is connected to VSS, the device address shall be 0010 111b and if the SA pin is connected to VDDSPD pin, the device address shall be 0110 111b.

Table 5. 7-Bit Address of TS5 Device

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0	SA	1	0	1	1	1	R/W
TS5 Device Type ID (LID Code)				Host ID (HID Code)			Read/Write

Switch from I²C Mode to I3C Basic Mode

By default when TS5 first powers on, it operates in I²C mode. The TS5 device shall operate in I²C mode until put into I3C Basic mode via command.

In I²C mode, the Host is allowed to issue only 3 CCCs (DEVCTRL, SETHID, SETAASA). All other CCCs are not supported and the TS5 device may simply ignore it. The Host must issue DEVCTRL and SETHID CCCs first (if required) followed by SETAASA CCC.

The Host puts the TS5 device in I3C Basic mode by issuing SETAASA CCC.

- When SETAASA CCC is registered by the TS5 device, it updates the MR18[5] to '1'.
- When SETHID CCC is registered by the TS5 device, it updates the MR7[3:1].

Switch from I3C Basic Mode to I²C Mode

The Host can put the TS5 device back in I²C mode from I3C mode at any time by issuing RSTDAA CCC. When RSTDAA CCC is registered by the TS5 device, it updates the MR18[5] to '0'.

DEVICE INTERFACE - PROTOCOL (continued)

I²C Target Protocol

The TS5 devices operate on a standard I²C serial interface. Transactions where the TS5 device is the targeted Target device begin with the Host issuing a Start condition followed by a 7-bit TS5 device address then a read or write bit, R/W. All data are transmitted with the most significant bit MSB first. During the address followed by R/W bit transmission, the TS5 device typically replies with an ACK unless there are conditions when it may passively assert a NACK. The TS5 device accepts 1 byte of address which covers 256 bytes of registers. The TS5 device volatile register space does not require page selection process as all registers are within first 256 bytes.

Write Operation - Data Packet

Table 6. Write Command Data Packet

START	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	A/N	STOP
S or Sr (1)	0	X	1	0	HID			W = 0	A	
	Address [7:0]								A	
	Data								A	
	Data								A	
	…								A	
	Data								A	Sr or P

1. In I²C mode, Start or Repeat Start operation followed by 7'h7E with W = 0 is only allowed for the purpose of issuing CCCs that are allowed in I²C mode. Any other operation including another Repeat Start is considered an illegal operation.

Read Operation - Data Packet

Table 7. Read Command Data Packet

START	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	A/N	STOP
S or Sr (1)	0	0	1	0	HID			W = 0	A	
	Address [7:0]								A	
Sr	0	0	1	0	HID			R = 1	A (2)	
	Data								A	
	Data								A	
	…								A	
	Data								N	Sr or P

1. In I²C mode, Start or Repeat Start operation followed by 7'h7E with W = 0 is only allowed for the purpose of issuing CCCs that are allowed in I²C mode. Any other operation including another Repeat Start is considered an illegal operation.
2. If Target device NACKs during Repeat Start for any reason, the Host may re-try Repeat Start again. The Host can do the Repeat Start as many times it may desire.

Default Read Address Pointer Mode

During normal operation of the DDR5 DIMM, the Host periodically may poll critical information from the same location. An example may be the TS5 device's temperature readout. To help improve the efficiency of the I²C bus protocol, the TS5 offers a Default Read Address pointer mode so that whenever the TS5 device sees the Stop operation on its SCL and SDA bus, its read address pointer always resets to default address. The default read pointer address mode is enabled through register MR18[4] and default starting address for read operation is selectable through register MR18[3:2]. This allows Host to read the read command data packet as shown in Table 8. The Default Read Address pointer reduces the packet overhead by 2 bytes. The Host typically enables this mode when the normal operation of the DDR5 DIMM begins.

Table 8. Read Command Data Packet w/ DEFAULT Address Pointer Mode

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N	Stop
S or Sr	0	X	1	0	HID			R = 1	A	
	Data								A	
	…								A	
	Data								N	Sr or P

DEVICE INTERFACE - PROTOCOL (continued)

I3C Basic Target Protocol - Host to TS5 Device

Write Operation Data Packet

The TS5 devices operate on a standard I3C serial interface. Transactions where the TS5 device is the targeted Target device begin with the Host issuing a Start condition followed by a 7-bit TS5 device address then a write bit, R/W. All data are transmitted with the most significant bit MSB first. During the address followed by R/W bit transmission, the TS5 device typically replies with an ACK unless there are conditions when it may passively assert a NACK. The 'T' bit carries Parity information from the Host for each byte.

The Packet Error Code (PEC) function is disabled by default when the TS5 device is put in I3C Basic mode.

The Host may enable this function through DEVCTRL CCC (RegMod = '0'). If enabled, the PEC is appended at the end of all transactions. If PEC is enabled, the Host must complete the burst length as indicated in CMD field. In other words, the Host must not interrupt the burst length pre-maturely for Write operation.

Table 9. Write Command Data Packet; PEC Disabled

START	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	A/N/T	STOP
S or Sr	0	X	1	0	HID			W = 0	A (1) (2) (3)	
	Address [7:0]								T	
	Data								T	
	…								T	
	Data								T	Sr (4) or P

1. See Figure 10 to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull operation (1st bit of Address, bit[7]).
2. The TS5 NACKs if there is a parity error in a previous transaction when Host performs consecutive transactions with Repeat Start.
3. The TS5 device does not check for parity error in subsequent bytes when it determines 7-bit device select code issued by the Host does not match with its own device code. The TS5 device ignores the entire packet until Stop or next Repeat Start operation.
4. Repeat Start or Repeat Start with 7'h7E.

Table 10. Write Command Data Packet; PEC Enabled

START	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	A/N/T	STOP
S or Sr	0	X	1	0	HID			W = 0	A (1) (2) (3)	
	Address [7:0]								T	
	CMD			W = 0	0	0	0	0	T	
	Data								T	
	…								T	
	Data									
	PEC								T	Sr (4) or P

1. See Figure 10 to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation (1st bit of Address, bit[7]).
2. The TS5 NACKs if there is a parity or PEC error in a previous transaction when Host performs consecutive transactions with Repeat Start.
3. The TS5 device does not check for parity or PEC error in subsequent bytes when it determines 7-bit device select code issued by the Host does not match with its own device code. The TS5 device ignores the entire packet until Stop or next Repeat Start operation.
4. Repeat Start or Repeat Start with 7'h7E.

DEVICE INTERFACE - PROTOCOL (continued)

The Host may optionally allow TS5 device to request IBI. For this case, the transactions to the TS5 device begin with the I3C Basic Host issuing a Start condition followed by 7'h7E and then write bit. If TS5 device has a pending IBI, it transmits its 7-bit device select code followed by R = '1'. If TS5 device has no pending IBI, there is no action taken by TS5. The Table 11 and Table 12 show the I3C Basic bus write command data packet with optional IBI header for PEC disabled and PEC enabled cases respectively. Note that in Table 12, PEC calculation does not include IBI header byte (7'h7E followed by W = 0).

Table 11. Write Command Data Packet w/ IBI Header; PEC Disabled

START	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	A/N/T	STOP
S	1	1	1	1	1	1	0	W = 0	A (1) (3)	
Sr	0	X	1	0	HID			W = 0	A (2) (3) (4)	
	Address [7:0]								T	
	Data								T	
	…								T	
	Data								T	Sr (5) or P

1. See Figure 10 to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation (Repeat Start).
2. See Figure 12 to see how the transition occurs from Host Push Pull Operation to Target Open Drain (ACK) and Figure 10 to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation (1st bit of Address, bit[7]).
3. The TS5 NACKs if there is a parity error in a previous transaction when Host performs consecutive transactions with Repeat Start.
4. The TS5 device does not check for parity error in subsequent bytes when it determines 7-bit device select code issued by the Host does not match with its own device code. The TS5 device ignores the entire packet until Stop or next Repeat Start operation.
5. Repeat Start or Repeat Start with 7'h7E.

Table 12. Write Command Data Packet w/ IBI Header; PEC Enabled

START	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	A/N/T	STOP
S	1	1	1	1	1	1	0	W = 0	A (1) (3)	
Sr	0	X	1	0	HID			W = 0	A (2) (3) (4)	
	Address [7:0]								T	
	CMD			W = 0	0000				T	
	Data								T	
	…								T	
	Data								T	
	PEC								T	Sr (5) or P

1. See Figure 10 to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation (Repeat Start).
2. See Figure 12 to see how the transition occurs from Host Push Pull Operation to Target Open Drain (ACK) and Figure 10 to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation (1st bit of Address, bit[7]).
3. The TS5 NACKs if there is a parity error in a previous transaction when Host performs consecutive transactions with Repeat Start.
4. The TS5 device does not check for parity error in subsequent bytes when it determines 7-bit device select code issued by the Host does not match with its own device code. The TS5 device ignores the entire packet until Stop or next Repeat Start operation.
5. Repeat Start or Repeat Start with 7'h7E.

Read Operation Data Packet

The transactions to TS5 Target device begin with the I3C Basic Host issuing a Start condition followed by a 7-bit TS5 device type identifier then a write bit. All I3C Basic bus data are transmitted with the most significant bit MSB first. During select code transmission, the TS5 device typically replies with an ACK unless there are exceptional conditions when it may passively assert a NACK. See Table 13. The 'T' bit carries Parity information from the Host prior to Repeated Start. After Repeated Start, 'T' bit carries information from TS5 device to Host indicating Continuous ('1') or Stop ('0') whether it is transmitting the last byte or not.

The Packet Error Code (PEC) function is disabled by default when TS5 device is put in I3C Basic mode. The Host may enable this function through DEVCTRL CCC (RegMod = '0'). If enabled, the PEC is appended as shown in Table 14. If PEC is enabled, the Host must complete the burst length as indicated in CMD field. In other words, the Host must not interrupt the burst length pre-maturely for Read operation.

DEVICE INTERFACE - PROTOCOL (continued)

The Host may optionally allow TS5 device to request IBI. For this case, the transactions to the TS5 device begin with the I3C Basic Host issuing a Start condition followed by 7'h7E and then write bit. If TS5 device has a pending IBI, it transmits its 7-bit device select code followed by R = '1'. If TS5 device has no pending IBI, there is no action taken by TS5. Table 15 and Table 16 show the I3C Basic bus read command data packet with optional IBI header for PEC disabled and PEC enabled cases respectively. Note that in Table 16, PEC calculation (from Host to TS5) does not include IBI header byte (7'h7E followed by W = 0).

Table 13. Read Command Data Packet; PEC Disabled

START	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	A/N/T	STOP
S or Sr	0	X	1	0	HID			W = 0	A (1) (2) (3)	
	Address [7:0]								T	
S or Sr	0	X	1	0	HID			R = 1	A/N (4) (5)	
	Data								T = 1	
	…								T = 1	
	Data								T = 1 (6) (7)	Sr (8) or P

1. See Figure 10 to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation (1st bit of Address, bit[7]).
2. The TS5 NACKs if there is a parity error in a previous transaction when Host performs consecutive transactions with Repeat Start.
3. The TS5 device does not check for parity error in subsequent bytes when it determines 7-bit device select code issued by the Host does not match with its own device code. The TS5 device ignores the entire packet until Stop or next Repeat Start operation.
4. If Target device NACKs during Repeat Start for any reason, the Host may re-try Repeat Start again. The Host can do the Repeat Start as many times it may desire. If Target device NACKs due to parity error in previous bytes, it will always NACK regardless of how many times the Host tries Repeat Start. If there were no parity errors the TS5 may eventually ACK.
5. See Figure 12 to see how the transition occurs from Host Push Pull Operation to Target Open Drain (ACK).
6. See Figure 13 to see how Host ends Target device operation.
7. When last byte (i.e. MR255) is reached (extreme rare case), the Target device sends T = '0'. See Figure 14 to see how Target device ends the operation followed by Host Stop operation.
8. Repeat Start or Repeat Start with 7'h7E.

Table 14. Read Command Data Packet; PEC Enabled

START	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	A/N/T	STOP
S or Sr	0	X	1	0	HID			W = 0	A (1) (2) (3)	
	Address [7:0]								T	
	CMD			R = 1	0	0	0	0	T	
	PEC								T	
S or Sr	0	X	1	0	HID			R = 1	A/N (4) (5)	
	Data								T = 1	
	…								T = 1	
	Data								T = 1	
	PEC								T = 0 (6)	Sr (7) or P

1. See Figure 10 to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation (1st bit of Address, bit[7]).
2. The TS5 NACKs if there is a parity error in a previous transaction when Host performs consecutive transactions with Repeat Start.
3. The TS5 device does not check for parity or PEC error in subsequent bytes when it determines 7-bit device select code issued by the Host does not match with its own device code. The TS5 device ignores the entire packet until Stop or next Repeat Start operation.
4. If Target device NACKs during Repeat Start for any reason, the Host may re-try Repeat Start again. The Host can do the Repeat Start as many times it may desire. If Target device NACKs due to PEC error parity error in previous bytes, it will always NACK regardless of how many times the Host tries Repeat Start. If there were no parity or PEC errors, the TS5 may eventually ACK. The PEC calculation by the Target device only includes device select code of the ACK response of the Repeat start operation. In other words, if there are more than one Repeat Start operation, the Target device includes device select code of only the last Repeat Start from the Host when it ACKs in PEC calculation and all other NACK responses of the device select code of the Repeat Start are not included in PEC calculation.
5. See Figure 12 to see how the transition occurs from Host Push Pull Operation to Target Open Drain (ACK).
6. See Figure 14 to see how Target device ends the operation followed by Host Stop operation.
7. Repeat Start or Repeat Start with 7'h7E.

DEVICE INTERFACE - PROTOCOL (continued)

Table 15. Read Command Data Packet w/ IBI Header; PEC Disabled

START	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	A/N/T	STOP
S	1	1	1	1	1	1	0	W = 0	A(1) (3)	
Sr	0	X	1	0	HID			W = 0	A(2) (3) (4)	
	Address [7:0]								T	
Sr	0	X	1	0	HID			R = 1	A/N(5) (6)	
	Data								T = 1	
	…								T = 1	
	Data								T = 1(7) (8)	Sr (9) or P

1. See Figure 10 to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation (Repeat Start).
2. See Figure 12 to see how the transition occurs from Host Push Pull Operation to Target Open Drain (ACK) and Figure 13 to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation (1st bit of Address, bit[7]).
3. The TS5 NACKs if there is a parity error in a previous transaction when Host performs consecutive transactions with Repeat Start.
4. The TS5 does not check for parity error in subsequent bytes when it determines 7-bit device select code issued by the Host does not match with its own device code. The TS5 ignores the entire packet until Stop or next Repeat Start operation.
5. See Figure 12 to see how the transition occurs from Host Push Pull Operation to Target Open Drain (ACK).
6. If Target device NACKs during Repeat Start for any reason, the Host may re-try Repeat Start again. The Host can do the Repeat Start as many times it may desire. If Target device NACKs due to parity error in previous bytes, it will always NACK regardless of how many times the Host tries Repeat Start. If there were no parity errors, the TS5 may eventually ACK.
7. See Figure 13 to see how Host ends Target device operation.
8. When last byte (i.e. MR255) is reached (extreme rare case), the Target device sends T = '0'. See Figure 14 to see how Target device ends the operation followed by Host Stop operation.
9. Repeat Start or Repeat Start with 7'h7E.

Table 16. Read Command Data Packet w/ IBI Header; PEC Enabled

START	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	A/N/T	STOP
S	1	1	1	1	1	1	0	W = 0	A(1) (3)	
Sr	0	X	1	0	HID			W = 0	A(2) (3) (4)	
	Address [7:0]								T	
	CMD			R = 1	0000				T	
	PEC								T	
Sr	0	X	1	0	HID			R = 1	A/N(5) (6)	
	Data								T = 1	
	…								T = 1	
	Data								T = 1	
	PEC								T = 0(7)	Sr(8) or P

1. See Figure 10 to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation (Repeat Start).
2. See Figure 12 to see how the transition occurs from Host Push Pull Operation to Target Open Drain (ACK) and See Figure 7 to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation (1st bit of Address, bit[7]).
3. The TS5 NACKs if there is a parity or PEC error in a previous transaction when Host performs consecutive transactions with Repeat Start.
4. The TS5 does not check for parity or PEC error in subsequent bytes when it determines 7-bit device select code issued by the Host does not match its own device code. The TS5 ignores the entire packet until Stop or next Repeat Start operation.
5. See Figure 12 to see how the transition occurs from Host Push Pull Operation to Target Open Drain (ACK).
6. If Target device NACKs during Repeat Start for any reason, the Host may re-try Repeat Start again. The Host can do Repeat Start as many times it may desire. If Target device NACKs due to PEC error or parity error in previous bytes, it will always NACK regardless of how many times the Host tries Repeat Start. If there was no parity or PEC error, the TS5 may eventually ACK. The PEC calculation by the Target device only includes device select code of the ACK response of the Repeat Start operation. If there are more than one Repeat Start operation, the Target device includes device select of only the last Repeat Start from the Host when it ACKs in PEC calculation and all other NACK responses of the device select code of the Repeat Start are not included in PEC calculation.
7. See Figure 14 to see how Target device ends the operation followed by Host Stop operation.
8. Repeat Start or Repeat Start with 7'h7E.

DEVICE INTERFACE - PROTOCOL (continued)

Default Read Address Pointer Mode

This mode works the same exact way as explained in ***Default Read Address Pointer Mode*** section. Table 17 and Table 18 the read command data packet for PEC function disabled and enabled respectively. When PEC function is enabled, MR18[1] sets the number of bytes that TS5 device sends out followed by the PEC calculation. If PEC is enabled, the Host must complete the burst length as indicated in MR18[1] register. In other words, the Host must not interrupt the burst length pre-maturely for default address pointer read operation.

Table 17. Read Command Data Packet w/ Read Address Pointer Mode; PEC Disabled

START	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	A/N/T	STOP
S or Sr	0	X	1	0	HID			R = 1	A (1)	
	Data								T = 1	
	…								T = 1	
	Data								T = 1 (2) (3)	Sr (4) or P

1. The TS5 NACKs if there is a parity error in a previous transaction when Host performs consecutive transactions with Repeat Start.
2. See Figure 13 to see how Host ends Target device operation.
3. When last byte (i.e. MR255) is reached (extreme rare case), the Target device sends T = '0'. See Figure 14 to see how Target device ends the operation followed by Host Stop operation.
4. Repeat Start or Repeat Start with 7'h7E.

Table 18. Read Command Data Packet w/ Read Address Pointer Mode; PEC Enabled

START	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	A/N/T	STOP
S or Sr	0	X	1	0	HID			R = 1	A(1)	
	Data								T = 1	
	…								T = 1	
	Data								T = 1	
	PEC								T = 0 (2)	Sr (3) or P

1. The TS5 NACKs if there is a parity or PEC error in a previous transaction when Host performs consecutive transactions with Repeat Start.
2. See Figure 14 to see how Target device ends the operation followed by Stop operation.
3. Repeat Start or Repeat Start with 7'h7E.

Table 19. Read CMD Data Packet w/ Read Address Pointer Mode and IBI Header; PEC Disabled

START	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	A/N/T	STOP
S	1	1	1	1	1	1	0	W = 0	A(1) (2)	
Sr	0	X	1	0	HID			R = 1	A/N2,3	
	Data								T = 1	
	…								T = 1	
	Data								T = 1 4,5	Sr6 or P

1. See Figure 10 to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation (Repeat Start).
2. The TS5 NACKs if there is a parity error in a previous transaction when Host performs consecutive transactions with Repeat Start.
3. See Figure 12 to see how the transition occurs from Host Push Pull Operation to Target Open Drain (ACK).
4. See Figure 13 to see how Host ends Target device operation.
5. When last byte (i.e. MR255) is reached (extreme rare case), the Target device sends T = '0'. See Figure 14 to see how Target device ends the operation followed by Host Stop operation.
6. Repeat Start or Repeat Start with 7'h7E.

Table 20. Read CMD Data Packet w/ Read Address Pointer Mode and IBI Header; PEC Enabled

START	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	A/N/T	STOP
S	1	1	1	1	1	1	0	W = 0	A(1) (2)	
Sr	0	X	1	0	HID			R = 1	A/N (2) (3)	
	Data								T = 1	
	…								T = 1	
	Data								T = 1	
	PEC								T = 0(4)	Sr(5) or P

1. See Figure 10 to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation (Repeat Start).
2. The TS5 NACKs if there is a parity or PEC error in a previous transaction when Host performs consecutive transactions with Repeat Start.
3. See Figure 12 to see how the transition occurs from Host Push Pull Operation to Target Open Drain (ACK).
4. See Figure 14 to see how Target device ends the operation followed by Stop operation.
5. Repeat Start or Repeat Start with 7'h7E.

DEVICE INTERFACE - PROTOCOL (continued)

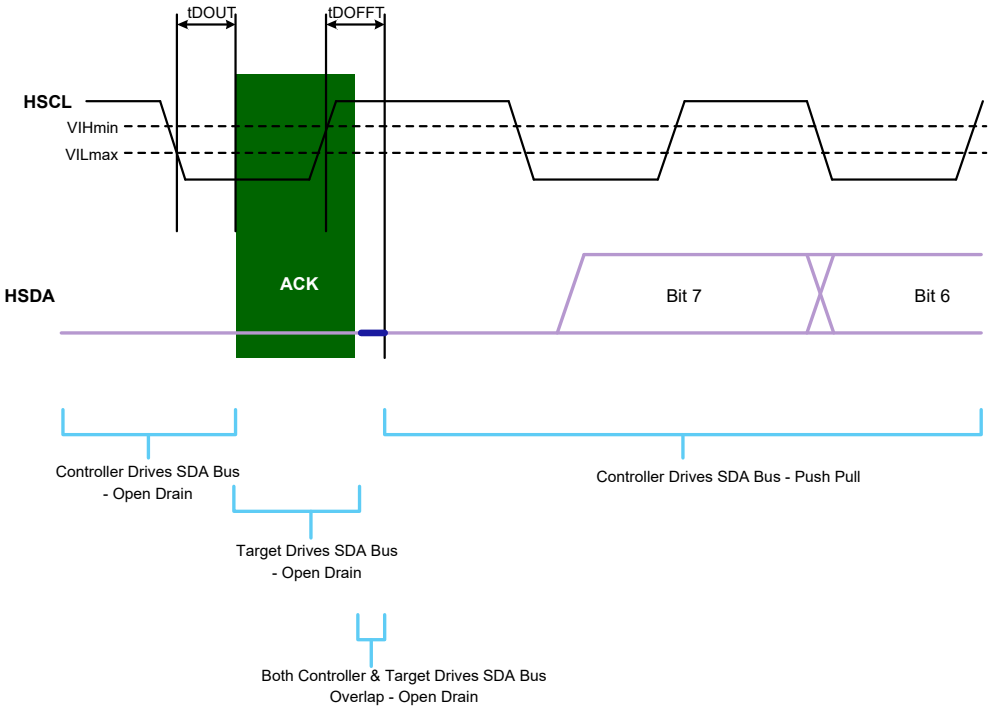


Figure 10. Target Open Drain to Host Push Pull Hand Off Operation

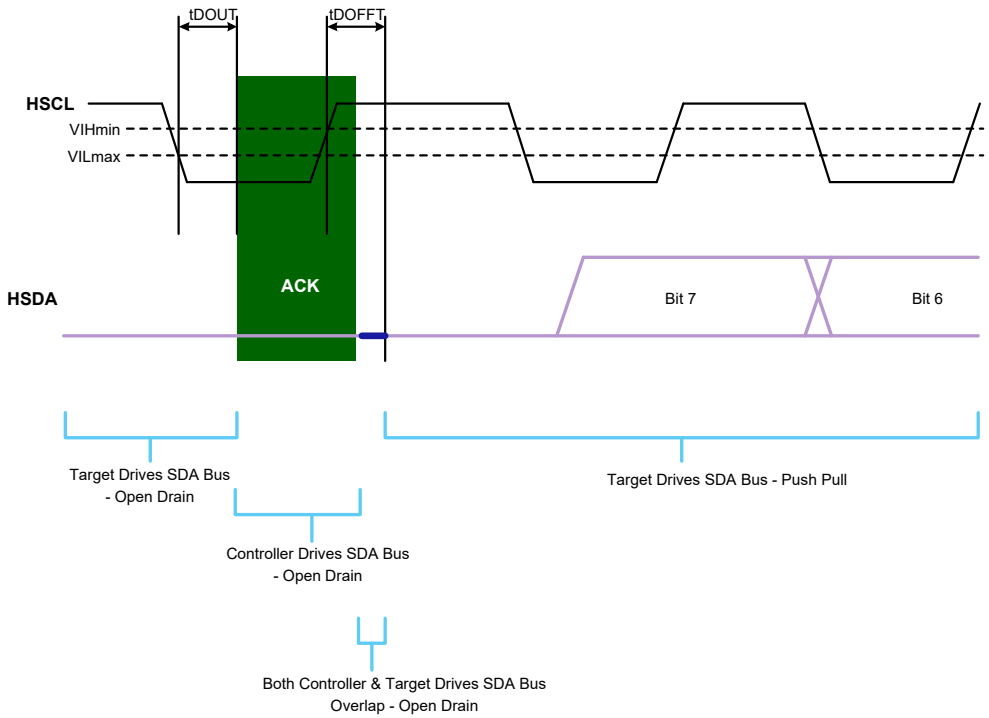


Figure 11. Controller Open Drain (ACK) to Target Push Pull Hand Off Operation

DEVICE INTERFACE - PROTOCOL (continued)

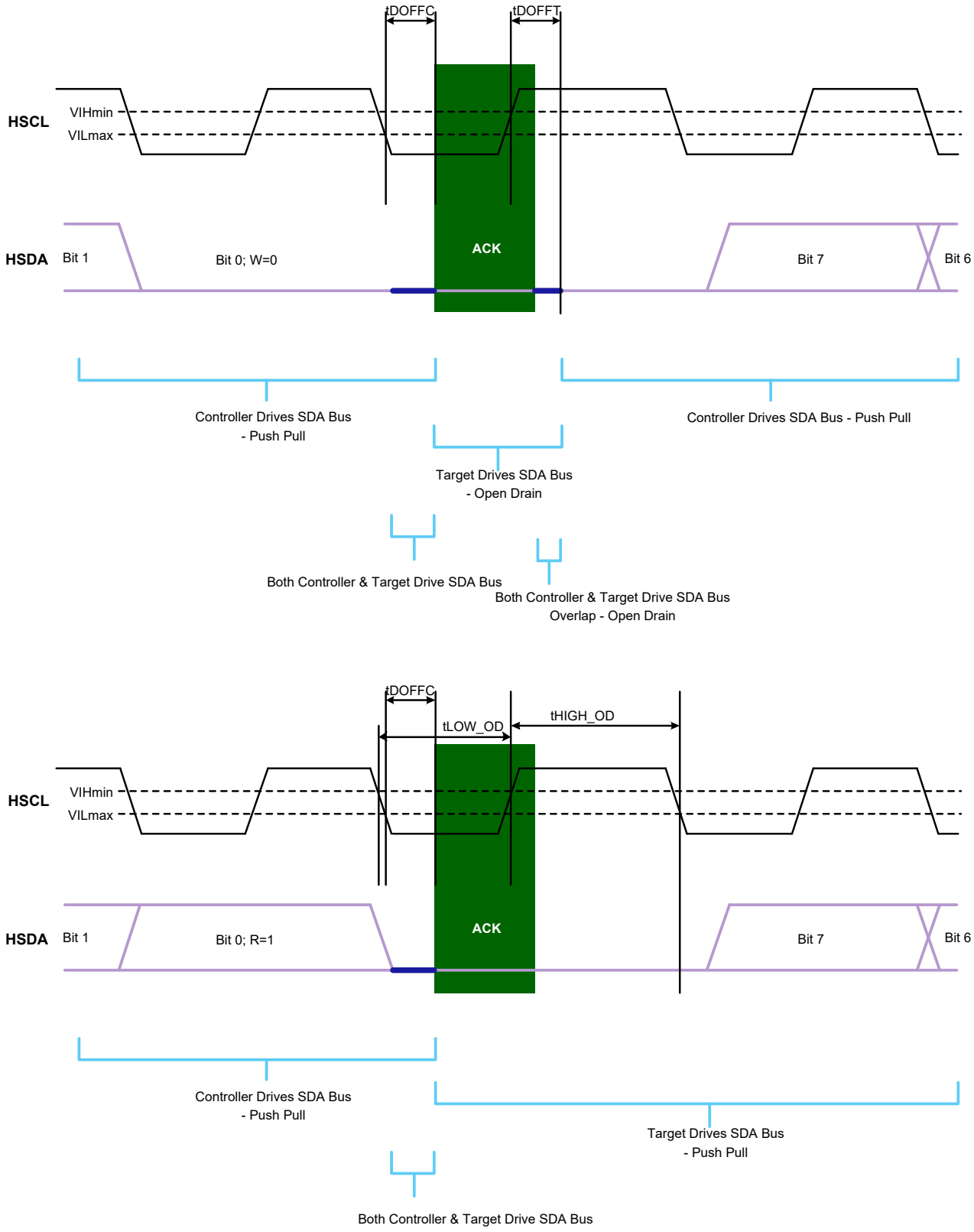


Figure 12. Controller Push Pull to Target Open Drain Hand Off Operation

DEVICE INTERFACE - PROTOCOL (continued)

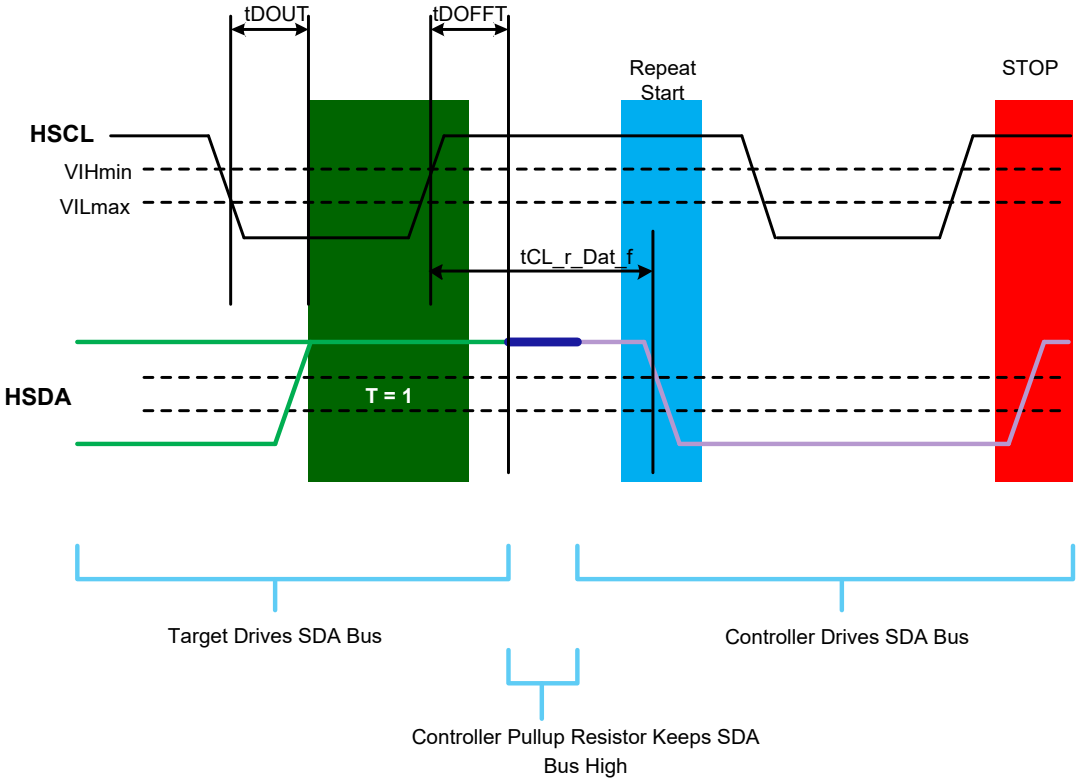


Figure 13. T = 1; Host Ends Read with Repeated Start and Stop Waveform

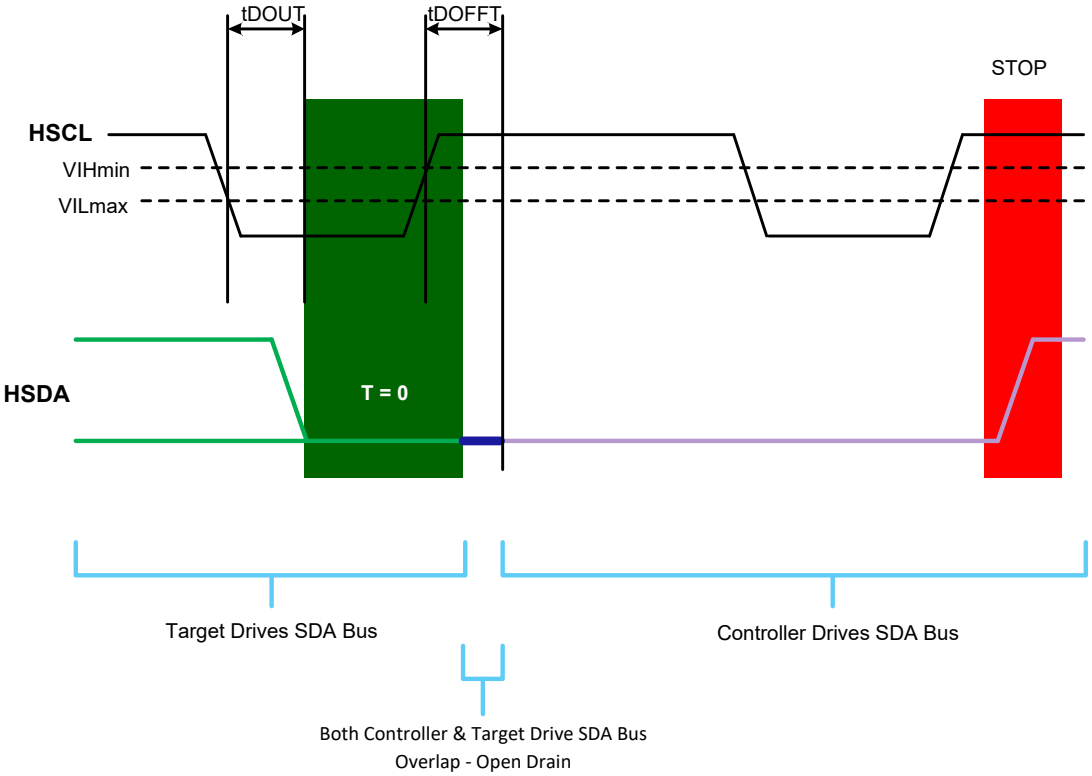


Figure 14. T = 0; Target Ends Read; Host Generates Stop

DEVICE INTERFACE - PROTOCOL (continued)

I3C Basic Common Command Codes (CCC)

The I3C Basic specification lists large number of Common Command Codes (CCC). Not all CCC are required to be supported. The TS5 device NACKs for all unsupported CCC. The TS5 supports CCC as listed in Table 21 below.

The TS5 device requires Stop operation in between when switching from CCC operation to private device specific Write or Read or Default Read Address Pointer mode operation and vice versa. In other words, any CCC operation must be followed by Stop operation before continuing to any device specific Write or Read or Default Read Address Pointer mode operation. Similarly, any device specific Write or Read or Default Read Address Pointer mode operation must be followed by Stop operation before continuing to any CCC operation. The TS5 device also requires Stop operation between any direct CCC to broadcast CCC.

The TS5 device does allow Repeat Start operation between any direct CCC to any other direct CCC or between any broadcast CCC to any other broadcast CCC or between any private Write or Read or Default Read Address Pointer mode operation to any other private Write or Read or Default Read Address Pointer mode operation.

CCC is an I3C concept by definition, and shall always conform to I3C SDR timings, irrespective of whether the device has switched from I²C mode or not.

Prior to dynamic address assignment (SETAASA/P), the Target device(s) may drive the ACK/NACK past the Open Drain SCL rising but before the next SCL falling transition, as a longer overlap in Open Drain is harmless. Immediately after the Open Drain ACK (upon the next SCL falling edge), the bus should transition to Push Pull mode (though still at 1MHz) as described in the *MIPI I3C Basic Specification V1.0, Section 5.1.2.3 "Handoff from Address ACK to SDR Controller Write Data"* and *Figure 32 "I3C Data Transfer - ACK by Target"*.

For additional details on how to handle the ACK transition, please refer to the *MIPI I3C Basic Specification V1.0, Section 5.1.2.3.1 "Transition from Address ACK to SDR Controller Write Data"*.

Table 21. TS5 CCC Support Requirement

CCC	Mode	Code	DESCRIPTION
ENEC	Broadcast	0x00	Enable Event Interrupts
	Direct	0x80	
DISEC	Broadcast	0x01	Disable Event Interrupts
	Direct	0x81	
RSTDAA	Broadcast	0x06	Put the device in I²C Mode (aka: Reset Dynamic Address Assignment)
SETAASA	Broadcast	0x29	Put the device in I3C Basic Mode (aka: Set All Addresses to Static Address)
GETSTATUS	Direct	0x90	Get Device Status
DEVCAP (1)	Direct	0xE0	Get Device Capability
SETHID (1)	Broadcast	0x61	TS5 updates 3-bit HID field, updates 'T' bit with updated parity calculation for all devices behind Hub and stops 3-bit HID translation.
DEVCTRL (1)	Broadcast	0x62	Configure TS5 and all devices behind Hub

1. JEDEC specific CCC.

DEVICE INTERFACE - PROTOCOL (continued)

ENEC CCC

The ENEC CCC is only supported after device is put in I3C Basic mode. In I²C mode, it is illegal for Host to issue this CCC. When ENEC CCC is registered by the TS5, it updates MR27[4] = '1' and it takes in effect at the next Start operation (i.e. after Stop condition). Table 22 to Table 25 shows an example of a single ENEC CCC. Table 26 shows the encoding definition for ENEC CCC.

If PEC function is enabled, the PEC calculation starts with Start or Repeat Start operation but does not include 7'h7E with W = 0 byte in PEC calculation.

Table 22. ENEC CCC - Broadcast

START	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	A/N/T	STOP
S or Sr	1	1	1	1	1	1	0	W = 0	A (1)	
	0x00 (Broadcast)								T	
	7'h00							ENINT	T	Sr (2) or P

1. The TS5 NACKs if there is a parity error in a previous transaction when Host performs consecutive transactions with Repeat Start.
2. Repeat Start or Repeat Start with 7'h7E.

Table 23. ENEC CCC - Broadcast w/ PEC

START	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	A/N/T	STOP
S or Sr	1	1	1	1	1	1	0	W = 0	A (1)	
	0x00 (Broadcast)								T	
	7'h00							ENINT	T	
	PEC								T	Sr (2) or P

1. The TS5 NACKs if there is a parity or PEC error in a previous transaction when Host performs consecutive transactions with Repeat Start.
2. Repeat Start or Repeat Start with 7'h7E.

Table 24. ENEC CCC - Direct

START	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	A/N/T	STOP
S or Sr	1	1	1	1	1	1	0	W = 0	A (1)	
	0x80 (Direct)								T	
Sr	DevID[6:0]							W = 0	A (1) (2)	
	7'h00							ENINT	T	Sr (3) or P

1. The TS5 NACKs if there is a parity error in a previous transaction when Host performs consecutive transactions with Repeat Start.
2. The TS5 device does not check for parity error in subsequent bytes when it determines 7-bit device select code issued by the Host does not match with its own device code. The TS5 device ignores the entire packet until Stop or next Repeat Start operation.
3. Repeat Start or Repeat Start with 7'h7E.

Table 25. ENEC CCC - Direct w/ PEC

START	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	A/N/T	STOP
S or Sr	1	1	1	1	1	1	0	W = 0	A (1)	
	0x80 (Direct)								T	
	PEC								T	
Sr	DevID[6:0]							W = 0	A (1) (2)	
	7'h00							ENINT	T	
	PEC								T	Sr (3) or P

1. The TS5 NACKs if there is a parity or PEC error in a previous transaction when Host performs consecutive transactions with Repeat Start.
2. The TS5 device does not check for parity or PEC error in subsequent bytes when it determines 7-bit device select code issued by the Host does not match with its own device code. The TS5 device ignores the entire packet until Stop or next Repeat Start operation.
3. Repeat Start or Repeat Start with 7'h7E.

Table 26. ENEC CCC Byte Encoding

BIT	ENCODING	NOTES
ENINT	0 = No Action 1 = Enable IBI Interrupt	It is illegal for Host to issue ENEC CCC with ENINT bit = '0'

DEVICE INTERFACE - PROTOCOL (continued)

DISEC CCC

The DISEC CCC is only supported after device is put in I3C Basic mode. In I²C mode, it is illegal for Host to issue this CCC. When DISEC CCC is registered by the TS5, it updates MR27[4] = '0'and it takes in effect at the next Start operation (i.e. after Stop condition). Table 27 to Table 30 shows an example of a single DISEC CCC. Table 31 shows the encoding definition for DISEC CCC.

If PEC function is enabled, the PEC calculation starts with Start or Repeat Start operation but does not include 7'h7E with W = 0 byte in PEC calculation.

Table 27. DISEC CCC - Broadcast

START	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	A/N/T	STOP
S or Sr	1	1	1	1	1	1	0	W = 0	A (1)	
	0x01 (Broadcast)								T	
	7'h00							DISINT	T	Sr (2) or P

1. The TS5 NACKs if there is a parity error in a previous transaction when Host performs consecutive transactions with Repeat Start.
2. Repeat Start or Repeat Start with 7'h7E.

Table 28. DISEC CCC - Broadcast w/ PEC

START	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	A/N/T	STOP
S or Sr	1	1	1	1	1	1	0	W = 0	A (1)	
	0x01 (Broadcast)								T	
	7'h00							DISINT	T	
	PEC								T	Sr (2) or P

1. The TS5 NACKs if there is a parity or PEC error in a previous transaction when Host performs consecutive transactions with Repeat Start.
2. Repeat Start or Repeat Start with 7'h7E.

Table 29. DISEC CCC - Direct

START	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	A/N/T	STOP
S or Sr	1	1	1	1	1	1	0	W = 0	A (1)	
	0x81 (Direct)								T	
Sr	DevID[6:0]							W = 0	A (1) (2)	
	7'h00							ENINT	T	Sr (3) or P

1. The TS5 NACKs if there is a parity error in a previous transaction when Host performs consecutive transactions with Repeat Start.
2. The TS5 device does not check for parity error in subsequent bytes when it determines 7-bit device select code issued by the Host does not match with its own device code. The TS5 device ignores the entire packet until Stop or next Repeat Start operation.
3. Repeat Start or Repeat Start with 7'h7E.

Table 30. DISEC CCC - Direct w/ PEC

START	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	A/N/T	STOP
S or Sr	1	1	1	1	1	1	0	W = 0	A (1)	
	0x81 (Direct)								T	
	PEC								T	
Sr	DevID[6:0]							W = 0	A (1) (2)	
	7'h00							DISINT	T	
	PEC								T	Sr (3) or P

1. The TS5 NACKs if there is a parity or PEC error in a previous transaction when Host performs consecutive transactions with Repeat Start.
2. The TS5 device does not check for parity or PEC error in subsequent bytes when it determines 7-bit device select code issued by the Host does not match with its own device code. The TS5 device ignores the entire packet until Stop or next Repeat Start operation.
3. Repeat Start or Repeat Start with 7'h7E.

Table 31. DISEC CCC Byte Encoding

BIT	ENCODING	NOTES
DISINT	0 = No Action 1 = Disable IBI Interrupt	It is illegal for Host to issue DISEC CCC with DISINT bit = '0'

DEVICE INTERFACE - PROTOCOL (continued)

RSTDAA CCC

The RSTDAA CCC is only supported after device is put in I3C Basic mode. In I²C mode, this CCC is ignored. When RSTDAA CCC is registered by the TS5, it updates MR18[5] = '0'and it takes in effect at the next Start operation (i.e. after Stop condition). Further it disables IBI and PEC function (MR27[4] = '0', MR18[7] = '0' respectively) and clears parity function (MR18[6] = '0'). Table 32 to Table 33 shows an example of a single RSTDAA CCC.

If PEC function is enabled, the PEC calculation starts with Start or Repeat Start operation but does not include 7'h7E with W = 0 byte in PEC calculation.

Table 32. RSTDAA CCC - Broadcast

START	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	A/N/T	STOP
S or Sr	1	1	1	1	1	1	0	W = 0	A (1)	
	0x06 (Broadcast)								T	Sr (2) or P

1. The TS5 NACKs if there is a parity error in a previous transaction when Host performs consecutive transactions with Repeat Start.
2. Repeat Start or Repeat Start with 7'h7E.

Table 33. RSTDAA CCC - Broadcast w/ PEC

START	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	A/N/T	STOP
S or Sr	1	1	1	1	1	1	0	W = 0	A (1)	
	0x06 (Broadcast)								T	
	PEC								T	Sr (2) or P

1. The TS5 NACKs if there is a parity or PEC error in a previous transaction when Host performs consecutive transactions with Repeat Start.
2. Repeat Start or Repeat Start with 7'h7E.

SETAASA CCC

The SETAASA CCC is only supported when device is in I²C mode; however, it still follows I3C SDR timings compliant to CCC definitions. In I²C mode, when the Host issues this CCC, to guarantee that this CCC is registered by the device without any error, the Host shall limit the maximum speed operation for this CCC to 1MHz. In I3C Basic mode, this CCC is ignored. When SETAASA CCC is registered by the TS5, it updates MR18[5] = '1'and it takes in effect at the next Start operation (i.e. after Stop condition). Table 34 shows an example of a single SETAASA CCC.

SETAASA CCC does not support PEC function as device is in I²C mode and there is no PEC function in I²C mode.

Table 34. SETAASA CCC - Broadcast

START	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	A/N/T	STOP
S or Sr	1	1	1	1	1	1	0	W = 0	A	
	0x29 (Broadcast)								T	P

DEVICE INTERFACE - PROTOCOL (continued)

GETSTATUS CCC

The GETSTATUS CCC is supported in I3C Basic mode. In I²C mode, this CCC is ignored (i.e. it is not executed internally and GETSTATUS CCC code is not acknowledged and Host must do Stop operation). Table 35 to Table 36 shows an example of a single GETSTATUS CCC. Table 37 shows the encoding definition for GETSTATUS CCC.

If PEC function is enabled, the PEC calculation starts with Start or Repeat Start operation but does not include 7'h7E with W = 0 byte in PEC calculation.

When the TS5 device responds to GETSTATUS CCC, after it completes the response, the PEC_Err, P_Err and Pending Interrupt Bits [3:0] do not automatically get cleared. The Host must explicitly clear the appropriate status register through Clear command by writing '1' to corresponding register or by issuing Global Clear command. Once the TS5 device clears the appropriate status register, the PEC_Err, P_err and Pending Interrupt Bits [3:0] get cleared.

After Host issues Clear command, if the condition is still present, the device will again set the appropriate status register, sets the IBI status register to '1' and Pending Interrupt Bits [3:0] to '0001'.

Table 35. GETSTATUS CCC - Direct

START	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	A/N/T	STOP
S or Sr	1	1	1	1	1	1	0	W = 0	A (1)	
	0x90 (Direct)								T	
Sr	DevID[6:0]							R = 1	A (1)	
	PEC_Err	0	0	0	0	0	0	0	T = 1	
	0	0	P_Err	0	Pending Interrupt				T = 0	Sr (2) or P

1. The TS5 NACKs if there is a parity error in a previous transaction when Host performs consecutive transactions with Repeat Start.
2. Repeat Start or Repeat Start with 7'h7E.

Table 36. GETSTATUS CCC - Direct w/ PEC1

START	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	A/N/T	STOP
S or Sr	1	1	1	1	1	1	0	W = 0	A (2)	
	0x90 (Direct)								T	
	PEC								T	
Sr	DevID[6:0]							R = 1	A (1)	
	PEC_Err	0	0	0	0	0	0	0	T = 1	
	0	0	P_Err	0	Pending Interrupt				T = 1	
	PEC								T = 0	Sr (3) or P

1. GETSTATUS CCC with PEC check is only supported in I3C Basic mode.
2. The TS5 NACKs if there is a parity or PEC error in a previous transaction when Host performs consecutive transactions with Repeat Start.
3. Repeat Start or Repeat Start with 7'h7E.

Table 37. GETSTATUS CCC Byte Encoding

BIT	ENCODING	NOTES
PEC_Err	0 = No Error 1 = PEC Error occurred	This register is cleared when Host issues clear command to MR20[1] for PEC error.
P_Err	0 = No Error 1 = Protocol Error; Parity Error occurred	This register is cleared when Host issues clear command to MR20[0] for Parity error.
Pending Interrupt	0000 = No Pending Interrupt 0001 = Pending Interrupt All other encodings are reserved	This register is cleared when Host issues clear command to any appropriate device status register that causes IBI status register to get cleared.

DEVICE INTERFACE - PROTOCOL (continued)

DEVCAP CCC

The DEVCAP CCC is only supported after device is put in I3C Basic mode. In I²C mode, it is illegal for Host to issue this CCC. Table 38 to Table 39 shows an example of a single DEVCAP CCC. Table 40 shows the encoding definition for DEVCAP CCC.

If PEC function is enabled, the PEC calculation starts with Start or Repeat Start operation but does not include 7'h7E with W = 0 byte in PEC calculation.

Table 38. DEVCAP CCC - Direct

START	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	A/N/T	STOP
S or Sr	1	1	1	1	1	1	0	W = 0	A (1)	
	0xE0 (Direct)								T	
Sr	DevID[6:0]							R = 1	A (1)	
	MSB (Each bit defines capability)								T = 1	
	LSB (Each bit defines capability)								T = 0	Sr (2) or P

1. The TS5 NACKs if there is a parity error in a previous transaction when Host performs consecutive transactions with Repeat Start.
2. Repeat Start or Repeat Start with 7'h7E.

Table 39. DEVCAP CCC - Direct w/ PEC

START	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	A/N/T	STOP
S or Sr	1	1	1	1	1	1	0	W = 0	A (1)	
	0xE0 (Direct)								T	
	PEC								T	
Sr	DevID[6:0]							R = 1	A (1)	
	MSB (Each bit defines capability)								T = 1	
	LSB (Each bit defines capability)								T = 1	
	PEC								T = 0	Sr (2) or P

1. The TS5 NACKs if there is a parity or PEC error in a previous transaction when Host performs consecutive transactions with Repeat Start.
2. Repeat Start or Repeat Start with 7'h7E.

Table 40. DEVCAP CCC Byte Encoding

BIT	ENCODING	NOTES
MSB[7]	RFU	Coded as '0'
MSB[6]	RFU	Coded as '0'
MSB[5]	RFU	Coded as '0'
MSB[4]	RFU	Coded as '0'
MSB[3]	RFU	Coded as '0'
MSB[2]	0 = No Support for Timer based Reset 1 = Supports Timer based Reset	TS5 hard codes to '1'
MSB[1:0]	RFU	Coded as '0'
LSB[7:0]	RFU	Coded as '0'

DEVICE INTERFACE - PROTOCOL (continued)

SETHID CCC

The SETHID CCC is supported only when device is in I²C mode. In I²C mode, when the Host issues this CCC, to guarantee that this CCC is registered by the device without any error, the Host shall limit the maximum speed operation for this CCC to 1 MHz. In I3C Basic mode, it is illegal for Host to issue this CCC. When SETHID CCC is registered by the TS5, it updates MR7[3:1] with the HID code received by the TS5 and it takes in effect at the next Start operation (i.e. after Stop condition). Table 41 shows an example of a single SETHID CCC. As the device is in I²C mode when SETHID CCC is issued, the PEC function is not supported.

Once TS5 receives SETHID CCC and updates its 3-bit HID code, after the Stop operation, TS5 device only responds to updated 7-bit address. The 4-bit LID code of the TS5 device remains as is.

The Host may issue SETHID CCC more than one time.

Table 41. SETHID CCC - Broadcast

START	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	A/N/T	STOP
S or Sr	1	1	1	1	1	1	0	W = 0	A	
	0x61 (Broadcast)								T	
	0	0	0	0	0	0	0	0	T	P

DEVCTRL CCC

On a typical I3C Basic bus there can be up to 120 devices. For DDR5 DIMM application environment, there are up to 8 TS5 devices and behind each TS5 device, there are 4 local Target devices totaling up to 40 or more devices on I3C Basic bus. For certain operation such as enable or disable functions that are common to all devices (i.e. Packet Error Check), the Host must go through one device at a time which takes significant amount of time at initial power up. Further, it requires additional complexity on the Host because it must speak different protocol depending on how it may access the device until all devices are configured identically.

To help expedite this configuration operation and to simplify the Host complexity, the device supports the DEVCTRL CCC. The DEVCTRL CCC is supported either in I²C mode or I3C Basic mode of operation. In I²C mode, when the Host issues this CCC, to guarantee that this CCC is registered by the device without any error, the Host shall limit the maximum speed operation for this CCC to 1MHz. Table 42 to Table 43 shows an example of a single DEVCTRL CCC.

If PEC function is enabled, the PEC calculation starts with Start or Repeat Start operation but does not include 7'h7E with W = 0 byte in PEC calculation.

The Host shall pay attention to DEVCTRL CCC. If DEVCTRL CCC is used to access device specific registers (e.g. RegMod = '1'), the Host shall still follow any device specific register restriction. For example, if device specific register requires Stop operation for device to take in the effect of the setting, the Host must also use Stop operation when using DEVCTRL CCC to access device specific register.

Table 42. DEVCTRL CCC - Broadcast

START	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	A/N/T	STOP
S or Sr	1	1	1	1	1	1	0	W = 0	A (1)	
	0x62 (Broadcast)								T	
	AddrMask[2:0]			StartOffset[1:0]		PEC BL[1:0]		RegMod	T	
	DevID[6:0]							0	T (2)	
	Byte 0 Data Payload								T	
	Byte 1 Data Payload								T	
	Byte 2 Data Payload								T	
	Byte 3 Data Payload								T	Sr (3) or P

1. The TS5 NACKs if there is a parity error in a previous transaction when Host performs consecutive transactions with Repeat Start.
2. An exception is made for DEVCTRL CCC where device does report a parity error when it determines 7-bit device select code issued by the Host does not match with its own device code. If 7-bit device select code does not match but if parity is still valid, the device does not check for parity error in subsequent bytes; ignores the entire packet and waits until Stop or next Repeat Start operation.
3. Repeat Start or Repeat Start with 7'h7E.

DEVICE INTERFACE - PROTOCOL (continued)

Table 43. DEVCTRL CCC - Broadcast w/ PEC (1)

START	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	A/N/T	STOP
S or Sr	1	1	1	1	1	1	0	W = 0	A (2)	
	0x62 (Broadcast)								T	
	AddrMask[2:0]			StartOffset[1:0]		PEC BL[1:0]		RegMod	T	
	DevID[6:0]							0	T (3)	
	Byte 0 Data Payload								T	
	Byte 1 Data Payload								T	
	Byte 2 Data Payload								T	
	Byte 3 Data Payload								T	
	PEC								T	Sr (4) or P

1. DEVCTRL CCC with PEC check is only supported in I3C Basic mode.
2. The TS5 NACKs if there is a parity or PEC error in a previous transaction when Host performs consecutive transactions with Repeat Start.
3. An exception is made for DEVCTRL CCC where device does report a parity error when it determines 7-bit device select code issued by the Host does not match with its own device code. The device does not check for PEC as all subsequent bytes are discarded due to parity error. If 7-bit device select code does not match but if parity is still valid, the device does not check for parity error in subsequent bytes; ignores the entire packet and waits until Stop or next Repeat Start operation.
4. Repeat Start or Repeat Start with 7'h7E.

Table 44. DEVCTRL CCC Command Definition

PARAMETER	DEFINITION
AddrMask[2:0]	Broadcast, Unicast or Multicast Command Selection 000 = Unicast Command; TS5 device responds if DevID[6:0] field matches with TS5 device's own 7-bit address (4-bit LID + 3-bit HID) 011 = Multicast Command; TS5 device and possible other device respond if DevID[6:3] field matches with TS5 device's own 4-bit LID address 111 = Broadcast Command; All devices respond to this command All other encodings are reserved.
StartOffset[1:0]	Only applicable if RegMod = '0' Identifies the starting Byte (Byte 0 or Byte 1 or Byte 2 or Byte 3) for DEVCTRL CCC. Host can start at any Byte (from Byte 0 to Byte 3) and has continuous access to next byte until Stop operation. If Byte 3 is reached, the Host is responsible for applying Stop operation. 00 = Byte 0 01 = Byte 1 10 = Byte 2 11 = Byte 3
PEC BL[1:0]	Only applicable if RegMod = '0' and PEC function is enabled. Identifies the burst length just for this DEVCTRL CCC. The device uses the setting in this field to know when the PEC byte is expected after the data bytes. 00 = 1 Byte 01 = 2 Byte 10 = 3 Byte 11 = 4 Byte
RegMod	Identifies if DEVCTRL is going to be used for General Registers as identified in Byte 0 to Byte 3 or device specific address offset register. 0 = Access to General Registers in Byte 0 to Byte 3 (i.e. StartOffset[1:0] = Valid) 1 = Device Specific Offset Address (i.e. StartOffset[1:0] and PECBL[1:0] is a don't care and does not apply). The Host shall NOT use RegMod = '1' with Broadcast Command if there are different types of devices on the I3C Basic bus.
DevID[6:0]	Identifies 7-bit device address. Device responds to DEVCTRL CCC data packet depending on AddrMask[2:0]. If AddrMask[2:0] = '111', DevID[6:0] is a don't care and device always responds. If AddrMask[2:0] = '000', DevID[6:0] must match for device to respond. If AddrMask[2:0] = '011', DevID[6:3] must match for device to respond. DevID[2:0] is don't care. For any other codes for AddrMask[2:0], the device always NACKs.

DEVICE INTERFACE - PROTOCOL (continued)

Table 45. DEVCTRL CCC Data Payload Definition

BYTES	BITS	FUNCTION	DEFINITION	COMMENT
Byte 0	D[7]	PEC Enable	0 = Disable 1 = Enable	MR18[7] is updated
	D[6]	Parity Disable	0 = Disable 1 = Enable	MR18[6] is updated
	D[5:2]	RFU	RFU	
	D[1]	RSVD	0 = RSVD 1 = RSVD	TS5 device always ignores this bit.
	D[0]	RFU	RFU	
Byte 1	D[7:4]	RFU	RFU	
	D[3]	Global and IBI Clear	0 = No Action 1 = Clear All Event and pending IBI (1)	MR27[7] is updated.
	D[2:0]	RFU	RFU	
Byte 2	D[7:0]	RFU	RFU	
Byte 3	D[7:0]	RFU	RFU	

1. After Target device clears the event, the device can still have certain registers set to '1' if the event is still present in which case, the device will generate an IBI again at the next opportunity.

DEVICE INTERFACE - PROTOCOL (continued)

DEVCTRL CCC Examples - RegMod = '0'

Table 46 shows an example of DEVCTRL CCC data packet. It assumes that all devices on the bus are already in I3C Basic mode with PEC function disabled and parity function enabled. In this example, the Host uses DEVCTRL CCC as Multicast command. Host sends Multicast command to all devices with 4-bit LID code of '1001' on I3C Basic bus to do VR Enable followed by all devices with 4-bit LID code of '0110' to disable parity function. The Host sends AddrMask = '011' to indicate Multicast command with DevID[6:3] match; StartOffset = '00' to indicate starting Byte 0 and RegMod = '0' to indicate general register. Upon receiving this command, all devices with DevID[6:3] that matches to '1001' will do the VR Enable command and DevID[6:3] that matches to '0110' with disable the parity function.

Table 46. DEVCTRL CCC Example - Multicast Command to '1001' and '0110' Devices

START	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	A/N/T	STOP
S	1	1	1	1	1	1	0	W = 0	A (1)	
	0x62 (Broadcast)								T	
	011			00		00		0	T	
	1001 000							0	T	
	0000 0010								T	
Sr	1	1	1	1	1	1	0	W = 0	A (1)	
	0x62 (Broadcast)								T	
	011			00		00		0	T	
	0110 000							0	T	
	0100 0000								T	P

1. See Figure 10 to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation.

Table 47 shows an example of DEVCTRL CCC data packet. It assumes that all devices on the bus are already in I3C Basic mode with PEC function disabled and parity function enabled. In this example, the Host uses DEVCTRL CCC as Broadcast command to enable PEC function. The Host sends AddrMask = '111' to indicate Broadcast command; StartOffset = '00' to indicate starting Byte 0 and RegMod = '0' to indicate general register. Upon receiving this command, all devices will enable PEC function.

Table 47. DEVCTRL CCC Example - Broadcast Command to all Devices

START	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	A/N/T	STOP
S	1	1	1	1	1	1	0	W = 0	A (1)	
	0x62 (Broadcast)								T	
	111			00		00		0	T	
	0000 000							0	T	
	1000 0000								T	P

1. See Figure 10 to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation.

Table 48 shows an example of DEVCTRL CCC data packet. It assumes that all devices on the bus are already in I3C Basic mode with PEC function disabled and parity function enabled. In this example, the Host uses DEVCTRL CCC as Unitcast command to enable VR on DIMM5. The Host sends AddrMask = '000' to indicate Unicast command; StartOffset = '00' to indicate starting Byte 0 and RegMod = '0' to indicate general register. Upon receiving this command, PMIC on DIMM5 will enable its regulator.

Table 48. DEVCTRL CCC Example - Unicast Command to PMIC on DIMM5

START	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	A/N/T	STOP
S	1	1	1	1	1	1	0	W = 0	A (1)	
	0x62 (Broadcast)								T	
	000			00		00		0	T	
	1001 101							0	T	
	0000 0010								T	P

1. See Figure 10 to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation.

DEVICE INTERFACE - PROTOCOL (continued)

DEVCTRL CCC Examples - RegMod = '1'

Table 49 shows an example of DEVCTRL CCC data packet for the purpose of configuring device specific address offset register. It assumes that all devices on the bus are already in I3C Basic mode with PEC function enabled and parity function enabled. In this example, the Host sends Multicast command to all devices with 4-bit LID code of '0010' on the I3C Basic bus to write to address offset of 0x1C and 0x1D with data 0xFF and 0x55 respectively followed by all devices with 4-bit LID of '1001' on the I3C Basic bus to write to address offset of 0x15 with data 0x78.

The PEC calculation starts with Start or Repeat Start operation but does not include 7'h7E with W = 0 byte in PEC calculation.

Table 49. DEVCTRL CCC Example - Multicast Command to '0010' and '1001' Devices

START	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	A/N/T	STOP
S	1	1	1	1	1	1	0	W = 0	A[1]	
	0x62 (Broadcast)								T	
	011			00		00		1	T	
	0010 000							0	T	
	0001 1100 (address offset 0x1C)								T	
	0010 0000 (CMD field = 2 bytes of data)								T	
	1111 1111 (data)								T	
	0101 0101 (data)								T	
	PEC								T	
Sr	1	1	1	1	1	1	0	W = 0	A[1]	
	0x62 (Broadcast)								T	
	011			00		00		1	T	
	1001 000							0	T	
	0001 0101 (address offset 0x15)								T	
	0000 0000 (CMD field = 1 byte of data)								T	
	0111 1000 (data)								T	
	PEC								T	P

Table 50 shows an example of DEVCTRL CCC data packet for the purpose of configuring device specific address offset register. It assumes that all devices on the bus are already in I3C Basic mode with PEC function disabled and parity function enabled. In this example, the Host sends Multicast command to all devices with 4-bit LID code of '1001' on the I3C Basic bus to write to address offset of 0x13 with data 0xFF and it continues to write data 0x01 to the next address.

Table 50. DEVCTRL CCC Example - Multicast Command to '1001' Devices

START	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	A/N/T	STOP
S	1	1	1	1	1	1	0	W = 0	A[1]	
	0x62 (Broadcast)								T	
	011			00		00		1	T	
	1001 000							0	T	
	0001 0011 (address offset 0x13)								T	
	1111 1111 (data)								T	
	0000 0001 (data)								T	P

1. See Figure 10 to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation.

IN BAND INTERRUPT (IBI)

In I²C mode, in band interrupt function is not supported. Only I3C Basic mode supports in band interrupt function.

Enabling and Disabling In Band Event Interrupt Function

By default, all interrupt sources are disabled (i.e. set to '0'). The Host may enable following interrupts in the TS5 device. Once enabled, the TS5 device sends an IBI when that event occurs.

1. Error Interrupt Enable in MR27[4]:

- When MR27[4] = '1', the device sends the IBI at next available opportunity when any of the register bit in MR52[1:0] is set to '1' and sets MR48[7] = '1' and updates Pending Interrupt Bits [3:0] = '0001' for GETSTATUS CCC.
- When MR27[4] = '0', the device does not send the IBI regardless of the register bit status in MR52[1:0]. However, the device does set MR48[7] = '1' and updates Pending Interrupt Bits [3:0] = '0001' for GETSTATUS CCC.

2. Temperature Sensor Interrupt Enable in MR27[3:0]: The Host can set any combination of register bits to '1':

- When any of the register bits in MR27[3:0] = '1' and if MR27[4] = '1', the device sends the IBI at next available opportunity when the corresponding register bit in MR51[3:0] is set to '1' and sets MR48[7] = '1' and updates Pending Interrupt Bits [3:0] = '0001' for GETSTATUS CCC.
- When any of the register bits in MR27[3:0] = '0' or MR27[4] = '0', the device does not send the interrupt regardless of the corresponding register bit status in MR51[3:0]. However, the device does set MR48[7] = '1' and updates Pending Interrupt Bits [3:0] = '0001' for GETSTATUS CCC if any of the bits in MR27[3:0] = '1' and MR27[4] = '0'.

Mechanics of Interrupt Generation

Event interrupts may be generated by the local device if IBI is enabled. When there is a pending interrupt (i.e. MR48[7] = '1) and if IBI is enabled (i.e. MR27[4] = '1'), the TS5 device requests an interrupt after detecting Start condition by transmitting its 7-bit binary address (LID bits followed by HID bits) followed by R/W = '1' on the SDA bus serially (synchronized by SCL falling transitions).

If TS5 device detects no Start condition but if the I3C Basic bus (SDA and SCL) has been inactive (no edges seen) for t_{AVAL} period, then the TS5 device may assert SDA low by t_{IBI_ISSUE} time to request an interrupt. When the TS5 device requests an interrupt, the Host toggles the SCL. The TS5 device transmits its 7-bit binary address (LID bits followed by HID bits) followed by R/W bit = '1' to the Host.

When the TS5 device requests an interrupt, the Host may take one of the two actions below.

- The Host sends ACK on 9th bit to accept the interrupt request. At this point, if the TS5 device confirms that it has won the arbitration, the TS5 device transmits the IBI payload as shown in Table 51 and Table 52 for PEC disabled and PEC enabled configuration, respectively. See Figure 15. It just shows only first two data bits of the MDB byte to illustrate the timing. The interrupt payload contains MDB followed by 8-bit register contents of MR51 and MR52 in order. The Host then issues the Stop command. Note the timing waveform in Figure 15. The Host then accepts the IBI payload if it sends an ACK on 9th bit to accept the interrupt request. The Host can interrupt the IBI payload at 'T'. If Host stops the IBI payload at 'T' bit in the middle of payload, the TS5 device retains the IBI status flag MR48[7] = '1' and Pending Interrupt Bits [3:0] internally and waits for the next opportunity to request an interrupt. If the TS5 device successfully transmits the entire IBI payload, it then clears IBI status flag MR48[7] = '0' and Pending Interrupt Bits [3:0] = '0000' on its own and does not request for an IBI again unless there is another different event occurs; for another same event, the device does not request for an IBI.
- The Host sends NACK on the 9th bit as shown in Figure 16 followed by a Stop command. In this case, the TS5 device does not transmit the IBI payload and waits for the next opportunity to request an interrupt. At this point, though Host sent a NACK, it does have a knowledge of which TS5 device sent the IBI request. The TS5 retains the IBI status flag MR48[7] = '1' and Pending Interrupt Bits [3:0] = '0001'.

IN BAND INTERRUPT (IBI) (continued)

Table 51. TS5 IBI Payload Packet; PEC is Disabled

START	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	A/N/T	STOP
S	0	X	1	0	HID			R = 1	A (1)	
	MDB = 0x00								T = 1	
	MR51[7:0]								T = 1	
	MR52[7:0]								T = 0 (2)	P

1. See Figure 11 to see how the transition occurs from Host Open Drain (ACK) to Target Push Pull Operation (1st bit of MDB, bit [7]).
2. See Figure 14 to see how Target device ends the operation followed by Host Stop operation.

Table 52. TS5 IBI Payload Packet; PEC is Enabled

START	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	A/N/T	STOP
S	0	X	1	0	HID			R = 1	A (1)	
	MDB = 0x00								T = 1	
	MR51[7:0]								T = 1	
	MR52[7:0]								T = 1	
	PEC								T = 0 (2)	P

1. See Figure 11 to see how the transition occurs from Host Open Drain (ACK) to Target Push Pull Operation (1st bit of MDB, bit [7]).
2. See Figure 14 to see how Target device ends the operation followed by Host Stop operation.

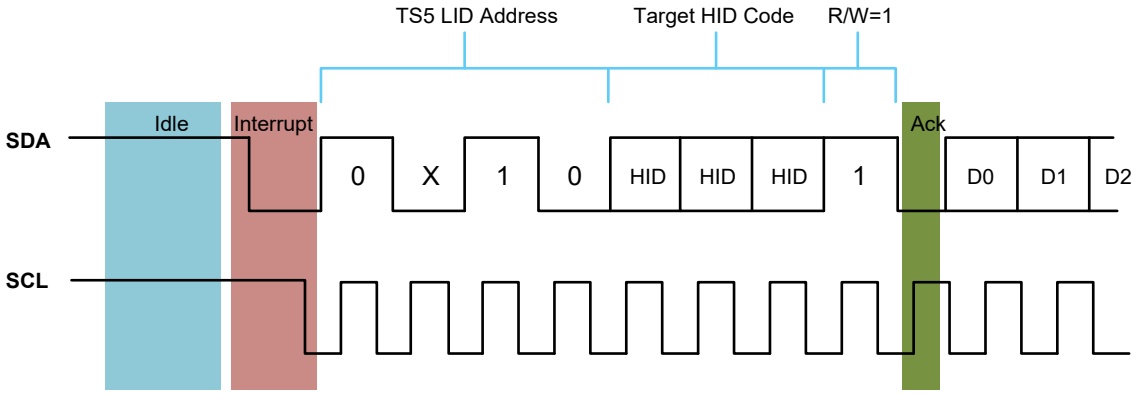


Figure 15. TS5 Interrupt; Host Ack Followed by TS5 Device IBI Payload

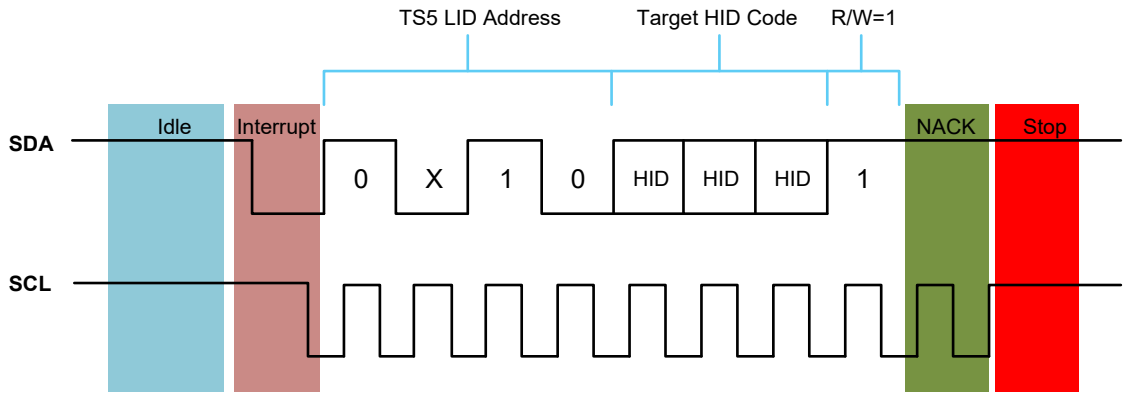


Figure 16. TS5 Interrupt; Host NACK followed by Stop

IN BAND INTERRUPT (IBI) (continued)

Interrupt Arbitration

As there are multiple devices I3C Basic bus, multiple devices may request an interrupt when the Host I3C Basic bus is inactive for t_{AVAL} period. Arbitration process is required.

For DDR5 DIMM application environment, there could be up to total of 13 difference devices including the TS5 on I3C Basic bus.

On a typical DDR5 DIMM application environment, all devices have the same 3-bit HID code. Hence the arbitration is always won by the lowest 4-bit LID code. For example, if one TS5 Target device has LID code of '0010' and other device (PMIC) has a LID code of '1001', through the arbitration process, the LID code of TS5 '0010' wins. The other device (PMIC) with a LID code of '1001' must release the bus and wait for next opportunity to request an interrupt. Table 53 shows the arbitration priority based on the LID code for the local devices. The Green color cells in Table 53 are the likely devices that will be on a standard DDR5 RDIMM or DDR5 LRDIMM.

Table 53. Interrupt Arbitration - Among Local Target Devices

DEVICE	TARGET DEVICE LID CODE	TARGET DEVICE HID CODE	ARBITRATION PRIORITY
N/A	0000	N/A	N/A
RFU	0001	111	1
TS0	0010	111	2
RFU	0011	111	3
RFU	0100	111	4
RFU	0101	111	5
TS1	0110	111	6
RFU	0111	111	7
PMIC1	1000	111	8
PMIC0	1001	111	9
SPD Hub	1010	HID	N/A
RCD	1011	111	10
PMIC2	1100	111	11
RFU	1101	111	12
RFU	1110	111	13
N/A	1111	N/A	N/A

In an uncommon but possible scenario would be that at the exact same time as when the Hub or local Target devices (i.e. TS5) are requesting an interrupt, the Host is starting an operation to the Hub or local Target devices (i.e. TS5). When this happens, Host also gets involved in the arbitration process along with the Hub or the local Target devices (i.e. TS5). During the arbitration phase, there will be always only one winning device and it could be either the Hub or the local Target device (i.e. TS5) or the Host.

If the Host wins during the arbitration phase, it continues with normal operation. The losing Hub or local Target device waits for next opportunity to send an interrupt.

If the Host loses during the arbitration phase, it must let go of the bus. When the Host loses during the arbitration, the Host must let the Hub or local Target device (i.e. TS5) finish sending its 4-bit LID code followed by 3-bit HID code followed by R/W = '1'. At this point, during the 9th bit, the Host has two options to take the action as noted below:

- Host sends an ACK to accept the interrupt and hence accepts the IBI payload from the winning SDP5 Hub or local Target device (i.e. TS5). After the IBI payload, the Host issues Stop operation.
- Host sends an NACK followed by Stop operation.

In a rare but still possible scenario would be that at the exact same time as when the TS5 device is requesting an interrupt, the Host is starting an operation to the same TS5. When this happens, neither Host nor the TS5 knows it is a winner until the 8th bit and Host always wins. This is because, the TS5 sends R = 1 (8th bit) during the interrupt. The Host sets W = 0 (8th bit) during the operation. As a result, the Host wins and the TS5 must let go of the bus and wait for the next opportunity to send an interrupt.

IN BAND INTERRUPT (IBI) (continued)

In an extreme rare but still possible scenario would be that at the exact same time as when the TS5 device is requesting an interrupt, the Host is requesting a read operation with Default Read Address pointer mode to the same TS5 device. When this happens, there is no winning device. This is the only time there is no winning device. This is because, the TS5 device sends R = 1 (8th bit) during the interrupt and Host also sends R = 1 for read request with Default Read Address pointer mode. As a result, there is no winner because Host is waiting for TS5 to ACK and TS5 is waiting for Host to ACK. In this case, neither Host nor TS5 will ACK. Since there is no ACK (i.e. NACK) by either device, the Host must time out and repeats the read request with Repeat Start. When Host repeats the read request with Repeat Start, the TS5 does not send an interrupt because of Repeat Start.

Clearing Device Status and IBI Status Registers

The TS5 device provides the IBI status in MR48[7] by setting it to '1'. The TS5 device clears the IBI status register MR48[7] to '0' automatically when it sends a complete IBI (including payload and without interruption) and it also clears Pending Interrupt Bits [3:0] to '0000'. Once IBI status register is cleared, the TS5 does not request for an IBI again unless another event occurs.

The TS5 device provides the device status in MR51 and MR52 registers. The status information in MR51 and MR52 are latched and remains set even after the TS5 device sends IBI payload and clears the IBI status register MR48[7] to '0'. The Host must explicitly clear the status register through Clear command by writing '1' for appropriate status or by issuing a Global Clear command.

After Host issues Clear command, if the condition is no longer present, the TS5 device clears the appropriate status register, clears the IBI status register to '0' and Pending Interrupt Bits [3:0] to '0000' even if the TS5 device has not sent the IBI. After Host issues Clear command, if the condition is still present, the device will again set the appropriate status register, sets the IBI status register to '1' and Pending Interrupt Bits [3:0] to '0001' even if the device has already sent the IBI and entire IBI payload.

ERROR CHECK FUNCTION

Packet Error Check (PEC) Function

In I²C mode, packet error checking is not supported. Only I3C Basic mode supports packet error checking.

The TS5 device implements an 8-bit Packet Error Code (PEC) which is appended at the end of all transactions if PECs is enabled through DEVCTRL CCC. The PEC is a CRC-8 value calculated on all the message bytes except for Start, Repeated Start, Stop conditions or 'T' bits, ACK and NACK and IBI header (7'h7E followed by W = 0) bits.

The polynomial for CRC-8 calculations is:

$$C(X) = X^8 + X^2 + X^1 + 1 \quad (1)$$

The seed value for PEC function is all zero.

When Host calculates PEC for TS5 device, it includes LID and HID bits followed by R/W bit.

Parity Error Check Function

In I²C mode, parity error checking is not supported except for supported CCCs. Only I3C Basic mode supports parity error checking.

By default, when TS5 device is put in I3C Basic mode, parity function is automatically enabled. The Host can disable the function after it is enabled. Host can only disable the parity function with DEVCTRL CCC (RegMod = '0'). When parity function is disabled, the TS5 device simply ignores the 'T' bit information from the Host. The Host may actually choose to compute the parity and send that information during 'T' bit or simply drive static low or high in 'T' bit.

The TS5 device implements ODD parity. If an odd number of bits in the byte are '1', the parity bit value is '0'.

If even number of bits in the byte are '1', the parity bit value is '1'. The Host computes the parity and sends it during 'T' bit.

Packet Error Check and Parity Error Handling

There are two types of error checking done by the TS5 device: parity error checking and packet error checking. By default, the parity error checking is always enabled and packet error checking is disabled when the TS5 device is put in I3C Basic mode. The Host may enable the packet error checking at any time. The parity error is calculated for each byte. The Host sends parity error information in 'T' bit.

I3C Basic defines TE0, TE1, TE2, TE3, TE4, TE5, TE6 error detection for Target devices. Only TE1 and TE2 error detection is supported by the TS5 for parity checking. All other errors are not supported and not applicable.

Write Command Data Packet Error Handling - PEC Disabled

The TS5 device checks for the parity error for each byte in a packet except for the device select code byte that it receives from the Host as shown in Table 9.

Write command - if no parity error:

- The TS5 device executes the command.

Write command - if parity error:

- The TS5 device discards the byte in the packet that had a parity error.
- The TS5 device discards all subsequent bytes in that packet until the Stop operation. The TS5 device may or may not check parity for all sub-sequent bytes in that packet.
- Note that as the packet contains more than one byte, if first byte had no parity error but the second byte had a parity error, the TS5 device may or may not execute the first byte operation but second byte and all subsequent bytes operations are discarded.
- The TS5 device sets the MR52[0], MR48[7] and P_Err in GETSTATUS CCC to '1'; updates Pending Interrupt Bits [3:0] to '0001' and waits for the next opportunity to send an in band interrupt if IBI is enabled.

ERROR CHECK FUNCTION (continued)

Read Command Data Packet Error Handling - PEC Disabled

The TS5 device checks for parity error for each byte in a packet except for the device select code byte that it receives from the Host prior to Repeat Start as shown in Table 13.

The TS5 device does not compute the parity when it sends the data to the Host. The Host does not check for parity error for the bytes that TS5 device sends. The TS5 device sends Continuous (‘1’) or Stop (‘0’) information during ‘T’ bit.

Read Command - If no parity error:

- The TS5 sends ACK back to the Host when Host performs Start Repeat operation.
- The TS5 device executes the command and sends the data as shown in Table 13.

Read Command - If parity error:

- The TS5 device discards the byte in the packet that had a parity error.
- The TS5 device discards second byte in that packet if the parity error occurred in first byte. The TS5 device may or may not check the parity for second byte in that packet.
- The TS5 sends NACK back to the Host when Host performs a Start Repeat operation. This is shown in the RED color cell in Table 13. The NACK represents either a parity error in one of the two bytes or that TS5 is not able to start the read operation. The Host may re-try Repeat Start again. The Host may do the Repeat Start as many times as it may desire. If the TS5 device NACKs due to parity error in a previous byte from the Host, it will always NACK regardless of how many times Host tries Repeat Start.
- The TS5 does not send the data shown in Table 13 and instead expects Host to perform Stop operation.
- The TS5 device sets MR52[0] and MR48[7] and P_Err in GETSTATUS CCC to ‘1’; updates Pending Interrupt Bits [3:0] in GETSTATUS to ‘0001’ and waits for the next opportunity to send an in band interrupt if IBI is enabled.

Write Command Data Packet Error Handling - PEC Enabled

The TS5 device checks for the parity error for each byte in a packet except for the device select code byte that it receives from the Host as shown in Table 10. Further, the TS5 device checks for the packet error for the entire packet (from Start condition until last byte of Data) that receives from the Host as shown in Table 10.

Write command - if no parity error:

- The TS5 device waits for the entire packet. If no error in packet, the TS5 device executes the command. If there is an error in the packet, the TS5 device discards the entire packet and does not execute that packet and waits for Stop, sets the MR52[1] and MR48[7] to ‘1’ and PEC_Err in GETSTATUS CCC to ‘1’ and updates Pending Interrupt Bits [3:0] in GETSTATUS CCC to ‘0001’ and waits for the next opportunity to send in band interrupt if IBI is enabled.

Write command - if parity error:

- The TS5 device discards that byte and the entire packet until Stop operation.
- The TS5 device sets MR52[0] and MR48[7] and P_Err in GETSTATUS CCC to ‘1’; updates Pending Interrupt Bits [3:0] in GETSTATUS CCC to ‘0001’ and waits for the next opportunity to send in band interrupt if IBI is enabled.
- The TS5 device may or may not check the error for the packet. If the TS5 device checks for the packet error, likely it will detect an error in the packet and the device may also set MR52[1] and PEC_Err in GETSTATUS CCC to ‘1’ as well.

ERROR CHECK FUNCTION (continued)

Read Command Data Packet Error Handling - PEC Enabled

The TS5 device checks for the parity error for each byte in a packet except for the device select code byte that it receives from the Host prior to Repeat Start as shown in Table 14.

The TS5 device does not compute the parity when it sends the data to the Host. It does not check for parity error for the bytes shown in Table 14. The TS5 device sends Continuous (‘1’) or Stop (‘0’) information during ‘T’ bit when TS5 device is sending the read data.

The TS5 device checks for the PEC error for a packet that it receives from the Host from Start condition to Repeat Start condition (from first device select code followed by the address offset and CMD byte).

The TS5 device computes the packet error code for the entire packet starting with Repeat Start (device select code and the data TS5 device transmits back to Host)

Read command - If no parity error and no PEC error:

- The TS5 sends ACK back to the Host when Host performs a Start Repeat operation.
- The TS5 device executes the command and sends the data as shown in Table 14.
- The TS5 computes PEC for the bytes (from Start condition to PEC byte prior to Repeat Start) shown in Table 14.

Read command - if parity error or PEC error:

- The TS5 device discards the byte in the packet that had a parity error.
- The TS5 device discards second byte in that packet if a parity error occurred in first byte. The SPD5 Hub device may or may not check parity for the second byte in that packet.
- The TS5 device discards the packet if there is a PEC error.
- The TS5 sends NACK back to the Host when Host performs Start Repeat operation.

This is shown in the RED color cell in Table 14. The NACK represents either PEC error or a parity error in one of the three bytes or that TS5 is not able to start the read operation. The Host may re-try Repeat Start again. The Host may do the Repeat Start as many times it may desire. The PEC calculation by TS5 device only includes device select code of the ACK responses of the Repeat Start operation. In other words, if there are more than one Repeat Start operation, the TS5 device includes the device select of only the last Repeat Start from the Host when it ACKs in PEC calculation and other NACK responses of the device select codes of the Repeat Start are not included in PEC calculation. If the TS5 device NACKs due to PEC error or a parity error in previous bytes from Host, it will always NACK regardless of how many times Host tries Repeat Start.

- The TS5 does not send any data shown in Table 14 and instead expects Host to perform Stop operation.
- The TS5 device sets MR52[0] and MR48[7] and P_Err in GETSTATUS CCC to ‘1’ for parity error and MR52[1] and MR48[7] and PEC_Err in GETSTATUS CCC to ‘1’ for PEC error. Further, the TS5 updates Pending Interrupt Bits [3:0] in GETSTATUS CCC to ‘0001’ and waits for the next opportunity to send an in band interrupt if IBI is enabled.

CCC Packet Error Handling

Parity error and PEC error detected in a CCC packet are handled in the same way as described for normal Read/Write operations.

Error Reporting

All error conditions including PEC error check and parity error check detected by the TS5 devices are captured in MR51 and MR52 registers.There are three different possible ways error information can be communicated to the Host.

1. The Host makes the read request to MR51 and MR52 registers.
2. The Host starts any transaction with 7’h7E IBI header (only applicable in I3C mode).
3. The TS5 device sends in band interrupt if enabled, when its SCL and SDA input has been idle for t_{AVAL} time (only applicable in I3C Basic mode).

COMMAND TRUTH TABLE

The command truth table as shown in Table 54 only applies in I3C Basic mode with PEC enabled. In I²C mode and I3C Basic mode with PEC disabled, the command truth table does not apply.

Table 54. For I3C Basic Mode Only w/ PEC Enabled - Command Truth Table

TS5 Command	Command Name	Command Code	R/W	Address
		2nd Byte Bits [7:5]	2nd Byte Bit [4]	1st Byte Bits [5:0]
Write 1 Byte to Register	W1R	000	0	V
Read 1 Byte from Register	R1R		1	V
Write 2 Byte to Register	W2R	001	0	V
Read 2 Byte from Register	R2R		1	V
Reserved	RSVD	010 to 111	RSVD	RSVD

REGISTERS

Register Attribute Definition

All volatile registers have Base Attributes as defined in Table 55. Some register attributes are further modified with Attribute Modifiers, as defined in Table 56.

The volatile register space has a continuous address.

Table 55. Register Base Attributes

ATTRIBUTE	ABBREVIATION	DESCRIPTION
Read Only	R	This bit can be read by software. Writes have no effect.
Read/Write	RW	This bit can be read or written by software.
Write Only	W	This bit can only be written by software.
Reserved	RV	This bit is reserved for future expansion and its value must not be modified by software. The bit will return ‘0’ when read. When writing this bit, software must preserve the value read unless otherwise indicated.

Table 56. Register Attribute Modifier

ATTRIBUTE	ABBREVIATION	DESCRIPTION
Write 1 Only	1O	This bit can only be set (i.e. write ‘1’) but not reset (i.e. write ‘0’)
Persistent	E	Persistent.

REGISTERS (continued)

Table 57. Register Map

REGISTER NAME	REGISTER ADDRESS (HEX)	ATTRIBUTE	DESCRIPTION
MR0	0x00	ROE	Device Type; Most Significant Byte
MR1	0x01	ROE	Device Type; Least Significant Byte
MR2	0x02	ROE	Device Revision
MR3	0x03	ROE	Vendor ID Byte 0
MR4	0x04	ROE	Vendor ID Byte 1
MR5 - MR6	0x05 - 0x06	RV	Reserved
MR7	0x07	RO	Device Configuration; HID
MR8 - MR17	0x08 - 0x11	RV	Reserved
MR18	0x12	RO, RW	Device Configuration
MR19	0x13	1O	Clear Register MR51 Temperature Status Command
MR20	0x14	1O	Clear Register MR52 Error Status Command
MR21 - MR25	0x15 - 0x19	RV	Reserved
MR26	0x1A	RW	TS Configuration
MR27	0x1B	1O, RO, RW	Interrupt Configurations
MR28	0x1C	RW	TS Temperature High Limit Configuration - Low Byte
MR29	0x1D	RW	TS Temperature High Limit Configuration - High Byte
MR30	0x1E	RW	TS Temperature Low Limit Configuration - Low Byte
MR31	0x1F	RW	TS Temperature Low Limit Configuration - High Byte
MR32	0x20	RW	TS Critical Temperature High Limit Configuration – Low Byte
MR33	0x21	RW	TS Critical Temperature High Limit Configuration – High Byte
MR34	0x22	RW	TS Critical Temperature Low Limit Configuration – Low Byte
MR35	0x23	RW	TS Critical Temperature Low Limit Configuration – High Byte
MR36 - MR47	0x24 - 0x2F	RV	Reserved for Device Configuration Type of Registers
MR48	0x30	RO	Device Status
MR49	0x31	RO	TS Current Sensed Temperature - Low Byte
MR50	0x32	RO	TS Current Sensed Temperature - High Byte
MR51	0x33	RO	TS Temperature Status
MR52	0x34	RO	Misc. Error Status
MR53 - MR79	0x35 - 0x4F	RV	Reserved
MR80	0x50	ROE	Serial Number Byte 0
MR81	0x51	ROE	Serial Number Byte 1
MR82	0x52	ROE	Serial Number Byte 2
MR83	0x53	ROE	Serial Number Byte 3
MR84	0x54	ROE	Serial Number Byte 4
MR85 - MR127	0x55 - 0x7F	RV	Reserved
MR127 - MR255	0x80 - 0xFF	RV	Reserved for Vendor Specific Registers

REGISTERS (continued)

Thermal Sensor Registers Read Out Mechanism

All thermal registers are 16-bit quantities stored in two consecutive registers; low byte first and then high byte. Five bits are reserved for future use. Reserved bits are Read only bits and must be set to '0' when Host writes to low and high bytes. The device returns '0' in reserved bits when Host reads from the low and high bytes. Remaining 11 bits in these paired registers form a signed value of multiples of 0.25 ranging from -256.00 to + 255.75. Units for all thermal registers are ℃.

The format of each pair of thermal registers is shown in Table 58 below.

Table 58.Thermal Register - Low Byte and High Byte

REGISTER		BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
MRX	Low Byte	8	4	2	1	0.5	0.25	Reserved	Reserved
MRX + 1	High Byte	Reserved	Reserved	Reserved	Sign	128	64	32	16

Bit 'Sign' decides whether the readout temperature is positive or negative. The examples (reserved bits in grey, sign bit highlighted in blue) is shown in Table 59 below.

Table 59. Thermal Register Examples

HIGH BYTE	LOW BYTE	VALUE	UNITS
0000 0101	1111 0000	+95.00	℃
0000 0101	0101 0000	+85.00	℃
0000 0100	1011 0000	+75.00	℃
0000 0000	0001 0000	+1.00	℃
0000 0000	0000 1100	+0.75	℃
0000 0000	0000 1000	+0.50	℃
0000 0000	0000 0100	+0.25	℃
0000 0000	0000 0000	0.00	℃
0001 1111	1111 1100	-0.25	℃
0001 1111	1111 1000	-0.50	℃
0001 1111	1111 0100	-0.75	℃
0001 1111	1111 0000	-1.00	℃
0001 1101	1000 0000	-40.00	℃

REGISTER DESCRIPTION

REG0x00: MR0 Register: Device Type; Most Significant Byte

BITS	BIT NAME	TYPE	DEFAULT	DESCRIPTION
D[7:0]	MSB_DEV_TYPE[7:0]	ROE	-	Device Type (1) - These are hard coded. 0x51: Temperature Sensor without Serial Number 0x52: Temperature Sensor with Serial Number

1. The code in this register is used in conjunction with any device type in MR1 register.

REG0x01: MR1 Register: Device Type; Least Significant Byte

BITS	BIT NAME	TYPE	DEFAULT	DESCRIPTION
D[7:0]	LSB_DEV_TYPE[7:0]	ROE	0x11	Device Type (1) - Temperature Sensor - These are hard coded. 0x11: Grade A Temperature Sensor

1. The code in this register is used in conjunction with any device type in MR0 register.

REG0x02: MR2 Register: Device Revision

BITS	BIT NAME	TYPE	DEFAULT	DESCRIPTION
D[7:6]	Reserved	RV	0	Reserved
D[5:4]	DEV_REV_MAJOR[1:0]	ROE	00	Major Revision 00 = Revision 1 (default) 01 = Revision 2 10 = Revision 3 11 = Revision 4
D[3:1]	DEV_REV_MINOR[2:0]	ROE	000	Minor Revision 000 = Revision 0 (default) 001 = Revision 1 010 = Revision 2 … 111 = Revision 7
D[0]	Reserved	RV	0	Reserved

REG0x03: MR3 Register: Vendor ID Byte 0

BITS	BIT NAME	TYPE	DEFAULT	DESCRIPTION
D[7:0]	VENDOR_ID_BYTE0[7:0]	ROE	0x0E	Vendor ID Byte 0

REG0x04: MR4 Register: Vendor ID Byte 1

BITS	BIT NAME	TYPE	DEFAULT	DESCRIPTION
D[7:0]	VENDOR_ID_BYTE1[7:0]	ROE	0x8F	Vendor ID Byte 1

REG0x07: MR7 Register: Device Configuration; HID

BITS	BIT NAME	TYPE	DEFAULT	DESCRIPTION
D[7:4]	Reserved	RV	0000	Reserved
D[3:1]	DEV_HID_CODE[2:0]	RO	111	Device HID Code (1). The TS5 device responds to unique 7-bit address as formed by 4 bit LID code as in Table 5 and 3-bit HID code as configured in this register. This register is updated when SETHID CCC is registered by the TS5 device or when TS5 device goes through bus reset as described in ***Bus Reset Section***.
D[0]	Reserved	RV	0	Reserved

1. The write (or update) transaction to this register must be followed by Stop operation to allow the TS5 device to update the setting.

REGISTER DESCRIPTION (continued)

REG0x12: MR18 Register: Device Configuration (1)

BITS	BIT NAME	TYPE	DEFAULT	DESCRIPTION
D[7]	PEC_EN	RO	0	PEC Enable (2) (3) 0 = Disable (default) 1 = Enable
D[6]	PAR_DIS	RO	0	Parity ('T' bit) Disable (3) (4) 0 = Enable (default) 1 = Disable
D[5]	INF_SEL	RO	0	Interface Selection 0 = I²C Protocol (Max speed of 1 MHz) (default) 1 = I3C Basic Protocol (5)
D[4]	DEF_RD_ADDR_POINT_EN	RW	0	Default Read Address Pointer Enable 0 = Disable Default Read Address Pointer (Address pointer is set by the Host) (default) (6) 1 = Enable Default Read Address Pointer; Address selected by register bits [3:2]
D[3:2]	DEF_RD_ADDR_POINT_START[1:0]	RW	00	Default Read Pointer Starting Address (7) 00 = MR49 (default) 01 = Reserved 10 = Reserved 11 = Reserved
D[1]	DEF_RD_ADDR_POINT_BL	RW	0	Burst Length for Read Pointer Address for PEC Calculation (8) 0 = 2 Bytes (default) 1 = 4 Bytes
D[0]	Reserved	RV	0	Reserved

1. The write (or update) transaction to this register must be followed by Stop operation to allow the TS5 device to update the setting.
2. This register is only applicable if MR18[5] = '1'.
3. This register is updated when RSTDAA CCC is registered by TS5 device or when TS5 device goes through bus reset as described in ***Bus Reset Section***.
4. This register is only applicable if MR18[5] = '1'. When parity function is disabled, the TS5 device simply ignores the 'T' bit information from the Host. The Host may actually choose to compute the parity and send that information in 'T' bit or simply drive static low or high in 'T' bit.
5. This register is automatically updated when SETAASA CCC or RSTDAA CCC is registered by the TS5 device or when TS5 device goes through bus reset as described in ***Bus Reset Section***. This register can be read by the Host through normal Read operation but it cannot be written with normal write operation either in I²C mode or I3C Basic mode of operation. When this register is updated, it takes in effect when there is a next Start operation (i.e. after Stop operation).
6. The setting in register MR18[3:1] is don't care.
7. This register is only applicable if MR18[4] = '1'.
8. This register is only applicable if MR18[4] = '1', MR18[7] = '1'.

REG0x13: MR19 Register: Clear Register MR51 Temperature Status Command (1)

BITS	BIT NAME	TYPE	DEFAULT	DESCRIPTION
D[7:4]	Reserved	RV	0000	Reserved
D[3]	CLR_TS_CRIT_LOW	1O	0	Clear Temperature Sensor Critical Low Status 1 = Clear MR51[3] Register
D[2]	CLR_TS_CRIT_HIGH	1O	0	Clear Temperature Sensor Critical High Status 1 = Clear MR51[2] Register
D[1]	CLR_TS_LOW	1O	0	Clear Temperature Sensor Low Status 1 = Clear MR51[1] Register
D[0]	CLR_TS_HIGH	1O	0	Clear Temperature Sensor High Status 1 = Clear MR51[0] Register

1. This entire register is self-clearing register after corresponding register is cleared.

REGISTER DESCRIPTION (continued)

REG0x14: MR20 Register: Clear Register MR52 Error Status Command (1)

BITS	BIT NAME	TYPE	DEFAULT	DESCRIPTION
D[7]	CLR_SPD_BUSY_ERROR	1O	0	Clear Write or Read Attempt while SPD Device Busy Error Status 1 = Clear MR52[7] Register
D[6]	CLR_WR_NVM_BLK_ERROR	1O	0	Clear Write Attempt to Protected NVM Block Error Status 1 = Clear MR52[6] Register
D[5]	CLR_WR_NVM_PRO_REG_ERROR	1O	0	Clear Write Attempt to NVM Protection Register Error Status 1 = Clear MR52[5] Register
D[4:3]	Reserved	RV	00	Reserved
D[1]	CLR_PEC_ERROR	1O	0	Clear Packet Error Status 1 = Clear MR52[1] Register
D[0]	CLR_PAR_ERROR	1O	0	Clear Parity Error Status 1 = Clear MR52[0] Register

1. This entire register is self-clearing register after corresponding register is cleared.

REG0x1A: MR26 Register: TS Configuration

BITS	BIT NAME	TYPE	DEFAULT	DESCRIPTION
D[7:1]	Reserved	RV	0000000	Reserved
D[0]	DIS_TS	RW	0	Disable Temperature Sensor (1) 0 = Enable thermal sensor (default) 1 = Disable thermal sensor

1. If this bit is set to '1' and then reset to '0', the Host must wait minimum of t_{INIT} before accessing samples on the thermal sensor.

REG0x1B: MR27 Register: Interrupt Configurations

BITS	BIT NAME	TYPE	DEFAULT	DESCRIPTION
D[7]	CLR_GLOBAL	1O	0	Global Clear Event Status and In Band Interrupt Status (1) (2) 1 = Clear MR48[7], MR51[3:0] and MR52[7:5, 1:0] Register
D[6:5]	Reserved	RV	00	Reserved
D[4]	IBI_ERROR_EN	RO	0	In Band Error Interrupt Enable for MR52 Error Log (3) 0 = Disable; Errors logged in MR52[7:5, 1:0] registers do not generate an IBI to Host (default) 1 = Enable; Errors logged in MR52[7:5, 1:0] registers generates an IBI to Host
D[3]	IBI_TS_CRIT_LOW_EN	RW	0	In Band Error Interrupt Enable for Temperature Sensor Critical Low 0 = Disable; MR51[3] = '1' does not generate an IBI to Host (default) 1 = Enable; MR51[3] = '1' and MR27[4] = '1' generates an IBI to Host
D[2]	IBI_TS_CRIT_HIGH_EN	RW	0	In Band Error Interrupt Enable for Temperature Sensor Critical High 0 = Disable; MR51[2] = '1' does not generate an IBI to Host (default) 1 = Enable; MR51[2] = '1' and MR27[4] = '1' generates an IBI to Host
D[1]	IBI_TS_LOW_EN	RW	0	In Band Error Interrupt Enable for Temperature Sensor Low 0 = Disable; MR51[1] = '1' does not generate an IBI to Host (default) 1 = Enable; MR51[1] = '1' and MR27[4] = '1' generates an IBI to Host
D[0]	IBI_TS_HIGH_EN	RV	0	In Band Error Interrupt Enable for Temperature Sensor High 0 = Disable; MR51[0] = '1' does not generate an IBI to Host (default) 1 = Enable; MR51[0] = '1' and MR27[4] = '1' generates an IBI to Host

1. This register is a self-clearing register after corresponding registers are cleared. Writing '0' in this register has no effect.
2. After this command is issued, the device does not generate an IBI for any pending event. But if new event occurs, the device does generate an IBI.
3. This register is automatically updated when ENEC CCC or DISEC CCC or RSTDAA CCC is registered by the TS5 device or when TS5 device goes through bus reset as described in ***Bus Reset Section***. This register can be read by the Host through normal read operation but cannot be written with normal write operation either in I²C mode or I3C Basic mode. When this register is updated, it takes effect when there is a next Start operation (i.e. after Stop operation).

REGISTER DESCRIPTION (continued)

REG0x1C: MR28 Register: TS Temperature High Limit Configuration - Low Byte (1) (2)

BITS	BIT NAME	TYPE	DEFAULT	DESCRIPTION
D[7:0]	TS_HIGH_LIMIT_LOW[7:0]	RW	0x70	MR28 and MR29 - 16-bit thermal registers define the high limit for thermal sensor. See **Table 58.Thermal Register - Low Byte and High Byte**.

1. Critical temperature high limit value must have a higher value than temperature high limit (MR28[7:0] and MR29[7:0]).
2. The Reserved bits are Read Only bits. The Host must write '0' in reserved bits when writing and device always returns '0' from reserved bits when reads this byte.

REG0x1D: MR29 Register: TS Temperature High Limit Configuration - High Byte (1) (2)

BITS	BIT NAME	TYPE	DEFAULT	DESCRIPTION
D[7:0]	TS_HIGH_LIMIT_HIGH[7:0]	RW	0x03	MR28 and MR29 - 16-bit thermal registers define the high limit for thermal sensor. See **Table 58.Thermal Register - Low Byte and High Byte**.

1. Critical temperature high limit value must have a higher value than temperature high limit (MR28[7:0] and MR29[7:0]).
2. The Reserved bits are Read Only bits. The Host must write '0' in reserved bits when writing and device always returns '0' from reserved bits when reads this byte.

REG0x1E: MR30 Register: TS Temperature Low Limit Configuration - Low Byte (1) (2)

BITS	BIT NAME	TYPE	DEFAULT	DESCRIPTION
D[7:0]	TS_LOW_LIMIT_LOW[7:0]	RW	0	MR30 and MR31 - 16-bit thermal registers define the low limit for thermal sensor. See **Table 58.Thermal Register - Low Byte and High Byte**.

1. Critical temperature low limit value must have a lower value than temperature low limit (MR30[7:0] and MR31[7:0]).
2. The Reserved bits are Read Only bits. The Host must write '0' in reserved bits when writing and device always returns '0' from reserved bits when reads this byte.

REG0x1F: MR31 Register: TS Temperature Low Limit Configuration - High Byte (1) (2)

BITS	BIT NAME	TYPE	DEFAULT	DESCRIPTION
D[7:0]	TS_LOW_LIMIT_HIGH[7:0]	RW	0	MR30 and MR31 - 16-bit thermal registers define the low limit for thermal sensor. See **Table 58.Thermal Register - Low Byte and High Byte**.

1. Critical temperature low limit value must have a lower value than temperature low limit (MR30[7:0] and MR31[7:0]).
2. The Reserved bits are Read Only bits. The Host must write '0' in reserved bits when writing and device always returns '0' from reserved bits when reads this byte.

REG0x20: MR32 Register: TS Critical Temperature High Limit Configuration - Low Byte (1) (2)

BITS	BIT NAME	TYPE	DEFAULT	DESCRIPTION
D[7:0]	TS_CRIT_HIGH_LIMIT_LOW[7:0]	RW	0x50	MR32 and MR33 - 16-bit thermal registers define the critical temperature high limit for thermal sensor. See **Table 58.Thermal Register - Low Byte and High Byte**.

1. Critical temperature high limit value must have a higher value than temperature high limit (MR28[7:0] and MR29[7:0]).
2. The Reserved bits are Read Only bits. The Host must write '0' in reserved bits when writing and device always returns '0' from reserved bits when reads this byte.

REG0x21: MR33 Register: TS Critical Temperature High Limit Configuration – High Byte (1) (2)

BITS	BIT NAME	TYPE	DEFAULT	DESCRIPTION
D[7:0]	TS_CRIT_HIGH_LIMIT_HIGH[7:0]	RW	0x05	MR32 and MR33 - 16-bit thermal registers define the critical temperature high limit for thermal sensor. See **Table 58.Thermal Register - Low Byte and High Byte**.

1. Critical temperature high limit value must have a higher value than temperature high limit (MR28[7:0] and MR29[7:0]).
2. The Reserved bits are Read Only bits. The Host must write '0' in reserved bits when writing and device always returns '0' from reserved bits when reads this byte.

REGISTER DESCRIPTION (continued)

REG0x22: MR34 Register: TS Critical Temperature Low Limit Configuration – Low Byte (1) (2)

BITS	BIT NAME	TYPE	DEFAULT	DESCRIPTION
D[7:0]	TS_CRIT_LOW_LIMIT_LOW[7:0]	RW	0	MR34 and MR35 – 16-bit thermal registers define the critical temperature low limit for thermal sensor. See **Table 58.Thermal Register - Low Byte and High Byte**.

1. Critical temperature low limit value must have a lower value than temperature low limit (MR30[7:0] and MR31[7:0]).
2. The Reserved bits are Read Only bits. The Host must write '0' in reserved bits when writing and device always returns '0' from reserved bits when reads this byte.

REG0x23: MR35 Register: TS Critical Temperature Low Limit Configuration – High Byte (1) (2)

BITS	BIT NAME	TYPE	DEFAULT	DESCRIPTION
D[7:0]	TS_CRIT_LOW_LIMIT_HIGH[7:0]	RW	0	MR34 and MR35 – 16-bit thermal registers define the critical temperature low limit for thermal sensor. See **Table 58.Thermal Register - Low Byte and High Byte**.

1. Critical temperature high limit value must have a higher value than temperature high limit (MR30[7:0] and MR31[7:0]).
2. The Reserved bits are Read Only bits. The Host must write '0' in reserved bits when writing and device always returns '0' from reserved bits when reads this byte.

REG0x30: MR48 Register: Device Status

BITS	BIT NAME	TYPE	DEFAULT	DESCRIPTION
D[7]	IBI_STATUS	RO	0	Device Event In Band Interrupt Status 0 = No pending IBI (default) 1 = Pending IBI
D[6:0]	Reserved	RV	0000000	Reserved

REG0x31: MR49 Register: TS Current Sensed Temperature - Low Byte (1)

BITS	BIT NAME	TYPE	DEFAULT	DESCRIPTION
D[7:0]	TS_SENSE_LOW[7:0]	RO	0	MR49 and MR50 – 16-bit thermal registers return the most recent conversion of the thermal sensor. See **Table 58.Thermal Register - Low Byte and High Byte**.

1. The device always returns '0' from reserved bits.

REG0x32: MR50 Register: TS Current Sensed Temperature - High Byte (1)

BITS	BIT NAME	TYPE	DEFAULT	DESCRIPTION
D[7:0]	TS_SENSE_HIGH[7:0]	RO	0	MR49 and MR50 – 16-bit thermal registers return the most recent conversion of the thermal sensor. See **Table 58.Thermal Register - Low Byte and High Byte.**

1. The device always returns '0' from reserved bits.

REG0x33: MR51 Register: TS Temperature Status

BITS	BIT NAME	TYPE	DEFAULT	DESCRIPTION
D[7:4]	Reserved	RV	0000	Reserved
D[3]	TS_CRIT_LOW_STATUS	RO	0	Temperature Sensor Critical Low 0 = Temperature is above the limit set in MR34 and MR35 (default) 1 = Temperature is below the limit set in MR34 and MR35
D[2]	TS_CRIT_HIGH_STATUS	RO	0	Temperature Sensor Critical High 0 = Temperature is below the limit set in MR32 and MR33 (default) 1 = Temperature is above the limit set in MR32 and MR33
D[1]	TS_LOW_STATUS	RO	0	Temperature Sensor Low 0 = Temperature above limit set in registers MR30 and MR31 (default) 1 = Temperature below limit set in registers MR30 and MR31
D[0]	TS_HIGH_STATUS	RO	0	Temperature Sensor High 0 = Temperature is below the limit set in registers MR28 and MR29 (default) 1 = Temperature is above the limit set in registers MR28 and MR29

REGISTER DESCRIPTION (continued)

REG0x34: MR52 Register: Misc. Error Status

BITS	BIT NAME	TYPE	DEFAULT	DESCRIPTION
D[7:2]	Reserved	RO	000000	Reserved
D[1]	PEC_ERROR_STATUS	RO	0	Packet Error (1) (2) 0 = No PEC Error (default) 1 = PEC Error in one or more packets
D[0]	PAR_ERROR_STATUS	RO	0	Parity Check Error (2) (3) 0 = No Parity Error (default) 1 = Parity Error in one or more bytes

1. Only applicable MR18[5] = '1' and if PEC function is enabled.
2. This register is updated when TS5 device goes through bus reset as described in ***Bus Reset Section***.
3. Only applicable in MR18[5] = '1' and if Parity function is not disabled or for supported CCC in I²C mode.

REG0x50: MR80 Register: Serial Number Byte 0

BITS	BIT NAME	TYPE	DEFAULT	DESCRIPTION
D[7:0]	SERIAL_NUMBER_BYTE0[7:0] (1)	ROE	-	Byte 0 of the unique 40-bit serial number stored in MR80 to MR84. The serial number is vendor specific.

1. Only applicable if MR0[7:0] programmed value is 0x52.

REG0x51: MR81 Register: Serial Number Byte 1

BITS	BIT NAME	TYPE	DEFAULT	DESCRIPTION
D[7:0]	SERIAL_NUMBER_BYTE1[7:0] (1)	ROE	-	Byte 1 of the unique 40-bit serial number stored in MR80 to MR84. The serial number is vendor specific.

1. Only applicable if MR0[7:0] programmed value is 0x52.

REG0x52: MR82 Register: Serial Number Byte 2

BITS	BIT NAME	TYPE	DEFAULT	DESCRIPTION
D[7:0]	SERIAL_NUMBER_BYTE2[7:0] (1)	ROE	-	Byte 2 of the unique 40-bit serial number stored in MR80 to MR84. The serial number is vendor specific.

1. Only applicable if MR0[7:0] programmed value is 0x52.

REG0x53: MR83 Register: Serial Number Byte 3

BITS	BIT NAME	TYPE	DEFAULT	DESCRIPTION
D[7:0]	SERIAL_NUMBER_BYTE3[7:0] (1)	ROE	-	Byte 3 of the unique 40-bit serial number stored in MR80 to MR84. The serial number is vendor specific.

1. Only applicable if MR0[7:0] programmed value is 0x52.

REG0x54: MR84 Register: Serial Number Byte 4

BITS	BIT NAME	TYPE	DEFAULT	DESCRIPTION
D[7:0]	SERIAL_NUMBER_BYTE4[7:0] (1)	ROE	-	Byte 4 of the unique 40-bit serial number stored in MR80 to MR84. The serial number is vendor specific.

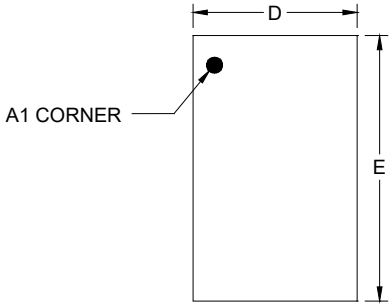
1. Only applicable if MR0[7:0] programmed value is 0x52.

REVISION HISTORY

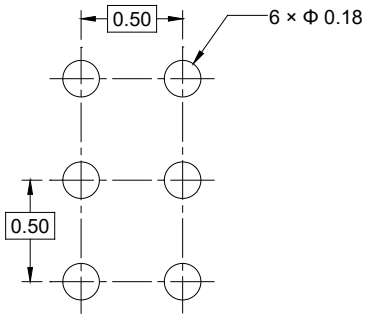
REVISION	DATE	COMMENTS
REV.A	Jan. 2023	Initial version release
REV.A.1	Oct. 2023	Added: — TDT521x Specification per JEDEC JESD302-1A — *REG0x50: MR80 Register: Serial Number Byte 0* to *REG0x51: MR81 Register: Serial Number Byte 1* Serial Number Byte 0 to Byte 5 Updated: — *Key Parameters* — MR80 to MR84 Register Description in *Table 57* — *Ordering Information*, *Top Markings*
REV.A.2	May. 2024	Removed: — Grade B device TDT5110/TDT5210 Ordering Information Updated: — *Top Markings* — *WLCSP Package Information*
REV.A.3	Oct. 2024	Removed: — TDT5211 Model Updated: — Table 1. AC Measurement Conditions — DC Characteristics and AC Characteristics — Table 56. Register Attribute Modifier — Package Outline Dimensions Added: — Tape and Reel Information

PACKAGE OUTLINE DIMENSIONS

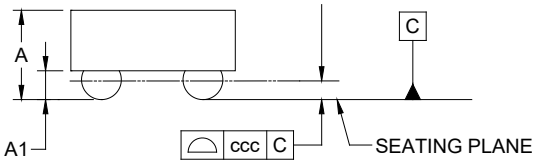
WLCSP-0.81×1.31-6B



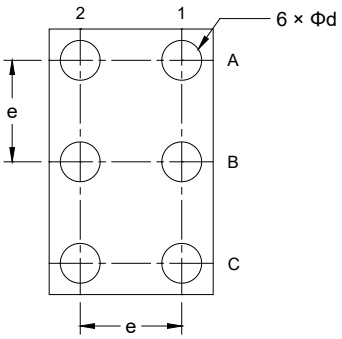
TOP VIEW



RECOMMENDED LAND PATTERN (Unit: mm)



SIDE VIEW



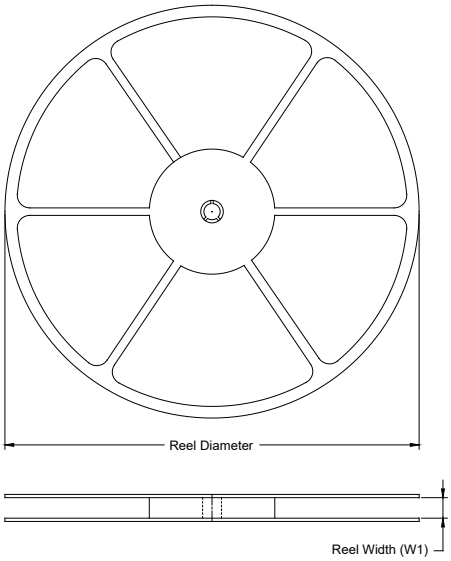
BOTTOM VIEW

Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	0.409	-	0.472
A1	0.122	-	0.162
D	0.778	-	0.838
E	1.278	-	1.338
d	0.166	-	0.226
e	0.500 BSC		
ccc	0.050		

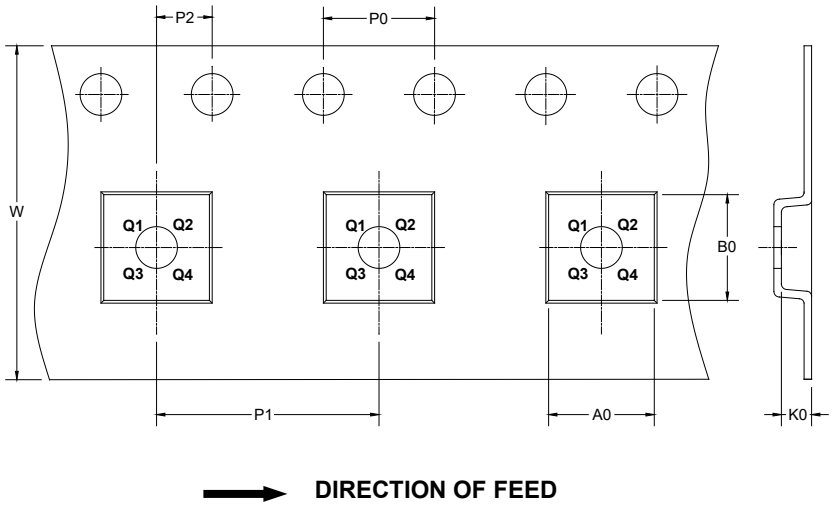
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



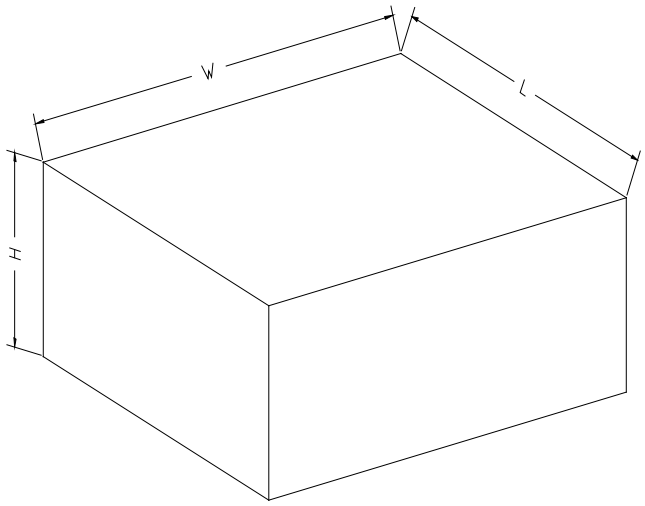
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
WLCSP-0.81×1.31-6B	7"	9.5	0.90	1.41	0.56	4.0	2.0	2.0	8.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18

DD0002