SGM3802
Positive/Negative Dual-Output 300mA Power Supply for TFT LCD Bias

GENERAL DESCRIPTION

The SGM3802 is designed for powering devices which require both positive and negative bias voltages, such as LCDs, AFEs, etc. The device integrates a Boost converter VO1 for VPO and an inverting Buck-Boost converter VO2 for VNO. Output voltages of both converters can be programmed in digital steps through the I^2C interface control pins.

The SGM3802 is available in Green WLCSP-1.25×1.75-12B and TQFN-2.5×3-14L packages. It operates over an ambient temperature range of -40℃ to +85℃.

APPLICATIONS

LCD Bias
Wearable Device Display/Audio
AFE with Positive & Negative Rails

FEATURES

- **Outputs Programmable with I^2C Interface**
- **4.6V to 6.4V Programmable Range with 100mV Step for Positive Output**
- **-4.6V to -6.4V Programmable Range with 100mV Step for Negative Output**
- **300mA Output Current for V_{PO} and V_{NO}**
- **Excellent Performance**
  - **Outstanding Transient Response**
- **1.45MHz Switching Frequency for Positive Rail**
- **1.25MHz Switching Frequency for Negative Rail**
- **Power Save Mode**
- **Configurable Active Discharge**
- **Internal Soft-Start to limit Inrush Current**
- **Over-Temperature Protection (OTP)**
- **Over-Current Protection (OCP)**
- **Short-Circuit Protection (SCP)**

TYPICAL APPLICATION

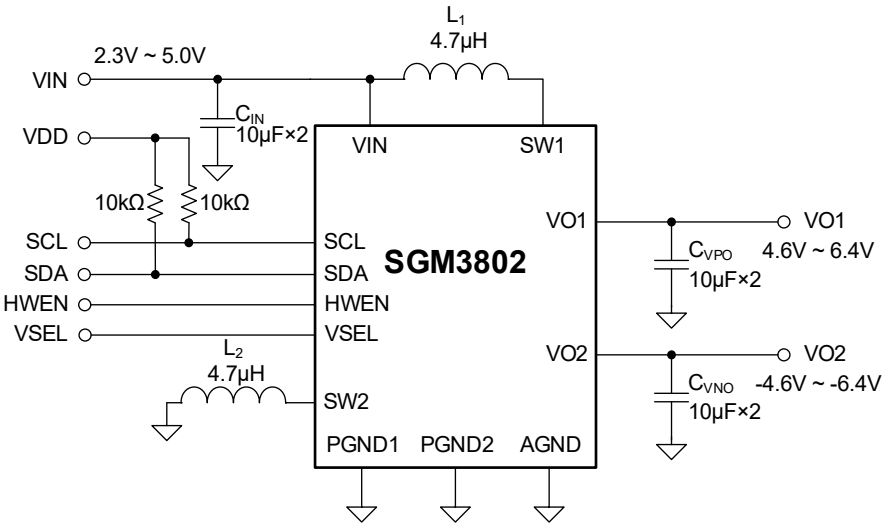


Figure 1. Typical Application Circuit

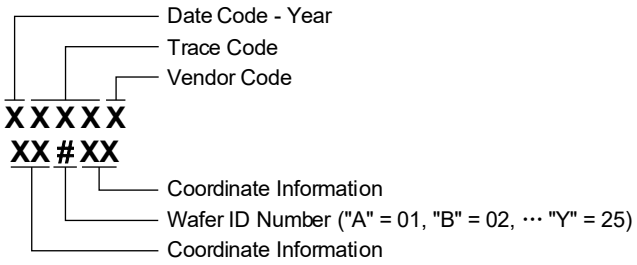
PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM3802	WLCSP-1.25×1.75-12B	-40℃ to +85℃	SGM3802YG/TR	3802 XXXXX XX#XX	Tape and Reel, 5000
	TQFN-2.5×3-14L	-40℃ to +85℃	SGM3802YTWB14G/TR	2KNTWB XXXXX	Tape and Reel, 10000

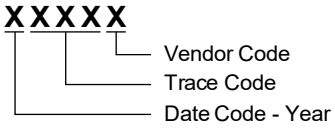
MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code. XX#XX = Coordinate Information and Wafer ID Number.

WLCSP-1.25×1.75-12B



TQFN-2.5×3-14L



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

VIN Voltage ..... -0.3V to 6V
VO1 Voltage ..... -0.3V to 7.5V
SW1 Voltage ..... -0.3V to 7.5V
SW1 Voltage (Transient: 10ns) ..... -1V to 9V
VO2 Voltage ..... -7.5V to 0.3V
SW2 Voltage ..... -7.5V to 6V
SW2 Voltage (Transient: 10ns) ..... -9V to 8V
SDA, SCL, HWEN, VSEL ..... -0.3V to 6V
PGND1, PGND2 to AGND ..... -0.3V to 0.3V
Package Thermal Resistance
WLCSP-1.25×1.75-12B, θ_{JA} ..... 101.5℃/W
WLCSP-1.25×1.75-12B, θ_{JB} ..... 35.7℃/W
WLCSP-1.25×1.75-12B, θ_{JC} ..... 29℃/W
TQFN-2.5×3-14L, θ_{JA} ..... 58.4℃/W
TQFN-2.5×3-14L, θ_{JB} ..... 25.7℃/W
TQFN-2.5×3-14L, $\theta_{JC\ (TOP)}$ ..... 56.4℃/W
TQFN-2.5×3-14L, $\theta_{JC\ (BOT)}$ ..... 16.4℃/W
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility (1) (2)
HBM ..... ±2000V
CDM ..... ±1000V

NOTES:

1. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.

2. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

RECOMMENDED OPERATING CONDITIONS

Supply Voltage Range ..... 2.3V to 5V
Operating Ambient Temperature Range ..... -40℃ to +85℃
Operating Junction Temperature Range ..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

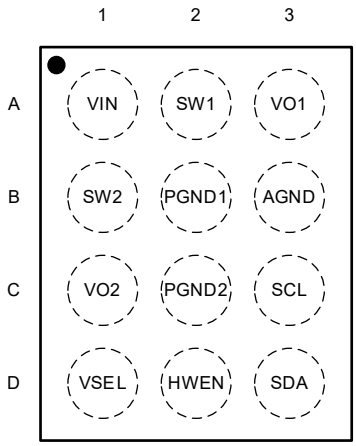
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

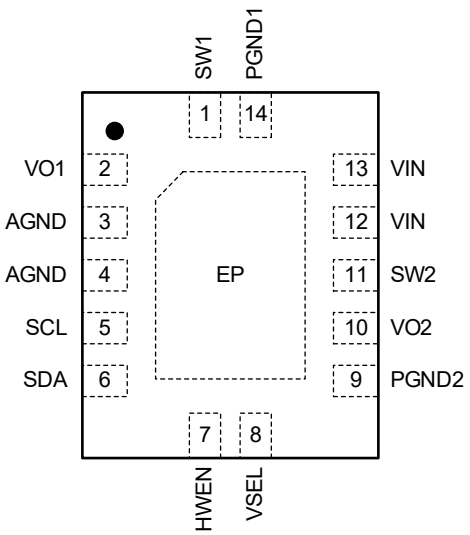
PIN CONFIGURATIONS

(TOP VIEW)



WLCSP-1.25×1.75-12B

(TOP VIEW)



TQFN-2.5×3-14L

PIN DESCRIPTION

PIN		NAME	I/O	FUNCTION
WLCSP-1.25×1.75-12B	TQFN-2.5×3-14L			
A1	12, 13	VIN	I	Supply Input.
A2	1	SW1	O	VO1 Boost Converter Switching Node.
A3	2	VO1	O	VO1 Boost Converter Output Pin.
B1	11	SW2	O	VO2 Inverting Buck-Boost Converter Switching Node.
B2	14	PGND1	G	VO1 Boost Converter Power Ground.
B3	3, 4	AGND	G	Analog Ground.
C1	10	VO2	O	VO2 Inverting Buck-Boost Converter Output Pin.
C2	9	PGND2	G	VO2 Inverting Buck-Boost Converter Power Ground.
C3	5	SCL	I	I^2C Interface Clock Signal.
D1	8	VSEL	I	Default Output Voltage Select Pin. High = ±6.0V; Low = ±5.4V; Floating = ±5.0V
D2	7	HWEN	I	Device Enable Pin.
D3	6	SDA	I/O	I^2C Interface Data Bus.
–	Exposed Pad	EP	–	Exposed Pad. It should be connected to the PCB ground plane (GND).

NOTE: I = input, O = output, I/O = input or output, G = ground.

ELECTRICAL CHARACTERISTICS

(At T_J = +25℃, V_{IN} = 3.8V, VPO_VNO_EN[1:0] = 11, V_{VO1} = 5V, V_{VO2} = -5V, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Current and Thermal Protection							
Input Voltage Range	V_{IN}	T_J = -40℃ to +85℃		2.3		5	V
Shutdown Current into VIN	I_{SD}	V_{IN} = 3.8V, all channels off, T_J = -40℃ to +85℃			0.7	1.5	μA
Quiescent Current into Input Supply	I_{QON}	V_{IN} = 3.8V, no load, VPO_VNO_EN[1:0] = 11			2.7		mA
Under-Voltage Lockout Threshold	V_{IT+}	V_{IN} rising, T_J = -40℃ to +85℃		2.05	2.15	2.25	V
	V_{IT-}	V_{IN} falling, T_J = -40℃ to +85℃		1.9	2	2.1	V
Thermal Shutdown Temperature	T_{SD}	Junction temperature rising			145		℃
		Junction temperature falling			135		℃
Logic Signals (SDA, SCL, HWEN, VSEL)							
SCL Clock Frequency	f_{SCL}	T_J = -40℃ to +85℃		100	400	1000	kHz
Logic Input High Level Voltage	V_{IH}	T_J = -40℃ to +85℃		0.8			V
Logic Input Low Level Voltage	V_{IL}	T_J = -40℃ to +85℃				0.4	V
Logic Input High Level Voltage (VSEL) (1)	V_{IH_VSEL}	T_J = -40℃ to +85℃		1			V
Logic Input Low Level Voltage (VSEL) (1)	V_{IL_VSEL}	T_J = -40℃ to +85℃				0.4	V
Boost Converter (V_{VO1})							
Positive Output Voltage	V_{VO1}	4.6V to 6.4V with 0.1V/step, default 5.0V, T_J = -40℃ to +85℃		4.6	5.0	6.4	V
Positive Output Voltage Accuracy (2)		V_{VO1} = 4.6V to 6.4V, no load		-0.6		0.6	%
		V_{VO1} = 4.6V to 6.4V, no load, T_J = -40℃ to +85℃		-0.8		0.8	%
SW1 MOSFET On-Resistance	$R_{DS(ON)11}$	I_{DS} = 100mA	WLCSP-1.25×1.75-12B		100		mΩ
			TQFN-2.5×3-14L		150		
SW1 MOSFET Rectifier On-Resistance	$R_{DS(ON)12}$	I_{DS} = 100mA	WLCSP-1.25×1.75-12B		320		mΩ
			TQFN-2.5×3-14L		360		
SW1 Switch Current Limit	I_{SW1}	Inductor valley current		1.1	1.35	1.6	A
SW1 Switching Frequency	f_{SW1}	I_{VO1} = 100mA, T_J = -40℃ to +85℃		1.25	1.45	1.65	MHz
Output Current Capability	I_{OUT1}	V_{IN} = 2.3V to 5V, V_{VO1} = 5V		400			mA
		V_{IN} = 2.3V to 5V, V_{VO1} = 6.4V		300			mA
Short-Circuit Threshold in Operation	$V_{VO1(SCP)}$	Percentage of nominal V_{VO1}			80		%
VO1 Discharge Resistance	$R_{VO1(DCG)}$	DISP = 1, I_{VO1} = 20mA			30		Ω
VO1 Discharge Time	t_{DVO1}	DISP = 1, V_{VO1} from 90% to 10%			0.8		ms
Line Transient Ripple	$VO1_{LINETRA}$	ΔV_{IN} = 0.5V, t_R = t_F = 10μs, I_{VO1} = 200mA			45		mV_{PP}
Line Regulation	$VO1_{LINEREG}$	I_{VO1} = 100mA, V_{IN} = 2.3V to 5V			±0.013		%/V
		No load, V_{IN} = 2.3V to 5V			±0.015		%/V
Output Voltage Ripple	$VO1_{RIPPLE}$	I_{VO1} = I_{VO2} = 0 to 100mA			7		mV_{PP}
Load Transient Ripple	$VO1_{LOADTRA}$	I_{VO1} = 200mA to 250mA, t_R = t_F = 10μs			48		mV_{PP}
Load Regulation	$VO1_{LOADREG}$	I_{VO1} = 1mA to 300mA	WLCSP-1.25×1.75-12B		±0.12		%/A
			TQFN-2.5×3-14L		±0.37		

ELECTRICAL CHARACTERISTICS (continued)

(At T_J = +25℃, V_{IN} = 3.8V, VPO_VNO_EN[1:0] = 11, V_{VO1} = 5V, V_{VO2} = -5V, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Buck-Boost Converter (VO2)							
Negative Output Voltage Range	V_{VO2}	-6.4V to -4.6V with 0.1V/step, default -5V, T_J = -40℃ to +85℃		-6.4	-5	-4.6	V
Negative Output Voltage Accuracy (2)		V_{VO2} = -5V, no load, T_J = -40℃ to +85℃		-0.6		0.6	%
SW2 MOSFET On-Resistance	$R_{DS(ON)21}$	I_{DS} = 100mA	WLCSP-1.25×1.75-12B		155		mΩ
			TQFN-2.5×3-14L		185		
SW2 MOSFET Rectifier On-Resistance	$R_{DS(ON)22}$	I_{DS} = 100mA	WLCSP-1.25×1.75-12B		300		mΩ
			TQFN-2.5×3-14L		315		
SW2 Switching Frequency	f_{SW2}	I_{VO2} = 100mA, T_J = -40℃ to +85℃		1.1	1.25	1.4	MHz
Output Current Capability	I_{OUT2}	V_{IN} = 2.3V to 5V, V_{VO2} = -5V		200			mA
		V_{IN} = 2.9V to 5V, V_{VO2} = -6.4V		300			mA
SW2 Switch Current Limit	I_{SW2}	Inductor peak current		1.35	1.70	2.05	A
Short-Circuit Threshold in Operation	$V_{VO2(SCP)}$	Percentage of nominal V_{VO2}			80		%
VO2 Discharge Resistance	$R_{VO2(DCG)}$	DISN = 1, I_{VO2} = 20mA			30		Ω
VO2 Discharge Time	t_{DVO2}	DISN = 1, V_{VO2} from 90% to 10%			0.8		ms
VO2 Leakage, No Discharge	I_{LEAK_VO2}	DISN = 0, T_J = -40℃ to +85℃			0.8	1.65	μA
Line Transient Ripple	$VO2_{LINETRA}$	ΔV_{IN} = 0.5V, t_R = t_F = 10μs, I_{VO2} = 200mA			55		mV_{PP}
Line Regulation	$VO2_{LINEREG}$	I_{VO2} = 100mA, V_{IN} = 2.3V to 5V	WLCSP-1.25×1.75-12B		±0.0032		%/V
			TQFN-2.5×3-14L		±0.011		
		No load, V_{IN} = 2.3V to 5V	WLCSP-1.25×1.75-12B		±0.0025		%/V
			TQFN-2.5×3-14L		±0.014		
Output Voltage Ripple	$VO2_{RIPPLE}$	I_{VO1} = I_{VO2} = 0 to 100mA			10		mV_{PP}
Load Transient Ripple	$VO2_{LOADTRA}$	I_{VO2} = 200mA to 250mA, t_R = t_F = 10μs			77		mV_{PP}
Load Regulation	$VO2_{LOADREG}$	I_{VO2} = 1mA to 300mA	WLCSP-1.25×1.75-12B		±0.074		%/A
			TQFN-2.5×3-14L		±0.36		

NOTES:
1. Guaranteed by design.
2. The output voltage accuracy parameters are initial accuracy values.

TIMING REQUIREMENTS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Short-Circuit Timer					
VO1 Short-Circuit Detection Time in Start-Up, T_J = -40℃ to +85℃	$t_{VO1(SCP)}$	3.5	4.2	5.0	ms
VO1 Short-Circuit Detection Time in Operation, T_J = -40℃ to +85℃		1.2	1.4	1.6	
VO2 Short-Circuit Detection Time in Start-Up, T_J = -40℃ to +85℃	$t_{VO2(SCP)}$	3.5	4.2	5.0	
VO2 Short-Circuit Detection Time in Operation, T_J = -40℃ to +85℃		1.2	1.4	1.6	
Power Sequence					
I^2C Interface Active Time after Enable	t_{D_I2C}			0.1	ms
VO1 Start-Up Time	t_{SS1}		2		
VO2 Start-Up Time	t_{SS2}		1		
Start-Up/Power-Down Time Delay	t_{DELAY}	-10	0	10	

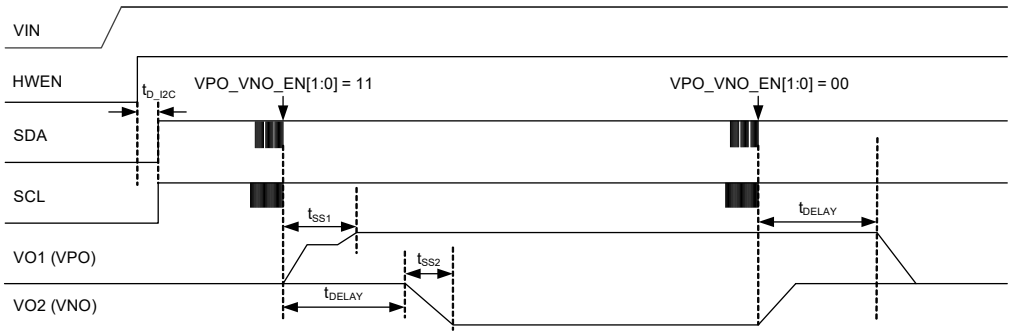
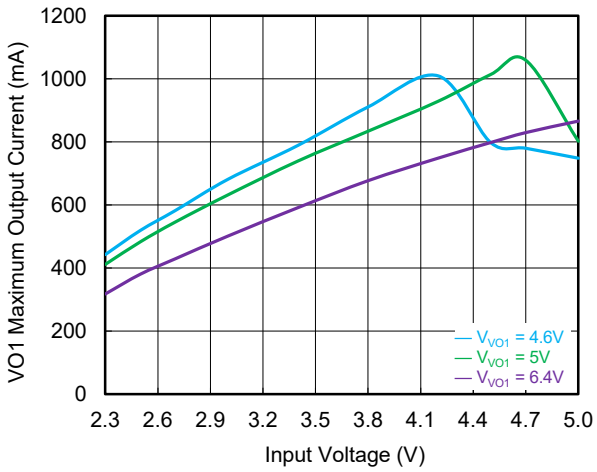


Figure 2. Timing Diagram

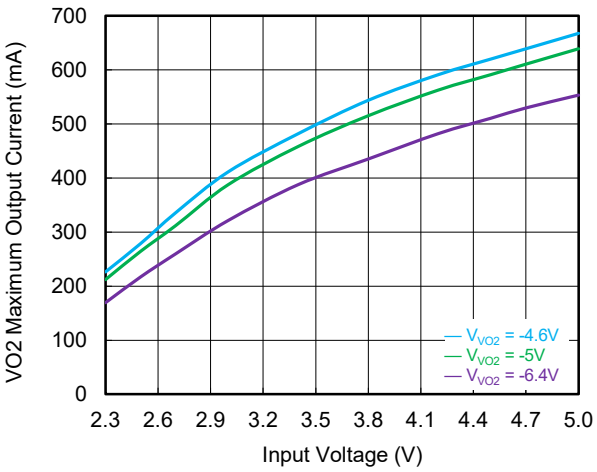
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 3.8V, V_{VO1} = 5V, V_{VO2} = -5V, unless otherwise noted.

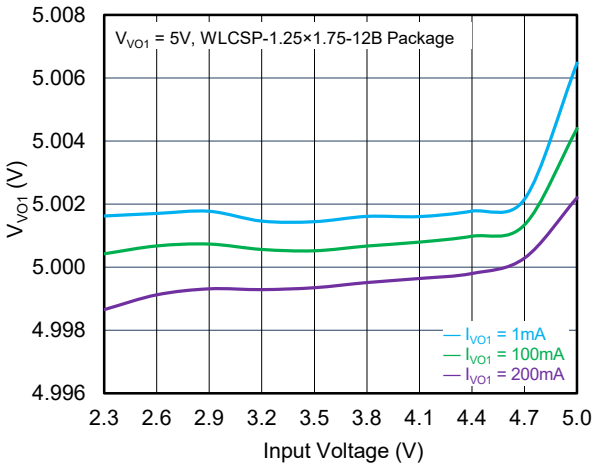
VO1 Maximum Output Current vs. Input Voltage



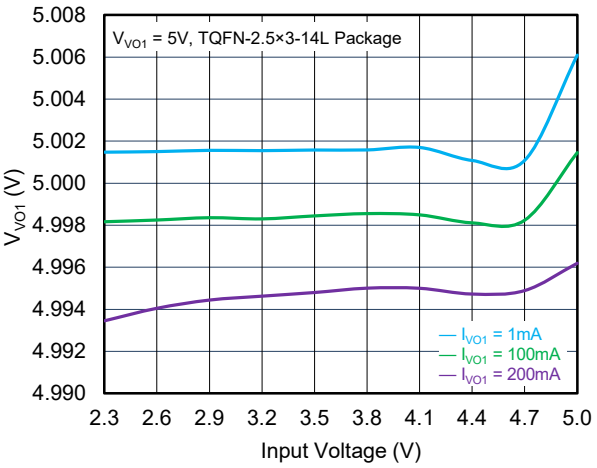
VO2 Maximum Output Current vs. Input Voltage



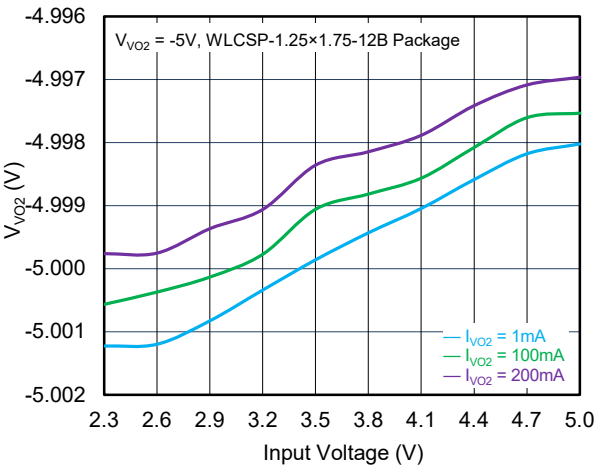
VO1 Line Regulation



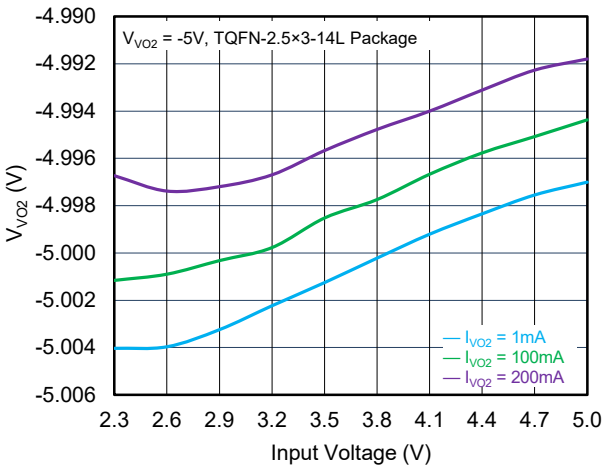
VO1 Line Regulation



VO2 Line Regulation



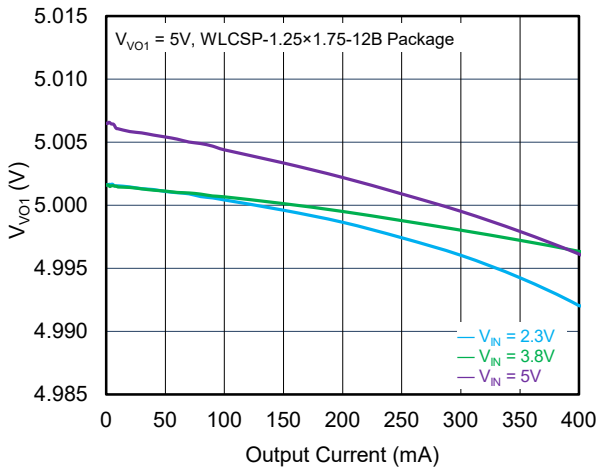
VO2 Line Regulation



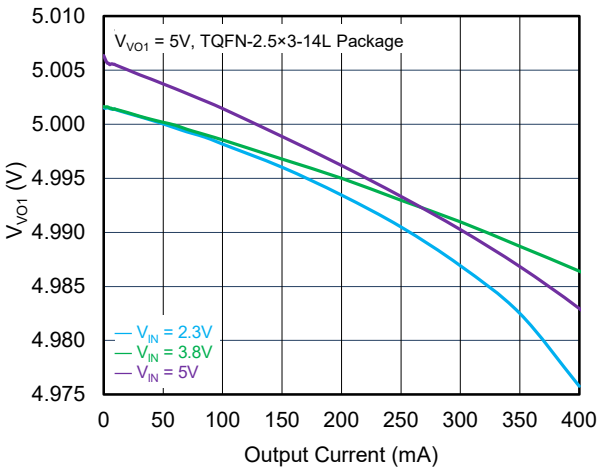
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

V_{IN} = 3.8V, V_{VO1} = 5V, V_{VO2} = -5V, unless otherwise noted.

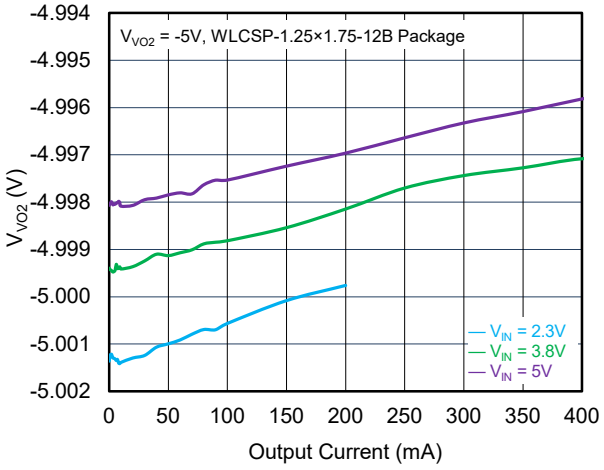
VO1 Load Regulation



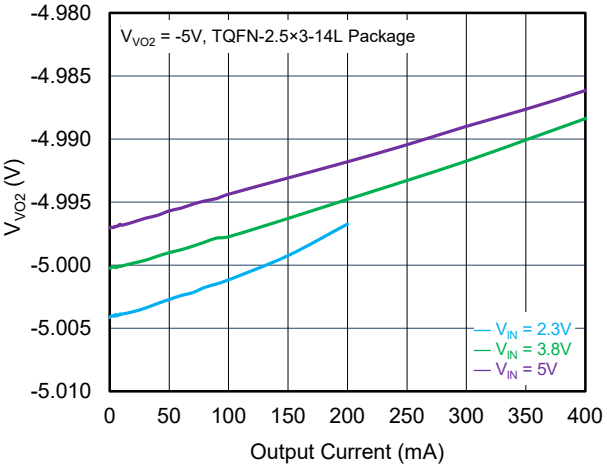
VO1 Load Regulation



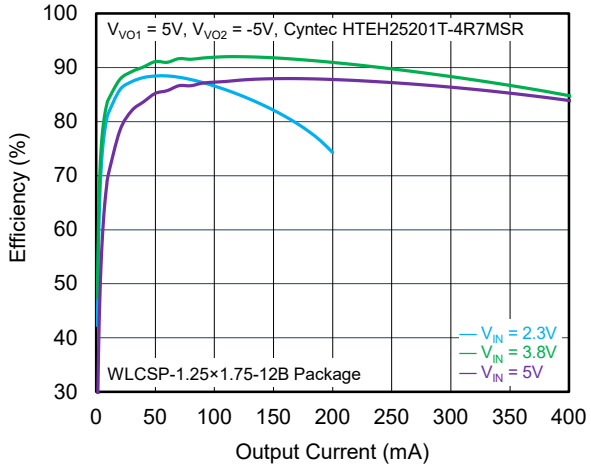
VO2 Load Regulation



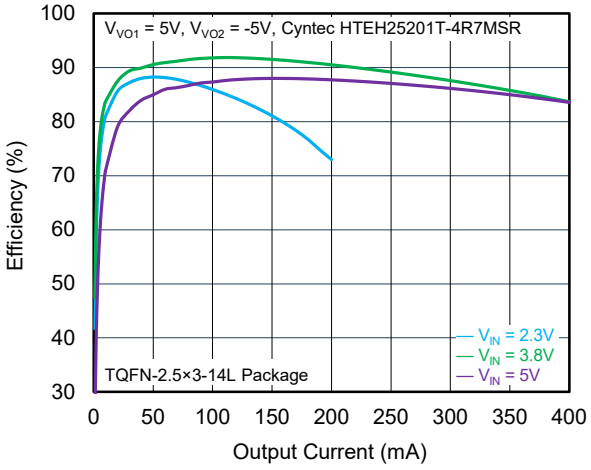
VO2 Load Regulation



VO1 and VO2 Combined Efficiency vs. Output Current



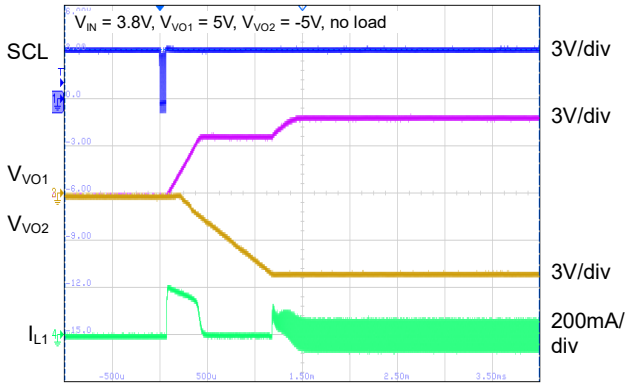
VO1 and VO2 Combined Efficiency vs. Output Current



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

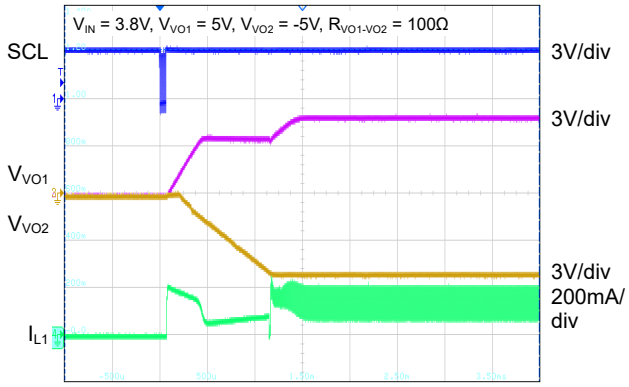
V_{IN} = 3.8V, V_{VO1} = 5V, V_{VO2} = -5V, unless otherwise noted.

Start-Up Sequence



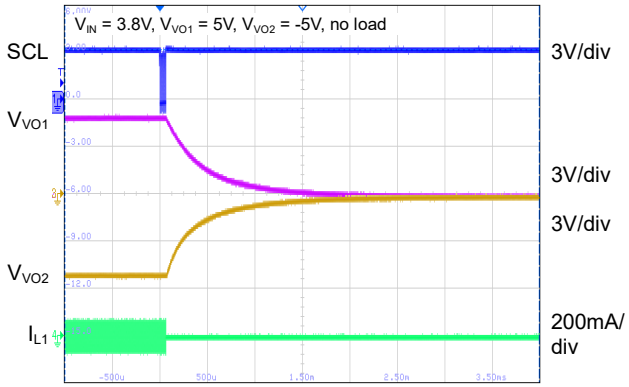
Time (500μs/div)

Start-Up Sequence



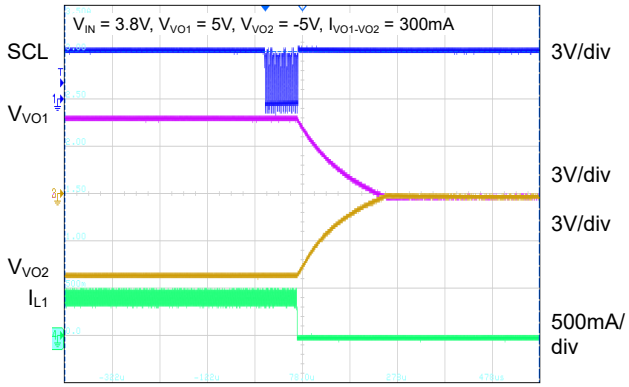
Time (500μs/div)

Power-Down Sequence



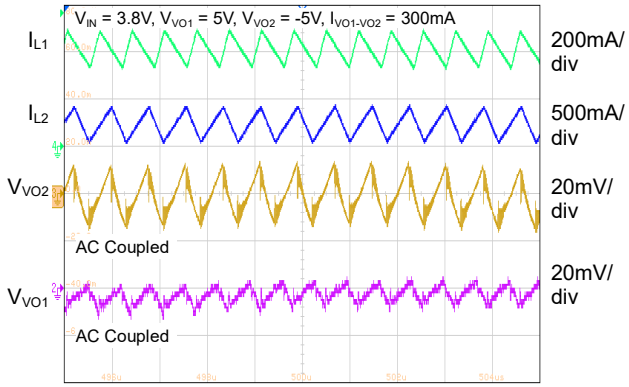
Time (500μs/div)

Power-Down Sequence



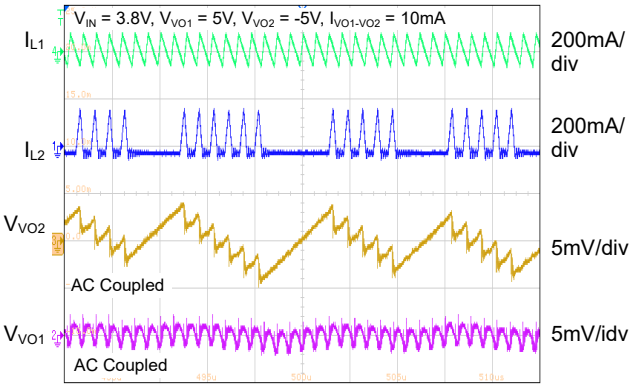
Time (100μs/div)

Output Voltage Ripple at 300mA Load



Time (1μs/div)

Output Voltage Ripple at 10mA Load

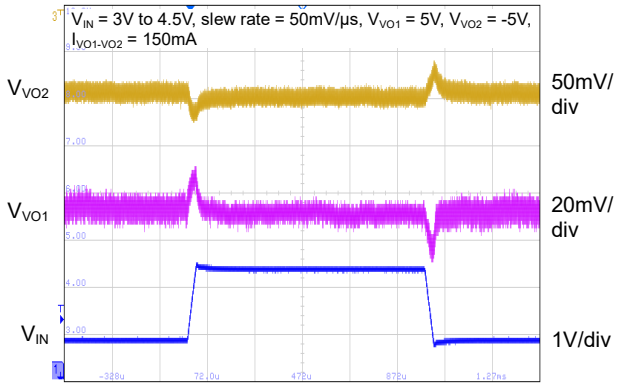


Time (2.5μs/div)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

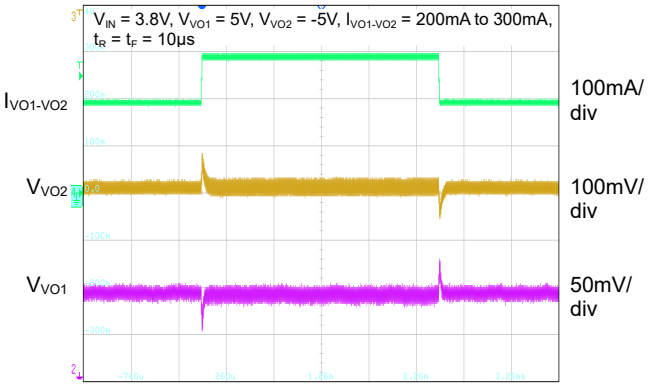
V_{IN} = 3.8V, V_{VO1} = 5V, V_{VO2} = -5V, unless otherwise noted.

Line Transient



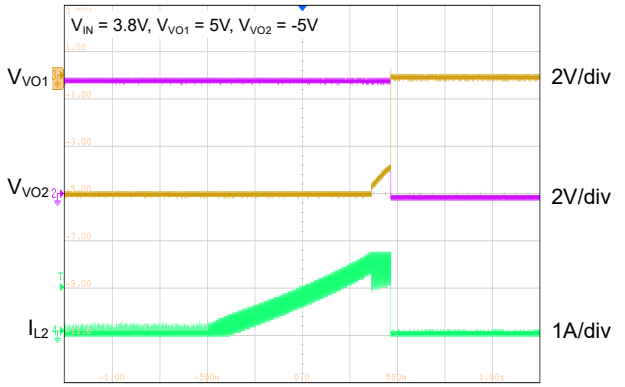
Time (200μs/div)

Load Transient



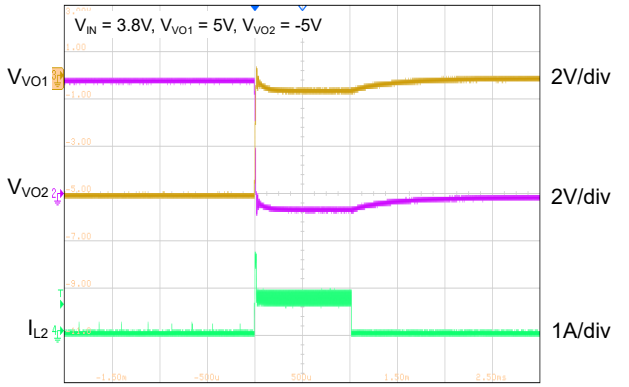
Time (500μs/div)

Sweep $I_{VO1-VO2}$ to Trigger OCP and SCP



Time (250ms/div)

Short VO1 and VO2 to Trigger SCP



Time (500μs/div)

FUNCTIONAL BLOCK DIAGRAM

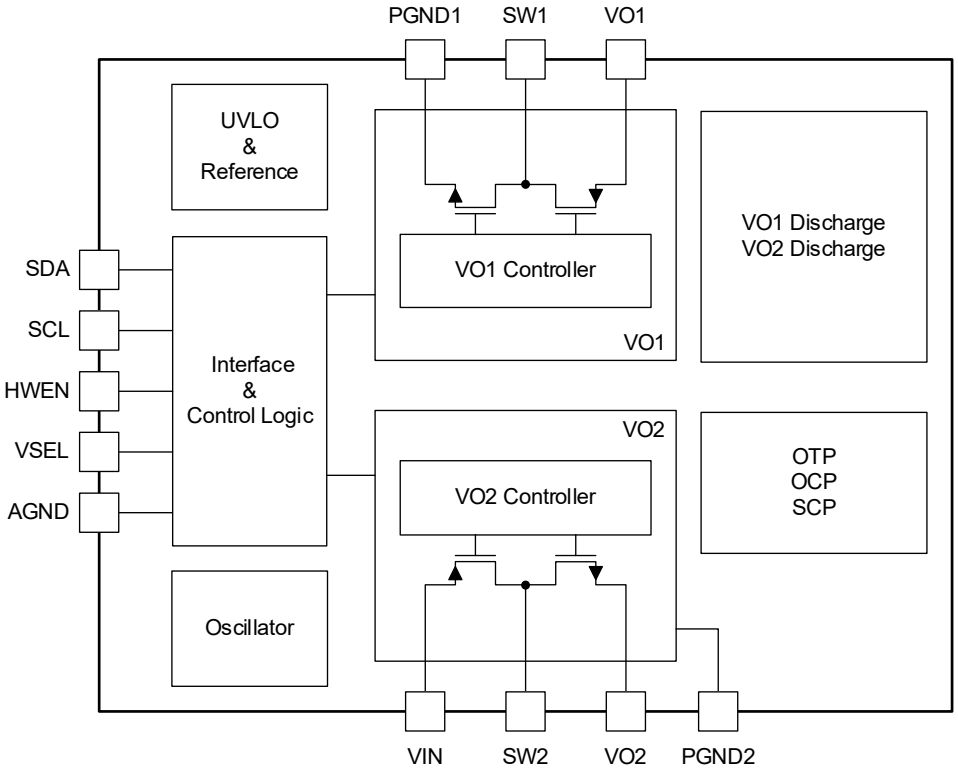


Figure 3. SGM3802 Functional Block Diagram

RECOMMENDED COMPONENTS OF TEST CIRCUITS

Reference	Quantity	Description	Part Number	Package	Supplier
L_1, L_2	2	4.7μH/100mΩ/1.9A	HTEH25201T-4R7MSR	2.5mm × 2.0mm × 1.0mm	Cyntec
C_{IN}	2	10μF/16V/X5R	GRM188R61C106MA73	0603	Murata
C_{VPO} (1)	2	10μF/16V/X5R	GRM188R61C106MA73	0603	Murata
C_{VNO} (1)	2	10μF/16V/X5R	GRM188R61C106MA73	0603	Murata

NOTE:

1. The output capacitors of each output must be less than 50μF.

DETAILED DESCRIPTION

The SGM3802 is designed for powering devices which require both positive and negative bias voltages. The device integrates a Boost converter VO1 for VPO and an inverting Buck-Boost converter VO2 for VNO. Output voltages of both converters can be programmed in digital steps through the I^2C interface control pins.

Under-Voltage Lockout (UVLO)

The built-in under-voltage lockout function (UVLO) monitors the input voltage and disables the device when the input voltage is too low to operate.

Thermal Shutdown (TSD)

The device has a function of thermal shutdown, which prevents the device from damage due to overheating and excessive power dissipation. The device stops switching and shuts down the outputs once the junction temperature exceeds +145℃ (TYP), and restarts with the same programmed voltages and sequences when the temperature decreases to +135℃ (TYP).

Start-Up Sequence

VPO and VNO can be enabled separately with no delay or be enabled simultaneously with delay timer t_{DELAY} through the P2N_SEQ and VPO_VNO_EN[1:0] bits.

Active Discharge

An active discharge for 0.8ms of the positive rail and the negative rail is preset, and the discharge function of both rails can be disabled respectively by programming the DISP and DISN bits.

Boost Converter VO1 (VPO)

The Boost converter VO1 operates with a valley-current-mode topology and fixed 1.45MHz (TYP) frequency. The VO1 output voltage can be programmed between 4.6V and 6.4V with 100mV steps (see VPO_SET register).

The output of VO1 is fully isolated in shutdown mode.

Inverting Buck-Boost Converter VO2 (VNO)

The inverting Buck-Boost converter VO2 operates with a peak-current-mode topology and fixed 1.25MHz (TYP) frequency. The VO2 output voltage can be programmed between -6.4V and -4.6V with 100mV steps (see VNO_SET register).

The output of VO2 is fully isolated in shutdown mode.

EMI and Acoustic Interference

Switching noise propagating along wire connections commonly dominates the EMI from the device operation, which may degrade receiver sensitivities by injecting interference into its carrier band or interim band through inter-modulation in its down converters. Inserting a ferrite bead into input power path and making short and straightforward path always work well in practice.

The device limits its lowest pulse skip frequency to be higher than audible frequency range for acoustic interference free operation.

DETAILED DESCRIPTION (continued)

Soft-Start, Discharge, Start-Up and Timing Shutdown

The built-in soft-start function is adopted to limit the inrush current.

Writing 11 to VPO_VNO_EN[1:0] bits enables the VO1 Boost converter and VO2 inverting Buck-Boost converter with a sequence which is determined by P2N_SEQ and TDELAY[1:0] bits. Also the VO1 and VO2 can be enabled or disabled separately as shown in the VPO_VNO_EN[1:0] bits.

VO1 starts with a pre-charge function and a 0.35A soft-start current limit until it rises to the programmed voltage. Then the full current limit is active (1.35A, TYP).

t_{DELAY} after/before VO1 is enabled, the VO2 converter starts switching with a 0.7A current limit until the VO2 rises to the programmed voltage. Then the full current limit is active (1.7A, TYP).

The output discharge function can be controlled by the fast discharge control bits (DISP & DISN).

Short-Circuit and Overload Protection

The built-in Short-Circuit protection (SCP) prevents the device from damage. If either of the two outputs (VO1 and VO2) is shorted to the ground or VO1 and VO2 are shorted together, the SGM3802 will trigger the function. When a short or an overload occurs at VO1 or VO2, both the two converters stop switching, the outputs are shut down and latched.

A SCP or overload occurs if any of the following events happens:

- VO1 is not in regulation 4.2ms after VO1 is enabled then VO1 (and VO2) converter/s shut down.
- VO2 is not in regulation 4.2ms after t_{DELAY} then VO2 (and VO1) converter/s shut down.
- VO1 falls below 80% of the programmed output voltage longer than 1.4ms then all converters shut down.
- VO2 rises above 80% of the programmed output voltage longer than 1.4ms then all converters shut down.

Device Reset

In order to reset the whole device, VIN has to cycle below UVLO.

- A power cycle resets all settings to default values.
- Short-circuit at one of the VO1 and VO2 resets all enable bit settings of the two converters.
- Writing VPO_VNO_EN[1:0] = 00 resets the output voltage of VO1 and VO2.
- Fast discharge control bits (DISP & DISN) can only be reset by power cycle.
- All voltage settings can only be reset by input power restart or toggling HWEN to low.
- The flag registers can only be reset by read or input power restart.

DETAILED DESCRIPTION (continued)

I²C Serial Interface and Data Communication

Standard I²C interface is used to program SGM3802 parameters and get status reports. I²C is well-known 2 wire serial communication interface that can connect one (or more) master device(s) to some slave devices for two-way communication. The bus lines are named serial data (SDA) and serial clock (SCL). The device that initiates a data transfer is a master and generates the SCL clock as long as it is master. Slave devices have unique addresses to identify. A master is typically a micro controller or a digital signal processor.

The SGM3802 operates as a slave device with address 0x36 (36H). It has five 8-bit registers.

Physical Layer

Bus lines are pulled high by pull-up resistors and in logic high state with no clocking when the bus is free. The pull-up resistors that are tied to SDA and SCL lines should be greater than 1.2kΩ at 3.3V or 1.8kΩ at 5V supply respectively. The SGM3802 does not support the general call. The SDA pin is open-drain.

I²C Data Communication

START and STOP Conditions

A transaction is started by taking control of the bus by master if the bus is free. The transaction is terminated by releasing the bus when the data transfer job is done as shown in Figure 4. All transactions begin by master which applies a START condition on the bus lines to take over the bus and exchange data. At the end, the master terminates the transaction by applying one (or more) STOP condition. START condition is defined when SCL is high and a high to low transition on the SDA is generated by master. Similarly, a STOP is defined when SCL is high and SDA goes from low to high. START and STOP are always generated by a master. After a START and before a STOP the bus is considered busy.

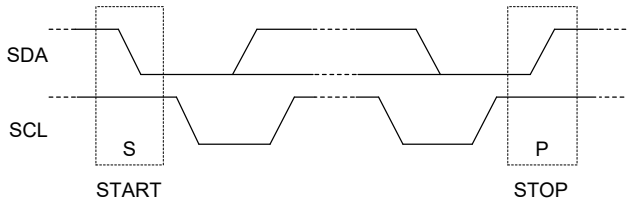


Figure 4. I²C Bus in START and STOP Conditions

Data Bit Transmission and Validity

The data bit (high or low) must remain stable on the SDA line during the high period of the clock. The state of the SDA can only change when the clock (SCL) is low. For each data bit transmission, one clock pulse is generated by master. Bit transfer in I²C is shown in Figure 5.

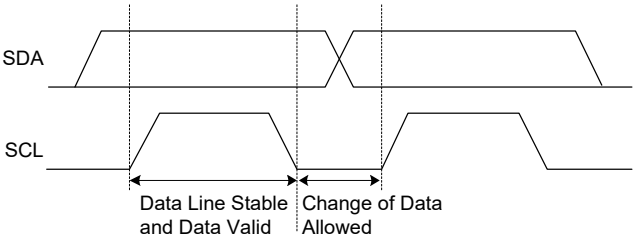


Figure 5. I²C Bus Bit Transfer

Byte Format

Data is transmitted in 8-bit packets (one byte at a time). The number of bytes in one transaction is not limited. In each packet the 8 bits are sent successively with the Most Significant Bit (MSB) first. An acknowledge (or not-acknowledge) bit must come after the 8 data bits. This bit informs the transmitter whether the receiver is ready to proceed for the next byte or not. If the slave is busy and cannot transfer another byte of data, it can hold the SCL line low and keep the master in a wait state (called clock stretching). When the slave is ready for another byte of data, it releases the clock line and data transfer can continue with clocks generated by master. Figure 6 shows the byte transfer process with I²C interface.

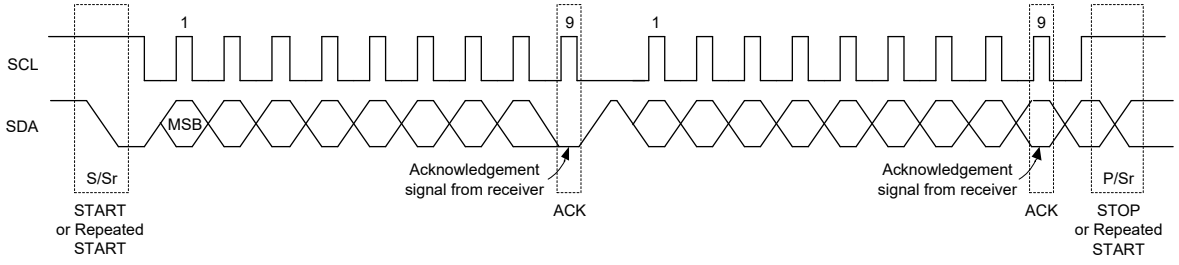


Figure 6. Byte Transfer Process

DETAILED DESCRIPTION (continued)

Acknowledge (ACK) and Not Acknowledge (NCK)

After transmission of each byte by transmitter, an acknowledge bit is replied by the receiver as the ninth bit. With the acknowledge bit the receiver informs the transmitter that the byte is received, and another byte is expected or can be sent (ACK) or it is not expected (NCK = not ACK). Clock (SCL) is always generated by master, including for the acknowledge clock pulse. SDA line is released for receiver control during the acknowledge clock pulse. And the receiver can pull the SDA line low as ACK (reply a 0 bit) or let it be high as NCK during the SCL high pulse. After that, the master can either apply a STOP (P) condition to end the transaction or send a new START (S) condition to start a new transfer (called repeated start). For example, when master wants to read a register in slave, one start is needed to send the slave address and register address, and then without a STOP condition another start is sent by master to initiate the receiving transaction from slave. Master then sends the STOP condition and releases the bus.

Data Direction Bit and Addressing Slaves

The first byte sent by master after the START is always the target slave address (7 bits) and an eighth data-direction bit (R/$\overline{W}$). R/$\overline{W}$ bit is 0 for a WRITE transaction and 1 for READ (when master is asking for data). Data direction is the same for all next bytes of the transaction. To reverse it, a new START or repeated START condition must be sent by master (STOP will end the transaction). Usually the second byte is a WRITE sending the register address that is supposed to be accessed in the next byte(s). The data transfer transaction is shown in Figure 7.

WRITE: If the master wants to write in the register, the third byte can be written directly as shown in Figure 8 for a single write data transfer. After receiving the ACK, master may issue a STOP condition to end the transaction or send the next register data, which will be written to the next address in a slave as multi-write. A STOP is needed after sending the last data.

READ: If the master wants to read a single register (Figure 9), it sends a new START condition along with device address with R/$\overline{W}$ bit = 1. After ACK is received, master reads the SDA line to receive the content of the register. Master replies with NCK to inform slave that no more data is needed (single read) or it can send an ACK to request for sending the next register content (multi-read). This can continue until an NCK is sent by master. A STOP must be sent by master in any case to end the transaction.

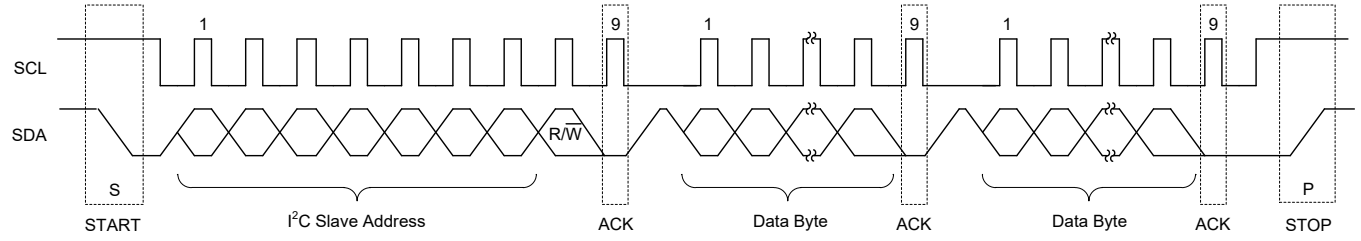


Figure 7. Data Transfer Transaction

DETAILED DESCRIPTION (continued)

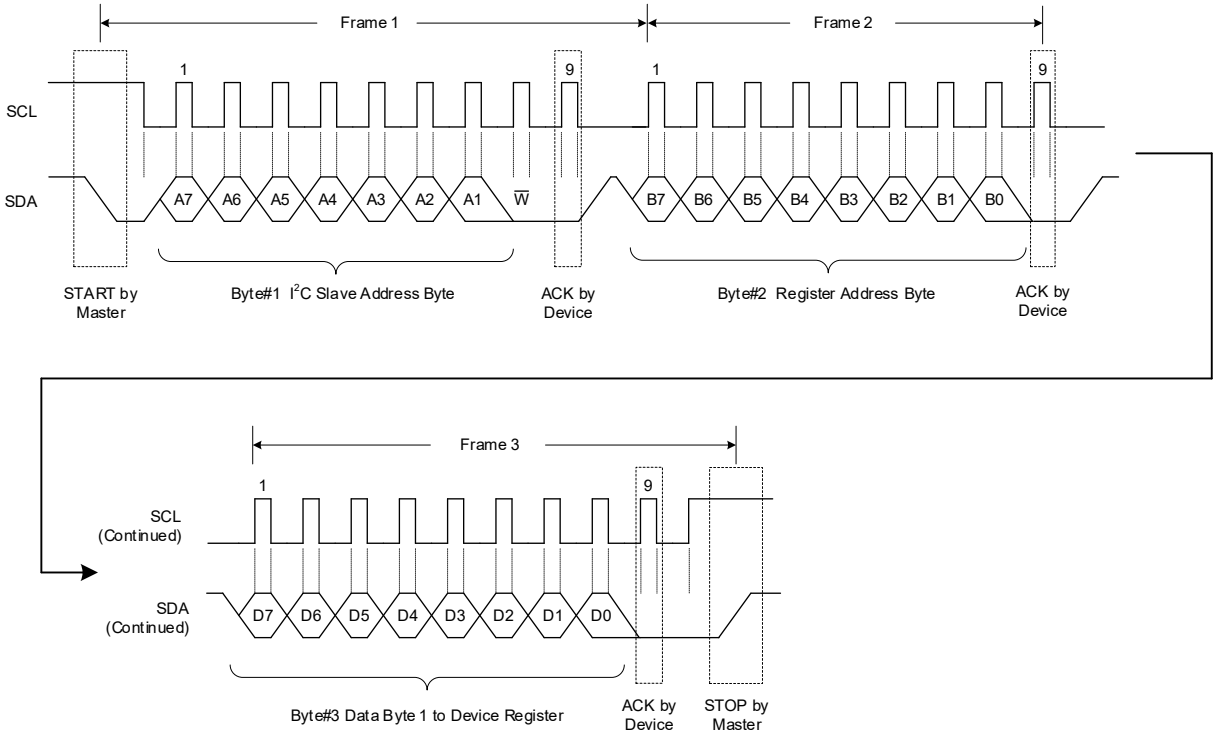


Figure 8. A Single Write Transaction

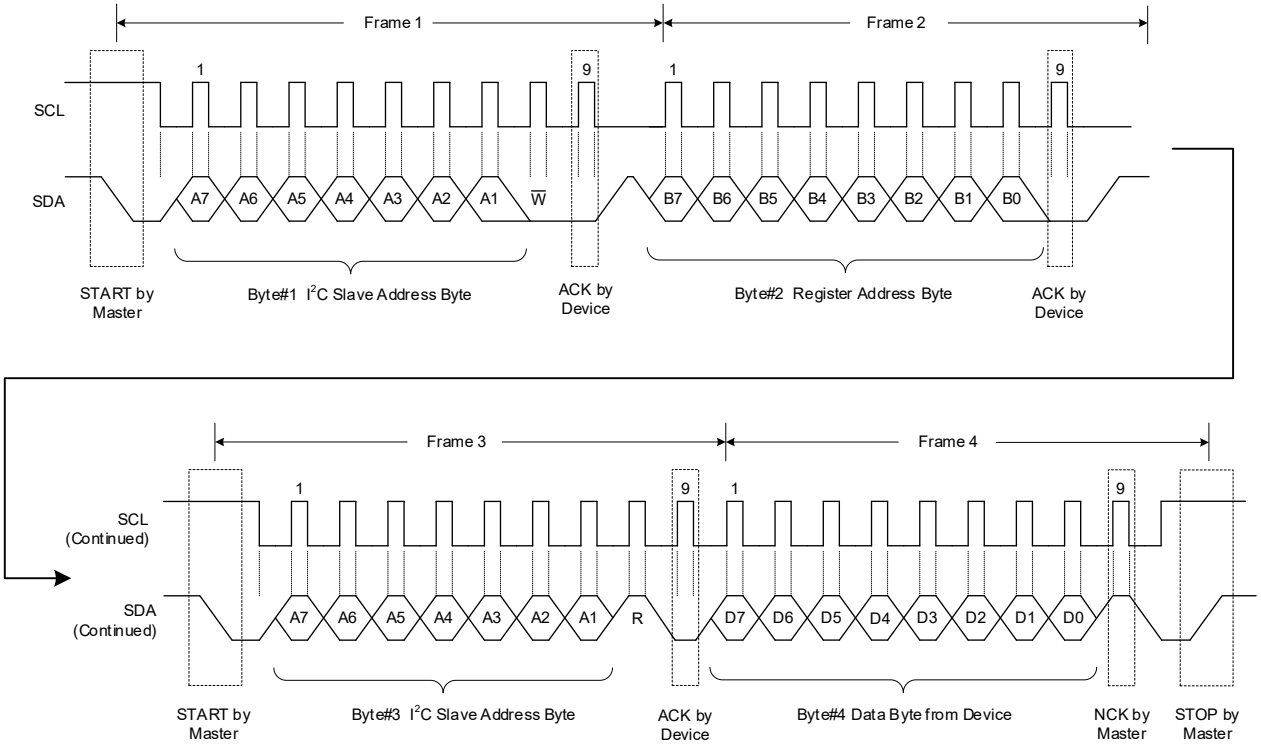


Figure 9. A Single Read Transaction

DETAILED DESCRIPTION (continued)

Data Transactions with Multi-Read or Multi-Write

Multi-read and multi-write are supported by SGM3802 as explained in Figure 10 and Figure 11. In a multi-write transaction, every new data byte sent by master is written to the next register of the device. A STOP is sent whenever master is done with writing into device registers.

In a multi-read transaction, after receiving the first register data (whose address is already written to the slave), the master replies with an ACK to send the slave for sending the next register data. This can continue as much as it is needed by master. Master sends back an NCK after the last received byte and issues a STOP condition.

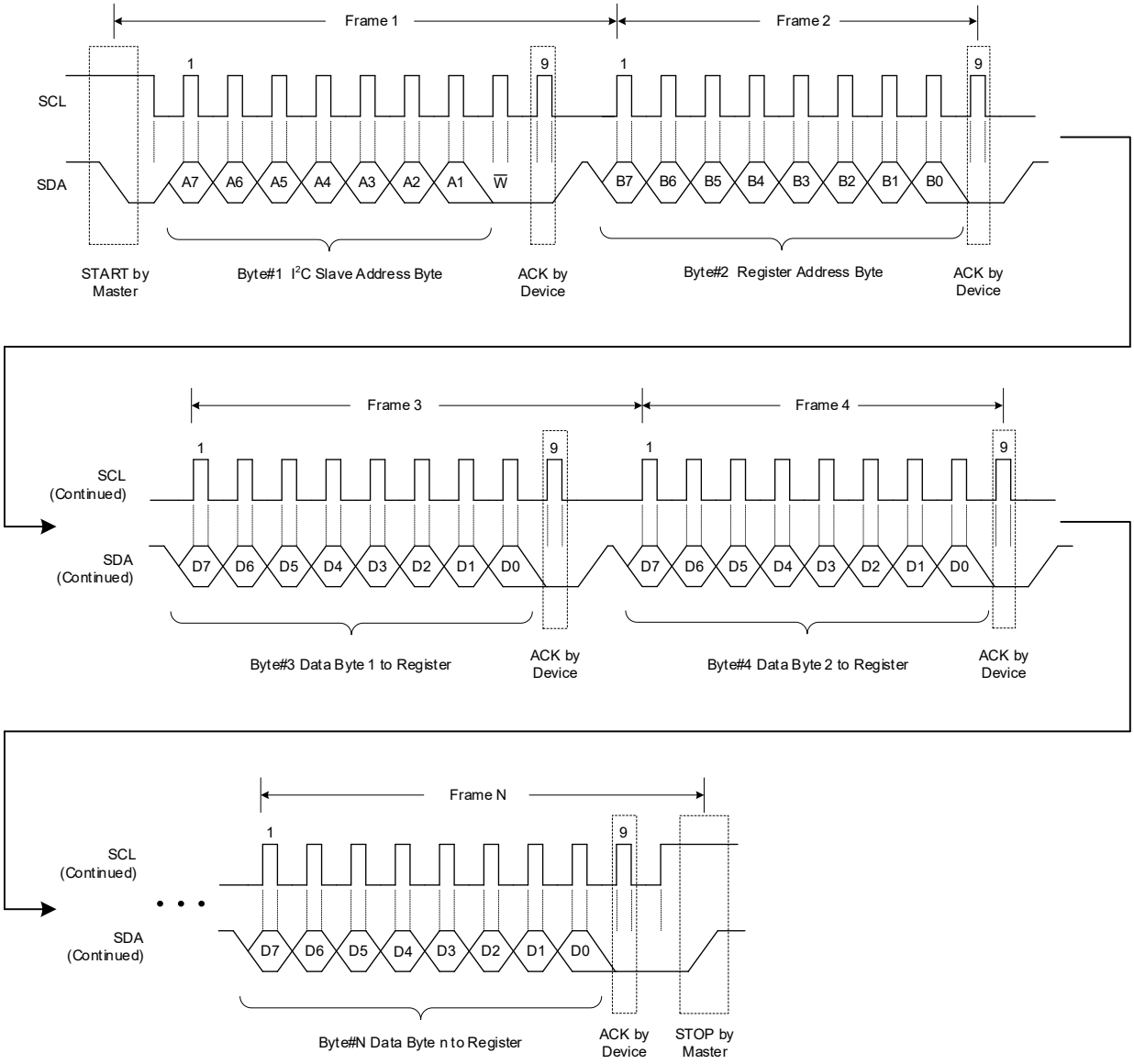


Figure 10. A Multi-Write Transaction

DETAILED DESCRIPTION (continued)

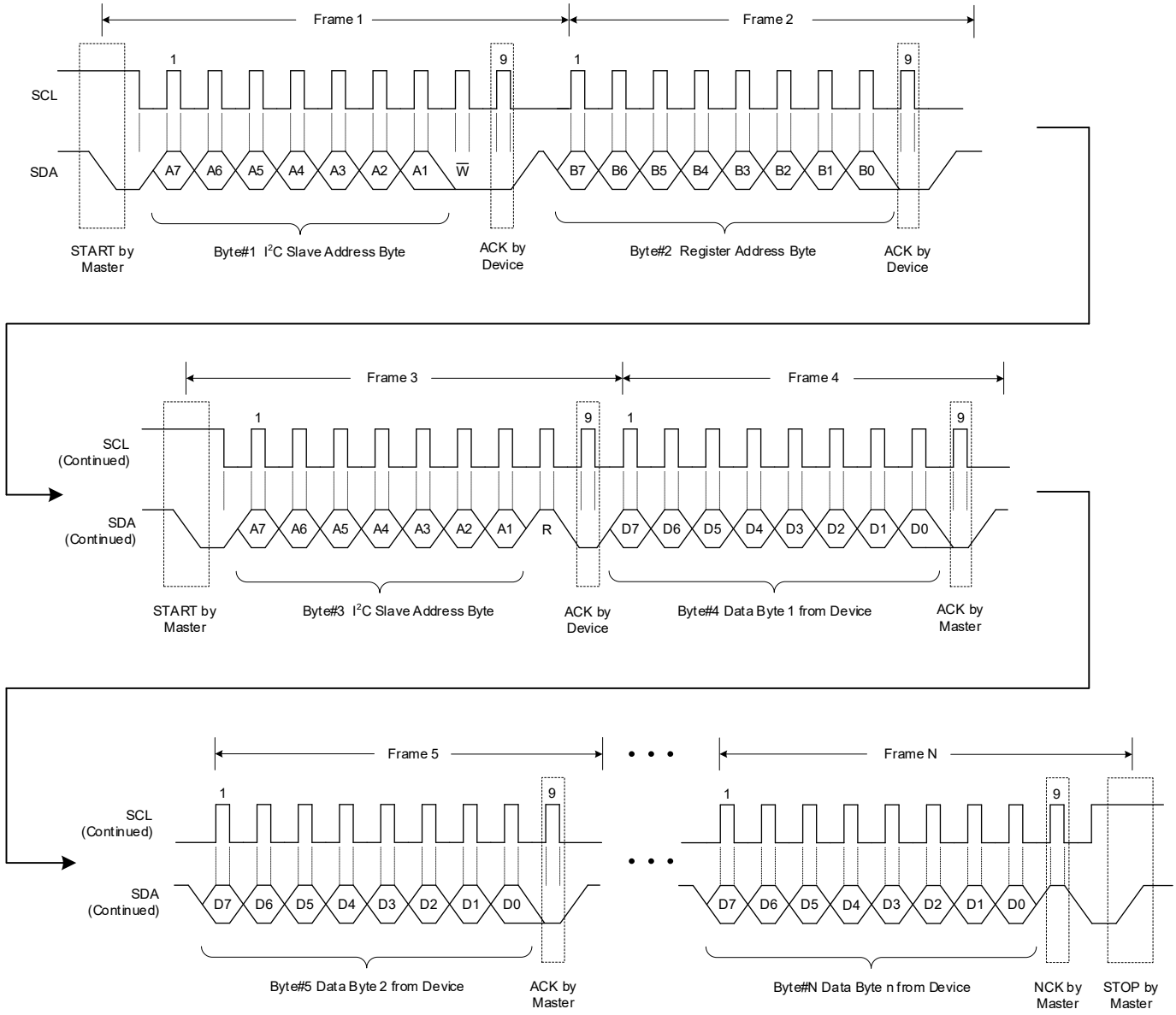


Figure 11. A Multi-Read Transaction

REGISTER MAP

All registers are 8-bit and individual bits are named from D[0] (LSB) to D[7] (MSB).

I²C Slave Address of SGM3802 is: 0x36 (0b0110110 + R/W)

Bit Types:
R: Read only
R/W: Read/Write
RC: Read Clear

Table 1. Register Map

Address	Register Name	Default Value (Hex)	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
0x01	VPO_SET	0x04 [VSEL Floating]	Reserved	VPO_DM_TIM[1:0]		VPO_SET[4:0]				
0x02	VNO_SET	0x04 [VSEL Floating]	Reserved	VO2_MIN_FREQ[1:0]		VNO_SET[4:0]				
0x03	ENABLE	0x0C	Reserved	P2N_SEQ	TDELAY[1:0]		DISP	DISN	VPO_VNO_EN[1:0]	
0x04	FLAG	0x00	Reserved				UVLO_FLAG	TSD_FLAG	VNO_SCP_FLAG	VPO_SCP_FLAG
0x05	DEVICE	0x00	DEVICE_ID[5:0]						DEVICE_REV[1:0]	

REG0x01: VPO_SET Register [reset = 0x04, 0x08 or 0x0E]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	Reserved	0	R/W	Reserved
D[6:5]	VPO_DM_TIM[1:0]	00	R/W	VPO Down Mode Hysteretic Deglitch Timer Setting 00 = 5μs (default) 01 = 1ms 10 = 20ms 11 = 50ms
D[4:0]	VPO_SET[4:0]	00100, 01000, or 01110	R/W	VPO Output Voltage Setting Refer to Table 2. Default: 5.0V, 5.4V or 6.0V, selected by VSEL

Table 2. VPO Output Voltage Setting

VPO_SET[4:0] Data (Hex)	VPO (V)	VPO_SET[4:0] Data (Hex)	VNO (V)
0x00	4.6	0x0A	5.6
0x01	4.7	0x0B	5.7
0x02	4.8	0x0C	5.8
0x03	4.9	0x0D	5.9
0x04	5.0	0x0E	6.0
0x05	5.1	0x0F	6.1
0x06	5.2	0x10	6.2
0x07	5.3	0x11	6.3
0x08	5.4	0x12	6.4
0x09	5.5	> 0x12	Remain last write value or default value

REGISTER MAPS (continued)

REG0x02: VNO_SET Register [reset = 0x04, 0x08 or 0x0E]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	Reserved	0	R/W	Reserved
D[6:5]	VO2_MIN_FREQ[1:0]	00	R/W	VO2 Operation Frequency Control at Light Load of Auto-Mode 00 = No setting (default) 01 = Frequency > 5kHz 10 = Frequency > 7.5kHz 11 = Frequency > 25kHz
D[4:0]	VNO_SET[4:0]	00100, 01000, or 01110	R/W	VNO Output Voltage Setting Refer to Table 3. Default: -5.0V, -5.4V or -6.0V, selected by VSEL

Table 3. VNO Output Voltage Setting

VNO_SET[4:0] Data (Hex)	VNO (V)	VNO_SET[4:0] Data (Hex)	VNO (V)
0x00	-4.6	0x0A	-5.6
0x01	-4.7	0x0B	-5.7
0x02	-4.8	0x0C	-5.8
0x03	-4.9	0x0D	-5.9
0x04	-5.0	0x0E	-6.0
0x05	-5.1	0x0F	-6.1
0x06	-5.2	0x10	-6.2
0x07	-5.3	0x11	-6.3
0x08	-5.4	0x12	-6.4
0x09	-5.5	> 0x12	Remain last write value or default value

REG0x03: ENABLE Register [reset = 0x0C]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	Reserved	0	R/W	Reserved
D[6]	P2N_SEQ	0	R/W	VPO and VNO Output Sequence 0 = VNO starts t_{DELAY} after VPO and shuts down before VPO (default) 1 = VPO starts t_{DELAY} after VNO and shuts down before VNO
D[5:4]	TDELAY[1:0]	00	R/W	VPO and VNO Delay Timer t_{DELAY} 00 = No delay (default) 01 = 1ms 10 = 5ms 11 = 10ms
D[3]	DISP	1	R/W	VPO Active Discharge Control when Shutdown 0 = No Discharge 1 = Discharge (default)
D[2]	DISN	1	R/W	VNO Active Discharge Control when Shutdown 0 = No Discharge 1 = Discharge (default)
D[1:0]	VPO_VNO_EN[1:0]	00	R/W	VPO & VNO Enable Control 00 = Disable Both VPO and VNO (default) 01 = Enable VPO and Disable VNO 10 = Enable VNO and Disable VPO 11 = Enable Both VPO and VNO with t_{DELAY}

REGISTER MAPS (continued)

REG0x04: FLAG Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:4]	Reserved	0000	R	Reserved
D[3]	UVLO_FLAG	0	RC	UVLO Fault Flag 0 = No UVLO fault (default) 1 = UVLO fault
D[2]	TSD_FLAG	0	RC	Thermal Shutdown Fault Flag 0 = No thermal shutdown fault (default) 1 = Thermal shutdown fault
D[1]	VNO_SCP_FLAG	0	RC	VNO Short-Circuit Fault Flag 0 = No VNO Short Fault (default) 1 = VNO Short Fault
D[0]	VPO_SCP_FLAG	0	RC	VPO Short-Circuit Fault Flag 0 = No VPO Short Fault (default) 1 = VPO Short Fault

REG0x05: Device ID Register Address [reset = 0x08]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:2]	DEVICE_ID[5:0]	000010	R	Device ID 000010 = SGM3802
D[1:0]	DEVICE_REV[1:0]	00	R	Device Revision 00 = Rev 0.0

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

MAY 2026 – REV.A.1 to REV.A.2 **Page**

Added TQFN-2.5×3-14L package ..... 1 ~ 3
Added Electrical Characteristics section 4, 5
Added and Changed Typical Performance Characteristics section 7, 8
Changed Detailed Description section 13

NOVEMBER 2025 – REV.A to REV.A.1 **Page**

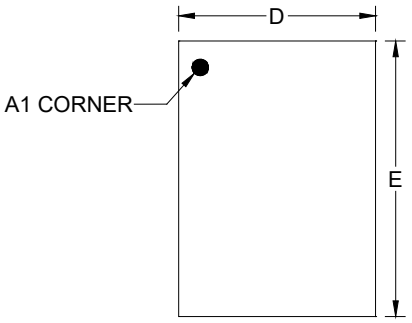
Changed Electrical Characteristics section 4, 5
Added Timing Requirements section 6

Changes from Original to REV.A (SEPTEMBER 2025) **Page**

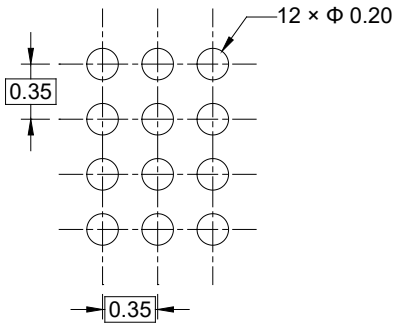
Changed from product preview to production data ..... All

PACKAGE OUTLINE DIMENSIONS

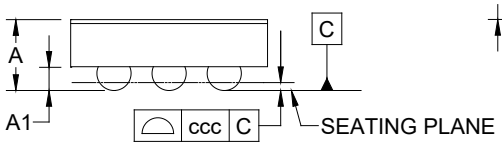
WLCSP-1.25×1.75-12B



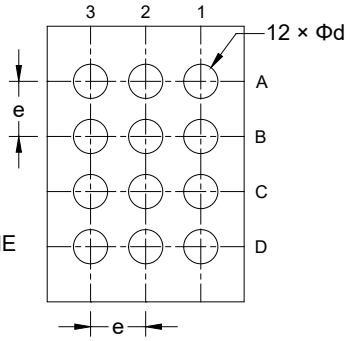
TOP VIEW



RECOMMENDED LAND PATTERN (Unit: mm)



SIDE VIEW



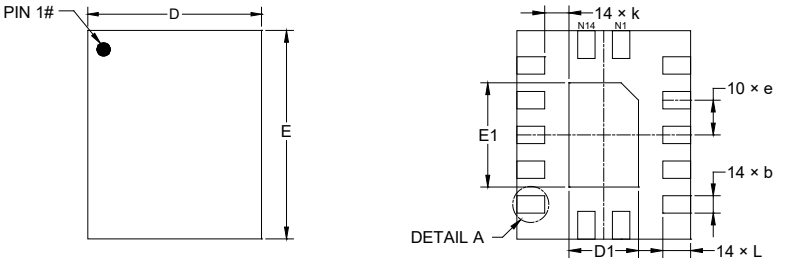
BOTTOM VIEW

Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	-	-	0.495
A1	0.131	-	0.171
D	1.220	-	1.280
E	1.720	-	1.780
d	0.187	-	0.247
e	0.350 BSC		
ccc	0.050		

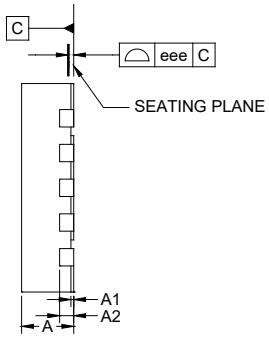
NOTE: This drawing is subject to change without notice.

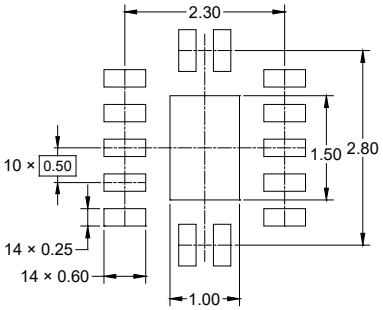
PACKAGE OUTLINE DIMENSIONS

TQFN-2.5×3-14L



TOP VIEW **BOTTOM VIEW**





SIDE VIEW **RECOMMENDED LAND PATTERN** (Unit: mm)

ALTERNATE A-1 ALTERNATE A-2

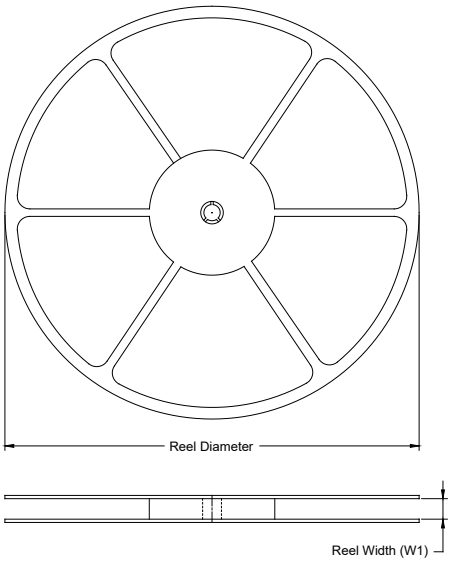
DETAIL A
ALTERNATE TERMINAL CONSTRUCTION

Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	0.700	-	0.800
A1	0.000	-	0.050
A2		0.203 REF	
b	0.200	-	0.300
D	2.400	-	2.600
D1	0.900	-	1.100
E	2.900	-	3.100
E1	1.400	-	1.600
e		0.500 BSC	
k		0.350 REF	
L	0.300	-	0.500
eee		0.080	

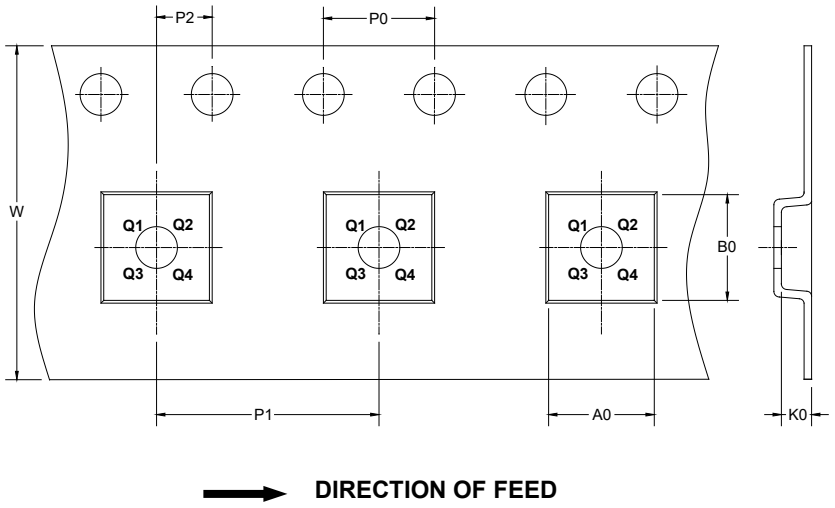
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



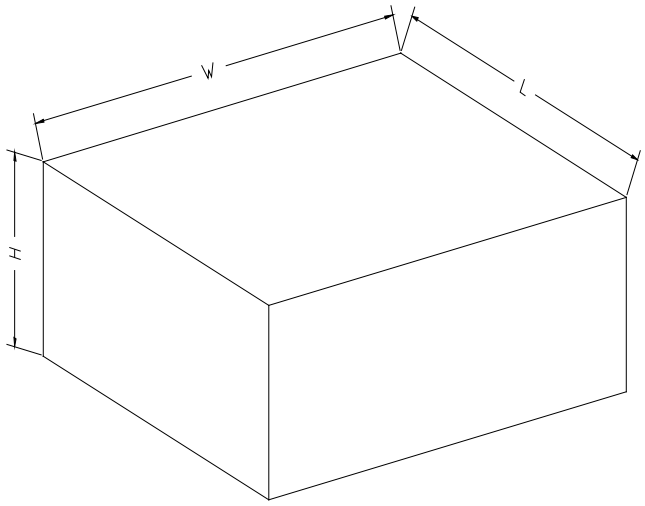
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
WLCSP-1.25×1.75-12B	7"	9.5	1.37	1.94	0.69	4.0	4.0	2.0	8.0	Q1
TQFN-2.5×3-14L	13"	12.4	2.80	3.30	1.15	4.0	4.0	2.0	12.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18
13″	386	280	370	5

DD0002