SGM882
36V Window Voltage Detector with Internal Reference for OV/UV Monitoring

GENERAL DESCRIPTION

The SGM882 is a 2.3V to 36V wide-supply voltage window detector for over-voltage (OV) and under-voltage (UV) detection. It features two high-accuracy comparators with an internal reference voltage of 400mV and two open-drain reset outputs, capable of handling up to 36V. The device can function as either two independent voltage monitors or as a window voltage detector adjusted via external resistors.

If the IN1 voltage falls below the negative threshold, nRESET1 is pulled low. And if the IN1 voltage rises over the positive threshold, nRESET1 is pulled high.

If the IN2 voltage rises over the positive threshold, nRESET2 is pulled low. And if the IN2 voltage falls below the negative threshold, nRESET2 is pulled high.

To prevent false triggering and ensure stable output operation of the device, the two comparators feature built-in hysteresis for noise rejection.

The SGM882 is available in a Green SOT-23-6 package. It operates in the temperature range of -40℃ to +125℃.

TYPICAL APPLICATION

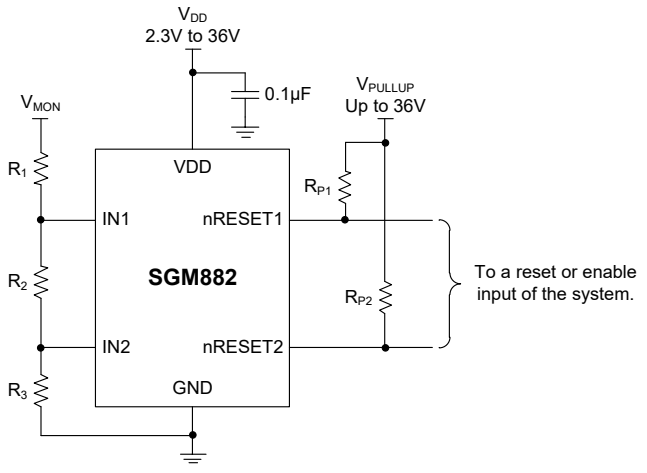


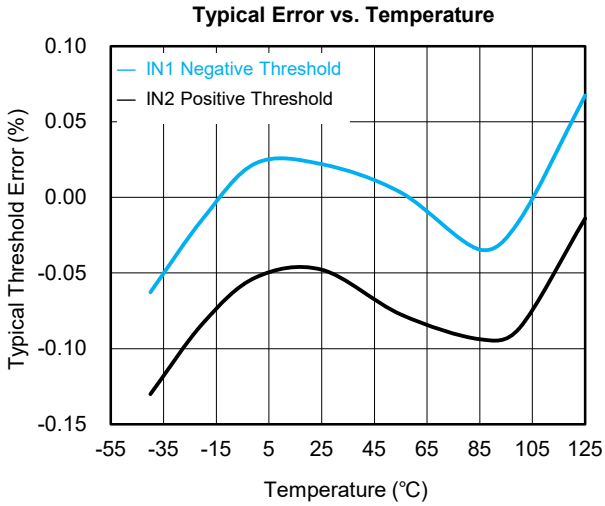
Figure 1. Typical Application Circuit

FEATURES

- **Wide Input Voltage Range: 2.3V to 36V**
- **Adjustable Threshold Down to 400mV**
- **Low Quiescent Current: 3.2μA (TYP)**
- **Low-to High Propagation Delay:**
  - **SGM882BA: 5.5μs**
  - **SGM882BB: 10ms**
  - **SGM882BC: 40ms**
  - **SGM882BD: 160ms**
  - **Accuracy: 15%**
- **High Threshold Accuracy**
  - **-40℃ to +125℃: 1.2%**
- **Internal Hysteresis: 27.5mV (TYP)**
- **Active-Low Open-Drain Reset Outputs for OV and UV Detection**
- **Available in a Green SOT-23-6 Package**

APPLICATIONS

Industrial Control Systems
Embedded Computing Modules
DSP or Microcontroller
FPGA and ASIC Systems
Notebooks and Tablet Computers
Portable and Handheld Devices
Battery-Powered Products

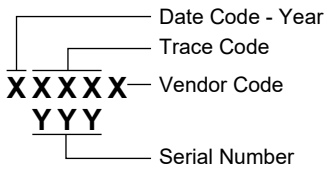


PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM882BA	SOT-23-6	-40℃ to +125℃	SGM882BAXN6G/TR	XXXXX 2FH	Tape and Reel, 3000
SGM882BB	SOT-23-6	-40℃ to +125℃	SGM882BBXN6G/TR	XXXXX 2FI	Tape and Reel, 3000
SGM882BC	SOT-23-6	-40℃ to +125℃	SGM882BCXN6G/TR	XXXXX 2FJ	Tape and Reel, 3000
SGM882BD	SOT-23-6	-40℃ to +125℃	SGM882BDXN6G/TR	XXXXX 2FK	Tape and Reel, 3000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

VDD Voltage, V_{DD} ..... -0.3V to 45V
IN1, IN2 Voltage ..... -0.3V to 6.5V
nRESET1, nRESET2 Voltage..... -0.3V to 40V
nRESET1, nRESET2 Current.....20mA
Package Thermal Resistance
SOT-23-6, θ_{JA} ..... 147.2℃/W
SOT-23-6, θ_{JB} ..... 30.2℃/W
SOT-23-6, θ_{JC} ..... 80.3℃/W
Junction Temperature.....+150℃
Storage Temperature Range .....-65℃ to +150℃
Lead Temperature (Soldering, 10s).....+260℃
ESD Susceptibility (1) (2)
HBM.....±6000V
CDM .....±1000V

NOTES:

1. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.

2. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

RECOMMENDED OPERATING CONDITIONS

VDD Voltage, V_{DD} .....2.3V to 36V
IN1, IN2 Voltage .....0V to 5.5V
nRESET1, nRESET2 Voltage.....0V to 36V
nRESET1, nRESET2 Current.....0mA to 10mA
Operating Junction Temperature Range .....-40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

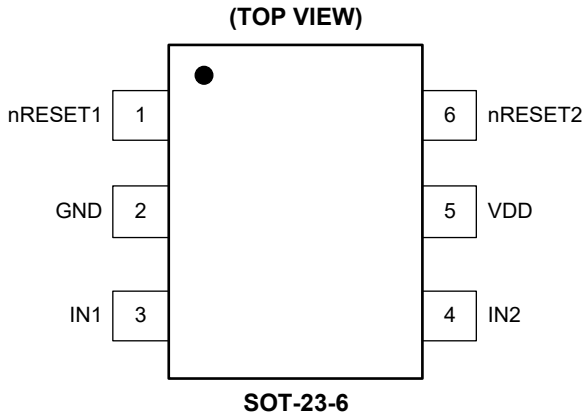
ESD SENSITIVITY CAUTION

This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION



PIN DESCRIPTION

PIN	NAME	TYPE	FUNCTION
1	nRESET1	O	IN1 Comparator Open-Drain Output. If the IN1 voltage drops below V_{IT-_IN1}, nRESET1 is pulled low. And if the IN1 voltage rises over V_{IT+_IN1}, nRESET1 is pulled high.
2	GND	G	Ground.
3	IN1	I	Comparator 1 Input. Connect IN1 to the voltage being monitored via an external resistor divider. If the IN1 voltage drops below V_{IT-_IN1}, nRESET1 is pulled low.
4	IN2	I	Comparator 2 Input. Connect IN2 to the voltage being monitored via an external resistor divider. If the IN2 voltage rises over V_{IT+_IN2}, nRESET2 is pulled low.
5	VDD	I	2.3V to 36V Power Supply Voltage. Connect a 0.1μF ceramic capacitor between VDD and GND.
6	nRESET2	O	IN2 Comparator Open-Drain Output. If the IN2 voltage rises over V_{IT+_IN2}, nRESET2 is pulled low. And if the IN2 voltage drops below V_{IT-_IN2}, nRESET2 is pulled high.

NOTE: I = input, O = output, G = ground.

ELECTRICAL CHARACTERISTICS

(V_{DD} = 2.3V to 36V, T_A = -40℃ to +125℃, R_{P1} = R_{P2} = 100kΩ, typical values are measured at V_{DD} = 12V and T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage Range	V_{DD}			2.3		36	V
Power-On Reset Voltage (1)	V_{POR}	V_{OL} ≤ 0.2V, pulled up to an external voltage rail of 36V				1.4	V
IN1 Pin Negative Input Threshold Voltage	V_{IT-_IN1}			395.2	400	404.8	mV
IN1 Pin Positive Input Threshold Voltage	V_{IT+_IN1}			421	427.5	434	mV
IN1 Pin Hysteresis Voltage (V_{HYS_IN1} = V_{IT+_IN1} - V_{IT-_IN1})	V_{HYS_IN1}			20	27.5	35	mV
IN2 Pin Negative Input Threshold Voltage	V_{IT-_IN2}			366	372.5	379	mV
IN2 Pin Positive Input Threshold Voltage	V_{IT+_IN2}			395.2	400	404.8	mV
IN2 Pin Hysteresis Voltage (V_{HYS_IN2} = V_{IT+_IN2} - V_{IT-_IN2})	V_{HYS_IN2}			20	27.5	35	mV
Low-Level Output Voltage	V_{OL}	V_{DD} = 2.3V, I_{nRESET} = 3mA			40	100	mV
		V_{DD} = 5V, I_{nRESET} = 5mA			60	130	
Input Current at IN1 and IN2 Pins	I_{IN}	0V ≤ V_{IN1} = V_{IN2} ≤ 3V		-30	1	30	nA
Open-Drain Output Leakage Current	I_{D_LEAK}	V_{nRESET} = 36V			10	200	nA
Supply Current	I_{DD}				3.2	6.6	μA
Under-Voltage Lockout	UVLO	V_{DD} rising		1.7	2	2.3	V
High-to-Low Propagation Delay (2)	t_{PD_HL}	V_{DD} = 12V, ±200mV input overdrive, R_L = 100kΩ, V_{OH} = 0.9 × V_{DD}, V_{OL} = 250mV			5.3		μs
Low-to-High Propagation Delay (2)	t_{PD_LH}	V_{DD} = 12V, ±200mV input overdrive, V_{OH} = 0.9 × V_{DD}, V_{OL} = 250mV	SGM882BA		5.5		μs
			SGM882BB	8.5	10	11.5	ms
			SGM882BC	34	40	46	
			SGM882BD	136	160	184	
Startup Delay (3)	t_{D_START}	V_{DD} = 5V			740		μs
Output Rise Time	t_R	V_{DD} = 12V, C_L ≤ 10pF, V_O = (0.1 to 0.9) × V_{DD}			5		μs
Output Fall Time	t_F	V_{DD} = 12V, C_L ≤ 10pF, V_O = (0.9 to 0.1) × V_{DD}			0.08		μs

NOTES:

1. V_{POR} represents the minimum VDD voltage to ensure a controlled output condition.
2. High-to-low and low-to-high refers to the transition at nRESET1 and nRESET2 pins.
3. During power-on, V_{DD} must exceed UVLO for at least t_{D_START} to finish the startup procedure.

ELECTRICAL CHARACTERISTICS (continued)

Timing Diagram

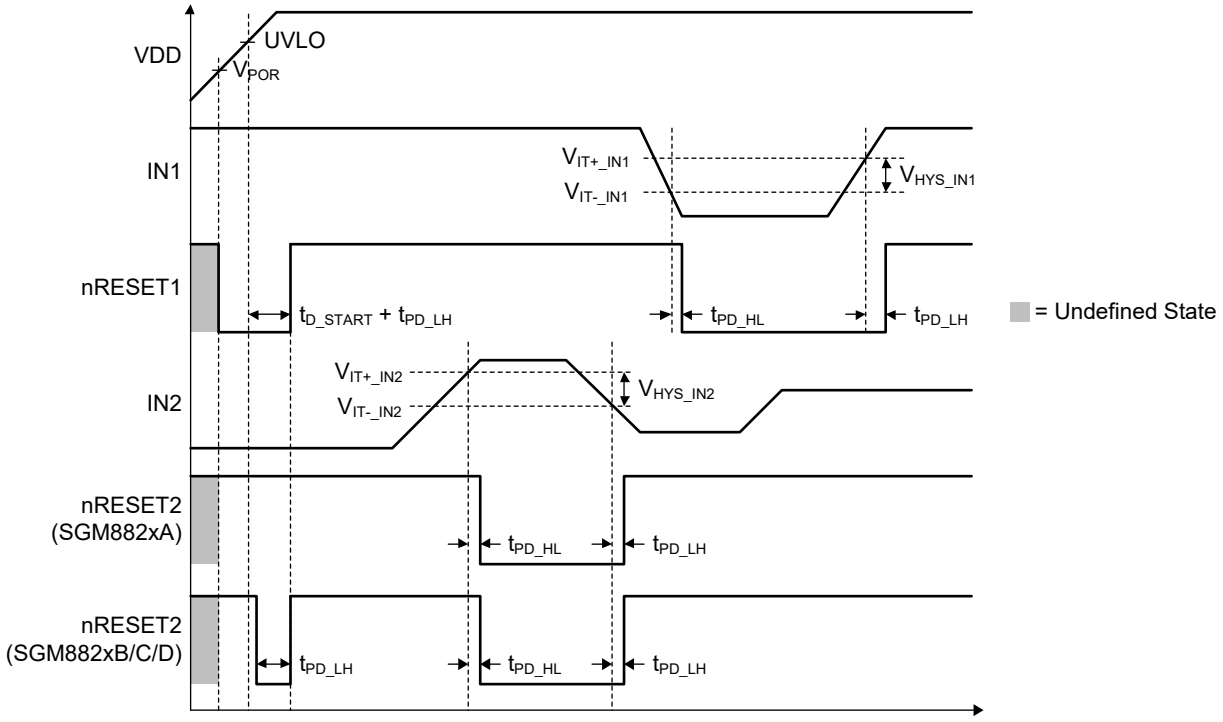
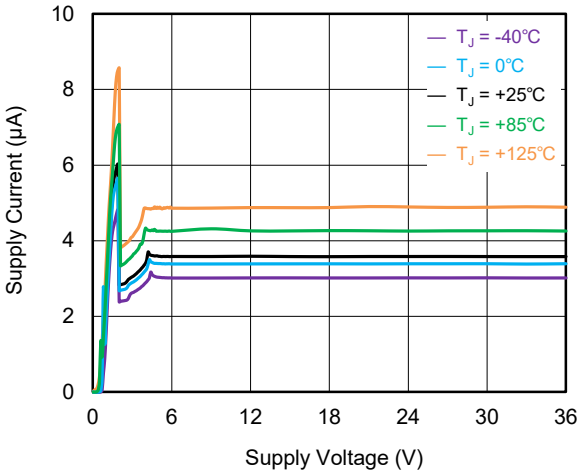


Figure 2. Timing Diagram

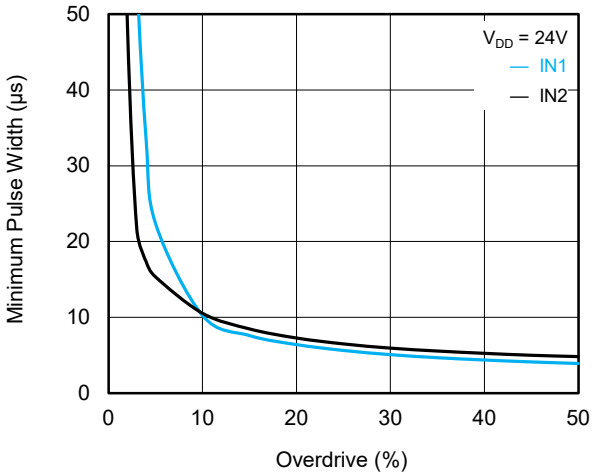
TYPICAL PERFORMANCE CHARACTERISTICS

T_J = +25℃ and V_{DD} = 12V, unless otherwise noted.

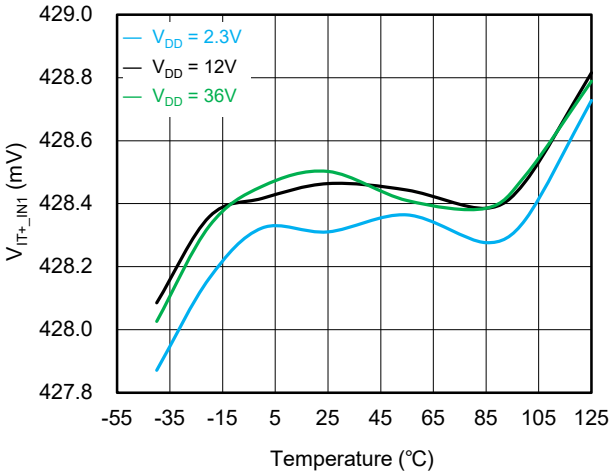
Supply Current vs. Supply Voltage



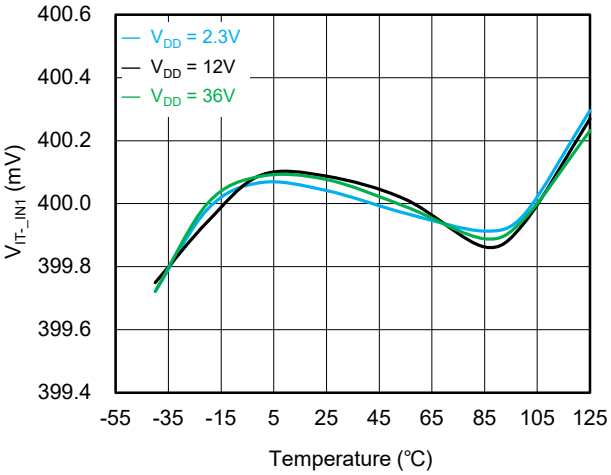
Minimum Pulse Duration vs. Threshold Overdrive Voltage (1)



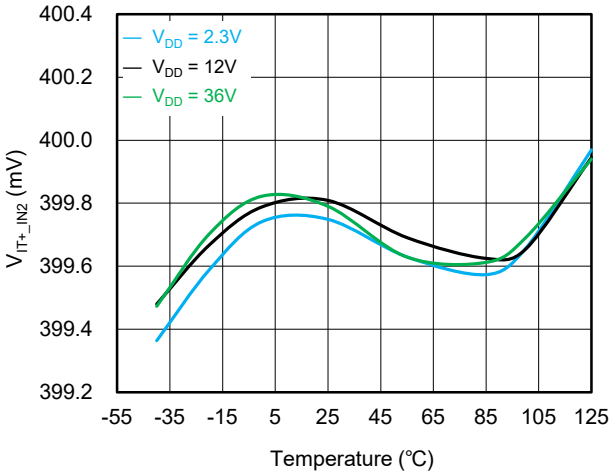
IN1 Positive Input Threshold Voltage (V_{IT+_IN1}) vs. Temperature



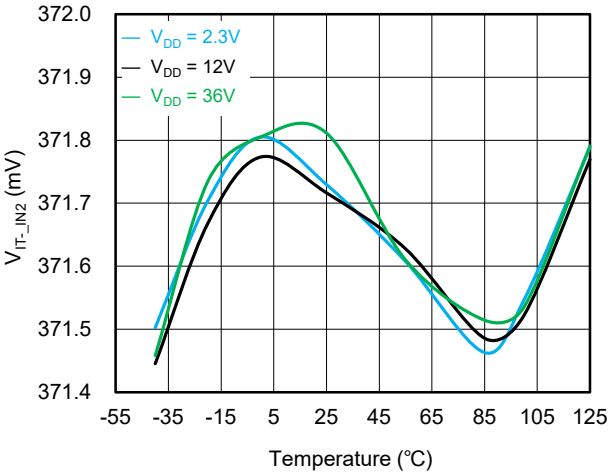
IN1 Negative Input Threshold Voltage (V_{IT-_IN1}) vs. Temperature



IN2 Positive Input Threshold Voltage (V_{IT+_IN2}) vs. Temperature



IN2 Negative Input Threshold Voltage (V_{IT-_IN2}) vs. Temperature

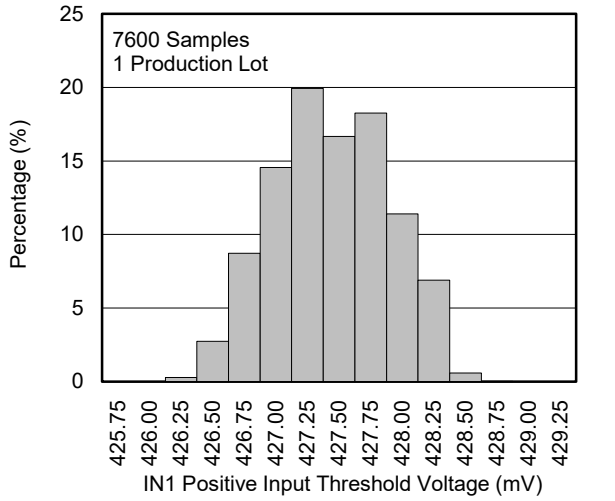


NOTE: 1. Minimum pulse duration required to trigger output high-to-low transition. IN1 = negative spike below V_{IT-_IN1} and IN2 = positive spike above V_{IT+_IN2}.

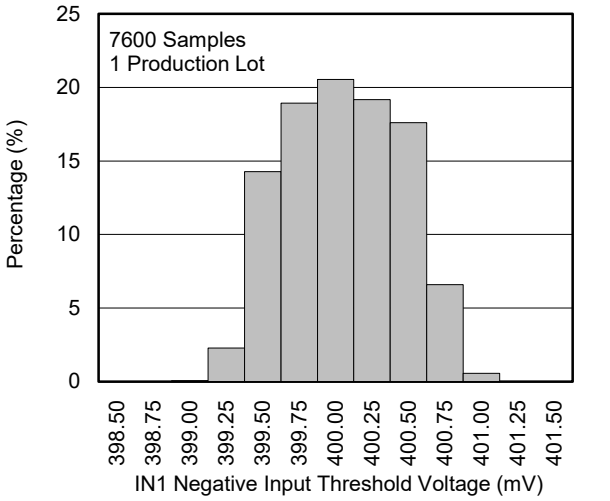
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_J = +25℃ and V_{DD} = 12V, unless otherwise noted.

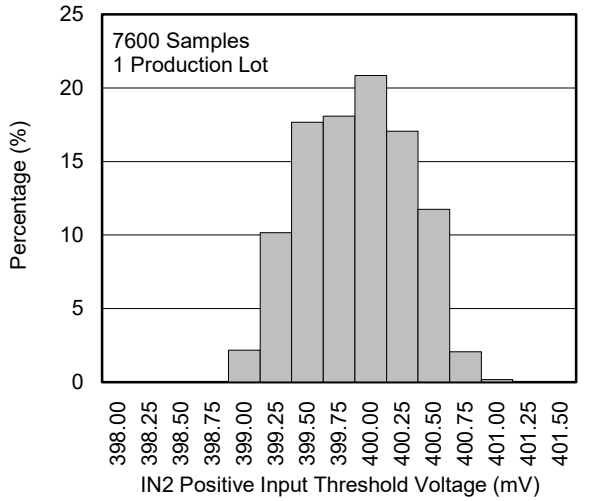
IN1 Positive Input Threshold Voltage (V_{IT+_IN1}) Distribution



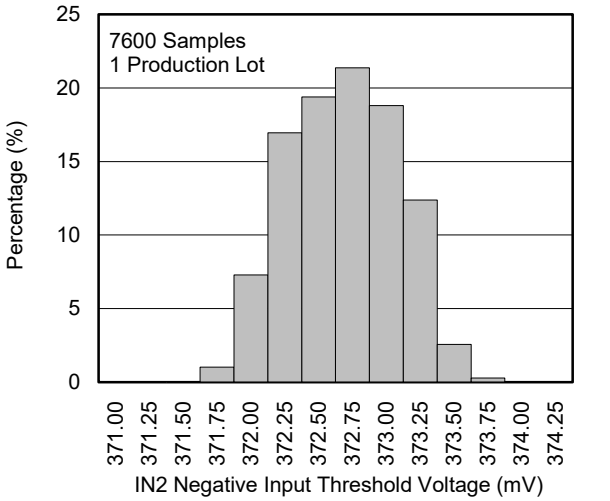
IN1 Negative Input Threshold Voltage (V_{IT-_IN1}) Distribution



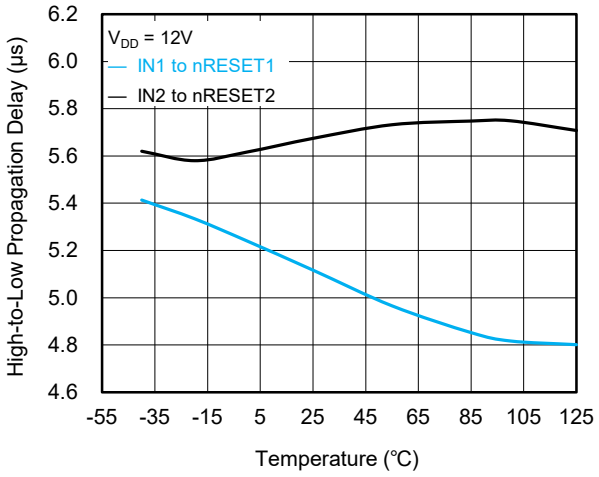
IN2 Positive Input Threshold Voltage (V_{IT+_IN2}) Distribution



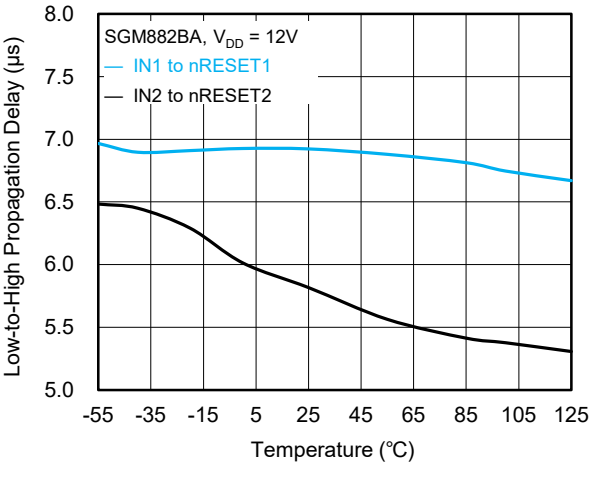
IN2 Negative Input Threshold Voltage (V_{IT-_IN2}) Distribution



High-to-Low Propagation Delay vs. Temperature



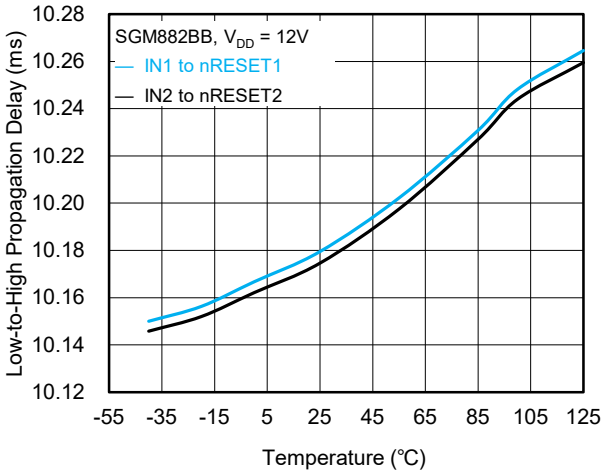
Low-to-High Propagation Delay vs. Temperature



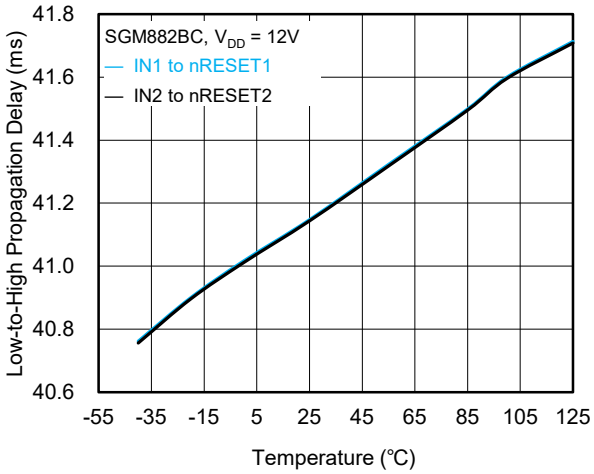
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_J = +25℃ and V_{DD} = 12V, unless otherwise noted.

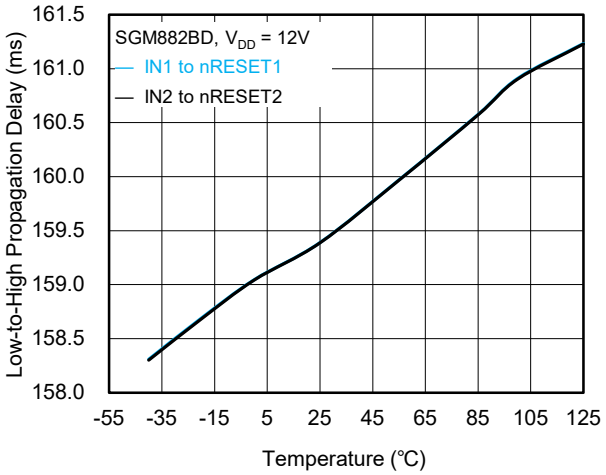
Low-to-High Propagation Delay vs. Temperature



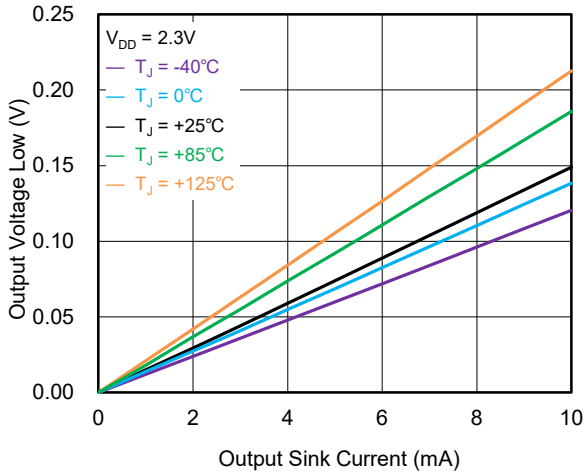
Low-to-High Propagation Delay vs. Temperature



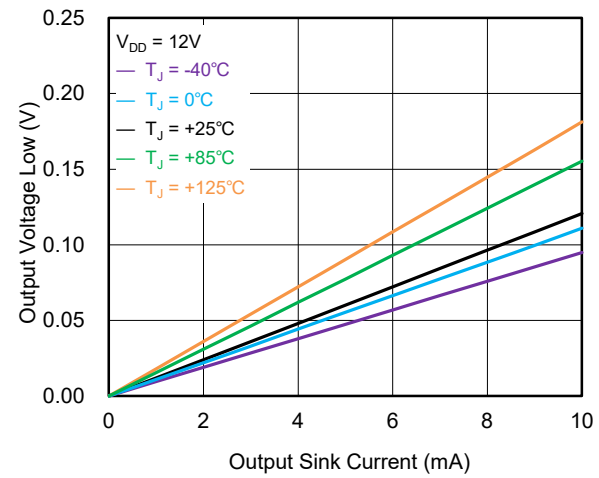
Low-to-High Propagation Delay vs. Temperature



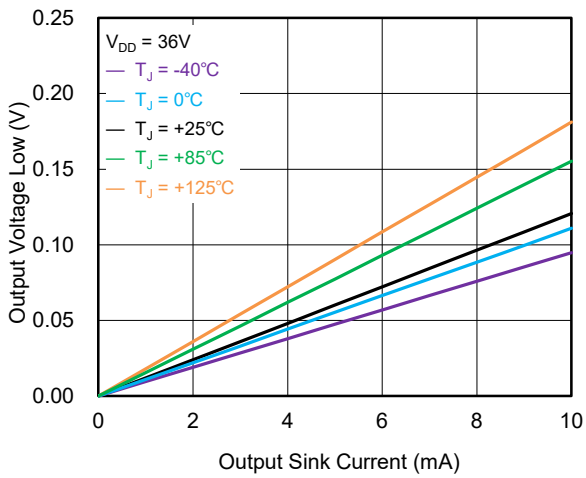
Output Voltage Low vs. Output Sink Current



Output Voltage Low vs. Output Sink Current



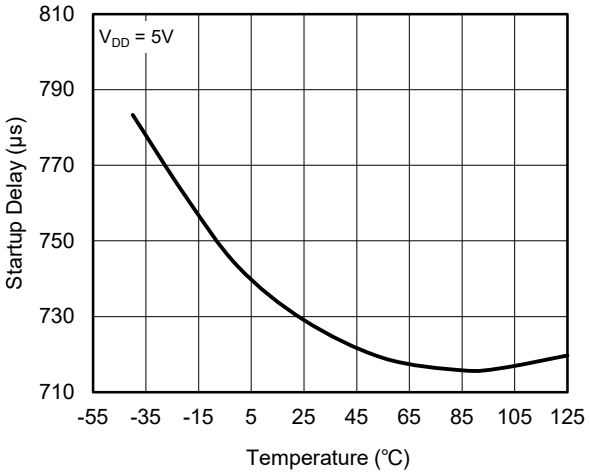
Output Voltage Low vs. Output Sink Current



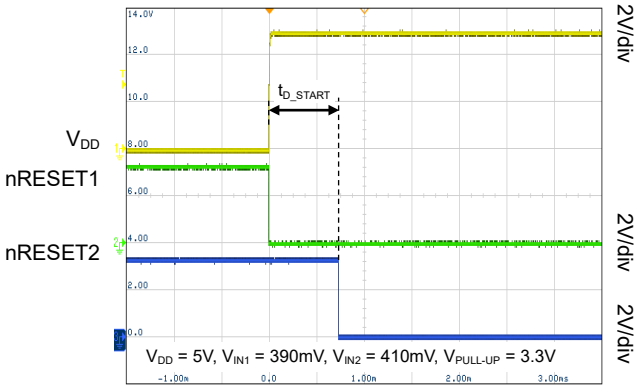
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_J = +25℃ and V_{DD} = 12V, unless otherwise noted.

Startup Delay vs. Temperature

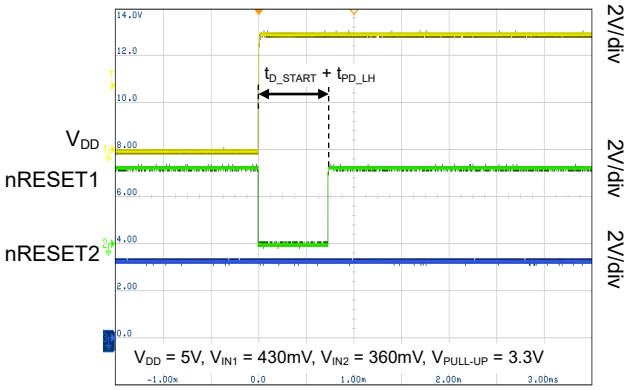


Startup Delay (SGM882BA)



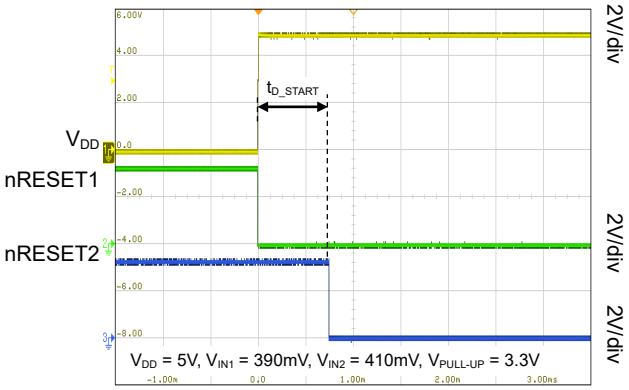
Time (500μs/div)

Startup Delay (SGM882BA)



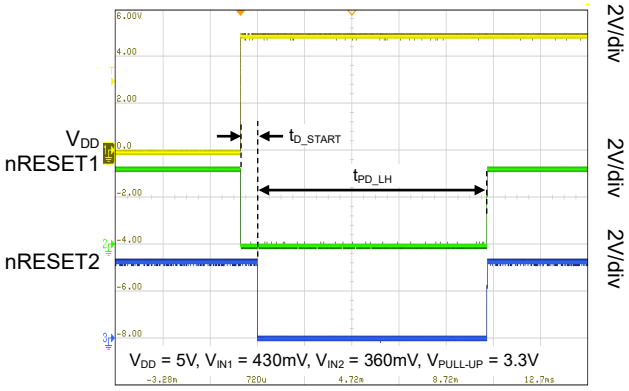
Time (500μs/div)

Startup Delay (SGM882BB)



Time (500μs/div)

Startup Delay (SGM882BB)



Time (2ms/div)

FUNCTIONAL BLOCK DIAGRAM

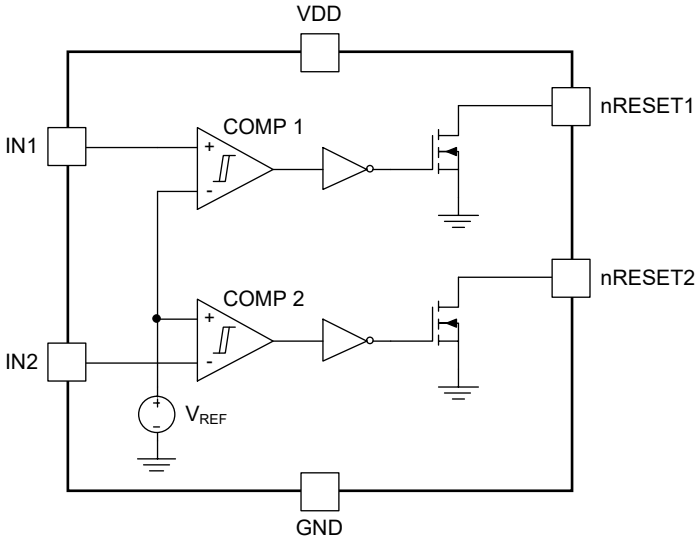


Figure 3. Block Diagram

DETAILED DESCRIPTION

Overview

The SGM882 is a 2.3V to 36V wide-supply voltage window detector for over-voltage (OV) and under-voltage (UV) detection. It features two high-accuracy comparators (referred to as 1 and 2) with an internal reference voltage of 400mV and two open-drain reset outputs, capable of handling up to 36V and can sink up to 10mA.

Use an external resistor divider network to set the IN1 and IN2 pins to sense voltages greater than 0.4V. These inputs allow the use of high-value resistors in the divider without sacrificing measurement accuracy for the low leakage current. To implement a window voltage detection function, connect both input pins through a three-resistor network (see the Window Voltage Detector Considerations section). In this configuration, the SGM882 triggers its output signals when the monitored voltage remains inside the defined window range. The two comparators can also be used as separate, independent monitors. The relationship between input states and output behavior is summarized in Table 1. The device supports wide range of threshold voltages, making it suitable for various system requirements.

Table 1. Truth Table

Condition	Output	Status
IN1 > V_{IT+_IN1}	nRESET1 high	Output 1 high impedance
IN1 < V_{IT-_IN1}	nRESET1 low	Output 1 asserted
IN2 > V_{IT+_IN2}	nRESET2 low	Output 2 asserted
IN2 < V_{IT-_IN2}	nRESET2 high	Output 2 high impedance

Feature Description

Inputs (IN1, IN2)

The SGM882 integrates two high-accuracy comparators with built-in hysteresis, providing noise immunity and ensuring stable operation. Each comparator has one external input and one internal input connected to the internal reference. The IN2 rising threshold and the IN1 falling threshold are designed and trimmed to match the reference voltage of 400mV. It enhances device accuracy when functioning as a window voltage detector. It is recommended to add a 1nF to 10nF bypass capacitor at the comparator (IN1 and IN2) input for noisy applications, as it helps to reduce susceptibility to transient voltage fluctuations in the monitored signal.

Comparator 1 drives its output (nRESET1) to a logic low state when the IN1 voltage drops below the V_{IT-_IN1} threshold. nRESET1 returns to a high-impedance condition once IN1 exceeds the V_{IT+_IN1} level. Similarly, comparator 2 pulls nRESET2 low when IN2 rises above V_{IT+_IN2}, while nRESET2 reverting to high-impedance once IN2 falls below V_{IT-_IN2}. The timing relationship between thresholds and outputs is illustrated in Figure 2. Dual-comparators enable comprehensive window voltage monitoring functionality, and further implementation details are provided in the Window Voltage Detector Considerations section.

IN1 and IN2 both have internal clamp. When IN1 or IN2 monitors high-voltage rail via resistor divider as Figure 1, if R_3 or R_2 & R_3 is open-circuited, the clamp circuit has limited protection for the IN1/2 pin. The protection is limited as IN1/2 = 6.5V, the current flows through IN1/2 is about 300μA. So considering the monitored voltage and the connecting resistor, the clamp is valid when open-circuit event happens and the current through the resistor is smaller than 300μA, as (V_{MON} - 6.5)/R_1 < 300μA.

Otherwise, the internal clamp protection is invalid and IN1/2 may be damaged if the voltage at the IN1/2 pin is higher than the absolute voltage.

Outputs (nRESET1, nRESET2)

The reset output pins are designed to be used as reset inputs or enable inputs for typical applications like a micro-processor (μP), a DC/DC converter or a low dropout linear regulator (LDO).

The nRESETx pins are open-drain outputs. There must be a pull-up resistor to pull up the nRESETx high when the outputs enter a high-impedance state. Connect the pull-up resistors to appropriate voltage rails, ensuring the outputs can interface with other devices at correct voltage levels. The outputs of SGM882 support pull-up voltages up to 36V, regardless of the device's supply voltage. To maintain proper voltage levels, carefully consider the values of pull-up resistor. These values are determined by V_{OL}, output capacitive loading, and output leakage current (I_{D_LEAK}), all of which are specified in the Electrical Characteristics table. Wired-OR logic can be used to combine nRESET1 and nRESET2 into a single logic signal.

DETAILED DESCRIPTION (continued)

Output assertion and high-impedance transitions follow the behavior described in Table 1 and the Inputs (IN1, IN2) section. The dynamic relationship between threshold crossings and output states is depicted in the timing diagram of Figure 2.

Device Functional Modes

V_{DD} is below V_{POR} (V_{DD} < V_{POR})

When V_{DD} is below V_{POR}, the nRESET1 and nRESET2 are in a high-impedance state.

Under-Voltage Lockout (V_{POR} ≤ V_{DD} < UVLO)

When V_{POR} ≤ V_{DD} < UVLO, the nRESET1 signal is asserted to logic low and the nRESET2 will turn into a high-impedance state regardless of the IN1/2 signal.

Normal Operation (V_{DD} ≥ UVLO)

When V_{DD} is above or equal to UVLO, the nRESET1/2 signal is determined by IN1/2 respectively, as shown in Table 1.

APPLICATION INFORMATION

Application Information

The SGM882 operates as a precision dual-voltage detector in various systems. The monitored voltage (V_{MON}), supply voltage (V_{DD}), and output pull-up rail can be powered independently or interconnected, offering flexible design options. The subsequent sections provide a detailed explanation of how to configure the connection schemes.

Window Voltage Detector Considerations

By using a resistor divider network, the inverting and non-inverting configurations of the comparators form a window voltage detector circuit (see Figure 4 and Figure 5). With a resistor divider network, the input pins can monitor any system voltage exceeding 400mV. Specifically, IN1 is used for under-voltage monitoring, while IN2 is used for over-voltage monitoring.

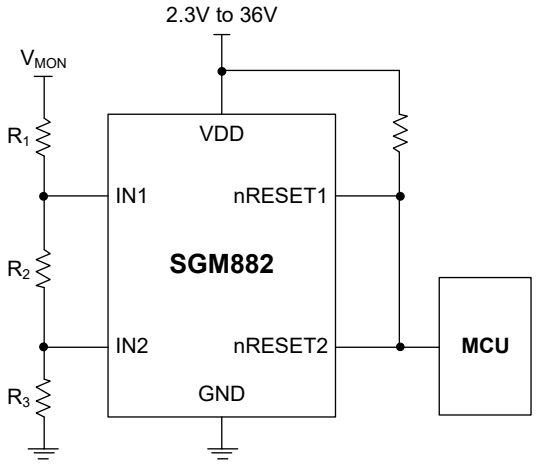


Figure 4. Window Voltage Detector Block Diagram

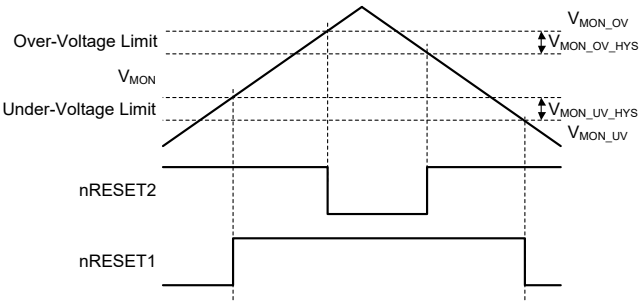


Figure 5. Window Voltage Detector Timing Diagram

The SGM882 identifies over-voltage or under-voltage conditions with maximum accuracy. Its most accurate threshold voltages are V_{IT-_IN1} and V_{IT+_IN2}, which correspond to the falling under-voltage flag and rising over-voltage flag, respectively. These thresholds reflect the accuracy when the monitored voltage lies within the valid window (where both nRESET1 and nRESET2 are in a high-impedance state) and respond to the under-voltage limit (V_{MON_UV}) and over-voltage limit (V_{MON_OV}) trigger voltages, respectively. If the monitored voltage falls outside the valid window — i.e., V_{MON} is below V_{MON_UV} or above the V_{MON_OV} — the input threshold voltages required to re-enter the valid window are V_{IT+_IN1} or V_{IT-_IN2}, which correspond to the monitored voltages, V_{MON_UV} + $V_{MON\_UV\_HYS}$ and V_{MON_OV} - $V_{MON\_OV\_HYS}$, respectively.

Use Equations 1 to 3 to calculate resistor divider values.

$$R_{TOTAL} = R_1 + R_2 + R_3 \quad (1)$$

Select an R_{TOTAL} value such that the current flowing through the divider is roughly 100 times higher than the input current at the IN1 and IN2 pins. High-value resistors reduce current consumption, but input bias current will compromise V_{IT} accuracy when the current through the resistors is too low.

APPLICATION INFORMATION (continued)

Calculate R_3 through Equation 2:

$$R_3 = \frac{R_{TOTAL}}{V_{MON\_OV}} \times V_{IT+\_IN2} \quad (2)$$

V_{MON_OV} refers to the target voltage corresponding to the occurrence of over-voltage.

Calculate R_2 through Equation 3:

$$R_2 = \left(\frac{R_{TOTAL}}{V_{MON\_UV}} \times V_{IT-\_IN1} \right) - R_3 \quad (3)$$

V_{MON_UV} refers to the target voltage corresponding to the occurrence of under-voltage.

Input and Output Configurations

The examples of different input/output configurations are shown in Figure 6 to Figure 9.

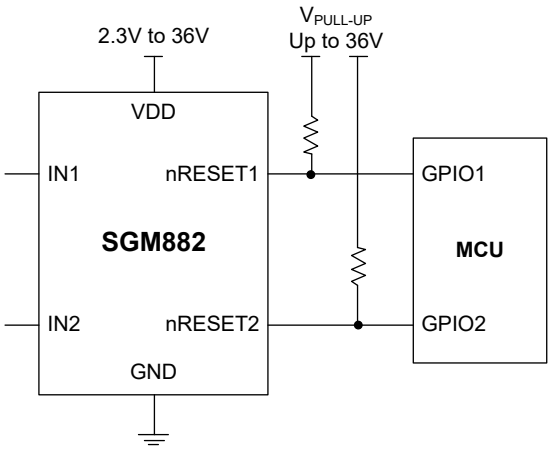


Figure 6. Interfacing to Voltages Other than V_{DD}

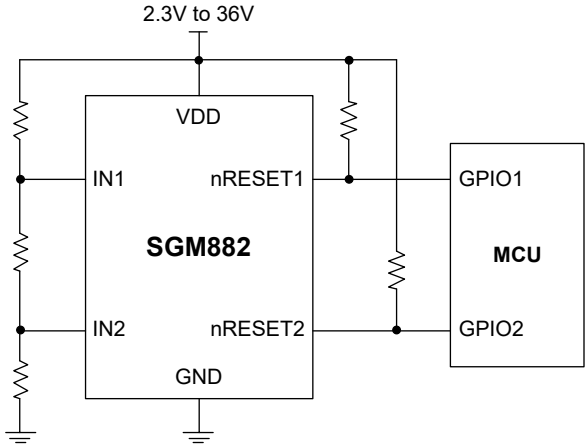
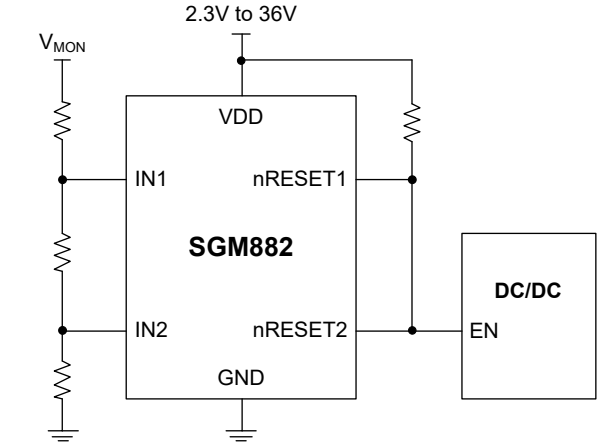
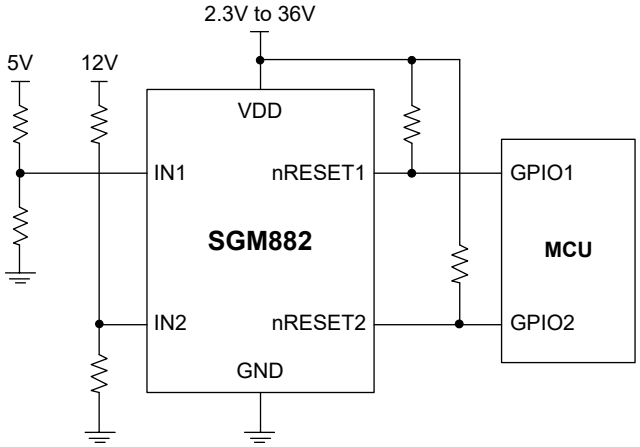


Figure 7. Monitoring the Same Voltage as V_{DD}



NOTE: Users can monitor the voltage higher than V_{DD_MAX} by connecting an external resistor divider.

Figure 8. Monitoring a Voltage Other than V_{DD}



NOTE: nRESET1 is pulled low when an UV condition is detected on the 5V rail, while nRESET2 is pulled low when an OV condition is detected on the 12V rail.

Figure 9. Monitoring Over-Voltage for One Rail and Under-Voltage for a Different Rail

Immunity to Input Pin Voltage Transients

The SGM882 can suppress short voltage transient spikes on its input pins. Sensitivity to such transients depends on both transient duration and amplitude. Refer to the Minimum Pulse Duration vs. Threshold Overdrive Voltage curve in Typical Performance Characteristics for details.

APPLICATION INFORMATION (continued)

Typical Application

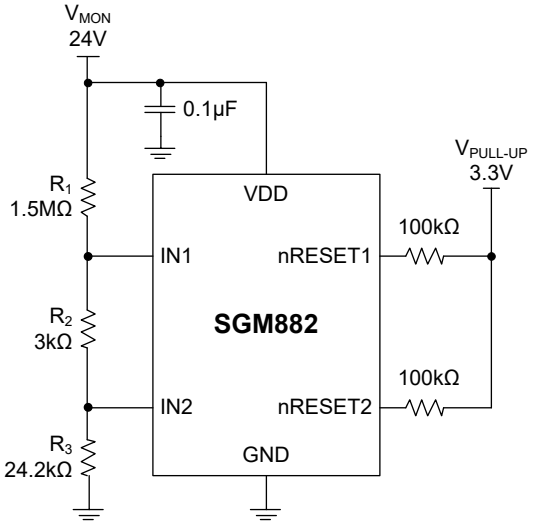


Figure 10. 24V, 10% Window Voltage Detector

Design Requirements

Table 2 lists the design parameters for this example.

Table 2. Design Parameters

Parameter	Design Requirement	Design Result
Monitored Voltage	24V nominal, rising (V_{MON_OV}) and falling (V_{MON_UV}) threshold ±10% nominal (26.4V and 21.6V, respectively)	V_{MON_OV} = 25.59V V_{MON_UV} = 22.13V
Output Logic Voltage	3.3V CMOS	3.3V CMOS
Maximum Current Consumption	30μA	16μA

Detailed Design Procedure

Given the 24V supply requirement for MCU (±10% tolerance) and the power source (±2% regulation accuracy), the UV and OV thresholds must be positioned within the center of the allowable monitoring window.

Use Equation 1 to calculate the minimum total resistance of the resistor network required to meet the current consumption specification. In this example, the current through the resistor network is set to 16μA, though a lower current can be chosen. Be cautious of the leakage currents resulting from the manufacturing process. If these leakage currents exceed 1% of the resistor network current, they will significantly affect accuracy.

Thus, the value of R_{TOTAL} can be calculated as:

$$R_{TOTAL} = \frac{V_{MON\_OV}}{I} = \frac{26.4V}{16\mu A} = 1.65M\Omega \quad (4)$$

R_3 can be calculated by Equation 5 with R_{TOTAL}.

$$R_3 = \frac{R_{TOTAL}}{V_{MON\_OV}} \times V_{IT+\_IN2} = \frac{1.65M\Omega}{26.4V} \times 0.4V \approx 24.2k\Omega \quad (5)$$

Take the value of R_3 into Equation 6.

$$R_2 = \left(\frac{R_{TOTAL}}{V_{MON\_UV}} \times V_{IT-\_IN1} \right) - R_3$$
$$= \frac{1.65M\Omega}{21.6V} \times 0.4V - 24.2k\Omega \approx 3k\Omega \quad (6)$$

Calculate R_1 using Equation 7.

$$R_1 = R_{TOTAL} - R_3 - R_2$$
$$= 1.65M\Omega - 24.2k\Omega - 3k\Omega \approx 1.5M\Omega \quad (7)$$

The four extreme scenarios for minimum/maximum UV and OV thresholds are calculated below.

APPLICATION INFORMATION (continued)

Minimum/maximum over-voltage threshold:

$$V_{MON\_OV\_MIN} = 0.4V \times (1-1.2\%) \times \left(1+\frac{R_1 \times (1-0.1\%) + R_2 \times (1-0.1\%)}{R_3 \times (1+0.1\%)}\right) = 24.89 > 24.48V \quad (8)$$

$$V_{MON\_OV\_MAX} = 0.4V \times (1+1.2\%) \times \left(1+\frac{R_1 \times (1+0.1\%) + R_2 \times (1+0.1\%)}{R_3 \times (1-0.1\%)}\right) = 25.59V < 26.4V \quad (9)$$

The maximum and minimum over-voltage threshold values lie within the 24.48V to 26.4V range specified.

Minimum/maximum under-voltage threshold:

$$V_{MON\_UV\_MIN} = 0.4V \times (1-1.2\%) \times \left(1+\frac{R_1 \times (1-0.1\%)}{R_2 (1+0.1\%) + R_3 (1+0.1\%)}\right) = 22.13 > 21.6V \quad (10)$$

$$V_{MON\_UV\_MAX} = 0.4V \times (1+1.2\%) \times \left(1+\frac{R_1 \times (1+0.1\%)}{R_2 \times (1-0.1\%) + R_3 \times (1-0.1\%)}\right) = 22.76V < 23.52V \quad (11)$$

The values stay within the under-voltage range, and all four worst-case scenarios pass the tolerance check, confirming the design approach as valid.

If the reset outputs enter High-Z state, the nRESETx node rising time depends on the pull-up resistance and node capacitance. It is recommended to select a 100kΩ resistor for low-capacitive loads.

Application Curve

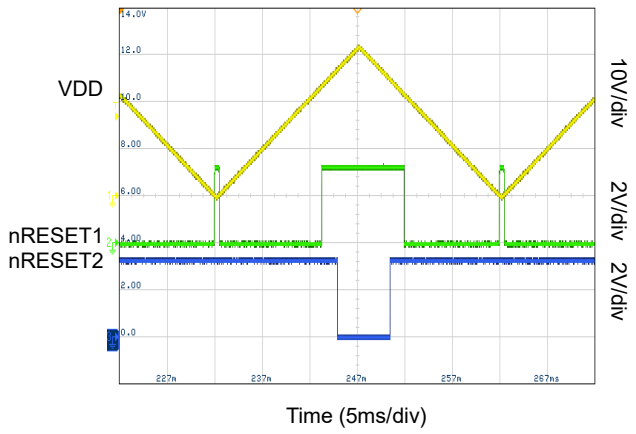


Figure 11. 24V Window Monitor Output Response of SGM882BA

Power Supply Recommendations

The VDD pin of the SGM882 has an absolute maximum voltage rating of 45V, with a recommended operating range up to 36V. In applications where the supply is subject to large transients exceeding 40V or the slew rate is greater than 1V/μs, additional protection is recommended. A series RC filter, consisting of a 100Ω resistor and a 0.1μF capacitor, should be installed between the power supply and VDD pin to suppress high-frequency disturbances, as shown in Figure 12.

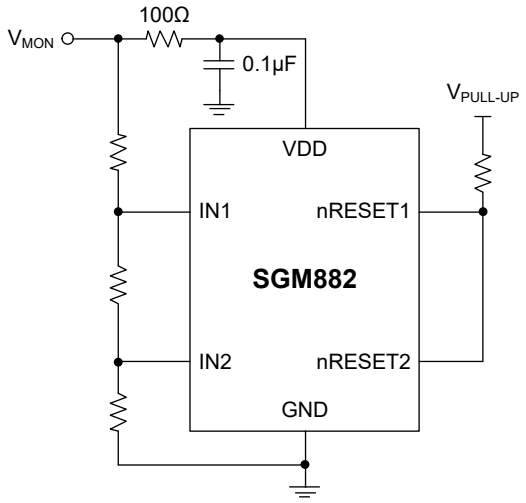


Figure 12. Filtering High-Frequency Disturbances on VDD by Using an RC Filter

Layout Guidelines

Place the external resistors network close to the device to mitigate noise effect.

Place the VDD capacitor as close to the VDD pin as possible.

Keep the VDD traces short to avoid LC resonance from the decoupling capacitor and parasitic inductance of the trace. If long traces are unavoidable, refer to Figure 12 for a VDD filtering example.

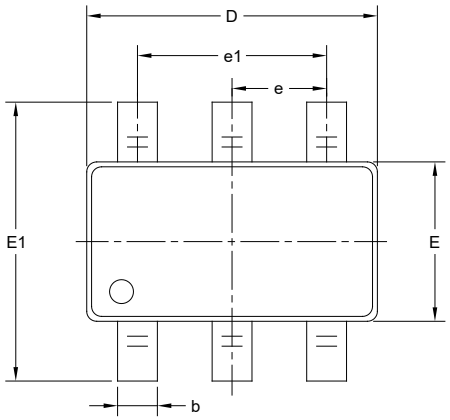
REVISION HISTORY

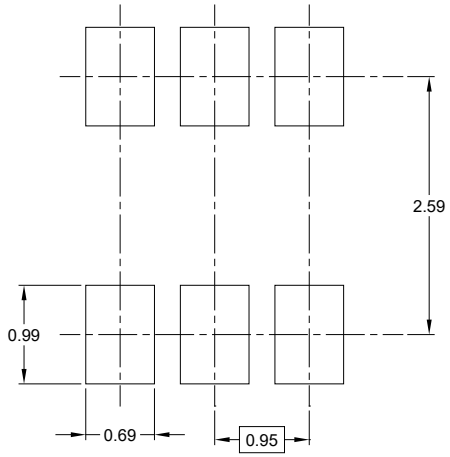
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original to REV.A (DECEMBER 2025)	Page
Changed from product preview to production data	All

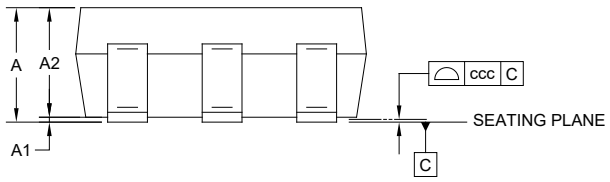
PACKAGE OUTLINE DIMENSIONS

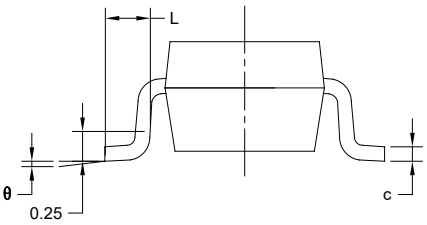
SOT-23-6





RECOMMENDED LAND PATTERN (Unit: mm)



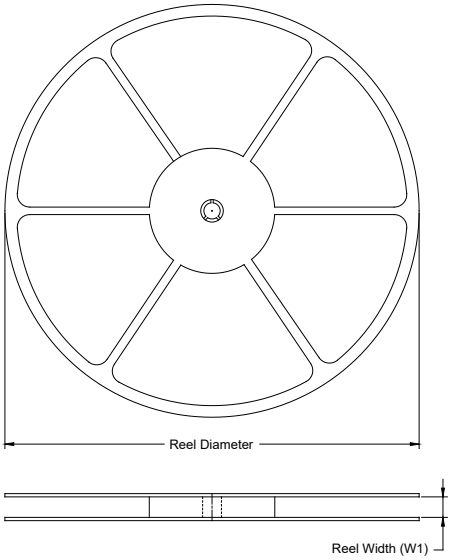


Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	-	-	1.450
A1	0.000	-	0.150
A2	0.900	-	1.300
b	0.300	-	0.500
c	0.080	-	0.220
D	2.750	-	3.050
E	1.450	-	1.750
E1	2.600	-	3.000
e	0.950 BSC		
e1	1.900 BSC		
L	0.300	-	0.600
θ	0°	-	8°
ccc	0.100		

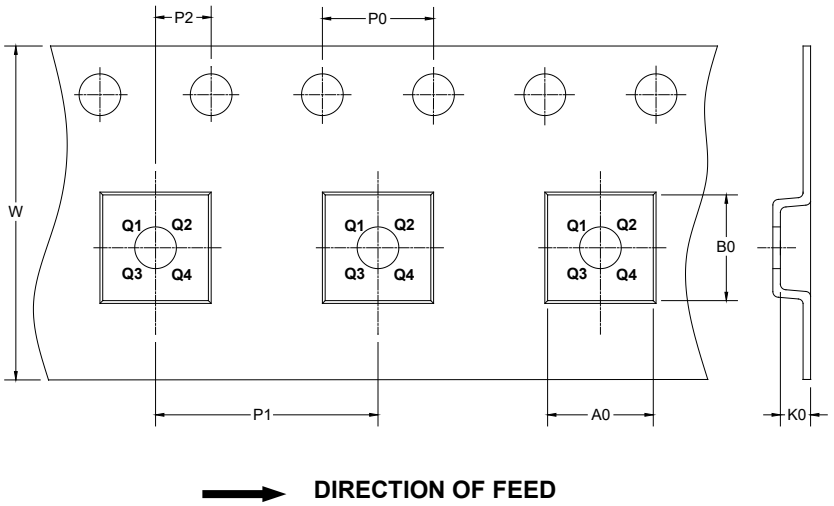
NOTES:
1. This drawing is subject to change without notice.
2. The dimensions do not include mold flashes, protrusions or gate burrs.
3. Reference JEDEC MO-178.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



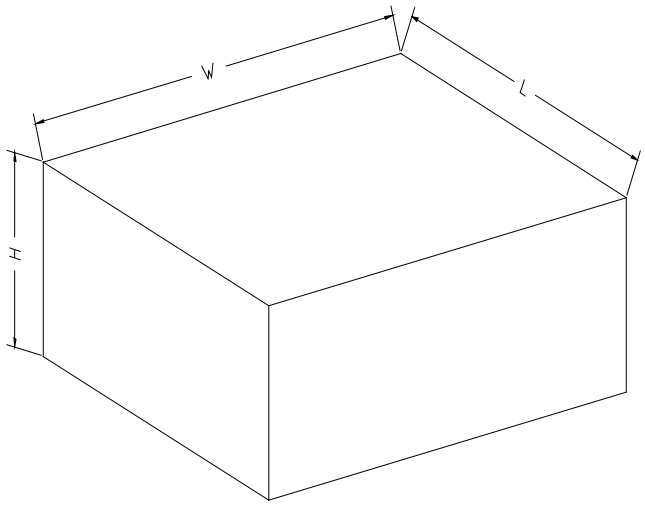
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
SOT-23-6	7″	9.5	3.23	3.17	1.37	4.0	4.0	2.0	8.0	Q3

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18

DD0002