

GENERAL DESCRIPTION

The SGM61223C is a synchronous Buck converter with a wide input voltage range of 4.5V to 28V. This device can deliver up to 2A to the output over a wide input voltage. It is an easy-to-use device with power switches integrated in a small 6-pin package. A typical 3ms soft-start ramp is also included to minimize the inrush current.

This device employs cycle-by-cycle current limit, output over-voltage protection and thermal shutdown with auto recovery. Auto recovery after over-current, output short, overheating or over-voltage fault maintains the system operational with no shutdown.

This converter has a pseudo-fixed 710kHz switching frequency. However, the actual frequency drops during PSM (pulse skip mode) to maximize efficiency at light load.

The SGM61223C is available in a Green TSOT-23-6 package.

FEATURES

- Wide 4.5V to 28V Input Voltage Range
- 2A Continuous Output Current
- Integrated 130mΩ/65mΩ Power MOSFETs
- Low Quiescent Current: 44μA (TYP)
- Shutdown Current: 2.3μA (TYP)
- 3ms Internal Soft-Start Time
- Pseudo-Fixed 710kHz Switching Frequency
- Power Save Mode
- 0.598V to 7V Output Voltage Range
- Adaptive Constant-On-Time Mode Control
- Support 4.7μH and 2.2μH Inductor
- Internal Loop Compensation
- Cycle-By-Cycle Over-Current Limit
- Hiccup Mode for Under-Voltage Protection
- Output Over-Voltage Protection
- Adjustable Input Under-Voltage Lockout
- Thermal Shutdown with Auto Recovery
- Available in a Green TSOT-23-6 Package

APPLICATIONS

12V Distributed Power Supply Buses
Industrial and Consumer Applications
White Goods
Audio Equipment
Set Top Boxes
Digital Television Printers

TYPICAL APPLICATION

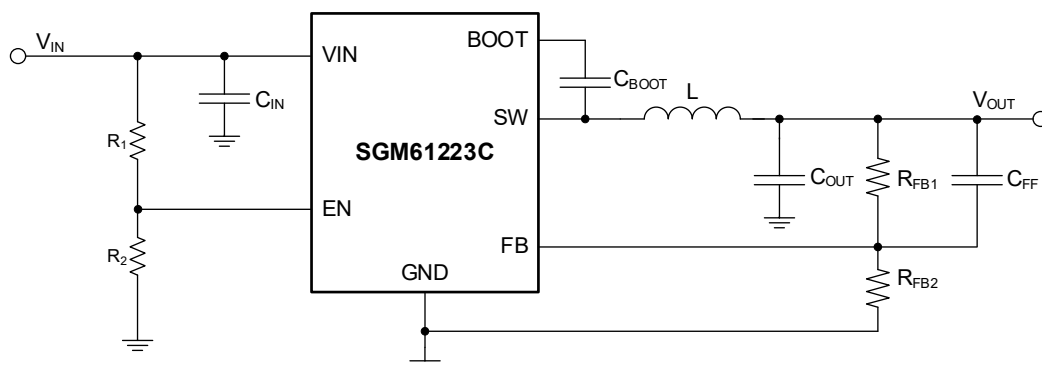


Figure 1. Typical Application Circuit

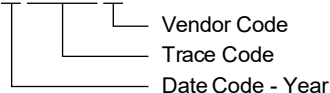
PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM61223C	TSOT-23-6	-40°C to +125°C	SGM61223CXTN6G/TR	18Q XXXXX	Tape and Reel, 3000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.

XXXXX



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Input Voltage Range	-0.3V to 30V
EN and BOOT-SW Voltages.....	-0.3V to 6V
SW Voltage	-0.3V to 30V
SW (20ns Transient) Voltage.....	-5V to 30V
FB Voltage.....	-0.3V to 5V
Package Thermal Resistance	
TSOT-23-6, θ_{JA}	102.4°C/W
TSOT-23-6, θ_{JB}	24.5°C/W
TSOT-23-6, θ_{JC}	59.5°C/W
Junction Temperature	+150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 10s)	+260°C
ESD Susceptibility ^{(1) (2)}	
HBM.....	±5000V
CDM.....	±1500V

NOTES:

1. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.
2. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

RECOMMENDED OPERATING CONDITIONS

Input Voltage Range	4.5V to 28V
Operating Junction Temperature Range	-40°C to +125°C

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

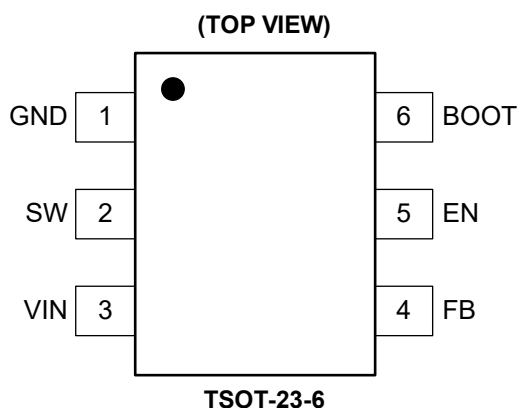
ESD SENSITIVITY CAUTION

This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION



PIN DESCRIPTION

PIN	NAME	TYPE	FUNCTION
1	GND	G	Device Ground Reference Pin.
2	SW	O	Switching Node. Connection point of the internal converter lower and upper power MOSFETs. Connect this pin to the output inductor and the bootstrap capacitor.
3	VIN	P	Input Supply Voltage Pin. VIN powers the internal control circuitry and the power converter. Decouple this pin for very high frequency and high di/dt transitions, with small and high frequency ceramic capacitors placed as close as possible between VIN and GND pins. Input under-voltage is protected by a UVLO comparator.
4	FB	I/O	Feedback (Sense) Pin for Output Voltage and Programming. Tap an output feedback resistor divider to this pin.
5	EN	I	Device Enable Pin. Device will operate if EN voltage is high and will shut down if it is low. Device will be disabled if this pin is left floating.
6	BOOT	O	Bootstrap Pin. Place a 0.1μF capacitor (C_{BOOT}) between BOOT and SW pins close to the device to provide the required drive voltage for the high-side switch.

NOTE: O = output, I = input, I/O = input or output, P = power, G = ground.

ELECTRICAL CHARACTERISTICS

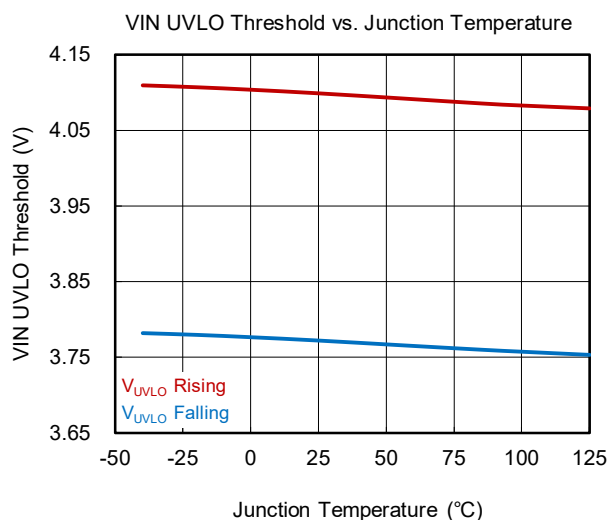
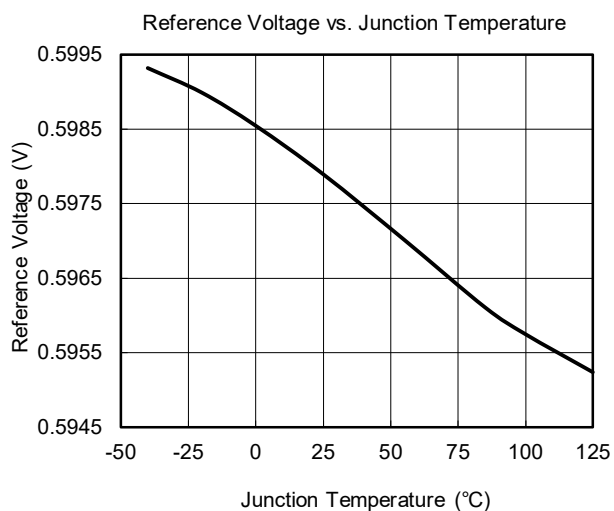
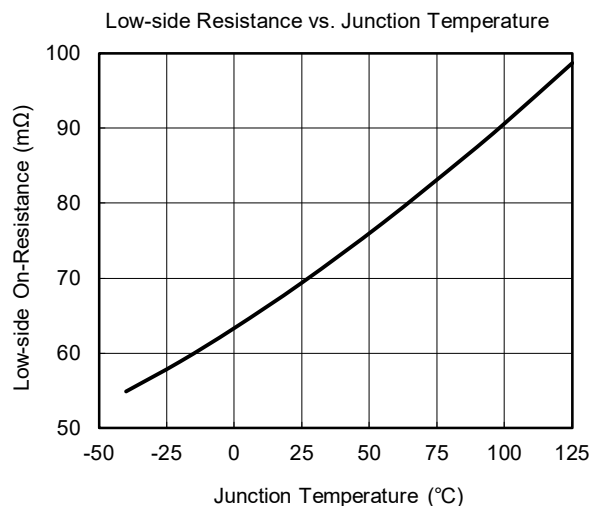
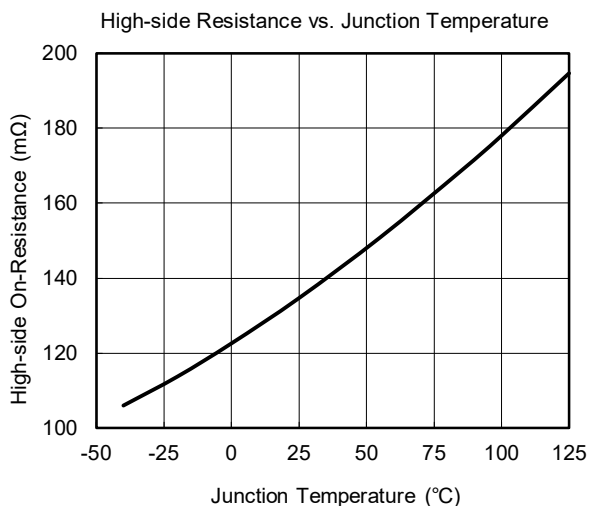
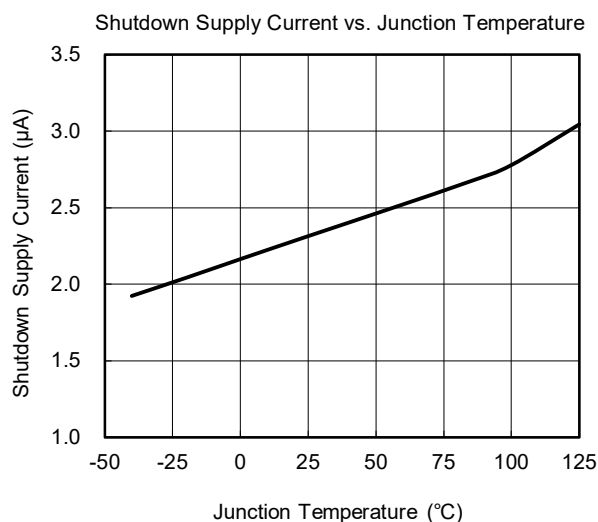
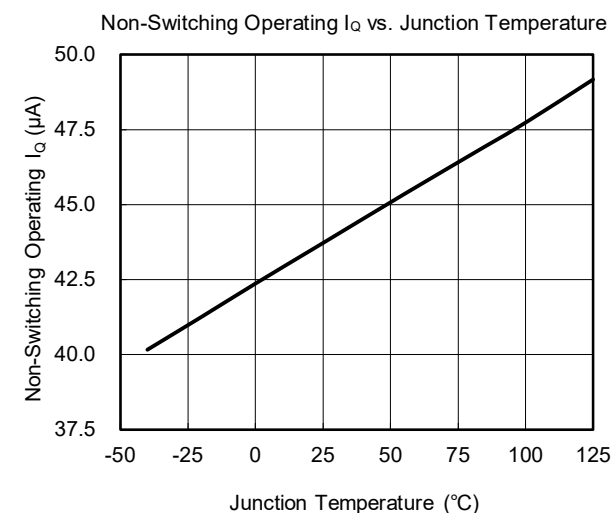
(V_{IN} = 4.5V to 28V, T_J = -40°C to +125°C, typical values are at T_J = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Voltage Range	V _{IN}		4.5		28	V
Non-Switching Quiescent Current	I _Q	V _{IN} = 12V, V _{EN} = 5V, V _{FB} = 1V		44		μA
Shutdown Supply Current	I _{SD}	V _{IN} = 12V, EN = GND		2.3		μA
EN Terminal Input Threshold	V _{IH}	Rising		1.19	1.29	V
	V _{IL}	Falling	1.05	1.15		
EN Terminal Hysteresis Current	I _{EN_HYS}	V _{IN} = 12V, V _{EN} = 1.5V		1.2		μA
EN Internal Pull-Down Resistance	R _{EN_PD}	V _{IN} = 12V		1		MΩ
Feedback						
Feedback Voltage	V _{FB}	V _{IN} = 12V, T _J = +25°C	0.586	0.598	0.610	V
Power Stage						
High-side FET On-Resistance	R _{DSON_HS}	V _{IN} = 12V, V _{BOOT} - V _{SW} = 5V		130	200	mΩ
Low-side FET On-Resistance	R _{DSON_LS}	V _{IN} = 12V		65	100	mΩ
Current Limit						
Low-side Current Limit	I _{LIM_LS}	V _{IN} = 12V, T _J = +25°C, maximum inductor valley current	2.2	2.8	3.5	A
Input Under-Voltage Lockout						
UVLO Threshold Voltage	V _{UVLO}	Rising V _{IN}		4.1	4.5	V
		Falling V _{IN}	3.4	3.77		
UVLO Hysteresis	V _{UVLO_HYS}			330		mV
Over-Temperature Protection						
Thermal Shutdown	T _{SHDN}	Rising temperature		150		°C
Thermal Shutdown Hysteresis	T _{HYS}			20		°C
Oscillator						
Switching Frequency	f _{SW}	V _{IN} = 12V, V _{OUT} = 5V, I _{OUT} = 1A, T _J = +25°C	550	710	870	kHz
Timing Requirements						
Soft-Start Time	t _{SS}			3		ms
On-Time Timer Control						
Minimum Off-Time ⁽¹⁾	t _{OFF_MIN}			180		ns
Output Under-Voltage and Over-Voltage Protection						
Output OVP Threshold	V _{OVP}	OVP detect		108% × V _{REF}		V
Output UVP Threshold	V _{UVP}	Hiccup detect		65% × V _{REF}		V
Hiccup Wait Time	t _{HICCUP_ON}			512		cycles
Hiccup Time before Restart	t _{HICCUP_OFF}			30		ms

NOTE: 1. Guaranteed by design.

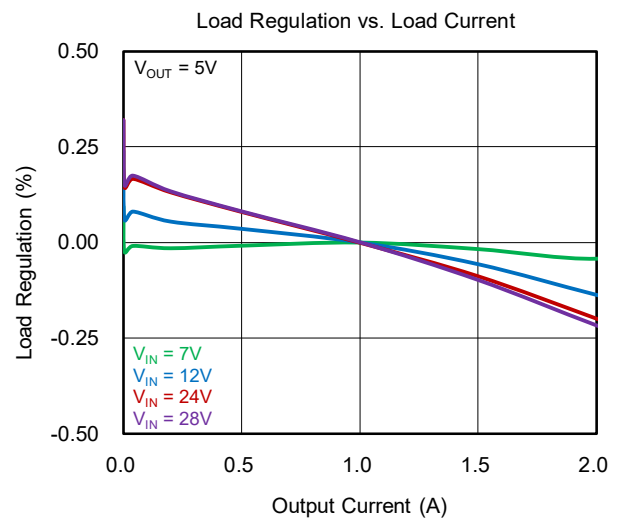
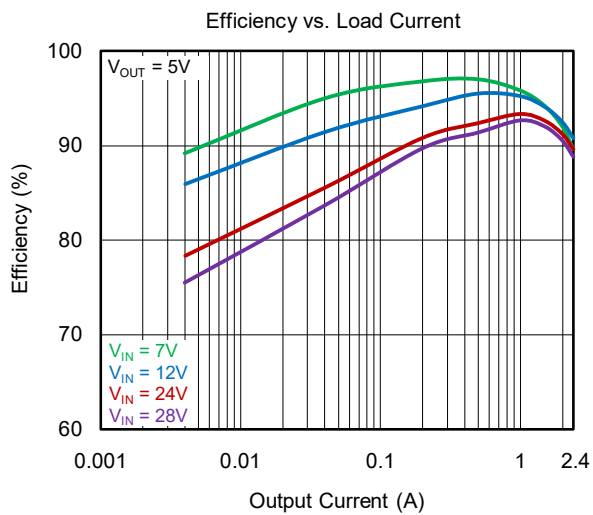
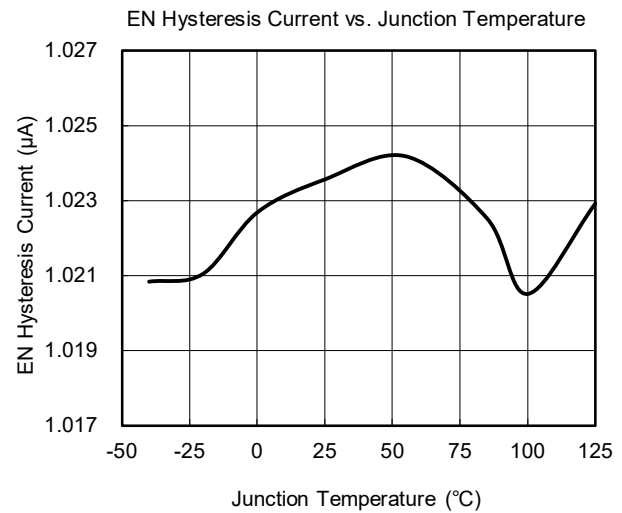
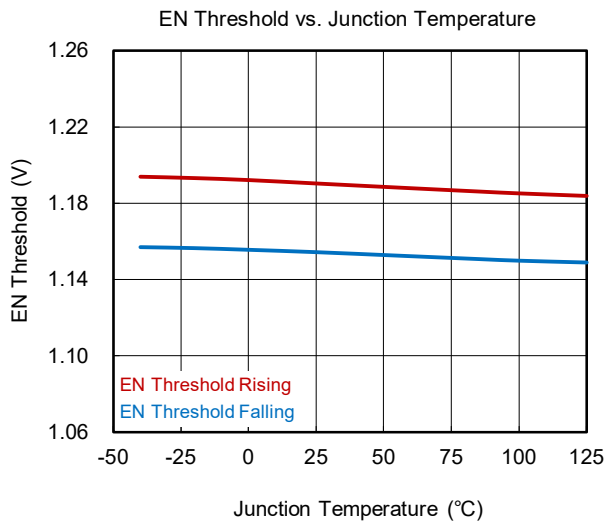
TYPICAL PERFORMANCE CHARACTERISTICS

$V_{IN} = 12V$, $V_{OUT} = 5V$, $f_{SW} = 710kHz$, $L = 6.8\mu H$, $C_{OUT} = 94\mu F$, $T_A = +25^\circ C$, unless otherwise noted.

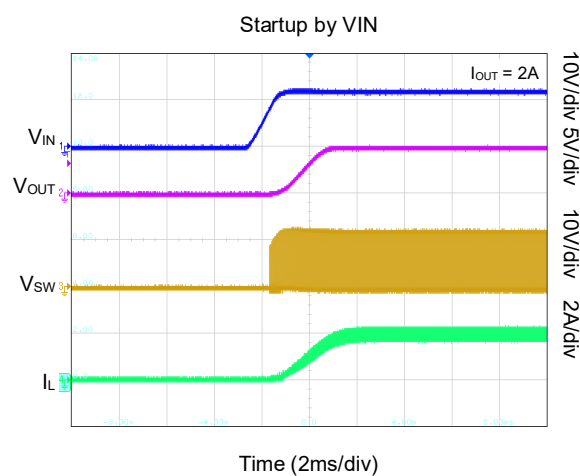
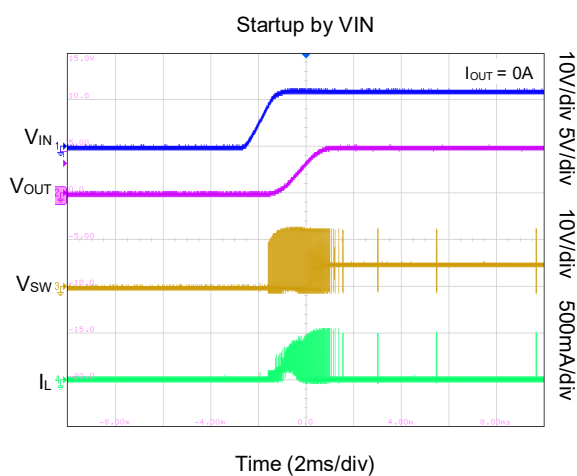
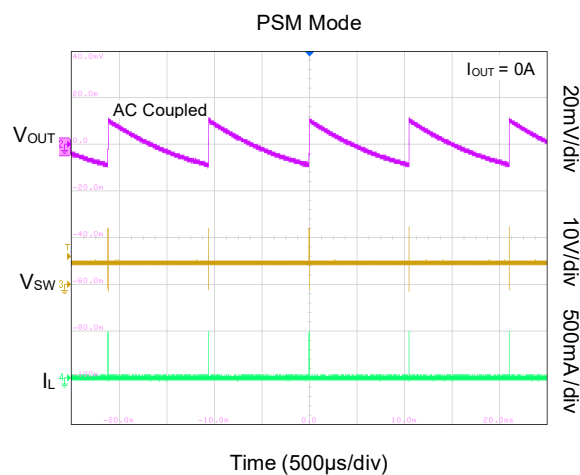
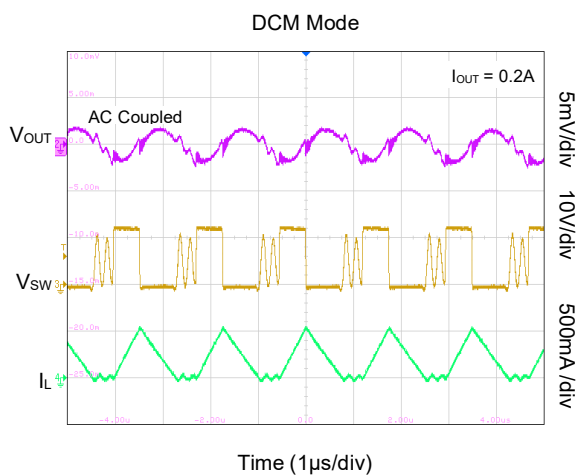
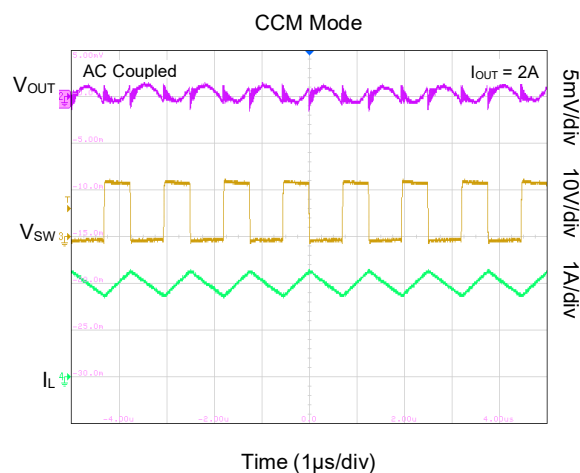
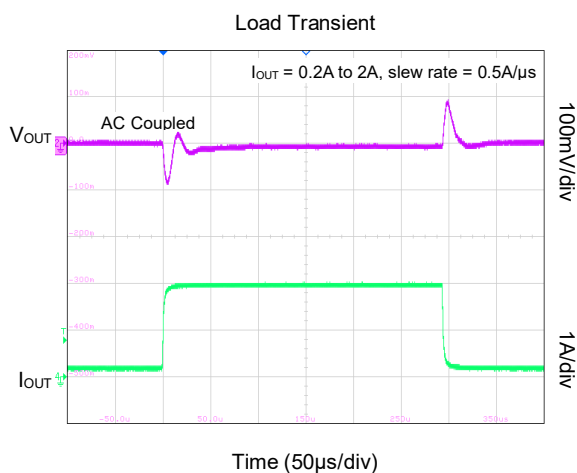


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

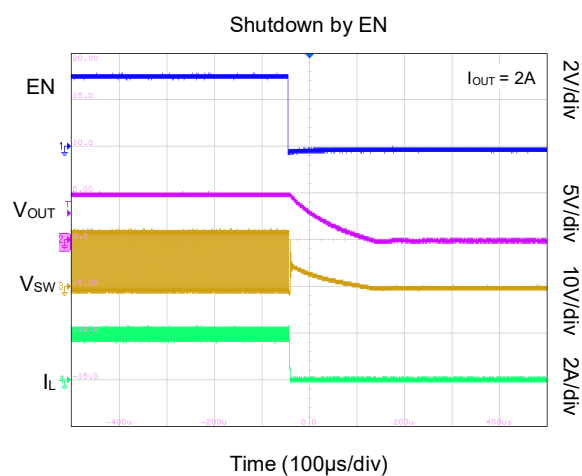
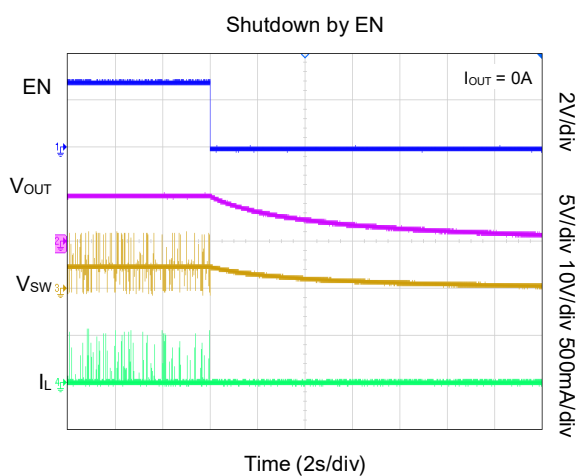
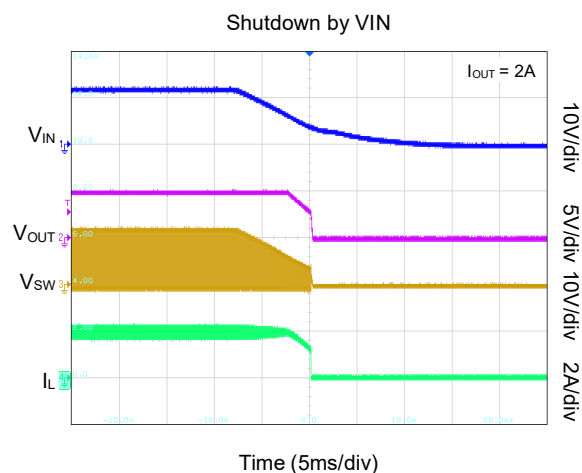
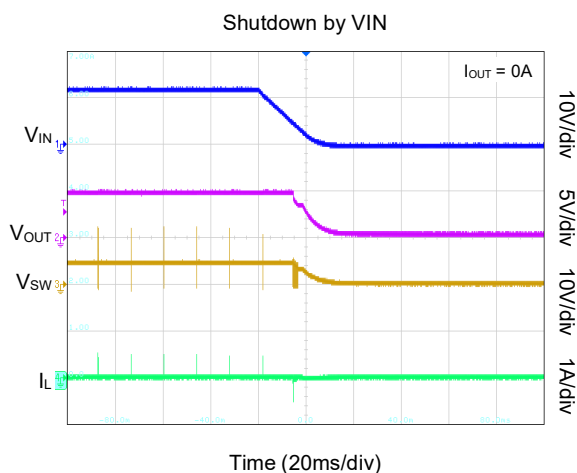
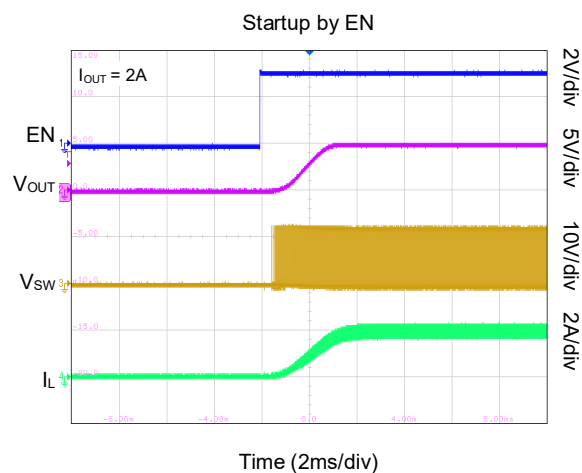
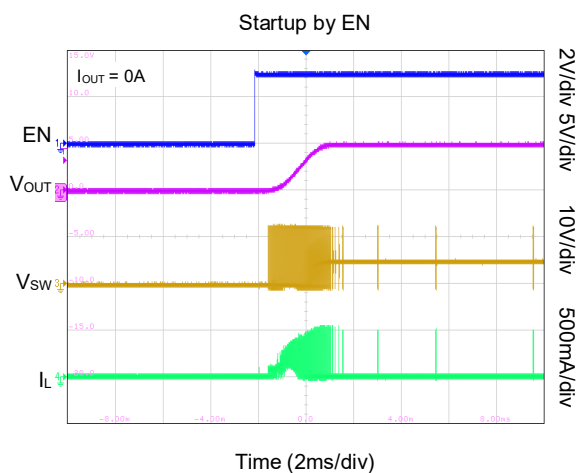
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TYPICAL PERFORMANCE CHARACTERISTICS (continued)

 $V_{IN} = 12V$ and $V_{OUT} = 5V$, unless otherwise noted.

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 $V_{IN} = 12V$ and $V_{OUT} = 5V$, unless otherwise noted.

FUNCTIONAL BLOCK DIAGRAM

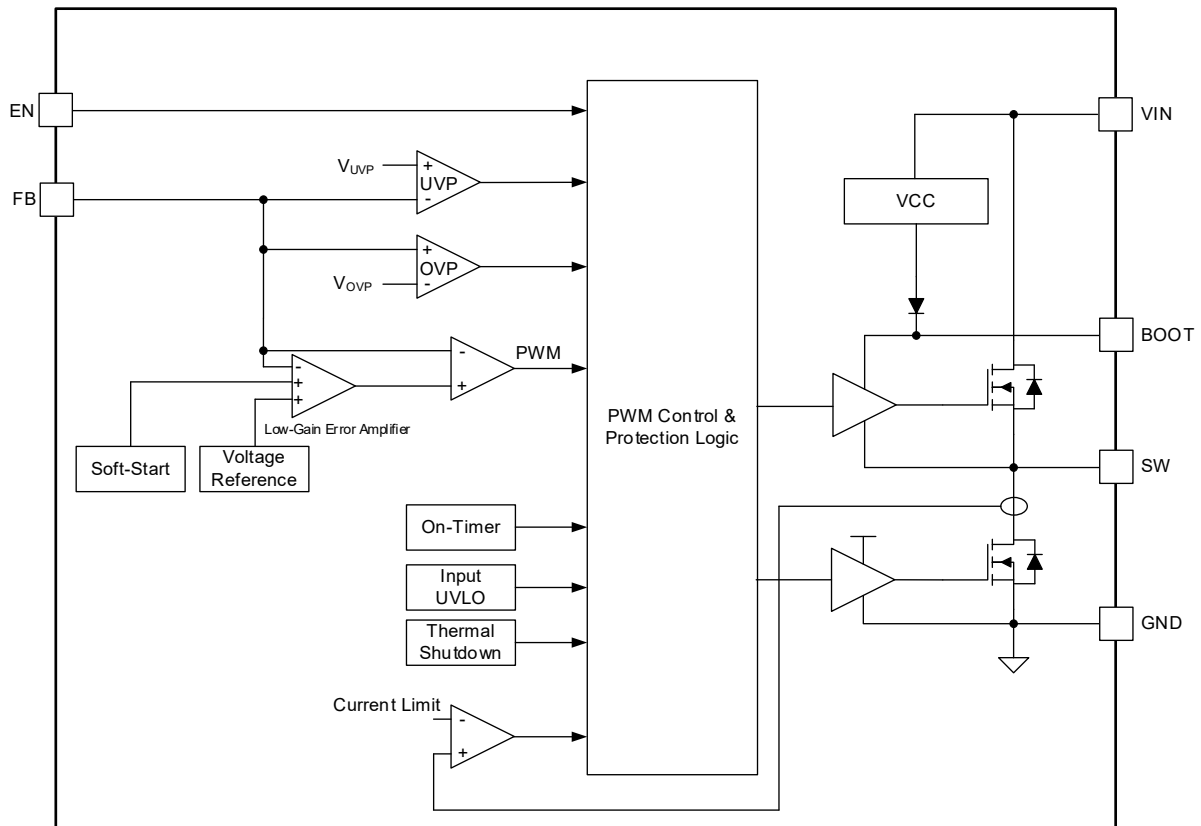


Figure 2. Block Diagram

DETAILED DESCRIPTION

Overview

The SGM61223C is a 28V, 2A synchronous Buck converter with over-current, short-circuit and thermal shutdown with auto recovery. Figure 2 shows the simplified block diagram of the SGM61223C. The two integrated MOSFET switches of the power stage (130mΩ high-side and 65mΩ low-side) can provide up to 2A of continuous current with high efficiency.

The device is powered up when V_{IN} exceeds the UVLO threshold (4.1V TYP). At light load condition, the SGM61223C enters in pulse-skip mode (PSM) to improve efficiency. At no load and with no switching, the typical operating current of SGM61223C is 44μA (TYP) and when the device is disabled by EN pin, it is only 2.3μA (TYP). The internal ripple injection minimizes the BOM cost and simplifies the design. The inrush current is also limited by an internal 3ms soft-start ramp.

Adaptive Constant On-Time Control

In conventional voltage mode control (VMC) or current mode control (CMC) converters, a fixed frequency clock timing signal generates a saw-tooth ramp that is compared with the compensation network output to adjust the PWM duty cycle (on-time) as control variable and regulate the output voltage and/or current feedback(s) to govern the control variable and keep the output regulated with fast reaction to load or V_{IN} variations. The existence of the compensator in VMC or CMC converter inherently introduces some delay in the loop response.

The adaptive constant on-time (ACOT) control differs from voltage mode control (VMC) or current mode control (CMC) in that it operates without clock signal and instead uses hysteretic mode control. At the start of each switching cycle, the ACOT control generates a relatively constant on-time pulse when the internal comparator detects that the output voltage has dropped below the desired level. The feedback (FB) pin senses the output voltage through a resistor divider and compares it to the internal reference voltage (V_{REF}) using a low-gain error amplifier. The amplifier output is then sent to a comparator. When the feedback voltage (V_{FB}) falls below the amplifier output, the on-time control logic is triggered which turns on the high-side switch. ACOT control can dynamically adjust the on-time duration based on the input and output voltage, achieving a relatively constant frequency during steady-state operation and minimizing electromagnetic interference at certain frequencies. Additionally, an internal ramp is added to the reference voltage to

simulate output ripple, allowing for use with low equivalent series resistance (ESR) output capacitors.

Enable Pin and UVLO Adjustment

The EN pin can be used to turn the device on and off or to change the UVLO thresholds. The device is enabled when the EN pin voltage exceeds its high threshold (1.19V TYP). A low EN voltage disables the device which brings it to the low-quiescent (I_Q) state.

The EN pin is internally pulled down by a resistor (1MΩ TYP), so the device is disabled if EN pin is floated. A Zener diode is used to clamp the EN input voltage (5.5V TYP) and the Zener diode is not allowed to go through large current (1mA MAX). SGM61223C also allows EN to connect to V_{IN} by only a pull-up resistor R_1 (typical 510kΩ). R_1 is not allowed smaller than 30kΩ. R_1 must also not be a too large resistor to avoid EN not being able to turn on. So R_1 range is 30kΩ to 2.7MΩ.

V_{IN} is monitored by the internal under-voltage lockout circuit and if it is below UVLO threshold, the device is disabled. The internal UVLO has a 330mV hysteresis. If higher thresholds are needed, EN pin can be used as shown in Figure 3.

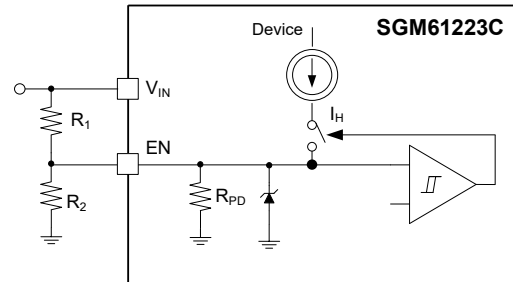


Figure 3. Adjustable V_{IN} Under-Voltage Lockout

The EN pull-up current is used to set the hysteresis. The pull-up current is increased by I_H when the EN pin exceeds its high threshold. Use Equations 1 and 2 to calculate the R_1 and R_2 values for the desired UVLO low (V_{UV_L}) and high (V_{UV_H}) thresholds.

$$R_1 = \frac{V_{UV_H} - V_{IH}}{V_{IH}} \times \frac{V_{UV_H} \times V_{IL} - V_{UV_L} \times V_{IH}}{I_H \times V_{UV_H}} \quad (1)$$

$$R_2 = \frac{R_{PD} \times (V_{UV_H} \times V_{IL} - V_{UV_L} \times V_{IH})}{R_{PD} \times I_H \times V_{UV_H} + V_{UV_L} \times V_{IH} - V_{UV_H} \times V_{IL}} \quad (2)$$

where:

$I_H = 1.2\mu A$ (TYP)

$V_{IL} = 1.15V$ (TYP)

$V_{IH} = 1.19V$ (TYP)

DETAILED DESCRIPTION (continued)**Bootstrap Voltage (BOOT)**

To power the upper switch gate driver, a voltage higher than V_{IN} is needed. Bootstrap technique is used to provide this voltage from the switching node by using a $0.1\mu\text{F}$ bootstrap capacitor between SW and BOOT pins along with an internal bootstrap diode. The voltage is internally regulated for driving the high-side switch. An X5R or X7R ceramic capacitor is recommended for C_{BOOT} to have stable capacitance against temperature and voltage variations.

Output Voltage Programming

Output voltage of the SGM61223C is set by a resistor divider between V_{OUT} and GND that is tapped to the FB pin. It is recommended to use 1% or higher quality resistors with low thermal tolerance for an accurate and thermally stable output voltage.

Use Equation 3 and Figure 4 to calculate the output voltage. Lower divider resistor values increase loss and reduce light load efficiency. Consider larger resistors to improve efficiency at light load, and start with $100\text{k}\Omega$ for the upper resistor (R_{FB1}). Note that if R_{FB1} is too high ($> 1\text{M}\Omega$), the FB pin leakage current and other noises can easily affect the accuracy and performance of the regulator.

$$V_{OUT} = V_{REF} \times \left[\frac{R_{FB1}}{R_{FB2}} + 1 \right] \quad (3)$$

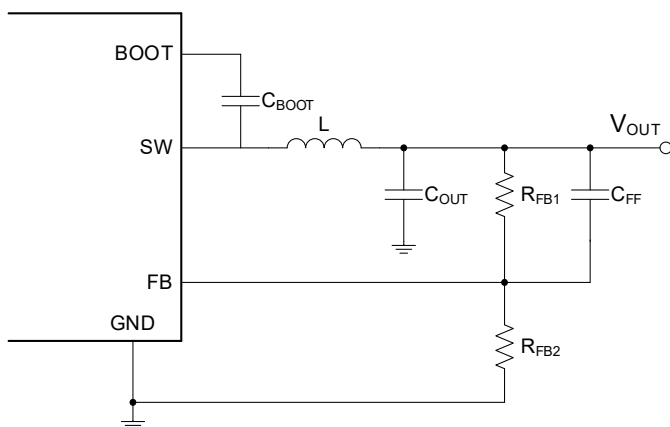


Figure 4. Adjustable Output Voltage

Internal Voltage Reference and Soft-Start

The SGM61223C device has an internal 0.598V reference (V_{REF}) to program the output at the desired level. When the converter starts (or is enabled), an internal ramp voltage begins to rise from near 0V to slightly above 0.598V with a ramp time of 3ms . The lower of V_{REF} and this ramp is used as reference for the error amplifier, therefore, during startup the ramp provides a soft-start for the output. The soft-start is essential to prevent high inrush currents caused by rapid increase of output voltage across output capacitors and the load.

Over-Current and Short-Circuit Protection

The SGM61223C supports overload mode. When the output current continues to overload during the system power-up, the SGM61223C exports the maximize power and limits the maximum valley current of the low-side FET switch. The device keeps in cycle-by-cycle limit to meet the system's power request. The SGM61223C does not shut down until the device heats and then goes to thermal shutdown. As the load increases continuously, the output voltage decreases. If the output voltage drops to 65% of V_{REF} and the current of the low-side switch is higher than the low-side current limit for 512 consecutive cycles, the hiccup current-protection mode will be activated. In hiccup mode, the regulator is shut down and kept off for 30ms typically before the SGM61223C tries to start again. If over-current or a short-circuit fault condition still exists, the hiccup mode will repeat until the fault condition is removed. Hiccup mode can help to reduce power dissipation and prevent overheating and potential damage to the device.

Output Over-Voltage Protection (OVP)

An over-voltage protection is included in the device to minimize the output voltage overshoots that may occur after recovery from an output fault or a large unloading transient. The FB pin voltage is compared with the OVP thresholds. If the V_{FB} exceeds 108% of the V_{REF} , the high-side switch is forced to turn off, and the low-side switch is turned on until zero cross current limit is triggered. When the V_{FB} falls below 104% of the V_{REF} , the high-side switch is allowed to turn on again.

DETAILED DESCRIPTION (continued)**Light Load Operation with Pulse-Skip Mode**

When SGM61223C operates in discontinuous conduction mode (DCM) with light loads, it goes into the pulse-skip mode (PSM) in which internal power dissipation is significantly reduced. Moreover, the operating frequency starts to drop depending on the load. At very light load and when the off-time exceeds $18\mu\text{s}$, device goes to the sleep mode to lower internal dissipation.

The details are explained in Figure 5 that shows the timings of the ACOT control in DCM. Inductor current (I_L) is monitored with a zero-crossing detector and when I_L crosses the zero and $V_{FB} > V_{REF_EA}$ (the output of the low-gain error amplifier), both high-side and low-side MOSFETs are turned off. They will not be turned on again until the V_{FB} falls below V_{REF_EA} and triggers a new on-time pulse. During this off-time period, all non-essential circuits are shut down to minimize losses and the load is supplied by the output capacitor stored energy. The control circuitry wakes up when the new on-pulse is triggered. When t_1 is longer than $18\mu\text{s}$, the device goes into sleep mode in which the system current dissipation is only about $44\mu\text{A}$.

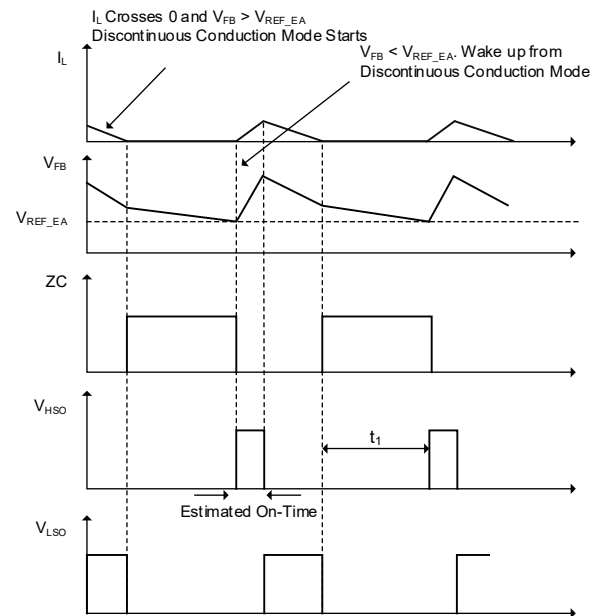


Figure 5. Pulse-Skip Mode in DCM

Thermal Shutdown

If the junction temperature exceeds $+150^{\circ}\text{C}$ (TYP), the device is forced to stop switching. It will recover automatically when T_J falls below the recovery threshold.

APPLICATION INFORMATION

The design method and component selection for the SGM61223C Buck converter is explained in this section. Schematic of a basic design is shown in Figure 6. Only a few external components are needed to provide a constant output voltage from a wide input voltage range.

The external components are designed based on the application requirements and device stability. Some suitable output filters (L and C_{OUT}) along with C_{FF} and divider resistor values are provided in Table 1 to simplify component selection.

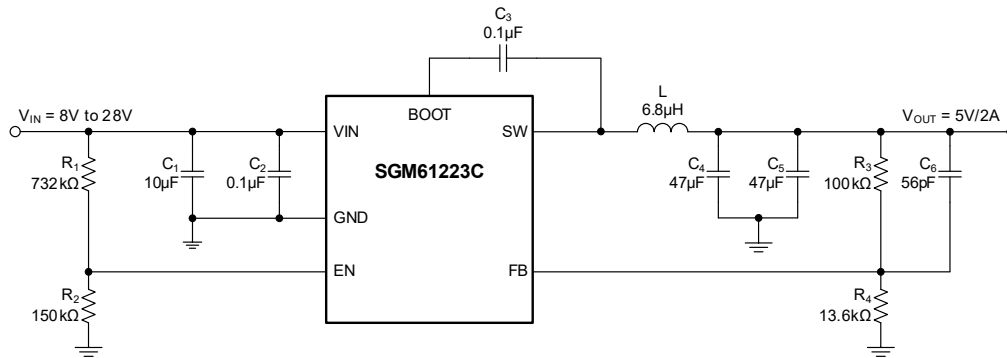


Figure 6. A Reference Design for 5V/2A Application

Table 1. Recommended Component Values

V _{OUT} (V)	L (μH)	C ₄ + C ₅ (μF)	R ₃ (kΩ)	R ₄ (kΩ)	C ₆ (pF)
0.6	1	400	100	--	56
3.3	4.7	94	100	22.1	56
5	6.8	94	100	13.6	56
6.5	10	47	100	10	56

Design Requirements

A typical application circuit for the SGM61223C as a Buck converter is shown in Figure 6. It is used for converting an 8V to 28V supply voltage to a lower voltage level supply voltage (5V) suitable for the system. The design parameters given in Table 2 are used for this design example.

Table 2. Design Parameters

Design Parameters	Example Values
Input Voltage	12V (TYP), 8V to 28V
Start Input Voltage (Rising V _{IN})	8V
Stop Input Voltage (Falling V _{IN})	7V
Input Ripple Voltage	360mV, 3% of V _{IN,TYP}
Output Voltage	5V
Output Voltage Ripple	50mV, 1% of V _{OUT}
Output Current Rating	2A
Transient Response, 0A to 2A Load Step	250mV, 5% of V _{OUT}
Operation Frequency	710kHz

Input Capacitor Selection

A high-quality ceramic capacitor (X5R or X7R or better dielectric grade) must be used for input decoupling of the SGM61223C. At least 3μF of effective capacitance (after de-ratings) is needed on

the VIN input. In some applications, additional bulk capacitance may also be required for the VIN input, for example, when the SGM61223C is more than 5cm away from the input source. The V_{IN} capacitor ripple current rating must also be greater than the maximum input current ripple. The input current ripple can be calculated using Equation 4 and the maximum value occurs at 50% duty cycle. Using the design example values, I_{OUT} = 2A, yields an RMS input ripple current of 1A.

$$I_{CIN_RMS} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \frac{(V_{IN} - V_{OUT})}{V_{IN}}} = I_{OUT} \times \sqrt{D \times (1-D)} \quad (4)$$

For this design, a ceramic capacitor with at least 50V voltage rating is required to support the maximum input voltage. So, a 10μF/50V capacitor is selected for VIN to cover all DC bias, thermal and aging de-ratings. The input capacitance determines the regulator input voltage ripple. This ripple can be calculated from Equation 5. In this example, the total effective capacitance of the 10μF/50V capacitor is around 4μF at 12V input, and the input voltage ripple is 171mV.

$$\Delta V_{IN} = \frac{I_{OUT} \times D \times (1-D)}{C_{IN} \times f_{SW}} \quad (5)$$

It is recommended placing an additional small size 0.1μF ceramic capacitor right beside VIN and GND pins for high frequency filtering.

APPLICATION INFORMATION (continued)

Inductor Selection

Equation 6 is conventionally used to calculate the output inductance of a Buck converter. The ratio of inductor current ripple (ΔI_L) to the maximum output current (I_{OUT}) is represented as K_{IND} factor ($\Delta I_L/I_{OUT}$). The inductor ripple current is bypassed and filtered by the output capacitor and the inductor DC current is passed to the output. Inductor ripple is selected based on a few considerations. The peak inductor current ($I_{OUT} + \Delta I_L/2$) must have a safe margin from the saturation current of the inductor in the worst-case conditions especially if a hard-saturation core type inductor (such as ferrite) is chosen. The ripple current also affects the selection of the output capacitor. C_{OUT} RMS current rating must be higher than the inductor RMS ripple. Typically, a 40% ripple is selected ($K_{IND} = 0.4$).

$$L = \frac{V_{IN_MAX} - V_{OUT}}{I_{OUT} \times K_{IND}} \times \frac{V_{OUT}}{V_{IN_MAX} \times f_{SW}} \quad (6)$$

In this example, the calculated inductance will be $7.23\mu H$ with $K_{IND} = 0.4$, so the nearest inductance of $6.8\mu H$ is selected. The ripple, RMS and peak inductor current calculations are summarized in Equations 7, 8 and 9 respectively.

$$\Delta I_L = \frac{V_{IN_MAX} - V_{OUT}}{L} \times \frac{V_{OUT}}{V_{IN_MAX} \times f_{SW}} \quad (7)$$

$$I_{L_RMS} = \sqrt{I_{OUT}^2 + \frac{\Delta I_L^2}{12}} \quad (8)$$

$$I_{L_PEAK} = I_{OUT} + \frac{\Delta I_L}{2} \quad (9)$$

Note that during startup, load transients or fault conditions, the peak inductor current may exceed the calculated I_{L_PEAK} . Therefore, it is always safer to choose the inductor saturation current higher than the switch current limit.

Output Capacitor Selection

The output capacitors and inductor filter the AC part of the PWM switching voltage and provide an acceptable level of output voltage ripple superimposed on the desired output DC voltage. Additionally, the capacitors store energy to assist in maintaining output voltage regulation during load transient. The output voltage ripple (ΔV_{OUT}) depends on the output capacitor value at the operating voltage, temperature ($^{\circ}C$) and its parasitic parameters (ESR and ESL):

$$\Delta V_{OUT} = \Delta I_L \times ESR + \frac{V_{IN} - V_{OUT}}{L} \times ESL + \frac{\Delta I_L}{8 \times f_{SW} \times C_{OUT}} \quad (10)$$

The voltage rating of the output capacitors should be selected with enough margins to ensure that capacitance drop (voltage and temperature de-rating) is not significant. The type of output capacitors will determine which terms of Equation 10 are dominant. For ceramic output capacitors, the ESR and ESL are virtually zero, so the output voltage ripple will be dominated by the capacitive term.

To reduce the voltage ripple, either inductance or the total capacitance is increased. For electrolytic output capacitors, the value of capacitance is relatively high, and compared with ESR and ESL terms, the third term in Equation 10 can be ignored:

Higher quality capacitors, larger inductance or using parallel capacitors can help reduce the output ripple in a design using electrolytic output capacitors.

The ESR of some commercial electrolytic capacitors can be quite high, and it is recommended using quality capacitors with the ESR or the total impedance clearly documented in the datasheet. ESR of an electrolytic capacitor may increase significantly at cold ambient temperatures with a factor of 10 or so, which increases the ripple and can deteriorate the regulator stability.

The transient response of the regulator also depends on the quantity and type of output capacitors. In general, reducing the ESR of the output capacitance will lead to a better transient response. The ESR can be minimized by simply adding more capacitors in parallel or by using higher quality capacitors. When a fast load transient of magnitude ΔI_L and rate of di/dt occurs, the output voltage will jump or dip by a transient magnitude of ΔV_{OUT} :

$$\Delta V_{OUT} = \Delta I_L \times ESR + \frac{di}{dt} \times ESL \quad (11)$$

Right after the transient, the inductor current remains almost constant especially for larger inductors and the transient current is carried by the capacitor. The output voltage will deviate from its nominal value for a short time depending on the system bandwidth, the inductor and the output capacitance. Eventually, the error amplifier and feedback bring the output voltage back to its nominal value. A higher bandwidth is usually preferred to get shorter settling time, however, it may be more difficult to get acceptable gain and phase margins. In this example, according to Table 1, $2 \times 47\mu F/16V$ X5R ceramic capacitors with $2m\Omega$ of ESR can meet the above conditions.

APPLICATION INFORMATION (continued)**Bootstrap Capacitor Selection**

Use a 0.1μF high-quality ceramic capacitor (X5R or X7R) with 10V or higher voltage rating for the bootstrap capacitor (C₃).

VIN UVLO Setting

The input UVLO can be programmed by using an external voltage divider on the EN pin of the SGM61223C. In this design, R₁ is connected between VIN pin and EN pin and R₂ is connected between EN pin and GND (see Figure 6). The UVLO has two thresholds (hysteresis), one for power-up (turn-on) when the input voltage is rising and one for power-down (turn-off) when the voltage is falling. In this design, the turn-on (enable to start switching) occurs when V_{IN} rises above 8V (UVLO rising threshold). When the regulator is working, it will not stop switching (disabled) until the input falls below 7V (UVLO falling threshold). Equations 1 and 2 are provided to calculate the resistors. For this example, the nearest standard resistor values are R₁ = 732kΩ and R₂ = 150kΩ.

Output Voltage Setting

Use an external resistor divider (R₃ and R₄) to set the output voltage using Equation 12:

$$R_4 = R_3 \times \left(\frac{V_{REF}}{V_{OUT} - V_{REF}} \right) \quad (12)$$

where V_{REF} = 0.598V is the internal reference. For example, by choosing R₃ = 100kΩ, the R₄ value for 5V output will be calculated as 13.6kΩ.

Feed-Forward Capacitor Selection

The SGM61223C contains an internal compensation circuit, an internal ramp is added to reference voltage to simulate output ripple. For ultra-low output capacitance ESR (ceramic capacitor) applications, it is recommended adding a 56pF feed-forward capacitor (C₆) to provide a low-impedance path for output voltage ripple and ensure minimal phase shift of the voltage ripple at the feedback node while maintaining acceptable transient response.

LAYOUT INFORMATION

PCB is an essential element of any switching power supply. The converter operation can be significantly disturbed due to the existence of the large and fast rising/falling voltages that can couple through stray capacitances to other signal paths, and also due to the large and fast changing currents that can interact through parasitic magnetic couplings, unless those interferences are minimized and properly managed in the layout design. Insufficient conductance in copper traces for the high current paths results in high resistive losses in the power paths and voltage errors. The following guidelines provided here are necessary to design a good layout:

- ◆ Bypass VIN pin to GND pin with low-ESR ceramic capacitors (X5R or X7R better dielectric) placed as close as possible to VIN pin.
- ◆ Use short, wide and direct traces for high-current connections (IN, SW and GND).
- ◆ Keep the BOOT-SW voltage path as short as possible.
- ◆ Place the feedback resistors as close as possible to the FB pin that is sensitive to noise.
- ◆ Minimize the area and path length of the loop formed by VIN pin, bypass capacitors connections and SW pin.

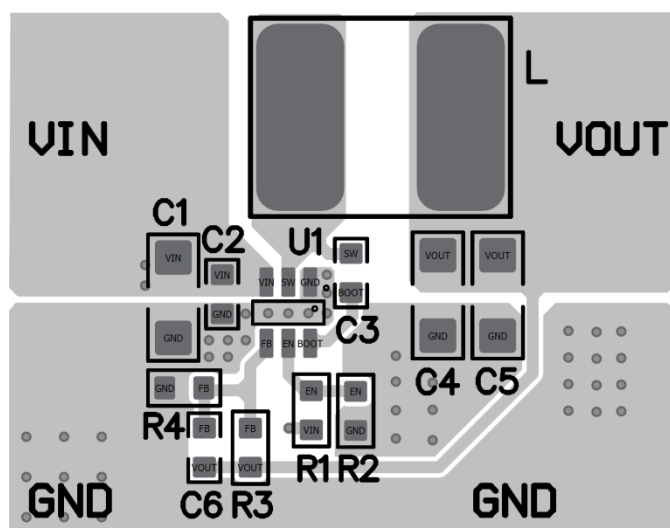


Figure 7. PCB Top Layer

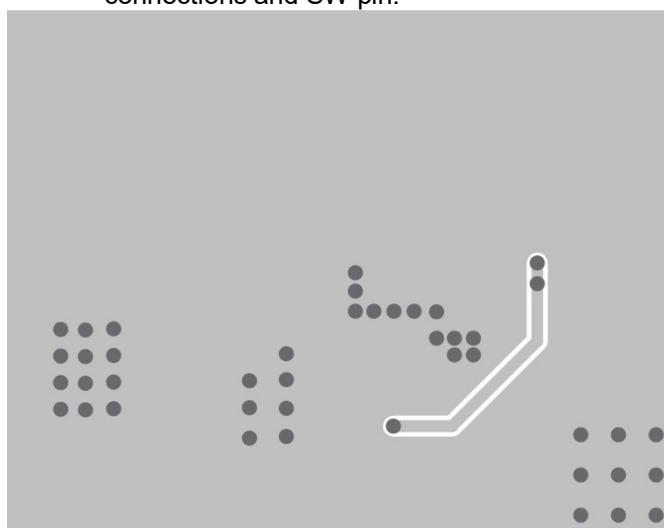


Figure 8. PCB Bottom Layer

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (APRIL 2025) to REV.A

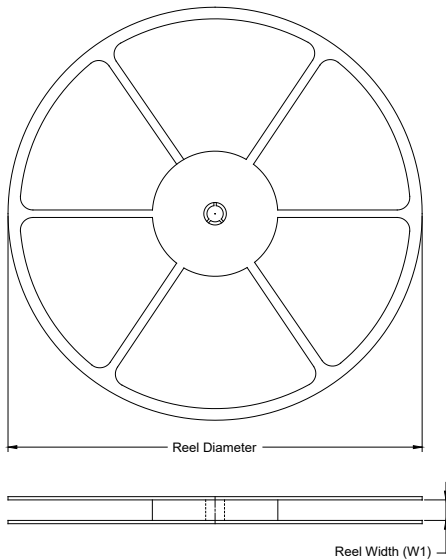
Page

Changed from product preview to production data..... All

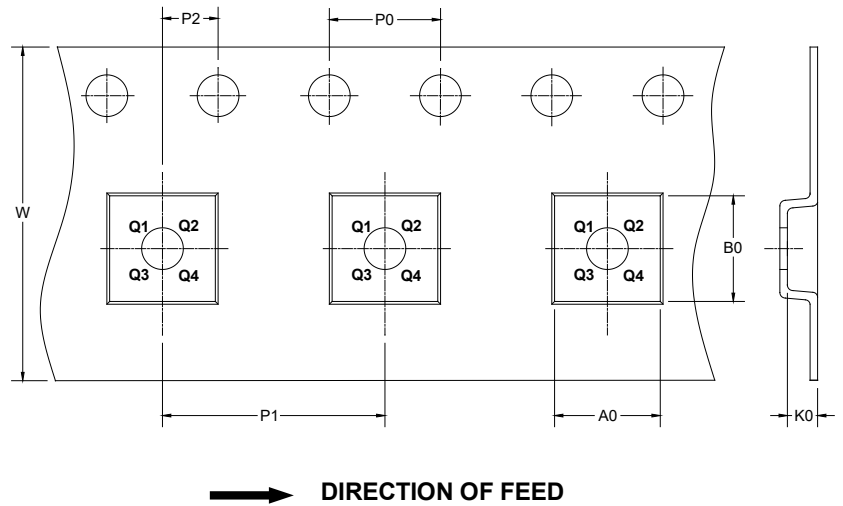
PACKAGE INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

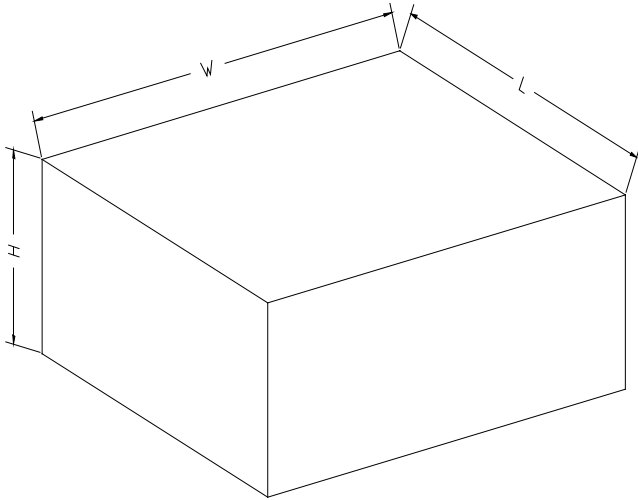
KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TSOT-23-6	7"	9.5	3.20	3.10	1.10	4.0	4.0	2.0	8.0	Q3

DD0001

PACKAGE INFORMATION

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

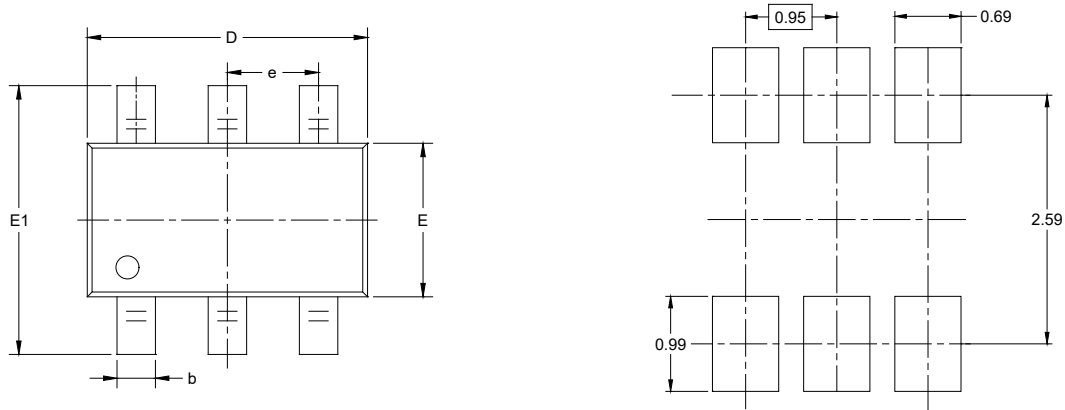
KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7" (Option)	368	227	224	8
7"	442	410	224	18

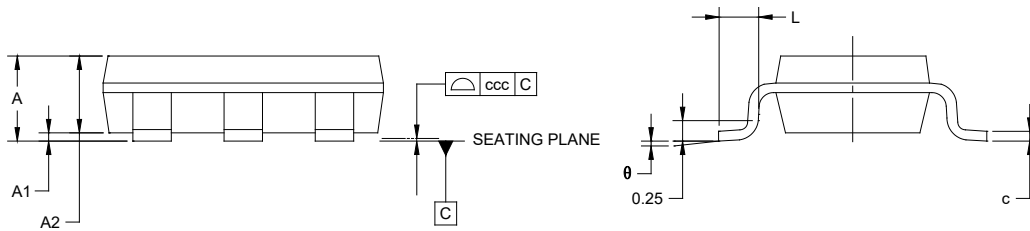
DD0002

PACKAGE OUTLINE DIMENSIONS

TSOT-23-6



RECOMMENDED LAND PATTERN (Unit: mm)



Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	-	-	1.100
A1	0.000	-	0.100
A2	0.700	-	1.000
b	0.300	-	0.500
c	0.080	-	0.200
D	2.750	-	3.050
E	1.450	-	1.750
E1	2.600	-	3.000
e	0.950 BSC		
L	0.300	-	0.600
θ	0°	-	8°
ccc	0.100		

NOTES:

1. This drawing is subject to change without notice.
2. The dimensions do not include mold flashes, protrusions or gate burrs.
3. Reference JEDEC MO-193.