SGM25135
16V, 35A, 1.1mΩ R_{DSON}, Hot-Swap Intelli-Fuse Solution

GENERAL DESCRIPTION

SGM25135 is a hot-plug protection device, which can not only protect its output circuit from input transients, but also protect its input from harmful short circuits and transients from its output.

The device includes an IMON option that generates a voltage proportional to the power supply current through the power supply device, which is set by the resistance of IMON pin to ground. An integrated high-efficiency charge pump drives the gate of the power device, allowing the power FET with an extremely low on-resistance of 1.1mΩ to turn on.

During startup, the surge current is limited by the slew rate at the output. The slew rate is controlled by an external capacitor at the SS pin.

The current of the detection FET topology limits the maximum load at the output. The current limiting amplitude is controlled by a low power resistor from the ILIM pin to the ground.

Full protection features include damaged MOSFET detection, thermal shutdown, current limit, over-voltage protection (OVP), and under-voltage protection (UVP).

The SGM25135 is available in a Green TLGA-3×5-22L package.

APPLICATIONS

Hot-Swap
PC Cards
Disk Drives
Servers
Networking
Laptops

FEATURES

- **Operating Input Voltage Range: 2.7V to 16V**
- **Output Current: 35A (MAX)**
- **Integrated Switch with 1.1mΩ R_{DSON}**
- **IMON Accuracy: -1%/+1.5% at T_J = +25℃, I_{OUT} = 17A**
- **VIN/VOUT/Temperature Monitor**
- **Built-In MOSFET Driver**
- **3.3V LDO Output**
- **PG Detector and Indication**
- **PG De-Asserts Low when V_{IN} = 0V**
- **Fault Signal Output**
- **Integrated Current Sensing with Sense Output**
- **Programmable Over-Current Limit**
- **Programmable Short-Circuit Current Limit**
- **Pin Programmable Input Over-Voltage Protection Threshold (OV)**
- **Pin Programmable OCP Fault Regulation Time**
- **Adjustable Soft-Start (SS)**
- **Output Short-Circuit Protection (SCP)**
- **Over-Temperature Protection (OTP)**
- **Built-In Fuse Health Reporting**
- **Available in a Green TLGA-3×5-22L Package**

TYPICAL APPLICATION

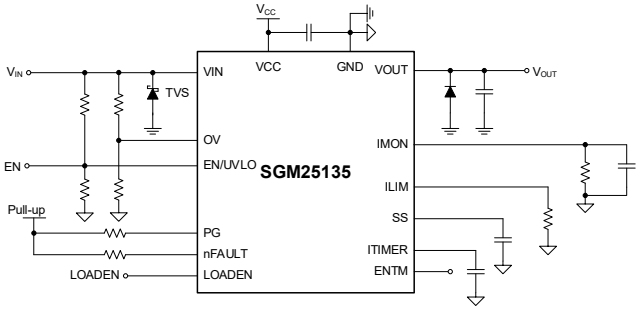


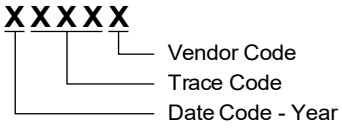
Figure 1. Typical Application Circuit

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM25135	TLGA-3×5-22L	-40℃ to +125℃	SGM25135XTLAX22G/TR	SGM25135 TLAX22 XXXXX	Tape and Reel, 5000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

V_{IN} (DC) ..... -0.3V to 20V
V_{IN} (1μs) 24V
V_{IN} (25ns) 29V
V_{OUT} ..... -0.3V to 20V
V_{OUT} (200ns) ..... -1.5V
All Other Pins ..... -0.3V to 4.2V
Package Thermal Resistance
TLGA-3×5-22L, θ_{JA} ..... 28.6℃/W
TLGA-3×5-22L, θ_{JB} ..... 2℃/W
TLGA-3×5-22L, $\theta_{JC\ (TOP)}$ ..... 21.1℃/W
TLGA-3×5-22L, $\theta_{JC\ (BOT)}$ ..... 2.3℃/W
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility (1) (2)
HBM ..... ±4000V
CDM ..... ±1000V

NOTES:

1. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.

2. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

RECOMMENDED OPERATING CONDITIONS

Input Voltage Operating Range ..... 2.7V to 16V
Operating Junction Temperature ..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

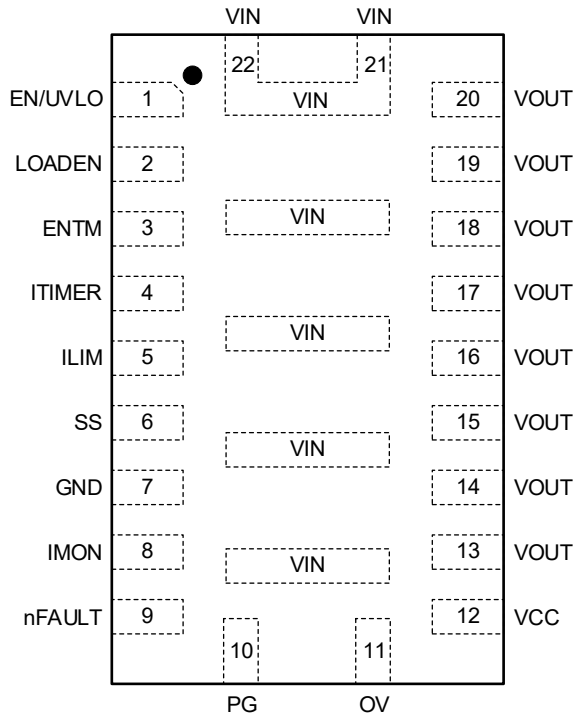
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

(TOP VIEW)



TLGA-3×5-22L

PIN DESCRIPTION

PIN	NAME	TYPE	FUNCTION
1	EN/UVLO	I	Enable Input or Under-Voltage Lockout. Asserting EN/UVLO pin high enables the device. As a UVLO pin, the UVLO threshold is configured using an external resistor divider. Do not leave this pin floating.
2	LOADEN	I	Load Enable Input. The LOADEN input controls the power switch. High level turns it on. To restore operation after shutdown, both LOADEN and EN must be asserted. The LOADEN pin cannot re-enable the switch by itself.
3	ENTM	—	LOADEN Blanking Time Set. The blanking time of LOADEN can be set by connecting an external capacitor. As soon as EN is activated, the timer is started and LOADEN is disabled. When EN is low or a fault occurs, the switch will shut down. However, LOADEN low does not operate during the blanking time.
4	ITIMER	—	Timer Set. An external capacitor from this pin to GND sets the fault timeout period and the hot-plug insertion time delay.
5	ILIM	—	Current Limit Set Pin. Set the over-current limit value by place a resistor to ground.
6	SS	—	Soft-Start. An external capacitor on the SS pin configures the output voltage soft-start timing. At startup, the internal circuitry regulates the output voltage's slew rate. Leaving SS floating forces the soft-start interval to its shortest possible duration (1ms).
7	GND	G	Ground.
8	IMON	O	Output Current Monitor. This pin delivers a voltage proportional to power supply output current. The gain of the IMON output voltage is configured by grounding the resistor (R_{IMON}). When in used, a capacitor exceeding 10nF should be connected in parallel with R_{IMON} to ensure stability.

PIN DESCRIPTION (continued)

PIN	NAME	TYPE	FUNCTION
9	nFAULT	O	Active-Low Fault Indicator. Active-low open-drain output. It is asserted during over-current, over-voltage, over-temperature, FET health or short-circuit fault condition. Pull nFAULT pin up to an external power supply through a 10kΩ to 100kΩ resistor.
10	PG	O	Power Good. Open-drain output. PG pin is pulled up to the external power supply via a 10kΩ to 100kΩ resistor. A high PG level indicates a power good condition.
11	OV	I	Over-Voltage Enable Input. Set the over-voltage disable threshold by connecting OV to an external resistor divider. Turn off the internal MOSFET by pulling OV high.
12	VCC	I	LDO Regulator. The internal 3.3V LDO regulator provides the output voltage. A 1μF decoupling capacitor must be placed adjacent to the VCC and GND pins to ensure stable power delivery.
13, 14, 15, 16, 17, 18, 19, 20	VOUT	O	Output Voltage which is Controlled by IC. A Schottky diode should be connected between VOUT and GND to ensure suppression of reverse voltage spikes during operation.
21, 22, Exposed Pads	VIN	P	Input Power Supply for Main Power.

NOTE: I = input, O = output, P = power, G = ground.

ELECTRICAL CHARACTERISTICS

(V_{IN} = 12V, R_{ILIM} = 7.5kΩ, T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Current							
Quiescent Current	I_Q	Intelli-Fuse on, no load	T_J = +25℃		0.45	0.75	mA
			T_J = -40℃ to +125℃			0.80	
		Fault latch off	T_J = +25℃		0.40	0.55	
			T_J = -40℃ to +125℃			0.75	
		Intelli-Fuse off with EN = 0V, V_{IN} = 12V	T_J = +25℃		0.20	0.30	
			T_J = -40℃ to +125℃			0.50	
		Intelli-Fuse off with EN = 0V, V_{IN} = 16V	T_J = +25℃		0.25	0.35	
			T_J = -40℃ to +125℃			0.55	
VCC Regulator and Under-Voltage Lockout (UVLO)							
VCC Regulator Output Voltage	V_{CC}	I_{VCC} = 0mA	T_J = +25℃	3.31	3.41	3.51	V
			T_J = -40℃ to +125℃	3.26		3.56	
		I_{VCC} = 10mA			3.39		
		I_{VCC} = 20mA			3.38		
VCC Under-Voltage Lockout Threshold Rising	V_{CCVTH_R}	T_J = +25℃		2.33	2.53	2.73	V
		T_J = -40℃ to +125℃		2.28		2.78	
VCC Under-Voltage Lockout Threshold Falling	V_{CCVTH_F}	T_J = +25℃		2.05	2.35	2.65	
		T_J = -40℃ to +125℃		2.0		2.7	
VCC Under-Voltage Lockout Threshold Hysteresis	V_{CCHYS}				180		mV
VIN Regulator and Under-Voltage Lockout (UVLO)							
VIN Under-Voltage Lockout Threshold Rising	V_{INVTH_R}	T_J = +25℃		2.36	2.56	2.76	V
		T_J = -40℃ to +125℃		2.31		2.81	
VIN Under-Voltage Lockout Threshold Falling	V_{INVTH_F}	T_J = +25℃		2.07	2.37	2.67	
		T_J = -40℃ to +125℃		2.02		2.72	
VIN Under-Voltage Lockout Threshold Hysteresis	V_{INHYS}				190		mV
EN/UVLO (Enable and VIN UVLO)							
EN/UVLO Input Rising Threshold	V_{EN_R}	T_J = +25℃		1.18	1.22	1.26	V
		T_J = -40℃ to +125℃		1.16		1.28	
EN/UVLO Input Falling Threshold	V_{EN_F}	T_J = +25℃		1.07	1.11	1.15	
		T_J = -40℃ to +125℃		1.05		1.17	
EN/UVLO Hysteresis	V_{EN_HYS}				110		mV
EN/UVLO Blanking Time	t_{EN_BLANK}	EN/UVLO recycling			1.06		ms
OV							
OV Input Rising Threshold	V_{OV_R}	T_J = +25℃		1.18	1.22	1.26	V
		T_J = -40℃ to +125℃		1.16		1.28	
OV Input Falling Threshold	V_{OV_F}	T_J = +25℃		1.10	1.14	1.18	
		T_J = -40℃ to +125℃		1.08		1.20	
OV Hysteresis	V_{OV_HYS}				80		mV

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 12V, R_{ILIM} = 7.5kΩ, T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Power FET							
On-Resistance	R_{DSON}	T_J = +25℃, I_{OUT} = 2A, V_{IN} = 12V			1.1	1.6	mΩ
		T_J = +25℃, I_{OUT} = 2A, V_{IN} = 2.7V			1.1	1.6	
		T_J = +125℃, I_{OUT} = 2A, V_{IN} = 12V			1.6	2.1	
		T_J = +125℃, I_{OUT} = 2A, V_{IN} = 2.7V			1.6	2.1	
Off-State Leakage Current	I_{OFF}	V_{IN} = 16V, power FET off, T_J = +25℃				3	μA
ENTM							
ENTM Rising Threshold	V_{ENTM_R}	T_J = +25℃		1.18	1.22	1.26	V
		T_J = -40℃ to +125℃		1.16		1.28	
Charge Current	I_{ENTM}	T_J = +25℃		0.70	1.0	1.30	μA
		T_J = -40℃ to +125℃		0.60		1.40	
LOADEN Pin							
LOADEN Low Voltage	V_{LOADEN_L}	T_J = +25℃				1.0	V
		T_J = -40℃ to +125℃				0.8	
LOADEN High Voltage	V_{LOADEN_H}	T_J = +25℃		1.8			V
		T_J = -40℃ to +125℃		2.0			
Thermal Shutdown							
Over-Temperature Threshold	T_{SD}				148		℃
Current Monitor Output (IMON)							
IMON Sense Gain	I_{MON}/I_{FET}	I_{OUT} = 17A	T_J = +25℃, initial accuracy	19.8	20.0	20.3	μA/A
			T_J = -40℃ to +125℃	19.4		20.6	
		15A >I_{OUT} > 4A	T_J = +25℃, initial accuracy	19.7	20.0	20.5	
			T_J = -40℃ to +125℃	18.9		21.1	
		I_{OUT} > 15A	T_J = +25℃, initial accuracy	19.5	20.0	20.4	
			T_J = -40℃ to +125℃	19.2		20.6	
IMON Sense Offset		I_{OUT} > 4A	T_J = +25℃	-0.5		0.5	μA
			T_J = -40℃ to +125℃	-0.5		0.5	
Current Limit							
ILIM Voltage	V_{ILIM}	T_J = +25℃		-5%	0.605	5%	V
		T_J = -40℃ to +125℃		-7%		7%	
OC Internal Current Sensing Gain		1/10 of IMON gain			2		μA/A
Current Limit at Normal Operation	I_{OC_NOR}	R_{ILIM} = 7.5kΩ	T_J = +25℃	-7%	40	7%	A
			T_J = -40℃ to +125℃	-12%		12%	
Current Limit at Soft-Start	I_{OC_SS}	I_{OC_NOR} < 32A, V_{OUT} < 90%V_{IN}			I_{OC_NOR}		A
		I_{OC_NOR} > 32A, V_{OUT} < 90%V_{IN}			32		A
OC Regulation Time at Soft Start	t_{OC_REG}				1.59		ms
Fast-Trip Threshold	I_{FT}				2 × I_{OC_NOR}		A
Short-Circuit Current Limit	I_{SC}				80		A
Short-Circuit Protection Response Time	t_{SC}				200		ns

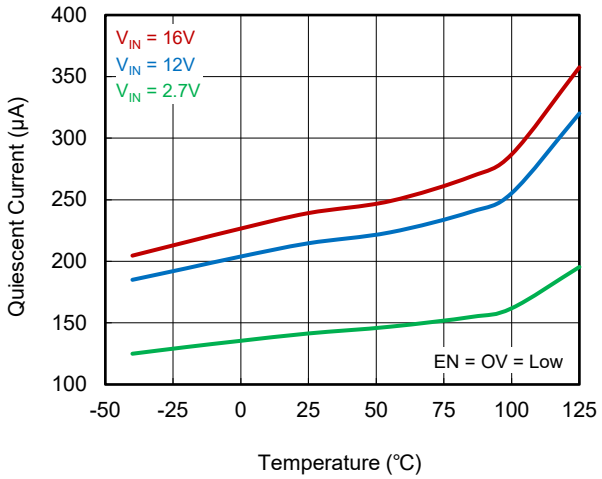
ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 12V, R_{ILIM} = 7.5kΩ, T_J = +25℃, unless otherwise noted.)

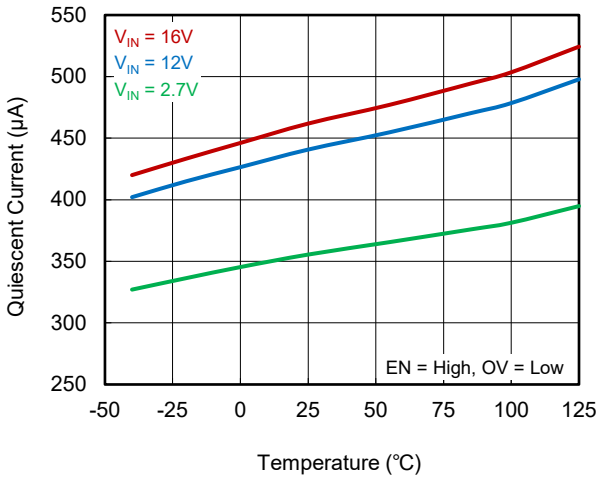
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
ITIMER							
Upper Threshold Voltage	V_{ITIMER_H}	T_J = +25℃		1.15	1.19	1.23	V
		T_J = -40℃ to +125℃		1.13		1.25	
Insertion Delay Charge Current	I_{INSRT}	T_J = +25℃		3.4	4.0	4.6	μA
		T_J = -40℃ to +125℃		3.2		4.8	
OCP Fault Timeout Charge Current	I_{FLT_ITIMER}	T_J = +25℃		32	40	48	μA
		T_J = -40℃ to +125℃		30		50	
Discharge R_{DSON}	R_{ITIMER}				11.0		Ω
Soft Start (SS)							
SS Pull-Up Current	I_{SS}	V_{IN} = 12V	T_J = +25℃	11.5	13.5	15.5	μA
			T_J = -40℃ to +125℃	8.5		19.5	
nFAULT							
Output Low Voltage	V_{OL}	I_{SINK} = 10mA	T_J = +25℃			0.25	V
			T_J = -40℃ to +125℃			0.30	
Off-State Leakage Current	I_{LK}	V_{nFAULT} = 3.3V	T_J = +25℃			0.5	μA
			T_J = -40℃ to +125℃			1.0	
Power Good Output (PG)							
PG Rising Threshold	PG_{VTH_R}	V_{IN} = 12V	T_J = +25℃	88.5	93.0	97.5	%V_{IN}
			T_J = -40℃ to +125℃	88.0		98.0	
		V_{IN} = 2.7V			2.15		V
PG Falling Threshold	PG_{VTH_F}	V_{IN} = 12V	T_J = +25℃	73.5	78.0	82.5	%V_{IN}
			T_J = -40℃ to +125℃	73.0		83.0	
		V_{IN} = 2.7V			2.05		V
Output Low Voltage	V_{OL}	I_{SINK} = 10mA	T_J = +25℃			0.2	V
			T_J = -40℃ to +125℃			0.3	
Off-State Leakage Current	I_{LK}	V_{PG} = 3.3V	T_J = +25℃			0.7	μA
			T_J = -40℃ to +125℃			1.0	
FET Short Detection							
FET Drain-to-Source Short Entry Threshold	$V_{OUT\_DSTH\_ENT}$	V_{IN} = 12V	T_J = +25℃	88.5	93.0	97.5	%V_{IN}
			T_J = -40℃ to +125℃	88.0		98.0	
		V_{IN} = 2.7V			2.15		V
FET Drain-to-Source Short Recovery Threshold	$V_{OUT\_DSTH\_EXT}$	V_{IN} = 12V	T_J = +25℃	73.5	78.0	82.5	%V_{IN}
			T_J = -40℃ to +125℃	73.0		83.0	
		V_{IN} = 2.7V			2.05		V
Gate-to-Source Short Protection Delay Time	t_{GS_ST}	V_{SS} > V_{CC} - 0.7			200		ms

TYPICAL PERFORMANCE CHARACTERISTICS

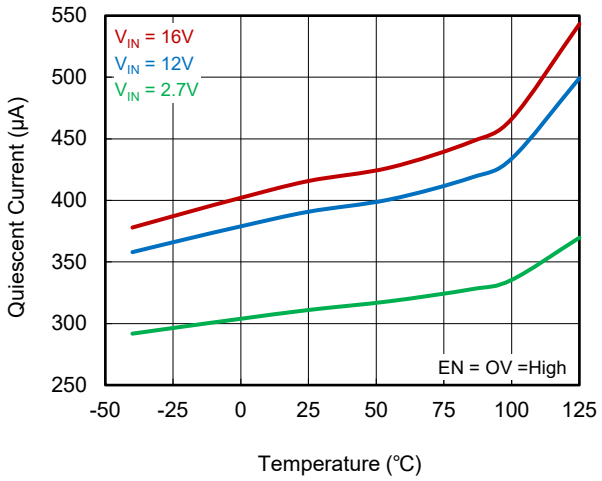
Quiescent Current vs. Temperature



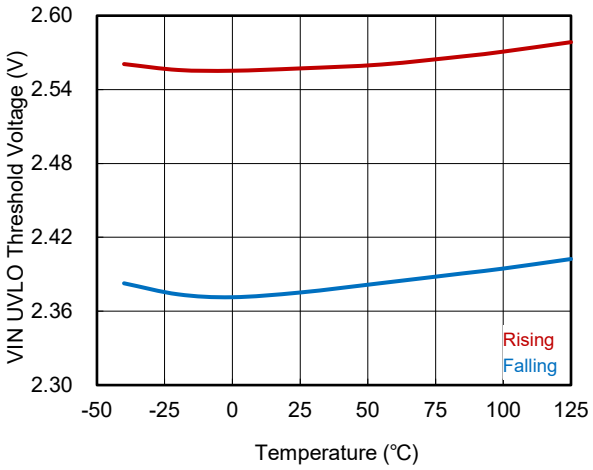
Quiescent Current vs. Temperature



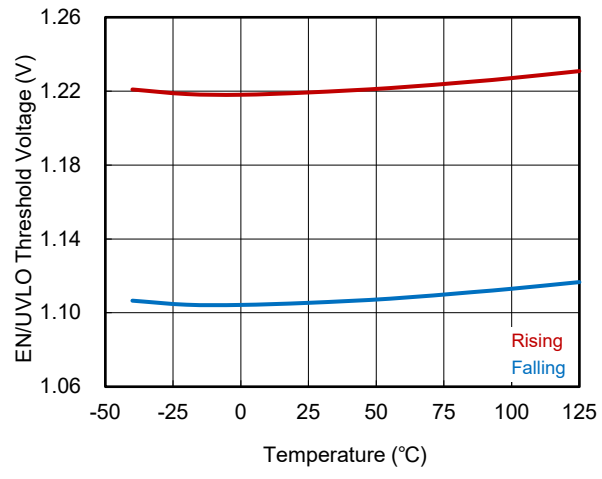
Quiescent Current vs. Temperature



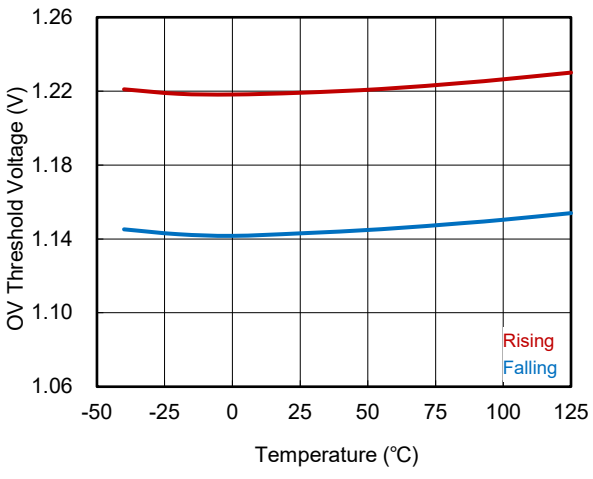
VIN UVLO Threshold vs. Temperature



EN/UVLO Threshold vs. Temperature

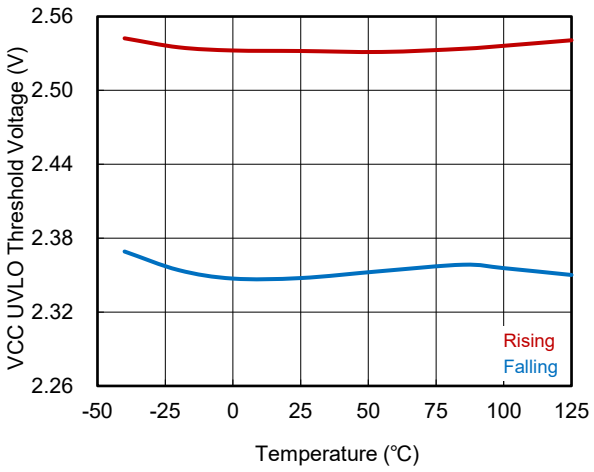


OV Threshold vs. Temperature

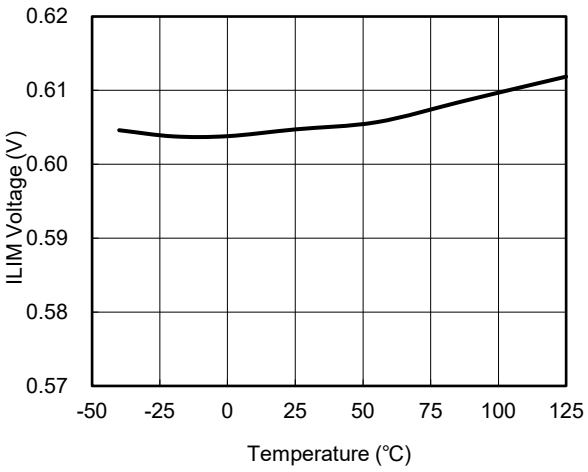


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

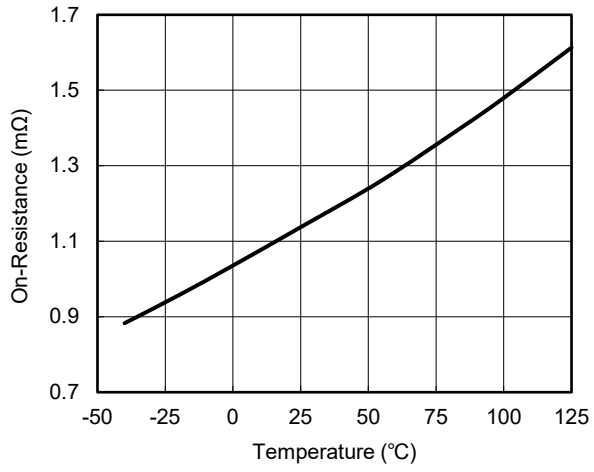
VCC UVLO Threshold vs. Temperature



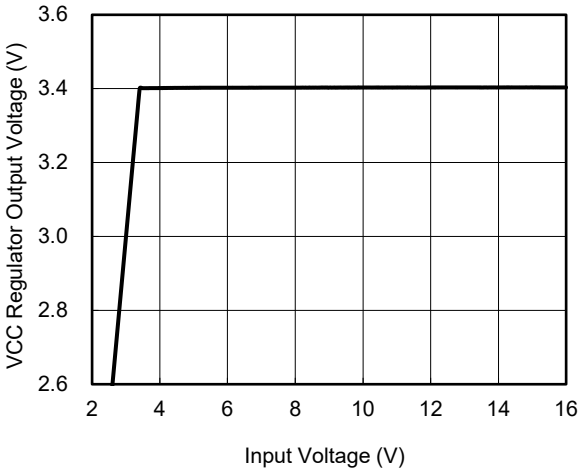
ILIM Voltage vs. Temperature



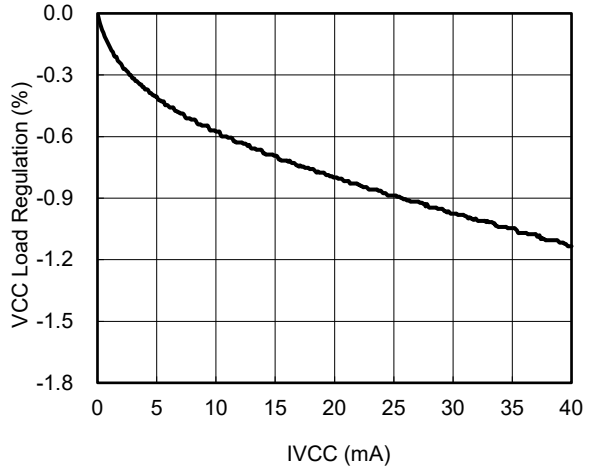
On-Resistance vs. Temperature



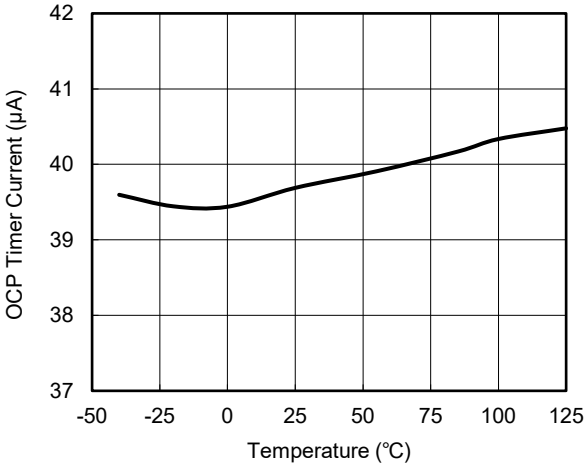
VCC Regulator Output Voltage vs. Input Voltage



VCC Load Regulation



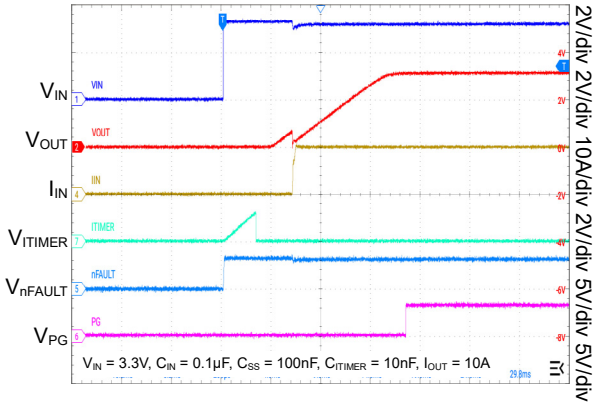
OCP Timer Current vs. Temperature



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

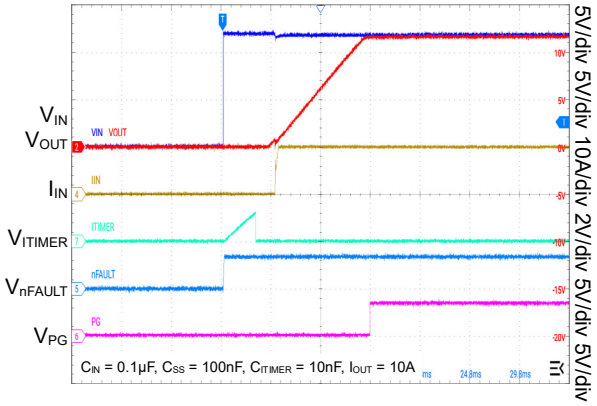
V_{IN} = 12V, R_{ILIM} = 7.5kΩ, R_{IMON} = 1kΩ, T_A = +25℃, and PG and nFAULT are pulled up to VCC, unless otherwise noted.

VIN Hot-Plug at 3.3V



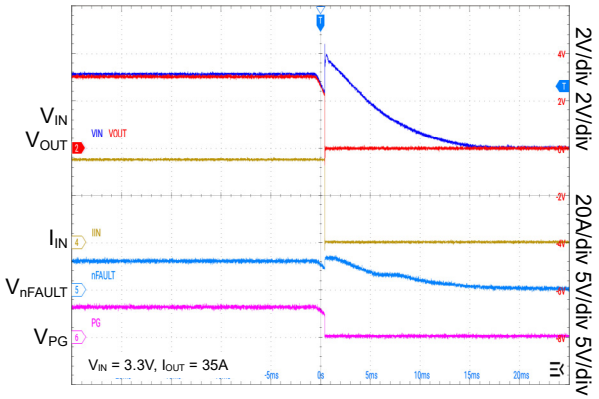
Time (5ms/div)

VIN Hot-Plug at 12V



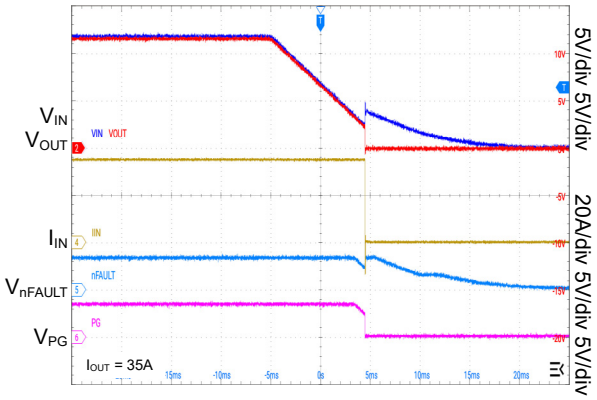
Time (5ms/div)

VIN Shutdown at 3.3V



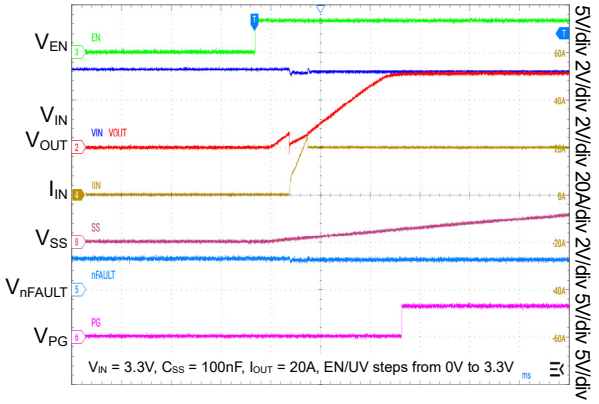
Time (5ms/div)

VIN Shutdown at 12V



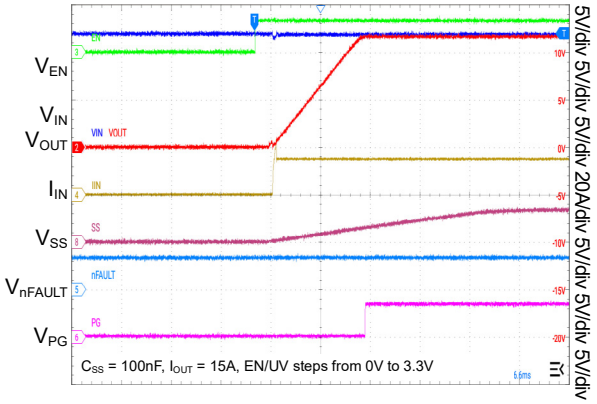
Time (5ms/div)

Startup through EN/UVLO at 3.3V Input



Time (5ms/div)

Startup through EN/UVLO at 12V Input

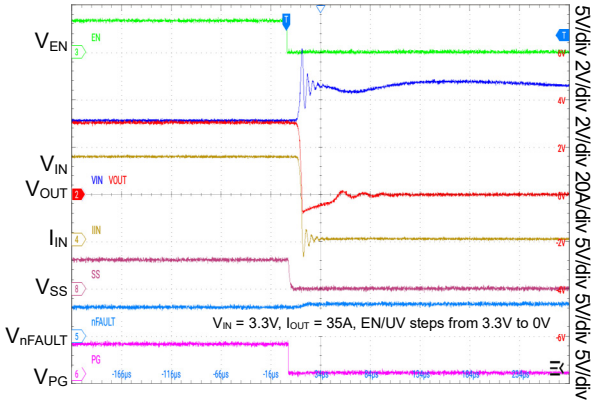


Time (5ms/div)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

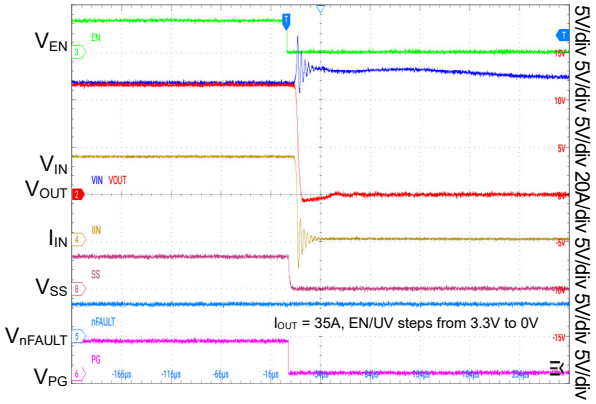
V_{IN} = 12V, R_{ILIM} = 7.5kΩ, R_{IMON} = 1kΩ, T_A = +25℃, and PG and nFAULT are pulled up to VCC, unless otherwise noted.

Shutdown through EN/UVLO at 3.3V Input



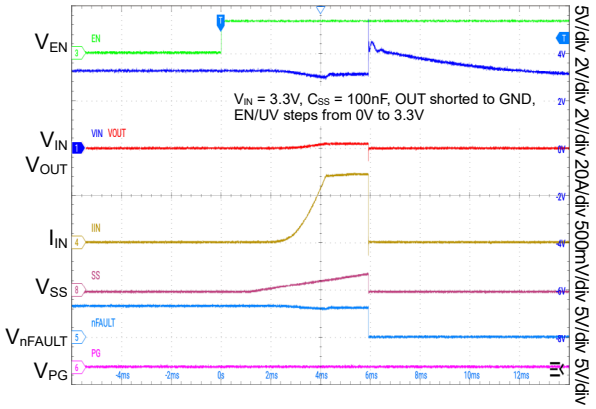
Time (50μs/div)

Shutdown through EN/UVLO at 12V Input



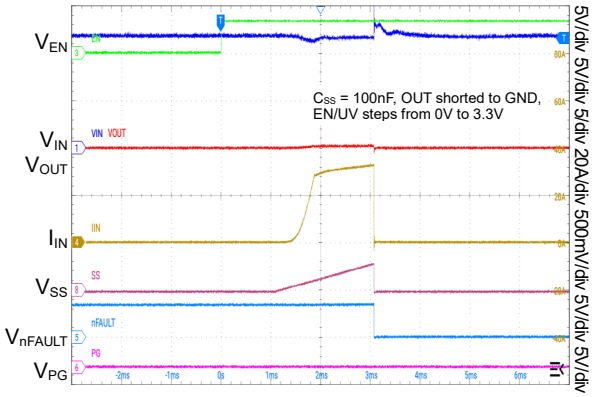
Time (50μs/div)

Short-Circuit Startup at 3.3V Input



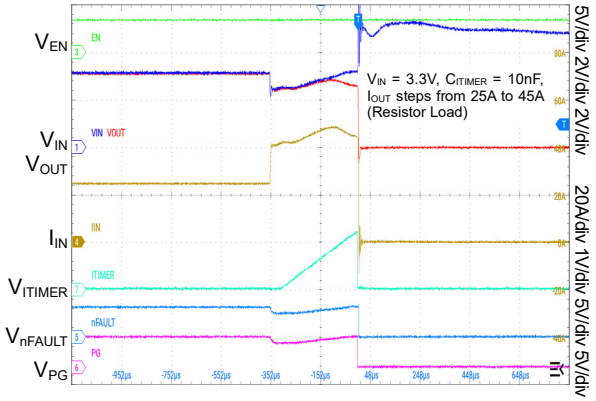
Time (2ms/div)

Short-Circuit Startup at 12V Input



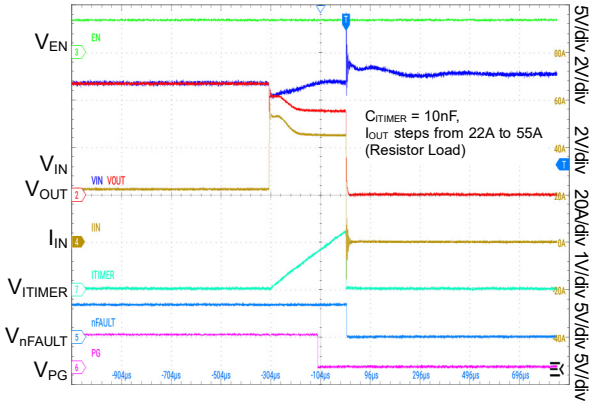
Time (1ms/div)

Over-Current Protection at 3.3V Input



Time (200μs/div)

Over-Current Protection at 12V Input

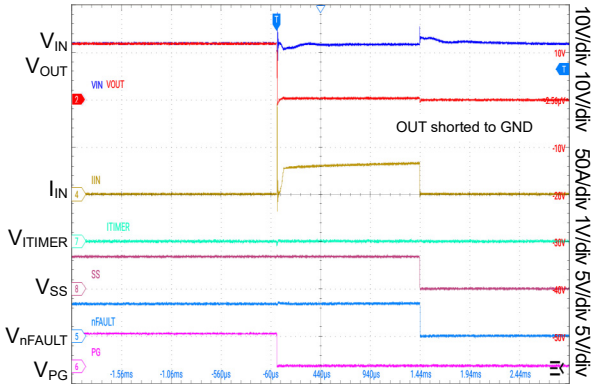


Time (200μs/div)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

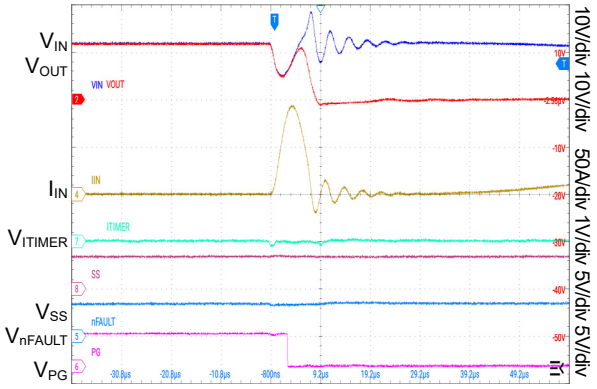
V_{IN} = 12V, R_{ILIM} = 7.5kΩ, R_{IMON} = 1kΩ, T_A = +25℃, and PG and nFAULT are pulled up to VCC, unless otherwise noted.

Short-Circuit Protection



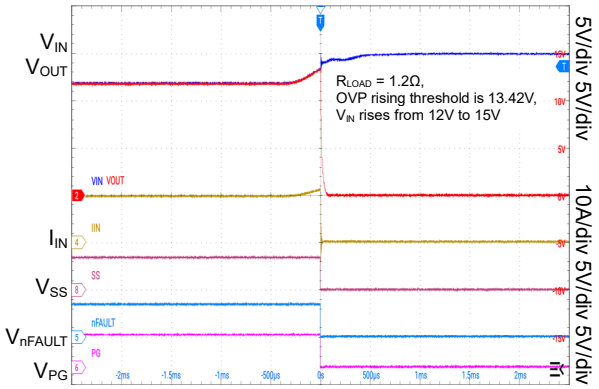
Time (500μs/div)

Short-Circuit Protection (Zoomed)



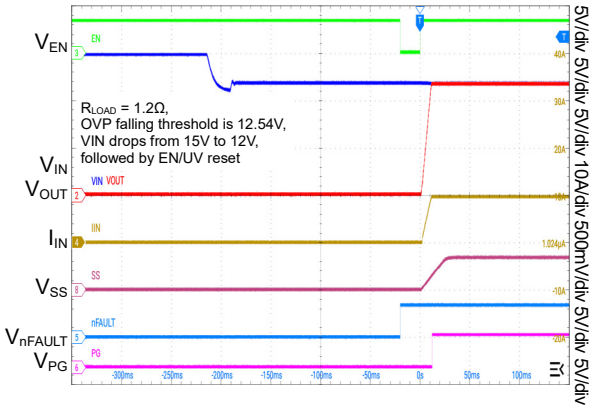
Time (10μs/div)

VIN OVP Shutdown



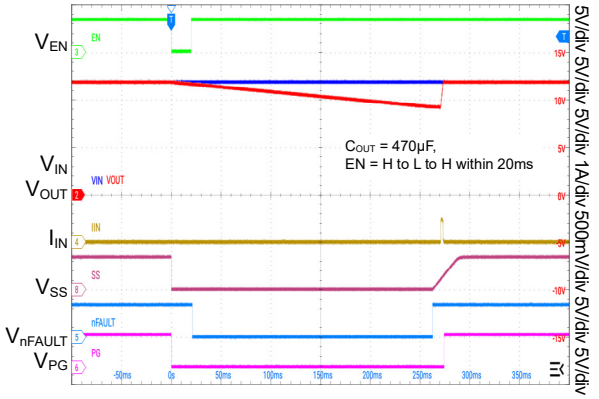
Time (500μs/div)

VIN OVP Recovery



Time (50ms/div)

Drain-to-Source Short Protection



Time (50ms/div)

FUNCTIONAL BLOCK DIAGRAM

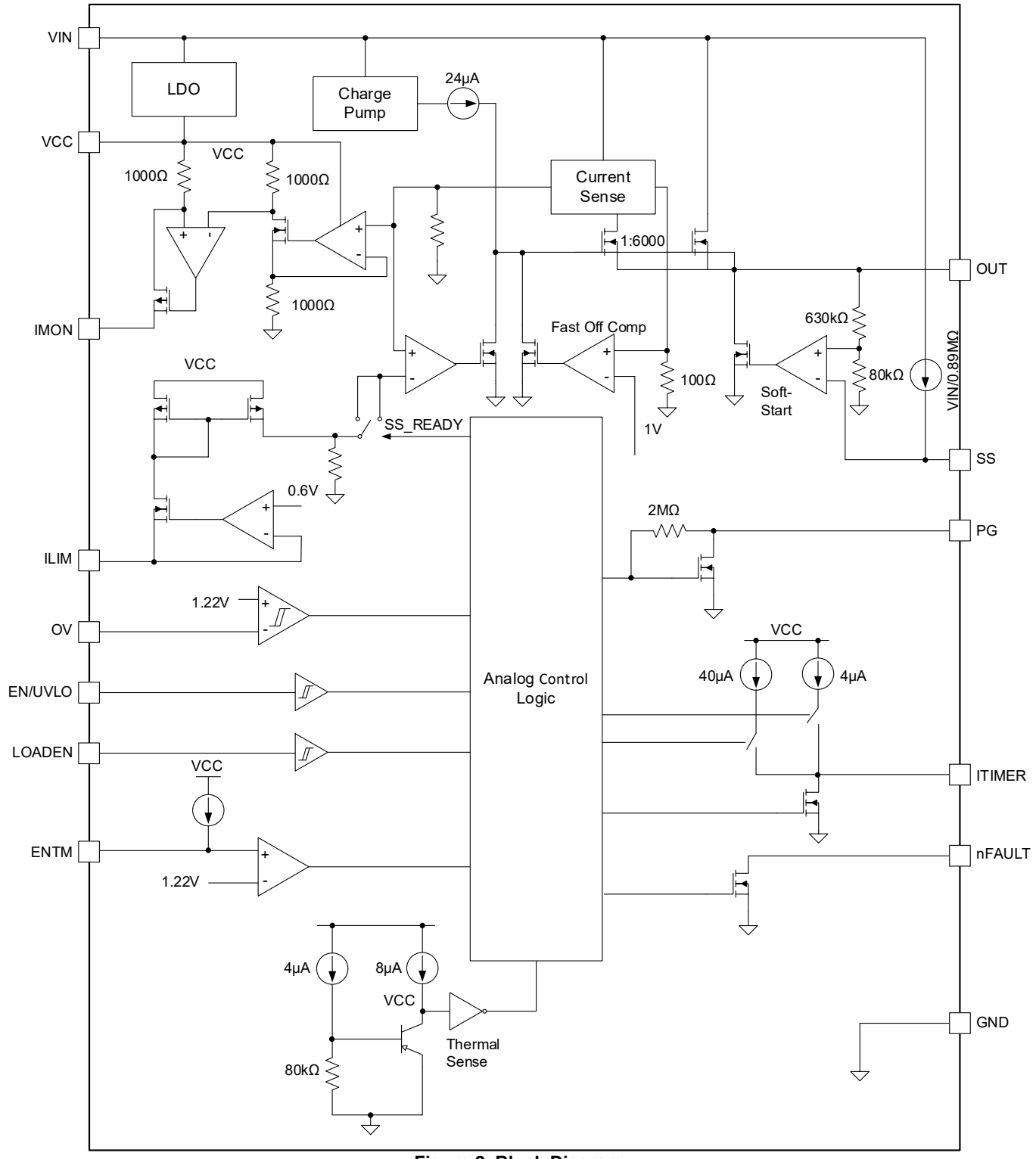


Figure 2. Block Diagram

OPERATION

The SGM25135 is a monolithic e-Fuse device with an integrated, 1.1mΩ R_{DSON} power N-MOSFET that is ideally suited for large current applications. The device supports up to 35A of continuous output current per device at room temperature and minimizes backplane voltage drop by regulating inrush current during hot-swap insertion of a circuit card into a live backplane power source.

During hot-swap operation and the device is enabled, the MOSFET gate charging process initiates only after a programmable insertion delay period. This delay is set by an external capacitor connected to the ITIMER pin, where the capacitance value determines the length of the delay. The output voltage then increases gradually as the SS (soft-start) voltage ramps up, with the slope of this ramp controlling the gate charging slew rate. After a successful startup sequence, the device then actively monitors its load current, input voltage and protects the load from harmful over-current and over-voltage conditions. Additionally, it senses the junction temperature and shuts down the device once the temperature exceeds the safe operating conditions.

Power-Up Sequence

During hot-swap operations, inductive voltage transients may manifest at the SGM25135's supply terminal during connector mating events, primarily attributed to PCB trace inductance (L_trace) and the input capacitor's equivalent series inductance (ESL). To ensure stable rail conditions during power-up, a controlled timing sequence precedes main FET activation: the ITIMER initiates a 4μA current-limited charging path to C_{ITIMER} upon UVLO engagement. The timing cycle completes when the ITIMER reference potential achieves 1.19V, with C_{ITIMER} values derivable from Equation 1:

$$t_{DELAY} = \frac{1.19}{4} \times C_{ITIMER} \quad (1)$$

Where t_{DELAY} is the insertion delay time (ms), and C_{ITIMER} is the timer capacitor (nF). For instance, a 10nF capacitor corresponds to an insertion delay timer of 3ms.

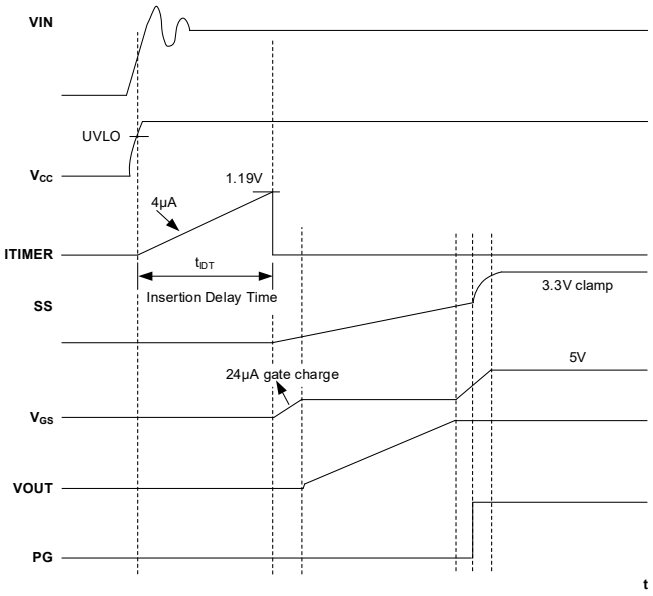


Figure 3. Power Sequence

Once V_{IN} and V_{CC} exceed the UVLO thresholds, the ITIMER pin uses an internal 4μA current source to charge the external C_{ITIMER} capacitor. The insertion delay time (t_{IDT}) is defined as the time required for the capacitor to rise from 0V to 1.19V under this charging mechanism. t_{IDT} can be configured by selecting an appropriate capacitor value for the C_{ITIMER} connected between the ITIMER pin and ground.

When the insertion delay period ends and EN exceeds 1.22V, the internal 24μA charge pump starts charging the MOSFET. The MOSFET conducts once its gate-source voltage (V_{GS}) surpasses the threshold (V_{GS_TH}), raising VOUT.

Soft-Start (SS)

SS uses a capacitor to determine the soft-start time. After the EN pin is pulled high and the startup delay period concludes, a constant current source that scales with the input voltage begins charging the SS capacitor voltage. This ensures consistent soft-start duration across varying input voltages. The output voltage's slew rate maintains tight synchronization with the SS voltage's charging profile. The SS capacitor value is determined via Equation 2:

$$C_{SS} = 9 \times \frac{t_{SS}}{R_{SS}} \quad (2)$$

Where t_{SS} is the soft-start time (ms), C_{SS} is the soft-start capacitor (nF), and R_{SS} is 0.89MΩ.

OPERATION (continued)

For instance, a 100nF capacitor yields an 8.9ms soft-start duration. When the load capacitance becomes excessively large, the current needed to sustain the set soft-start time surpasses the startup current threshold. Under such conditions, the voltage rise rate is governed by both the load capacitor's time constant and the current limit. Floating the SS pin generates a rapid voltage ramp-up. A 24μA current source drives the power FET's gate, where the gate charge current dictates the output voltage's rise profile. The resultant soft-start duration reaches 1ms, marking the minimal achievable output voltage ramp-up time under these parameters.

Enable and LOADEN

The enable/disable state of the SGM25135 is controlled by EN and LOADEN (see Table 1).

The exclusive switch can be enabled by setting EN = 1 during the LOADEN blanking period. After this period, EN = 1 and LOADEN = 1 must be asserted simultaneously to maintain the operation of the switch. EN = 0 unconditionally disables all working modes. To recover from the latch failure state, restart the EN control signal or VIN power supply.

Table 1. EN/LOADEN Blanking Time

LOADEN Blanking Time Over?	EN	LOADEN	Status
N	0	0	Off
N	0	1	Off
N	1	0	On
N	1	1	On
Y	0	0	Off
Y	0	1	Off
Y	1	0	Off
Y	1	1	On

Note that LOADEN deactivates the power switch after its blanking period, but cannot re-enable it solely by cycling LOADEN. See Figure 4.

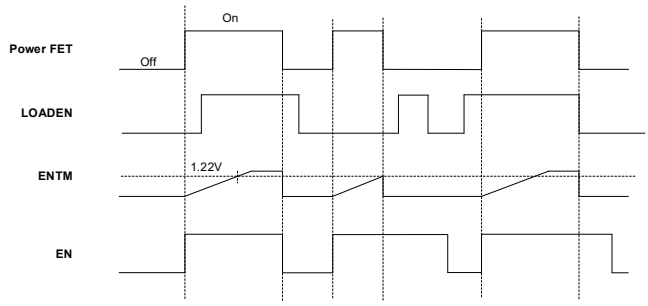


Figure 4. EN/LOADEN Timing Diagram

Upon enabling the component, the insertion delay mechanism activates. Once the delay interval completes, an internal 24μA current path is established to source charge to the power MOSFET's gate terminal. The voltage across gate-source (V_{GS}) achieves its threshold within approximately 1ms, after which the output voltage progression adheres to the soft-start (SS) defined slope profile.

LOADEN Blanking Time

When the enable signal (EN) is asserted high, LOADEN incorporates a programmable blanking time to inhibit de-assertion during the specified interval (refer to Figure 5). All fault detection functions remain enabled during startup. The power FET shuts down immediately upon fault detection. A transition of LOADEN to low during the blanking period does not deactivate the power FET switch.

Upon termination of the blanking period, LOADEN resumes standard operational control functionality.

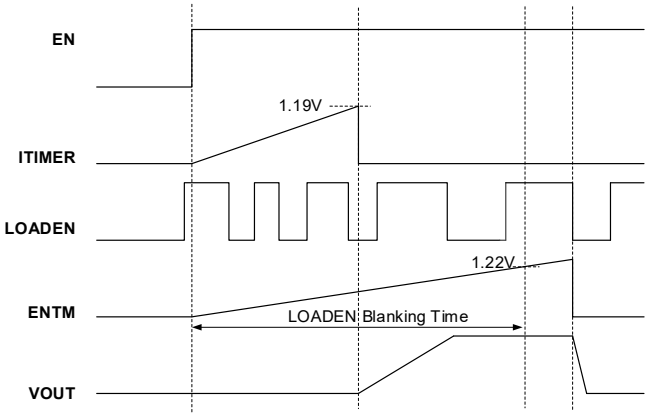


Figure 5. LOADEN Blanking Time

OPERATION (continued)

The blanking time is determined by a capacitor connected to the ENTM pin. The value of the blanking timer capacitor is calculated via Equation 3:

$$C_{ENTM} = \frac{1}{1.22} \times t_{LDNB} \quad (3)$$

Where t_{LDNB} (s) represents the LOADEN signal's blanking time, and C_{ENTM} (μF) the capacitor connected to the ENTM pin. For example, a 1μF capacitor results in a blanking time of 1.22s.

Connect ENTM to GND if LOADEN is not used.

Power Good (PG)

PG (Power Good) is an open-drain status monitor that asserts high when VOUT maintains regulation within specified input-referenced thresholds. This output requires a 10kΩ to 100kΩ pull-up resistor to the supply rail. During the startup sequence, PG remains in active-low state to enforce system shutdown, minimizing V_{OUT} loading for safe power-up operation. This active-low signaling facilitates inrush current mitigation and thermal optimization during initialization phases.

The power-good signal is asserted when all of the following conditions are met, enabling the system to operate at full power.

- V_{GS} > 2V
- V_{OUT} > 93% × V_{IN}, or V_{OUT} > V_{IN} - 0.55V

The PG signal asserts low when any of the following conditions occur:

- V_{OUT} < 78% × V_{IN}, or V_{OUT} < V_{IN} - 0.65V
- EN/UVLO = low
- Faults occurred

In the absence of an input signal, the PG pin remains low despite the presence of a pull-up resistor to the supply.

Fault Bar (nFAULT)

nFAULT (Fault Bar) is an open-drain fault indicator that asserts low when triggered. This output requires an external 10kΩ to 100kΩ pull-up resistor to the supply rail. The assertion occurs with 4μs maximum propagation delay from fault detection to active-low signaling.

- Over-current or output short
- Over-temperature
- Over-voltage
- V_{DS}/V_{GS} short

nFAULT goes high when the SGM25135 resumes normal operation. This means that the output voltage is higher than the setting voltage of the PG rising threshold, and the power FET is fully on (V_{GS} > 2V).

Over-Current Protection (OCP)

The SGM25135 uses an external resistor to set a constant current limit. When the current through the FET reaches the programmed threshold, the internal regulator adjusts the gate voltage of the power FET to maintain constant current flow. The current limit can be set using Equation 4:

$$I_{ILIM} = \frac{0.3V}{R_{ILIM}} \times 10^6 (A) \quad (4)$$

Where R_{ILIM} (Ω) is the resistor from ILIM to ground.

If V_{OUT} < max (V_{IN} - 0.55V, 93% of V_{IN}), the SGM25135 is in startup mode. During startup, the soft-start current limit (I_{OC_SS}) follows the normal current limit (I_{OC_NOR}), which is determined by the R_{ILIM}. To avoid overheating, I_{OC_SS} has a 32A internal current limit clamp during start up. The actual current limit value during startup is MIN (32A, I_{OC_NOR}).

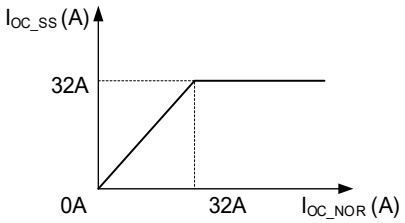


Figure 6. Startup Current Limit to Normal Over-Current Limit

If the output voltage V_{OUT} exceeds max (V_{IN} - 0.55V, 93% of V_{IN}), and the power FET gate voltage approaches the internal charge pump voltage, the device enters normal mode. When SGM25135 enters normal mode, and the current limiting I_{OC_NOR} is determined by I_{ILIM} only.

The response time of the device is typically 200μs. Due to the response time, the output current may have a small overshoot.

OPERATION (continued)

Intelli-Fuse OCP during Startup

During startup mode, if the current through the FET is regulated at I_{OC_SS} for OC regulation time (t_{OC_REG}), the FET is turned off and the nFAULT is asserted.The typical t_{OC_REG} is 1.59ms, while the actual regulation time also depends on the over-temperature protection. Once OTP is triggered before t_{OC_REG}, the FET is turned-off. Therefore, the maximum current limit regulation time during startup is t_{OC_REG}. See Figure 7.

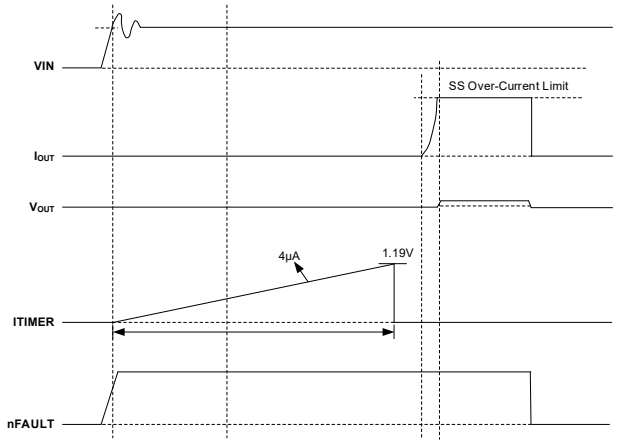


Figure 7. Soft-Start OCP Behavior

OCP during Normal Operation

During normal mode, when an over-current event triggers, the current is regulated at I_{OC_NOR} and the fault timer is initiated. The device resumes normal operation if the output current drops below the ILIM threshold before the fault timeout period (t_{OC}) expires. Conversely, if the over-current condition persists beyond t_{OC}, the power FET will be latched off. The duration of t_{OC} can be calculate by following Equation 5:

$$t_{OC} = \frac{1.19}{40} \times C_{ITIMER} \quad (5)$$

Where t_{OC} is the fault timer (ms), and C_{ITIMER} is the timer capacitor (nF). For instance, a 10nF capacitor corresponds to an insertion delay timer of 0.3ms.

Upon reaching the current limit threshold, the nFAULT is asserted low after a 4μs propagation delay. (see Figure 8).

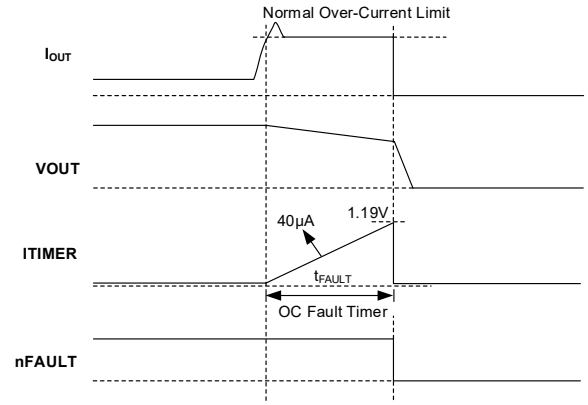


Figure 8. Normal Operation OCP Behavior

Short-Circuit Protection (SCP)

During short-circuit events causing rapid load current rise, instantaneous current may exceed the set threshold. The power FET must disable before reaching the short-circuit threshold to prevent damage. This fast response minimizes voltage droop during faults. The short-circuit response requires about 200ns.

After V_{OS} falls to a low level, the SGM25135 initiates an immediate restart to prevent input voltage line transients. The gate of the FET is then charged by an internal charge pump. When V_{OUT} starts again, under persistent short-circuit conditions, the load current is regulated by the I_{OC_SS} for t_{OC_REG} which is the same mechanism as over-current during startup mode.

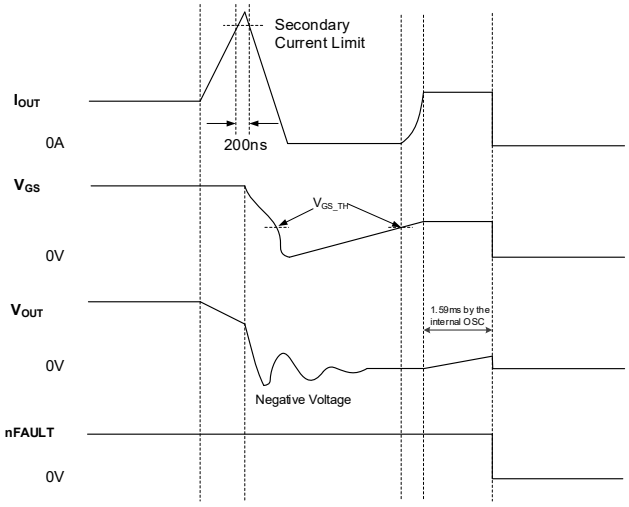


Figure 9. SCP Behavior

OPERATION (continued)

When a hard short arises causing the input voltage to descend below V_{CC} abruptly, the power FET gate voltage is forcibly pulled low instantaneously, independent of the secondary current limit's engagement status. Subsequently, the device initiates a secondary activation cycle while maintaining the persistent fault state.

The nFAULT asserts a low-state signal upon timer expiration if the sustained fault condition remains unresolved.

Over-Temperature Protection (OTP)

The SGM25135 incorporates integrated junction temperature monitoring. When the temperature exceeds the thermal shutdown threshold (T_{SD} = +148℃), the power FET shuts off and nFAULT indicates low.

V_{IN} Over-Voltage Protection (V_{IN} OVP)

The SGM25135 has input over-voltage protection, and once the input voltage exceeds the set OV voltage, the power FET is turned off and the nFAULT and SS are pulled low.

DS Short Detection

When EN is high, the SGM25135 activates continuous drain-source short monitoring. If V_{OUT} > min (V_{IN} - 0.55V, 93% × V_{IN}) during the insertion delay period, the device immediately drives GATE low to disable the power FET while asserting nFAULT and PG low. The FET remains off until V_{OUT} < min (78% × V_{IN}, V_{IN} - 0.65V). Upon detecting a drain-source short during normal operation, nFAULT and PG are actively pulled low. The system automatically resumes standard functionality when the short-circuit condition is eliminated.

GS Short Detection

When these conditions are satisfied, the device detects a GS short and disables the power FET.

- V_{GATE} < V_{CP} - 0.9V
- V_{SS} > V_{CC} - 0.7V
- NO OC fault
- Delay 200ms

APPLICATION INFORMATION

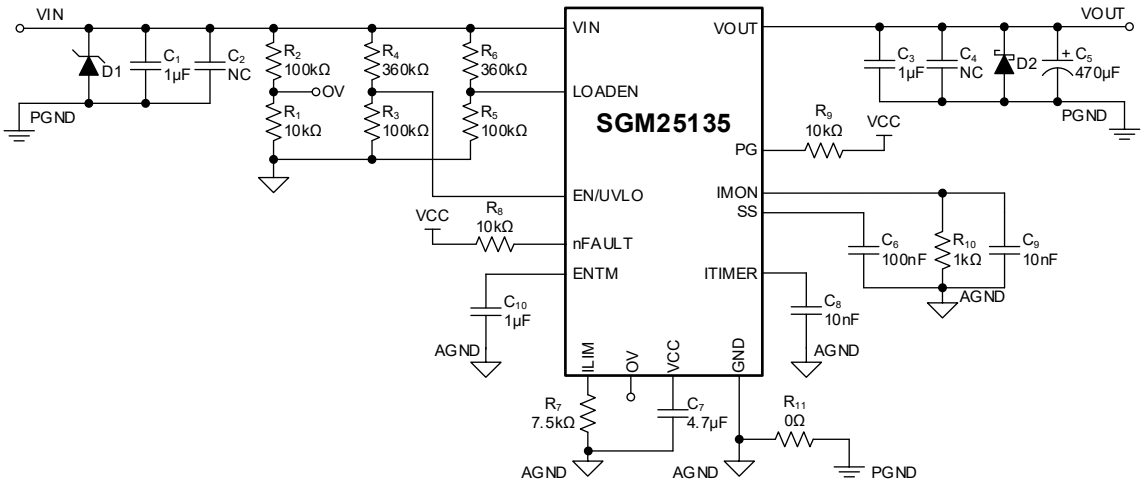


Figure 10. Typical Application Circuit

Current Limit Set (R_{SET})

The SGM25135's current limit setting must exceed the maximum expected load current in normal operation, with design margin accommodating current sense measurement tolerances. This threshold is configured through the calculation method specified in Equation 6:

$$I_{ILIM} = \frac{0.3V}{R_{ILIM}} \times 10^6 (A) \quad (6)$$

Current Monitor Set

The SGM25135 monitors the current level through the MOSFET by sensing the voltage on the IMON pin, with a R_{IMON} resistor must be connected between this pin and GND. The IMON current can be calculated by Equation 7:

$$I_{IMON} = I_{FET} \times 20\mu A / A \quad (7)$$

Where I_{FET} is the current flowing through the MOSFET.

Then, the voltage can be achieved through the Equation 8:

$$V_{IMON} = I_{IMON} \times R_{IMON} \quad (8)$$

Using a 1kΩ R_{IMON} resistor can achieve a gain of 20mV/A. A small capacitor such as 10nF can also be placed in parallel with the R_{IMON} resistor to smooth the indicator voltage.

PCB Layout Guidelines

To ensure optimal IC performance, careful consideration must be given to PCB layout design. The following key guidelines should be implemented:

• Place a transient voltage suppressor (TVS) diode between VIN and GND, placing it as close as possible to the power pins.

• Place a 1μF or larger ceramic decoupling capacitor between VIN and GND, placing it as close as possible to the power pins.

• Place a 1μF or larger ceramic capacitor between VCC and GND, placing it as close as possible to the pin.

• Connect the GND pad to an analog ground (AGND) plane, in which all the analog GNDs of the part are referenced. Connect the AGND plane to power ground (PGND) planes at single point.

• Place a Schottky diode close to VOUT and GND to absorb negative voltage spikes during FET shutdown.

• Place a low-ESR ceramic output capacitor between VOUT and GND, placing it as close as possible to the power pins.

• Route the connection between the R_{ILIM} resistor and the device using the shortest possible trace lengths to minimize parasitic inductance.

• Place enough vias close to the power traces to achieve better thermal performance.

• Ensure that all VIN and VOUT pins are connected together to achieve adequate current capability.

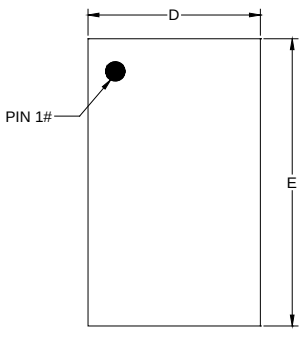
REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

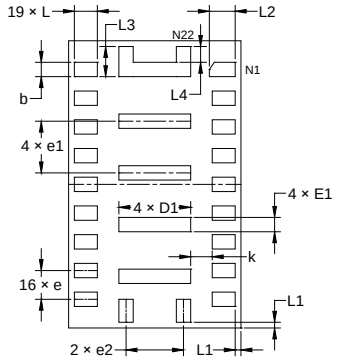
Changes from Original to REV.A (JULY 2026)	Page
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

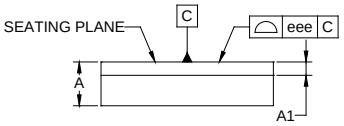
TLGA-3×5-22L



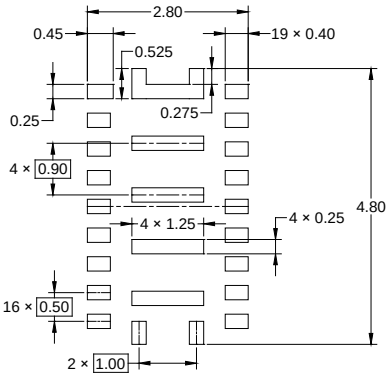
TOP VIEW



BOTTOM VIEW



SIDE VIEW



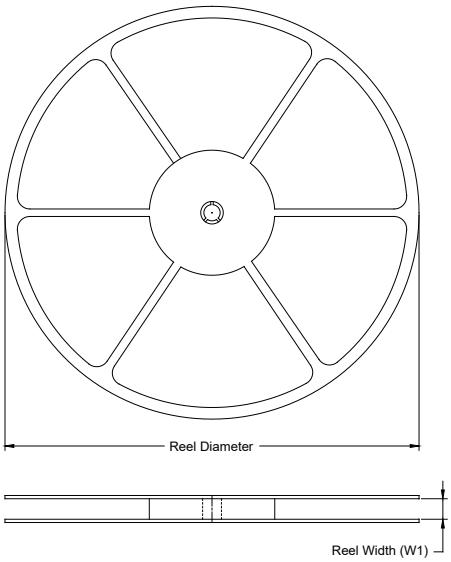
RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	0.712	-	0.810
A1		0.232 REF	
b	0.200	-	0.300
D	2.900	-	3.100
D1	1.150	-	1.350
E	4.900	-	5.100
E1	0.150	-	0.350
e		0.500 BSC	
e1		0.900 BSC	
e2		1.000 BSC	
k		0.375 REF	
L	0.350	-	0.450
L1		0.100 REF	
L2	0.400	-	0.500
L3	0.475	-	0.575
L4	0.225	-	0.325
eee		0.100	

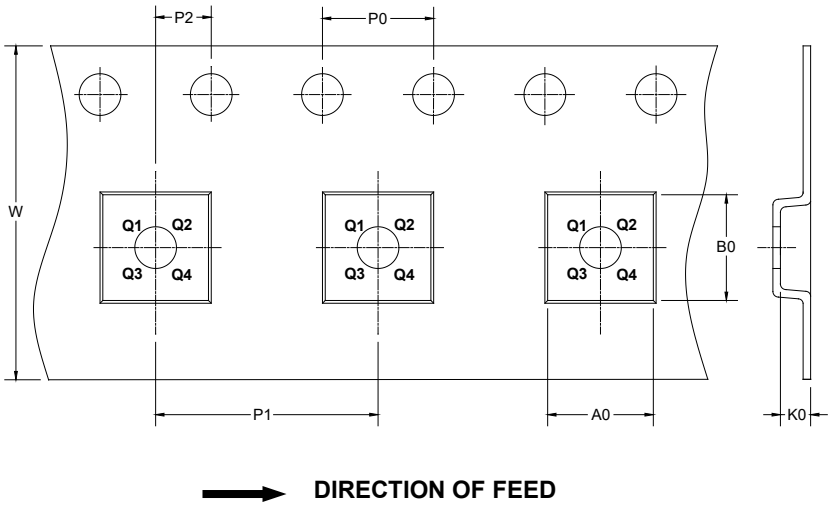
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



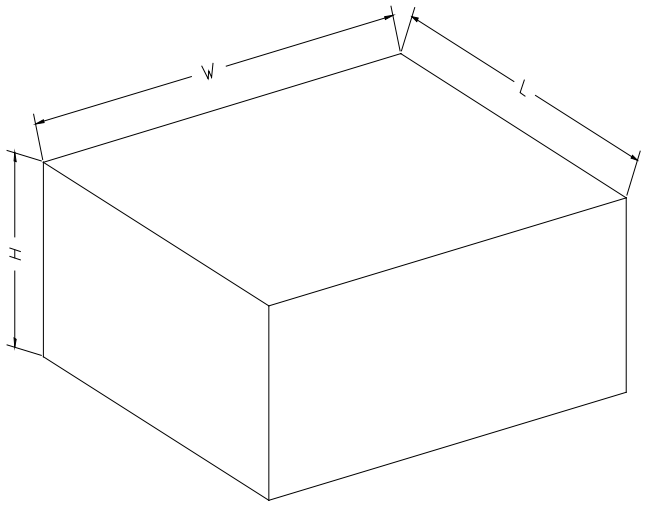
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TLGA-3×5-22L	13"	12.4	3.25	5.25	1.00	4.0	8.0	2.0	12.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002