SGM25063
10-Channel Load Switch with I²C Control

GENERAL DESCRIPTION

The SGM25063 is a five inputs and ten outputs highly integrated load switch. Each input can support 2 channel outputs: OUTxA and OUTxB which are independently controlled by I²C.

The device contains 10 N-MOSFETs that can operate input 1, 3 positive voltage and input 2, 4, 5 negative voltage with low R_{DSON}.

The switch can be controlled by I²C signal directly. Through the I²C interface, it can control the register to set the commands, so as to control the on/off, quick output discharge, rise time and power sequence of the load switch.

The SGM25063 is available in a Green WLCSP-2.15×1.65-20B package.

TYPICAL APPLICATION

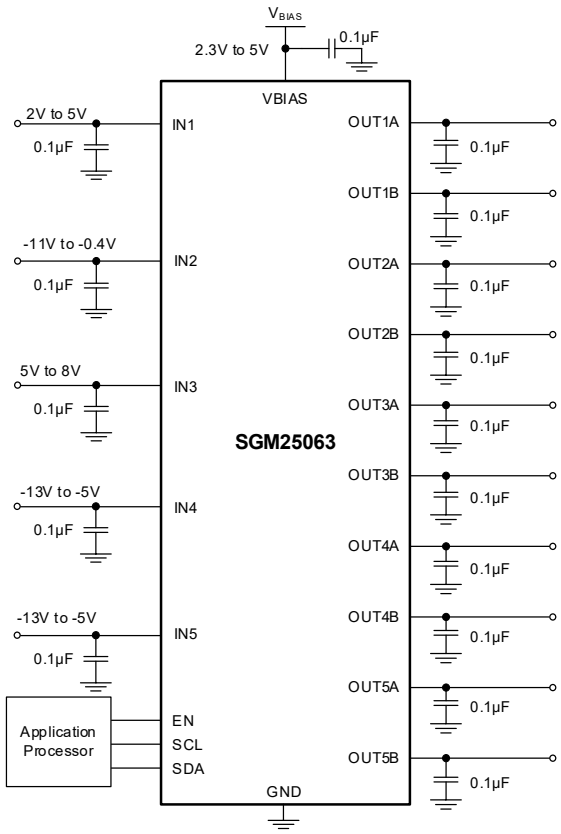


Figure 1. Typical Application Circuit

FEATURES

- **Integrated 10-Channel Load Switch**
- **V_{BIAS} Input Voltage Operating Range: 2.3V to 5V**
- **OUTxA, OUTxB Independent Control**
- **I²C Serial Control to Program Load Switch On/Off, QOD, Rise Time & Power Sequence**
- **Low Power Consumption:**
  - **On State: I_{BIAS_ON2} = 146μA (TYP)**
  - **Off State: I_{BIAS_OFF} = 0.2μA (TYP)**
- **Low On-Resistance:**
  - **Channel 1x: 19mΩ (TYP)**
  - **Channel 2x: 28mΩ (TYP)**
  - **Channel 3x: 53mΩ (TYP)**
  - **Channel 4x: 180mΩ (TYP)**
  - **Channel 5x: 180mΩ (TYP)**
- **Thermal Latch Off**
- **Available in a Green WLCSP-2.15×1.65-20B Package**

APPLICATIONS

Battery-Powered Device
Smartphones, Tablets
Cameras, DVRs, STB and Camcorders

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM25063	WLCSP-2.15×1.65-20B	-40℃ to +85℃	SGM25063YG/TR	25063 XXXXX XX#XX	Tape and Reel, 3000

Green (RoHS & HSF): We define "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances.

ABSOLUTE MAXIMUM RATINGS

IN1, OUT1A, OUT1B, VBIAS ..... -0.3V to 6V
EN, SDA, SCL ..... -0.3V to 6V
IN2, OUT2A, OUT2B ..... -12V to 0.3V
IN3, OUT3A, OUT3B ..... -0.3V to 9V
IN4, OUT4A, OUT4B, IN5, OUT5A, OUT5B ..... -14V to 0.3V
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
Package Thermal Resistance
WLCSP-2.15×1.65-20B, θ_{JA} ..... 44.1℃/W
WLCSP-2.15×1.65-20B, θ_{JB} ..... 12.9℃/W
WLCSP-2.15×1.65-20B, θ_{JC} ..... 18.8℃/W
ESD Susceptibility (1) (2)
HBM ..... ±4000V
CDM ..... ±1000V

NOTES:

1. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.

2. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

RECOMMENDED OPERATING CONDITIONS

CH1 Input Supply Voltage Range ..... 2V to 5V
CH2 Input Supply Voltage Range ..... -11V to -0.4V
CH3 Input Supply Voltage Range ..... 5V to 8V
CH4/5 Input Supply Voltage Range ..... -13V to -5V
Bias Voltage Range ..... 2.3V to 5V
Operation Junction Temperature Range ..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

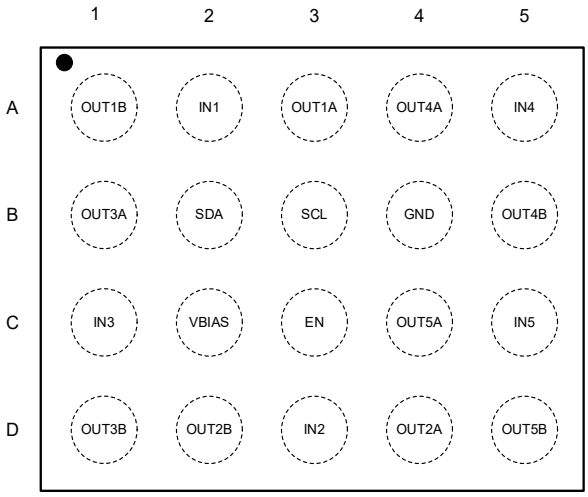
This integrated circuit can be damaged if ESD protections are not considered carefully. It recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

We reserve the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

(TOP VIEW)



WLCSP-2.15×1.65-20B

PIN DESCRIPTION

PIN	NAME	TYPE	FUNCTION
A1	OUT1B	O	Load Switch 1B Output.
A2	IN1	I	Load Switch 1 Supply Input.
A3	OUT1A	O	Load Switch 1A Output.
A4	OUT4A	O	Load Switch 4A Output.
A5	IN4	I	Load Switch 4 Supply Input.
B1	OUT3A	O	Load Switch 3A Output.
B2	SDA	I/O	I²C Data Signal. Once SDA keeps low for more than 25ms, SGM25063 will reset.
B3	SCL	I	I²C Clock Signal. Once SCL keeps low for more than 25ms, SGM25063 will reset.
B4	GND	G	Ground Pin.
B5	OUT4B	O	Load Switch 4B Output.
C1	IN3	I	Load Switch 3 Supply Input.
C2	VBIAS	I	System Supply Input.
C3	EN	I	Enable Logic. Internal 580kΩ pull-down resistor, this pin can be floating if not required.
C4	OUT5A	O	Load Switch 5A Output.
C5	IN5	I	Load Switch 5 Supply Input.
D1	OUT3B	O	Load Switch 3B Output.
D2	OUT2B	O	Load Switch 2B Output.
D3	IN2	I	Load Switch 2 Supply Input.
D4	OUT2A	O	Load Switch 2A Output.
D5	OUT5B	O	Load Switch 5B Output.

NOTE: I = Input, O = Output, I/O = Input or Output, G = Ground.

ELECTRICAL CHARACTERISTICS

(V_{IN1} = 2.8V, V_{IN2} = -4.8V, V_{IN3} = 6.5V, V_{IN4} = V_{IN5} = -10.5V, T_A = -40℃ to +85℃, V_{BIAS} = 3.5V, C_{BIAS} = 1μF. Typical values are at T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
VBIAS							
VBIAS Voltage Range	V_{BIAS}			2.3	3.5	5	V
VBIAS Rising Threshold	V_{BIASR}			2.1	2.15	2.25	V
VBIAS Falling Threshold	V_{BIASF}			1.9	2.05	2.1	V
VBIAS Current	I_{BIAS_ON1}	V_{EN} = high and enable chip by I²C, OUTxA or OUTxB on	T_A = +25℃		105	145	μA
			T_A = -40℃ to +85℃			160	
	I_{BIAS_ON2}	V_{EN} = high and enable chip by I²C, OUTxA and OUTxB on	T_A = +25℃		146	206	
			T_A = -40℃ to +85℃			220	
	I_{BIAS_OFF}	V_{IN} = floating, EN = low, V_{BIAS} = 2.3V to 5V	T_A = +25℃		0.2	1.2	
			T_A = -40℃ to +85℃			1.5	
Supply Current							
VIN Leakage Current	I_{LEAK_CH1}	V_{EN} = high and enable chip by I²C, OUT1A or OUT1B on, V_{IN1} = 2V to 5V	T_A = +25℃			9	μA
			T_A = -40℃ to +85℃			11	
	I_{LEAK_CH2}	V_{EN} = high and enable chip by I²C, OUT1A or OUT1B on, V_{IN2} = -11V to -0.4V	T_A = +25℃			15	
			T_A = -40℃ to +85℃			18	
	I_{LEAK_CH3}	V_{EN} = high and enable chip by I²C, OUT1A or OUT1B on, V_{IN3} = 5V to 8V	T_A = +25℃			7	
			T_A = -40℃ to +85℃			9	
	I_{LEAK_CH4}	V_{EN} = high and enable chip by I²C, OUT1A or OUT1B on, V_{IN4} = -13V to -5V	T_A = +25℃			24	
			T_A = -40℃ to +85℃			28	
	I_{LEAK_CH5}	V_{EN} = high and enable chip by I²C, OUT1A or OUT1B on, V_{IN5} = -13V to -5V	T_A = +25℃			24	
			T_A = -40℃ to +85℃			28	
Continuous Current (1)	I_{CH1}	V_{BIAS} = 2.3V to 5V, V_{IN1} = 2V to 5V		1.5			A
	I_{CH2}	V_{BIAS} = 2.3V to 5V, V_{IN2} = -11V to -0.4V		1.5			
	I_{CH3}	V_{BIAS} = 2.3V to 5V, V_{IN3} = 5V to 8V		300			mA
	I_{CH4}	V_{BIAS} = 2.3V to 5V, V_{IN4} = -13V to -5V		200			
	I_{CH5}	V_{BIAS} = 2.3V to 5V, V_{IN5} = -13V to -5V		200			
Short-Circuit							
Short-Circuit Protection Time (1)	t_{CH1_SC}	OUT1A/1B short to GND			20		ms
	t_{CH2_SC}	OUT2A/2B short to GND			25		
	t_{CH3_SC}	OUT3A/3B short to GND			28		
	t_{CH4_SC}	OUT4A/4B short to GND			28		
	t_{CH5_SC}	OUT5A/5B short to GND			28		
Current Limit							
Current Limit during Soft-Start (1)	I_{CH1_CL}	OUT1A/1B short to GND		4		50	mA
	I_{CH2_CL}	OUT2A/2B short to GND		5		160	
	I_{CH3_CL}	OUT3A/3B short to GND		4		110	
	I_{CH4_CL}	$C_{OUT4A/4B}$ = 10μF		5		80	
	I_{CH5_CL}	$C_{OUT5A/5B}$ = 10μF		5		80	

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN1} = 2.8V, V_{IN2} = -4.8V, V_{IN3} = 6.5V, V_{IN4} = V_{IN5} = -10.5V, T_A = -40℃ to +85℃, V_{BIAS} = 3.5V, C_{BIAS} = 1μF. Typical values are at T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Resistance							
IN to OUT On-Resistance	R_{CH1}	V_{IN1} = 2V to 5V, I_{OUT} = 1.5A	T_A = +25℃		19	28	mΩ
			T_A = -40℃ to +85℃			35	
	R_{CH2}	V_{IN2} = -11V to -0.4V, I_{OUT} = 1.5A	T_A = +25℃		28	40	
			T_A = -40℃ to +85℃			50	
	R_{CH3}	V_{IN3} = 5V to 8V, I_{OUT} = 200mA	T_A = +25℃		53	64	
			T_A = -40℃ to +85℃			80	
	R_{CH4}	V_{IN4} = -13V to -5V, I_{OUT} = 30mA	T_A = +25℃		180	210	
			T_A = -40℃ to +85℃			265	
	R_{CH5}	V_{IN5} = -13V to -5V, I_{OUT} = 30mA	T_A = +25℃		180	210	
			T_A = -40℃ to +85℃			265	
EN							
EN Input Voltage High	V_{ENH}			0.90			V
EN Input Voltage Low	V_{ENL}					0.35	V
Internal EN Pull Down Resistance	R_{EN}				580		kΩ
Output Auto Discharge Resistance	R_{DIS1}	EN = high, I²C disable, I_{DIS} = 10mA		90	115	140	Ω
	R_{DIS2}	EN = high, I²C disable, I_{DIS} = 10mA		40	65	85	
	R_{DIS3}	EN = high, I²C disable, I_{DIS} = 1mA		450	535	620	
	R_{DIS45}	EN = high, I²C disable, I_{DIS} = 10mA		45	67	90	
Output Auto Discharge Time (1)	t_{DIS1}	V_{IN1} = 2V to 5V, I_{OUT} = 0mA, C_{OUT} = 2 × 10uF, 90%V_{OUT} to 10%V_{OUT}				10	ms
	t_{DIS2}	V_{IN2} = -11V to -0.4V, I_{OUT} = 0mA, C_{OUT} = 2 × 10uF, 90%V_{OUT} to 10%V_{OUT}				10	
	t_{DIS3}	V_{IN3} = 5V to 8V, I_{OUT} = 0mA, C_{OUT} = 1 × 10uF, 90%V_{OUT} to 10%V_{OUT}				10	
	t_{DIS45}	$V_{IN4/5}$ = -13V to -5V, I_{OUT} = 0mA, C_{OUT} = 1 × 10uF, 90%V_{OUT} to 10%V_{OUT}				10	
SCL/SDA							
SCL/SDA Input Voltage High	V_{I2CH}			0.90			V
SCL/SDA Input Voltage Low	V_{I2CL}					0.40	V
SDA Logic Low Output	V_{OL}	3mA sink current				0.3	V
SCL/SDA Leakage Current	I_{I2C}	V_{EN} = 0V and V_{SCL} = V_{SDA} = V_{BIAS} or V_{SCL} = V_{SDA} = 0V			0.01	1	μA
SCL Clock Frequency	f_{SCL}					1	MHz
Thermal Shutdown							
Thermal Shutdown Temperature	T_{SD}				140		℃
Thermal Shutdown Hysteresis	T_{HYS}				10		℃

NOTE: 1. This parameter is guaranteed by design and characterization; not production tested.

TIMING CHARACTERISTICS

(C_{BIAS} = 1μF, V_{BIAS} = 3.5V, V_{IN1} = 2.8V, V_{IN2} = -4.8V, V_{IN3} = 6.5V, V_{IN4} = V_{IN5} = -10.5V, T_A = -40℃ to +85℃. Typical values are at T_A = +25℃, unless otherwise noted)

PARAMETERS	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Turn-On Delay (1)	t_{D_ON}	I²C enable to V_{OUT} start to rise with default rise time, C_{OUT} = open	CH1, CH3		25	70	μs
			CH4, CH5		40	90	
Turn-Off Delay (1)	t_{D_OFF}	I²C disable to V_{OUT} start to fall C_{OUT} = open, I_{OUT} = 1mA			4	20	μs

NOTE: 1. t_{D_ON}/t_{D_OFF} are defined in Figure 2.

TIMING DIAGRAM

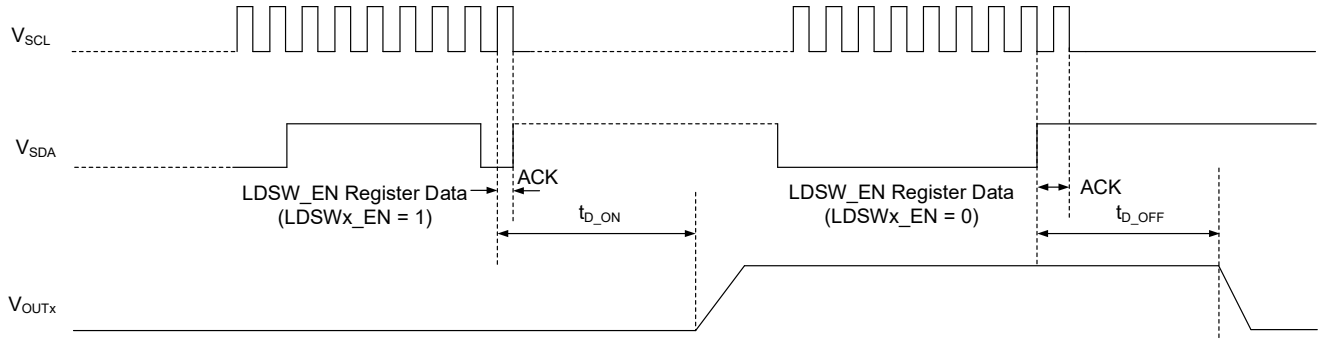


Figure 2. Timing Definition

I²C Mode Timing

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
SCL Clock Frequency	f_{SCL}	0.1		1	MHz
Bus Free Time Between a STOP and START Condition	t_{BUF}	1.3			μs
Hold Time (Repeated) START Condition	$t_{HD:STA}$	0.6			μs
Low Period of SCL Clock	t_{LOW}	1.3			μs
High Period of SCL Clock	t_{HIGH}	0.6			μs
Setup Time for a Repeated START Condition	$t_{SU:STA}$	0.6			μs
Data Hold Time	$t_{HD:DAT}$			0.9	μs
Data Setup Time	$t_{SU:DAT}$	100			ns
Data Hold Time2	t_R	20 + 0.1C_B (1)		300	ns
Data Hold Time2	t_F	20 + 0.1C_B		300	ns
Setup Time for STOP Condition	$t_{SU:STO}$	0.6			μs

NOTE: 1: C_B = total capacitance of one bus line in pF.

I²C Mode Timing Diagram

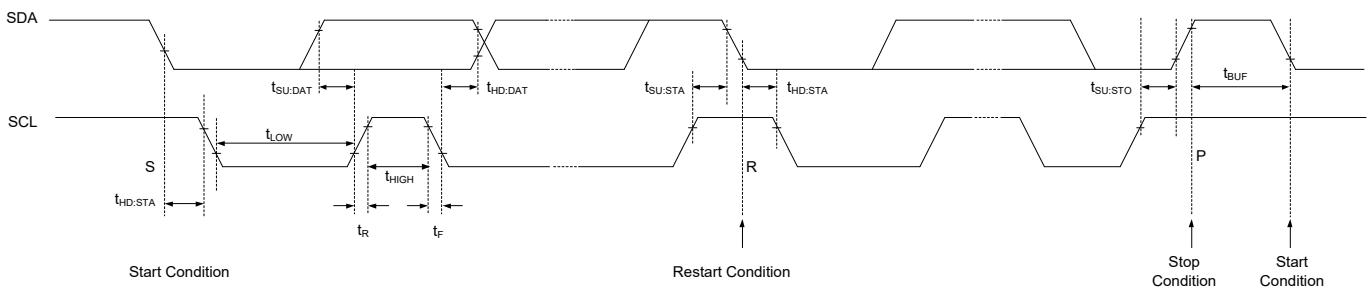
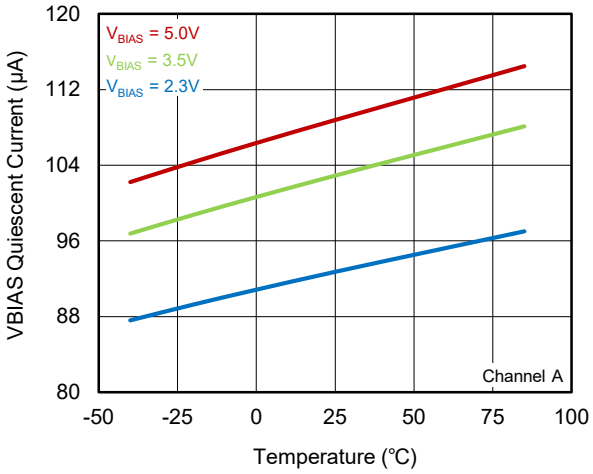


Figure 3. I²C Mode Timing Diagram

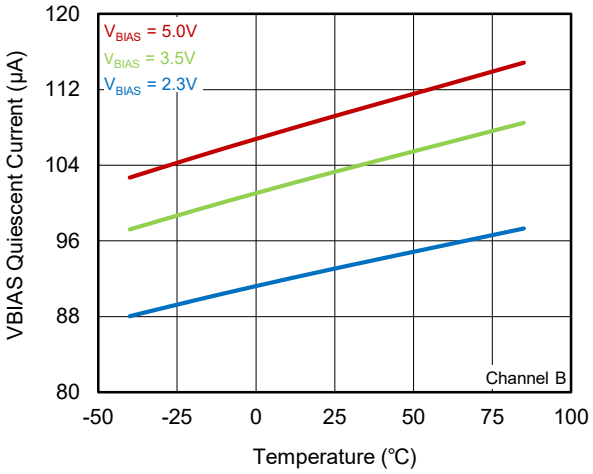
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = -40℃ to +85℃, unless otherwise noted.

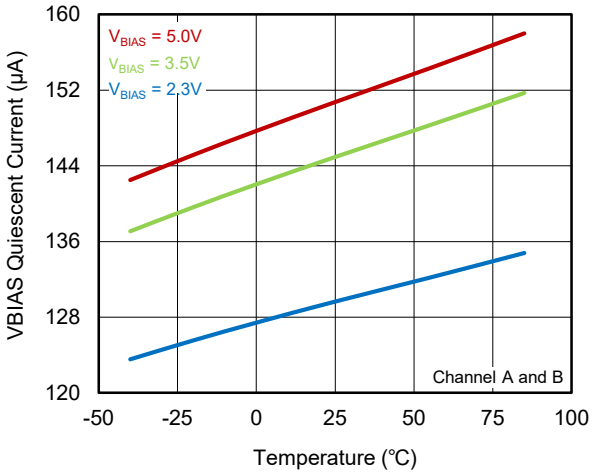
VBIAS Quiescent Current vs. Temperature



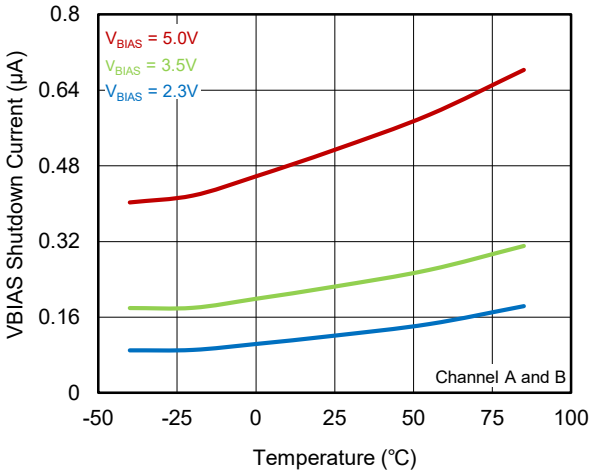
VBIAS Quiescent Current vs. Temperature



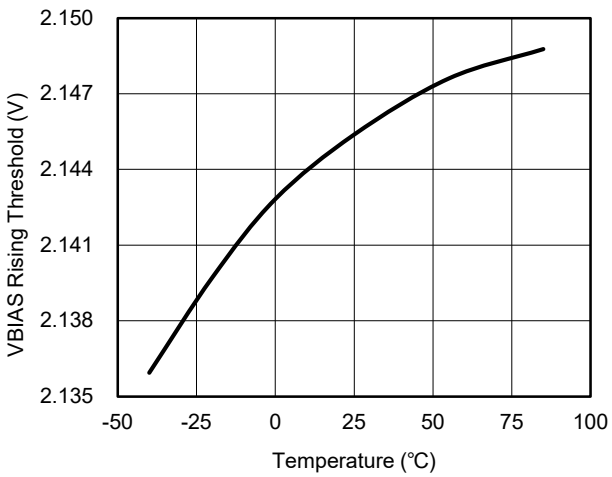
VBIAS Quiescent Current vs. Temperature



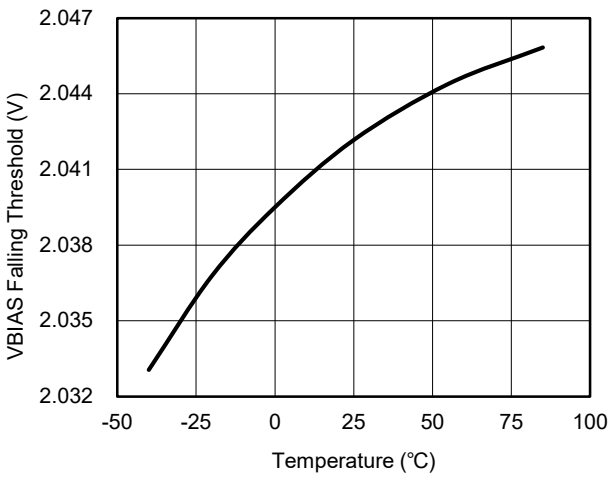
VBIAS Shutdown Current vs. Temperature



VBIAS Rising Threshold vs. Temperature



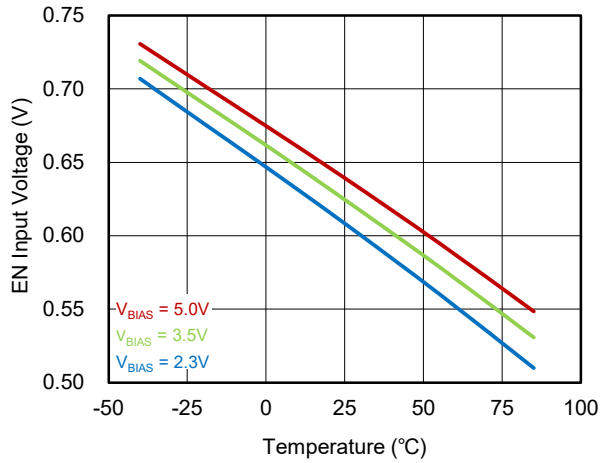
VBIAS Falling Threshold vs. Temperature



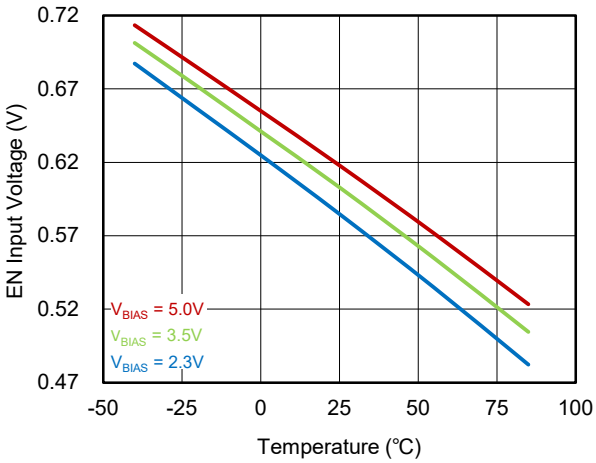
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = -40℃ to +85℃, unless otherwise noted.

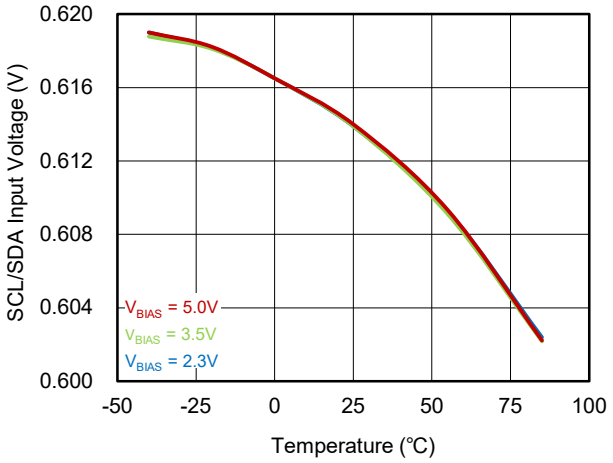
EN Input Voltage vs. Temperature (High)



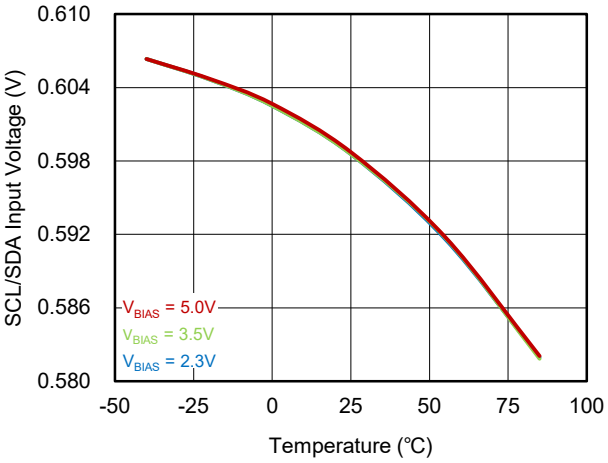
EN Input Voltage vs. Temperature (Low)



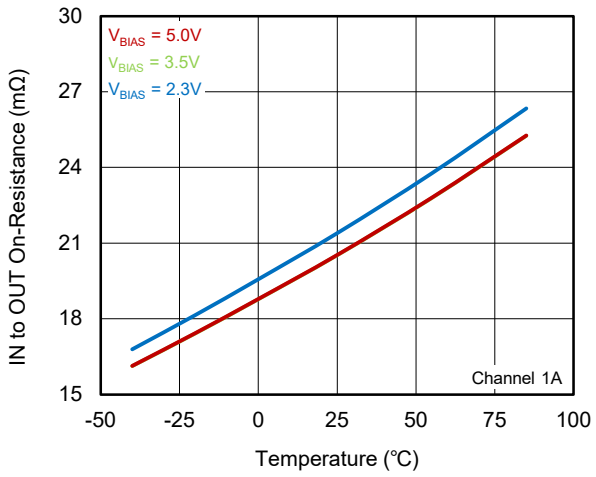
SCL/SDA Input Voltage vs. Temperature (High)



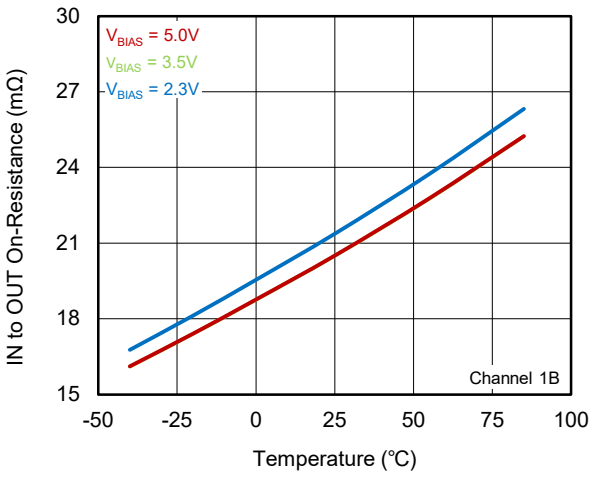
SCL/SDA Input Voltage vs. Temperature (Low)



IN to OUT On-Resistance vs. Temperature



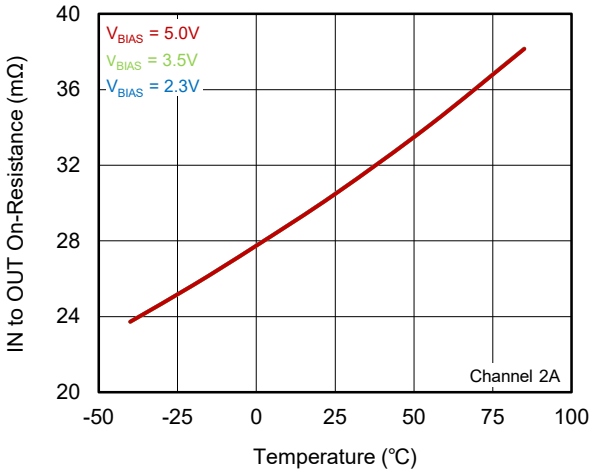
IN to OUT On-Resistance vs. Temperature



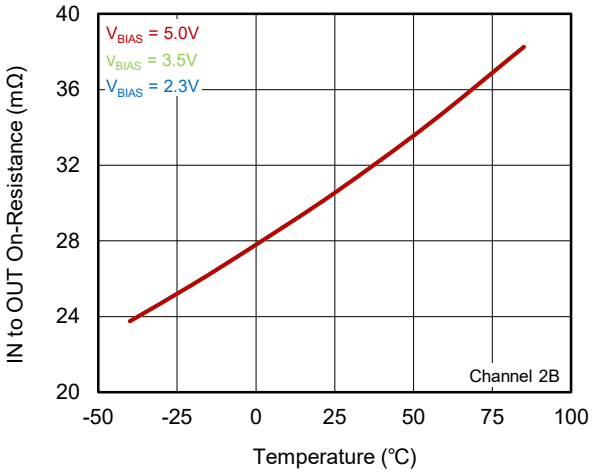
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = -40℃ to +85℃, unless otherwise noted.

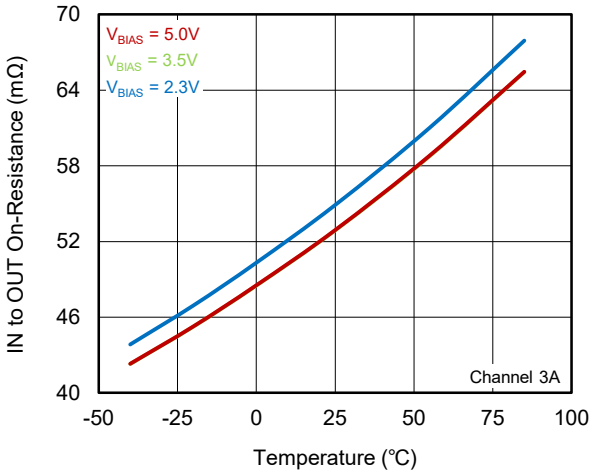
IN to OUT On-Resistance vs. Temperature



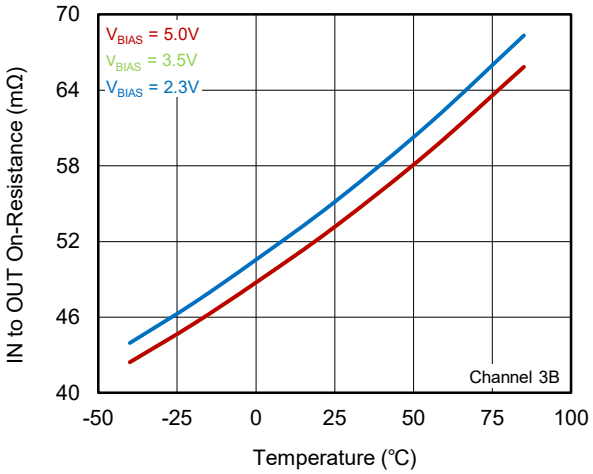
IN to OUT On-Resistance vs. Temperature



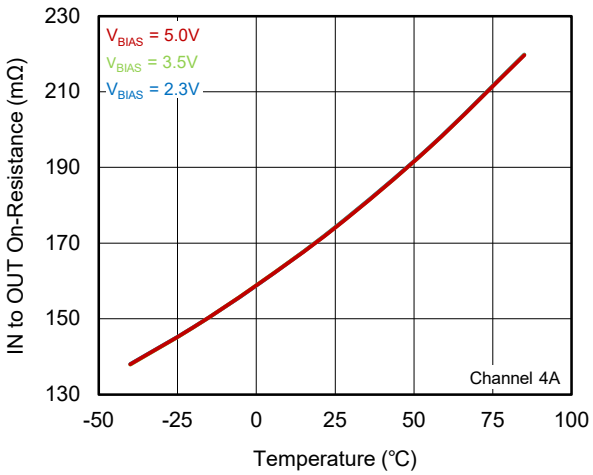
IN to OUT On-Resistance vs. Temperature



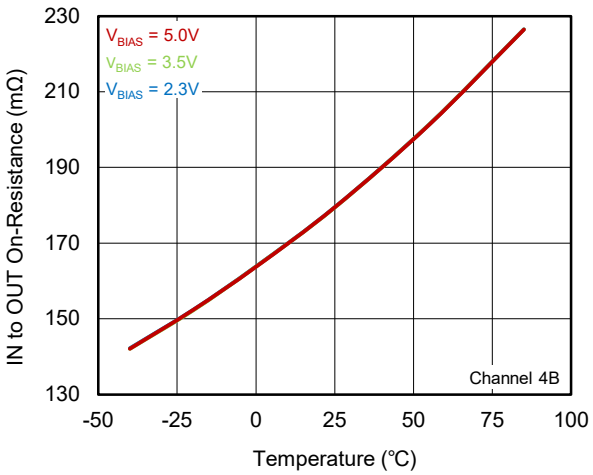
IN to OUT On-Resistance vs. Temperature



IN to OUT On-Resistance vs. Temperature



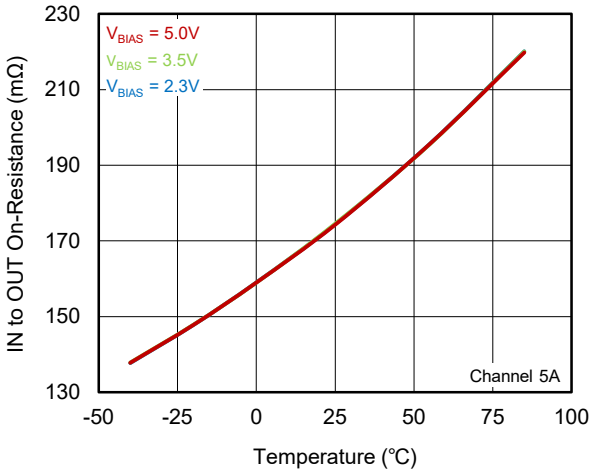
IN to OUT On-Resistance vs. Temperature



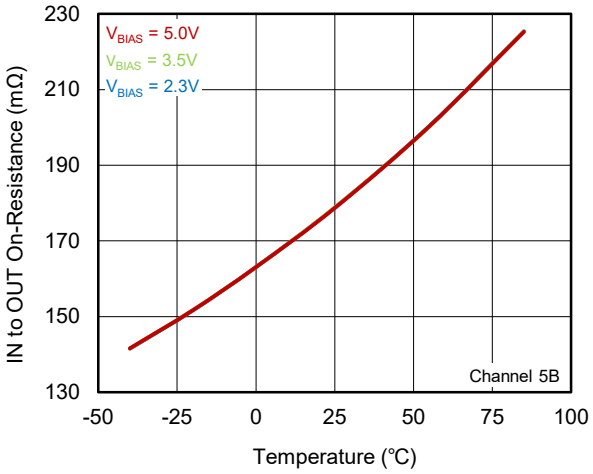
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = -40℃ to +85℃, unless otherwise noted.

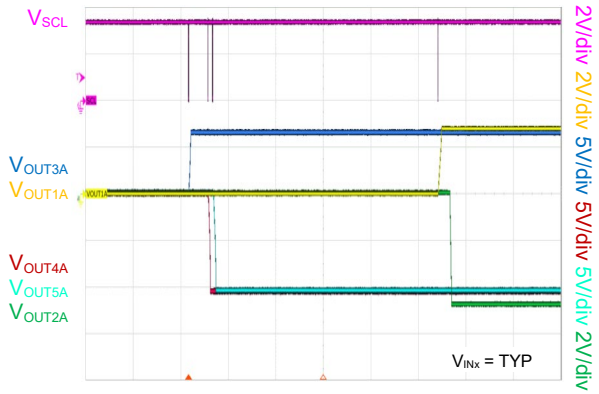
IN to OUT On-Resistance vs. Temperature



IN to OUT On-Resistance vs. Temperature

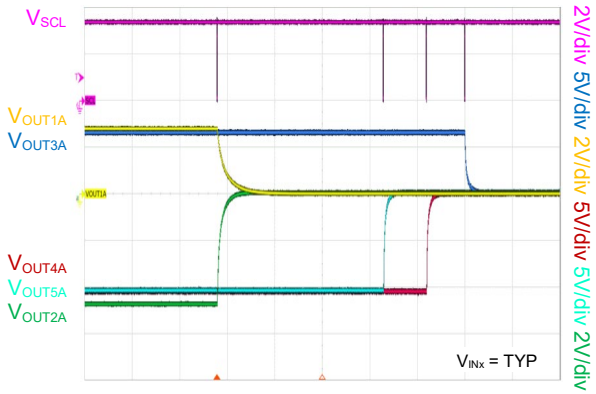


0x01: LDSWxA_EN = 1



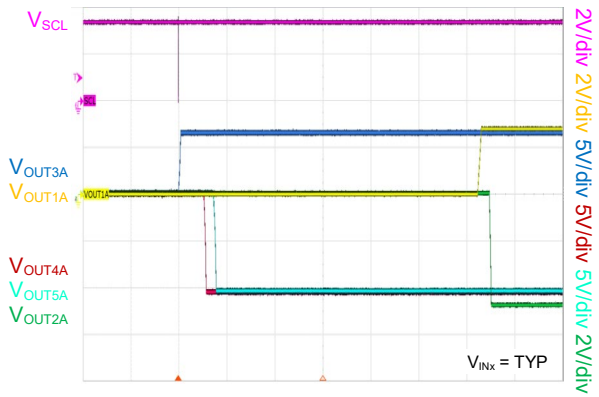
Time (20ms/div)

0x01: LDSWxA_EN = 0



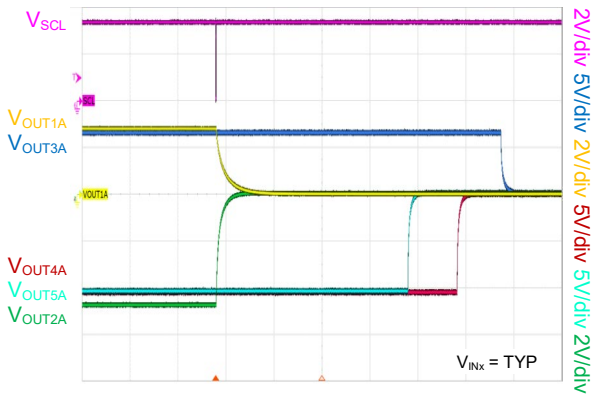
Time (10ms/div)

0x02: POWER_On_Seq_A_CTRL = 1



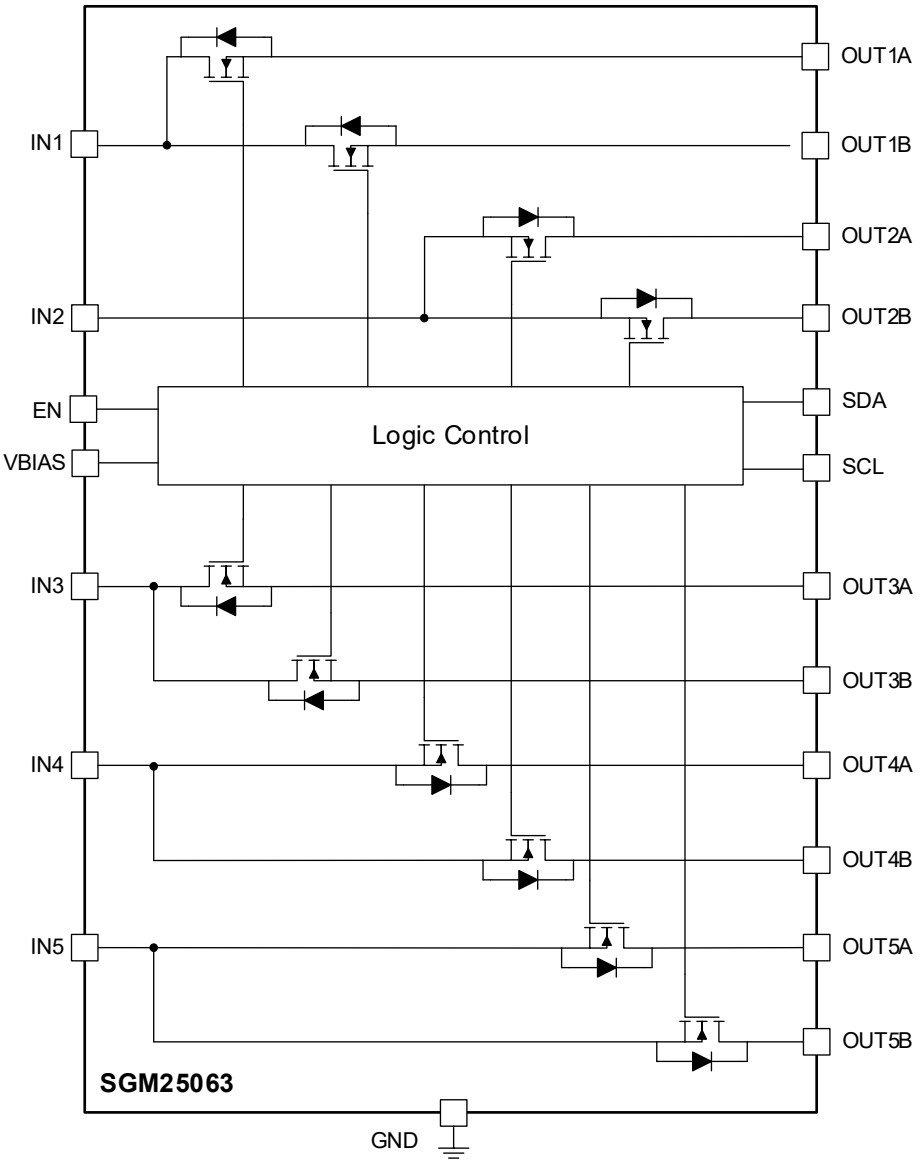
Time (20ms/div)

0x02: POWER_On_Seq_A_CTRL = 0



Time (10ms/div)

FUNCTIONAL BLOCK DIAGRAM



NOTE: The OUTx port has a fast turn-off discharge circuit. This function can be turned off by I²C command.

Figure 4. Block Diagram

DETAILED DESCRIPTION

The SGM25063 is a small size, 10-channel load switch which operates from input 1, 3 positive voltage and input 2, 4, 5 negative voltage with low R_{DSON}. Through the I²C interface, the register can be set by the command which controls the on/off, quick output discharge, rise time and customized power-up sequence and slot period.

On/Off Control

Turn-on and off of each channel can be controlled by an I²C register. There are two ways to set and control the LDSW by the I²C register when the EN control pin is active at high level.

- Setting the bit LDSWxx_EN = 1/0 in 0x01 register to enable/disable the corresponding channel respectively.
- Setting Power_On_Seq_A/B_CTRL in 0x02 register or Power_Off_Seq_A/B_CTRL in 0x03 register to enable the power-on/off sequence.

When V_{BIAS} is powered on and the EN pin is enabled, the device can be turned on/off through I²C even if the input voltage is 0V.

EN Pin

EN is the device enable control pin. High level is active. The default is pulled down to GND through a 580kΩ resistor. When the EN is driven high, the device is enabled and I²C is active. When the EN is driven low, the device is disabled. In this shutdown state, all the registers will be reset to their default values and I²C is invalid, so it cannot be written or read.

Input Capacitor

Turning on the N-MOSFET to charge the load capacitor will generate inrush current, which may lead to the decrease of V_{IN}. In order to prevent the drop, it is recommended to place a 0.1μF ceramic capacitor between the INx and GND pins. Higher capacitance values could further reduce the voltage drop.

Output Capacitor

It is recommended that the output capacitance between OUTx and GND should be at least 0.1μF. The capacitor should be placed near to the device pins. The capacitor prevents the VOUTx from falling below GND due to onboard parasitic inductance when the switch is turned off.

V_{BIAS} Power Supply

V_{BIAS} is the power supply to the inner circuit, including control logic, I²C, quick output discharge and charge pump. The support voltage range is from 2.3V to 5V. It is recommended to use ceramic capacitors of 0.1μF or larger.

Quick Output Discharge (QOD)

The QOD feature is available for each channel. The device has a QOD circuit which is not activated to discharge by default. When the output is shutdown, the resistor will be connected the OUTx and GND pins to discharge the output capacitor quickly and reduce the output pin voltage in a very short time. Setting LDSWxx_DIS related bits in 0x04/05 register can enable or disable QOD function.

Short-Circuit Protection Timer

The device will time the soft-start process, when the soft-start is not completed until the short-circuit protection timer expires, the device will shut down.

Thermal Shutdown

The SGM25063 features thermal shutdown circuitry. If the junction temperature exceeds +140℃ (TYP), the internal FETs latch off. In this shutdown state, all the registers will be reset to their default values, and I2C is invalid. QOD function is enable during thermal shutdown state. When the die temperature falls below +130℃ (TYP), recyle EN or VBIAS to re-power on.

I²C Data Communication

Bus Interface

I²C bus is 2 wire serial communication interface which is composed of SDA and SCL. SDA is the data line. SCL is the clock line. Both the SDA (open-drain) and SCL pins need to be pulled up through resistor. The micro-controller or DSP which generates the SCL pulses is usually used as a master device. SGM25063 is usually a slave device.

START and STOP Conditions

START condition is that SCL is high and a high to low transition on the SDA is generated by master. Similarly, a STOP is defined when SCL is high and SDA goes from low to high. START and STOP are always generated by a master. After a START and before a STOP the bus is considered busy.

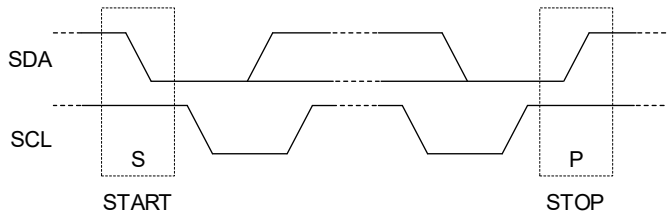


Figure 5. I²C Bus in START and STOP Conditions

DETAILED DESCRIPTION (continued)

Data Bit Transmission and Validity

The data bit (high or low) must remain stable on the SDA line during the high period of the clock. Only when the clock (SCL) is at a low level, the state of SDA will change. One clock pulse transmits one bit data. Bit transfer in I²C is shown in Figure 6.

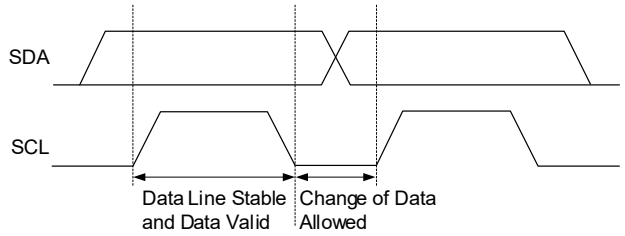


Figure 6. I²C Bus Bit Transfer

Byte Format

Data is transmitted in 8-bit packets (one byte at a time). There is no limit on the number of bytes in a transaction. In each data packet, 8 bits are sent in sequence, and the most significant bit (MSB) takes priority. The 8 data bits must be followed by an acknowledge (or not acknowledge) bit. This bit informs the transmitter whether the receiver is ready to proceed with the next byte or not. Figure 7 shows the byte transfer process with I²C interface.

Acknowledge (ACK) and Not-Acknowledge (NCK)

The acknowledge takes place following every byte. The acknowledge bit allows the receiver to signal the transmitter that the byte was successfully received and another byte may be sent. All clock pulses, including the acknowledge 9th clock pulse, are generated by the master. The transmitter releases the SDA line during the acknowledge clock pulse, so the receiver can pull the SDA line low and it remains stable low during the high period of this clock pulse. When SDA remains high during the 9th clock pulse, this is the not-acknowledge signal. Then the master can generate a STOP to abort the transmission or a repeated START to start a new transmission.

Slave Address and Data Direction Bit

A slave address is sent after the start. This address is 7 bits long followed by the 8th bit as a data direction bit (bit R/W). A zero indicates a transmission (Write) and a one indicates a data request (Read).

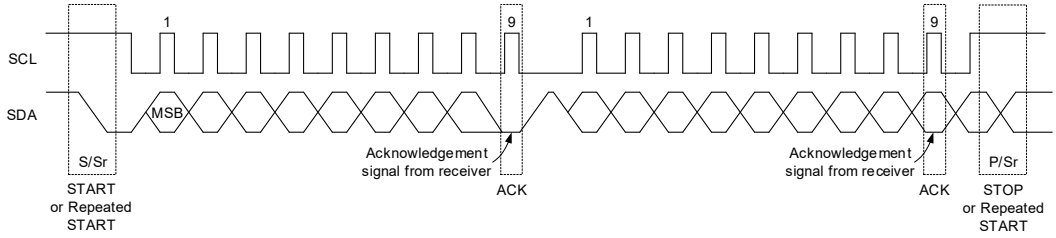


Figure 7. Byte Transfer Process

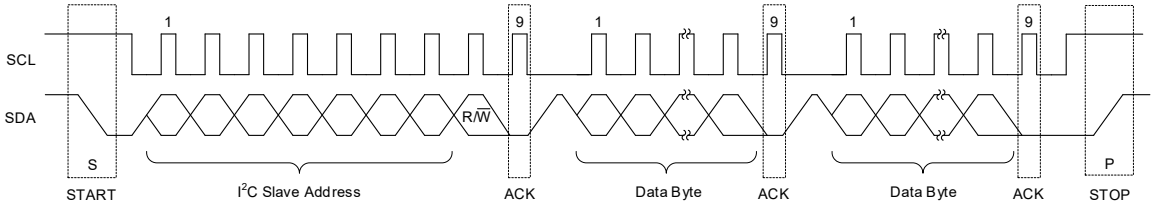


Figure 8. Data Transfer Transaction

DETAILED DESCRIPTION (continued)

Single-Read and Single-Write

Single-Write: If the master wants to write in the register, the third byte can be written directly as shown in Figure 9 for a single write data transfer. After receiving the ACK, master may issue a STOP condition to end the transaction or send the next register data, which will be written to the next address in a slave as multi-write. A STOP is needed after sending the last data.

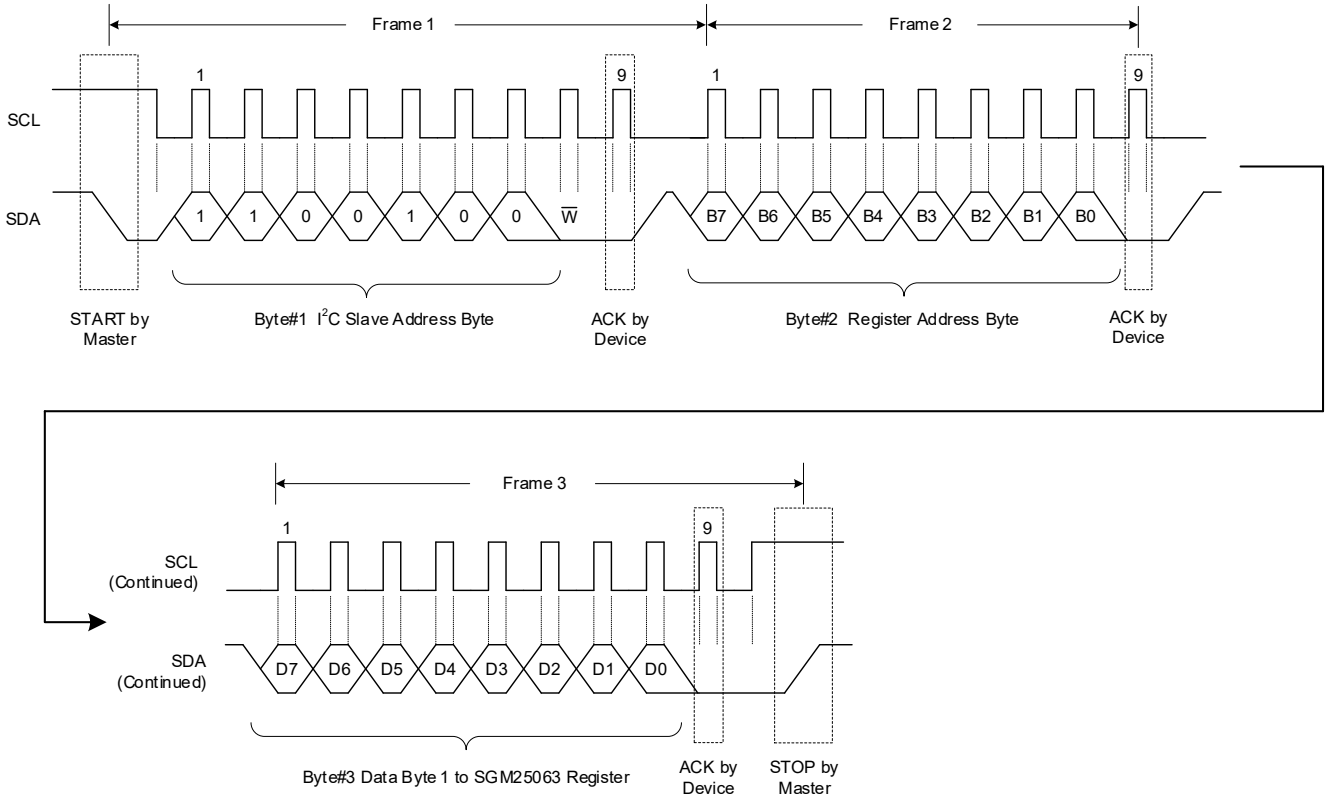


Figure 9. I²C Single-Writing Command Register

DETAILED DESCRIPTION (continued)

Single-Read: If the master wants to read a single register (Figure 10), it sends a new START condition along with device address with R/W bit = 1. After ACK is receiving, master reads the SDA line to receive the content of the register. Master replies with NCK to inform slave that no more data is needed (single read) or it can send an ACK to request for sending the next register content (multi-read). This can continue until an NCK is sent by master. In any case, the master must send a stop signal to end the transaction.

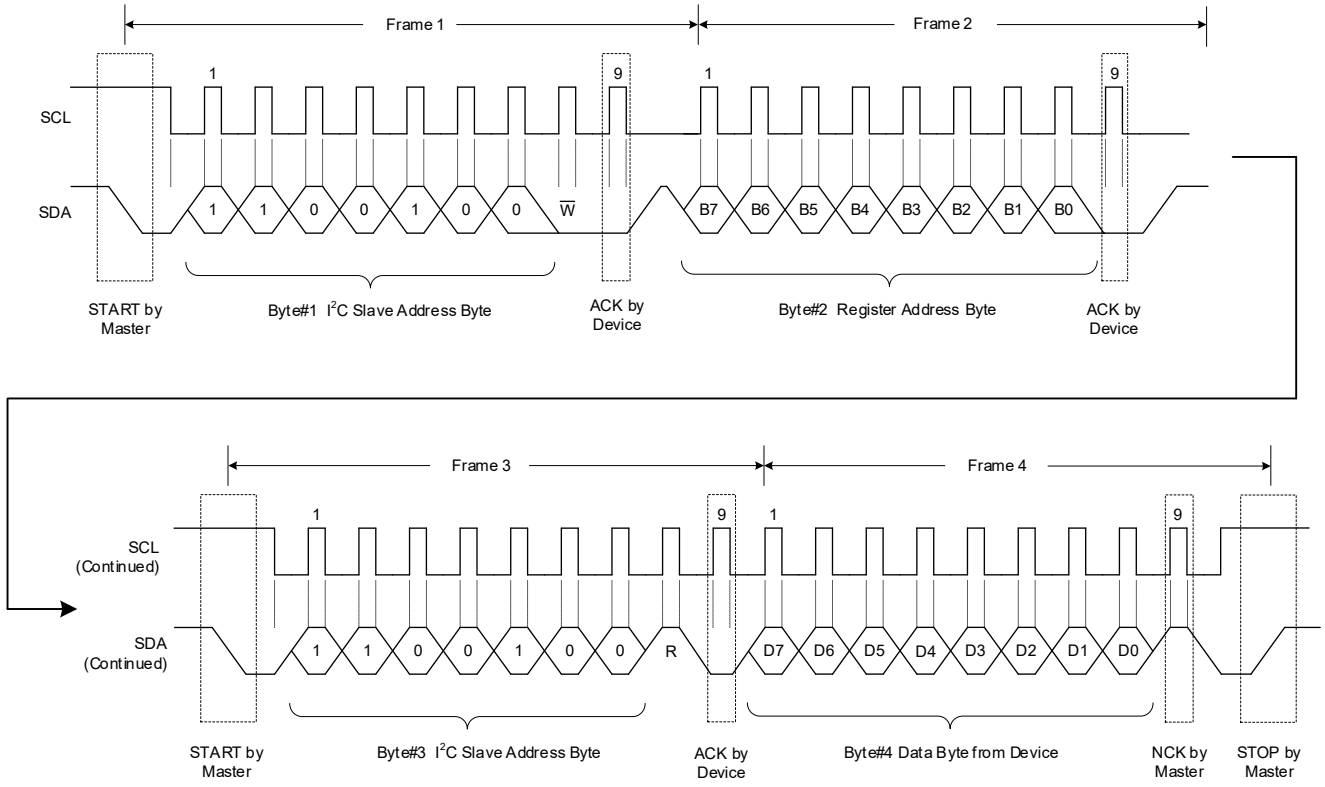


Figure 10. I²C Single-Reading Command Register

DETAILED DESCRIPTION (continued)

Multi-Write and Multi-Read

SGM25063 supports multi-write and multi-read.

Multi-Write: In the multi-write transaction, firstly write the chip address and command start address. Then the register data is sent and written to the command register addresses by the master byte by byte until a STOP occurs or a restart. In the multi-write, every new data byte sent by master is written to the next register of the device.

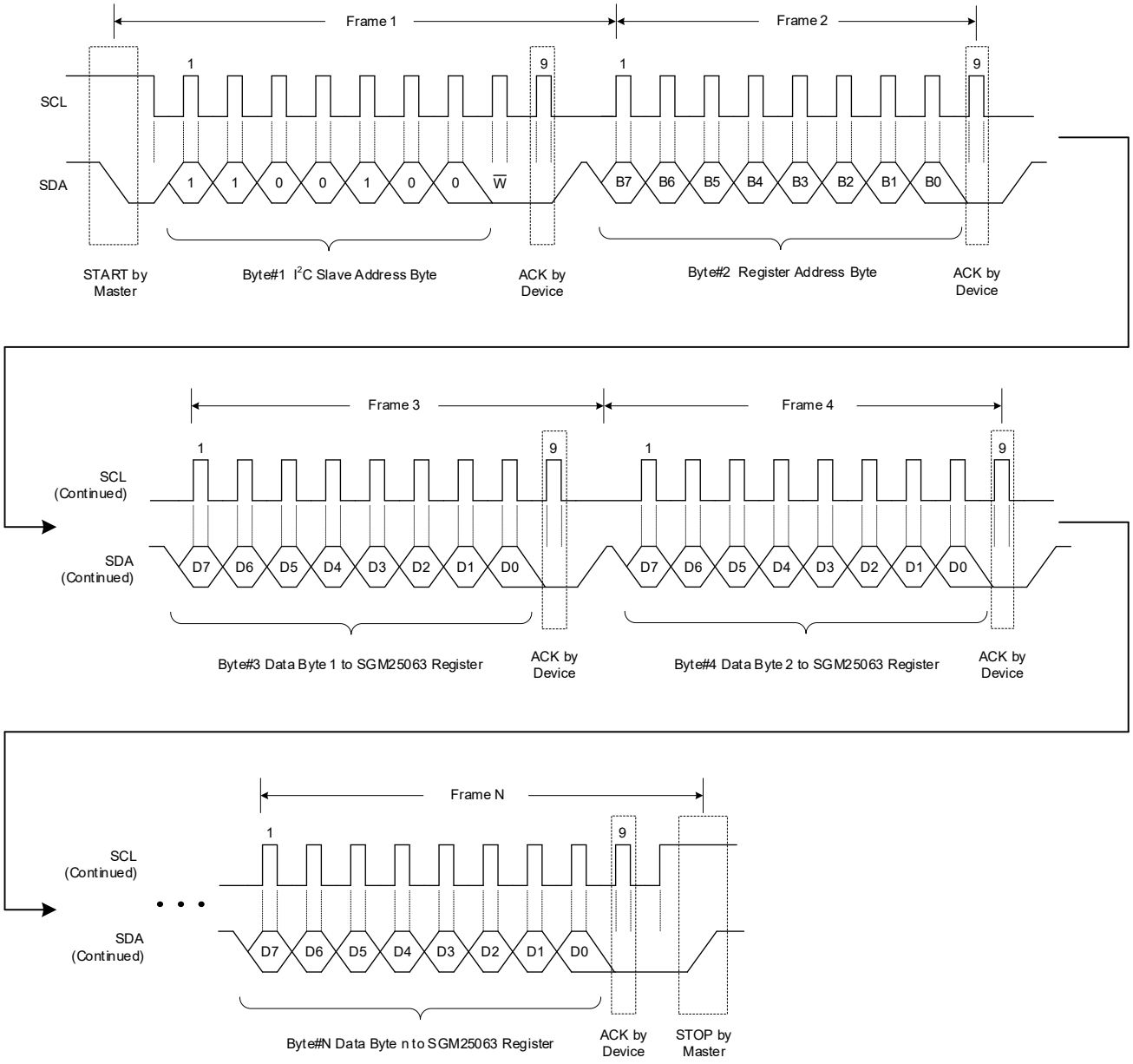


Figure 11. I²C Writing Command Register (Continuous)

DETAILED DESCRIPTION (continued)

Multi-Read: In the multi-read transaction, firstly write the chip address and command start address and then read the chip address. After that, the register dates are sent and read from the command start register address byte by byte until an NCK occurs following a STOP or a restart. In the multi-read, an ACK is sent to request for sending the next register content.

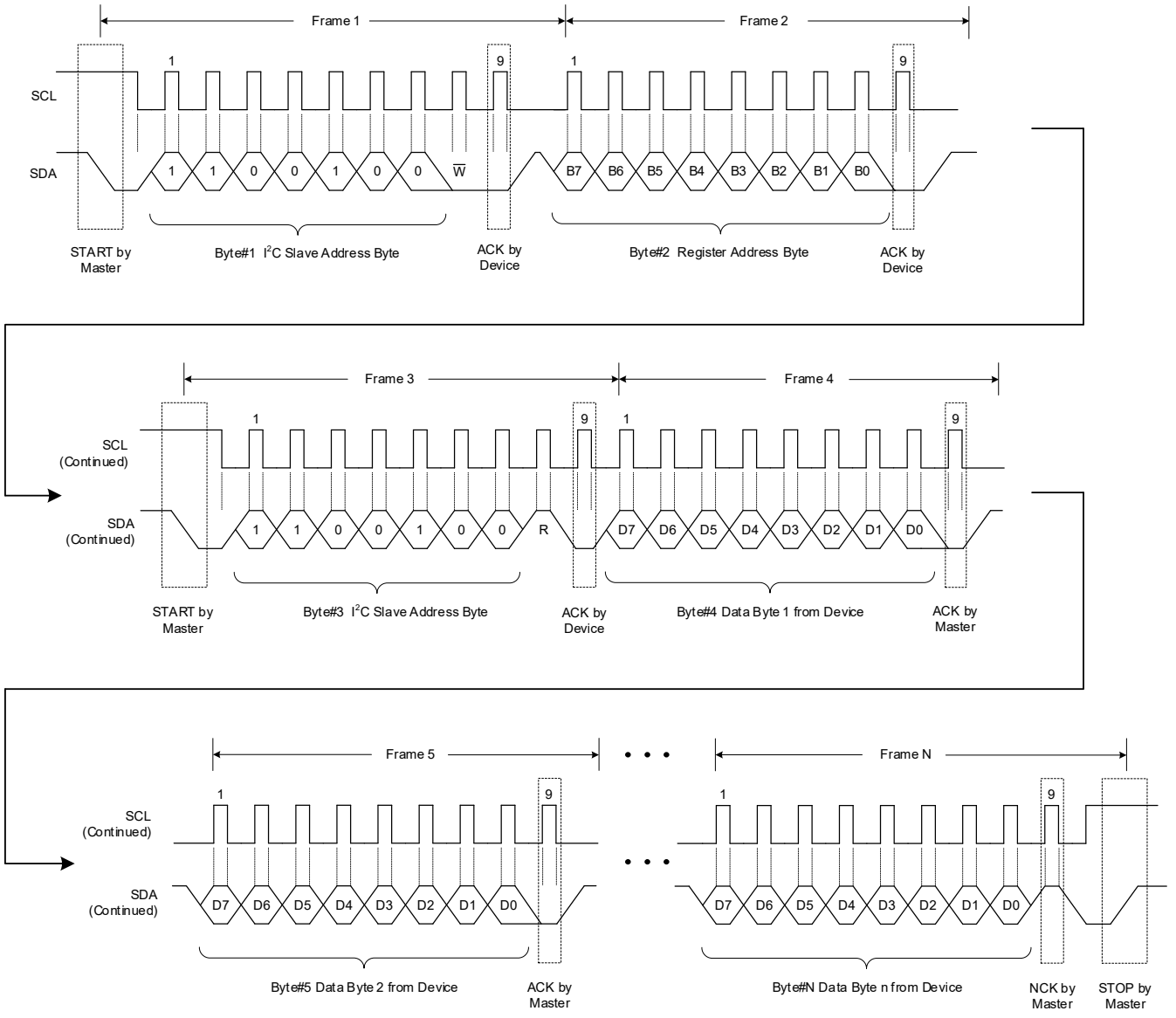


Figure 12. I²C Reading Command Register

REGISTER MAP

All registers are 8-bit and individual bits are named from D[0] (LSB) to D[7] (MSB).

I²C 7-Bit Slave Address of SGM25063: 0b1100 100 + W/R

R/W: Read/Write bit(s)
R: Read only bit(s)
R/W/C: Read/Write/Clear bit(s)

Table 1. Register Set Summary

ADDRESS (HEX)	NAME	R/W	DEFAULT	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
0x00	CHIPID	R	01000010	01000010							
0x01	LDSW_EN	R/W	00000000	LDSW5B_EN	LDSW5A_EN	LDSW4B_EN	LDSW4A_EN	LDSW3B_EN	LDSW3A_EN	LDSW1B_EN	LDSW1A_EN
0x02	LDSW_POWER_ON_SEQ	R/W/C	10101000	SEQ_DELAY_ON_CTRL51		SEQ_DELAY_ON_CTRL45		SEQ_DELAY_ON_CTRL34		Power_On_Seq_B_CTRL	Power_On_Seq_A_CTRL
0x03	LDSW_POWER_OFF_SEQ	R/W/C	10100000	SEQ_DELAY_OFF_CTRL15		SEQ_DELAY_OFF_CTRL54		SEQ_DELAY_OFF_CTRL43		Power_Off_Seq_B_CTRL	Power_Off_Seq_A_CTRL
0x04	LDSW_A_DIS	R/W	00011111	Reserved	Reserved	Reserved	LDSW5A_DIS	LDSW4A_DIS	LDSW3A_DIS	LDSW2A_DIS	LDSW1A_DIS
0x05	LDSW_B_DIS	R/W	00011111	Reserved	Reserved	Reserved	LDSW5B_DIS	LDSW4B_DIS	LDSW3B_DIS	LDSW2B_DIS	LDSW1B_DIS
0x06	LDSW_A_SF	R/W	01010100	LDSW5A_SF_CTRL		LDSW4A_SF_CTRL		LDSW3A_SF_CTRL		LDSW2A_SF_CTRL	LDSW1A_SF_CTRL
0x07	LDSW_B_SF	R/W	01010100	LDSW5B_SF_CTRL		LDSW4B_SF_CTRL		LDSW3B_SF_CTRL		LDSW2B_SF_CTRL	LDSW1B_SF_CTRL
0x08	LDSW_A_PG	R	00000000	Reserved	Reserved	Reserved	LDSW5A_PG	LDSW4A_PG	LDSW3A_PG	LDSW2A_PG	LDSW1A_PG
0x09	LDSW_B_PG	R	00000000	Reserved	Reserved	Reserved	LDSW5B_PG	LDSW4B_PG	LDSW3B_PG	LDSW2B_PG	LDSW1B_PG
0x0A	OT_FLAG	R	00000000	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	OT_FLAG
0x0B	A_SCP_FLAG	R	00000000	Reserved	Reserved	Reserved	5A_SCP_FLAG	4A_SCP_FLAG	3A_SCP_FLAG	2A_SCP_FLAG	1A_SCP_FLAG
0x0C	B_SCP_FLAG	R	00000000	Reserved	Reserved	Reserved	5B_SCP_FLAG	4B_SCP_FLAG	3B_SCP_FLAG	2B_SCP_FLAG	1B_SCP_FLAG

CHIPID

Register address: 0x00
Default = 0x42

REGISTER MAP (continued)

LDSW_EN

Register address: 0x01; R/W
Default = 0x00

Table 2. LDSW_EN Register Details

BITS	BIT NAME	DESCRIPTION	DEFAULT	TYPE
D[7]	LDSW5B_EN	LDSW5B Enable Control: **0 = Disable** 1 = Enable	0	R/W
D[6]	LDSW5A_EN	LDSW5A Enable Control: **0 = Disable** 1 = Enable	0	R/W
D[5]	LDSW4B_EN	LDSW4B Enable Control: **0 = Disable** 1 = Enable	0	R/W
D[4]	LDSW4A_EN	LDSW4A Enable Control: **0 = Disable** 1 = Enable	0	R/W
D[3]	LDSW3B_EN	LDSW3B Enable Control: **0 = Disable** 1 = Enable	0	R/W
D[2]	LDSW3A_EN	LDSW3A Enable Control: **0 = Disable** 1 = Enable	0	R/W
D[1]	LDSW1B_EN	LDSW1B Enable Control: **0 = Disable** 1 = Enable	0	R/W
D[0]	LDSW1A_EN	LDSW1A Enable Control: **0 = Disable** 1 = Enable	0	R/W

LDSW1x_EN and LDSW2x_EN (where x corresponds to either group A or group B channels) share the same enable control bit. When the register bit LDSW1x_EN transitions from 0 to 1, LDSW1x will start conducting first, and LDSW2x will start conducting after a delay of 2.5ms after LDSW1x is powered on. When the register bit LDSW1x_EN transitions from 1 to 0, both LDSW1x and LDSW2x will be turned off simultaneously. In the Power_On_Seq or Power_Off_Seq timing sequence, LDSW1x and LDSW2x are powered on and off according to the descriptions above too.

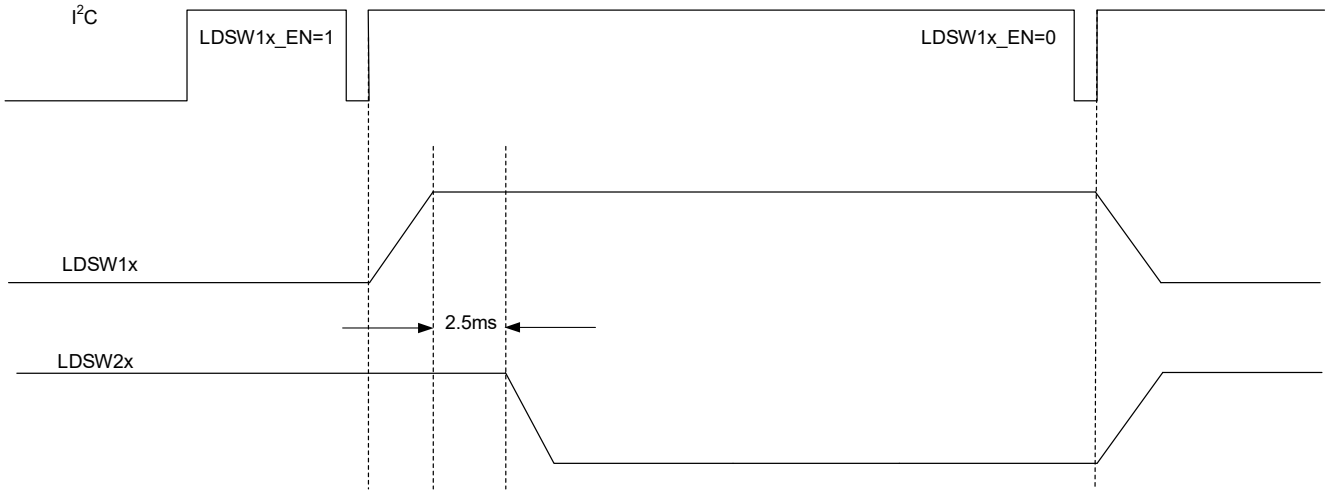


Figure 13. LDSW1x and LDSW2x Power On/Off Sequence

REGISTER MAP (continued)

LDSW_POWER_ON_SEQ

Register address: 0x02; R/W/C
Default = 0xA8

Table 3. LDSW_A_SF Register Details

BITS	NAME	DESCRIPTION	DEFAULT	TYPE
D[7:6]	SEQ_DELAY_ON_CTRL51	The delay time between LDSW 5 and LDSW 1 00 = 75ms 01= 85ms **10 = 95ms** 11 = 105ms	10	R/W
D[5:4]	SEQ_DELAY_ON_CTRL45	The delay time between LDSW 4 and LDSW 5 00 = 0ms 01 = 1ms **10 = 2ms** 11 = 4ms	10	R/W
D[3:2]	SEQ_DELAY_ON_CTRL34	The delay time between LDSW 3 and LDSW 4 00 = 4ms 01 = 6ms **10 = 8ms** 11 =10ms	10	R/W
D[1]	Power_On_Seq_B_CTRL	Power-on sequence enable control for the channels of group B **0 = Disable** 1 = Enable	0	W/C
D[0]	Power_On_Seq_A_CTRL	Power-on sequence enable control for the channels of group A **0 = Disable** 1 = Enable	0	W/C

When the Power_On_Seq_x_CTRL bit changes from 0 to 1, the x grpup will conduct sequentially according to the customized power on timing: LDSW3x → LDSW4x → LDSW5x → LDSW1x → LDSW2x. The interval time between adjacent channels is programmed with bits D[7:2] in 0x02 register. The starting point of channel delay time is the time from the previous channel soft-start finished point to the start of conduction of the next channel, see Figure 14. Note that, when the delay time between LDSW4x and LDSW5x is setted to 0ms, LDSW4x and LDSW5x start at the same time and channel 1 needs to be conducted after both channels 4 and 5 have completed soft-start.

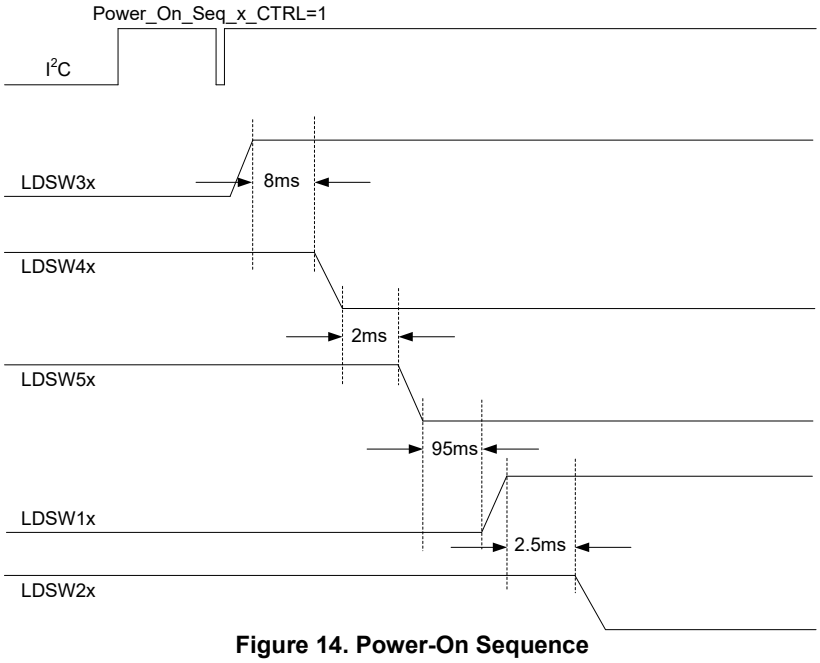


Figure 14. Power-On Sequence

During the power-on sequence, if any a channel triggers the soft-start short-circuit protection, the device will shut down. D[1:0] are write/clear bits.

REGISTER MAP (continued)

LDSW_POWER_OFF_SEQ

Register address: 0x03; R/W/C
Default = 0xA0

Table 4. LDSW_A_SF Register Details

BITS	NAME	DESCRIPTION	DEFAULT	TYPE
D[7:6]	SEQ_DELAY_OFF_CTRL15	The delay time between LDSW 5 and LDSW 1 00 = 25ms 01 = 30ms **10 = 35ms** 11 = 45ms	10	R/W
D[5:4]	SEQ_DELAY_OFF_CTRL54	The delay time between LDSW 4 and LDSW 5 00 = 0ms 01 = 6ms **10 = 9ms** 11 = 11ms	10	R/W
D[3:2]	SEQ_DELAY_OFF_CTRL43	The delay time between LDSW 3 and LDSW 4 **00 = 8ms** 01 = 10ms 10 = 12ms 11 = 14ms	00	R/W
D[1]	Power_Off_Seq_B_CTRL	Power-off sequence enable control for the channels of group B **0 = Disable** 1 = Enable	0	W/C
D[0]	Power_Off_Seq_A_CTRL	Power-off sequence enable control for the channels of group A **0 = Disable** 1 = Enable	0	W/C

When the Power_Off_Seq_x_CTRL bit changes from 0 to 1, the x grpup will turn off sequentially according to the customized power on timing: LDSW1x/LDSW2x → LDSW5x → LDSW4x → LDSW3x. The interval time between adjacent channels is programmed with bits D[7:2] in 0x03 register. The starting point of channel delay time is the time from the previous channel turn off point to the start of shutdown of the next channel, see Figure 15. D[1:0] are write/clear bits.

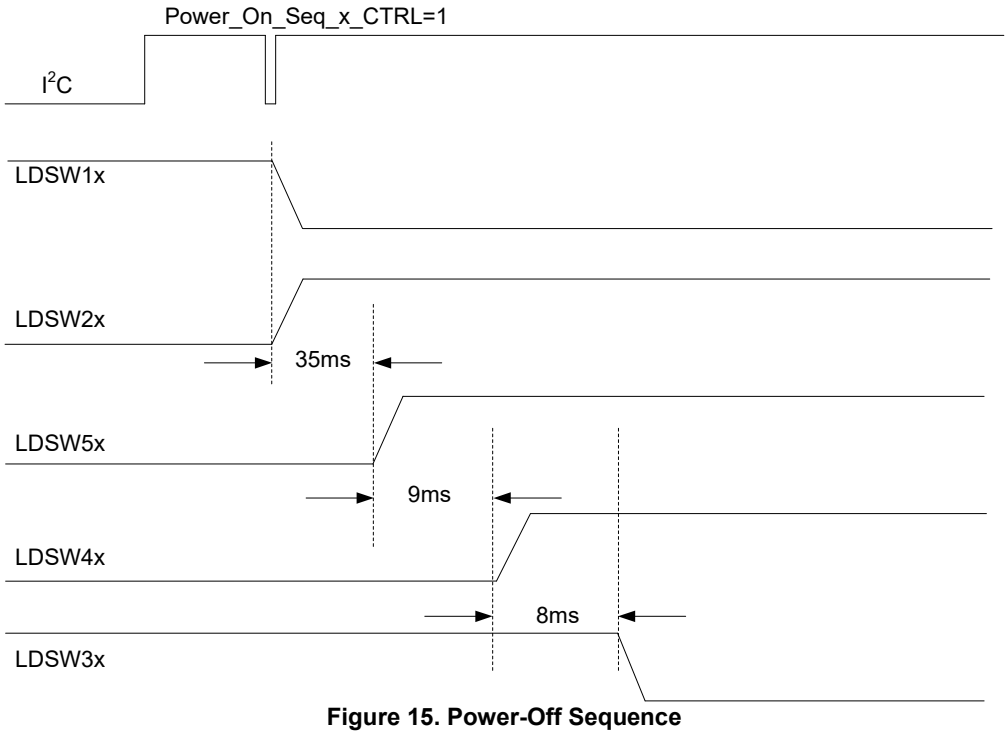


Figure 15. Power-Off Sequence

REGISTER MAP (continued)

LDSW_A_DIS

Register address: 0x04; R/W
Default = 0x1F

Table 5. LDSW_A_DIS Register Details

BITS	NAME	DESCRIPTION	DEFAULT	TYPE
D[7]	RESERVED	Reversed	0	R
D[6]	RESERVED	Reversed	0	R
D[5]	RESERVED	Reversed	0	R
D[4]	LDSW5A_DIS	LDSW5A Discharge Enabled/Disabled Control: 0 = Disable. QOD5 will not discharge the V_{OUT5A} when LDSW5A is disabled. **1 = Enable**. QOD5 will discharge the V_{OUT5A} when LDSW5A is disabled.	1	R/W
D[3]	LDSW4A_DIS	LDSW4A Discharge Enabled/Disabled Control: 0 = Disable. QOD4 will not discharge the V_{OUT4A} when LDSW4A is disabled. **1 = Enable**. QOD4 will discharge the V_{OUT4A} when LDSW4A is disabled.	1	R/W
D[2]	LDSW3A_DIS	LDSW3A Discharge Enabled/Disabled Control: 0 = Disable. QOD3 will not discharge the V_{OUT3A} when LDSW3A is disabled. **1 = Enable**. QOD3 will discharge the V_{OUT3A} when LDSW3A is disabled.	1	R/W
D[1]	LDSW2A_DIS	LDSW2A Discharge Enabled/Disabled Control: 0 = Disable. QOD2 will not discharge the V_{OUT2A} when LDSW2 is disabled. **1 = Enable**. QOD2 will discharge the V_{OUT2A} when LDSW2A is disabled.	1	R/W
D[0]	LDSW1A_DIS	LDSW1A Discharge Enabled/Disabled Control : 0 = Disable. QOD1 will not discharge the V_{OUT1A} when LDSW1A is disabled. **1 = Enable**. QOD1 will discharge the V_{OUT1A} when LDSW1A is disabled.	1	R/W

LDSW_B_DIS

Register address: 0x05; R/W
Default = 0x1F

Table 6. LDSW_B_DIS Register Details

BITS	NAME	DESCRIPTION	DEFAULT	TYPE
D[7]	RESERVED	Reversed	0	R
D[6]	RESERVED	Reversed	0	R
D[5]	RESERVED	Reversed	0	R
D[4]	LDSW5B_DIS	LDSW5B Discharge Enabled/Disabled Control: 0 = Disable. QOD5 will not discharge the V_{OUT5B} when LDSW5B is disabled. **1 = Enable**. QOD5 will discharge the V_{OUT5B} when LDSW5B is disabled.	1	R/W
D[3]	LDSW4B_DIS	LDSW4B Discharge Enabled/Disabled Control: 0 = Disable. QOD4 will not discharge the V_{OUT4B} when LDSW4B is disabled. **1 = Enable**. QOD4 will discharge the V_{OUT4B} when LDSW4B is disabled.	1	R/W
D[2]	LDSW3B_DIS	LDSW3B Discharge Enabled/Disabled Control: 0 = Disable. QOD3 will not discharge the V_{OUT3B} when LDSW3B is disabled. **1 = Enable**. QOD3 will discharge the V_{OUT3B} when LDSW3B is disabled.	1	R/W
D[1]	LDSW2B_DIS	LDSW2B Discharge Enabled/Disabled Control: 0 = Disable. QOD2 will not discharge the V_{OUT2B} when LDSW2B is disabled. **1 = Enable**. QOD2 will discharge the V_{OUT2B} when LDSW2A is disabled.	1	R/W
D[0]	LDSW1B_DIS	LDSW1B Discharge Enabled/Disabled Control : 0 = Disable. QOD1 will not discharge the V_{OUT1B} when LDSW1AB is disabled. **1 = Enable**. QOD1 will discharge the V_{OUT1B} when LDSW1AB is disabled.	1	R/W

The device has a QOD circuit which is not activated to discharge by default. When the channel is enabled, the QOD circuit is forcibly turned off, meaning that the QOD function only takes effect when the channel is disabled. When EN = L, SCP or OTP is triggered, QOD function is enabled. When VBIAS = L or VBIAS&EN = L, QOD function is enabled for a short time.

REGISTER MAP (continued)

LDSW_A_SF

Register address: 0x06; R/W
Default = 0x54

Table 7. LDSW_A_SF Register Details

BITS	NAME	DESCRIPTION	DEFAULT	TYPE
D[7:6]	LDSW5A_SF_CTRL	LDSW5A rise time: 00 = 3ms **01 = 4.5ms** 10 = 6ms 11 = 7.5ms	01	R/W
D[5:4]	LDSW4A_SF_CTRL	LDSW4A rise time: 00 = 3ms **01 = 4.5ms** 10 = 6ms 11 = 7.5ms	01	R/W
D[3:2]	LDSW3A_SF_CTRL	LDSW3A rise time: 00 = 3ms **01 = 4.5ms** 10 = 6ms 11 = 7.5ms	01	R/W
D[1]	LDSW2A_SF_CTRL	LDSW2A rise time: **0 = 3ms** 1 = 6ms	0	R/W
D[0]	LDSW1A_SF_CTRL	LDSW1A rise time: **0 = 3ms** 1 = 6ms	0	R/W

The soft-start time control of group A at typical voltage is used to limit the soft-start current and prevent input voltage fluctuations.

LDSW_B_SF

Register address: 0x07; R/W
Default = 0x54

Table 8. LDSW_B_SF Register Details

BITS	NAME	DESCRIPTION	DEFAULT	TYPE
D[7:6]	LDSW5B_SF_CTRL	LDSW5B rise time: 00 = 3ms **01 = 4.5ms** 10 = 6ms 11 = 7.5ms	01	R/W
D[5:4]	LDSW4B_SF_CTRL	LDSW4B rise time: 00 = 3ms **01 = 4.5ms** 10 = 6ms 11 = 7.5ms	01	R/W
D[3:2]	LDSW3B_SF_CTRL	LDSW3B rise time: 00 = 3ms **01 = 4.5ms** 10 = 6ms 11 = 7.5ms	01	R/W
D[1]	LDSW2B_SF_CTRL	LDSW2B rise time: **0 = 3ms** 1 = 6ms	0	R/W
D[0]	LDSW1B_SF_CTRL	LDSW1B rise time: **0 = 3ms** 1 = 6ms	0	R/W

The soft-start time control of group B at typical voltage is used to limit the soft-start current and prevent input voltage fluctuations.

REGISTER MAP (continued)

LDSW_A_PG

Register address: 0x08; R
Default = 0x00

Table 9. LDSW_A_PG Register Details

BITS	NAME	DESCRIPTION	DEFAULT	TYPE
D[7]	RESERVED	Reversed	0	R
D[6]	RESERVED	Reversed	0	R
D[5]	RESERVED	Reversed	0	R
D[4]	LDSW5A_PG	Power Good signal of LDSW5A **0: NG** 1: OK	0	R
D[3]	LDSW4A_PG	Power Good signal of LDSW4A **0: NG** 1: OK	0	R
D[2]	LDSW3A_PG	Power Good signal of LDSW3A **0: NG** 1: OK	0	R
D[1]	LDSW2A_PG	Power Good signal of LDSW2A **0: NG**) 1: OK	0	R
D[0]	LDSW1A_PG	Power Good signal of LDSW1A **0: NG** 1: OK	0	R

Power-Good indication of group A, when the channel of group A completes soft-start, LDSWxA_PG becomes 1, otherwise 0.

LDSW_A_PG

Register address: 0x09; R
Default = 0x00

Table 10. LDSW_B_PG Register Details

BITS	NAME	DESCRIPTION	DEFAULT	TYPE
D[7]	RESERVED	Reversed	0	R
D[6]	RESERVED	Reversed	0	R
D[5]	RESERVED	Reversed	0	R
D[4]	LDSW5B_PG	Power Good signal of LDSW5B **0: NG** 1: OK	0	R
D[3]	LDSW4B_PG	Power Good signal of LDSW4B **0: NG** 1: OK	0	R
D[2]	LDSW3B_PG	Power Good signal of LDSW3B **0: NG** 1: OK	0	R
D[1]	LDSW2B_PG	Power Good signal of LDSW2B **0: NG** 1: OK	0	R
D[0]	LDSW1B_PG	Power Good signal of LDSW1B **0: NG** 1: OK	0	R

Power-Good indication of group B, when the channel of group B completes soft-start, LDSWxB_PG becomes 1, otherwise 0.

REGISTER MAP (continued)

OT_FLAG

Register address: 0x0A; R
Default = 0x00

Table 11. OT_FLAG Register Details

BITS	NAME	DESCRIPTION	DEFAULT	TYPE
D[7]	RESERVED	Reversed	0	R
D[6]	RESERVED	Reversed	0	R
D[5]	RESERVED	Reversed	0	R
D[4]	RESERVED	Reversed	0	R
D[3]	RESERVED	Reversed	0	R
D[2]	RESERVED	Reversed	0	R
D[1]	RESERVED	Reversed	0	R
D[0]	OT_FLAG	Flag of over temperature **0: NG** 1: OT State	0	R

Over-temperature indication of the device, when OT is triggered, bit D[0] = 1, EN or VBIAS = L can clear this bit.

A_SCP_FLAG

Register address: 0x0B; R
Default = 0x00

Table 12. A_SCP_FLAG Register Details

BITS	NAME	DESCRIPTION	DEFAULT	TYPE
D[7]	RESERVED	Reversed	0	R
D[6]	RESERVED	Reversed	0	R
D[5]	RESERVED	Reversed	0	R
D[4]	5A_SCP_FLAG	SCP state of LDSW5A **0: OK** 1: SCP	0	R
D[3]	4A_SCP_FLAG	SCP state of LDSW4A **0: OK** 1: SCP	0	R
D[2]	3A_SCP_FLAG	SCP state of LDSW3A **0: OK** 1: SCP	0	R
D[1]	2A_SCP_FLAG	SCP state of LDSW2A **0: OK** 1: SCP	0	R
D[0]	1A_SCP_FLAG	SCP state of LDSW1A **0: OK** 1: SCP	0	R

Short-Circuit indication of group A, when any channel of group A triggers short-circuit, the corresponding bit is set to 1. EN or VBIAS = L can clear this bit.

REGISTER MAP (continued)

B_SCP_FLAG

Register address: 0x0C; R
Reset = 0x00

Table 13. B_SCP_FLAG Register Details

BITS	NAME	DESCRIPTION	DEFAULT	TYPE
D[7]	RESERVED	Reversed	0	R
D[6]	RESERVED	Reversed	0	R
D[5]	RESERVED	Reversed	0	R
D[4]	5B_SCP_FLAG	SCP state of LDSW5B **0: OK** 1: SCP	0	R
D[3]	4B_SCP_FLAG	SCP state of LDSW4B **0: OK** 1: SCP	0	R
D[2]	3B_SCP_FLAG	SCP state of LDSW3B **0: OK** 1: SCP	0	R
D[1]	2B_SCP_FLAG	SCP state of LDSW2B **0: OK** 1: SCP	0	R
D[0]	1B_SCP_FLAG	SCP state of LDSW1B **0: OK** 1: SCP	0	R

Short-circuit indication of group B, when any channel of group B triggers short-circuit, the corresponding bit is set to 1. EN or VBIAS = L can clear this bit.

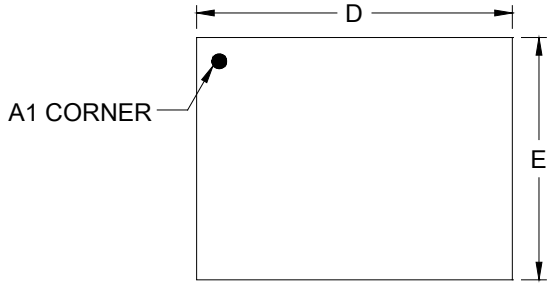
REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

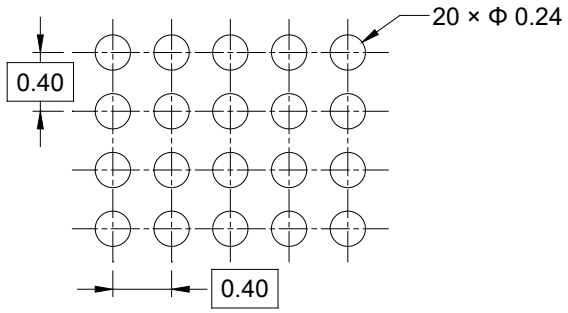
Changes from Original to REV.A	Page
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

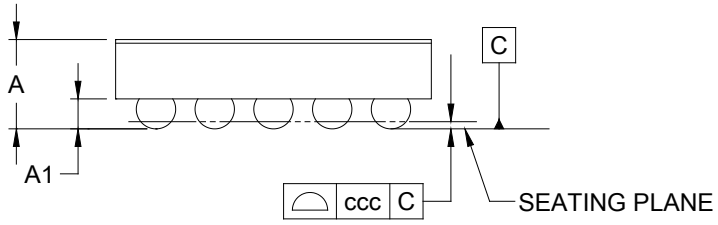
WLCSP-2.15×1.65-20B



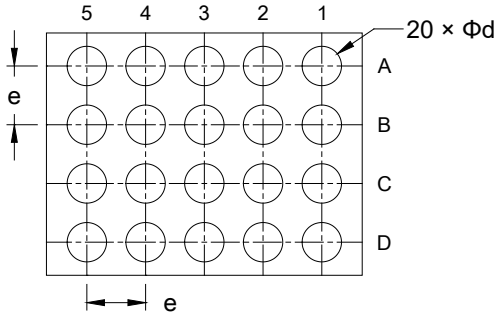
TOP VIEW



RECOMMENDED LAND PATTERN (Unit: mm)



SIDE VIEW



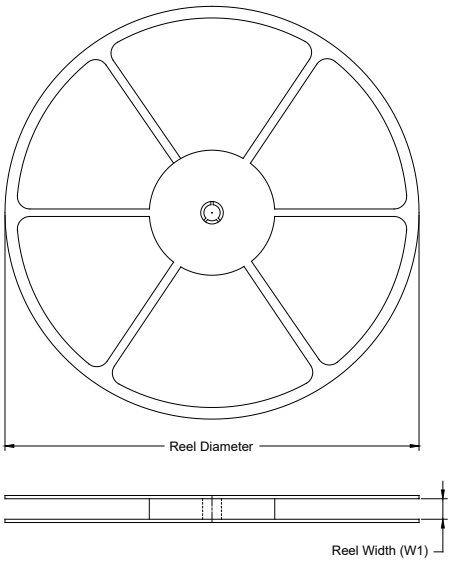
BOTTOM VIEW

Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	-	-	0.650
A1	0.184	-	0.224
D	2.120	-	2.180
E	1.620	-	1.680
d	0.238	-	0.298
e	0.400 BSC		
ccc	0.050		

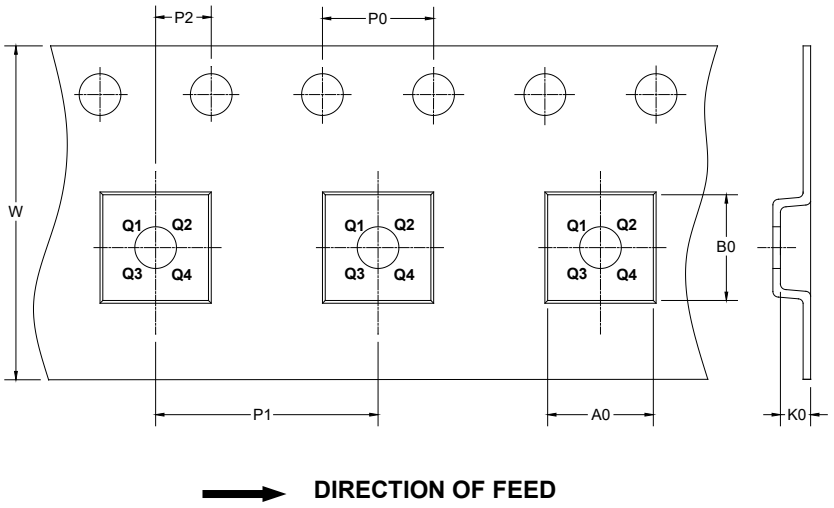
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



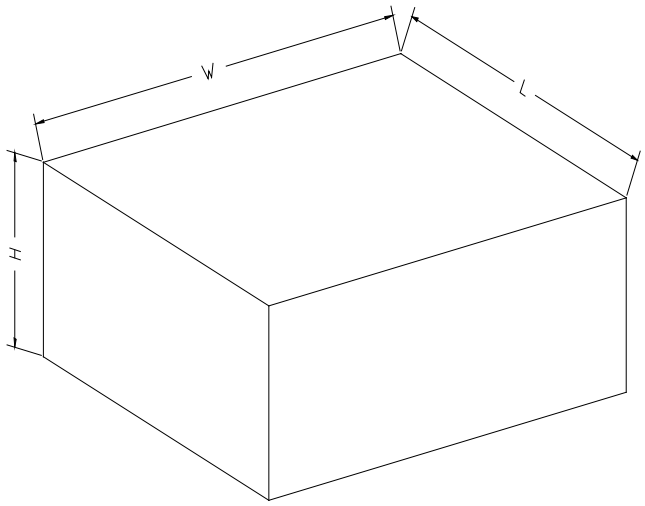
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
WLCSP-2.15×1.65-20B	7"	9.5	1.80	2.30	0.76	4.0	4.0	2.0	8.0	Q2

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18

DD0002