SGM4583X
High Voltage, CMOS Analog Switch

GENERAL DESCRIPTION

The SGM4583X is a TTL/CMOS compatible analog multiplexer which consists of three single-pole/double-throw (SPDT) switches. It operates from +3.6V to +11V single power supply or ±1.8V to ±5.5V dual power supplies.

Other features include high voltage, low on-resistance and low distortion. The high performances make it very suitable for multiple applications, such as cellular phones, audio and video signal routing, etc.

TTL/CMOS logic compatibility can be guaranteed when using a single +5V or dual ±5V power supplies because the logic thresholds of all digital inputs are between 0.8V and 2.4V.

The SGM4583X is available in Green SOIC-16, SSOP-16, TSSOP-16 and TQFN-3×3-16L packages. It operates over an ambient temperature range of -40℃ to +125℃.

FEATURES

- **Single Supply Voltage Range: +3.6V to +11V**
- **Dual-Supply Voltage Range: ±1.8V to ±5.5V**
- **On-Resistance:**
  51Ω (MAX) with ±5V Supplies
  84Ω (MAX) with Single +5V Supply
- **Low On-Resistance Flatness**
- **Low Off-Leakage Current: ±1μA (MAX)**
- **Low On-Leakage Current: ±1μA (MAX)**
- **Low Crosstalk: -85dB (R_L = 50Ω, f = 1MHz)**
- **High Off-Isolation: -62dB (R_L = 50Ω, f = 1MHz)**
- **Low Distortion: 0.02% (R_L = 600Ω, f = 20Hz to 20kHz)**
- **Rail-to-Rail Input and Output Operation**
- **TTL/CMOS-Logic Compatible**
- **-40℃ to +125℃ Operating Temperature Range**
- **Available in Green SOIC-16, SSOP-16, TSSOP-16 and TQFN-3×3-16L Packages**

APPLICATIONS

Automotive
Cellular Phones
Portable Equipment
Sample-and-Hold Circuits
Battery-Powered Systems
Audio and Video Signal Routing

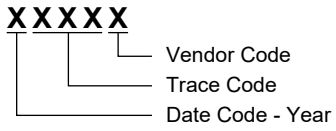
PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM4583X	SOIC-16	-40℃ to +125℃	SGM4583XS16G/TR	SGM4583XS16 XXXXX	Tape and Reel, 2500
	SSOP-16	-40℃ to +125℃	SGM4583XQS16G/TR	SGM4583 XQS16 XXXXX	Tape and Reel, 3000
	TSSOP-16	-40℃ to +125℃	SGM4583XTS16G/TR	SGM4583 XTS16 XXXXX	Tape and Reel, 3000
	TQFN-3×3-16L	-40℃ to +125℃	SGM4583XTQ16G/TR	4583TQ XXXXX	Tape and Reel, 3000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.

SOIC-16/SSOP-16/TSSOP-16/TQFN-3×3-16L



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Voltages Referenced to V_{EE}

V_{CC} ..... -0.3V to 13.2V

GND ..... -0.3V to 6V

Voltage into Any Terminal (1) ..... (V_{EE} - 0.3V) to (V_{CC} + 0.3V)

Continuous Current into Any Terminal ..... ±20mA

Peak Current, X_ (Pulsed at 1ms, 10% duty cycle) .... ±40mA

Package Thermal Resistance

SOIC-16, θ_{JA} ..... 97.2℃/W

SOIC-16, θ_{JB} ..... 59.2℃/W

SOIC-16, θ_{JC} ..... 59.9℃/W

SSOP-16, θ_{JA} ..... 95.2℃/W

SSOP-16, θ_{JB} ..... 56.5℃/W

SSOP-16, θ_{JC} ..... 55.7℃/W

TSSOP-16, θ_{JA} ..... 107.9℃/W

TSSOP-16, θ_{JB} ..... 72.4℃/W

TSSOP-16, θ_{JC} ..... 43℃/W

TQFN-3×3-16L, θ_{JA} ..... 44℃/W

TQFN-3×3-16L, θ_{JB} ..... 20.2℃/W

TQFN-3×3-16L, $\theta_{JC(TOP)}$ ..... 49.3℃/W

TQFN-3×3-16L, $\theta_{JC(BOT)}$ ..... 8.1℃/W

Junction Temperature ..... +150℃

Storage Temperature Range ..... -65℃ to +150℃

Lead Temperature (Soldering, 10s) ..... +260℃

ESD Susceptibility

HBM ..... ±3000V

CDM ..... ±1000V

NOTE: 1. Internal diodes will clamp the voltages on any signal that exceeding V_{CC} or V_{EE}. Limit the current through the forward diode to the maximum ratings.

RECOMMENDED OPERATING CONDITIONS

Operating Temperature Range ..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

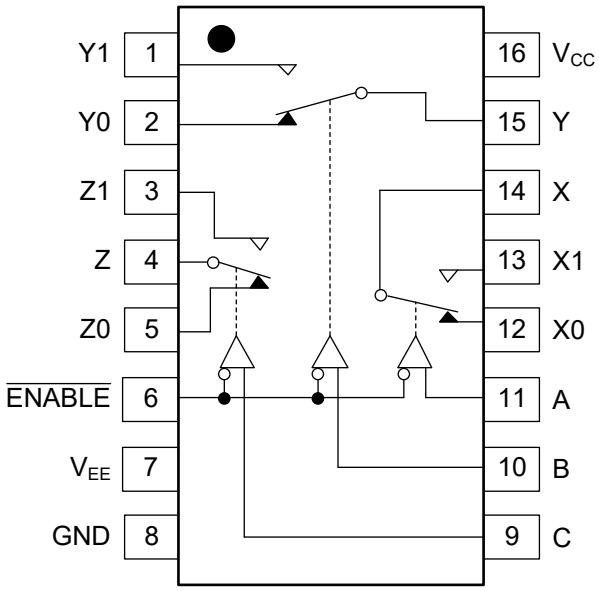
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

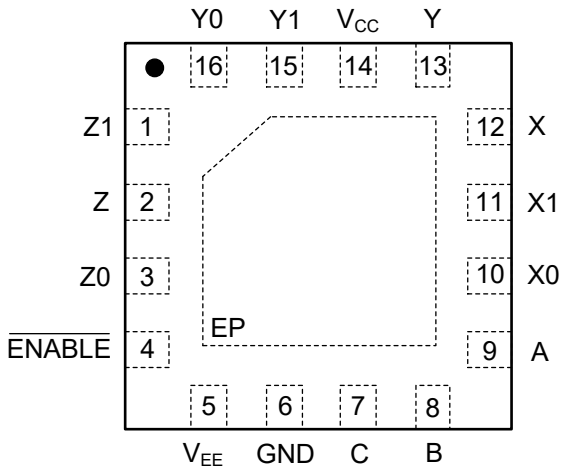
PIN CONFIGURATIONS

(TOP VIEW)



SOIC-16/SSOP-16/TSSOP-16

(TOP VIEW)



TQFN-3×3-16L

PIN DESCRIPTION

PIN		NAME	FUNCTION
SOIC-16, SSOP-16, TSSOP-16	TQFN-3×3-16L		
1	15	Y1	Analog Switch “Y” Normally Open Input Pin.
2	16	Y0	Analog Switch “Y” Normally Closed Input Pin.
3	1	Z1	Analog Switch “Z” Normally Open Input Pin.
4	2	Z	Analog Switch “Z” Output Pin.
5	3	Z0	Analog Switch “Z” Normally Closed Input Pin.
6	4	$\overline{\text{ENABLE}}$	Digital Enable Control Pin. Normally connected to GND.
7	5	V_{EE}	Negative Analog Supply Voltage Input Pin. Connect to GND for single-supply operation.
8	6	GND	Ground.
9	7	C	Digital Signal Input C Pin.
10	8	B	Digital Signal Input B Pin.
11	9	A	Digital Signal Input A Pin.
12	10	X0	Analog Switch “X” Normally Closed Input Pin.
13	11	X1	Analog Switch “X” Normally Open Input Pin.
14	12	X	Analog Switch “X” Output Pin.
15	13	Y	Analog Switch “Y” Output Pin.
16	14	V_{CC}	Positive Analog and Digital Supply Voltage Input Pin.
—	Exposed Pad	EP	Exposed Pad. Connect exposed pad to V_{EE} Pin.

NOTE:

Any input pin can be used as an output pin, and any output pin can also be used as an input pin. Signal transmission in both directions is equally well.

FUNCTION TABLE

$\overline{\text{ENABLE}}$ INPUT	SELECT INPUTS			ON SWITCHES
	C	B	A	
H	***X***	***X***	***X***	All Switches Open
L	L	L	L	X-X0, Y-Y0, Z-Z0
L	L	L	H	X-X1, Y-Y0, Z-Z0
L	L	H	L	X-X0, Y-Y1, Z-Z0
L	L	H	H	X-X1, Y-Y1, Z-Z0
L	H	L	L	X-X0, Y-Y0, Z-Z1
L	H	L	H	X-X1, Y-Y0, Z-Z1
L	H	H	L	X-X0, Y-Y1, Z-Z1
L	H	H	H	X-X1, Y-Y1, Z-Z1

X = Don’t care.

ELECTRICAL CHARACTERISTICS (Dual Supplies)

(V_{CC} = 4.5V to 5.5V, V_{EE} = -4.5V to -5.5V, GND = 0V, Full = -40℃ to +125℃, typical values are at T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	TEMP	MIN	TYP	MAX	UNITS
Analog Switch							
Analog Signal Range	$V_{X\_}$, $V_{Y\_}$, $V_{Z\_}$, V_X, V_Y, V_Z		Full	V_{EE}		V_{CC}	V
On-Resistance	R_{ON}	V_{CC} = 4.5V, V_{EE} = -4.5V, I_X, I_Y, I_Z = 1mA	+25℃		36	51	Ω
			Full			70	
On-Resistance Match between Channels	ΔR_{ON}	V_{CC} = 4.5V, V_{EE} = -4.5V, I_X, I_Y, I_Z = 1mA	+25℃		3	11	Ω
			Full			18	
On-Resistance Flatness	$R_{FLAT(ON)}$	V_{CC} = 4.5V, V_{EE} = -4.5V, I_X, I_Y, I_Z = 1mA	+25℃		15	25	Ω
			Full			30	
X_, Y_, Z_ Off Leakage Current	$I_{X\_(OFF)}$, $I_{Y\_(OFF)}$, $I_{Z\_(OFF)}$	V_{CC} = 5.5V, V_{EE} = -5.5V, $V_{X\_}$, $V_{Y\_}$, $V_{Z\_}$ = ±4.5V, V_X, V_Y, V_Z = ∓ 4.5V	Full		±0.01	±1	μA
X, Y, Z Off Leakage Current	$I_{X(OFF)}$, $I_{Y(OFF)}$, $I_{Z(OFF)}$	V_{CC} = 5.5V, V_{EE} = -5.5V, $V_{X\_}$, $V_{Y\_}$, $V_{Z\_}$ = ±4.5V, V_X, V_Y, V_Z = ∓ 4.5V	Full		±0.01	±1	μA
X, Y, Z On Leakage Current	$I_{X(ON)}$, $I_{Y(ON)}$, $I_{Z(ON)}$	V_{CC} = 5.5V, V_{EE} = -5.5V, V_X, V_Y, V_Z = ±4.5V	Full		±0.01	±1	μA
Digital I/O							
Logic Input Logic Threshold High	V_{AH}, V_{BH}, V_{CH}, $V_{\overline{ENABLEH}}$		Full	2.4			V
Logic Input Logic Threshold Low	V_{AL}, V_{BL}, V_{CL}, $V_{\overline{ENABLEL}}$		Full			0.8	V
Input-Current High	I_{AH}, I_{BH}, I_{CH}, $I_{\overline{ENABLEH}}$	V_A, V_B, V_C, $V_{\overline{ENABLE}}$ = V_{CC}	Full		±0.01	±1	μA
Input-Current Low	I_{AL}, I_{BL}, I_{CL}, $I_{\overline{ENABLEL}}$	V_A, V_B, V_C, $V_{\overline{ENABLE}}$ = 0V	Full		±0.01	±1	μA
Dynamic Characteristics							
Address Transition Time	t_{TRANS}	$V_{X\_}$, $V_{Y\_}$, $V_{Z\_}$ = ±3V, R_L = 300Ω, C_L = 35pF, Test Circuit 1	+25℃		70		ns
$\overline{ENABLE}$ Turn-On Time	t_{ON}	$V_{X\_}$, $V_{Y\_}$, $V_{Z\_}$ = 3V, R_L = 300Ω, C_L = 35pF, Test Circuit 2	+25℃		60		ns
$\overline{ENABLE}$ Turn-Off Time	t_{OFF}	$V_{X\_}$, $V_{Y\_}$, $V_{Z\_}$ = 3V, R_L = 300Ω, C_L = 35pF, Test Circuit 2	+25℃		70		ns
Break-Before-Make Delay Time	t_D	$V_{X\_}$, $V_{Y\_}$, $V_{Z\_}$ = 3V, R_L = 300Ω, C_L = 35pF, Test Circuit 3	+25℃		15		ns
Charge Injection	Q	R_S = 0Ω, C_L = 1nF, V_S = 0V, Test Circuit 4	+25℃		10		pC
Channel-to-Channel Crosstalk	V_{CT}	R_L = 50Ω, f = 1MHz, Test Circuit 5	+25℃		-85		dB
Off-Isolation	V_{ISO}	R_L = 50Ω, f = 1MHz, Test Circuit 6	+25℃		-62		dB
-3dB Bandwidth	BW	R_L = 50Ω, Test Circuit 7	+25℃		140		MHz
Input Off-Capacitance	$C_{X\_(OFF)}$, $C_{Y\_(OFF)}$, $C_{Z\_(OFF)}$	$V_{X\_}$, $V_{Y\_}$, $V_{Z\_}$ = 0V, f = 1MHz, Test Circuit 8	+25℃		12		pF
Output Off-Capacitance	$C_{X(OFF)}$, $C_{Y(OFF)}$, $C_{Z(OFF)}$	$V_{X\_}$, $V_{Y\_}$, $V_{Z\_}$ = 0V, f = 1MHz, Test Circuit 8	+25℃		15		pF
Output On-Capacitance	$C_{X(ON)}$, $C_{Y(ON)}$, $C_{Z(ON)}$	$V_{X\_}$, $V_{Y\_}$, $V_{Z\_}$ = 0V, f = 1MHz, Test Circuit 8	+25℃		35		pF
Total Harmonic Distortion	THD	R_L = 600Ω, $V_{X\_}$, $V_{Y\_}$, $V_{Z\_}$ = $5V_{P-P}$, f = 20Hz to 20kHz	+25℃		0.02		%
Power Supply							
Power Supply Range	V_{CC}, V_{EE}		Full	±1.8V		±5.5V	V
Power Supply Current	I_{CC}, I_{EE}	V_{CC} = 5.5V, V_{EE} = -5.5V, V_A, V_B, V_C, $V_{\overline{ENABLE}}$ = V_{CC} or 0V	+25℃		0.01	20	μA
			Full			22	

ELECTRICAL CHARACTERISTICS (Single Supply at +5V)

(V_{CC} = 4.5V to 5.5V, V_{EE} = GND = 0V, Full = -40℃ to +125℃, typical values are at T_A = +25℃, unless otherwise noted.)

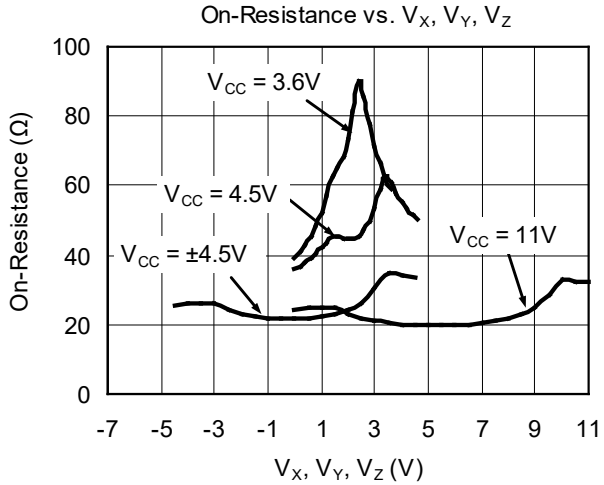
PARAMETER	SYMBOL	CONDITIONS	TEMP	MIN	TYP	MAX	UNITS
Analog Switch							
Analog Signal Range	$V_{X\_}$, $V_{Y\_}$, $V_{Z\_}$, V_X, V_Y, V_Z		Full	V_{EE}		V_{CC}	V
On-Resistance	R_{ON}	V_{CC} = 4.5V, I_X, I_Y, I_Z = 1mA	+25℃		66	84	Ω
			Full			110	
On-Resistance Match between Channels	ΔR_{ON}	V_{CC} = 4.5V, I_X, I_Y, I_Z = 1mA	+25℃		3	11	Ω
			Full			18	
X_, Y_, Z_ Off Leakage Current	$I_{X\_(OFF)}$, $I_{Y\_(OFF)}$, $I_{Z\_(OFF)}$	V_{CC} = 5.5V, $V_{X\_}$, $V_{Y\_}$, $V_{Z\_}$ = 1V, 4.5V, V_X, V_Y, V_Z = 4.5V, 1V	Full		±0.01	±1	μA
X, Y, Z Off Leakage Current	$I_{X(OFF)}$, $I_{Y(OFF)}$, $I_{Z(OFF)}$	V_{CC} = 5.5V, $V_{X\_}$, $V_{Y\_}$, $V_{Z\_}$ = 1V, 4.5V, V_X, V_Y, V_Z = 4.5V, 1V	Full		±0.01	±1	μA
X, Y, Z On Leakage Current	$I_{X(ON)}$, $I_{Y(ON)}$, $I_{Z(ON)}$	V_{CC} = 5.5V, V_X, V_Y, V_Z = 4.5V, 1V	Full		±0.01	±1	μA
Digital I/O							
Logic Input Logic Threshold High	V_{AH}, V_{BH}, V_{CH}, $V_{\overline{ENABLEH}}$		Full	2.4			V
Logic Input Logic Threshold Low	V_{AL}, V_{BL}, V_{CL}, $V_{\overline{ENABLEL}}$		Full			0.8	V
Input-Current High	I_{AH}, I_{BH}, I_{CH}, $I_{\overline{ENABLEH}}$	V_A, V_B, V_C, $V_{\overline{ENABLE}}$ = V_{CC}	Full		±0.01	±1	μA
Input-Current Low	I_{AL}, I_{BL}, I_{CL}, $I_{\overline{ENABLEL}}$	V_A, V_B, V_C, $V_{\overline{ENABLE}}$ = 0V	Full		±0.01	±1	μA
Dynamic Characteristics							
Address Transition Time	t_{TRANS}	$V_{X\_}$, $V_{Y\_}$, $V_{Z\_}$ = 3V/0V, R_L = 300Ω, C_L = 35pF, Test Circuit 1	+25℃		100		ns
$\overline{ENABLE}$ Turn-On Time	t_{ON}	$V_{X\_}$, $V_{Y\_}$, $V_{Z\_}$ = 3V, R_L = 300Ω, C_L = 35pF, Test Circuit 2	+25℃		70		ns
$\overline{ENABLE}$ Turn-Off Time	t_{OFF}	$V_{X\_}$, $V_{Y\_}$, $V_{Z\_}$ = 3V, R_L = 300Ω, C_L = 35pF, Test Circuit 2	+25℃		80		ns
Break-Before-Make Delay Time	t_D	$V_{X\_}$, $V_{Y\_}$, $V_{Z\_}$ = 3V, R_L = 300Ω, C_L = 35pF, Test Circuit 3	+25℃		25		ns
Charge Injection	Q	R_S = 0Ω, C_L = 1nF, V_S = 2.5V, Test Circuit 4	+25℃		5		pC
-3dB Bandwidth	BW	R_L = 50Ω, Test Circuit 7	+25℃		160		MHz
Power Supply							
Power Supply Range	V_{CC}, V_{EE}		+25℃	3.6		11	V
Power Supply Current	I_{CC}, I_{EE}	V_{CC} = 5.5V, V_A, V_B, V_C, $V_{\overline{ENABLE}}$ = V_{CC} or 0V	+25℃		0.01	20	μA
			Full			22	

ELECTRICAL CHARACTERISTICS (Single Supply at +3.6V)

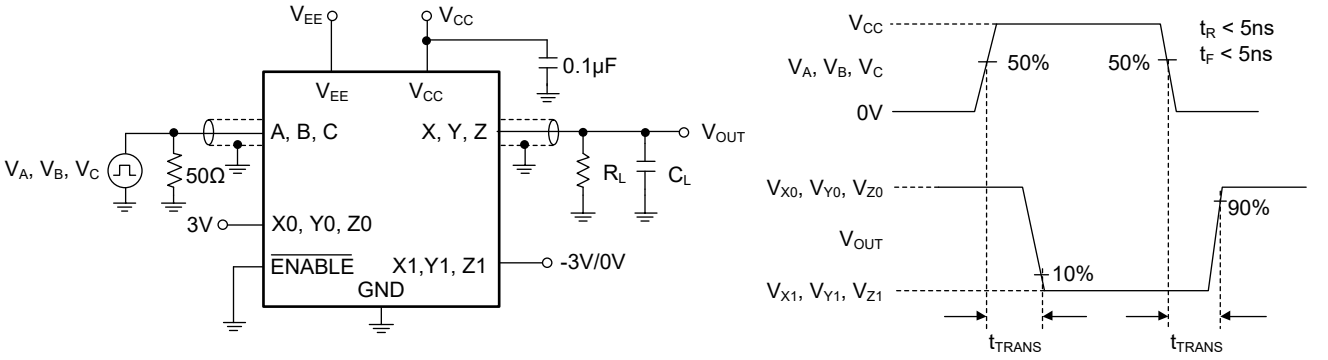
(V_{CC} = 3.6V, V_{EE} = GND = 0V, Full = -40℃ to +125℃, typical values are at T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	TEMP	MIN	TYP	MAX	UNITS
Analog Switch							
Analog Signal Range	$V_{X\_}$, $V_{Y\_}$, $V_{Z\_}$, V_X, V_Y, V_Z		Full	V_{EE}		V_{CC}	V
On-Resistance	R_{ON}	I_X, I_Y, I_Z = 1mA	+25℃		100	130	Ω
			Full			150	
X_, Y_, Z_ Off Leakage Current	$I_{X\_(OFF)}$, $I_{Y\_(OFF)}$, $I_{Z\_(OFF)}$	$V_{X\_}$, $V_{Y\_}$, $V_{Z\_}$ = 1V, 3V, V_X, V_Y, V_Z = 3V, 1V	Full		±0.01	±1	μA
X, Y, Z Off Leakage Current	$I_{X(OFF)}$, $I_{Y(OFF)}$, $I_{Z(OFF)}$	$V_{X\_}$, $V_{Y\_}$, $V_{Z\_}$ = 1V, 3V, V_X, V_Y, V_Z = 3V, 1V	Full		±0.01	±1	μA
X, Y, Z On Leakage Current	$I_{X(ON)}$, $I_{Y(ON)}$, $I_{Z(ON)}$	V_X, V_Y, V_Z = 3V, 1V	Full		±0.01	±1	μA
Digital I/O							
Logic Input Logic Threshold High	V_{AH}, V_{BH}, V_{CH}, $V_{\overline{ENABLEH}}$		Full	2			V
Logic Input Logic Threshold Low	V_{AL}, V_{BL}, V_{CL}, $V_{\overline{ENABLEL}}$		Full			0.5	V
Input-Current High	I_{AH}, I_{BH}, I_{CH}, $I_{\overline{ENABLEH}}$	V_A, V_B, V_C, $V_{\overline{ENABLE}}$ = V_{CC}	Full		±0.01	±1	μA
Input-Current Low	I_{AL}, I_{BL}, I_{CL}, $I_{\overline{ENABLEL}}$	V_A, V_B, V_C, $V_{\overline{ENABLE}}$ = 0V	Full		±0.01	±1	μA
Dynamic Characteristics							
Address Transition Time	t_{TRANS}	$V_{X\_}$, $V_{Y\_}$, $V_{Z\_}$ = 3V/0V, R_L = 300Ω, C_L = 35pF, Test Circuit 1	+25℃		140		ns
$\overline{ENABLE}$ Turn-On Time	t_{ON}	$V_{X\_}$, $V_{Y\_}$, $V_{Z\_}$ = 3V, R_L = 300Ω, C_L = 35pF, Test Circuit 2	+25℃		100		ns
$\overline{ENABLE}$ Turn-Off Time	t_{OFF}	$V_{X\_}$, $V_{Y\_}$, $V_{Z\_}$ = 3V, R_L = 300Ω, C_L = 35pF, Test Circuit 2	+25℃		90		ns
Break-Before-Make Delay Time	t_D	$V_{X\_}$, $V_{Y\_}$, $V_{Z\_}$ = 3V, R_L = 300Ω, C_L = 35pF, Test Circuit 3	+25℃		35		ns
Charge Injection	Q	R_S = 0Ω, C_L = 1nF, V_S = 1.8V, Test Circuit 4	+25℃		3		pC
-3dB Bandwidth	BW	R_L = 50Ω, Test Circuit 7	+25℃		160		MHz
Power Supply							
Power Supply Current	I_{CC}, I_{EE}	V_A, V_B, V_C, $V_{\overline{ENABLE}}$ = V_{CC} or 0V	+25℃		0.01	20	μA
			Full			22	

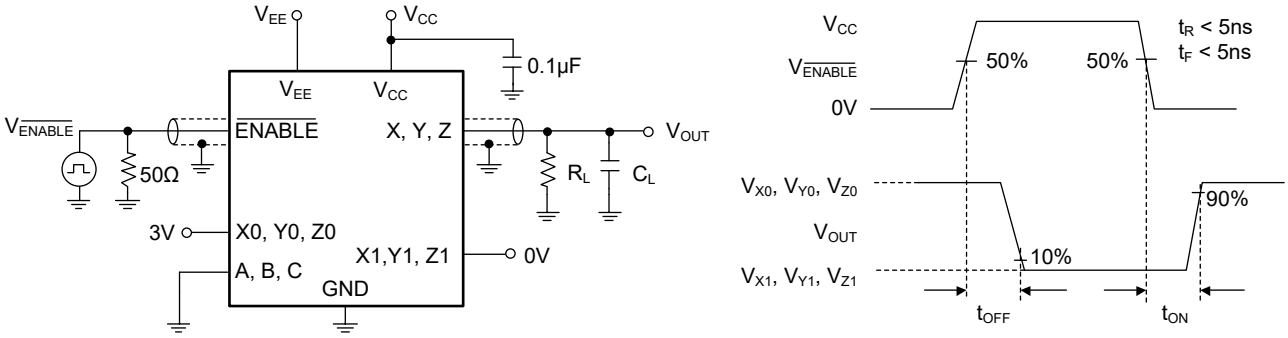
TYPICAL PERFORMANCE CHARACTERISTICS



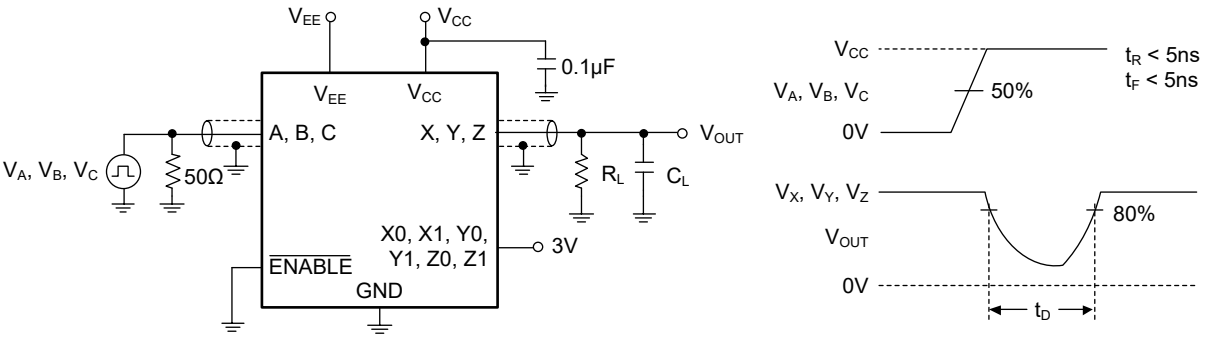
TEST CIRCUITS



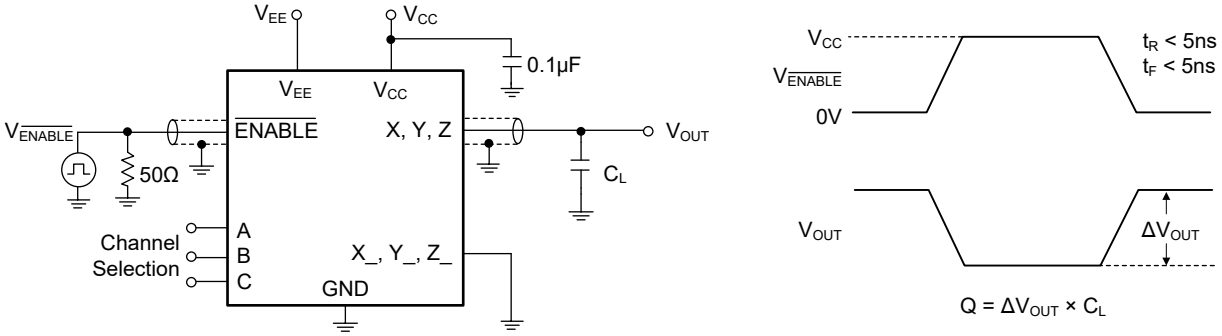
Test Circuit 1. Address Transition Times (t_{TRANS})



Test Circuit 2. Switching Times (t_{ON}, t_{OFF})

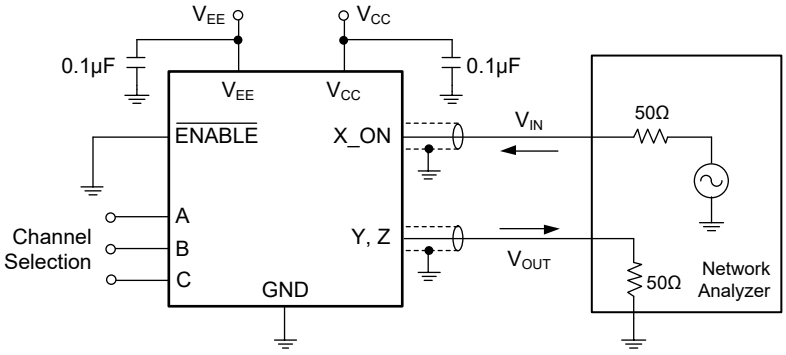


Test Circuit 3. Break-Before-Make Delay Time (t_D)



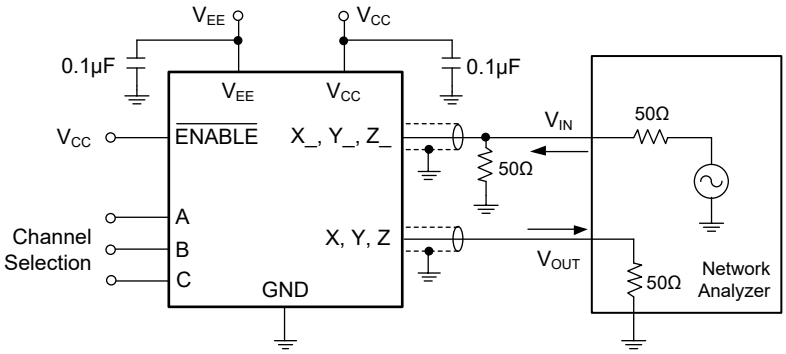
Test Circuit 4. Charge Injection (Q)

TEST CIRCUITS (continued)



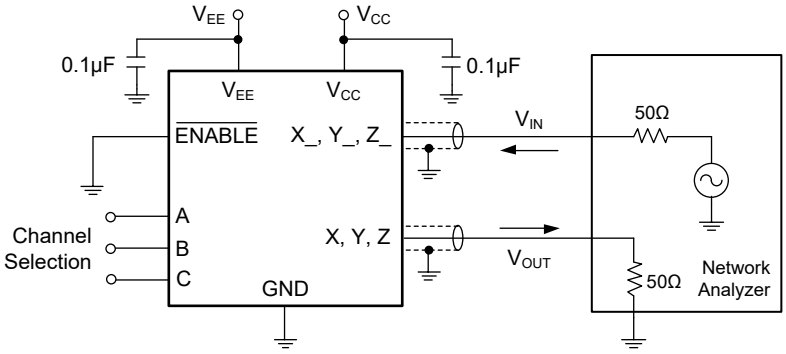
Channel-to-Channel Crosstalk = 20log (V_{OUT}/V_{IN})
Measured from One Channel (X, Y, Z) to All other Channels

Test Circuit 5. Channel-to-Channel Crosstalk



Off-Isolation = 20log(V_{OUT}/V_{IN})
Measured between X and "OFF" X_ Terminal on Each Switch

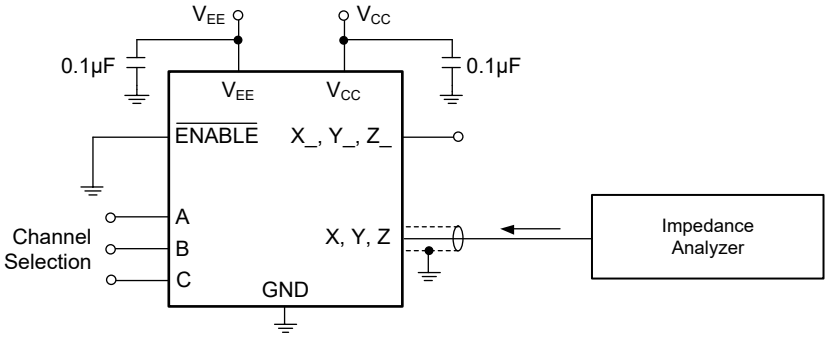
Test Circuit 6. Off-Isolation



On Loss = 20log(V_{OUT}/V_{IN})
Measured between X and "ON" X_ Terminal on Each Switch

Test Circuit 7. On Loss

TEST CIRCUITS (continued)



Test Circuit 8. Capacitance

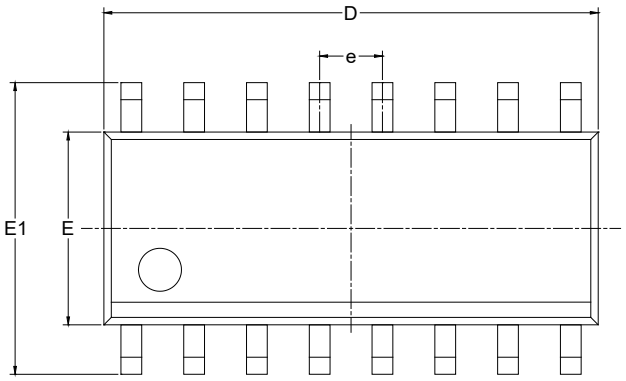
REVISION HISTORY

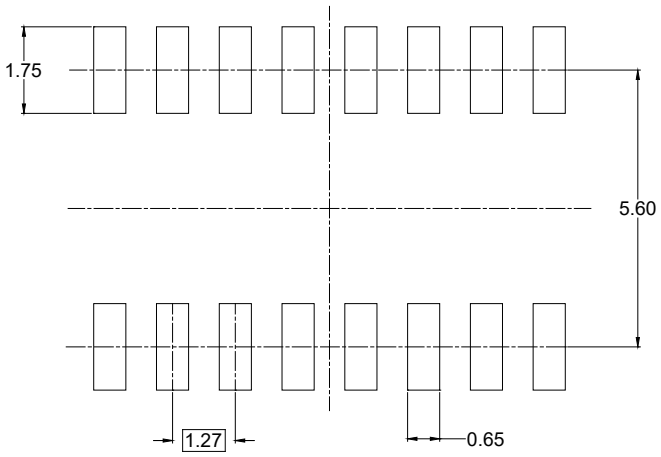
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original to REV.A (DECEMBER 2025)	Page
Changed from product preview to production data	All

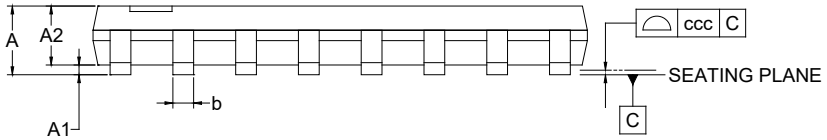
PACKAGE OUTLINE DIMENSIONS

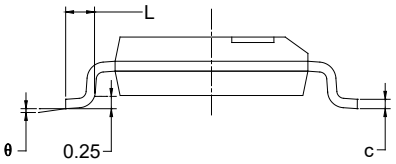
SOIC-16





RECOMMENDED LAND PATTERN (Unit: mm)



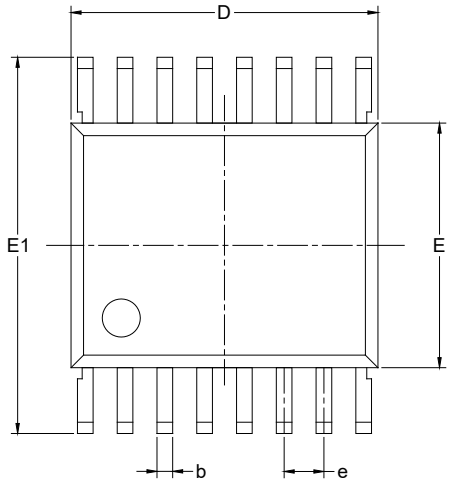


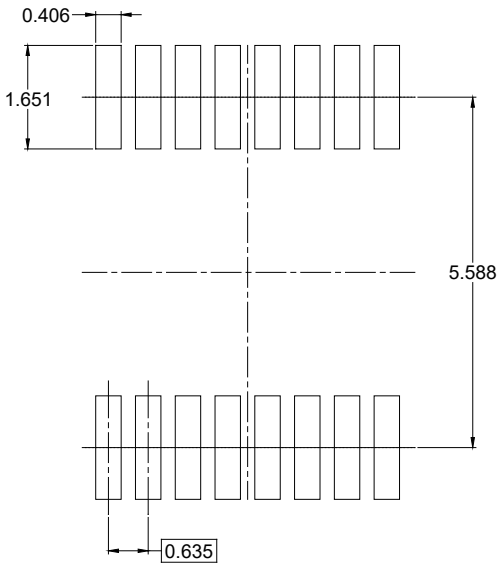
Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	-	-	1.750
A1	0.100	-	0.250
A2	1.250	-	1.550
b	0.310	-	0.510
c	0.100	-	0.250
D	9.800	-	10.200
E	3.800	-	4.000
E1	5.800	-	6.200
e	1.270 BSC		
L	0.400	-	1.270
θ	0°	-	8°
ccc	0.100		

NOTES:
1. This drawing is subject to change without notice.
2. The dimensions do not include mold flashes, protrusions or gate burrs.
3. Reference JEDEC MS-012.

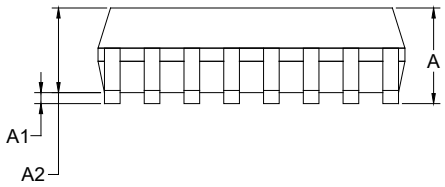
PACKAGE OUTLINE DIMENSIONS

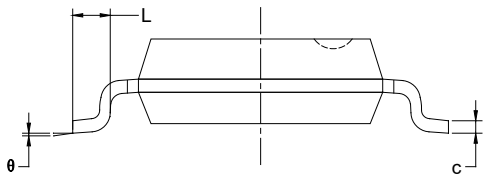
SSOP-16





RECOMMENDED LAND PATTERN (Unit: mm)



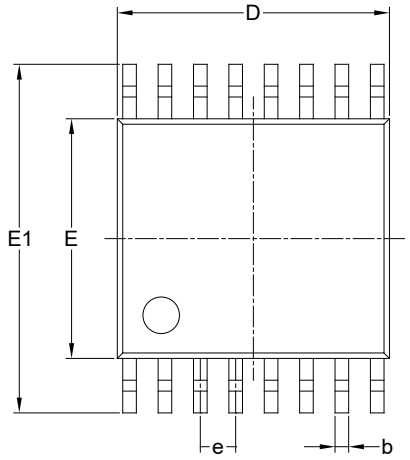


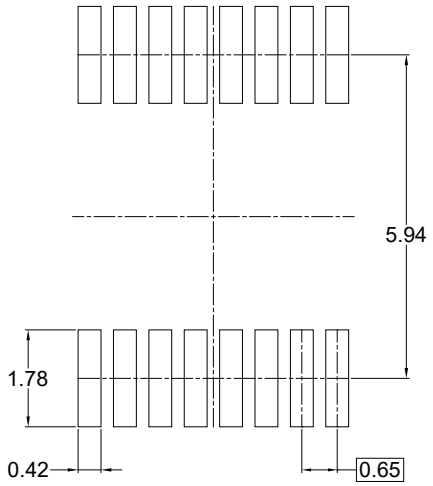
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.200	0.300	0.008	0.012
c	0.170	0.250	0.007	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	0.635 BSC		0.025 BSC	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

NOTES:
1. Body dimensions do not include mode flash or protrusion.
2. This drawing is subject to change without notice.

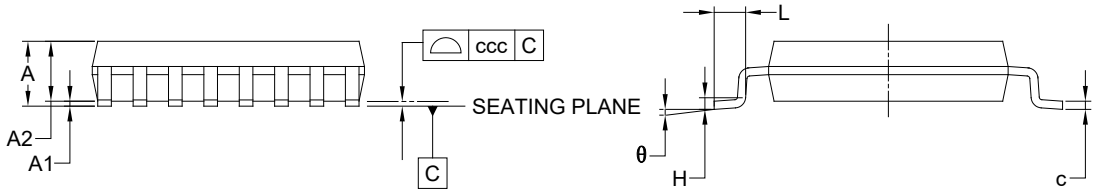
PACKAGE OUTLINE DIMENSIONS

TSSOP-16





RECOMMENDED LAND PATTERN (Unit: mm)

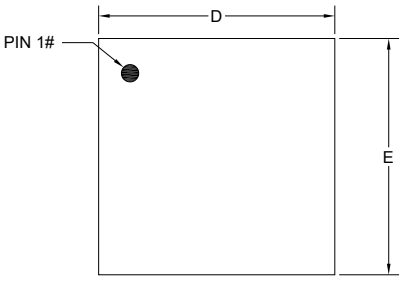


Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	-	-	1.200
A1	0.050	-	0.150
A2	0.800	-	1.050
b	0.190	-	0.300
c	0.090	-	0.200
D	4.860	-	5.100
E	4.300	-	4.500
E1	6.200	-	6.600
e	0.650 BSC		
L	0.450	-	0.750
H	0.250 TYP		
θ	0°	-	8°
ccc	0.100		

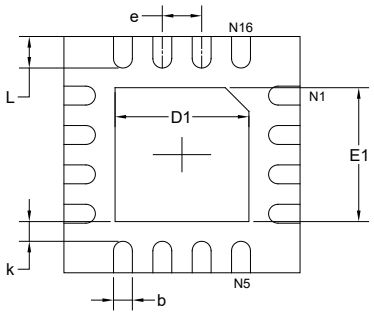
NOTES:
1. This drawing is subject to change without notice.
2. The dimensions do not include mold flashes, protrusions or gate burrs.
3. Reference JEDEC MO-153.

PACKAGE OUTLINE DIMENSIONS

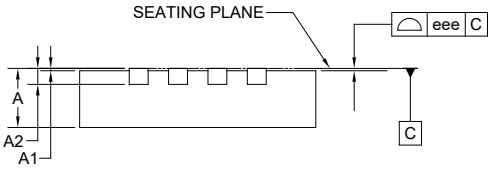
TQFN-3×3-16L



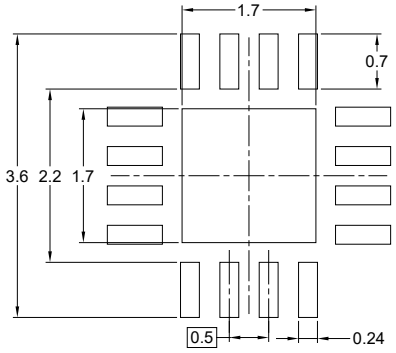
TOP VIEW



BOTTOM VIEW



SIDE VIEW



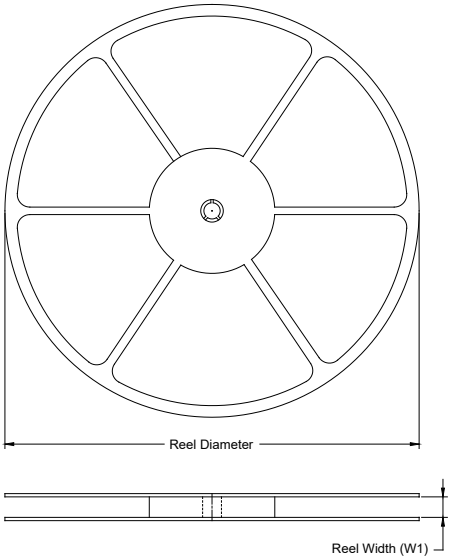
RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A2	0.203 REF		0.008 REF	
D	2.900	3.100	0.114	0.122
D1	1.600	1.800	0.063	0.071
E	2.900	3.100	0.114	0.122
E1	1.600	1.800	0.063	0.071
k	0.200 MIN		0.008 MIN	
b	0.180	0.300	0.007	0.012
e	0.500 TYP		0.020 TYP	
L	0.300	0.500	0.012	0.020
eee	0.080		0.003	

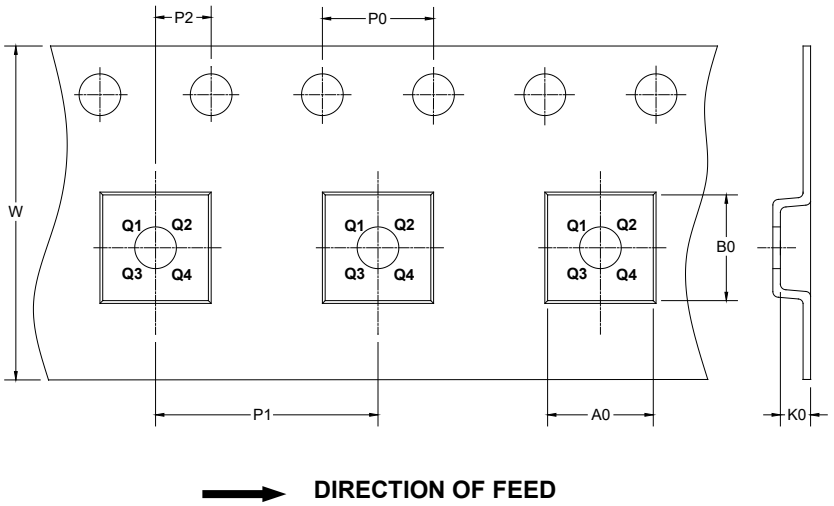
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



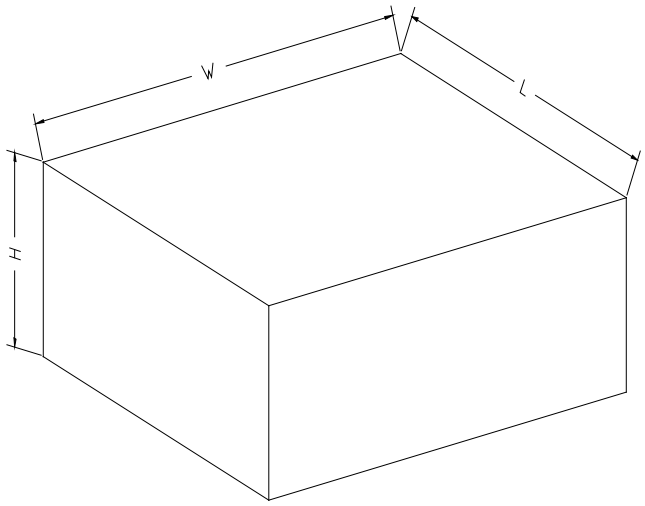
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
SOIC-16	13″	16.4	6.50	10.30	2.10	4.0	8.0	2.0	16.0	Q1
SSOP-16	13″	12.4	6.40	5.40	2.10	4.0	8.0	2.0	12.0	Q1
TSSOP-16	13″	12.4	6.90	5.60	1.50	4.0	8.0	2.0	12.0	Q1
TQFN-3×3-16L	13″	12.4	3.35	3.35	1.13	4.0	8.0	2.0	12.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002