SGM62125
3.5A Buck-Boost Converter with I²C Interface

GENERAL DESCRIPTION

The SGM62125 is a 4-switch Buck-Boost converter with programmable I²C interface for simple configuration of integrated rich features. Synchronous rectification improves system efficiency which is friendly for battery operated applications. In addition, the programmable light load PFM (pulse frequency modulation) mode and low quiescent current offer above 90% efficiency in the 10mA to 2.5A output current range.

The SGM62125 is capable to regulate the output voltage when the input voltage is below, above or equal to the output voltage. The mode transition is also optimized to ensure smooth operation and reduce output voltage ripple. The device implements peak current mode control architecture to achieve excellent load/line transient performance across the operating voltage range.

Dynamic voltage scaling is available via I²C controlled output voltage registers. The ADDR pin allows the programmability for I²C slave address and default start-up voltage.

The SGM62125 implements robust protection features such as over-temperature, input over-voltage, over-current, and short-circuit hiccup protections to protect device against unexpected system failure.

The SGM62125 is available in a Green WLCSP-1.46×2.3-15B package. High integration provides a compact solution with only four external components, allowing implementation in a PCB area as small as 39mm².

TYPICAL APPLICATION

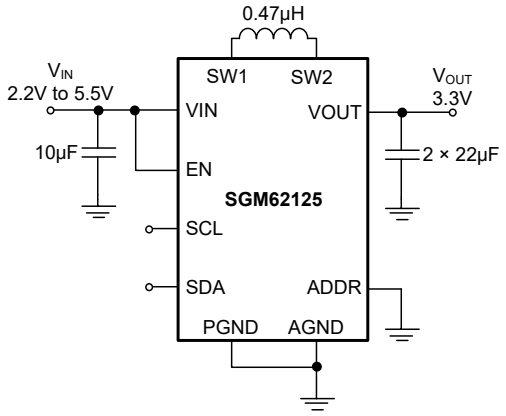


Figure 1. Typical Application Circuit

FEATURES

- 2.2V to 5.5V Input Voltage Range
  - 1.9V after Startup
- 1.8V to 5.5V Output Voltage Range
- Minimal Load Current Capability
  - 3.5A for V_{IN} ≥ 2.7V, V_{OUT} = 3.5V
  - 2.5A for V_{IN} ≥ 2.5V, V_{OUT} = 3.85V
  - 3.2A for V_{IN} ≥ 3V, V_{OUT} = 3.85V
- High Efficiency Performance
  - V_{IN} = 3.3V to 3.5V, V_{OUT} = 3.4V, I_{OUT} = 0.4A to 0.8A, η > 95%
  - V_{IN} = 3.8V, V_{OUT} = 3.4V, I_{OUT} = 0.4A to 0.8A, η > 95%
  - V_{IN} = 3.8V, V_{OUT} = 3.8V, I_{OUT} = 0.01A, η > 90%
- Load Transient Performance
  - V_{IN} = 3.8V, V_{OUT} = 3.45V, I_{OUT} = 0A to 1A, t_R = t_F = 10μs, Undershoot 100mV
- 2.25μA (TYP) Quiescent Current
- I²C Programmable FPWM and Ultrasonic Mode
- I²C Programmable Switching Frequency of 2.2MHz and 3.5MHz
- Slave Address and Default V_{OUT}
  - ADDR = High, 0x76h, 3.4V
  - ADDR = Low, 0x75h
    - 3.0V for SGM62125A
    - 2.5V for SGM62125B
    - 2.4V for SGM62125C
    - 2.6V for SGM62125D
  - ADDR = Floating, 0x77h, 3.6V
- DVS Step Size and Range: 50mV from 1.8V to 5.5V
- I²C Interface (Up to 1MHz Clock Speed)
  - Compatible with 3.3V, 1.8V and 1.2V I/O Logic
- Internal Soft-Start and Active Output Discharge
- OTP, Input OVP, OCP, Output OVP and Hiccup SCP
- Available in a Green WLCSP-1.46×2.3-15B Package

APPLICATIONS

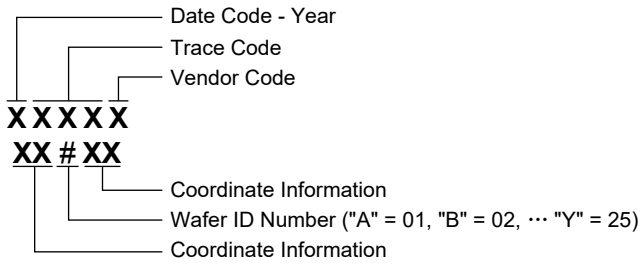
Smartphones, TWS and Tablets

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM62125A	WLCSP-1.46×2.3-15B	-40℃ to +125℃	SGM62125AXG/TR	62125A XXXXX XX#XX	Tape and Reel, 3000
SGM62125B	WLCSP-1.46×2.3-15B	-40℃ to +125℃	SGM62125BXG/TR	62125B XXXXX XX#XX	Tape and Reel, 3000
SGM62125C	WLCSP-1.46×2.3-15B	-40℃ to +125℃	SGM62125CXG/TR	62125C XXXXX XX#XX	Tape and Reel, 3000
SGM62125D	WLCSP-1.46×2.3-15B	-40℃ to +125℃	SGM62125DXG/TR	62125D XXXXX XX#XX	Tape and Reel, 3000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code. XX#XX = Coordinate Information and Wafer ID Number.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

VIN, VOUT Voltage ..... -0.3V to 6V
SCL, SDA, EN, ADDR Voltage ..... -0.3V to 6V
SW1, SW2 Voltage ..... -0.3V to 6V
Package Thermal Resistance
WLCSP-1.46×2.3-15B, θ_{JA} ..... 55℃/W
WLCSP-1.46×2.3-15B, θ_{JB} ..... 10.7℃/W
WLCSP-1.46×2.3-15B, θ_{JC} ..... 19.7℃/W
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility (1) (2)
HBM ..... ±3000V
CDM ..... ±1000V

NOTES:

1. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.

2. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

RECOMMENDED OPERATING CONDITIONS

Supply Voltage Range, V_{IN} ..... 1.9V to 5.5V
Output Voltage ..... 1.8V to 5.5V
EN Voltage ..... 0V to V_{IN}
Capacitance at V_{IN} = 2.5V to 5V, V_{OUT} = 3.3V, I_{OUT} = 2.2A
Effective Input Capacitance (1) ..... 5μF (MIN)
Effective Output Capacitance (1) ..... 16μF (13μF MIN)
Inductance ..... 100nH to 560nH (470nH TYP)
Operating Junction Temperature Range ..... -40℃ to +125℃

NOTE:

1. DC bias effect has been taken into account.

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

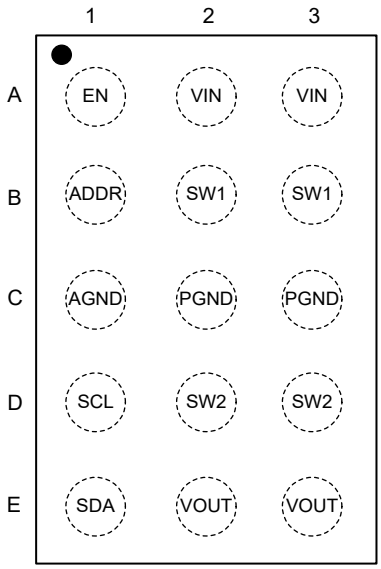
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

(TOP VIEW)



WLCSP-1.46×2.3-15B

PIN DESCRIPTION

PIN	NAME	TYPE	DESCRIPTION
A1	EN	I	Enable Input Pin. Pulling this pin logic high enables the device, logic low disables the device.
A2, A3	VIN	P	Input Power Supply.
B1	ADDR	I	I^2C Slave Address and Default Output Voltage Selection Pin.
B2, B3	SW1	P	Buck Switch Node Pin.
C1	AGND	G	Analog Ground Pin. Connect it to the PGND pins under the chip.
C2, C3	PGND	G	Power Ground Pin.
D1	SCL	I/O	I^2C Bus Clock Signal.
D2, D3	SW2	P	Boost Switch Node Pin.
E1	SDA	I/O	I^2C Bus Data Signal.
E2, E3	VOUT	O	Buck-Boost Converter Output Pin.

NOTE: I = Input, O = Output, I/O = Input and Output, G = Ground, P = Power.

ELECTRICAL CHARACTERISTICS

(V_{IN} = 3.6V, V_{OUT} = 3.3V, T_J = -40℃ to +125℃ and typical values are measured at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply						
Supply Current into VIN	I_Q	V_{IN} = V_{EN} = 3.6V, no switching, T_J = -40℃ to +85℃		2.25	5	μA
		V_{EN} = 3.6V, switching, no load, T_J = -40℃ to +85℃			20 (1)	
Shutdown Current into VIN	I_{SD}	V_{OUT} = V_{EN} = 0V, T_J = -40℃ to +85℃		0.2	2.5	μA
UVLO Rising Threshold Voltage	V_{UVLO_R}		2	2.1	2.2	V
UVLO Falling Threshold Voltage	V_{UVLO_F}	V_{OUT} < 2.2V	1.9	2	2.1	V
		V_{OUT} ≥ 2.2V	1.7	1.8	1.9	
UVLO Hysteresis Voltage	V_{HYS}			100		mV
POR Threshold Voltage	V_{POR}			1.7		V
I/O Signals						
Logic Voltage Rising Threshold	V_{IH}	For EN, ADDR, SDA, SCL			0.84	V
Logic Voltage Falling Threshold	V_{IL}	For EN, ADDR, SDA, SCL	0.36			V
High-Level Input Current	I_{IH}	For SCL, SDA, ADDR V_{SCL} = V_{SDA} = V_{ADDR} = 1.8V, no pull-up resistor		0.01	0.5	μA
Low-Level Input Current	I_{IL}	For SCL, SDA, ADDR V_{SCL} = V_{SDA} = 0V, no pull-up resistor		0.01	0.5	μA
Input Bias Current	I_{IB}	V_{EN} = 0V to 5.5V		0.01	0.5	μA
Power Stage						
Output Voltage Range	V_{OUT}		1.8		5.5	V
Output Voltage Initial Accuracy		PWM operation, T_J = -40℃ to +85℃	-1		1	%
		PFM operation, I_{OUT} ≥ 20mA, T_J = +25℃	-1		3	
Default Output Voltage	V_{OUT}	ADDR = high		3.4		V
		ADDR = low (SGM62125A)		3.0		
		ADDR = low (SGM62125B)		2.5		
		ADDR = low (SGM62125C)		2.4		
		ADDR = low (SGM62125D)		2.6		
		ADDR = floating		3.6		
Power FET R_{ON}	R_{ON_Q1}	I_{SW} = 1A		17		mΩ
	R_{ON_Q2}			16		
	R_{ON_Q3}			17		
	R_{ON_Q4}			21		
Switch Current Limit	I_{LIM}	V_{IN} = 4.1V, PWM operation, T_J = +25℃	6.5	7.5	8.5	A
		V_{IN} = 4.8V, V_{OUT} = 3.3V, FPWM operation, output sink current		-1.5		
PFM Exit Threshold (Peak) Current	I_{T_PFM}	V_{IN} = 4.2V		0.3		A
Output Discharge Current	I_{DIS}	V_{OUT} ≥ 0.8V	30	130		mA
Output Voltage Rising Power-Good Threshold	V_{T+}			96		%
Output Voltage Falling Power-Good Threshold	V_{T-}			90		%
VIN Rising Over-Voltage Threshold				5.8		V
Ultrasonic Mode	f_{USM}	Ultrasonic mode operation, I_{OUT} = 1mA		30		kHz
		V_{OUT} = V_{EN} = 3.6V			10	mA
Thermal Shutdown						
Thermal Shutdown Threshold	T_{SD}	T_J rising		150		℃
Thermal Shutdown Hysteresis	T_{HYS}			20		℃

NOTE: 1. Guaranteed by design.

TIMING REQUIREMENTS

(V_{IN} = 2.2V to 5.5V and T_J = -40℃ to +125℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCL Clock Frequency	f_{SCL}	Standard mode			100	kHz
		Fast mode			400	
		Fast mode plus			1000	
SCL Clock Low Period	t_{LOW}	Standard mode	4.7			μs
		Fast mode	1.3			
		Fast mode plus	0.5			
SCL Clock High Period	t_{HIGH}	Standard mode	4			μs
		Fast mode	0.6			
		Fast mode plus	0.26			
Bus Free Time between a STOP and a START Conditions	t_{BUF}	Standard mode	4.7			μs
		Fast mode	1.3			
		Fast mode plus	0.5			
Setup Time for a Repeated START Condition	$t_{SU,STA}$	Standard mode	4.7			μs
		Fast mode	0.6			
		Fast mode plus	0.26			
Hold Time (Repeated) START Condition	$t_{HD,STA}$	Standard mode	4			μs
		Fast mode	0.6			
		Fast mode plus	0.26			
Data Setup Time	$t_{SU,DAT}$	Standard mode	250			ns
		Fast mode	100			
		Fast mode plus	50			
Data Hold Time	$t_{HD,DAT}$	Standard mode	0			μs
		Fast mode	0			
		Fast mode plus	0			
Rise Time of SDA and SCL Signals	t_{RS}	Standard mode			1000	ns
		Fast mode	20		300	
		Fast mode plus			120	
Fall Time of SDA and SCL Signals	t_{FS}	Standard mode			300	ns
		Fast mode	$20 \times V_{DD}/5.5$		300	
		Fast mode plus	$20 \times V_{DD}/5.5$		120	
Setup Time for STOP Condition	$t_{SU,STO}$	Standard mode	4			μs
		Fast mode	0.6			
		Fast mode plus	0.26			
Data Valid Time	$t_{VD,DAT}$	Standard mode			3.45	μs
		Fast mode			0.9	
		Fast mode plus			0.45	
Data Valid Acknowledge Time	$t_{VD,ACK}$	Standard mode			3.45	μs
		Fast mode			0.9	
		Fast mode plus			0.45	
Capacitive Load on Each Bus Line	C_B	Standard mode			400	pF
		Fast mode			400	
		Fast mode plus			550	
ADDR Pulse Duration	t_{w_ADDR}	ADDR = high or low	5			μs

SWITCHING CHARACTERISTICS

(V_{IN} = 3.6V, V_{OUT} = 3.3V and T_J = -40℃ to +125℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
EN Rising Edge to Output Ramp Start Delay	t_{D_EN}	T_J = +25℃, V_{IN} = 5V		215		μs
Power-Good Delay	t_{D_PG}	V_{OUT} falling		2.0		ms
Slew Rate of Internal Ramp during Dynamic Voltage Scaling	SR	SLEW[1:0] = 00, FPWM operation		±1		V/ms
		SLEW[1:0] = 01, FPWM operation		±2.5		
		SLEW[1:0] = 10, FPWM operation		±5		
		SLEW[1:0] = 11, FPWM operation		±10		
Switching Frequency (1)	f_{SW}	Buck or Boost operation, V_{IN} = 5V		2.2		MHz
				3.5		
Soft-Start	t_{SS}	V_{OUT} from 0V to 0.95 × V_{OUT}		0.3	1 (2)	ms

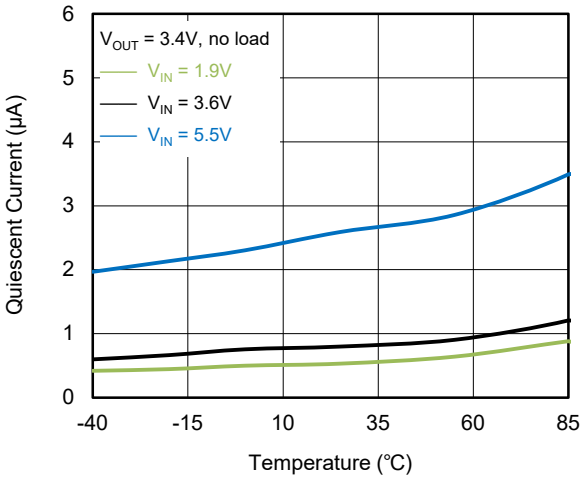
NOTES:

1. The switching frequency can be configured via I²C, with a default value of 2.2MHz.
2. Guaranteed by design.

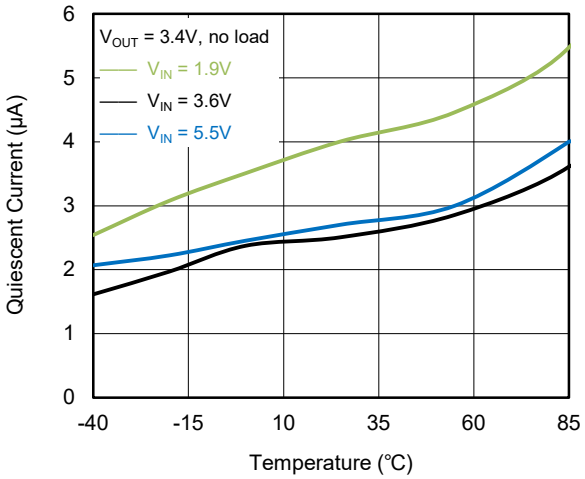
TYPICAL PERFORMANCE CHARACTERISTICS for 2.2MHz

V_{OUT} = 3.4V, T_A = +25℃, unless otherwise noted.

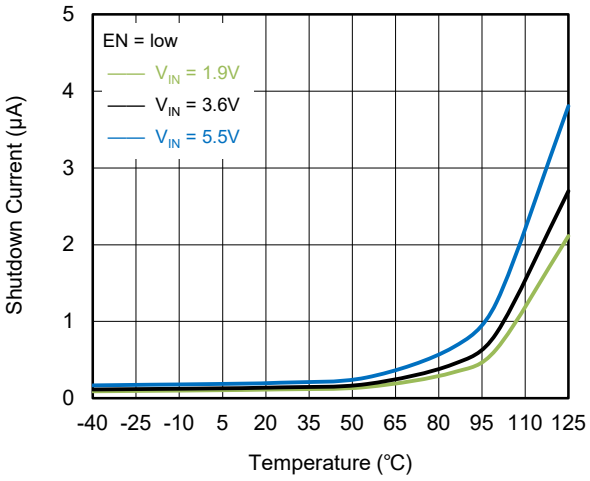
Quiescent Current vs. Temperature (No Switching)



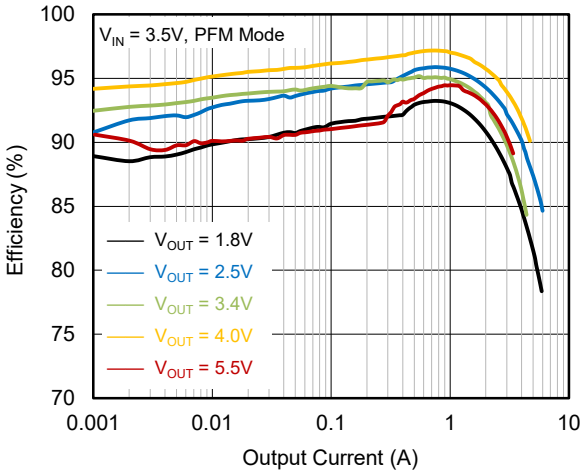
Quiescent Current vs. Temperature (Switching)



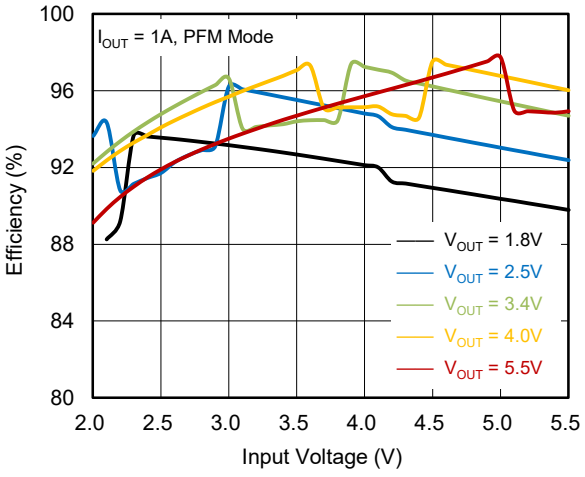
Shutdown Current vs. Temperature



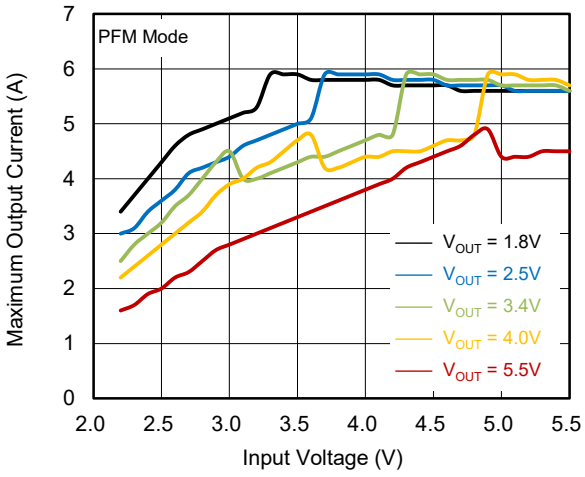
Efficiency vs. Output Current



Efficiency vs. Input Voltage



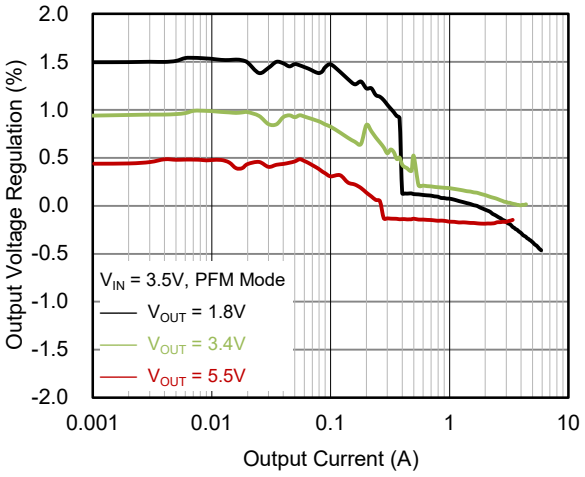
Maximum Output Current vs. Input Voltage



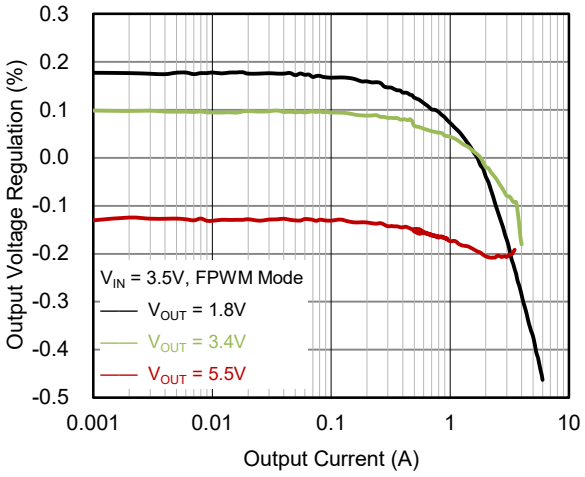
TYPICAL PERFORMANCE CHARACTERISTICS for 2.2MHz (continued)

V_{OUT} = 3.4V, T_A = +25℃, unless otherwise noted.

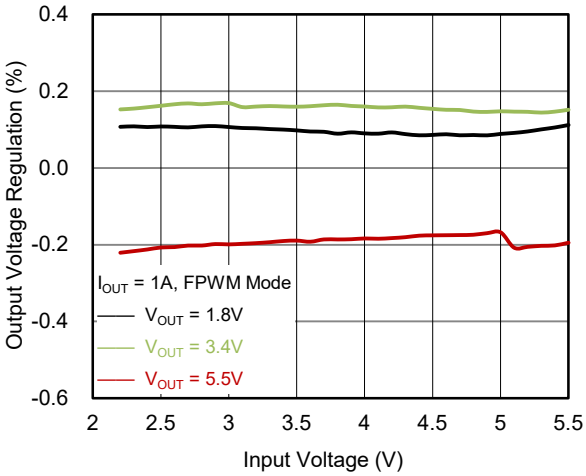
Load Regulation



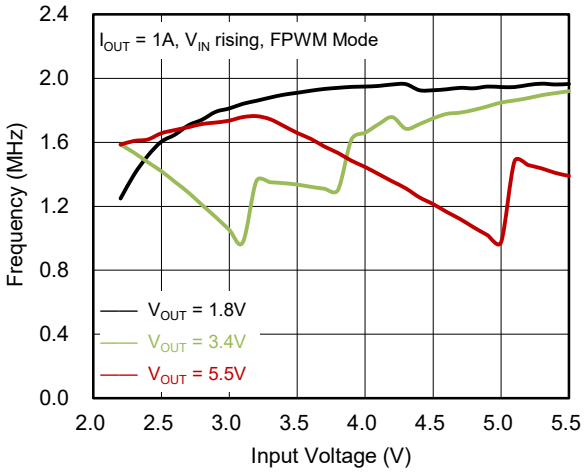
Load Regulation



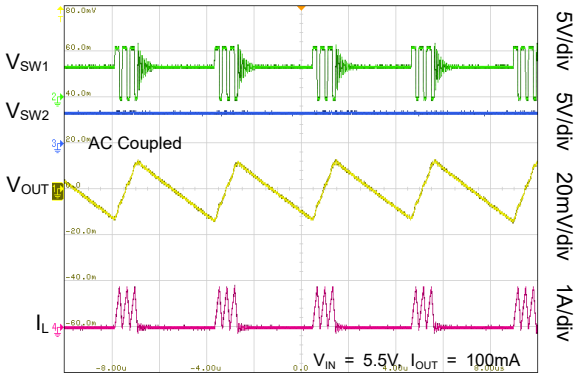
Line Regulation



Switching Frequency vs. Input Voltage

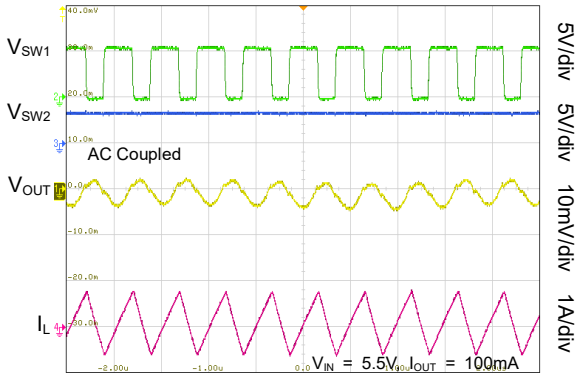


PFM Switching Waveforms in Buck Mode



Time (2μs/div)

FPWM Switching Waveforms in Buck Mode

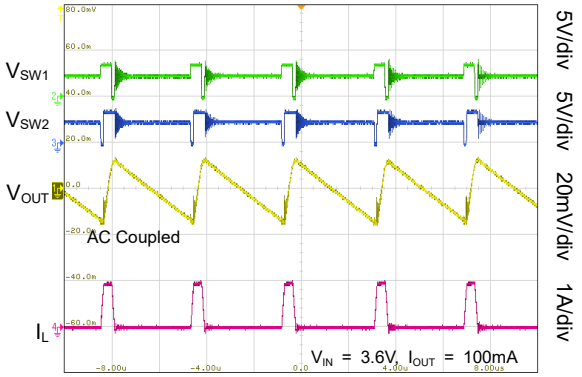


Time (500ns/div)

TYPICAL PERFORMANCE CHARACTERISTICS for 2.2MHz (continued)

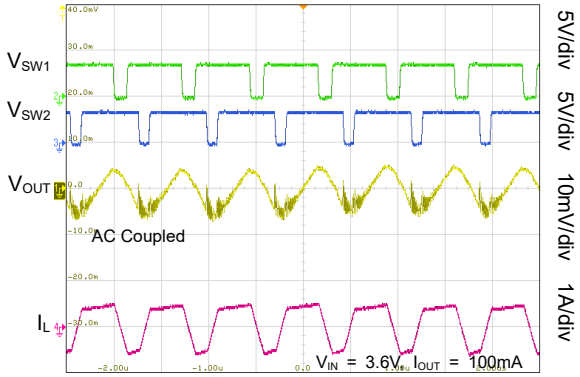
V_{OUT} = 3.4V, T_A = +25℃, unless otherwise noted.

PFM Switching Waveforms in Buck-Boost Mode



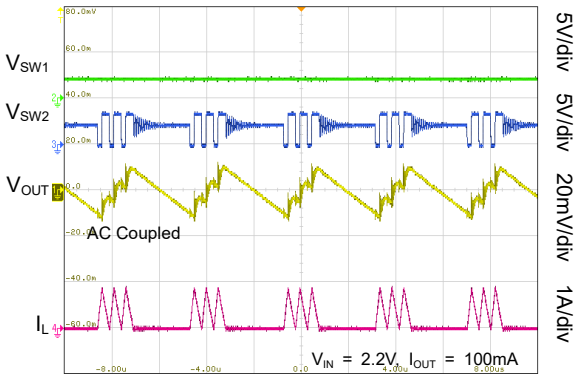
Time (2μs/div)

FPWM Switching Waveforms in Buck-Boost Mode



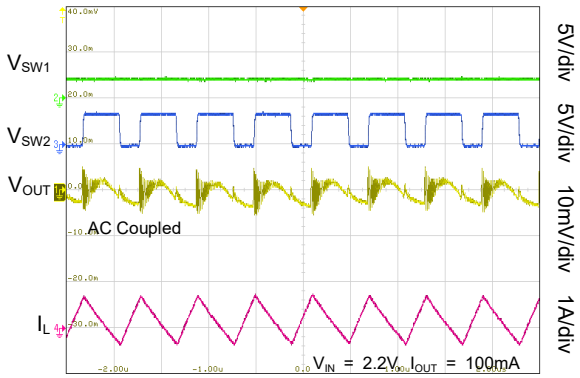
Time (500ns/div)

PFM Switching Waveforms in Boost Mode



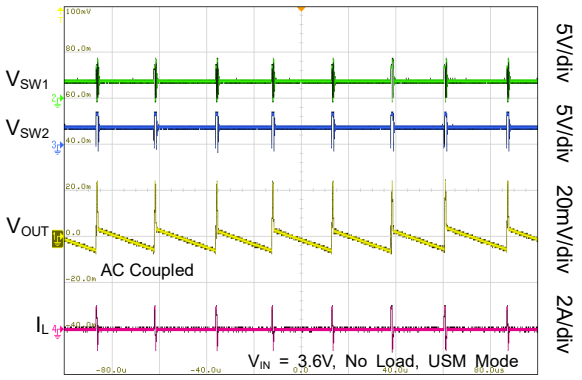
Time (2μs/div)

FPWM Switching Waveforms in Boost Mode



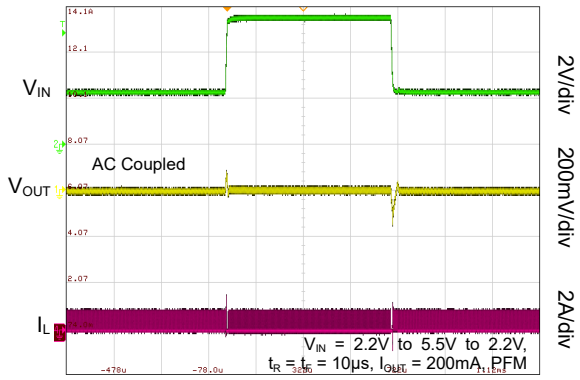
Time (500ns/div)

Ultrasonic Mode



Time (20μs/div)

Line Transient Response under Light Load

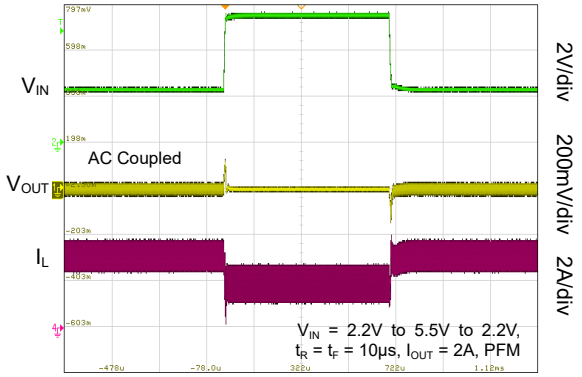


Time (200μs/div)

TYPICAL PERFORMANCE CHARACTERISTICS for 2.2MHz (continued)

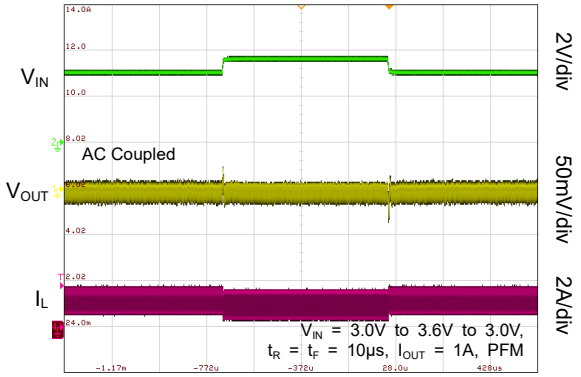
V_{OUT} = 3.4V, T_A = +25℃, unless otherwise noted.

Line Transient Response under Heavy Load



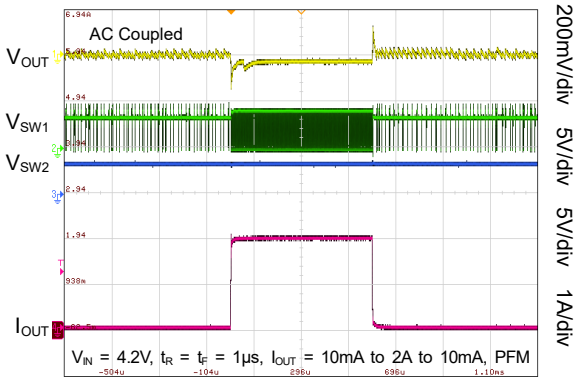
Time (200μs/div)

Line Transient Response (Typical Condition)



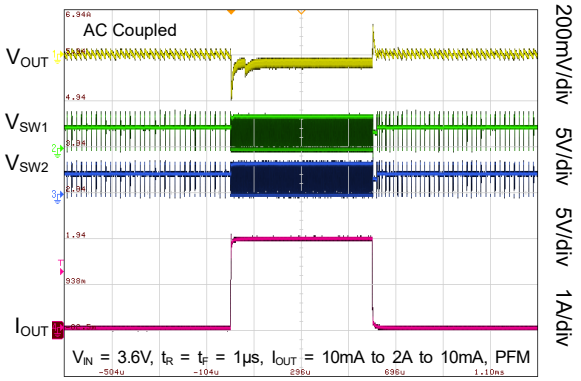
Time (200μs/div)

Load Transient Response in Buck Mode



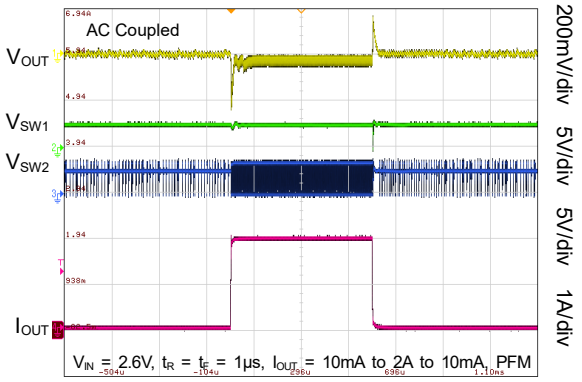
Time (200μs/div)

Load Transient Response in Buck-Boost Mode



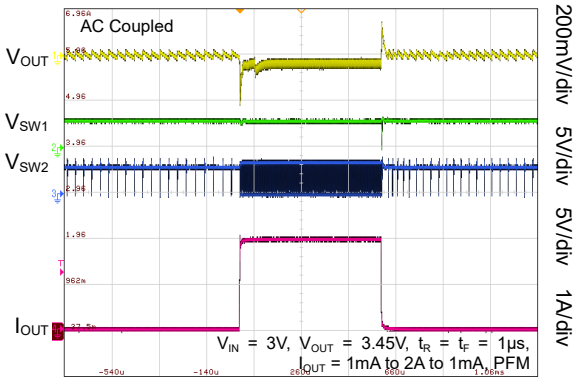
Time (200μs/div)

Load Transient Response in Boost Mode



Time (200μs/div)

Load Transient Response (Typical Condition 1)

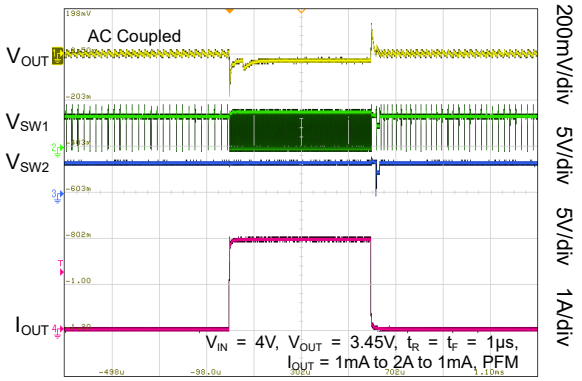


Time (200μs/div)

TYPICAL PERFORMANCE CHARACTERISTICS for 2.2MHz (continued)

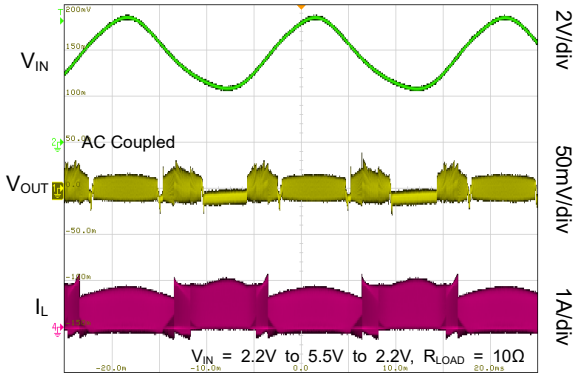
V_{OUT} = 3.4V, T_A = +25℃, unless otherwise noted.

Load Transient Response (Typical Condition 2)



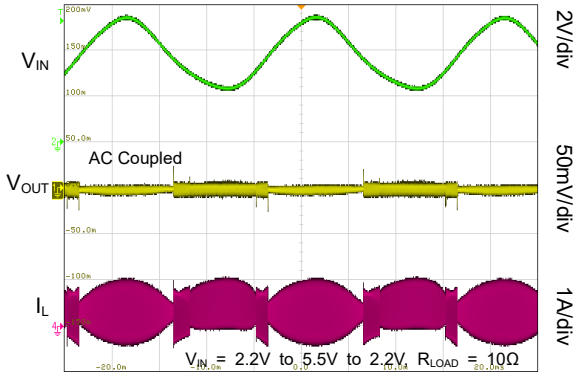
Time (200μs/div)

Line Sweep under PFM



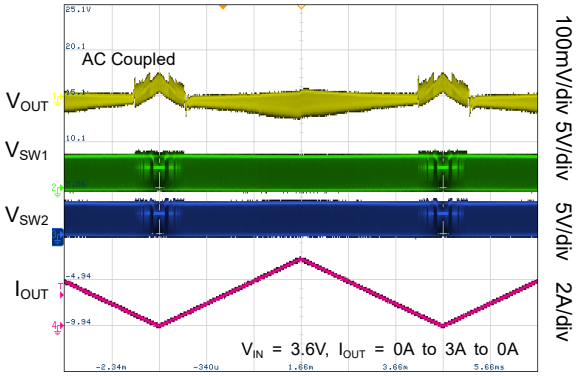
Time (5ms/div)

Line Sweep under FPWM



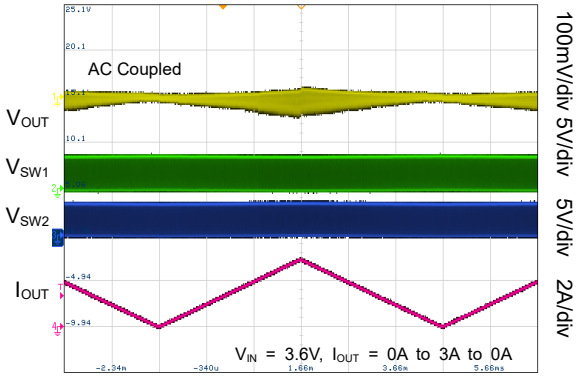
Time (5ms/div)

Load Sweep under PFM



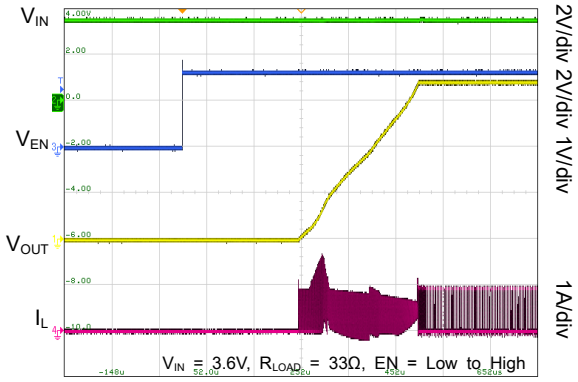
Time (1ms/div)

Load Sweep under FPWM



Time (1ms/div)

Startup under Light Load

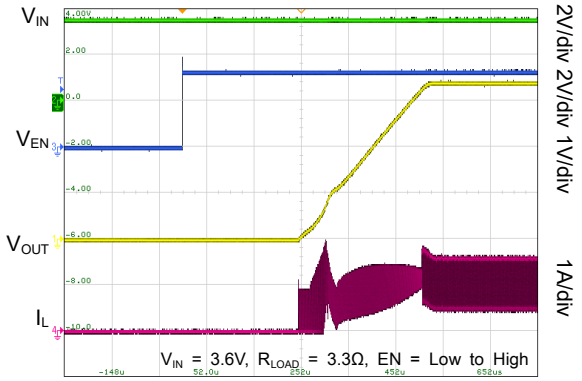


Time (100μs/div)

TYPICAL PERFORMANCE CHARACTERISTICS for 2.2MHz (continued)

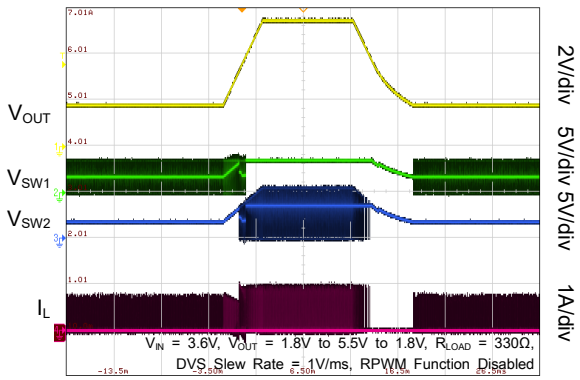
V_{OUT} = 3.4V, T_A = +25℃, unless otherwise noted.

Startup under Heavy Load



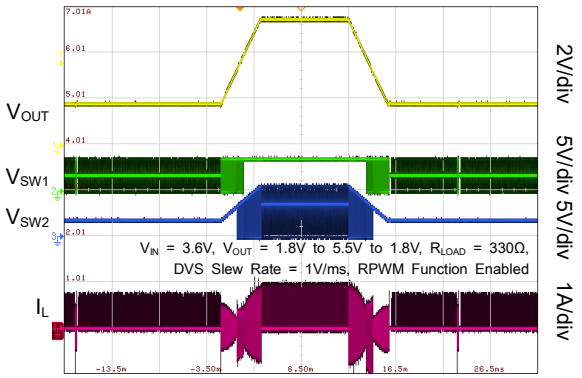
Time (100μs/div)

Dynamic Voltage Scaling under PFM



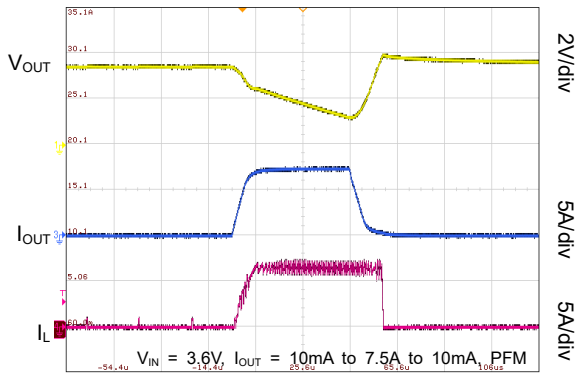
Time (5ms/div)

Dynamic Voltage Scaling under RPWM



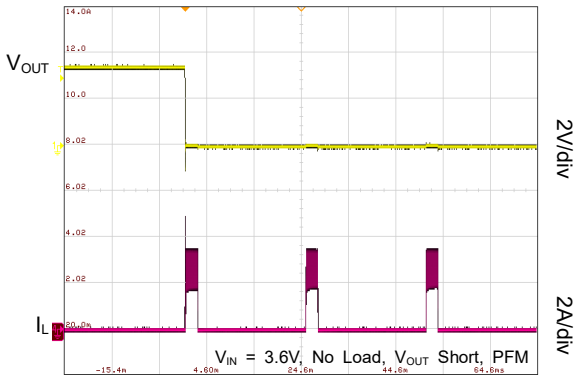
Time (5ms/div)

Over-Current Protection



Time (20μs/div)

Short-Circuit Protection

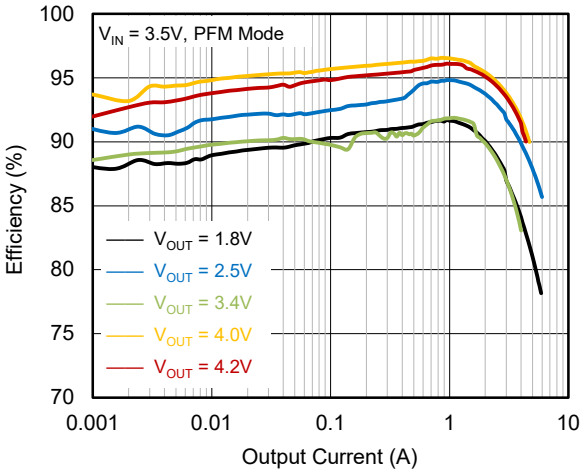


Time (10ms/div)

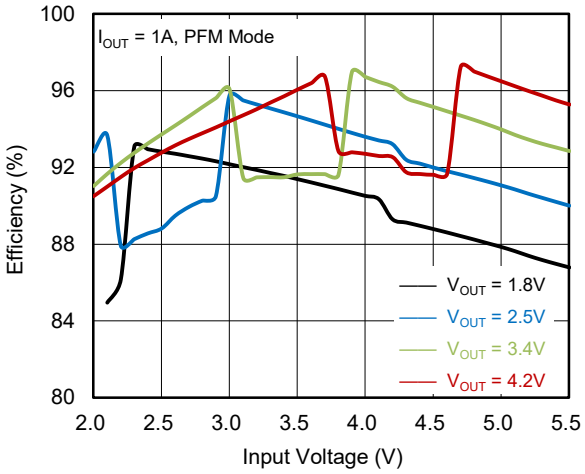
TYPICAL PERFORMANCE CHARACTERISTICS for 3.5MHz

V_{OUT} = 3.4V, T_A = +25℃, unless otherwise noted.

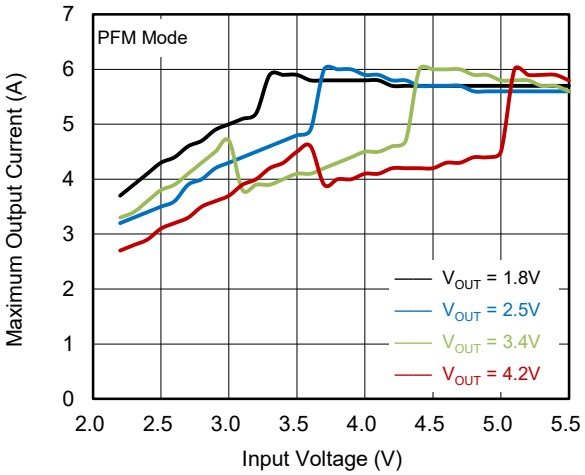
Efficiency vs. Output Current



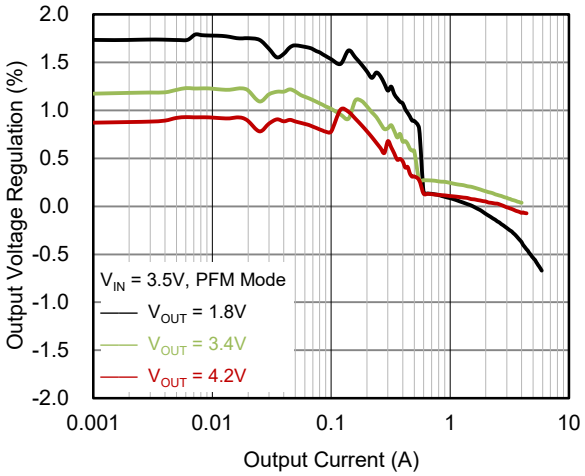
Efficiency vs. Input Voltage



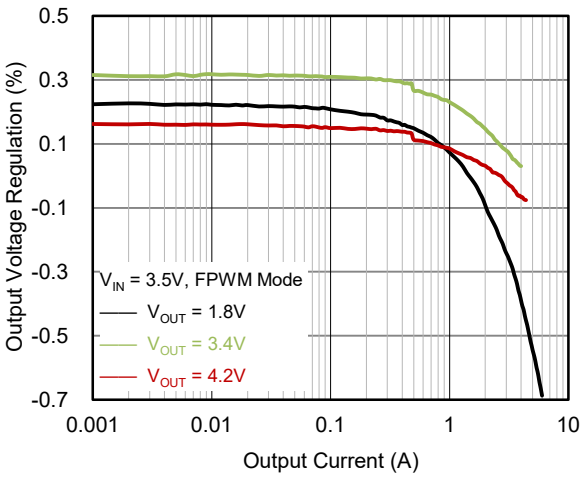
Maximum Output Current vs. Input Voltage



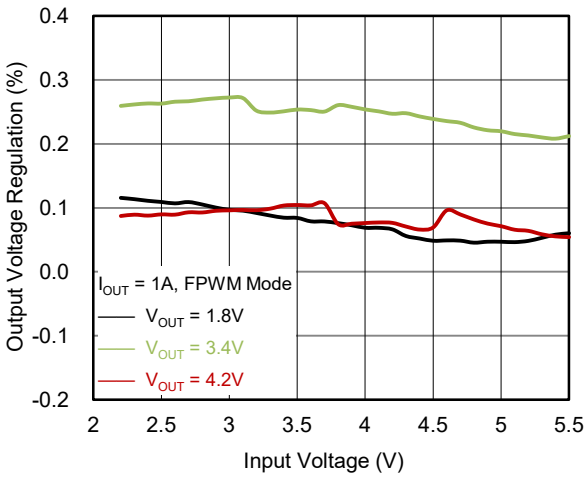
Load Regulation



Load Regulation



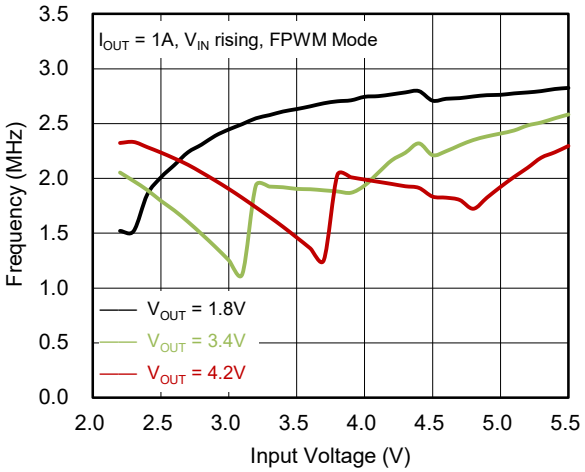
Line Regulation



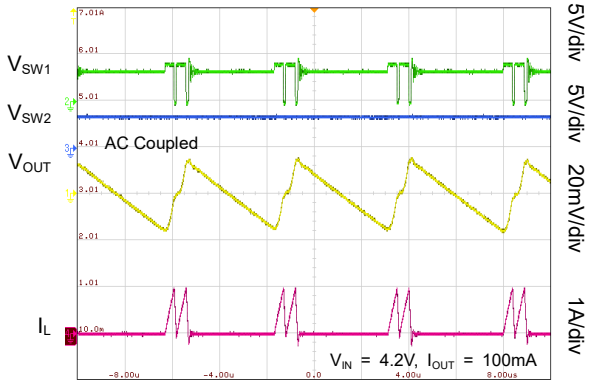
TYPICAL PERFORMANCE CHARACTERISTICS for 3.5MHz (continued)

V_{OUT} = 3.4V, T_A = +25℃, unless otherwise noted.

Switching Frequency vs. Input Voltage

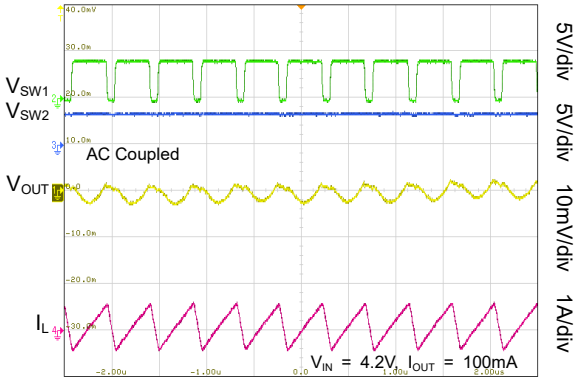


PFM Switching Waveforms in Buck Mode



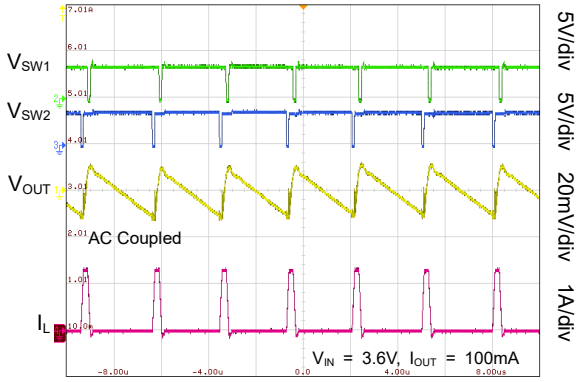
Time (2μs/div)

FPWM Switching Waveforms in Buck Mode



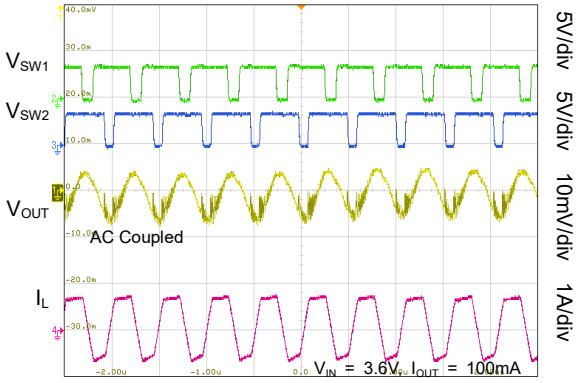
Time (500ns/div)

PFM Switching Waveforms in Buck-Boost Mode



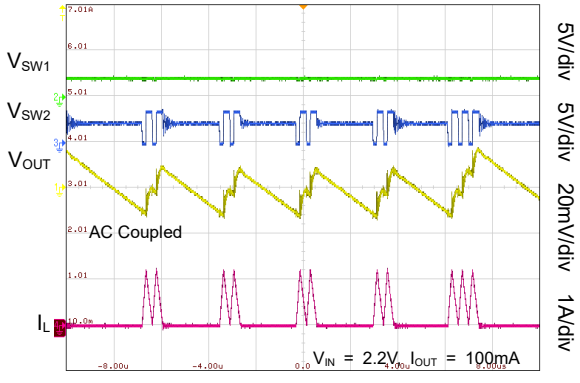
Time (2μs/div)

FPWM Switching Waveforms in Buck-Boost Mode



Time (500ns/div)

PFM Switching Waveforms in Boost Mode

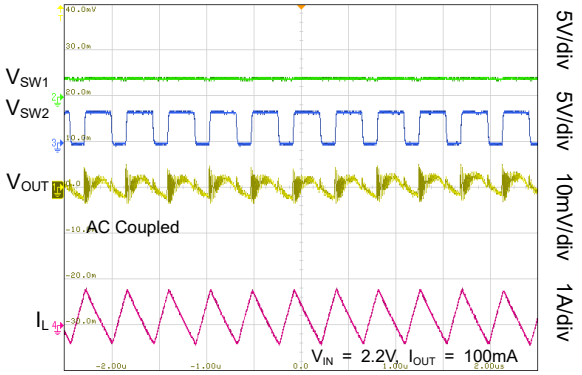


Time (2μs/div)

TYPICAL PERFORMANCE CHARACTERISTICS for 3.5MHz (continued)

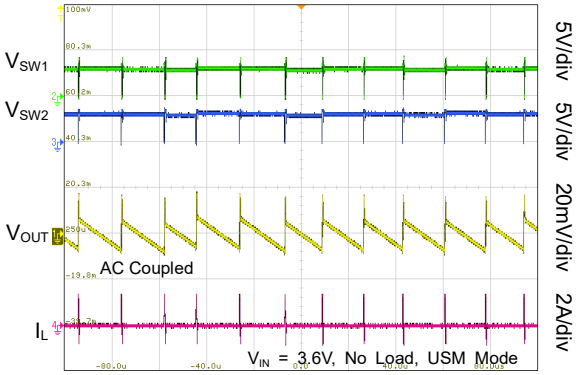
V_{OUT} = 3.4V, T_A = +25℃, unless otherwise noted.

FPWM Switching Waveforms in Boost Mode



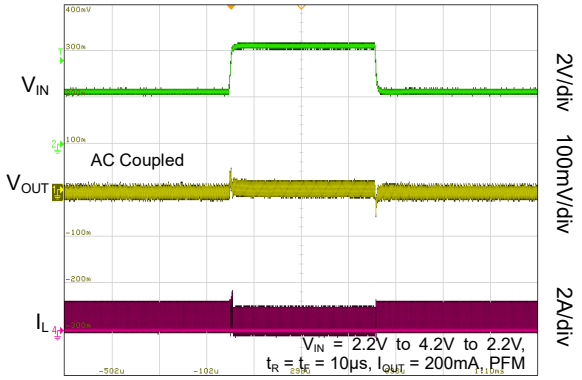
Time (500ns/div)

Ultrasonic Mode



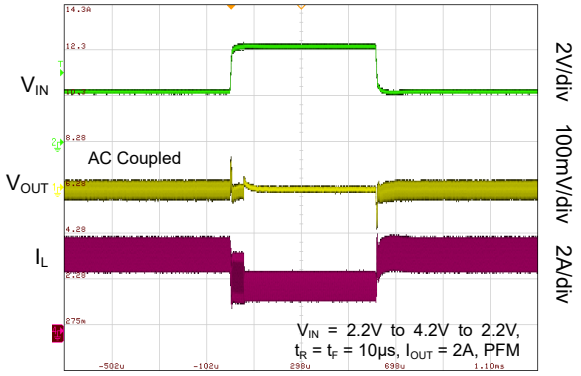
Time (20μs/div)

Line Transient Response under Light Load



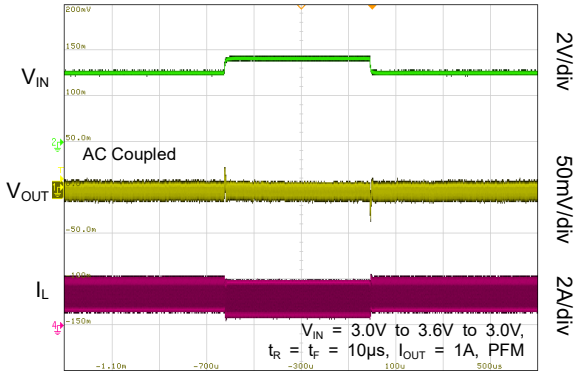
Time (200μs/div)

Line Transient Response under Heavy Load



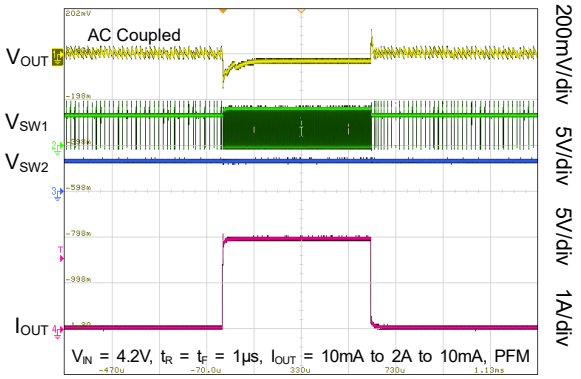
Time (200μs/div)

Line Transient Response (Typical Condition)



Time (200μs/div)

Load Transient Response in Buck Mode

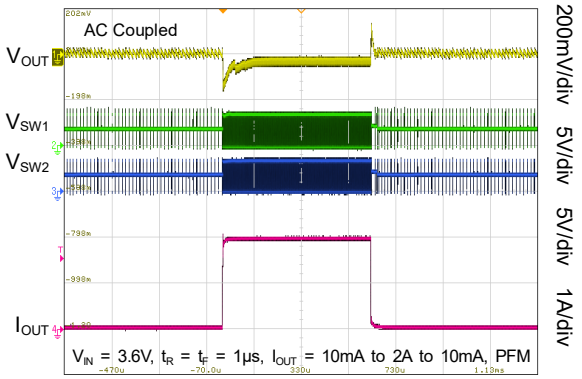


Time (200μs/div)

TYPICAL PERFORMANCE CHARACTERISTICS for 3.5MHz (continued)

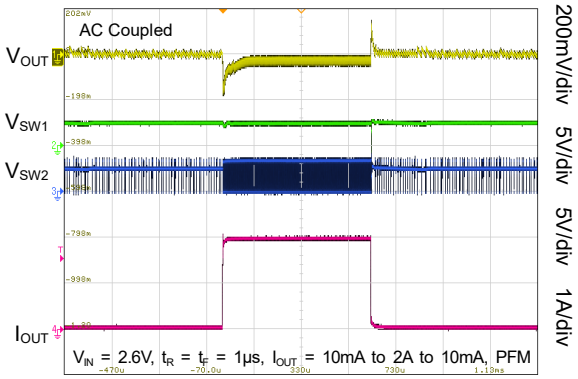
V_{OUT} = 3.4V, T_A = +25℃, unless otherwise noted.

Load Transient Response in Buck-Boost Mode



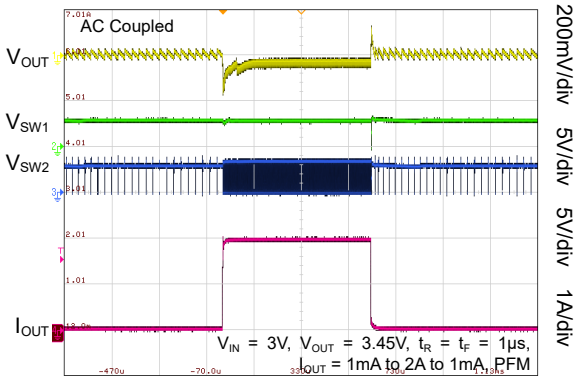
Time (200μs/div)

Load Transient Response in Boost Mode



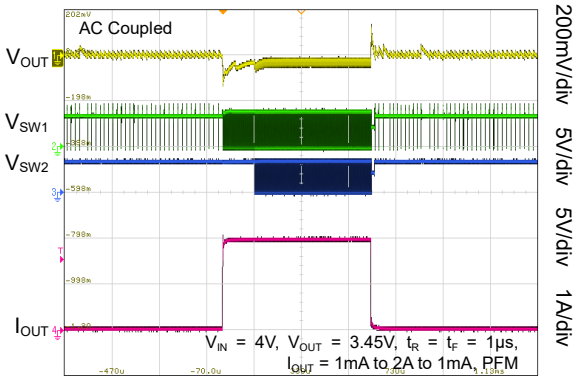
Time (200μs/div)

Load Transient Response (Typical Condition 1)



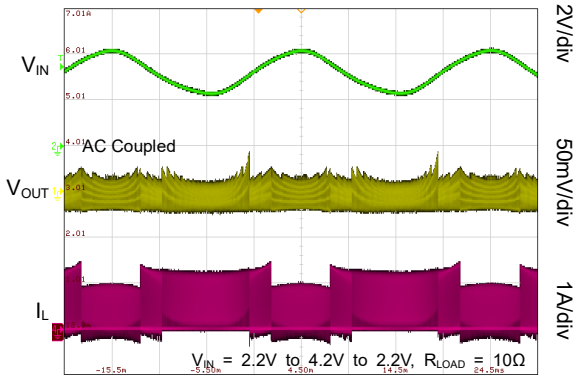
Time (200μs/div)

Load Transient Response (Typical Condition 2)



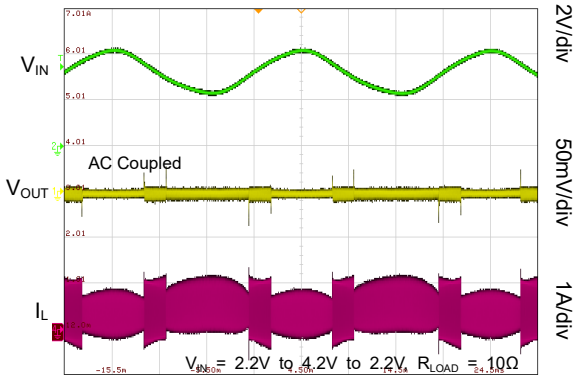
Time (200μs/div)

Line Sweep under PFM



Time (5ms/div)

Line Sweep under FPWM

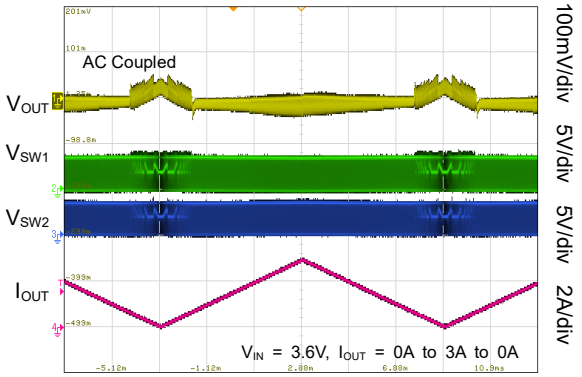


Time (5ms/div)

TYPICAL PERFORMANCE CHARACTERISTICS for 3.5MHz (continued)

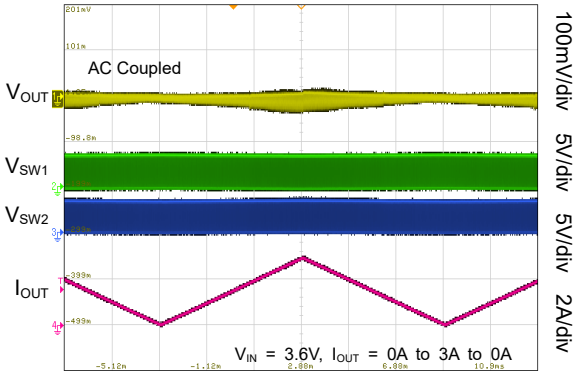
V_{OUT} = 3.4V, T_A = +25℃, unless otherwise noted.

Load Sweep under PFM



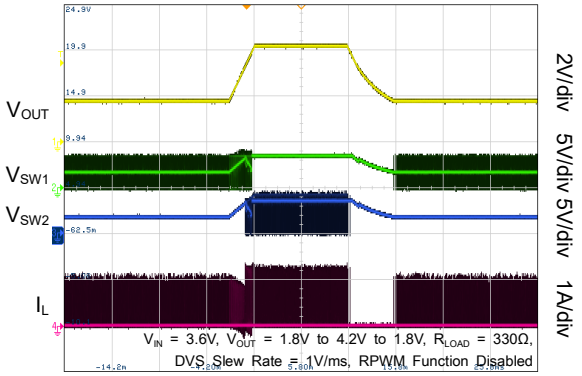
Time (2ms/div)

Load Sweep under FPWM



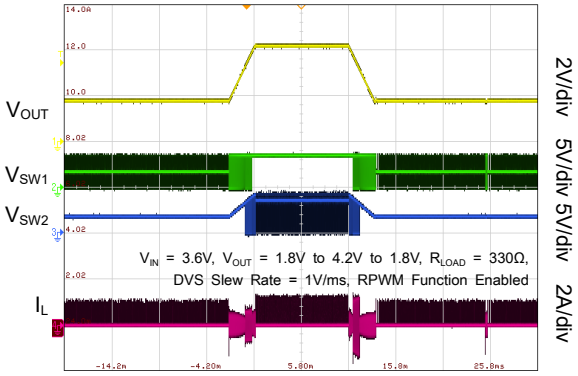
Time (2ms/div)

Dynamic Voltage Scaling under PFM



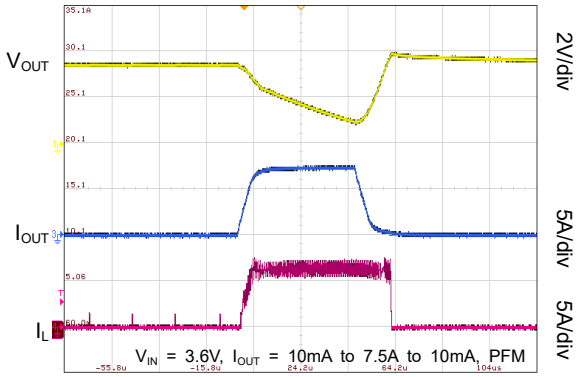
Time (5ms/div)

Dynamic Voltage Scaling under RPWM



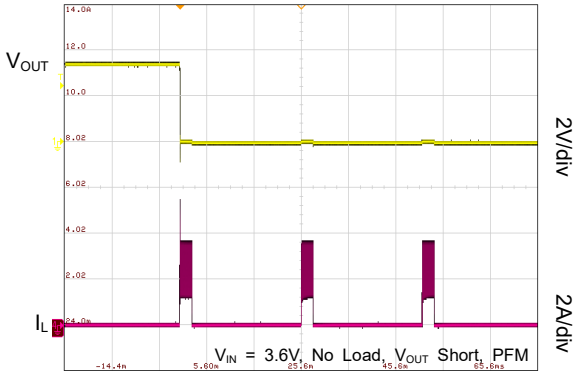
Time (5ms/div)

Over-Current Protection



Time (20μs/div)

Short-Circuit Protection



Time (10ms/div)

FUNCTIONAL BLOCK DIAGRAM

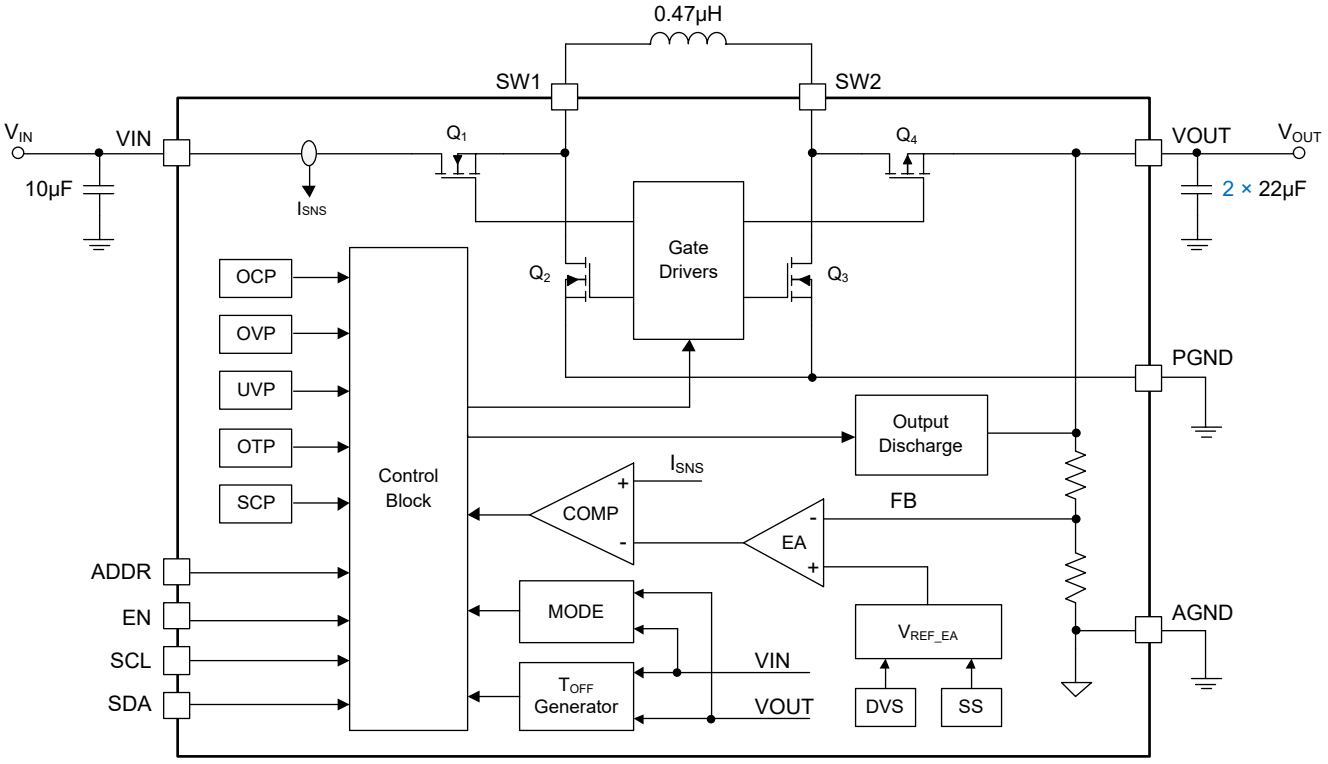


Figure 2. Block Diagram

DETAILED DESCRIPTION

Overview

The SGM62125 is a synchronous Buck-Boost converter with integrated switches that can operate over a wide input voltage and output current range with high efficiency. It is capable to change mode automatically among Buck, Boost and Buck-Boost depending on the input and output condition. When V_{IN} >> V_{OUT}, the device is in Buck mode, when V_{IN} << V_{OUT}, the device is in Boost mode, and when V_{OUT} ~ V_{IN}, the device is in 4-cycle Buck-Boost mode. In the Buck-Boost mode, the 4-cycle operation controls the four switches to turn on/off alternately to reduce the RMS current in the inductor and output capacitors to maintain low output voltage ripple and achieve high efficiency across entire input voltage range.

Mode Toggle

The SGM62125 automatically selects the operation mode based on the input and output voltages to maintain output voltage regulation.

Buck Mode

When V_{IN} >> V_{OUT}, the device operates as a Buck converter as shown in Figure 3. Q_1 is the control switch, Q_2 is the synchronous rectifier, Q_3 is off and Q_4 is always on. In Buck mode, each switching cycle has two phases (switch on and off). Note that Q_4 is P-channel MOSFET which eliminates the need for external bootstrap capacitor. Q_1 is a N-channel MOSFET with integrated bootstrap capacitor.

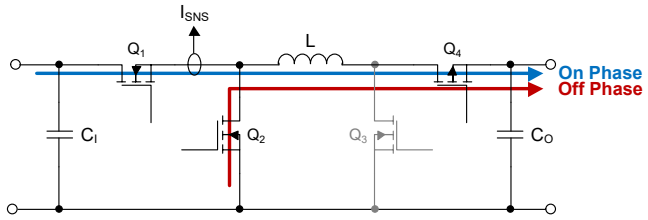


Figure 3. Buck Mode Switching

Boost Mode

If V_{IN} << V_{OUT}, the device operates as a Boost converter (see Figure 4). In the Boost mode, Q_1 is always on, Q_2 is off, Q_3 is the control switch, and Q_4 acts as the synchronous rectifier. Each cycle has two phases (switch on and off).

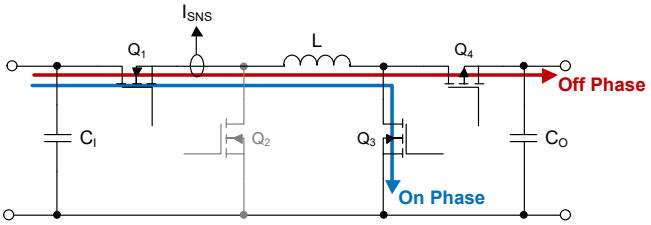


Figure 4. Boost Mode Switching

For small duty Boost mode operation where input voltage is close to the output voltage, bit [3] in the CONFIG register can be used to program the frequency foldback threshold. Default setting satisfies most application requirements, when programmed to 1, switching frequency will foldback more with the tradeoff increased output voltage ripple when the input voltage is close to output voltage.

Buck-Boost Mode

When V_{OUT} ~ V_{IN}, all four switches are controlled in a continuously on manner. The internal control loop controls all 4 switches adaptively based on the load, input voltage and output voltage. The inductor current is regulated to ensure output voltage regulation and load current delivery.

Control Scheme

The SGM62125 employs peak current mode control scheme. The error amplifier (EA) output of the output voltage loop sets the desired current loop threshold for PWM duty cycle control as well as modes of operation. The on phase is terminated and the next phase(s) of the switching cycle will start if the sensed peak inductor current (I_{LM}) reaches the reference signal from the error amplifier.

The off-time is a function of V_{IN} and V_{OUT} and the Buck, Boost or Buck-Boost operating mode of the converter.

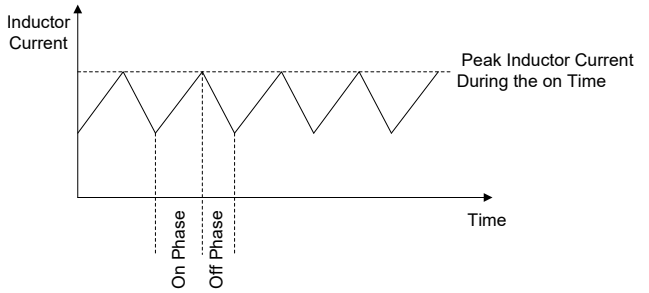


Figure 5. Buck or Boost Mode Peak Current Control

DETAILED DESCRIPTION (continued)

When the forced PWM (FPWM) mode is configured in the control register, the SGM62125 remains in continuous conduction mode even if the inductor current is negative, which causes current to flow in the reversed direction. During the negative current phase, the error amplifier will provide a negative reverse peak current threshold (-1.5A, TYP) for the inner current loop which causes the inductor's average current in reversed direction to become more negative. Therefore, as shown in Figure 6, smaller current limit levels must be used for the reverse current.

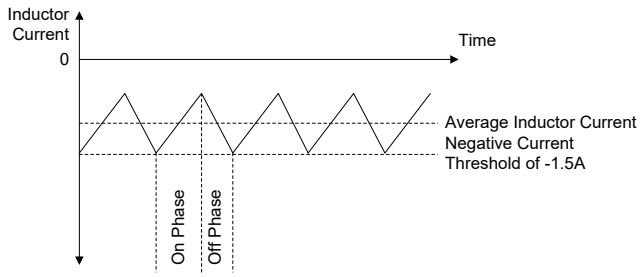


Figure 6. Buck or Boost Mode Reverse Peak Current Control

Power-Save Mode (PSM)

During startup, the device will be forced to operate in PSM mode until power-good status is reached for the first time. The default value for FPWM bit is 0 for PSM mode.

When PSM mode is configured, in medium to heavy load condition, the SGM62125 operates in the continuous current mode with constant switching frequency mode. To improve the efficiency at light load condition, the device switches to the PSM. In PSM, a sequence of on pulses is issued to charge up the output voltage, as the output voltage falls below the programmed voltage, the sequence is issued, this cycle repeats. The PSM switching frequency varies with load current.

In PSM, switching loss is reduced due to the reduced switching cycles. Some of the internal blocks are turned off in PSM to further improve the light load efficiency, however, output voltage ripple, DC output voltage accuracy and load transient performance are reduced in PSM (see Table 1).

Table 1. Comparison of the FPWM and PFM Performances

Parameter	Best Operating Mode
Low-Power Efficiency	PFM
DC Output Voltage Accuracy	FPWM
Transient Response	FPWM
Output Voltage Ripple	FPWM

Forced PWM (FPWM) Operation

Forced PWM mode is enabled via setting the FPWM bit to 1 in the control register. In the FPWM mode, in light load condition, the synchronous switches are not turned off when the inductor current goes negative to maintain a constant switching frequency. FPWM operation has lower output voltage ripple and better transient response compared to PFM. However, in the lower output currents, FPWM results in higher switching and conduction loss thus lower efficiency.

Device Enable (EN)

The SGM62125 implements an EN pin to enable the device. Apply a logic high signal on the EN pin, and the input voltage is above the UVLO rising threshold of 2.1V (TYP), the device starts switching and ramps the output voltage towards the programmed output voltage.

Under-Voltage Lockout (UVLO)

The under-voltage lockout feature disables the device when the input supply voltage is too low to prevent the device from malfunction. As the device turns on to regulate the output voltage, the device's power stage is supplied by the output voltage if the input voltage falls below the output voltage. If the programmed output voltage is higher than 2.2V, the SGM62125 is capable to operate down to 1.9V (MAX) before shutdown. If the programmed output voltage is lower than 2.2V, the SGM62125 is capable to operate down to 2.1V (MAX) before shutdown.

Switching Frequency

The SGM62125 is able to operate with 2.2MHz or 3.5MHz switching frequency to adapt with different inductor selection. Switching frequency is programmable via the FSW bit in the 0x04 register. 0.47μH inductance is recommended with 2.2MHz option, and 0.22μH inductance is recommended with 3.5MHz option.

DETAILED DESCRIPTION (continued)

Soft-Start

During startup, the built-in soft-start function will minimize the inrush current and limit the output voltage overshoot. When the device is turned on or enabled, the internal reference voltage follows an internal RC ramp to charge the output voltage. As the RC voltage ramps up, the device controls the inrush current based on loading condition and amount of output capacitance. The typical soft-start time for SGM62125 is 300μs. During soft-start period, the current limit is programmable to 25%, 50% or 75% of peak current limit to effectively minimize the inrush current drawn from the supply via CONFIG register bits [7:6]. This current limit foldback is also effective for hiccup on duration.

For startup into large output capacitance and high load current, the inductor current could reach current limit during startup. After soft-start time is expired, the current limit is released to full range.

nPG bit remains unchanged during successful startup, if the output voltage fails to reach power-good threshold (90% of programmed output) after 2ms programmable deglitch, the nPG bit is toggled to logic high.

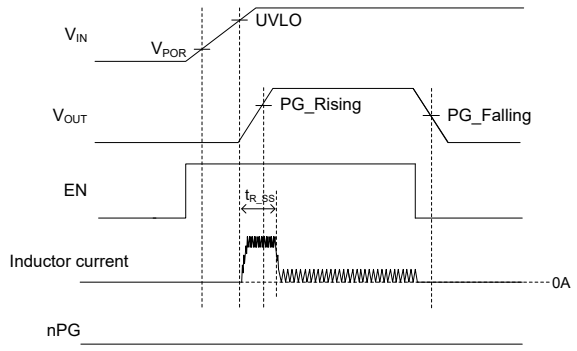


Figure 7. Startup Performance

Table 2 summarizes the nPG signal behavior during startup and shutdown.

Table 2. nPG Behavior

Application Case	nPG Behavior
Successful Startup	Remain Low
Unsuccessful Startup	Toggle to logic high after deglitch
Shutdown	Remain Low

I²C communication is available as soon as the input voltage reaches above the POR threshold of 1.7V (TYP).

Output Voltage Control and ADDR

The device output voltage can be programmed between 1.8V to 5.5V with a resolution of 50mV via 0x04 register.

In addition, the SGM62125 implements an ADDR pin to select the I²C communication slave address. Logic low on ADDR, slave address is configured to 0x75, and default output voltage is 3.0V for SGM62125A, 2.5V for SGM62125B, 2.4V for SGM62125C, 2.6V for SGM62125D. Logic high on ADDR, slave address is configured to 0x76, and default output voltage is 3.4V. Floating on ADDR, slave address is configured to 0x77, and default output voltage is 3.6V. Configuring the ADDR pin's logic is only valid during the initial startup, changing the ADDR logic after power good will not change the slave address as well as output voltage.

Ramp PWM Operation (RPWM)

Ramp PWM mode is configured via the RPWM bit and programs the device to operate in FPWM mode when the output ramps from one voltage to another. In light load condition and PFM mode is configured, when ramping from a higher voltage to a lower voltage, load cannot sink enough current to discharge the output capacitors. It is recommended to enable RPWM bit to control the output voltage ramp down in a controlled manner.

Set the RPWM bit in the control register to enable RPWM operation.

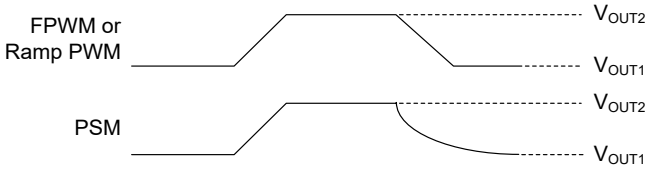


Figure 8. RPWM Operation

Ultrasonic Mode

The SGM62125 implements light load ultrasonic mode (USM) operation by clamping the light load switching frequency always higher than 30kHz even there is no load. USM effectively avoids acoustic noise issue during operation. USM can be enabled via CONTROL register's bit [4].

DETAILED DESCRIPTION (continued)

Dynamic Voltage Scaling (DVS)

Dynamic voltage scaling (DVS) allows changing of the output voltage with a controlled rate. Figure 9 explains the DVS function. The ramp control block changes the output voltage towards the target value in 50mV steps. The 2-bit SLEW[1:0] parameter in the control register is used to choose one of the four slew rate values of 1V/ms, 2.5V/ms, 5V/ms and 10V/ms.

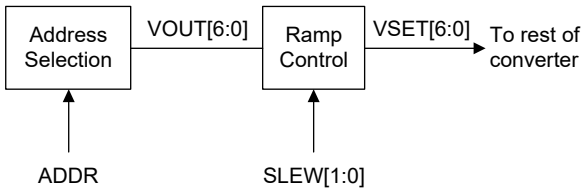


Figure 9. Block Diagram of the Dynamic Voltage Scaling

A DVS ramp is started when the host writes a new value in the active VOUT register. Note that if these changes occur during the startup (before the end of the soft-start and achieving the first power-good), the new value will take effect immediately, and the VOUT will change to the final value without gradual ramp. Besides, if these changes occur after the startup, when a new value is written before the previous DVS completes, the new value will take effect immediately, and the VOUT will continue DVS to the final value.

DVS timing initiated by an I²C write to change the output voltage in the active VOUT register.

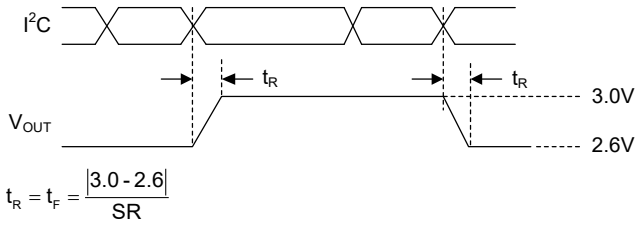


Figure 10. DVS Timing Initiated by a Write to the VOUT Register by I²C

Input Voltage Protection (IVP)

When the output ramps down to a lower voltage by DVS, the current can flow from the device output back to the input, especially in light load condition. While the load does not sink enough current to discharge the output capacitors, the only path for the current released by the output capacitors is flowing back to the input. This behavior can charge the input capacitor's voltage and cause the V_{IN} to rise in an uncontrolled manner. When operating in FPWM and Buck mode, the reverse current flow caused by rapid V_{OUT} transition to a lower range will cause the converter to act as a Boost circuit from output to input until triggering input over-voltage protection.

The SGM62125 provides IVP feature to ensure the voltage present on VIN pin never exceeds 5.8V during any condition. Switching is immediately terminated when IVP is triggered and resumes automatically when the condition is removed.

Over-Current and Short-Circuit Protection

The device implements peak inductor current limit to protect the device in an overload condition. The peak current limit is programmable to 75% of 7.5A via register 0x06 bit [0]. When the inductor peak current sensed by SGM62125 reaches above 7.5A (TYP) limit, the device stops ramping the inductor current higher. The OC, nPG and UV bits have programmable 0ms or 2ms deglitch time via CONFIG register bit [5]. If 0ms is programmed, when the output voltage drops below 90% of programmed output, OC, nPG and UV bits are toggled to logic 1 immediately, and if the output voltage is below 90% of programmed output for longer than 2ms, the device enters hiccup protection.

When 2ms deglitch is programmed, the over-current condition continues for longer than 2ms, but the output voltage does not drop below 90% of the programmed output, the device will not enter hiccup protection, OC, nPG and UV bits remain unchanged. If the over current condition causes the output voltage to drop below 90% of the programmed output and last longer than 2ms, OC, nPG and UV bits are toggled to logic high, and device enters hiccup protection. All bits in the STATUS register are read clear.

Table 3 summarizes the status signal behavior when a short occurs on SGM62125.

Table 3. Status Bit Behavior During short

Application Case	nPG Behavior
nPG during output short	Toggle to logic high after deglitch
UV during output short	Toggle to logic high after deglitch
OC during output short	Toggle to logic high after deglitch
nPG during short recovery	Host read clear
UV during short recovery	Host read clear
OC during short recovery	Host read clear

DETAILED DESCRIPTION (continued)

When the output of the SGM62125 is shorted to ground, the device enters hiccup protection mode to reduce the power dissipation within the device. During hiccup protection, the current limit is folded back to programmable 25%, 50% or 75% of the peak current limit via CONFIG register bits [7:6]. When short-circuit occurs, the output voltage drops below 0.9 × V_{OUT}, the nPG, UV, and OC bits are toggled to logic high after 2ms of deglitch, the device operates up to current limit threshold within the 2ms, then the device enters a hiccup off-time of 20ms. If 0ms is configured, nPG, UV, and OC bits are toggled to logic high immediately when short-circuit occurs, and device enters hiccup protection after 2ms. After the hiccup off time, 200μs soft-start time and hiccup on time of 2ms are issued to attempt to charge the output voltage to the programmed voltage. If the short condition remains, this hiccup on/off pattern repeats itself for continuous 5 seconds, the device turns off, toggling the EN pin or refresh the VIN voltage to restart the device. If the output short condition is removed within 5 seconds, the device automatically ramps the output voltage to the programmed output. If the output voltage is able to reach above 0.95 × V_{OUT} when the soft-start time completes, the nPG, UV and OC bits are toggled to logic low with a host read clear. Please refer to Figure 11 below.

Thermal Shutdown

If the junction temperature exceeds the +150 ℃ threshold, the converter will turn off (OTP) to protect the device. The device will automatically resume operation when T_J falls below +130℃. Note that the automatic recovery can result in a cyclic turn on and turn off if a permanent overload condition causes the OTP. Because after each shutdown, the device cools down and restarts operating. The I²C interface is functional even when the device is shut down due to OTP. If an over-temperature is detected, the TSD bit in the status register will be set to 1. This bit will be cleared if it is read by I²C when T_J is less than +130℃.

Over-Voltage Protection

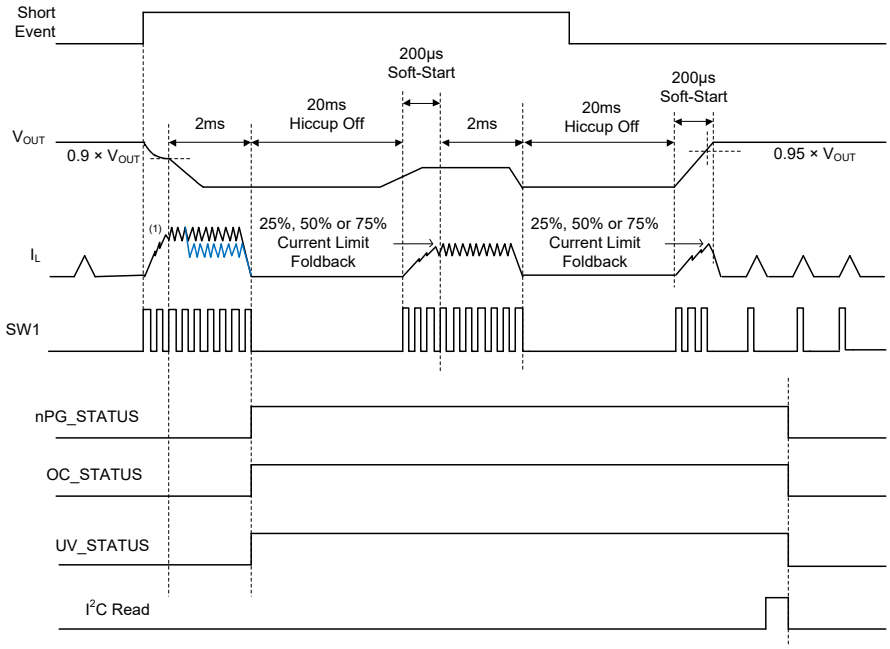
The device implements over-voltage protection feature. If the output voltage exceeds 5.8V (TYP), the device stops switching immediately. When the output voltage falls below 5.6V (TYP), the device resumes switching.

Load Disconnect in Shutdown

When the device is shut down, the input and output are disconnected, blocking any current flow between the input and output of the device.

Output Discharge

When a logic low is applied to the EN pin or V_{IN} < V_{UVLO_F}, the VOUT will be pulled to ground actively to discharge the output. This feature is beneficial for systems requiring strict power-down sequence.



NOTE: 1V < V_{OUT} < PG, 7.5A Peak; V_{OUT} < 1V, limit foldback after 30μs.

Figure 11. Short-Circuit Protection

PROGRAMMING

I²C Serial Interface and Programming

I²C is a widely used 2-wire, bi-directional serial communication interface. It is used in the SGM62125 to support I²C communication for parameter programming, receiving and reporting device status. The use of I²C significantly improves the design flexibility because most of the device functions can be programmed and adapted to the application requirements.

The I²C bus uses two open-drain lines called serial data (SDA) and serial clock (SCL) for communication. The SDA and SCL pins must be pulled up to the bus high voltage by a current source or pull-up resistors. All devices connected to the bus have their own addresses (7-bit) and each may act as a master or slave during a data transfer. The master is usually a processor or another host device that initiates a data transfer and generates the clock signals to allow transmission of the data bit. Any device that is addressed in a transfer sequence is considered as a slave. For more details about I²C refer to the “UM10204: I²C-bus specification and user manual, revision 6”.

The SGM62125 is slave device with 75h ((ADDR = low), 76h (ADDR = high) or 77h (ADDR = floating) address and only support 7-bit addressing and not 10-bit address or the general call address. The device supports standard mode (100kbps), fast mode (400kbps) and fast mode plus (1Mbps) data transfer speeds. Each device has five 8-bit registers with individual internal addresses that can be read or written (except the read-only bits) by a host. See the Register Map section for details. The register contents remain intact if V_{IN} remains higher than 2.1V. The data transfer protocol for the standard and fast speed modes are the same.

START and STOP Conditions (For All Modes)

In the idle state condition, both SDA and SCL line are high. A transaction is initiated by a master who takes the control of the bus when it is free (idle) by sending a START or S condition to initiate the exchange of data as shown in Figure 12. When the data transfer job is done, the master sends one (or more) STOP or P conditions to terminate the transaction and releases the bus. To ensure that the bus is properly reset after bus power up, it is recommended to initiate the bus by sending a STOP condition after power up.

A START condition is generated by pulling SDA from high to low when SCL is high. START is detected by all devices on the bus. Similarly, a STOP is applied on the bus by pulling SDA from low to high when SCL is high. The START and STOP conditions are always generated by a master. After a START and before a STOP the bus is considered busy. The master may not release the bus after a complete transaction with the slave and send a repeated START to initiate a new data exchange with the slave.

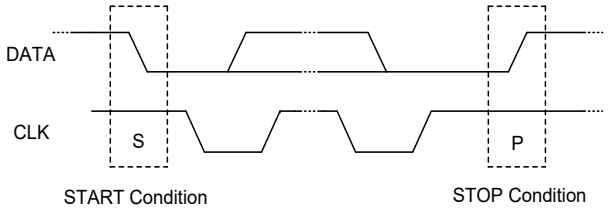


Figure 12. START and STOP Conditions

Data Bit Transmission and Validity

During a transaction all data bit (high or low) must remain stable on the SDA line during SCL = H period. The state of the SDA can only change when the clock (SCL) is low. For each data bit transmission, one clock pulse is generated by the master. Bit transferring procedure is shown in Figure 13.

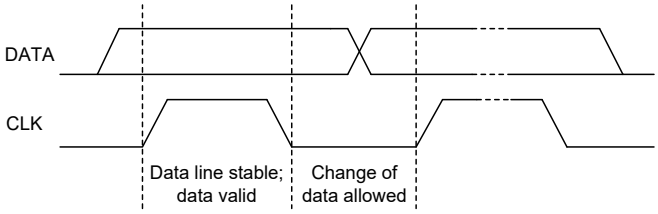


Figure 13. Bit Transfer on the Serial Interface

Bus Clear

If the I²C slave data line (slave SDA) is stuck low, the controller should send nine clock pulses. The device that held the bus low should release it sometime within those nine clocks.

PROGRAMMING (continued)

I²C Data Format

The data is transmitted one byte at a time. After detecting the START condition, the transmitter will send one byte (8-bit) of data, bit by bit, starting from the most significant bit (MSB), with each SCL pulse placing a new bit on the SDA line. After sending the 8th bit, the transmitter releases the SDA line during the 9th SCL pulse in order to receive an acknowledgement bit from the receiver. Therefore, a total of 9 bits is exchanged for each byte. The number of bytes in one transaction is not limited. After sending the ACK bit, if the receiver is busy and cannot transfer another byte of data, it can hold the SCL line low and keep the sender in wait state (clock stretching). When it is ready for another byte of data, it releases the clock line and the data transfer can continue with clocks generated by the master.

The 9th bit is the receiver response (slave or master) to show that the byte is received. Sending a low signal during the 9th clock cycle is interpreted as ACK. If the receiver responds a high or does not respond at all, the sender will receive a high for the 9th bit that is considered as not ACK, called NCK. An NCK means that the receiver does not expect more data. Therefore, the response of the receiver to the last byte in a transaction is an NCK. It also shows that there is a problem in the communication link (rare). After the 9th bit, a STOP or a repeated START should be sent by master. Figure 14 and Figure 15 show the byte transfer and acknowledgment procedures of the I²C interface.

I²C Data Communication Protocol

After power up, it is recommended to send a STOP condition by the host to assure all I²C slaves are reset and ready. All connected I²C devices recognize the STOP condition and know when the bus is idle to monitor the bus for START condition followed by an address. To communicate with a specific device, after the host or master sends a START condition, it generates the SCL (clock) pulses and transmits the 7-bit address of the destination device along with an 8th (R/W) data-direction bit as one byte. All devices compare the address to their own fixed address. The SDA line is released after the 8th bit for the target receiver to reply with an ACK (by pulling the SDA line low during the high period of the 9th clock). By receiving the ACK, the master realizes that the slave is ready and the link is OK.

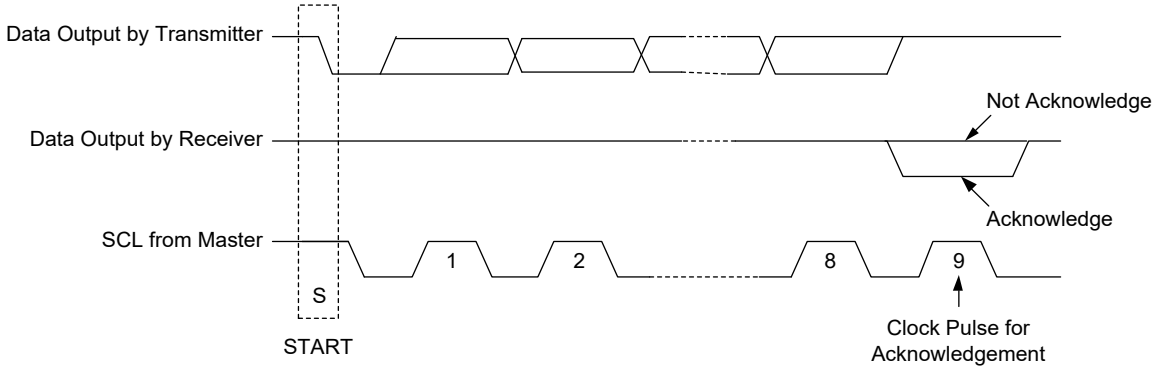


Figure 14. Acknowledgement on the I²C Bus

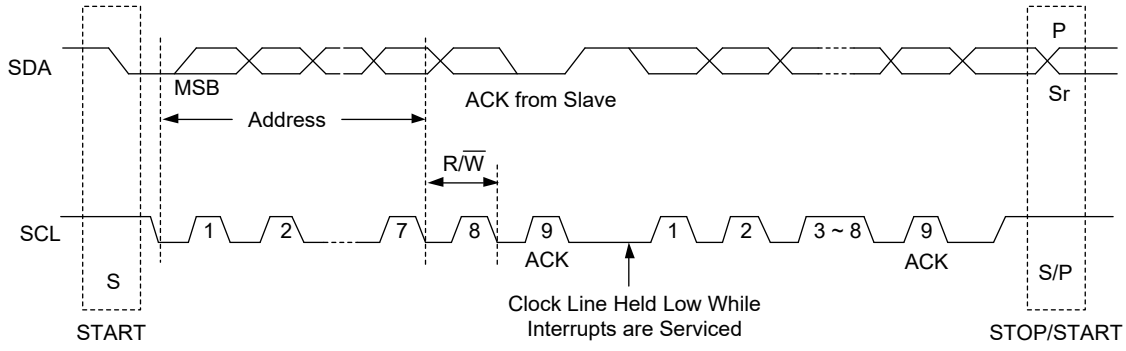


Figure 15. I²C Data Communication Protocol

PROGRAMMING (continued)

Register Read and Write

After sending a START condition, the master sends the slave address (7 bits) with an 8th data-direction bit (R/$\overline{W}$) to inform the slave if the following byte of data is supposed to be a received by slave (WRITE) or the slave should send a byte of data back to master (READ). After receiving the ACK from the addressed slave, the master continues to send more clock pulses for future read or write. Usually, the second byte is also a WRITE containing the register address that the master wants to access in the slave.

WRITE: If the sequence is a single write and the master wants to write in the addressed register in the slave, the third byte will be the content of the addressed register as shown in Figure 16 for a single write data transfer. Ignoring the slaves reply (ACK or NCK), the master issues a STOP and the transaction is ended.

READ: If the sequence is a single read and the master wants to read the content of the addressed register in the slave, the master first sends a new START (repeated START) before the third byte because the direction of read/write needs to be changed from write to read. Therefore, the third byte is still the slave address (7 bits) and an 8th data-direction bit will be R/$\overline{W}$ = 1. The slave will send an ACK bit followed by the content of the register as the fourth byte. Master may reply with an ACK or NCK and then issues a STOP condition. The format of a single read from a device register is shown in the Figure 17. Reading data from a register address that is not listed will be FFh.

The device register contents are updated on the falling edge of the acknowledge signal after the last byte.

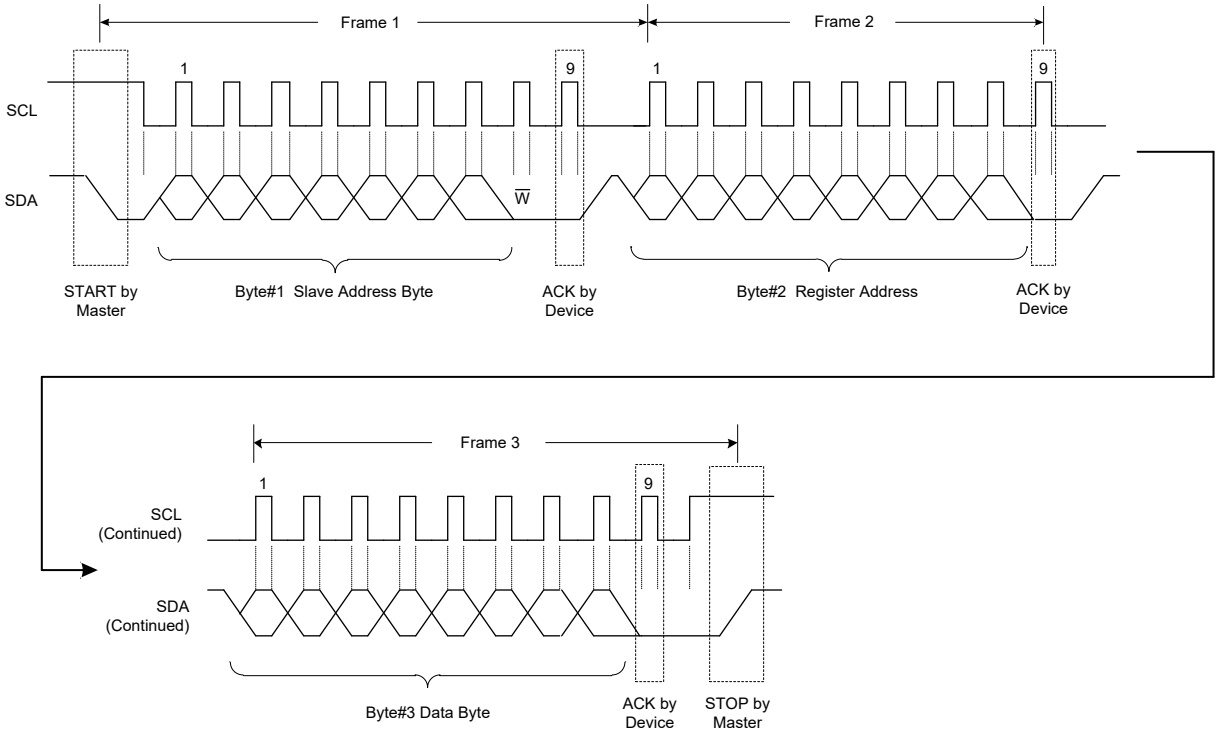


Figure 16. The Format of a WRITE into a Device Register in the Standard Mode, Fast Mode and Fast Mode Plus

PROGRAMMING (continued)

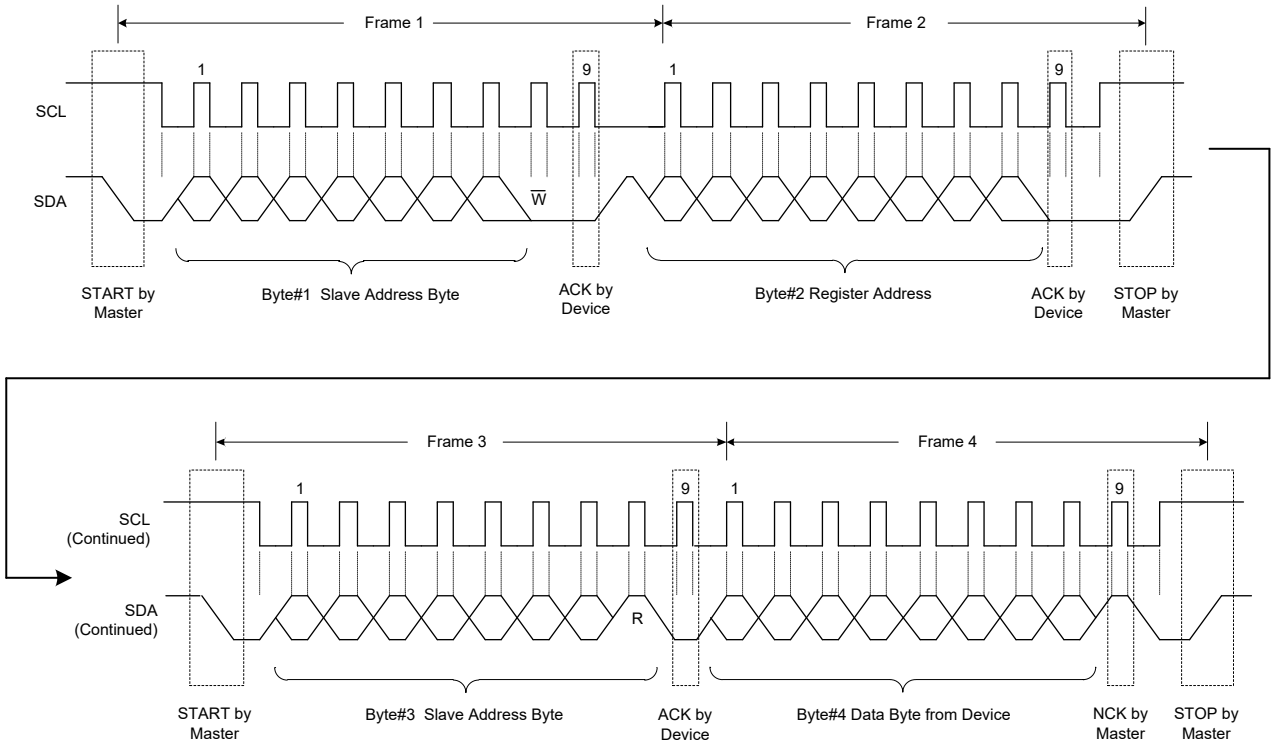


Figure 17. The Format of a READ from a Device Register in the Standard Mode, Fast Mode and Fast Mode Plus

REGISTER MAPS

Table 4 lists the map of the SGM62125 register. Any register address not listed in Table 4 should be considered as a reserved location and no write should be tried to modify them (they may be used in future revisions). Input POR or pulling EN pin low will reset the register to default.

Table 4. Device Registers

ADDRESS	ACRONYM	REGISTER NAME
01h	CONTROL	Control Register
02h	STATUS	Status Register
03h	DEVID	Device Identity Register
04h	VOUT (ADDR = L)	VOUT (ADDR = L) Register
	VOUT (ADDR = H)	VOUT (ADDR = H) Register
	VOUT (ADDR = Floating)	VOUT (ADDR = Floating) Register
05h	RESERVED	RESERVED
06h	CONFIG	CONFIG Register

R/W: Read/Write bit(s)
R: Read only bit(s)
RC: Bit(s) cleared to default by being read
PORV: Power-On Reset Value

01h: Control Register [reset value = 00h]

The Control register is a volatile register. The contents are lost when the input voltage drops below the POR threshold or a logic low is applied on EN pin. Control register is a read/write register which programs the operation mode of the device. Write to the reserved bit is not allowed.

BITS	BIT NAME	TYPE	PORV	DESCRIPTION	RESET BY
D[7]	RESERVED	R	0	Reserved.	—
D[6:5]	I²C_SDA_SLEW	R/W	00	SDA Pin Output Pull-Down Slew Rate. 00 = High (default) 01 = Medium 10 = Low 11 = Very Low	POR or EN pin = L
D[4]	Ultrasonic Mode	R/W	0	Light Load Ultrasonic Mode. 0 = Ultrasonic mode disabled (default) 1 = Ultrasonic mode enabled	
D[3]	FPWM	R/W	0	Set Forced PWM Operation. 0 = Disable (default) 1 = Enable	
D[2]	RPWM	R/W	0	Set Ramp PWM Operation. 0 = Disable (default) 1 = Enable	
D[1:0]	DVS_SLEW[1:0]	R/W	00	Set the Slew Rate. Set the slew rate of the output voltage change to a new value. 00 = 1V/ms (default) 01 = 2.5V/ms 10 = 5V/ms 11 = 10V/ms	

REGISTER MAPS (continued)

02h: Status Register [reset value = 00h]

A read operation clears all bits of this register (unless a status is still valid during the read and sets the bit again). It is a volatile register and loses its contents if the V_{IN} falls below POR threshold or the device is disabled by applying a low to the EN pin.

BITS	BIT NAME	TYPE	PORV	DESCRIPTION	RESET BY
D[7:5]	RESERVED	R	000	Reserved.	—
D[4]	HD	RC	0	The Status of the Hot-die Function. 0 = Normal operation (default) 1 = A hot-die event was detected	POR or EN pin = L or a read event
D[3]	UV	RC	0	The Status of the Output Under-voltage Function. 0 = Normal operation (default) 1 = An under-voltage event was detected	
D[2]	OC	RC	0	The Status of the Over-Current Function. 0 = Normal operation (default) 1 = An over-current event was detected	
D[1]	TSD	RC	0	Thermal Shutdown. It is cleared if this register is read and if the over-temperature condition no longer exists. 0 = Temperature good (default) 1 = An OTP event occurred	
D[0]	nPG	RC	0	Output Power-Good. PG is cleared with a read if the power-not-good condition no longer exists. 0 = Power-good (default) 1 = A power-not-good event was detected	

03h: Device Identity Register (reset value = 40h)

This is a read only register that holds the die revision of the device.

BITS	BIT NAME	TYPE	PORV	DESCRIPTION	RESET BY
D[7:4]	DEVICE[3:0]	R	0100	Device manufacturer. 0100 = SGM (default)	—
D[3:2]	MAJOR[1:0]	R	xx	Major Die Revision. 00 = A, initial silicon 01 = B, first major revision 10 = C, second major revision 11 = D, third major revision	
D[1:0]	MINOR[1:0]	R	xx	Minor Die Revision. 00 = 0, initial silicon 01 = 1, first minor revision 10 = 2, second minor revision 11 = 3, third minor revision	

REGISTER MAPS (continued)

04h: VOUT (ADDR = L) Register (reset value = 18h)

VOUT (ADDR = L) register determines the device output voltage if the ADDR pin is logic low. It is a volatile register and loses its contents if the V_{IN} voltage falls below POR threshold or the device is disabled by applying a low to the EN pin.

BITS	BIT NAME	TYPE	PORV	DESCRIPTION	RESET BY
D[7]	FSW	R/W	0	Switching Frequency Program. 0 = 2.2MHz (default) 1 = 3.5MHz	POR or EN pin = L
D[6:0]	VOUT[6:0]	R/W	0011000	Set VOUT Output Voltage when ADDR = L. 0000000 = 1.8V 0000001 = 1.85V 0000010 = 1.9V … 0001100 = 2.4V (default) for SGM62125C 0001101 = 2.45V 0001110 = 2.5V (default) for SGM62125B 0001111 = 2.55V 001000 = 2.6V (default) for SGM62125D … 0011000 = 3.0V (default) for SGM62125A … 1000010 = 5.1V 1000011 = 5.15V 1000100 = 5.2V … 1001010 ~ 1111111 = 5.5V	

04h: VOUT (ADDR = H) Register (reset value = 20h)

VOUT (ADDR = H) register determines the device output voltage if the ADDR pin is logic high. It is a volatile register and loses its contents if the V_{IN} voltage falls below POR threshold or the device is disabled by applying a low to the EN pin.

BITS	BIT NAME	TYPE	PORV	DESCRIPTION	RESET BY
D[7]	FSW	R/W	0	Switching Frequency Program. 0 = 2.2MHz (default) 1 = 3.5MHz	POR or EN pin = L
D[6:0]	VOUT[6:0]	R/W	0100000	Set VOUT Output Voltage when ADDR = H. 0000000 = 1.8V 0000001 = 1.85V 0000010 = 1.9V … 0100000 = 3.4V (default) … 1000010 = 5.1V 1000011 = 5.15V 1000100 = 5.2V … 1001010 ~ 1111111 = 5.5V	

REGISTER MAPS (continued)

04h: VOUT (ADDR = Floating) Register (reset value = 24h)

VOUT (ADDR = Floating) register determines the device output voltage if the ADDR pin is floating. It is a volatile register and loses its contents if the V_{IN} voltage falls below POR threshold or the device is disabled by applying a low to the EN pin.

BITS	BIT NAME	TYPE	PORV	DESCRIPTION	RESET BY
D[7]	FSW	R/W	0	Switching Frequency Program. 0 = 2.2MHz (default) 1 = 3.5MHz	POR or EN pin = L
D[6:0]	VOUT[6:0]	R/W	0100100	Set VOUT Output Voltage when ADDR = H. 0000000 = 1.8V 0000001 = 1.85V 0000010 = 1.9V … 0100100 = 3.6V (default) … 1000010 = 5.1V 1000011 = 5.15V 1000100 = 5.2V … 1001010 ~ 1111111 = 5.5V	

05h: RESERVED

BITS	BIT NAME	TYPE	PORV	DESCRIPTION	RESET BY
D[7:0]	RESERVED	R/W	00000000	Reserved.	—

06h: CONFIG Register (reset value = 41h)

The CONFIG register is a volatile register. The contents are lost when the input voltage drops below the POR threshold or a logic low is applied on EN pin. CONFIG register is a read/write register which programs the operation mode of the device. Write to the reserved bit is not allowed.

BITS	BIT NAME	TYPE	PORV	DESCRIPTION	RESET BY
D[7:6]	CL_FOLDBACK	R/W	01	Soft Start Current Limit Foldback Threshold. 00 = 25% of current limit 01 = 50% of current limit (default) 10 = 75% of current limit 11 = 100% of current limit	POR or EN pin = L
D[5]	PROTECTION_DEGLITCH	R/W	0	Protection Deglitch Time. 0 = 2ms (default) 1 = 0ms	
D[4]	INDUCTOR	R/W	0	Inductor Select. 0 = 470nH (default) 1 = 330nH	
D[3]	FREQ_FOLDBACK	R/W	0	Frequency Foldback Threshold. 0 = low (default) 1 = high	
D[2]	GM	R/W	0	Error Amplifier GM. 0 = low (default) 1 = high	
D[1]	COMP_RES	R/W	0	Compensation Resistor. 0 = high (default) 1 = low	
D[0]	PK_CL	R/W	1	Peak Current Limit. 0 = 75% of current limit 1 = 100% of current limit (default)	

APPLICATION INFORMATION

The SGM62125 is a perfect choice for applications that demand for a power supply with high efficiency over a wide load range and their input voltage can vary from below, near and above the desired output voltage. The peak current in the internal switch of the device is typically limited to a maximum of around 6A. Input and output voltage ranges are 2.2V to 5.5V and 1.8V to 5.5V respectively.

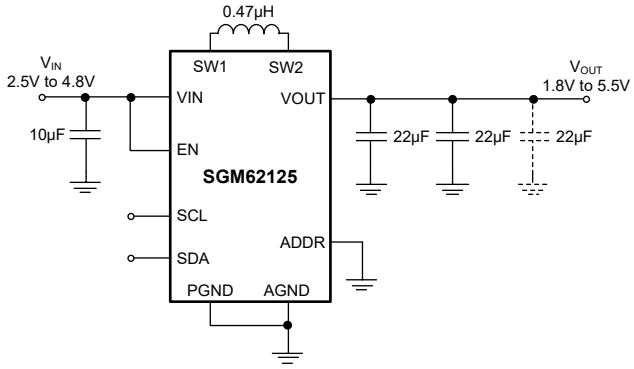


Figure 18. Application Example of 2A Power Supply with 1.8V to 5.5V Output

Design Requirements

This example of the design parameters is shown in Table 5.

Table 5. Design Parameters

Parameter	Symbol	Recommended Value
Input Voltage	V_{IN}	2.5V to 4.8V
Output Voltage	V_{OUT}	1.8V to 5.5V
Output Current	I_{OUT}	2A
I²C Bus Capacitance	C_B	100pF
I²C Bus Voltage	V_{BUS}	3.3V
I²C Bus Speed		Fast mode (400kHz)

Design Procedure

Input Capacitor

The total input capacitance after considering the DC bias de-rating is recommended to be above 5μF. It is recommended to use a 10μF, 6.3V ceramic capacitor in most applications. If the source is far away from the device, it is recommended to use additional bulk capacitance (such as a 47μF electrolytic or tantalum capacitor) for better stability.

Inductor

A 0.47μH inductor is recommended for use with 2.2MHz switching frequency option, and 0.22μH is recommended for 3.5MHz option. Lower DCR inductors are recommended for better efficiency. The rated saturation current (I_{SAT}) must be at least 20% above the maximum peak current in the worst cases including transients. Usually the worst cases occur in the Boost mode when operating at the lowest input voltage, highest output voltage and with the maximum load. Use Equation 1 to calculate the maximum duty cycle in Boost mode (corresponds to the maximum inductor current).

$$D_{MAX} = \frac{V_{OUT\_MAX} - V_{IN\_MIN}}{V_{OUT\_MAX}} \quad (1)$$

where:

D_{MAX} is the maximum duty cycle in Boost mode.

V_{IN_MIN} is the minimum input voltage.

V_{OUT_MAX} is the maximum output voltage.

In this application:

$$D_{MAX} = \frac{5.5V - 2.5V}{5.5V} \times 100\% = 55\%$$

The maximum inductor current can be calculated by:

$$I_{LM} = \frac{I_{OUT\_MAX}}{\eta(1 - D_{MAX})} + \frac{D_{MAX} \times V_{IN\_MIN}}{2 \times f_{SW} \times L} \quad (2)$$

where:

I_{LM} is the peak inductor current.

I_{OUT_MAX} is the maximum output current.

η is the converter efficiency (use application curves or choose 90%).

f_{SW} is the switching frequency (2.2MHz).

L is the inductance (0.47μH).

$$I_{LM} = \frac{2A}{0.9 \times (1 - 0.55)} + \frac{0.55 \times 2.5V}{2 \times 2.2MHz \times 0.47\mu H} = 5.6A$$

Choose the I_{SAT} value at least 20% higher than the calculated I_{LM} value. In this example, $I_{LM} \approx 5.6A$ and the selected inductor saturation current is 6.7A.

For output voltage higher than 4.2V applications, if 3.5MHz option is selected, a 0.24μH inductor is recommended.

APPLICATION INFORMATION (continued)

Output Capacitor

It is recommended to have at least 16μF effective output capacitance (after de-rating) for the SGM62125. Using two 22μF, 6.3V ceramic capacitors for output voltage < 3.6V application, using three 22μF, 6.3V ceramic capacitors or two 47μF, 6.3V ceramic capacitors is recommended for > 3.6V output application. To reduce high frequency noise, a 100nF ceramic capacitor in 0201 or 0402 package is recommended to place as close to the VOUT and GND pins as possible in parallel to the other output capacitors.

There is no upper limit for the SGM62125 output capacitance. However, using large output capacitance results in slower response to the transients and can cause other issues when the output is discharged.

Loop Response

The SGM62125 offers the flexibility to optimize the loop response for applications requiring fast load transient requirement via CONFIG register. Bit [2] programs the error amplifier's transconductance, and bit [1] programs the compensation resistance. Configuring bit [2] to 1 offers a faster loop response. Configure bit [1] to 1 for higher loop stability. Be noted, faster loop response comes with the trade-off of stability issue at low V_{IN}, adding more output capacitors helps to stabilize the loop.

In addition, if application wants to achieve faster loop response but still wants to use 2.2MHz switching without sacrificing efficiency, 330nH inductor can be used with 2.2MHz combination via bit [4].

I²C Pull-up Resistors

The standard I²C specifications and user manual can be used to set up the I²C bus. The maximum pull-up resistor value for the required bus speed can be calculated from Equation 3:

$$R_{P\_MAX} = \frac{t_R}{0.8473 \times C_B} \quad (3)$$

where:

t_R = The maximum allowed rise time (300ns for fast mode).

C_B = Total capacitive load on each bus line.

$$R_{P\_MAX} = \frac{300ns}{0.8473 \times 100pF} = 3.541k\Omega$$

If the bus capacitance is not known for the application, measure the rise time with an oscilloscope starting with a 1kΩ pull-up and then calculate the C_B from Equation 3 to find the maximum allowed pull-up resistor.

To find the minimum permitted pull-up resistor value for a specific bus speed, use Equation 4.

$$R_{P\_MIN} = \frac{V_{BUS} - V_{OL}}{I_{OL}} \quad (4)$$

where:

V_{BUS} is the I²C bus pull-up voltage.

V_{OL} is the low-level output voltage (0.4V).

I_{OL} is the low-level output current (3mA for the fast mode).

$$R_{P\_MIN} = \frac{3.3V - 0.4V}{3mA} = 967\Omega \quad (5)$$

The pull-up resistor of R_P = 3.3kΩ meets both requirements.

Application Example

Table 6 lists the component values and part numbers used for the tests and measurements outlined in the characteristic curves.

Table 6. Components used for Characteristic Curves

Reference	Description	Part Number	Manufacturer
C_1	Capacitor, 10μF, 6.3V, 0603, ceramic	GRM188R60J106KE47D	Murata
C_2, C_3	Capacitor, 22μF, 6.3V, 0603, ceramic	GRM188R60J226MEA0D	Murata
L_1	Inductor, 0.47μH (for 2.2MHz)	744383560047HT	Wurth
	Inductor, 0.22μH (for 3.5MHz)	XGL4018-221MEC	Coilcraft
U_1	Integrated circuit	SGM62125	SGMICRO

LAYOUT

Layout Guidelines

Layout plays a significant role for all switch modes in DC/DC power supplies. Improper layout could result in poor EMI performance, device unstable, and potential device damage. The input capacitor, output capacitor and the inductor should be placed as close as possible to the IC. Ensure that the power trace through VIN, the input capacitor and GND, as well as through VOUT, the output capacitor and GND is minimized. The SGM62125 implements power ground and control ground pins to minimize the ground noise effect on sensitive analog circuits. Connect the analog ground trace to the main power ground at a single point.

Figure 19 is an example layout which is also the PCB layout used to collect the data in the Application Example section.

Layout Example

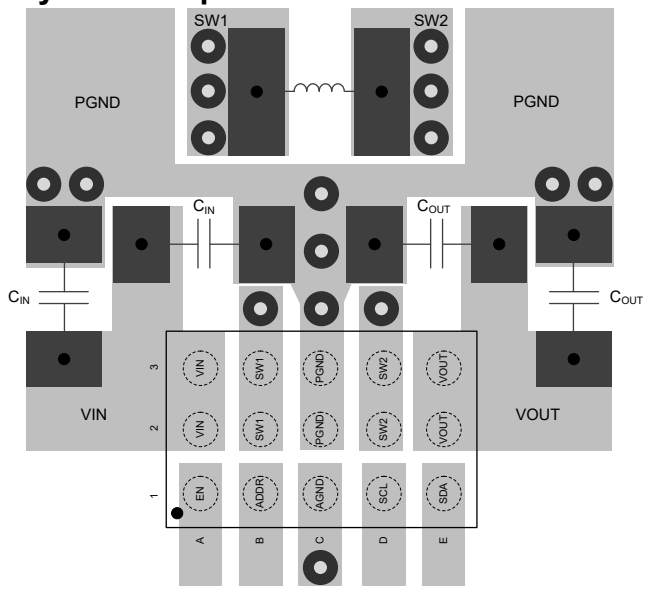


Figure 19. Recommended PCB Layout

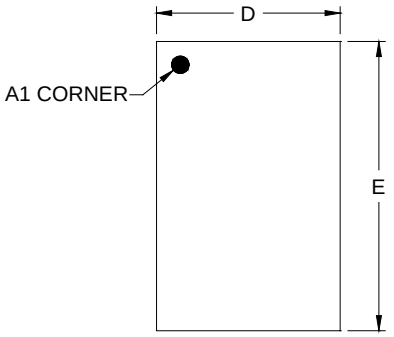
REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

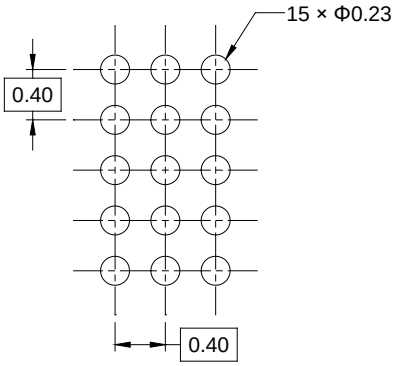
Changes from Original to REV.A (AUGUST 2026)	Page
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

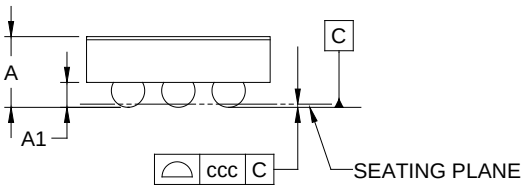
WLCSP-1.46×2.3-15B



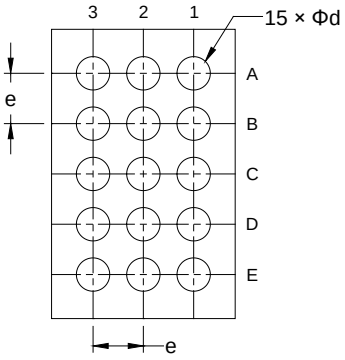
TOP VIEW



RECOMMENDED LAND PATTERN (Unit: mm)



SIDE VIEW



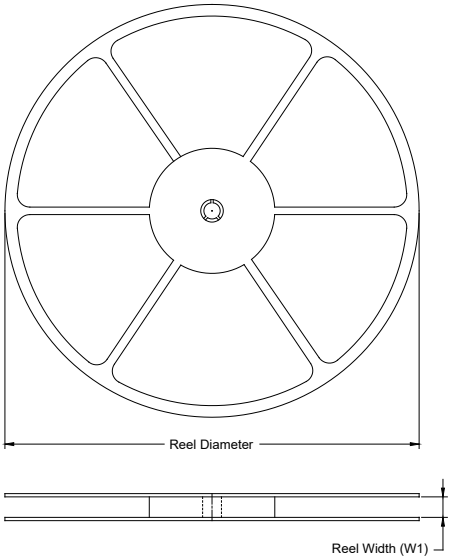
BOTTOM VIEW

Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	-	-	0.600
A1	0.178	-	0.218
D	1.423	-	1.483
E	2.267	-	2.327
d	0.235	-	0.295
e	0.400 BSC		
ccc	0.050		

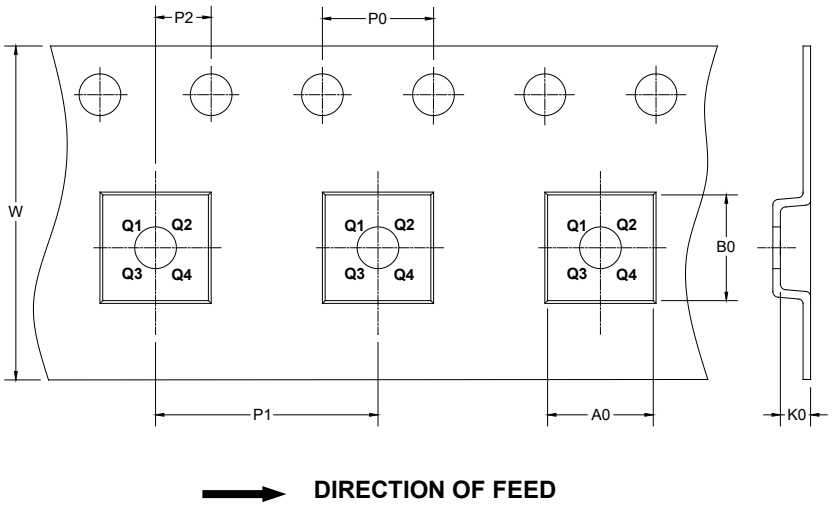
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



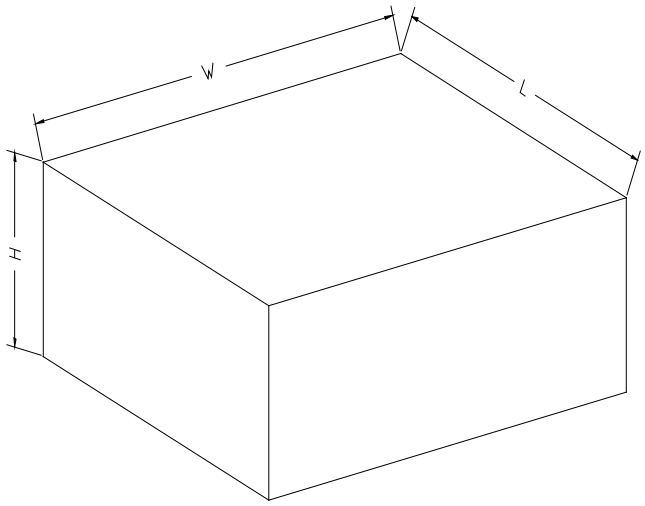
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
WLCSP-1.46×2.3-15B	7"	9.5	1.58	2.42	0.73	4.0	4.0	2.0	8.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18

DD0002