VCE4715
High-Performance AMR Angle Sensor

GENERAL DESCRIPTION

The VCE4715 is an AMR angle sensor with an integrated ADC-driving operational amplifier.

The sensor incorporates two Wheatstone bridges arranged at a 45° angle to each other. When a magnetic field rotates parallel to the x-y plane, it detects changes in the magnetic field angle and outputs sine and cosine (sin/cos) signals. The frequency of these signals is twice the angle between the sensor and the magnetic field direction. Its built-in fixed-gain instrumentation amplifier ensures that the output signal amplitude is proportional to the supply voltage, providing stable and clean signals that can be directly used by an ADC for angle signal acquisition.

The VCE4715 is available in a Green SOIC-8 package.

FEATURES

- **180° Sensing Angle Range**
- **Low Thermal and Lifetime Drift**
- **Analog Sine and Cosine Outputs Proportional to the Supply Voltage**
- **V_{DD} from 3V to 5.5V**
- **Minimal Phase Delay**
- **Temperature Range: -40℃ to +125℃**
- **Available in a Green SOIC-8 Package**

APPLICATIONS

Actuator Control and Positioning
Absolute Position Measurement (Linear and Angle)
Brushless DC Motor Control and Positioning
Contactless Angular Measurement
Magnetic Angular Position Sensing

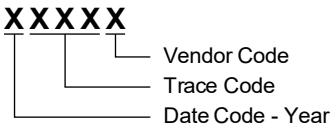
PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
VCE4715	SOIC-8	-40℃ to +125℃	VCE4715XS8G/TR	4715XS8 XXXXX	Tape and Reel, 4000

Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DD} ..... -0.3V to +6V
Package Thermal Resistance
SOIC-8, θ_{JA} ..... 108.6℃/W
SOIC-8, θ_{JB} ..... 55.9℃/W
SOIC-8, θ_{JC} ..... 51.2℃/W
Junction Temperature .....+150℃
Storage Temperature Range.....-50℃ to +150℃
Lead Temperature (Soldering, 10s) .....+260℃
ESD Susceptibility (1) (2)
HBM.....±4000V
CDM .....±1000V

NOTES:

1. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.

2. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

RECOMMENDED OPERATING CONDITIONS

Supply Voltage, V_{DD} .....3V to 5.5V
Operating Ambient Temperature Range..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

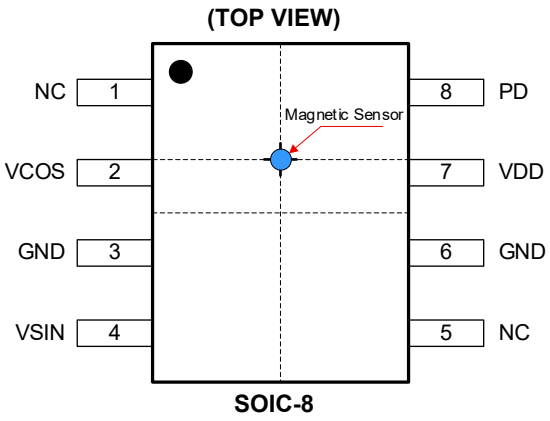
ESD SENSITIVITY CAUTION

This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION



PIN DESCRIPTION

PIN	NAME	TYPE	FUNCTION
1, 5	NC	—	Internal Pull-Down.
2	VCOS	O	Analog Cosine Output.
3	GND	G	Ground.
4	VSIN	O	Analog Sine Output.
6	GND	G	Ground.
7	V_{DD}	P	Supply Pin.
8	PD	I	Power-Down Pin, Active High.

NOTE:

1. I = input, O = output, G = ground, P = power.

ELECTRICAL CHARACTERISTICS

(V_{DD} = 3V to 5.5V, T_A = -40℃ to +125℃, C_L = 10nF to GND, R_L = 200kΩ to GND angle inaccuracies referred to homogenous magnetic field at 25kA/m; output signals and offset voltages are related to the common-mode level of V_{DD}/2, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply						
Supply Voltage	V_{DD}		3		5.5	V
Quiescent Supply Current	I_{SY}	PD = GND, no load	3.5	6.0	7.8	mA
		PD = V_{DD}, no load		8.0	12.5	μA
Power-Up Time	t_{PWRUP}	To 98% of desired output level after V_{DD} was reached			80	μs
		To 98% of desired output level after PD was released			40	μs
Digital Inputs						
Input Bias Current (PD)	I_{B_PD}	For PD pin, PD = GND		0.1	1	μA
		For PD pin, PD = V_{DD}		16	26	μA
Input Voltage (PD)						
High	V_{IH}		1.4			V
Low	V_{IL}				0.35	V
Hysteresis	V_{HYS}			0.6		V
Load Capacitor						
External Load Capacitance (1)	C_L	Between VSIN to GND and VCOS to GND, solder close to package	1			nF
Angular Performance						
Angle Measurement Range			0		180	Degrees
Uncorrected Angular Error (2)	A_{UNCORR}	T_A = -40℃	-3	±0.4	3	Degrees
		T_A = +25℃	-3	±0.3	3	Degrees
		T_A = +125℃	-4	±0.5	4	Degrees
Single Point Calibration Angular Error (3) (4)	A_{CAL}	T_A = -40℃ to +125℃		±0.3		Degrees
Dynamic Angular Error (4) (5)	$A_{DYNAMIC}$	T_A = -40℃ to +125℃, rotation frequency = 2000rpm		±0.25		Degrees
Angular Inaccuracy (6)	ΔA	After end of line (EOL) calibration for offset voltage error and amplitude synchronism at T_A = -40℃ to +125℃ (only 180° range)		0.07		Degrees
Output Parameters						
Amplitude	V_{AMP}	T_A = -40℃	61	71	81	%V_{DD}
		T_A = +25℃	50	57	64	%V_{DD}
		T_A = +125℃	30	39	48	%V_{DD}
Output Voltage Range	$V_{O-SWING}$	VSIN and VCOS, normal operation	8		92	%V_{DD}
Output Voltage Low	V_{OL}	VSIN or VCOS, broken bond wire detected			3.75	%V_{DD}
Output Referred Offset Voltage	V_{OFFSET}				3.75	%V_{DD}
Amplitude Synchronism Error (7)	k		-1.2	±0.25	1.2	%peak
Delay Time	t_{DEL}	Rotation frequency = 30,000rpm, C_L = 10nF		2.6		μs
Phase Error (8)	Φ_{ERR}	Rotation frequency = 30,000rpm, C_L = 10nF		1		Degrees
Orthogonality Error	OE			0.05		Degrees
Output Noise	V_{NOISE}	BW = 80kHz, RTO		200		μVrms
Output Series Resistance	R_O	Normal operation, PD = GND, no load		60		Ω
		PD = V_{DD}, no load	40	62		kΩ
Output -3dB Cutoff Frequency (9)	f_{-3dB}	Amplifier BW		90		kHz
Power Supply Rejection (9)	PSRR	Measured as output variation from V_{DD}/2, V_{DD} = 3V to 5.5V, R_L = 200kΩ to GND		80		dB

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 3V to 5.5V, T_A = -40℃ to +125℃, C_L = 10nF to GND, R_L = 200kΩ to GND angle inaccuracies referred to homogenous magnetic field at 25kA/m; output signals and offset voltages are related to the common-mode level of V_{DD}/2, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Short-Circuit Current	I_{SC}	Short to GND per pin (VSIN, VCOS)	7.5	17		mA
		Short to V_{DD} per pin (VSIN, VCOS)	10	19		mA
Sensitivity	SEN	A = 0° and 135°, T_A = +25℃		49		mV/°

NOTES:

1. A minimum load capacitance of 1nF is required for output buffer stability. A value of 4.7nF to 10nF is recommended: 4.7nF minimizes propagation delay and phase error in high-speed applications, whereas 10nF optimizes wideband noise performance. Larger capacitance values are not recommended, as they prolong power-up settling time, increase dynamic phase lag, and introduce additional angular error from channel-to-channel capacitance mismatch.

2. Total mechanical angular error post-arctan calculation (designated as A_{UNCORR}) encompasses all temperature-dependent error contributors prior to calibration. This specification undergoes 100% production validation at T_A = +25℃. Included among these error constituents are offset deviations, amplitude matching, amplitude matching temperature drift, thermal-induced offset drift, phase mismatch, hysteresis, orthogonality deviation, and electrical noise.

3. Total mechanical angular error post-arctan calculation (denoted as A_{CAL}) encompasses all temperature-dependent error contributors subsequent to a preliminary offset nulling procedure at T_A = +25℃. Included among these error constituents are amplitude synchronism temperature drift, amplifier gain matching discrepancies, thermal-induced offset drift, phase mismatch, hysteresis, orthogonality deviation, and electrical noise.

4. Guaranteed through characterization.

5. Total mechanical angular error post-arctan calculation (designated as $A_{DYNAMIC}$) encompasses all temperature-dependent error contributors following an ongoing background calibration routine. This calibration is implemented to rectify offset deviations and amplitude synchronism discrepancies. Included among these error constituents are phase mismatch, hysteresis, orthogonality deviation, electrical noise, and long-term lifetime drift.

6. Angular speed <300 rpm. Limited to 180° rotation. The value is calculated only with the third and fifth harmonics of the spectrum of output signal amplitude by the ideal homogeneous field.

7. Peak-to-peak amplitude mismatch. $k = 100 \times (1 - V_{SIN}/V_{COS})$.

8. Phase mismatch correlated with rotational frequency is characterized subsequent to precision offset rectification, amplitude calibration, and arctangent computation.

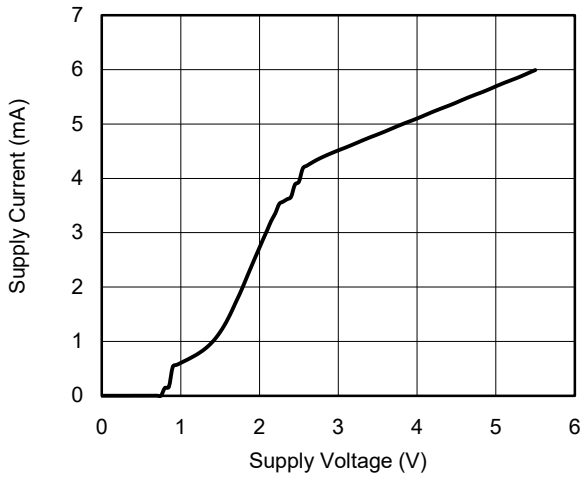
9. Guaranteed by design.

MAGNETIC CHARACTERISTICS

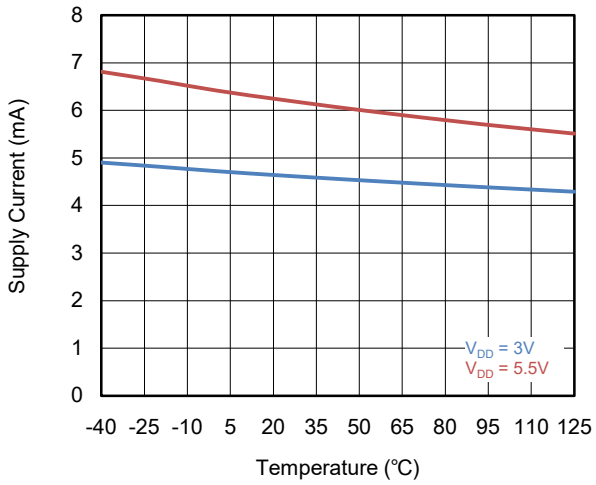
PARAMETER	VALUE	UNIT	TEST CONDITION/COMMMENTS
Magnetic Field Strength, Hext	25	kA/m	A defined magnetic field must be applied within the x-y plane of the sensor. On the top surface of the package, the “x-axis” is perpendicular to the line connecting pin 2 and pin 7, while the “y-axis” is aligned with the direction of the line between pin 2 and pin 7.
Maximum Magnetic Field Rotation Speed	50,000	rpm	
Reference Position Error	±50	μm	The reference positions are x = 0μm at the center of the package top, and y = 0μm along the straight line connecting pin 2 and pin 7.
Reference Angle Error	±2	Degrees	The line connecting pin 2 and pin 7 is parallel to the reference direction at which the angle is defined as angle Φ = 0°.

TYPICAL PERFORMANCE CHARACTERISTICS

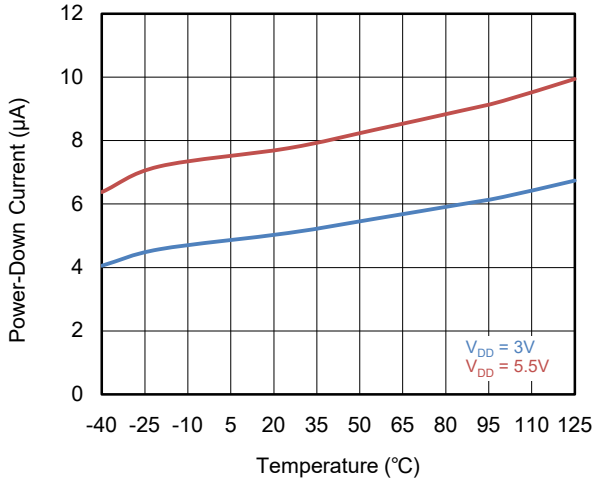
Supply Current vs. Supply Voltage



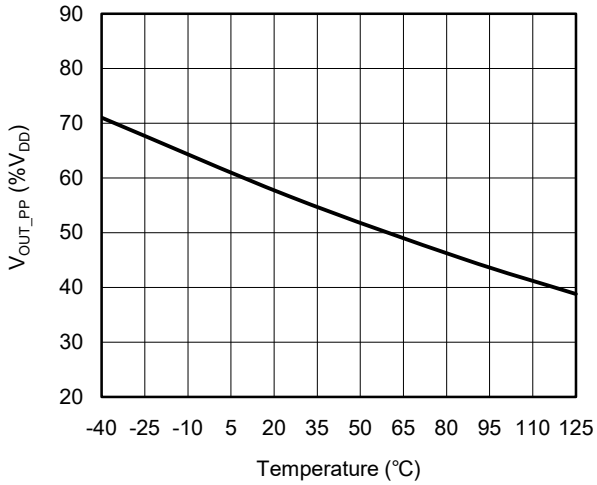
Supply Current vs. Temperature



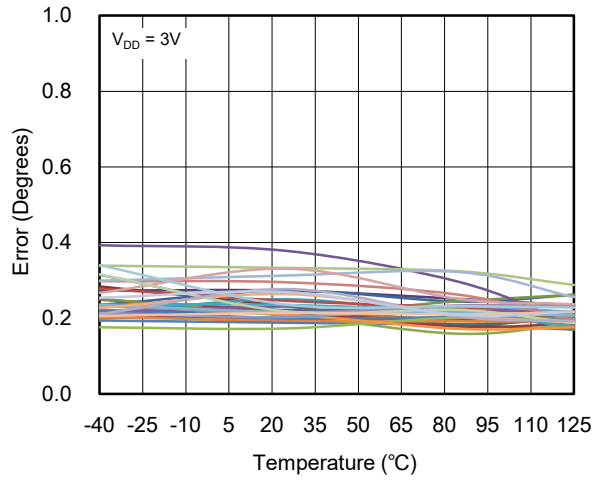
Power-Down Current vs. Temperature



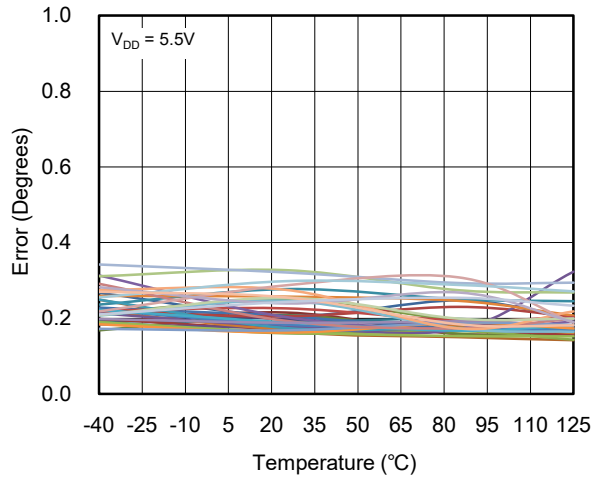
Output Voltage Peak-to-Peak vs. Temperature



Single Point Calibration Angular Error

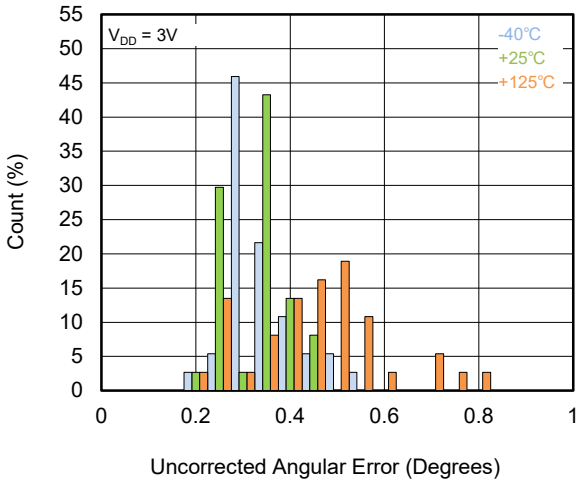


Single Point Calibration Angular Error

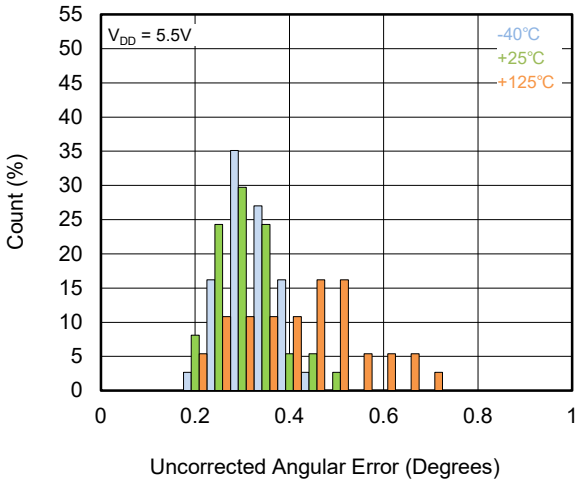


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

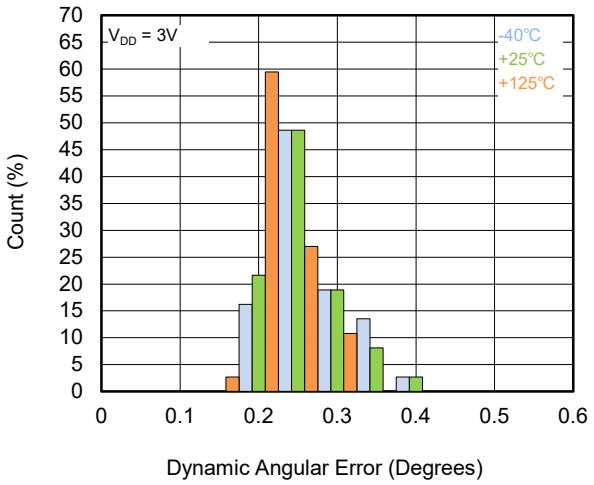
Uncorrected Angular Error



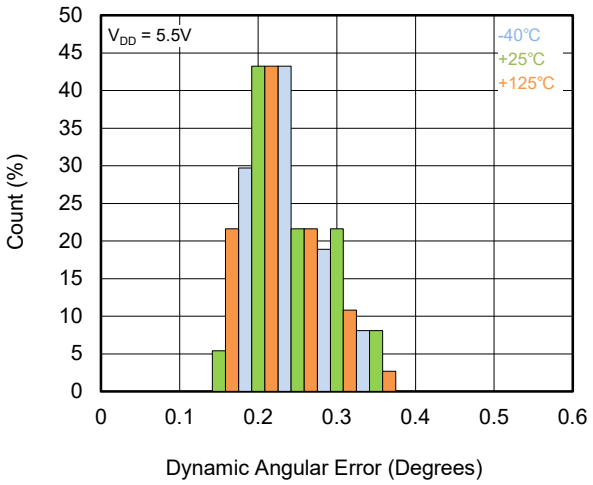
Uncorrected Angular Error



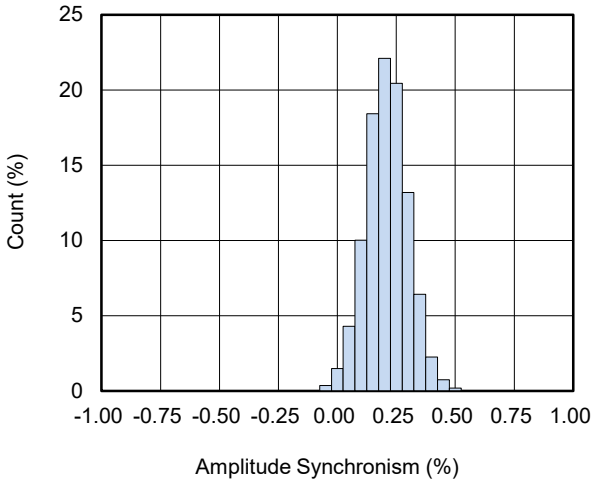
Dynamic Angular Error



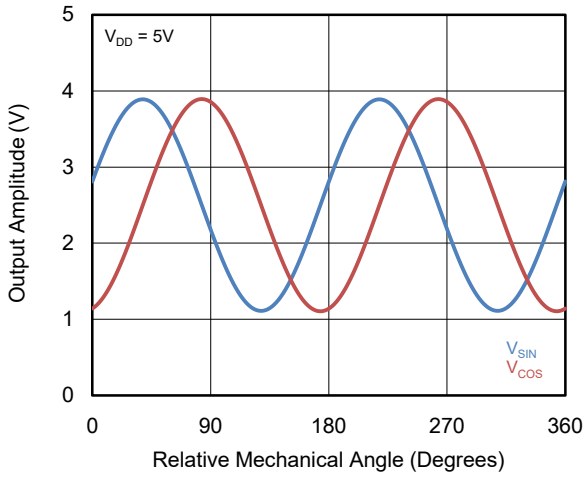
Dynamic Angular Error



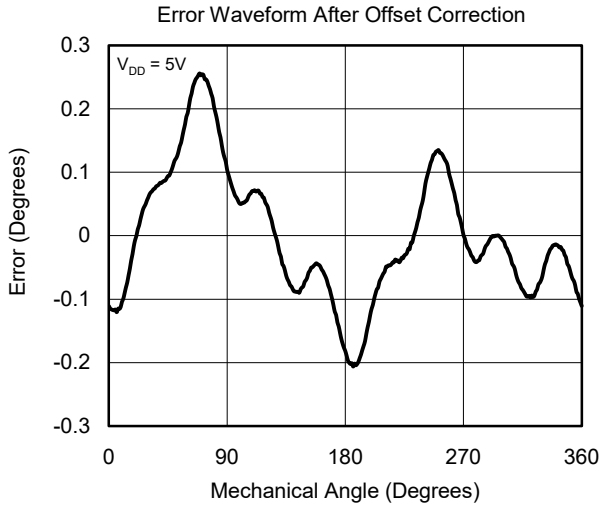
Amplitude Synchronism



Raw Output Waveforms



TYPICAL PERFORMANCE CHARACTERISTICS (continued)



FUNCTIONAL BLOCK DIAGRAM

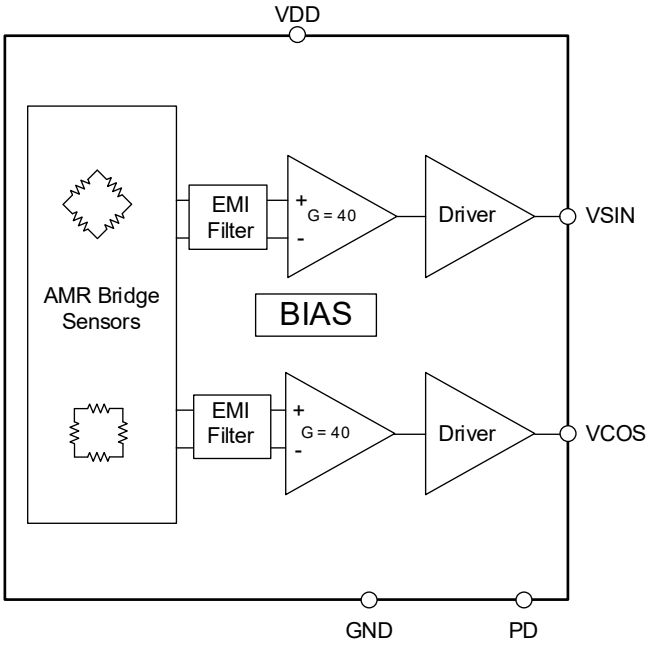


Figure 1. Block Diagram

DETAILED DESCRIPTION

Overview

The VCE4715 is an integrated AMR sensing solution. It combines an AMR sensing core with on-chip signal conditioning amplifiers and ADC driver circuitry, and delivers dual analog outputs (V_{SIN} and V_{COS}) that reflect the angular orientation of the ambient magnetic field.

The sine channel is illustrated in Figure 2. This channel integrates an AMR sensing element alongside auxiliary functional blocks for signal amplification, filtering, buffering, and control. Additionally, on-chip generation of a reference voltage is realized, with its magnitude scaled proportionally to the supply rail voltage.

Sensor bridge supply voltage regulation is handled by the device, with low-pass filtering implemented for the bridge supply to mitigate noise and enhance electromagnetic compatibility (EMC) performance. Bridge output voltages are scaled by a fixed gain factor and buffered to preserve signal integrity. Centered at the $V_{DD}/2$ common-mode voltage, the single-ended outputs can directly interface with the inputs of an external supply-referenced ADC.

To maximize utilization of the ADC input range, the sine and cosine output voltages follow the supply voltage closely—establishing a ratiometric operating configuration. Attaining superior signal performance requires precise amplitude and phase matching of the two output signals. Adequate amplifier bandwidth ensures minimal phase lag at the maximum rated rotational speed, supporting consistent signal integrity.

Integrated electromagnetic interference (EMI) filters at the sensor interface and inter-stage nodes effectively suppress high-frequency disturbances and out-of-band interference, ensuring clean signal transmission in noisy industrial environments.

The signal conditioning path consists of precision, ultra-low noise, continuous-time instrumentation amplifiers. To minimize silicon mismatch and maximize angular accuracy, a proprietary factory trimming process is executed at production, precisely nulling the initial input offset voltage and calibrating the dual-channel gain matching. This continuous-time architecture provides an inherently smooth, artifact-free analog output without the switching glitches or clock-induced ripple commonly found in modulated architectures.

Symmetrical layout and precision resistor networks provide excellent dc common-mode rejection ratio (CMRR) and power supply rejection ratio (PSRR). The amplifier front-end features an ultra-low broadband noise floor and exceptional phase linearity across the operating bandwidth, making it ideal for amplifying low-level AMR bridge signals in high-precision position sensing applications.

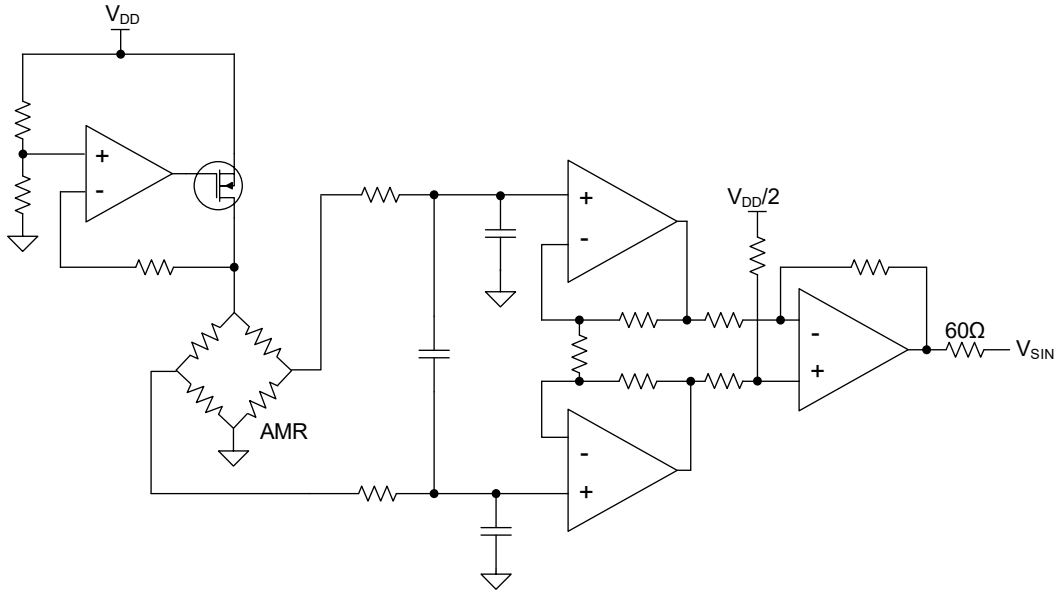


Figure 2. Detailed Internal Diagram of the VCE4715 Sine Channel

APPLICATION INFORMATION

The system features an inherent ratiometric nature. This is achieved when the ADC's input resolution aligns with V_{DD} in the same manner as the AMR sensor's output, minimizing the signal's reliance on supply voltage variations. Engineered for applications featuring a discrete processing integrated circuit (IC) or a supply voltage-referenced ADC, the on-chip AMR sensing integration delivers robust performance across voltage fluctuations.

Angle Calculation

Angle derivation from the AMR device's output requires the use of the arctangent2 trigonometric function. This enhanced function builds on the conventional inverse tangent by incorporating supplementary quadrant data. This additional quadrant information expands the magnetic angular range from -90° to 90° to a full span of -180° to +180°. Due to the detection range constraints of AMR technology, the computed magnetic angle repeats with each pole of the magnet. For a basic dipole magnet, absolute mechanical angle over 180° of rotation is derived via the following Equation:

$$\alpha = \frac{\arctan\left(\frac{V_{SIN}}{V_{COS}}\right)}{2}$$

Connection to Processor

Given the constrained output drive strength of the VCE4715, PCB interconnect trace length between the device and other integrated circuits (ICs) should be kept to a minimum. Implementing signal line shielding is advisable to mitigate interference. Optimal angular precision is achieved through mutual matching of external load capacitors and resistors. Bandwidth-limiting filters aligned with the system's sampling frequency should be incorporated prior to the ADC inputs, as this reduces the noise bandwidth effectively.

Within Figure 3, the input loading of the filter and ADC corresponds to the load resistance implemented on the V_{COS} and V_{SIN} pins. Meanwhile, the processor is capable of fulfilling arctan computations, offset calculation, storage of offset values, and supplementary calibration procedures.

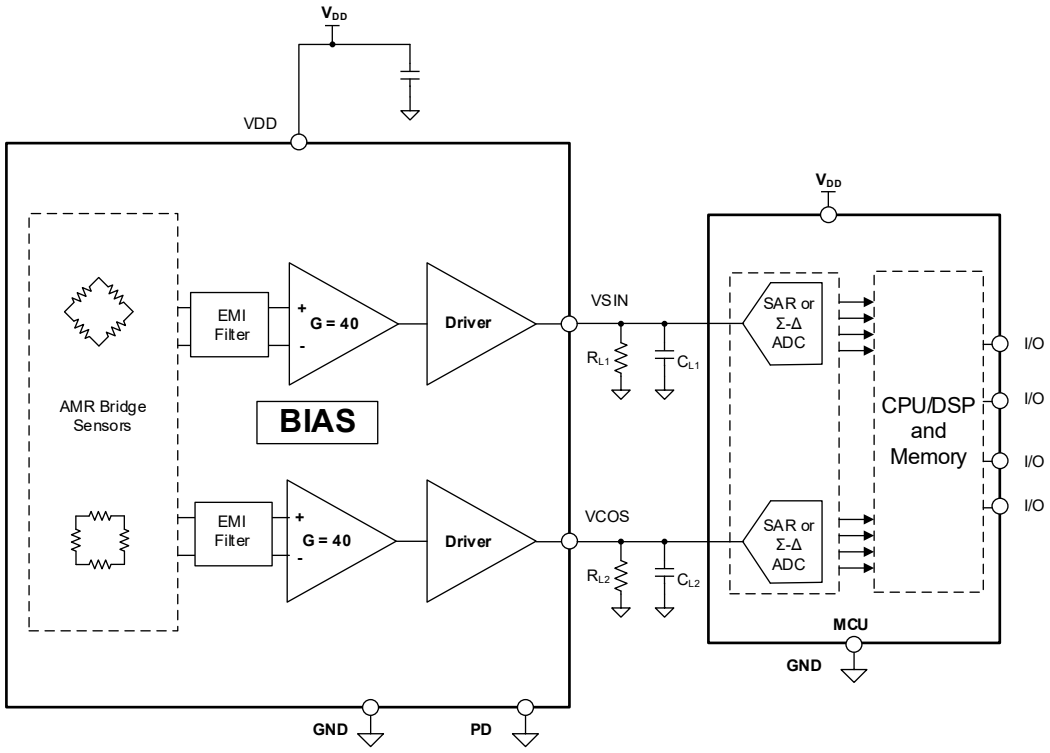


Figure 3. Typical Application Diagram with Separate Processor and Data Conversion

APPLICATION INFORMATION (continued)

Power-Down Mode

Tying the PD pin to VDD activates power-down mode. If PD is left floating, an on-chip pull-down keeps the device active. In power-down, the outputs are set to a moderately high internal resistance, so negligible current flows through the load resistors. Note that a short period is required at power-up to load the internal OTP values. Therefore, the PD pin must be kept low (grounded or left floating) for at least 1ms after V_{DD} reaches the minimum operating voltage (3V), and should not be pulled high during power-up.

Power Consumption

The VCE4715 exhibits a peak quiescent power dissipation of 43mW, measured when it operates at the upper-limit supply voltage of 5.5V with the supply current set to its rated maximum of 7.8mA.

V_{DD}, temperature, load resistance (R_L), load capacitance (C_L), and the frequency of the rotating magnetic field all influence the device's power consumption. Referencing R_L and C_L to ground is recommended for optimal performance. Internal current limiting protects the output pins against short circuits to VDD or ground.

Damage to the device may occur if it is inserted 180° reversed in the socket without limiting the supply current to 100mA.

Offset of Signal Outputs

An on-chip internally generated $V_{DD}/2$ serves as the reference for the single-ended output signals. Manufacturing process-related mismatch inaccuracies and additional imperfections give rise to offsets. To maintain tight tolerances, external loads connected to V_{SIN} and V_{COS} must be matched to one another. ESD and EMC protection is implemented via 60Ω series resistors integrated into the outputs, and using a large output load resistance reduces the influence of these series resistors to a minimum.

Signal Dependence on Air Gap Distance

Magnetic field direction sensing within the IC's x-y plane is achieved by the VCE4715, with the result showing minimal sensitivity to field strength once it surpasses the specified 25kA/m minimum threshold. Under homogeneous magnetic field conditions along the x-y axis, z-direction placement (airgap) is irrelevant to the outcome. The nominal z-axis spacing between the internal x-y plane and the plastic package's top surface is 0.400mm.

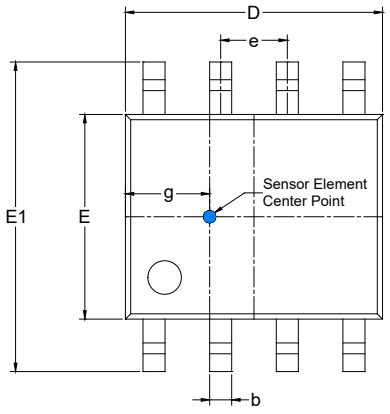
REVISION HISTORY

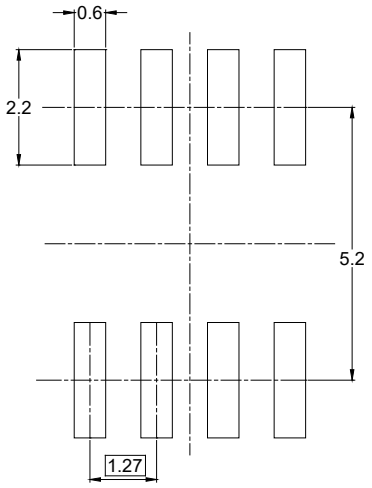
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original to REV.A (NOVEMBER 2026)	Page
Changed from product preview to production data	All

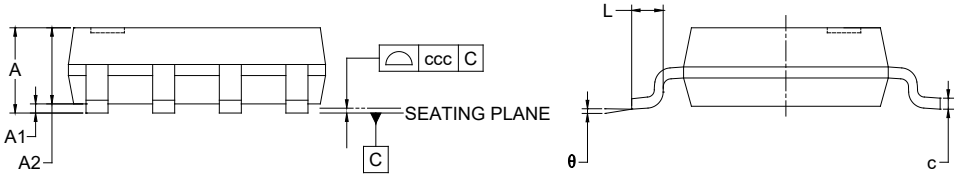
PACKAGE OUTLINE DIMENSIONS

SOIC-8





RECOMMENDED LAND PATTERN (Unit: mm)

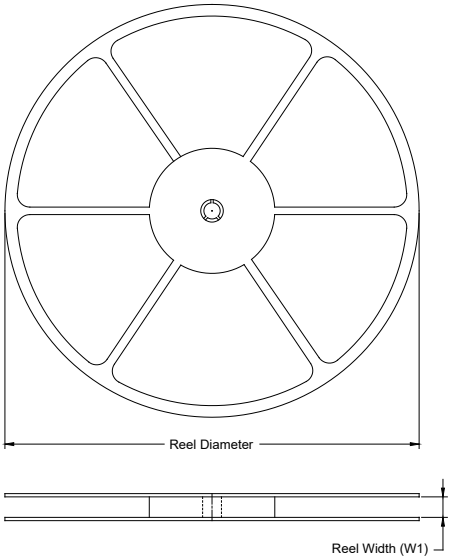


Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	1.450		1.750
A1	0.100	-	0.250
A2	1.350	-	1.550
b	0.330	-	0.510
c	0.170	-	0.250
D	4.700	-	5.100
E	3.800	-	4.000
E1	5.800	-	6.200
e	1.270 BSC		
g	1.570	-	1.640
L	0.400	-	1.270
θ	0°	-	8°
ccc	0.100		

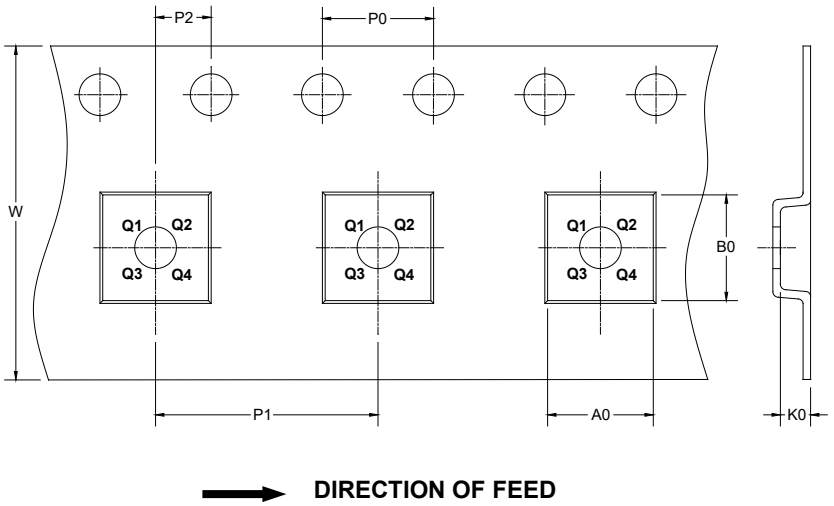
NOTES:
1. This drawing is subject to change without notice.
2. The dimensions do not include mold flashes, protrusions or gate burrs.
3. Reference JEDEC MS-012.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



DIRECTION OF FEED

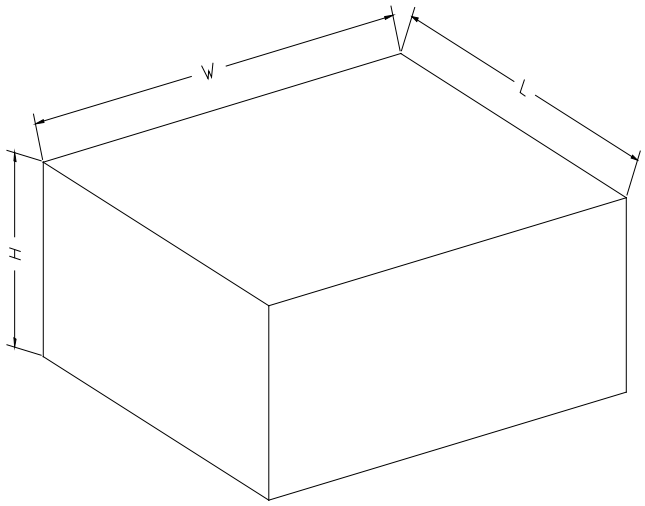
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
SOIC-8	13"	12.4	6.40	5.40	2.10	4.0	8.0	2.0	12.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002