VCE2755
14-Bit Anisotropic Magneto Resistive (AMR) Encoder

GENERAL DESCRIPTION

The VCE2755 is a highly integrated rotating magnetic encoder based on Anisotropic Magneto Resistive (AMR) and CMOS technologies. The single chip device provides digital output of magnetic field angle measurement with 14-bit resolutions in 360° angular range.

Utilizing the advantage of AMR being insensitive to magnetic field strength in its saturation mode, the VCE2755 has anti-vibration and anti-temperature drift features in angular detection, making it ideal for deployment in harsh environments. Its SAR-based ADC architecture yields ultra-low signal latency (<2μs) and supports high speeds up to 18000rpm.

Its built-in calibration algorithm provides real-time compensation for sensor and circuit zero-offset, amplitude, and temperature, while simultaneously offering various angle signal output methods: SPI, SSI, ABZ, UVW, and PWM. This makes it convenient for users to choose based on their different needs, making it suitable for various typical applications requiring angle position feedback and speed detection.

The VCE2755 is available in Green SOIC-8 and TQFN-3×3-16JL packages.

FEATURES

- **AMR and ASIC are Integrated into the Same Chip Package**
- **Wide Supply Voltage Range: 3.0V to 5.5V**
- **14-Bit Angular Resolution**
- **Accuracy Across Full Temperature Range: ±0.3°**
- **Interface: SPI, SSI, ABZ, UVW and PWM**
- **Maximum Tracking Speed: 18000rpm**
- **Angle Output Latency: <2μs**
- **0° to 360° Absolute Angular Outputs**
- **Low Magnetic Field Threshold Warning**
- **Compatible with Axial Installation and Eccentric Installation**
- **Built-in MTP, Allows Multiple Programming Cycles without Requiring a High-Voltage Programming Port**
- **Available in Green SOIC-8 and TQFN-3×3-16JL Packages**

APPLICATIONS

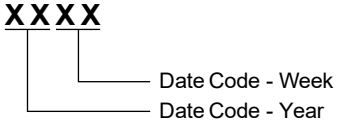
Brushless DC (BLDC) Motor
Servo Motor and Stepping Motor
UAV and Handheld Gimbal Angle Control
Rotary Angle Detection and Control for Industrial and Commercial Robot

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	CONFIGURATION	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
VCE2755	SOIC-8	-40℃ to +125℃	AB = 1000, Z = 4LSB, CW	VCE2755S076	2755 XXXX	Tape and Reel, 4000
			3-Wire SPI, CW	VCE2755S087		
			PWM = 971.1Hz, CW	VCE2755S108		
			AB = 256, Z = 1LSB, CW	VCE2755S121		
			3-Wire SPI, AB = 1024, Z = 1LSB, CCW	VCE2755S124		
			AB = 250, Z = 1LSB, CW	VCE2755S142		
			3-Wire SPI, AB = 256, Z = 1LSB, CCW	VCE2755S152		
			AB = 1024, Z = 4LSB, CCW	VCE2755S153		
	TQFN-3×3-16JL	-40℃ to +125℃	4-Wire SPI, AB = 1000, Z = 4LSB, CCW, Bandwidth BW0×4, Hysteresis 1LSB	VCE2755Q079	2755 XXXX	Tape and Reel, 4000
			4-Wire SPI, AB = 1024, Z = 4LSB, CCW, Bandwidth BW0×4, Hysteresis 1LSB	VCE2755Q102		
			4-Wire SPI, CW	VCE2755Q104		
			AB = 1024，Z = 1LSB，CW	VCE2755Q113		
			AB = 1000，Z = 1LSB，CCW	VCE2755Q134		

MARKING INFORMATION

NOTE: XXXXX = Date Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DD} ..... -0.5V to 6V
All Digital Port Pin Voltage ..... -0.5V to 6V
All Digital Port Pin Current……-20mA to 20mA
Junction Temperature .....+150℃
Storage Temperature Range……-50℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
Latch-Up ..... -400mA to 400mA
ESD Susceptibility (1) (2)
HBM.....±8000V
CDM .....±2000V

NOTES:

1. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.

2. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

RECOMMENDED OPERATING CONDITIONS

Supply Voltage, V_{DD} .....3.0V to 5.5V
All Digital Port Pin Voltage Range .....0.4V to V_{DD} - 0.4V
Operating Ambient Temperature Range.....-40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

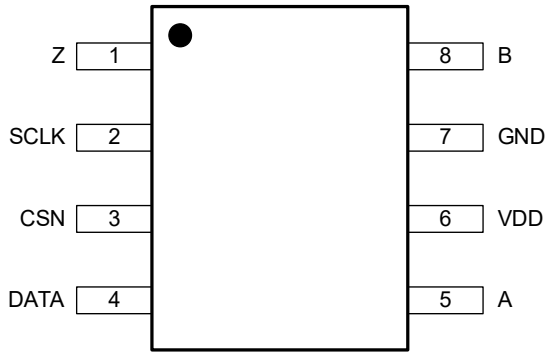
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

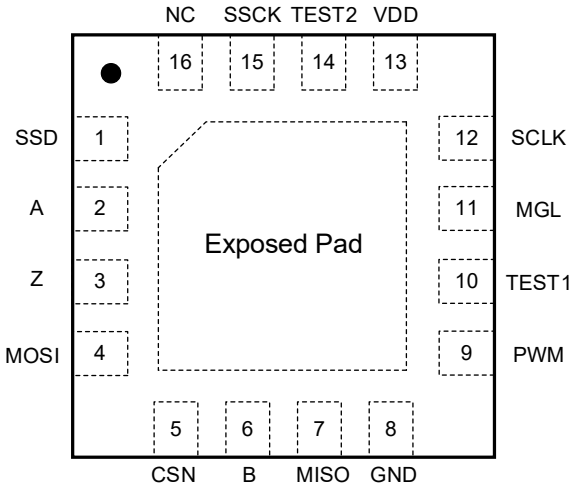
PIN CONFIGURATIONS

(TOP VIEW)



SOIC-8

(TOP VIEW)



TQFN-3×3-16JL

PIN DESCRIPTION

SOIC-8

PIN	PIN NAME			TYPE (1)	FUNCTION
	MODE 1	MODE 2	MODE 3		
1	Z	W	-	DO	Z/W signal output.
2	SCLK			DI	SPI clock signal, internal pull-up.
3	CSN			DI	SPI chip select signal, internal pull-up.
4	DATA			DI/O	SPI data input/output.
5	A	U	PWM	DO	A/U/PWM signal output.
6	VDD			P	Power supply.
7	GND			G	Ground.
8	B	V	-	DO	B/V signal output.

TQFN-3×3-16JL

PIN	PIN NAME				TYPE (1)	FUNCTION
	MODE 1	MODE 2	MODE 3	MODE 4		
1	SSD (SSI)	SSD (SSI)	U	A-	DO	SSD(SSI)/U/A - data output.
2	A	U	A	A+	DO	A/U/A+ signal output.
3	Z	W	Z	Z+	DO	Z/W/Z+ signal output.
4	MOSI (SPI 4-Wire) DATA (SPI 3-Wire)				DI/O	SPI 4-wire MOSI. SPI 3-wire DATA.
5	CSN				DI	SPI chip select signal, internal pull-up.
6	B	V	B	B+	DO	B/V/B+ signal output.
7	MISO (SPI 4-Wire) NC (SPI 3-Wire)				DO	SPI 4-wire MISO. SPI 3-wire NC.
8	GND				G	Ground.
9	PWM	PWM	V	B-	DO	PWM/V/B- signal output, PWM internal pull-up.
10	TEST1				DI	For production test only, keep floating in application.
11	MGL (2)	MGL (2)	W	Z-	DI	MGL (2)/W/Z-.
12	SCLK				DI	SPI Clock signal, internal pull-up.
13	VDD				P	Power Supply.
14	TEST2				DI	For production test only, keep floating in application.
15	SSCK(SSI)				DI	SSI interface Clock signal, internal pull-down.
16	NC				NC	NC.
-	Exposed Pad				-	Float or connect to ground.

NOTES:

1. DI: Digital Input, DO: Digital Output, DI/O: Digital Input and Output, G: Ground, P: Power.

2. Weak-field Warning. The MGL outputs a high level when the magnetic field is low, and outputs a low level when the magnetic field is normal.

ELECTRICAL CHARACTERISTICS

(T_A = -40℃ to +125℃, V_{DD} = 3.0V to 5.5V, typical values are measured at T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply						
Power Supply Voltage	V_{DD}	T_A = -40℃ to +125℃	3.0	3.3/5.0	5.5	V
Active Supply Current	I_{DD}			10		mA
DC Characteristics						
Minimum Resolution	LSB	14-bit effective angular resolution		0.022		°
Integral Non-Linearity	INL	Full temperature range, operating magnetic field > 300Gs		±0.3		°
Maximum Tracking Speed	Speed	1-pole pair			18000	rpm
Transient Noise (1)	TN	T_A = +25℃, RMS		0.01		°
Window Hysteresis	HYST	Configurable, HYST[2:0] = 010		0.022		°
System Delay	t_{DELAY}	Actual latency without compensation		2		μs
Power-On-Reset	V_{POR}		2.59	2.65	2.75	V
POR Hysteresis	V_{POR_HYS}			0.15		V
System Power-Up Time	$t_{POWER-UP}$			16		ms
Operational Temperature	T_A		-40		+125	℃
Angle Range	A		0		360	°
Digital I/O Characteristics						
Output Rising Time	t_{RO}	C_{LOAD} = 15pF			30	ns
Output Falling Time	t_{FO}	C_{LOAD} = 15pF			30	ns
Digital I/O Output Logic High Level	V_{HSO}	I_{OUT} = 2mA	V_{DD} - 0.4			V
Digital I/O Output Logic Low Level	V_{LSO}	I_{OUT} = 2mA			0.4	V
Digital I/O Input Logic High Level	V_{HSI}		0.7 × V_{DD}			V
Digital I/O Input Logic Low Level	V_{LSI}				0.3 × V_{DD}	V

NOTE: 1. Transient noise can be configured and adjusted according to the system filter bandwidth.

DYNAMIC CHARACTERISTICS

(T_A = -40℃ to +125℃, V_{DD} = 3.0V to 5.5V, typical values are measured at T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ABZ/PWM/UVW Output Mode Parameters						
AB Pulse/Turn	R_{AB}	Configurable	1		1024	ppr
Pair of Poles/Turn	R_{UVW}	Configurable	1		16	Pair
Frequency in PWM Mode	f_{PWM}	Configurable, PWM_FREQ = 0	-5%	971.1	+5%	Hz
		Configurable, PWM_FREQ = 1	-5%	485.6	+5%	
Rising Time of PWM Mode	t_{PWM-R}	C_{LOAD} = 1nF		1		μs
Falling Time of PWM Mode	t_{PWM-F}	C_{LOAD} = 1nF		1		μs
MTP Characteristics						
Read/Write Voltage	V_{MTP}		3.0		5.5	V
Erasable/Write Cycles	Memory Endurance			1000		Cycle
Data Retention		T_J = +150℃		10		Year

TYPICAL PERFORMANCE CHARACTERISTICS

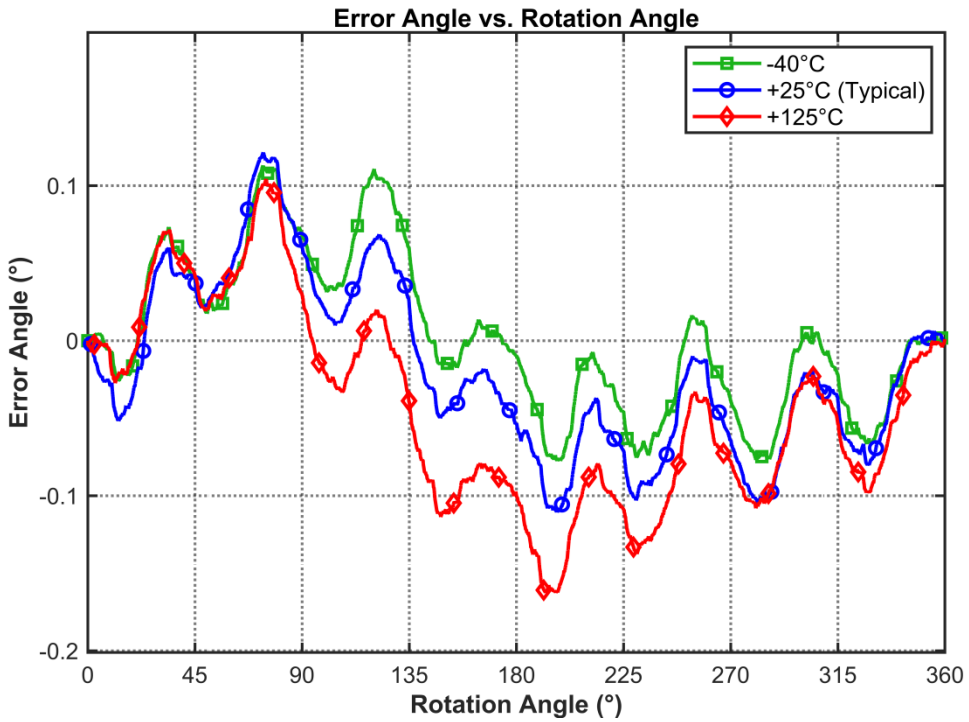


Figure 1. Full Temperature Range Accuracy (INL) and Angle Curve (Working Magnetic Field > 300Gs)

TYPICAL APPLICATION CIRCUITS

For the VCE2755 in an SOIC-8 package, when operating in ABZ/UVW/PWM/3-wire SPI output modes, the application reference circuit diagram is shown in Figure 2:

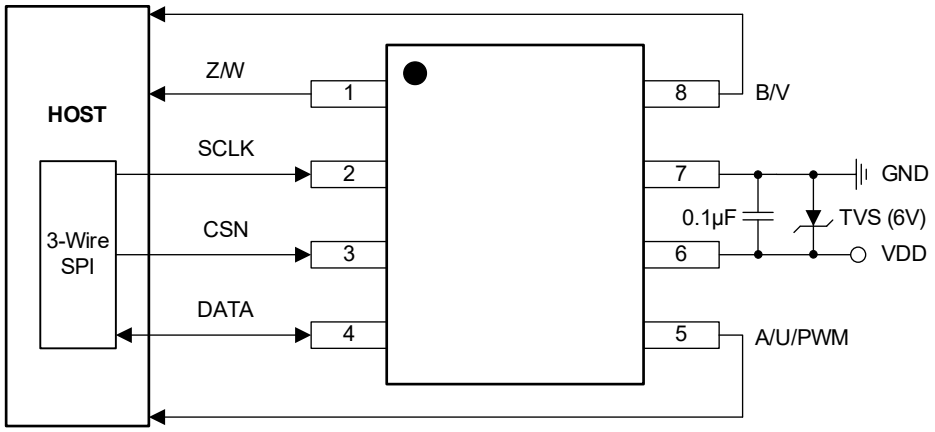


Figure 2. Application Circuit for ABZ/UVW/PWM/3-Wire SPI Modes (SOIC-8)

For the VCE2755 in an TQFN-3×3-16JL package, when operating in ABZ/UVW/PWM/4-wire SPI output modes, the application reference circuit diagram is shown in Figure 3:

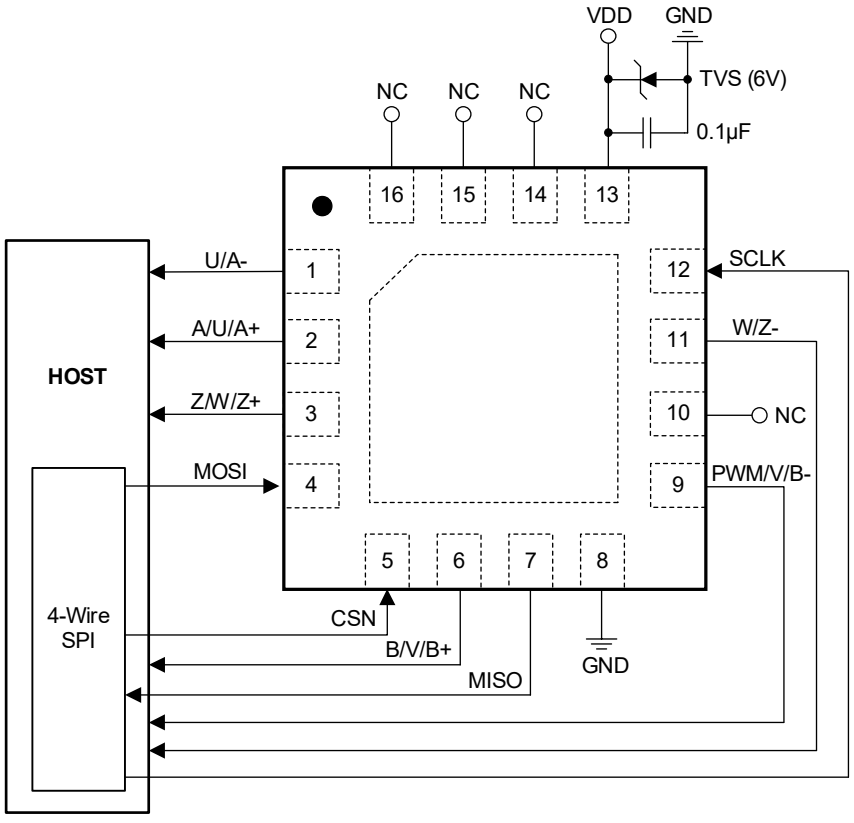


Figure 3. Application Circuit for ABZ/UVW/PWM/4-Wire SPI Modes (TQFN-3×3-16JL)

FUNCTIONAL BLOCK DIAGRAM

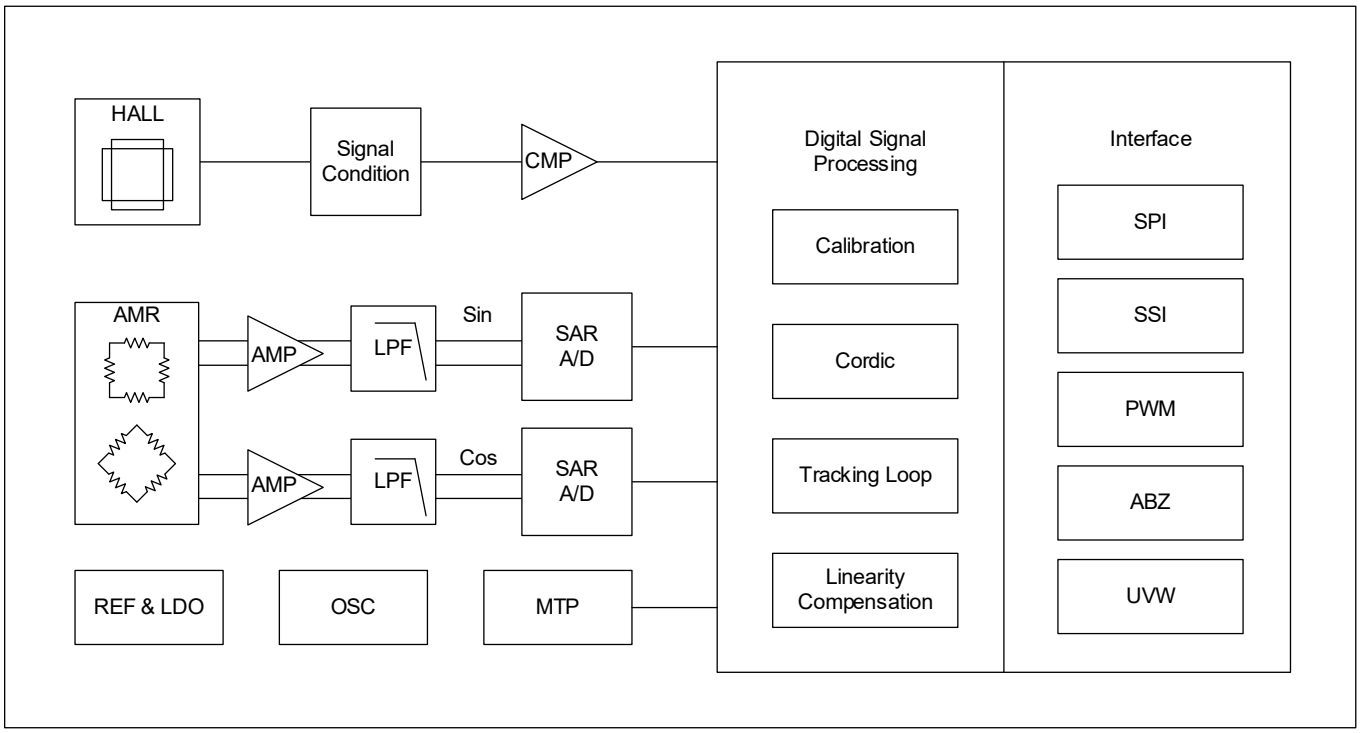


Figure 4. Block Diagram

DETAILED DESCRIPTION

Overview

VCE2755 incorporates two channels of AMR magnetic sensors, which provide sine and cosine outputs that vary with the magnetic field angle. The signals are amplified and digitally converted, then processed together with Hall signals through an algorithm to obtain an angle signal ranging from 0° to 360°, which is then output via various interfaces. The SAR-structured ADC combined with Tracking Loop filtering ensures extremely low signal latency. The MTP stores configurations of various modes, compensation parameters, and the zero position of external motors, and can be rewritten multiple times.

Rotation Direction Definition and Output Signals

With the magnet mounted directly above the chip and centers aligned, Figure 5 shows the top-view schematic and output data versus angle during clockwise rotation, while Figure 6 displays the same for counterclockwise rotation.

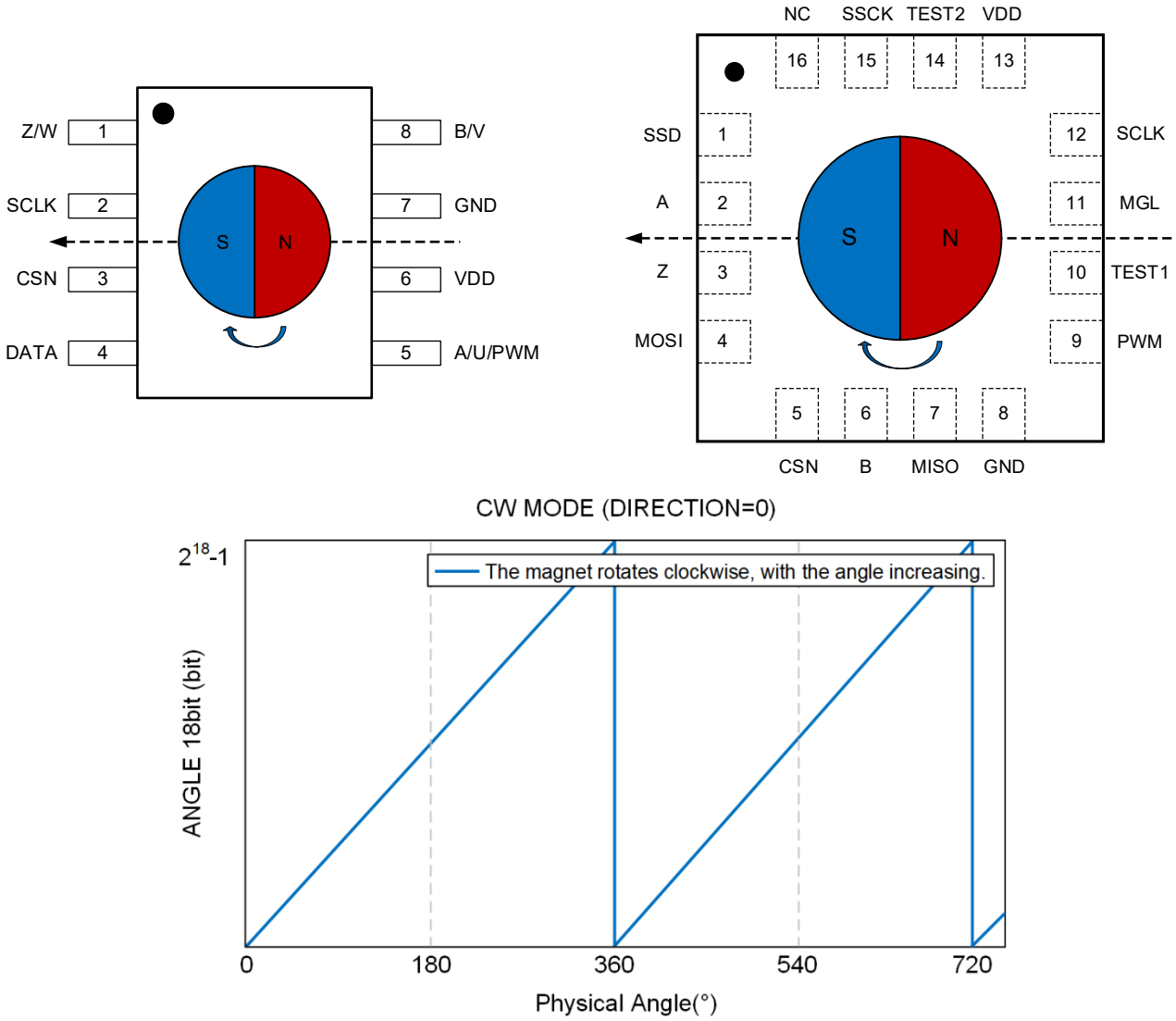


Figure 5. CW Mode: The Magnet Rotates Clockwise. Magnet-Chip Relation and Angle Output

DETAILED DESCRIPTION (continued)

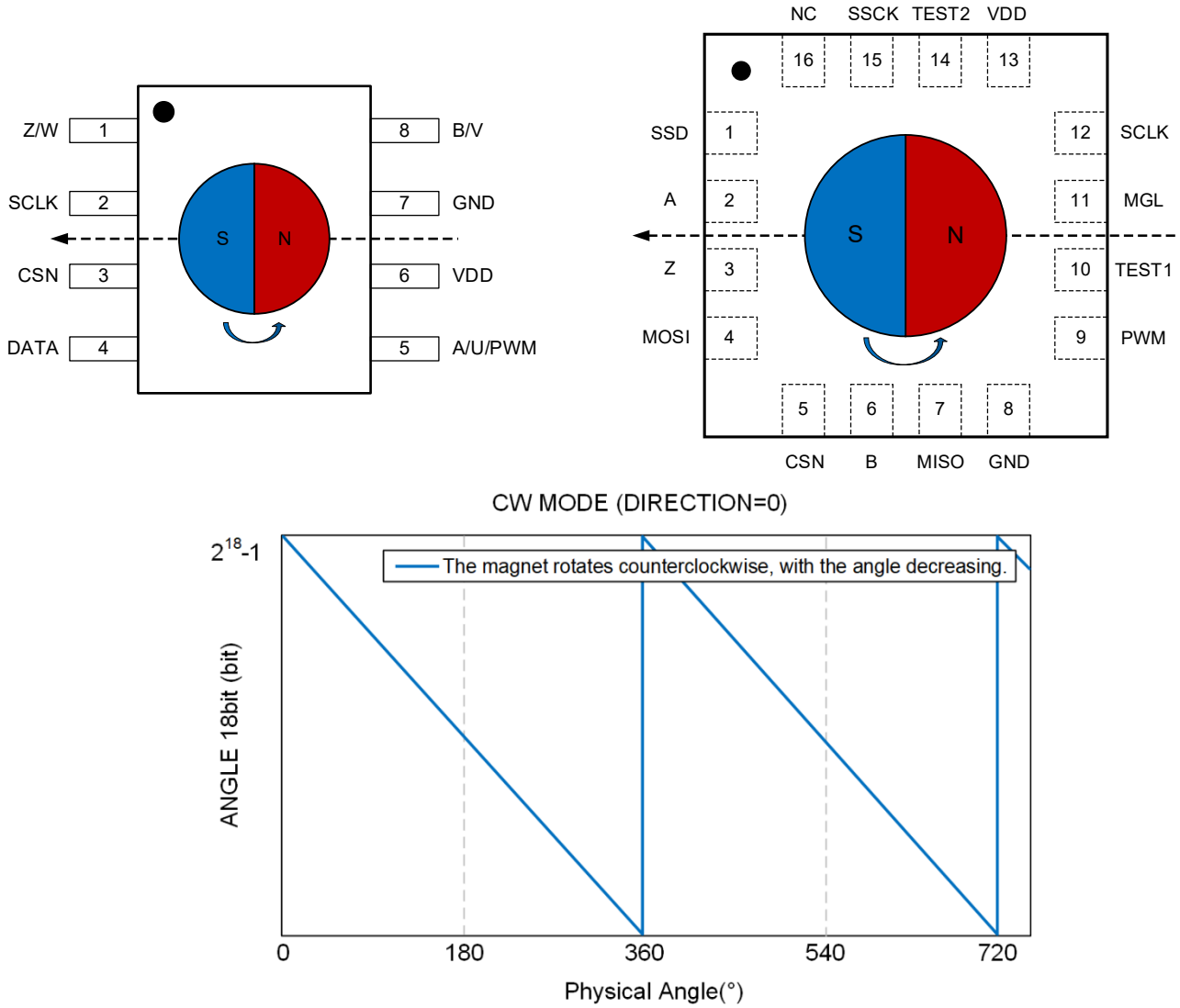


Figure 6. CW Mode: The Magnet Rotates Counterclockwise. Magnet-Chip Relation and Angle Output

DETAILED DESCRIPTION (continued)

ABZ Output Mode

Figure 7 illustrates the output signals of A, B, and Z during clockwise (CW)/counterclockwise (CCW) magnet rotation. For CW rotation (refer to Figure 5), the A signal lags the B signal by a quarter-period. For CCW rotation (refer to Figure 6), the A signal leads the B signal by a quarter-period. The Z signal indicates the 0° angular position, generating one pulse per 360° magnet rotation. The Z-signal high-level pulse width is user-programmable via register Z_WIDTH[2:0] to achieve specific duty cycle requirements. Alternatively, the Z high-level width can be set to 180°, where one complete Z pulse cycle (high + low states) constitutes a 360° signal output.

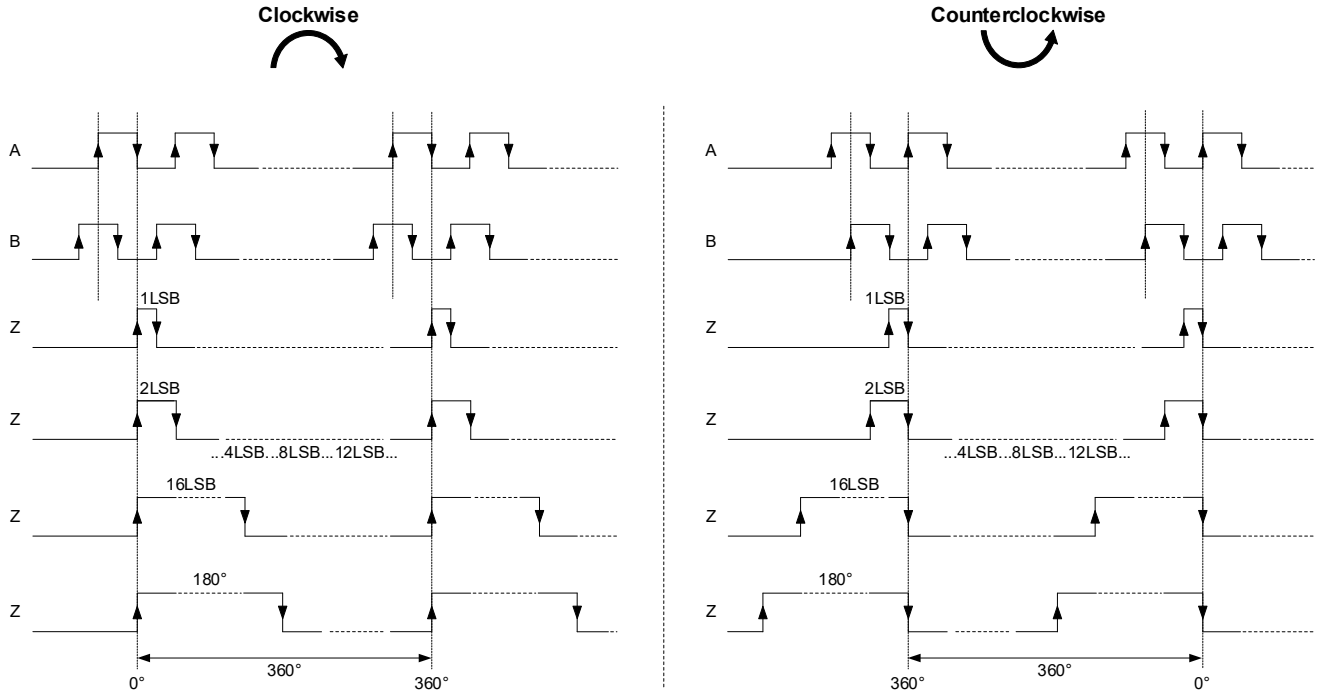


Figure 7. ABZ Signal Output Diagram (Z Pulse Width Optional: 1/2/4/8/12/16LSB/180°)

The ABZ output resolution (PPR) is configurable via register ABZ_RES[9:0], supporting 1~1024 pulses per revolution (PPR). As shown in Figure 8, when configured for 1024 PPR, the output provides 4096 steps per revolution.

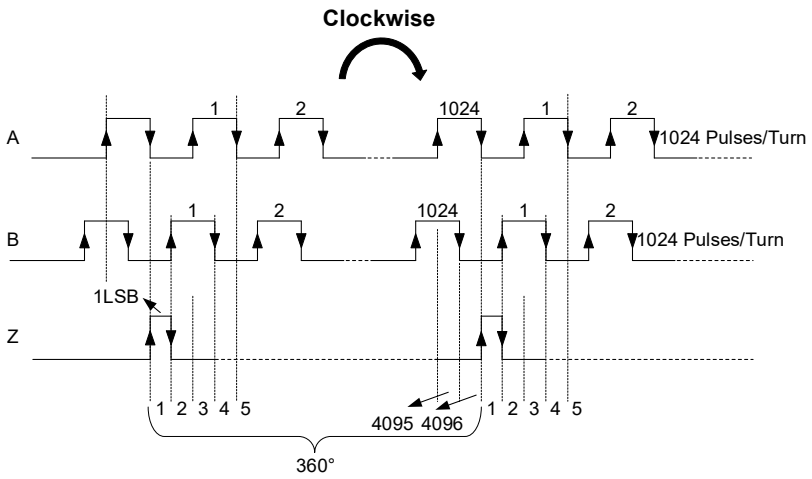


Figure 8. AB Signal Resolution is 1024 Pulses per Revolution in CW Mode during Clockwise Magnet Rotation

In addition, the polarity of the ABZ output signal can be inverted by configuring the ABZ_INV[0] register.

DETAILED DESCRIPTION (continued)

Output Pulse Sequences of ABZ Signals during the Power-Up

During the $t_{POWER-UP}$ period in ABZ output mode, the output pulse sequence can be configured via the ABZ_INI_DELAY[1:0] register. There are three selectable options. The factory default is Pulse Sequence 1.

Pulse Sequence 1: This is the standard pulse output during power-up, as shown in Figure 9.
Pulse Sequence 2: During power-up, the Z1 pulse goes from low to high and remains high for 5ms. Following this, the AB outputs the absolute angle pulse signal of the power-up initial position, as shown in Figure 10.
Pulse Sequence 3: During power-up, the Z1 pulse goes from low to high and remains high for 10ms. Following this, the AB outputs the absolute angle pulse signal of the power-up initial position, as shown in Figure 11.

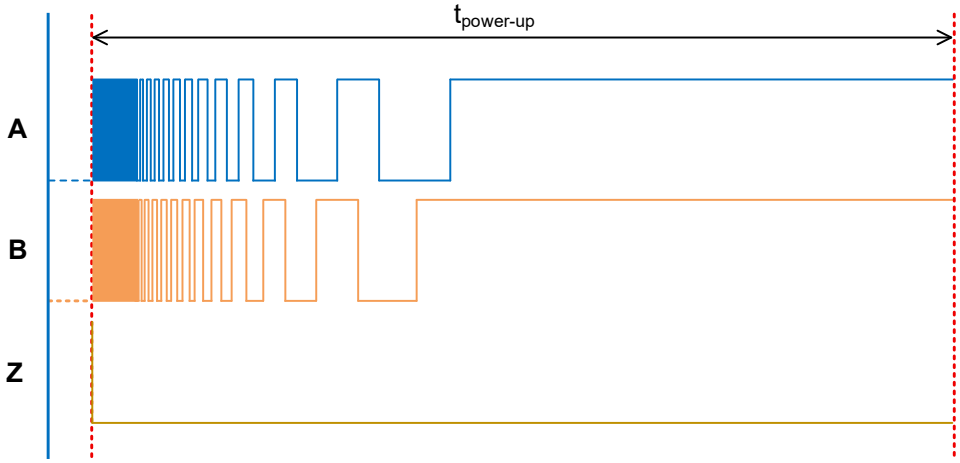


Figure 9. Power-Up Status Signal of Pulse Sequence 1

In Pulse Sequences 2 and 3, the Z pulse is divided into two parts: Z1 and Z2. The high-level duration of Z1 is fixed, being 5ms in Pulse Sequence 2 and 10ms in Pulse Sequence 3. The high-level duration of Z2 depends entirely on the ABZ resolution and the configuration of the Z signal width register. By counting the number of AB pulses after the Z pulse transition point (i.e., the end of Z1 and the beginning of Z2), the user can calculate the initial angular position at power-up (relative to the chip's zero position), namely the absolute angle at power-up. The calculation depends on the resolution PPR and the AB pulse count (see Table 1). Furthermore, the AB output pulse frequency is related to the PPR and can be calculated using the formula: Frequency = PPR × 244.140625Hz. When the ABZ resolution is set to 1024 and the Z signal width register is configured to 8 LSB, the ABZ output waveforms of Pulse Sequences 2 and 3 are shown in Figure 10 and Figure 11.

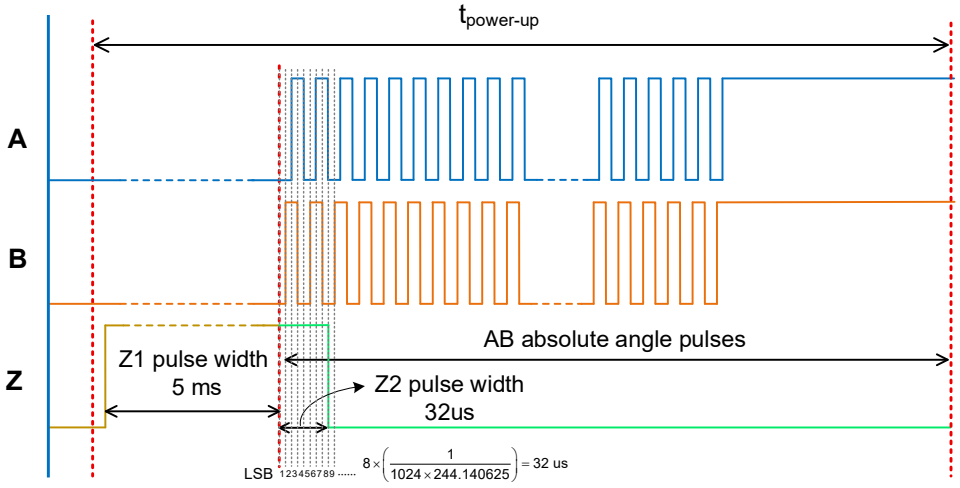


Figure 10. Power-Up Angular Output Signal of Pulse Sequence 2

DETAILED DESCRIPTION (continued)

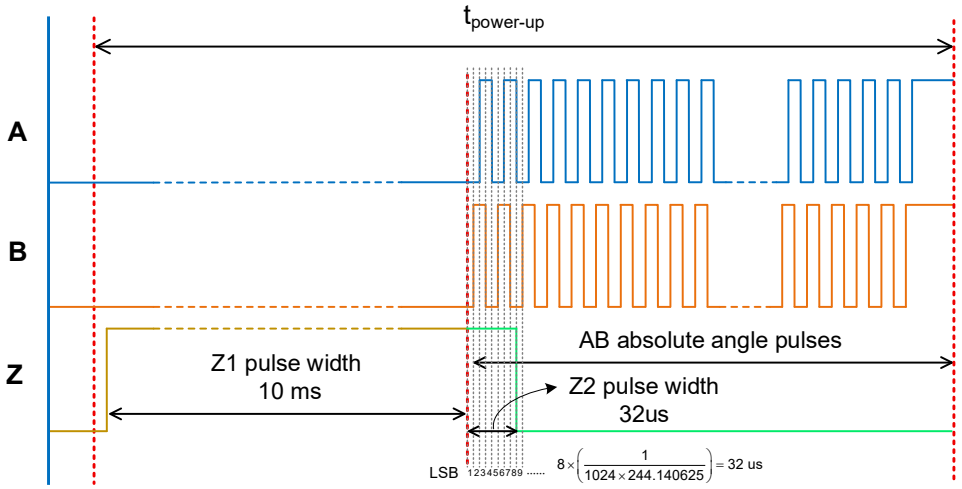


Figure 11. Power-Up Angular Output Signal of Pulse Sequence 3

Table 1. ABZ Output Power-Up Pulse Sequences Configuration Description

Pulse Sequence	Angle Range	Calculation
B leads A	0° to 180°	ANGLE = $\frac{360}{PPR}$ ×number of pulse read
A leads B	180° to 360°	ANGLE = 360 - $\frac{360}{PPR}$ ×number of pulse read

Example: When PPR = 1024, the number of A (B) pulses at power-up is 415, and since A leads B, the power-up absolute angle = $360-\frac{360}{1024}\times415=214.1016°$.

DETAILED DESCRIPTION (continued)

UVW Output Mode

The electrical phases U, V, and W are separated by 120 electrical degrees. The corresponding mechanical angle is determined by the motor's pole pair count. Users can configure the UVW pole pairs per revolution (PPR_UVW) through register UVW_RES[3:0] to meet application requirements. Figure 12 illustrates the UVW output signals for 1 pole pair and 2 pole pairs during clockwise (CW) rotation (DIRECTION register = 0) of the magnet. Figure 13 shows the ABZ and UVW output waveforms during clockwise rotation (CW mode, DIRECTION register = 0) with AB resolution PPR = 9, Z pulse width = 1LSB (Least Significant Bit), and UVW configured for 3 pole pairs.

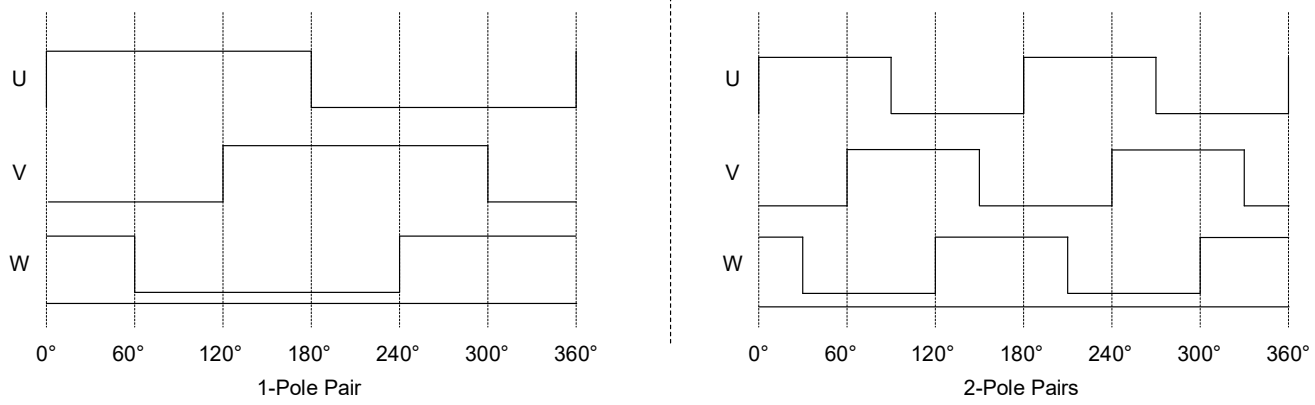


Figure 12. UVW Waveform for 1 and 2 Pole Pairs in CW Mode with Clockwise Magnet Rotation

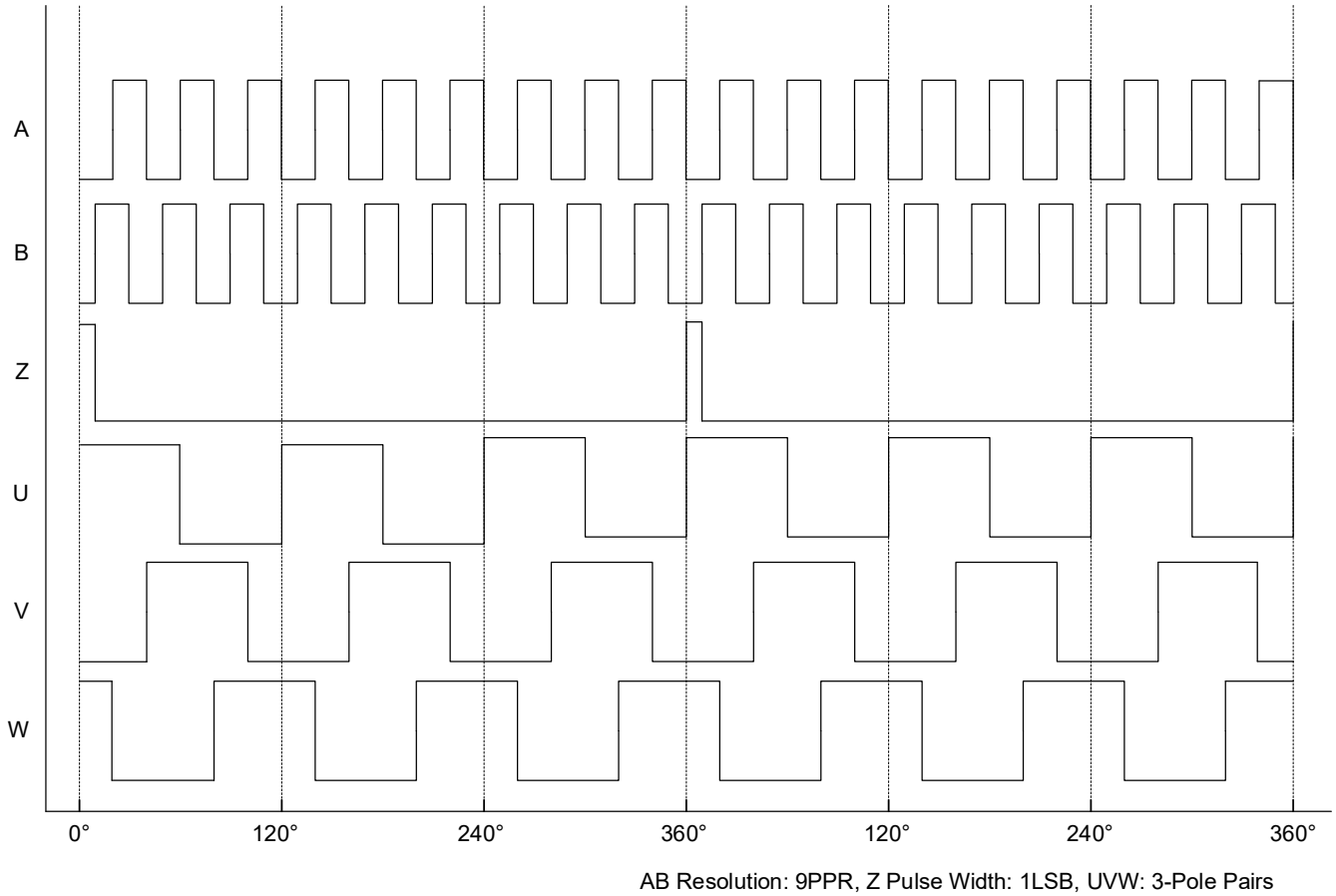


Figure 13. ABZ and UVW Output Waveform in CW Mode with Clockwise Magnet Rotation

DETAILED DESCRIPTION (continued)

PWM Output Mode

The PWM output resolution is 12 bits. One full PWM signal period consists of 4119 minimum unit pulse widths t_U, where each t_U depends on the PWM output frequency. By default, the PWM output frequency is 971.1Hz, corresponding to a minimum unit t_U of 250ns. The PWM output frequency can also be set to 485.6Hz by configuring the PWM_FREQ[0] register, in which case the minimum unit t_U is 500ns.

As shown in Figure 14, the PWM signal begins with a start pulse $t_{START,}$ consisting of 16 consecutive high-level unit widths t_U, and ends with an end pulse $t_{END,}$ consisting of 8 consecutive low-level unit widths t_U. The intermediate minimum unit pulse count from 0 to 4095 corresponds to an absolute angle range of 0° to 360°. With the default PWM output frequency of 971.1Hz, each unit t_U has a width of 250ns, corresponding to an angular resolution of 0.088°.

PWM angle calculation formula: $\text{Angle} = \left[4119\left(\frac{t_{ON}}{t_{PWM}}\right) - 16\right] \times \frac{360}{4096}$

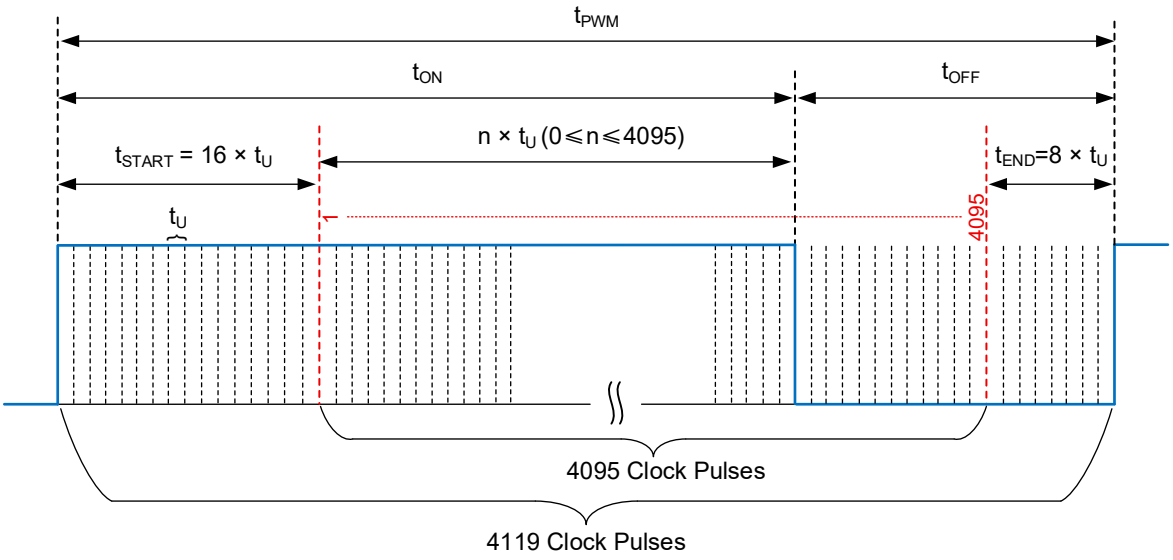


Figure 14. PWM Output Signal Diagram

DETAILED DESCRIPTION (continued)

SPI Interface

VCE2755 supports both 3-wire and 4-wire SPI synchronous serial communication interfaces. The transfer protocol uses Mode 3, specifically CPOL = 1, CPHA = 1, where SCLK idles at high level, the first clock edge is falling edge, the second clock edge is rising edge, and data is sampled on the rising edge. The SPI timing is shown in Figure 15.

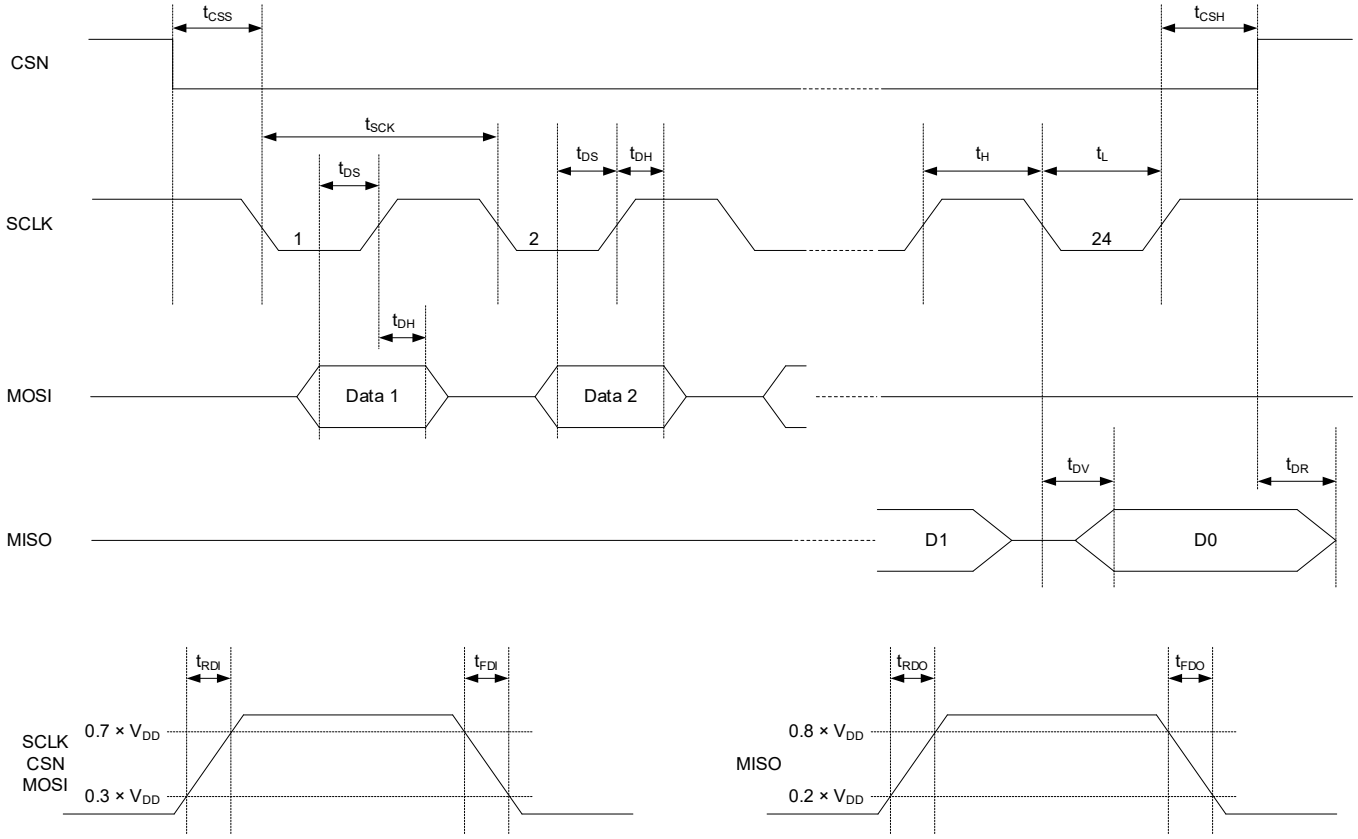


Figure 15. SPI Timing Sequence

Table 2. SPI Timing Requirement

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
CSN Setup Time	t_{CSS}	100			ns
CSN Hold Time	t_{CSH}	0.5 × t_{SCK}			ns
SCLK High Time	t_H	30			ns
SCLK Low Time	t_L	30			ns
SCLK Cycle Time	t_{SCK}	60			ns
Input Rise Time	t_{RDI}		10		ns
Input Fall Time	t_{FDI}		10		ns
Data Output Rise Time	t_{RDO}		10		ns
Data Output Fall Time	t_{FDO}		10		ns
Data Setup Time	t_{DS}	10			ns
Data Hold Time	t_{DH}	10			ns
Data Valid Time	t_{DV}			25	ns
Data Release Time	t_{DR}			30	ns

DETAILED DESCRIPTION (continued)

SPI Register Read/Write

SPI communication is triggered on the falling edge of the chip-select signal CSN and ends on its rising edge. Data is sampled on the rising edge of the SCLK clock signal. In 4-wire SPI applications, MOSI serves as the chip data input and MISO as the chip data output. In 3-wire SPI applications, DATA functions as both input and output. R/W defines the SPI read/write command: when R/W=0, an SPI write operation is performed; when R/W=1, an SPI read operation is performed.

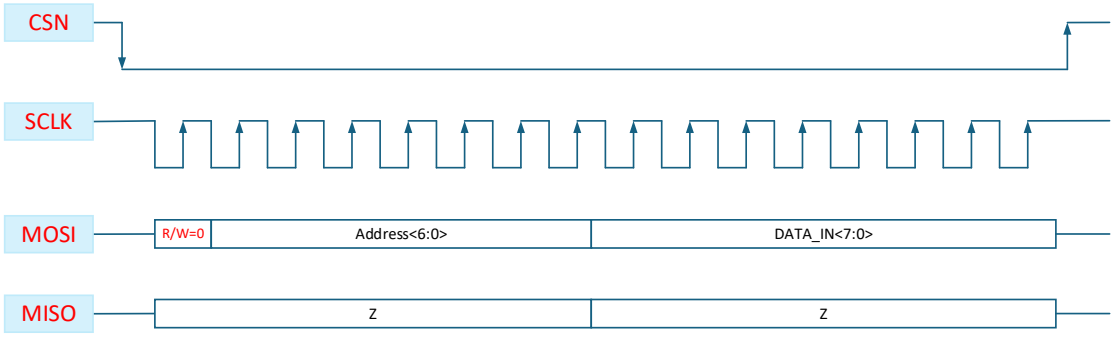


Figure 16. 4-Wire SPI Write Mode Timing Diagram

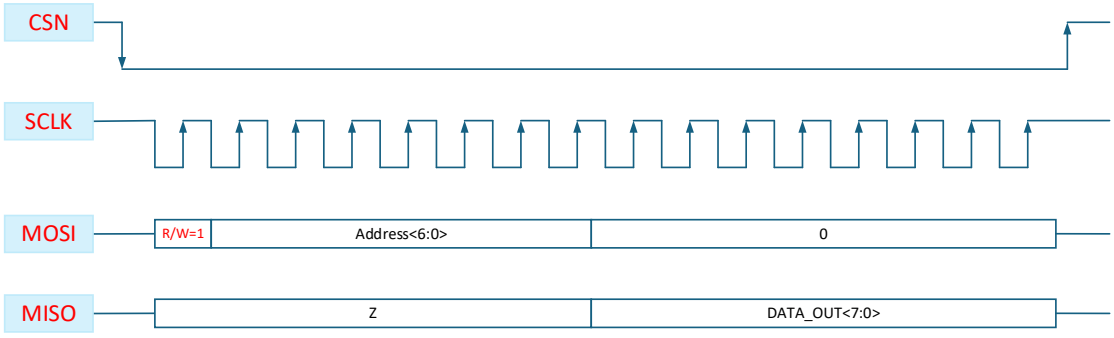


Figure 17. 4-Wire SPI Read Mode Timing Diagram

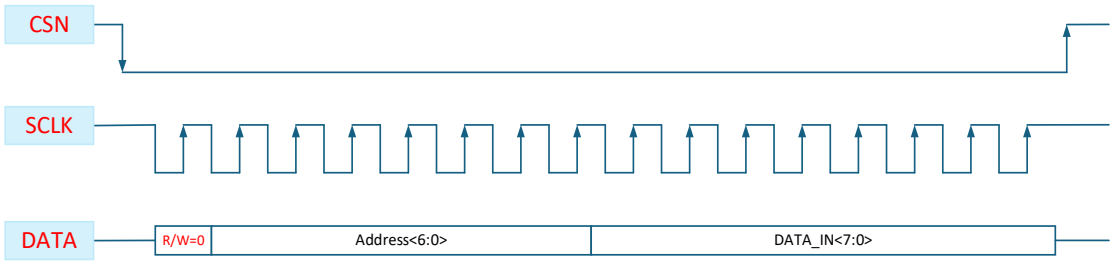


Figure 18. 3-Wire SPI Write Mode Timing Diagram

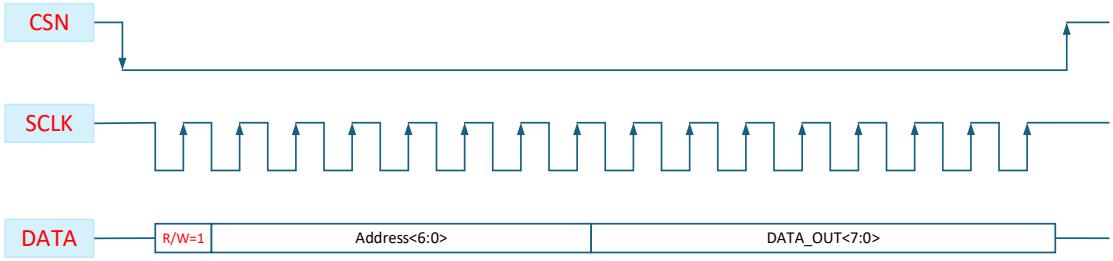


Figure 19. 3-Wire SPI Read Mode Timing Diagram

DETAILED DESCRIPTION (continued)

SPI Single and Continuous Angle Reading

In single-read mode, one complete set of angle data is read out with each operation. After CSN is pulled low, a read command 0x83 (R/W=1b, Address<6:0>=000 0011b) must be sent, and the register group 0x03, 0x04, and 0x05 is read. After the data group is retrieved, CSN is pulled high. To read the next group of data, CSN must be pulled low again and the read command resent. The 4-wire SPI timing is shown in Figure 20, and the 3-wire SPI timing is shown in Figure 22.

To improve the efficiency of angle data reading, continuous-read mode can be used. As shown in Figure 21 for 4-wire SPI and Figure 23 for 3-wire SPI, after CSN is pulled low, a single read command 0x83 (R/W=1b, Address[6:0]=000 0011b) is sent. Without pulling CSN high, data will be cyclically read in groups of 0x03, 0x04, and 0x05, until CSN is pulled high to terminate the continuous read. In this mode, while the CRC of the N^{th} data group is being read, the angle data of the $(N+1)^{th}$ group is latched.

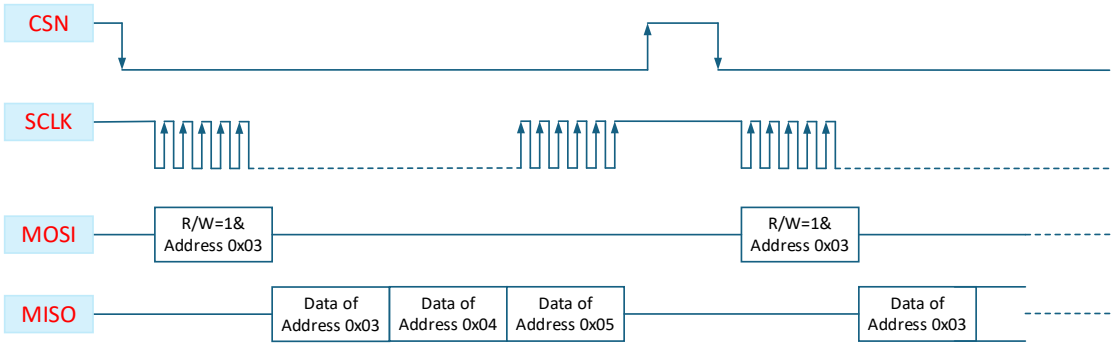


Figure 20. 4-Wire SPI Single Read Angle Data

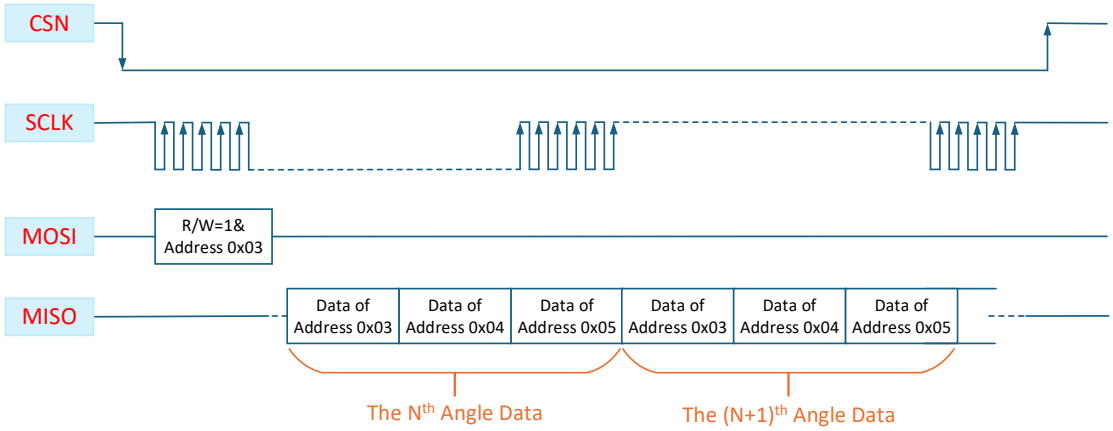


Figure 21. 4-Wire SPI Continuous Read Angle Data

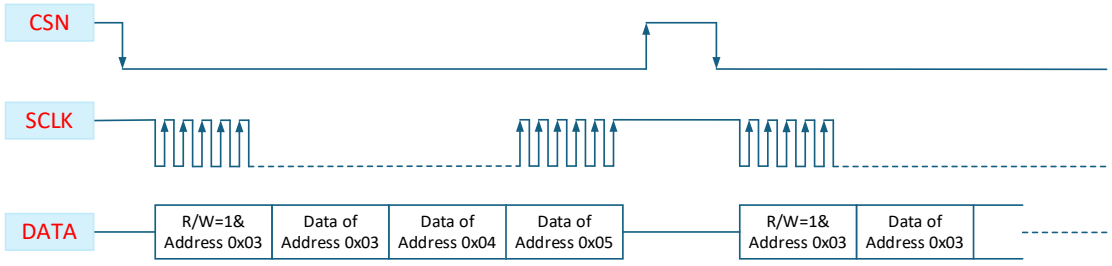


Figure 22. 3-Wire SPI Single Read Angle Data

DETAILED DESCRIPTION (continued)

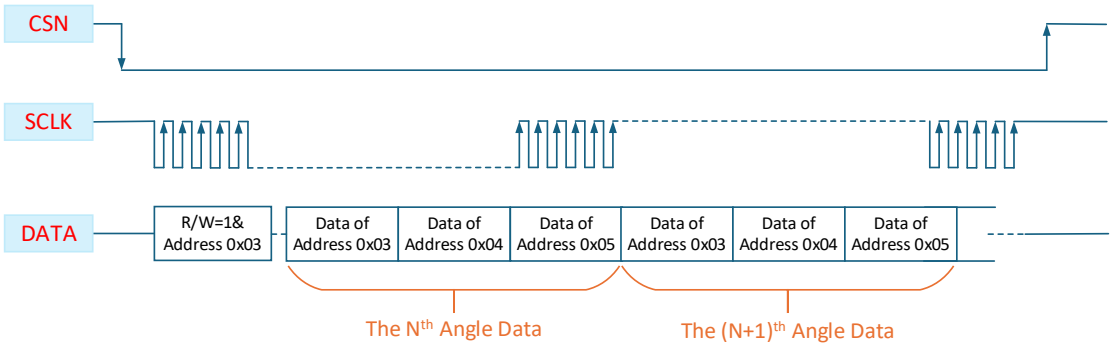


Figure 23. 3-Wire SPI Continuous Read Angle Data

SPI Angle Output

Registers 0x03, 0x04, and 0x05 store 18-bit angle data, where the effective number of bits for the angle data is 14 bits. Users can obtain higher-resolution data through filtering based on the acquired 18-bit angle data. The read angle data is based on the zero-position angle defined by the application. The current 18-bit angle output ANGLE = the internally generated original 18-bit angle (filter output) - the 18-bit offset angle ANG_OS (the high 12 bits are the zero-position register ZERO_POS[11:0], and the low 6 bits are padded with zeros).

Angle Calculation Formula: ANGLE = ANGLE (18-bit) × $\frac{360}{2^{18}}$

SSI Interface

The SSI interface timing and its parameters are shown in Figure 24 and Table 3.

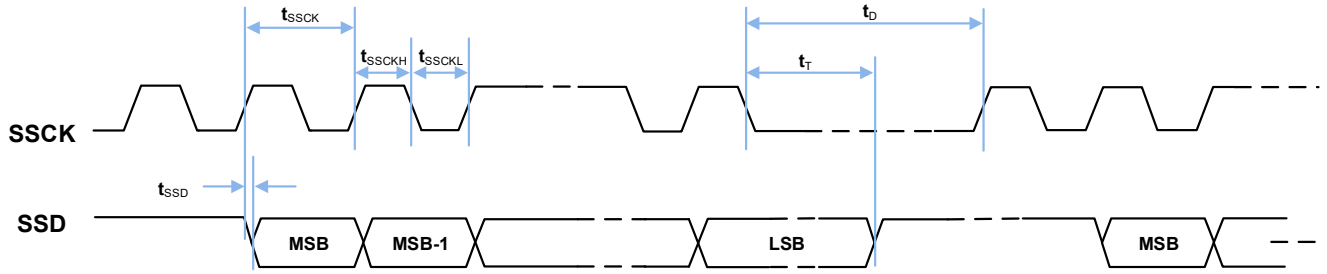


Figure 24. SSI Timing

Table 3. SSI Timing Requirement

PARAMETER	SYMBOL	MIN	MAX	UNITS
	t_{SSD}		25	ns
SSCK Period	t_{SSCK}	0.05	16	μs
SSCK Low Level	t_{SSCKL}	0.02	8	μs
SSCK High Level	t_{SSCKH}	0.02	8	μs
Transfer Timeout (Monoflop Time)	t_T	25		μs
Interval Time (Wait Time for Next Data Reading)	t_D	40		μs

DETAILED DESCRIPTION (continued)

As shown in Figure 25, SSI communication uses 25 clock cycles per data frame. The first clock serves as the start signal, and data transmission begins from the second clock, with data sampled on the falling edge of SSCK. When idle, SSCK remains low, and the interval between two data frames is ≥ 40μs.
One data frame consists of 24 bits, including 16-bit angle data, 2-bit status bits, and 6-bit CRC check bits, as follows:

- D15~D0: 16-bit angle data.
- S1 and S0: 2-bit status bits. S1 indicates a weak magnetic field warning, and S0 is an internally defined flag.
- CRC5~CRC0: 6-bit CRC, calculated over the above 18-bit data (16-bit angle data + 2-bit status bits). The corresponding CRC generator polynomial is $X^6 + X + 1$, with an initial value of 000000b. Data input and output are not inverted.

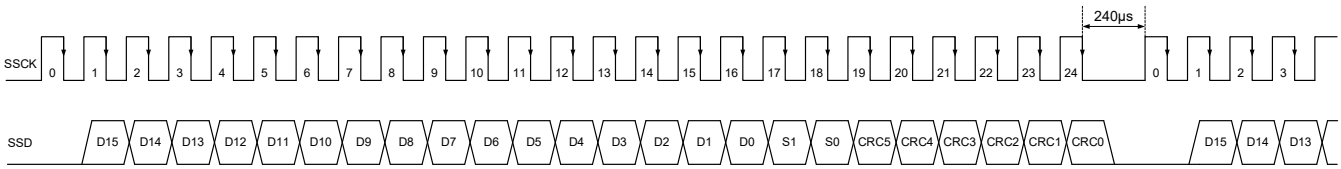


Figure 25. SSI Timing Diagram and Data Structure

Calibration and Compensation

The VCE2755 features enabled-by-default automatic calibration. Upon the first full motor rotation, the system collects relevant parameters and performs continuous background calibration, updating compensation coefficients through a smoothing algorithm. This compensates for temperature-induced variations and drift. To disable this function, contact Technical Support for MTP (Memory through Programming) modification.

For high-precision and off-axis applications, paired-motor calibration provides 32-segment parameters for piecewise compensation, enhancing accuracy by a factor of 3 to 5. This procedure requires guidance from the manufacturer's applications engineering team.

Angle Hysteresis

To prevent angle transient jitter, different levels of angle hysteresis can be selected by configuring register HYST[2:0] to suppress jitter.

Weak-Field Warning

The VCE2755 enables the weak field alarm function by default. When the magnet is moved away or detached, or when the magnetic field is too weak, the register SMF sets the flag. In the VCE2755 TQFN-3×3-16JL package, the MGL pin will be pulled high. In both the VCE2755 SOIC-8 and VCE2755 TQFN-3×3-16JL packages, the weak magnetic field flag (SMF) register changes from 0 to 1. The threshold and enable settings for the weak field alarm can be configured via register WEAK_MAG_LVL[1:0].

Digital Filtering

To suppress signal noise for enhanced accuracy, configurable digital filtering offers four selectable strength levels, programmable via register BANDWIDTH[5:0].

DETAILED DESCRIPTION (continued)

Magnet Installation Requirements

The VCE2755 can be mounted on a fixed plane together with a parallel rotating magnet to measure rotational angle, speed, and direction. It is recommended to use a radially magnetized cylindrical magnet with one pole pair (see Figure 26), with the magnet center aligned to the chip center, corresponding to an on-axis configuration. The AMR sensor only requires a minimum magnetic field strength and has no limitation on the maximum field strength. The closer the magnet is to the chip surface, the higher the magnetic field. For optimal performance, it is recommended to place the chip as close to the magnet as possible. Due to mounting tolerances, a certain offset may exist between the magnet center and the chip center, which will introduce angular measurement errors. This effect is more pronounced for magnets with smaller diameters. Therefore, provided that space permits, it is recommended to use magnets with a larger diameter to minimize angular errors caused by mounting offset.

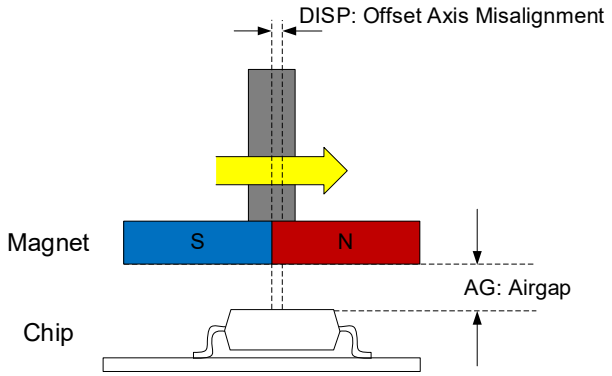


Figure 26. Magnet Installation Diagram

This product uses cylindrical magnets, radial magnetization, with a pair of N/S poles, the parameters are as follows:

Table 4. External Magnetic Field Parameters

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Airgap	Airgap	The distance between the magnet and the chip surface			3	mm
Offset	Offset	The offset between the magnet center and the chip center			0.3	mm
Magnet Diameter	Diameter	1-pole magnet, radial magnetization		10		mm
Magnet Thickness	Thickness			2.5		mm
Working Magnetic	H	Parallel magnetic field between two surfaces of the chip	300			Gauss

REGISTER MAPS

All registers are 8-bit and individual bits are named from D[0] (LSB) to D[7] (MSB).

Address	Name	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	MTP
0x00	Chip Config	Chip ID[7:0]								√
0x03	Data Read (1)	ANGLE[17:10]								×
0x04		ANGLE[9:2]								×
0x05		ANGLE[1:0]		SMF (2)	BTE (3)	CRC[3:0] (1)				×
0x40	User Config0	Reserved		ABZ_INI_DELAY[1:0]		IO_MUX[1:0]		IO_DS	SPI_3W	√
0x41	User Config1	Reserved	PWM_FREQ	Reserved					ABZ_INV	√
0x42	User Config2	Reserved		DIRECTION	Reserved					√
0x43	User Config3	Reserved						ABZ_RES[9:8] (4)		√
0x44		ABZ_RES[7:0] (4)								√
0x46	User Config4	Reserved				ZERO_POS[11:8]				√
0x47		ZERO_POS[7:0]								√
0x48	User Config5	HYST[2:0]			Reserved					√
0x4A	User Config6	Z_WIDTH[2:0]			Reserved					√
0x4C	User Config7	Reserved				UVW_RES[3:0]				√
0x4D	User Config8	WEAK_MAG_LVL[1:0]		BANDWIDTH[5:0]						√

NOTES:

1. CRC0 to CRC3 are 4-bit CRC values, which are the CRC check results for 20-bit data including ANGLE + SMF + BTE. The corresponding CRC generator polynomial is $X^4 + X + 1$, with an initial value of 0000b (binary), and data input/output is not inverted.
2. Weak magnetic field alarm flag (SMF). SMF=1 indicates an alarm, and SMF=0 indicates normal status.
3. Internally defined flag.
4. Pulses per revolution (PPR) = ABZ_RES[9:0] + 1.

REG0x00: Chip Configure Register Address

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	PACKAGE
D[7:0]	Chip ID[7:0]	0x5A	R/W	Indicates the device ID. This register also can be written by an 8-bit data to complete the recognition.	SOIC-8
		0x5B			TQFN-3×3-16JL

REG0x03 to REG0x05: Data Read Register Address

ADDR	BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
0x03	D[7:0]	ANGLE[17:10]	0x00	R	18-bit Angle Data, where 14 bits are valid.
0x04	D[7:0]	ANGLE[9:2]	0x00	R	
0x05	D[7:6]	ANGLE[1:0]	00	R	
	D[5]	SMF	0	R	Low Magnetic Field (SMF) Alarm Flag 0 = Indicates normal operation (default) 1 = Indicates an alarm
	D[4]	BTE	0	R	Internally Defined Flag.
	D[3:0]	CRC[3:0]	0000	R	ANGLE+SMF+BTE 20-bit, Data CRC, CRC generator polynomial = $X^4 + X + 1$, data input/output is not inverted.

REGISTER MAPS (continued)

REG0x40: User Configure0 Register Address

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:6]	Reserved	00	R/W	For internal system use only. User write access is prohibited, otherwise normal system operation may be affected.
D[5:4]	ABZ_INI_DELAY[1:0]	00	R/W	ABZ Power-Up Output Configuration 00 = Standard pulse output during power-up (default) 01 = During power-up, after the Z1 pulse goes from low to high and remains high for 5ms, the AB output provides the absolute angle pulse signal for the initial power-up position 11 = During power-up, after the Z1 pulse goes from low to high and remains high for ms, the AB output provides the absolute angle pulse signal for the initial power-up position
D[3:2]	IO_MUX[1:0]	00	R/W	SOIC-8 Package Multiplexed Mode Configuration 00 = MODE 1 (ABZ/SPI) (default) 01 = MODE 2 (UVW/SPI) 10 = MODE 3 (PWM/SPI) TQFN-3×3-16JL Package Multiplexed Mode Configuration 00 = MODE 1 (ABZ/PWM/SSI/SPI) (default) 01 = MODE 2 (UVW/PWM/SSI/SPI) 10 = MODE 3 (ABZ/UVW/SPI) 11 = MODE 4 (Differential ABZ/SPI)
D[1]	IO_DS	0	R/W	I/O Driver Configuration 0 = 2mA I/O driving capability (default) 1 = 4mA I/O driving capability
D[0]	SPI_3W	0	R/W	TQFN-3×3-16JL Package SPI Interface Configuration 0 = SPI 4-Wire (default) 1 = SPI 3-Wire (The SPI interface of the VCE2755 SOIC-8 package is not configurable and only supports the 3-wire interface.)

REG0x41: User Configure1 Register Address

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	Reserved	0	R/W	For internal system use only. User write access is prohibited, otherwise normal system operation may be affected.
D[6]	PWM_FREQ	0	R/W	PWM Frequency Configuration 0 = 971.1Hz PWM frequency, minimum unit pulse width = 250ns (default) 1 = 485.6Hz PWM frequency, minimum unit pulse width = 500ns
D[5:1]	Reserved	00000	R/W	For internal system use only. User write access is prohibited, otherwise normal system operation may be affected.
D[0]	ABZ_INV	0	R/W	Invert ABZ Polarity 0 = ABZ signal polarity is maintained (default) 1 = ABZ signal polarity inversion

REG0x42: User Configure2 Register Address

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:6]	Reserved	00	R/W	For internal system use only. User write access is prohibited, otherwise normal system operation may be affected.
D[5]	DIRECTION	0	R/W	Rotation Direction Configuration 0 = CW Mode: (default) The magnet rotates clockwise above the chip (B leads A by 1/4 cycle), and the angle increases. The magnet rotates counterclockwise above the chip (B lags A by 1/4 cycle), with decreasing angle. 1 = CCW Mode: The magnet rotates counterclockwise above the chip (B leads A by 1/4 cycle), and the angle increases. The magnet rotates clockwise above the chip (B lags A by 1/4 cycle), with decreasing angle.
D[4:0]	Reserved	00000	R/W	For internal system use only. User write access is prohibited, otherwise normal system operation may be affected.

REGISTER MAPS (continued)

REG0x43 to REG0x44: User Configure3 Register Address

ADDR	BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
0x43	D[7:2]	Reserved	000000	R/W	For internal system use only. User write access is prohibited, otherwise normal system operation may be affected.
	D[1:0]	ABZ_RES[9:8]	00	R/W	10-bit AB Signal Resolution Configuration.
0x44	D[7:0]	ABZ_RES[7:0]	0x00	R/W	

REG0x46 to REG0x47: User Configure4 Register Address

ADDR	BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
0x46	D[7:4]	Reserved	0000	R/W	For internal system use only. User write access is prohibited, otherwise normal system operation may be affected.
	D[3:0]	ZERO_POS[11:8]	0000	R/W	12-bit Angle Data, Internal Raw Angle Offset. Current 18-bit angle output (ANGLE) = internal raw 18-bit angle (filter output) - 18-bit offset angle ANG_OS (high 12 bits correspond to zero position register ZERO_POS[11:0], low 6 bits are padded with zeros).
0x47	D[7:0]	ZERO_POS[7:0]	0x00	R/W	

REG0x48: User Configure5 Register Address

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:5]	HYST[2:0]	000	R/W	Angle Hysteresis Configuration 000 = 0 (default) 001 = 0.011° 010 = 0.022° 011 = 0.044° 100 = 0.066° 101 = 0.088° 110 = 0.132° 111 = 0.176°
D[4:0]	Reserved	00000	R/W	For internal system use only. User write access is prohibited, otherwise normal system operation may be affected.

REG0x4A: User Configure6 Register Address

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:5]	Z_WIDTH[2:0]	000	R/W	ABZ Mode Z Pulse Width Configuration 000 = 1LSB (default) 001 = 2LSB 010 = 4LSB 011 = 8LSB 100 = 12LSB 101 = 16LSB 110 = 180° 111 = 1LSB Z pulse width is configurable in either LSB (Least Significant Bit) or degrees (°).
D[4:0]	Reserved	00000	R/W	For internal system use only. User write access is prohibited, otherwise normal system operation may be affected.

REGISTER MAPS (continued)

REG0x4C: User Configure7 Register Address

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:4]	Reserved	0000	R/W	For internal system use only. User write access is prohibited, otherwise normal system operation may be affected.
D[3:0]	UVW_RES[3:0]	0000	R/W	Pole Pairs of UVW Mode Configuration 0000 = 1 (default) 0001 = 2 0010 = 3 0011 = 4 0100 = 5 0101 = 6 0110 = 7 0111 = 8 1000 = 9 1001 = 10 1010 = 11 1011 = 12 1100 = 13 1101 = 14 1110 = 15 1111 = 16

REG0x4D: User Configure8 Register Address

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:6]	WEAK_MAG_LVL[1:0]	00	R/W	Weak Magnetic Field Alarm Threshold Configuration 00 = 1/8 (default) 01 = 1/2 10 = 1/4 11 = Disable The ratio of the ADC output signal range to the full scale. When the ratio is less than the set threshold, the system outputs a field weakening alarm.
D[5:0]	BANDWIDTH[5:0]	011001	R/W	Digital-Filter Bandwidth Configuration 011001 = BW0 × 8 (default) 100011 = BW0 × 4 101101 = BW0 × 2 110111 = BW0

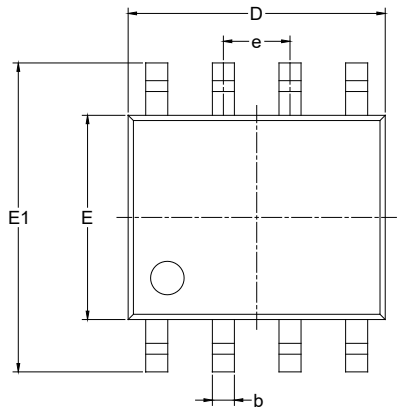
REVISION HISTORY

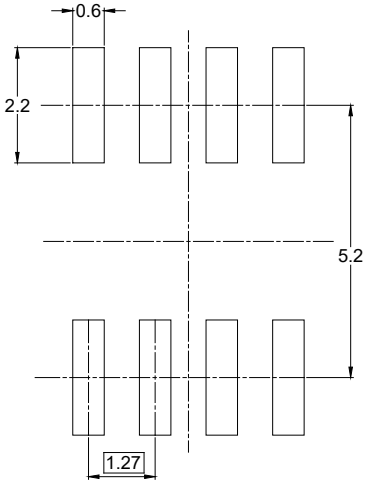
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original to REV.A (AUGUST 2025)	Page
Changed from product preview to production data	All

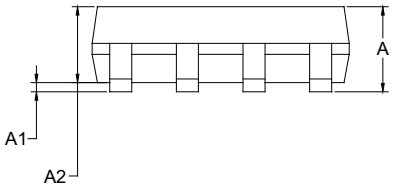
PACKAGE OUTLINE DIMENSIONS

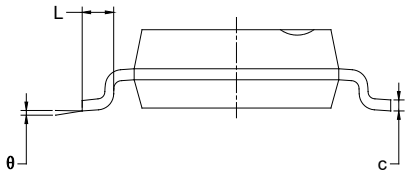
SOIC-8





RECOMMENDED LAND PATTERN (Unit: mm)



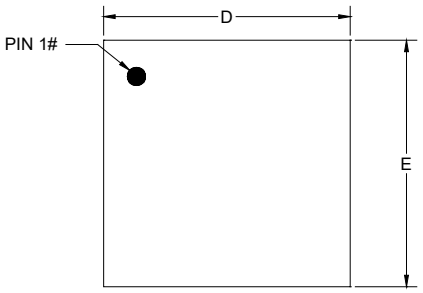


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.27 BSC		0.050 BSC	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

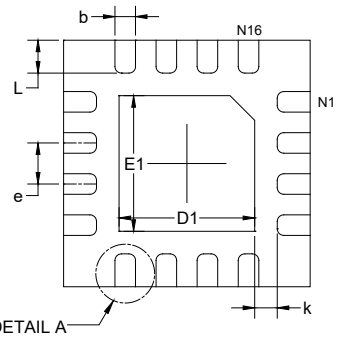
NOTES:
1. Body dimensions do not include mode flash or protrusion.
2. This drawing is subject to change without notice.

PACKAGE OUTLINE DIMENSIONS

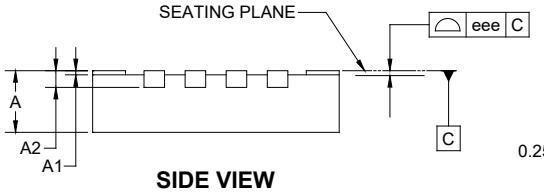
TQFN-3×3-16JL



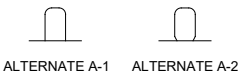
TOP VIEW



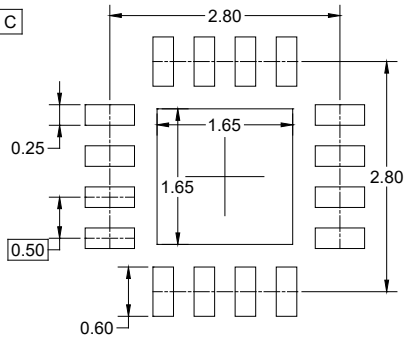
BOTTOM VIEW



SIDE VIEW



DETAIL A
ALTERNATE TERMINAL CONSTRUCTION



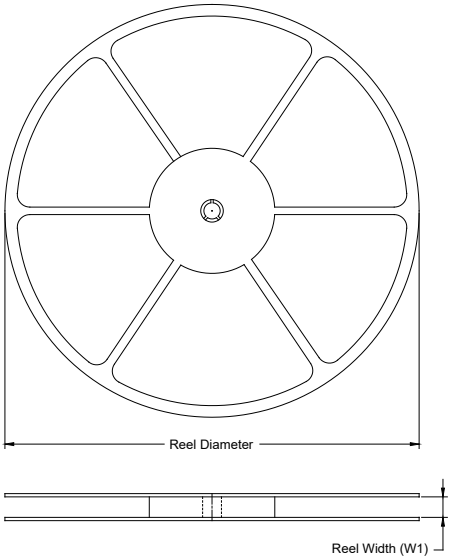
RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	0.700	-	0.800
A1	0.000	-	0.050
A2		0.203 REF	
b	0.200	-	0.300
D	2.900	-	3.100
D1	1.550	-	1.750
E	2.900	-	3.100
E1	1.550	-	1.750
e		0.500 BSC	
k		0.275 REF	
L	0.300	-	0.500
eee		0.080	

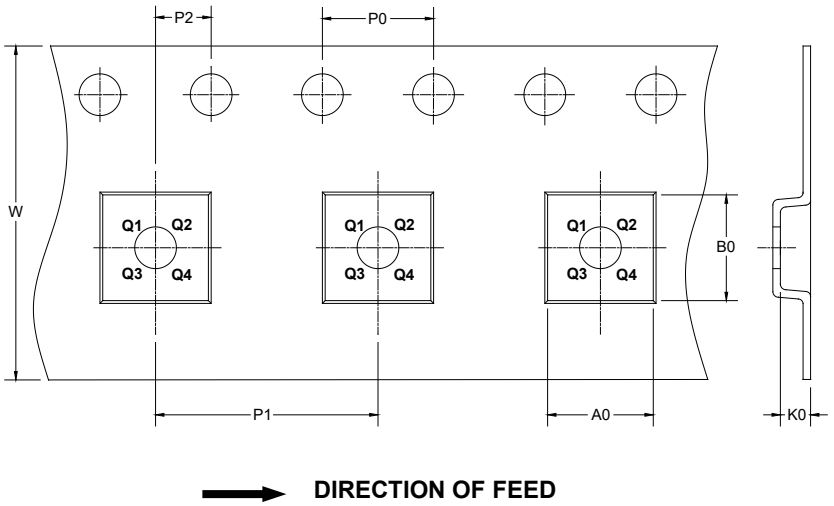
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



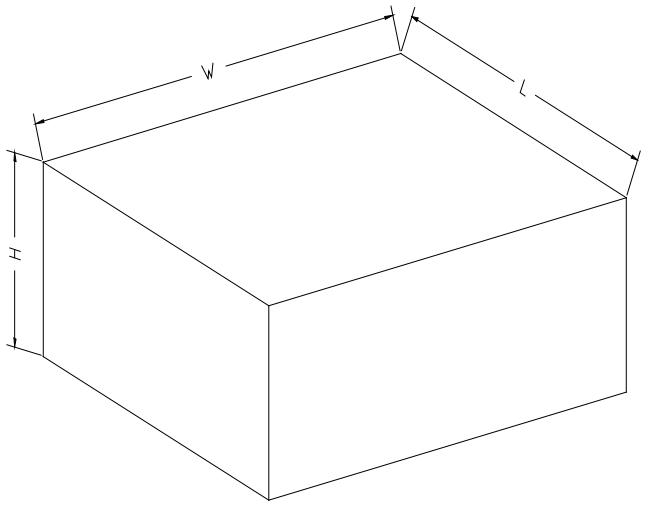
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
SOIC-8	13"	12.4	6.40	5.40	2.10	4.0	8.0	2.0	12.0	Q1
TQFN-3×3-16JL	13"	12.4	3.35	3.35	1.10	4.0	8.0	2.0	12.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002