



# SGM7221A

## USB Type-C Configuration Channel Logic and Port Control with OVP Function

### GENERAL DESCRIPTION

The SGM7221A is a configuration channel (CC) logic and port control device applied in USB Type-C interface with low power, high efficiency and OVP function. The single supply range is from 2.7V to 5.5V. The SGM7221A supports cable orientation detection, attachment detection, PORT detection, current mode detection and  $V_{BUS}$  voltage detection. The SGM7221A is compatible with USB Type-C cable and can be configured as an upstream facing port (UFP), a downstream facing port (DFP) or a dual role port (DRP) based on the Type-C Specification Release 2.1.

The setting of the ADDR pin determines which control mode the SGM7221A supports, GPIO control mode or  $I^2C$  control mode. The SDA (INOUT1), SCL (INOUT2) and INT\_N (OUT3) pins are multiplexed to realize necessary functions in different control modes. The PORT pin can be used to configure this chip as source (SRC), sink (SNK) or dual role port (DRP). The SGM7221A is active low and enters low power mode when the ENB pin is pulled to high.

The SGM7221A is available in a Green UTQFN-1.6×1.6-12L package. It operates over an operating temperature range of -40°C to +125°C.

### FEATURES

- Power Supply Range: 2.7V to 5.5V
- CC1, CC2 and VBUSD Pins Support 25V (MAX) Input Voltage
- Enable Control: Active Low (ENB Pin)
- Low Power Mode Control
- $I^2C$  or GPIO Control
- Role Configuration Control through  $I^2C$
- Mode Configuration
  - ♦ DFP Mode: Source
  - ♦ UFP Mode: Sink
  - ♦ Standard DRP
  - ♦ Try.SRC DRP
  - ♦ Try.SNK DRP
- Support Type-C Specification Release 2.1
- Support 400kHz  $I^2C$  Bus
- Support Default, 1.5A and 3A Current Mode Detect and Control
- $V_{BUS}$  Detection
- -40°C to +125°C Operating Temperature Range
- Available in a Green UTQFN-1.6×1.6-12L Package

### APPLICATIONS

USB Type-C Interface Detection Applications  
Consumer Electronics  
Smart Phones  
Laptops  
Xpads

**PACKAGE/ORDERING INFORMATION**

| MODEL    | PACKAGE DESCRIPTION | SPECIFIED TEMPERATURE RANGE | ORDERING NUMBER    | PACKAGE MARKING | PACKING OPTION      |
|----------|---------------------|-----------------------------|--------------------|-----------------|---------------------|
| SGM7221A | UTQFN-1.6×1.6-12L   | -40°C to +125°C             | SGM7221AXUQT12G/TR | 240<br>XXX      | Tape and Reel, 3000 |

**MARKING INFORMATION**

NOTE: XXX = Date Code and Trace Code.

**Y Y Y** — Serial Number  
**X X X**  

Trace Code  
Date Code - Year

Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

**ABSOLUTE MAXIMUM RATINGS**

Supply Voltage Range,  $V_{DD}$  ..... -0.3V to 6V  
ADDR, ID, ENB, INT\_N/OUT3 Pins ..... -0.3V to 6V  
SDA/INOUT1, SCL/INOUT2 Pins ..... -0.3V to 6V  
CC1, CC2, VBUS Pins ..... -0.3V to 25V  
Package Thermal Resistance  
UTQFN-1.6×1.6-12L,  $\theta_{JA}$  ..... 124.4°C/W  
UTQFN-1.6×1.6-12L,  $\theta_{JB}$  ..... 32.7°C/W  
UTQFN-1.6×1.6-12L,  $\theta_{JC}$  ..... 79.9°C/W  
Junction Temperature ..... +150°C  
Storage Temperature Range ..... -65°C to +150°C  
Lead Temperature (Soldering, 10s) ..... +260°C  
ESD Susceptibility <sup>(1) (2)</sup>  
HBM ..... ±3000V  
CDM ..... ±1000V

**NOTES:**

- For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.
- For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

**RECOMMENDED OPERATING CONDITIONS**

Supply Voltage Range,  $V_{DD}$  ..... 2.7V to 5.5V  
Operating Junction Temperature Range ..... -40°C to +125°C

**OVERSTRESS CAUTION**

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

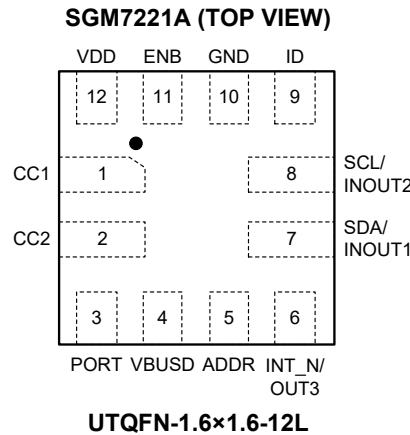
**ESD SENSITIVITY CAUTION**

This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

**DISCLAIMER**

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

## PIN CONFIGURATION



## PIN DESCRIPTION

| PIN | NAME           | TYPE | FUNCTION                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |                                                                                                                                                                                                                                   |
|-----|----------------|------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1   | CC1            | I/O  | Type-C CC Logic Signal Channel 1 with Over-Voltage Protection (OVP) Function.                                                                                                                                                                                                                                                                                                                                                                                                        |                                                                                                                                                                                                                                   |
| 2   | CC2            | I/O  | Type-C CC Logic Signal Channel 2 with Over-Voltage Protection (OVP) Function.                                                                                                                                                                                                                                                                                                                                                                                                        |                                                                                                                                                                                                                                   |
| 3   | PORT           | AI   | Tri-State Input Signal Configuring the PORT of Device.<br>Floating = DRP (suggest to connect a 4.7nF capacitor from the PORT pin to GND).<br>H = DFP (suggest to be pulled up to VDD directly).<br>L = UFP (suggest to be pulled down to GND directly).                                                                                                                                                                                                                              |                                                                                                                                                                                                                                   |
| 4   | VBUSD          | AI   | Detecting whether there is a Power Connection.                                                                                                                                                                                                                                                                                                                                                                                                                                       |                                                                                                                                                                                                                                   |
| 5   | ADDR           | AI   | Tri-state input signal determines which control mode the SGM7221A supports, GPIO control mode or I <sup>2</sup> C control mode.<br>Floating = GPIO control mode (suggest to connect a 4.7nF capacitor from the ADDR pin to GND).<br>H = I <sup>2</sup> C, 7-bit address is 0x67 (suggest to be pulled up to VDD directly).<br>L = I <sup>2</sup> C, 7-bit address is 0x47 (suggest to be pulled down to GND directly).                                                               |                                                                                                                                                                                                                                   |
| 6   | INT_N/<br>OUT3 | DO   | INT_N: this pin could indicate the changes of I <sup>2</sup> C register status in I <sup>2</sup> C control mode.<br>H = No detection. L = indicating the changes of I <sup>2</sup> C registers status.                                                                                                                                                                                                                                                                               |                                                                                                                                                                                                                                   |
|     |                |      | OUT3: Acting as audio accessory detection.<br>H = No detection. L = The audio accessory connection.                                                                                                                                                                                                                                                                                                                                                                                  |                                                                                                                                                                                                                                   |
| 7   | SDA/<br>INOUT1 | I/O  | SDA and INOUT1 Dual-Function Pin. This pin only supports open-drain output. If the ADDR pin is pulled to high or low, the SGM7221A would be configured as I <sup>2</sup> C control mode and this pin is used as I <sup>2</sup> C data input/output. If the ADDR pin is keeping floating, the SGM7221A would be configured as GPIO control mode. In GPIO control mode, the Type-C current mode is detected according to the INOUT1 and INOUT2 level when the SGM7221A is in UFP mode. | INOUT2 and INOUT1 in GPIO Control mode indications:<br>H H = Unattached state, default current<br>H L = Attached state, medium current (1.5A)<br>L H = Attached state, default current<br>L L = Attached state, high current (3A) |
| 8   | SCL/<br>INOUT2 | I/O  | SCL and INOUT2 Dual-Function Pin. This pin only supports open-drain output. If the ADDR pin is pulled to high or low, the SGM7221A would be configured as I <sup>2</sup> C control mode and this pin is used as I <sup>2</sup> C clock Input. If the ADDR pin is keeping floating, the SGM7221A would be configured as GPIO control mode. In GPIO control mode, the Type-C current mode is detected according to the INOUT1 and INOUT2 level when the SGM7221A is in UFP mode.       |                                                                                                                                                                                                                                   |
| 9   | ID             | AO   | Open-Drain Output Pin. When detecting device attachment, this pin is pulled to low when port is a Source (DFP) or dual PORT (DRP) acting as source (DFP).                                                                                                                                                                                                                                                                                                                            |                                                                                                                                                                                                                                   |
| 10  | GND            | G    | Ground.                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |                                                                                                                                                                                                                                   |
| 11  | ENB            | AI   | Enable Input Pin. It is pulled up to VDD internally.<br>H = The SGM7221A is disabled by default. L = Active                                                                                                                                                                                                                                                                                                                                                                          |                                                                                                                                                                                                                                   |
| 12  | VDD            | P    | Power Supply Pin.                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |                                                                                                                                                                                                                                   |

NOTE: AI = analog input, AO = analog output, DO = digital output, I/O = input/output, P = power, G = ground.

## FUNCTIONAL BLOCK DIAGRAM

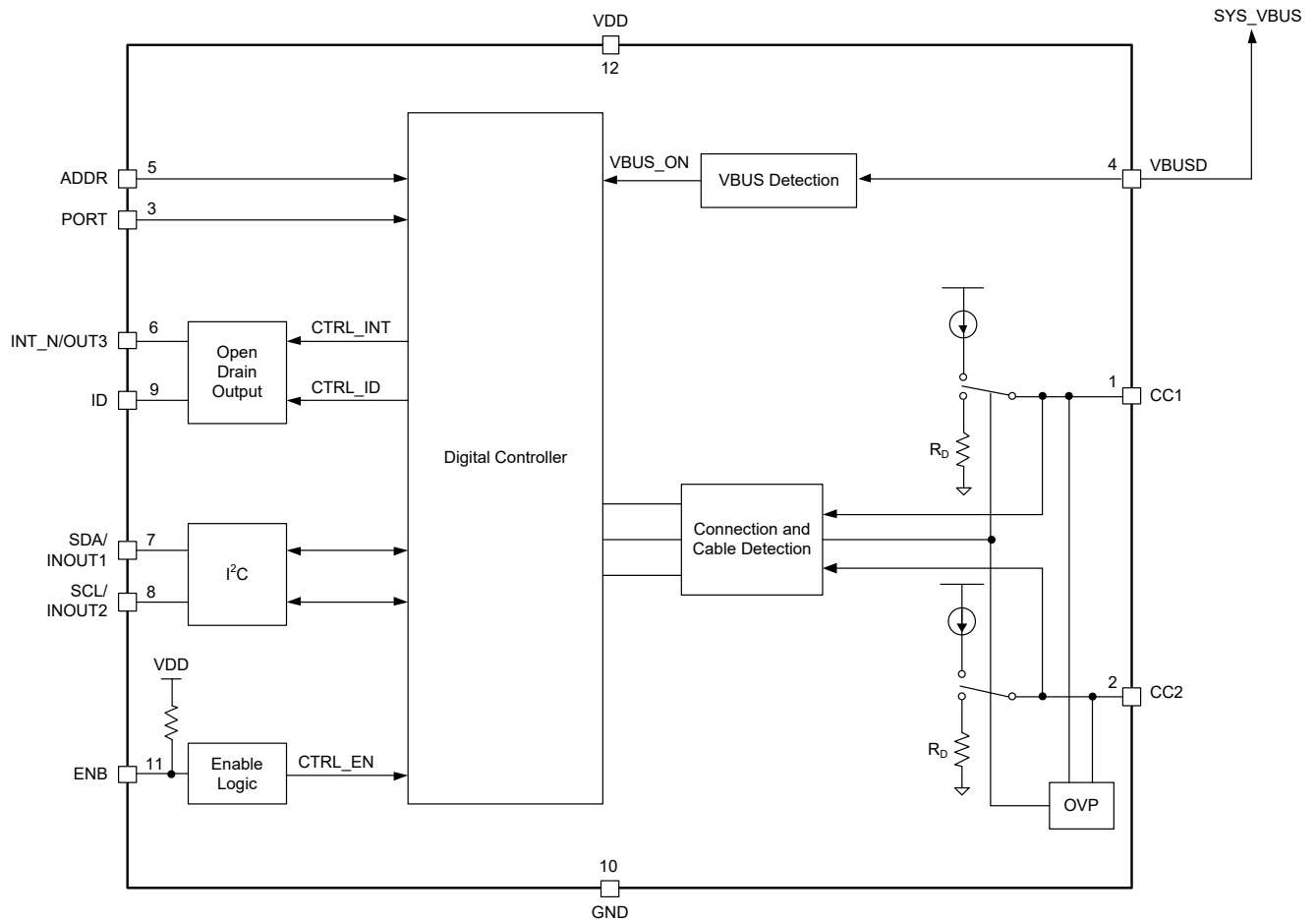
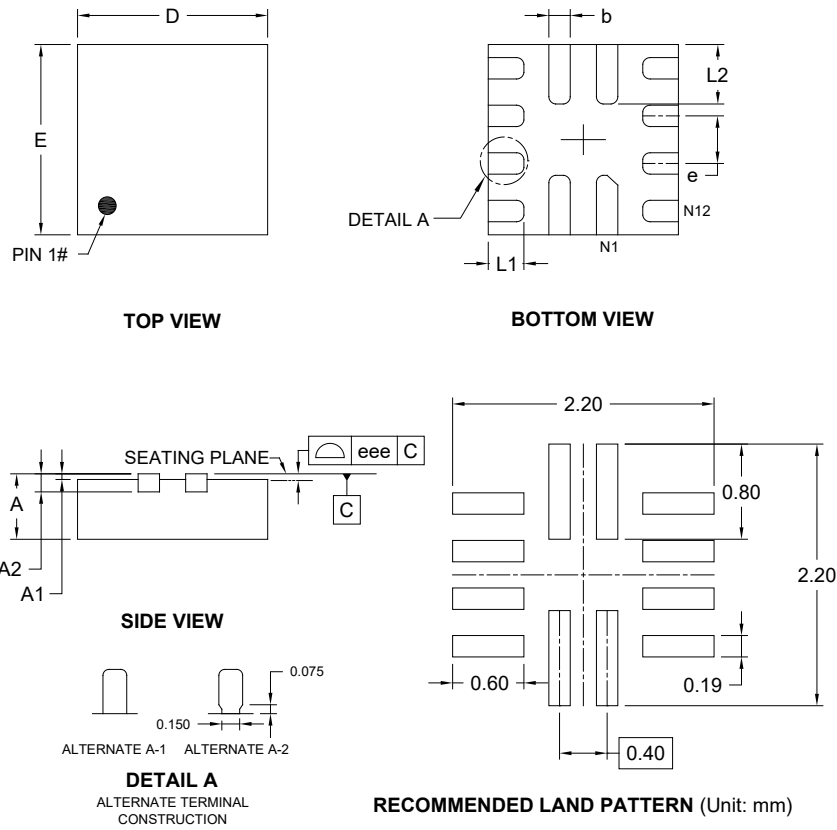


Figure 1. Block Diagram

## PACKAGE OUTLINE DIMENSIONS

### UTQFN-1.6×1.6-12L

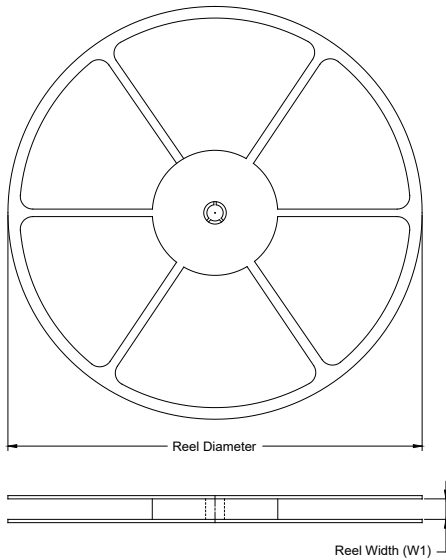


| Symbol | Dimensions In Millimeters |       |       |
|--------|---------------------------|-------|-------|
|        | MIN                       | NOM   | MAX   |
| A      | 0.450                     | -     | 0.600 |
| A1     | -                         | -     | 0.050 |
| A2     | 0.152 REF                 |       |       |
| e      | 0.400 BSC                 |       |       |
| D      | 1.550                     | 1.600 | 1.650 |
| E      | 1.550                     | 1.600 | 1.650 |
| b      | 0.130                     | 0.190 | 0.250 |
| L1     | 0.250                     | 0.300 | 0.350 |
| L2     | 0.450                     | 0.500 | 0.550 |
| eee    | -                         | 0.080 | -     |

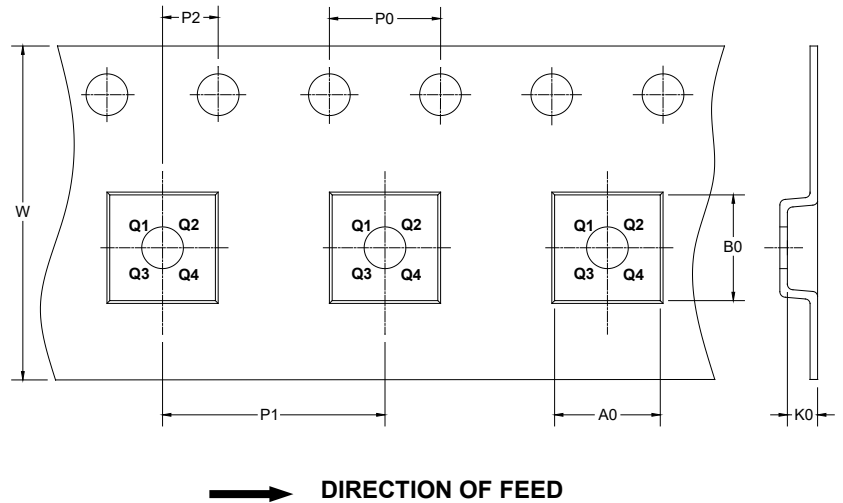
NOTE: This drawing is subject to change without notice.

## TAPE AND REEL INFORMATION

### REEL DIMENSIONS



### TAPE DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

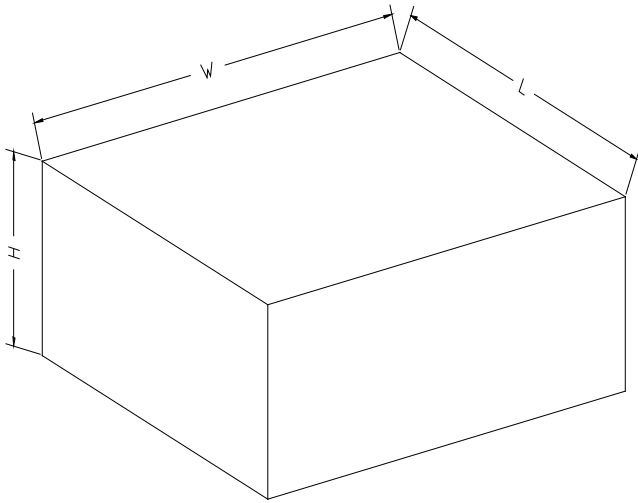
### KEY PARAMETER LIST OF TAPE AND REEL

| Package Type      | Reel Diameter | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P0 (mm) | P1 (mm) | P2 (mm) | W (mm) | Pin1 Quadrant |
|-------------------|---------------|--------------------|---------|---------|---------|---------|---------|---------|--------|---------------|
| UTQFN-1.6×1.6-12L | 7"            | 9.0                | 1.78    | 1.78    | 0.69    | 4.0     | 4.0     | 2.0     | 8.0    | Q2            |

DD0001

## PACKAGE INFORMATION

### CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

### KEY PARAMETER LIST OF CARTON BOX

| Reel Type   | Length (mm) | Width (mm) | Height (mm) | Pizza/Carton |
|-------------|-------------|------------|-------------|--------------|
| 7" (Option) | 368         | 227        | 224         | 8            |
| 7"          | 442         | 410        | 224         | 18           |

DD0002