SGM611A13
16V/12A, Synchronous Buck Converter with Adjustable Current Limit, Selectable Frequency, and Voltage Tracking

GENERAL DESCRIPTION

The SGM611A13 is a high-efficiency high-frequency synchronous Buck DC/DC converter with a wide input voltage range of 4.5V to 16V and a wide output current range, optimized for compact solutions. With an internally compensated constant on-time (COT) control mode architecture, ultra-fast dynamic response is achieved, and loop stabilization is guaranteed with ease.

The switching frequency of the converter can be set to 600kHz, 800kHz or 1000kHz with a MODE pin, which allows the converter frequency to stay at a fixed value independent of the input and output voltages.

The SGM611A13 has voltage tracking capability in which output voltage can track the voltage applied at the TRK/REF pin. A ceramic capacitor, which determines the soft-start time, should be placed as close to TRK/REF pin as possible.

The power-good (PGOOD pin) is an open-drain output that is provided to signal the status of the output voltage to the downstream system. When the input supply is unable to power the device, the V_{PG} can be clamped low by itself with external pull-up resistor.

The device integrates various protection features such as over-voltage protection, over-current protection, input under-voltage lockout and thermal shutdown. In addition, the synchronous rectifier supports short circuit protection which further improves the robustness of the device.

The SGM611A13 is available in a Green TQFN-3×4-21L package.

APPLICATIONS

Sever, Computing, Storage
Telecom, Base Stations
SSD
Optical Module
General Purpose Point-of-Load

FEATURES

- **Adaptive COT (Constant On-Time) for Ultra-Fast Transient Response**
- **Wide Input Voltage Range:4.5V to 16V**
- **Wide Output Adjustable Voltage Range: 0.6V to (90% × V_{IN}) with an Upper Limit of 5.5V**
- **Selectable Switching Frequency: 600kHz, 800kHz and 1000kHz**
- **Remote Differential Sense of Output Voltage**
- **Adjustable Current Limit Level**
- **Output Current: 12A**
- **Integrated Low R_{DSON} Power FETs**
- **Stable with Low-ESR Output Capacitor**
- **1% Reference Voltage at T_J = 0℃ to +85℃**
- **1.5% Reference Voltage at T_J = -40℃ to +125℃**
- **Programmable Pulse Saving Operation or Forced CCM**
- **Outstanding Load Regulation**
- **Power Good Open-Drain Output**
- **Output Voltage Tracking Capability**
- **Output Discharge Function**
- **Adjustable Soft-Start Time from 0.91ms Timer**
- **Safe Pre-Bias Startup Capability**
- **Available in a Green TQFN-3×4-21L Package**

TYPICAL APPLICATION

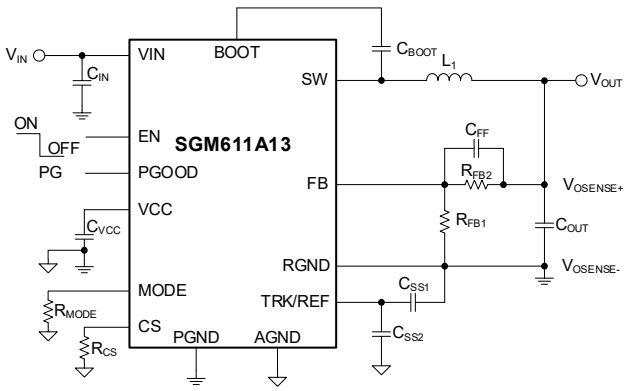


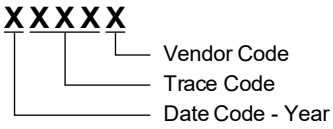
Figure 1. Typical Application Circuit

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM611A13	TQFN-3×4-21L	-40℃ to +125℃	SGM611A13XTWD21G/TR	SGM 15GTWD XXXXX	Tape and Reel, 4000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage Range, V_{IN} ..... -0.3V to 18V
SW Voltage (DC) ..... -0.3V to V_{IN} + 0.3V
SW Voltage (25ns) (1) ..... -3V to 25V
BOOT Voltage ..... V_{SW} + 6V
EN, VCC Voltages ..... -0.3V to 6V
Other Pins ..... -0.3V to 6V
Package Thermal Resistance
TQFN-3×4-21L, θ_{JA} ..... 44.7℃/W
TQFN-3×4-21L, θ_{JB} ..... 3.4℃/W
TQFN-3×4-21L, θ_{JC} ..... 28.6℃/W
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility (2) (3)
HBM ..... ±3000V
CDM ..... ±1000V

NOTES:

1. When the input voltage is 16V, the rated voltage is in the range of -3V to 25V for a period shorter than 25ns, and the maximum repetition frequency is 1000kHz.

2. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.

3. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

RECOMMENDED OPERATING CONDITIONS

Supply Voltage Range, V_{IN} ..... 4.5V to 16V
Output Voltage Range, V_{OUT} ..... 0.6V to 5.5V
Maximum Output Current, I_{OUT_MAX} 12A
Maximum Output Current Limit, I_{OC_MAX} 16A
Operating Junction Temperature (T_J) ..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

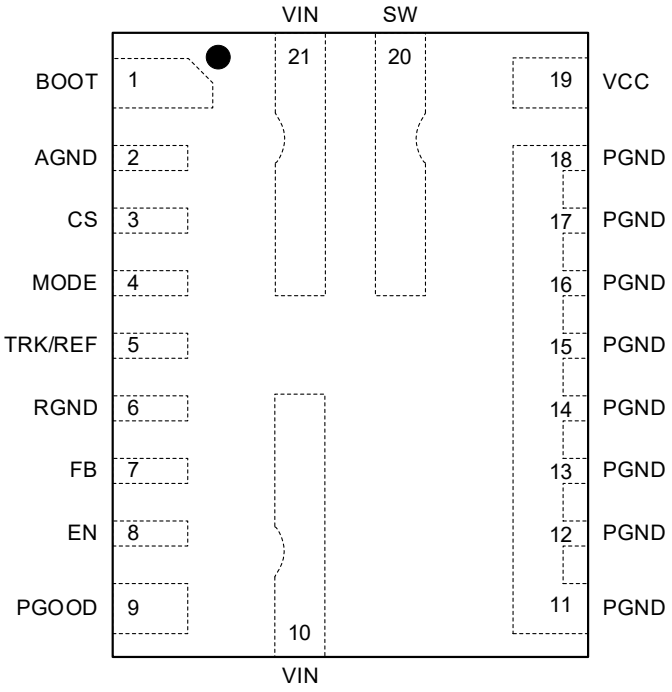
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

(TOP VIEW)



TQFN-3×4-21L

PIN DESCRIPTION

PIN	NAME	FUNCTION
1	BOOT	Bootstrap Supply for the High-side Gate Driver. A bootstrap capacitor should be connected between SW and BOOT pins.
2	AGND	Analog Ground. Select AGND as the internal circuit reference point of the analog circuits.
3	CS	Current Limit Adjust and Current Sense Comparator Input. A current sourced from the CS pin through an external resistor programs the threshold voltage for valley current limiting.
4	MODE	Mode Selection. 1: CCM. 2: Pulse Saving Mode. 3: Operating Switching Frequency.
5	TRK/REF	Soft-Start and External Voltage-Tracking Pin Input. A ceramic capacitor should be placed as close to TRK/REF pin as possible. The X5R and X7R type capacitors should be the primary choices due to their stability.
6	RGND	Negative Input of Remote Sense Differential Amplifier. This pin serves as the negative input (RGND) of the remote sense differential amplifier.
7	FB	Feedback. A resistor divider from the output to FB to RGND sets the output voltage level.
8	EN	Active High Device Enable Input. Do not leave EN floating.
9	PGOOD	Open-Drain Power-Good Output. A pull-up resistor is needed if this feature is used.
10, 21	VIN	Supply Input of the Device. Connect a low ESR ceramic capacitor from this pin to PGND.
11-18	PGND	System Ground. PGND pin provides the reference ground for the regulated output voltage.
19	VCC	Internal LDO Output. Decouple with a ceramic capacitor as close to VCC pin as possible. The X5R and X7R type capacitors should be the primary choices due to their stability.
20	SW	Switching Node Pin. SW is tied to the VIN voltage during the on-time of the PWM duty cycle. SW is driven low during the off-time. Use wide PCB traces to connect to the bootstrap capacitor and inductor.

ELECTRICAL CHARACTERISTICS

(V_{IN} = 12V, T_A = -40℃ to +125℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current						
Shutdown Current	I_{SD}	V_{EN} = 0V		3	10	μA
Quiescent Current	I_Q	V_{EN} = 2V, V_{FB} = 0.62V		440	750	μA
Power MOSFETs						
High-side Leakage Current	I_{LKG_HS}	V_{EN} = 0V, V_{SW} = 0V		0	10	μA
Low-side Leakage Current	I_{LKG_LS}	V_{EN} = 0V, V_{SW} = 12V		3	30	
High-side On-State Resistance	$R_{DS\_ON\_HS}$			10.8		mΩ
Low-side On-State Resistance	$R_{DS\_ON\_LS}$			4.4		mΩ
Current Limit						
Current Limit Threshold Voltage	V_{CL}		0.21	0.24	0.27	V
I_{CS} to I_{OUT} Ratio	I_{CS}/I_{OUT}	I_{OUT} ≥ 2A		5		μA/A
Low-side Negative Current Limit	I_{LIM_NEG}			-10		A
Switching Frequency						
Switching Frequency (1)	f_{SW}	R_{MODE} = 30.1kΩ, I_{OUT} = 6A, V_{OUT} = 3.3V	720	800	880	kHz
Minimum On-Time (2)	t_{ON_MIN}	V_{FB} = 500mV		60		ns
Minimum Off-Time (2)	t_{OFF_MIN}	V_{FB} = 500mV		140		ns
Over-Voltage and Under-Voltage Protection						
Over-Voltage Threshold	V_{OVP}		111%	117%	122%	V_{REF}
Under-Voltage Threshold	V_{UVP}		76%	81%	85%	V_{REF}
Feedback Voltage and Soft-Start						
Feedback Voltage	V_{REF}	T_A = -40℃ to +125℃	591	600	609	mV
		T_A = 0℃ to +85℃	594	600	606	mV
TRK/REF Pin Sourcing Current	I_{TRACK_Source}	$V_{TRK/REF}$ = 0V		48		μA
TRK/REF Pin Sinking Current	I_{TRACK_Sink}	$V_{TRK/REF}$ = 1V		13		μA
Soft-Start Time	t_{SS}	C_{TRACK} = 1nF, T_A = +25℃	0.40	0.91	1.40	ms
		C_{TRACK} = 1nF	0.37	0.91	1.44	
Error Amplifier						
Error Amplifier Offset	V_{OS}		-10	0	10	mV
Feedback Current	I_{FB}	V_{FB} = V_{REF}		50	150	nA
Enable and UVLO						
Enable Input Rising Threshold	$V_{IH\text{-}EN}$		1.167	1.22	1.273	V
Enable Hysteresis	$V_{EN\text{-}HYS}$			200		mV
Enable Input Current	I_{EN}	V_{EN} = 2V		0		μA
Discharge FET	R_{ON_DISCH}	V_{SW} = 5V		85	150	Ω

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 12V, T_A = -40℃ to +125℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
VIN UVLO						
VIN Under-Voltage Lockout Threshold Rising	$V_{IN\ UVLO\_R}$	V_{CC} = 3.3V	3.7	4.1	4.5	V
VIN Under-Voltage Lockout Threshold Falling	$V_{IN\ UVLO\_F}$	V_{CC} = 3.3V	3.21	3.44	3.67	V
VCC Regulator						
VCC Under-Voltage Lockout Threshold Rising	$V_{CC\ UVLO\_R}$		4.07	4.24	4.41	V
VCC Under-Voltage Lockout Threshold Falling	$V_{CC\ UVLO\_F}$		3.38	3.68	3.98	V
VCC Regulator	V_{CC}		4.57	4.77	4.97	V
VCC Load Regulation		I_{CC} = 25mA		0.2		%
Power Good						
Power Good High Threshold	$V_{PG\ HIGH\_R}$	FB from low to high	87.5%	93.5%	98.5%	V_{REF}
Power Good Low Threshold	$V_{PG\ LOW\_R}$	FB from low to high	111%	117%	122%	V_{REF}
	$V_{PG\ LOW\_F}$	FB from high to low	76%	81%	85%	
Power Good Low to High Delay	t_{PG}	T_A = +25℃	0.68	1.14	1.6	ms
			0.65	1.14	1.63	
Power Good Sink Current Capability	V_{PG}	I_{PG} = 1mA			0.2	V
Power Good Leakage Current	I_{PG_LEAK}	V_{PG} = 3.3V			1	μA
Power Good Low-Level Output Voltage	V_{OL_100}	V_{IN} = 0V, Pull PGOOD up to 3.3V through a 100kΩ resistor		630	880	mV
	V_{OL_10}	V_{IN} = 0V, Pull PGOOD up to 3.3V through a 10kΩ resistor		830	1080	
Thermal Protection						
Thermal Shutdown (2)	T_{SD}			160		℃
Thermal Shutdown Hysteresis (2)	T_{SD_HYS}			30		℃

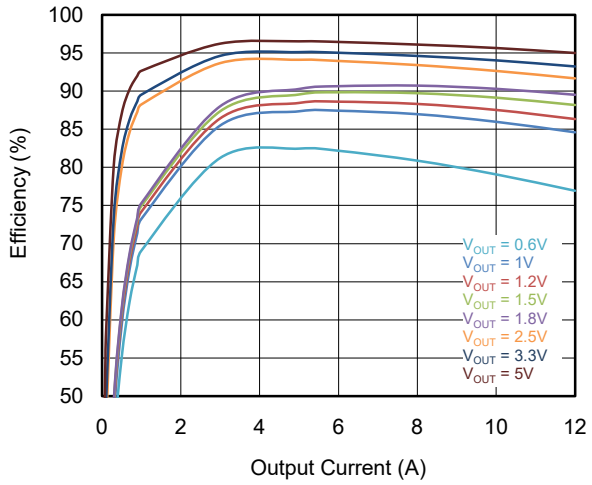
NOTES:

1. Guaranteed by design over temperature.
2. Guaranteed by design, not tested.

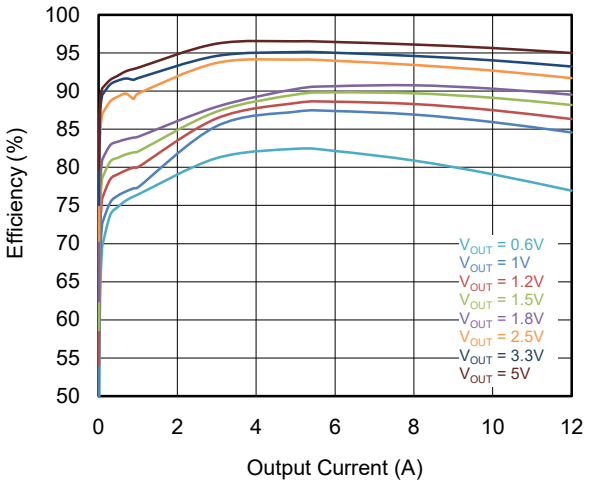
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = +25℃, V_{IN} = 12V, V_{OUT} = 1.2V, f_{SW} = 800kHz, unless otherwise noted.

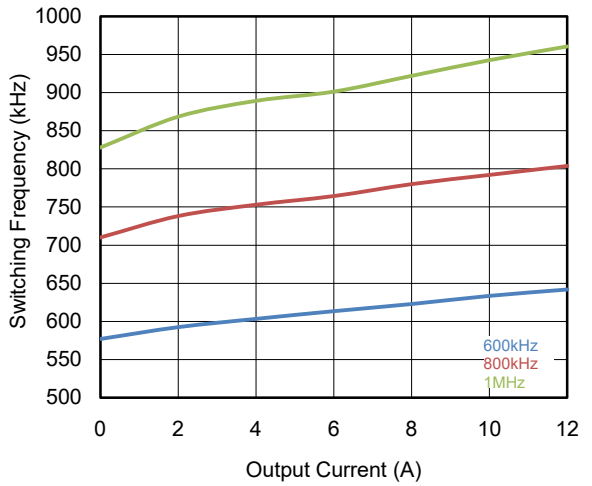
Efficiency vs. Output Current (FCCM)



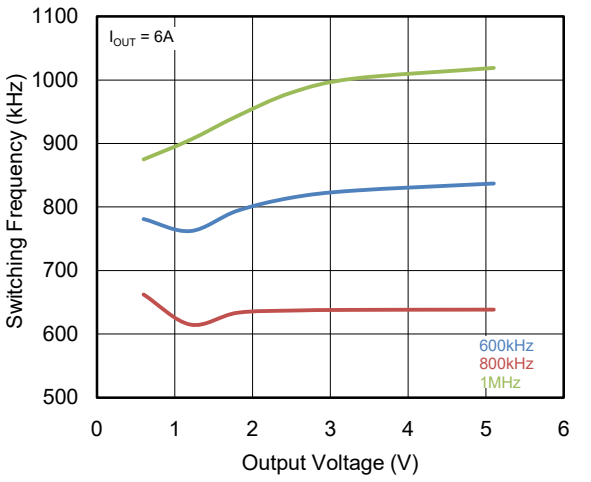
Efficiency vs. Output Current (PSM)



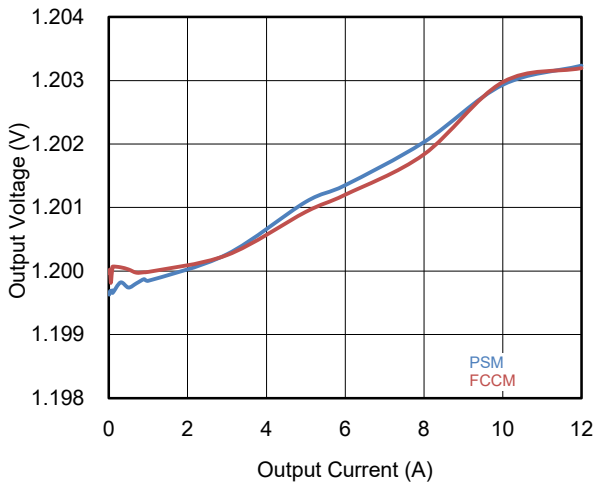
Switching Efficiency vs. Output Current (FCCM)



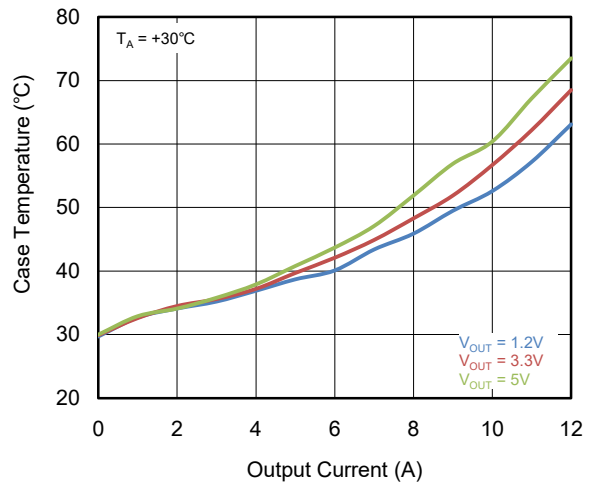
Switching Efficiency vs. Output Voltage



Load Regulation



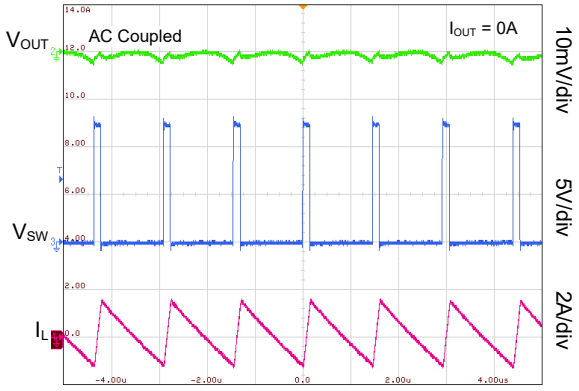
Thermal Results



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

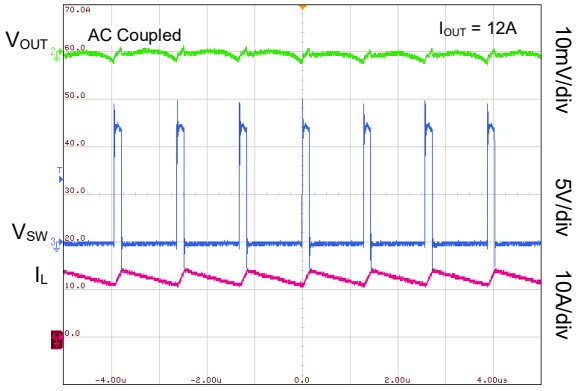
T_A = +25℃, V_{IN} = 12V, V_{OUT} = 1.2V, f_{SW} = 800kHz, unless otherwise noted.

Switching Waveform at No Load (FCCM)



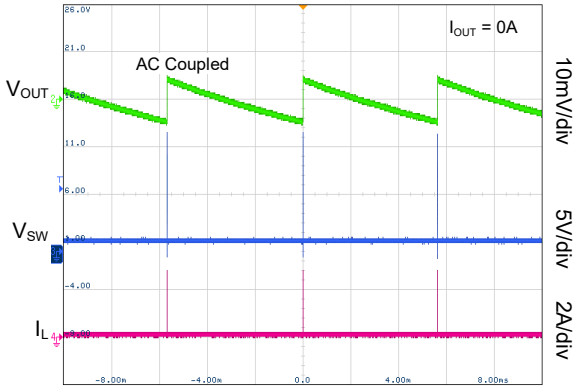
Time (1μs/div)

Switching Waveform at Heavy Load (FCCM)



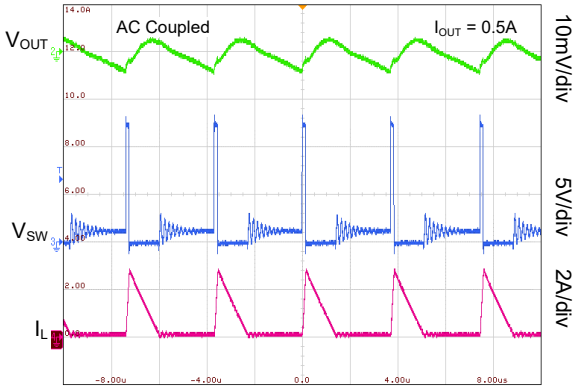
Time (1μs/div)

Switching Waveform at No Load (PSM)



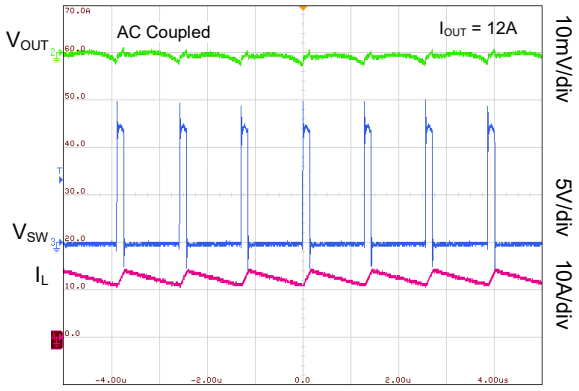
Time (2ms/div)

Switching Waveform at Light Load (PSM)



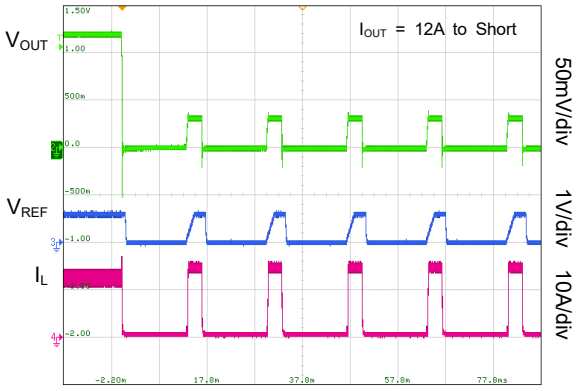
Time (2μs/div)

Switching Waveform at Heavy Load (PSM)



Time (1μs/div)

Over-Current Protection Entry

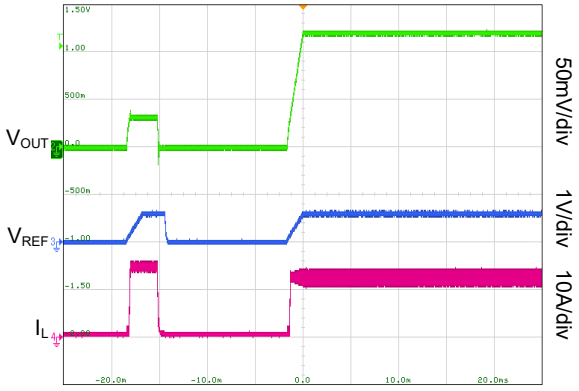


Time (10ms/div)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

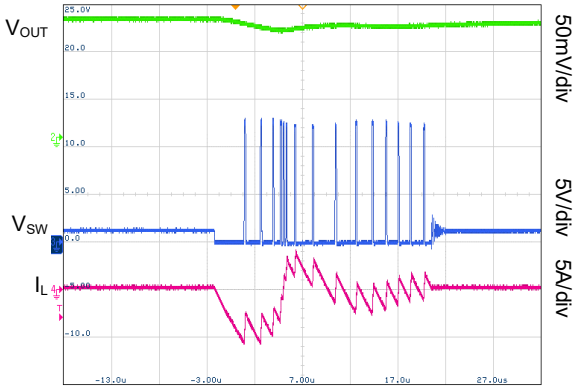
T_A = +25℃, V_{IN} = 12V, V_{OUT} = 1.2V, f_{SW} = 800kHz, unless otherwise noted.

Over-Current Protection Recovery



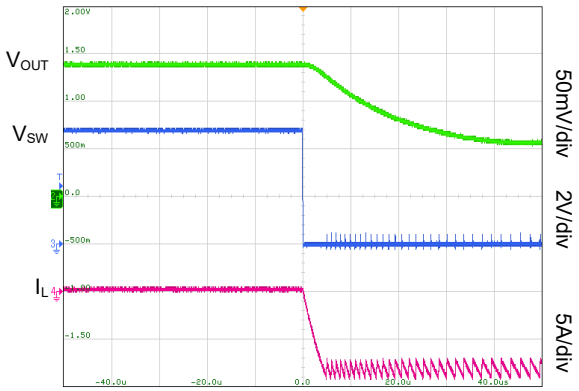
Time (5ms/div)

Output Sinking Mode Operation



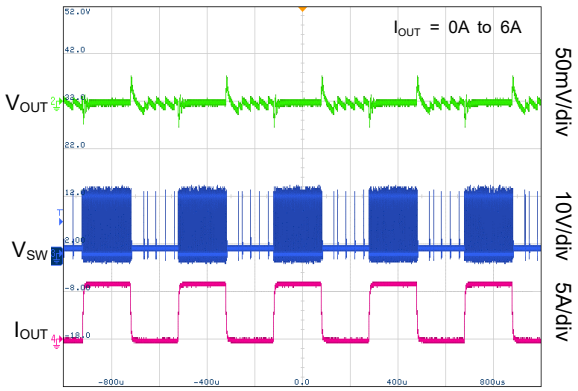
Time (5μs/div)

Over-Voltage Protection (PSM)



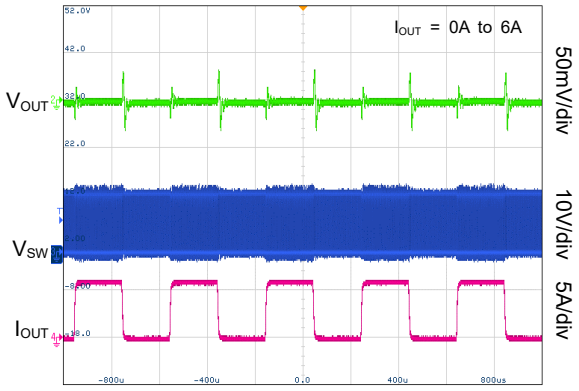
Time (10μs/div)

Load Transient (PSM)



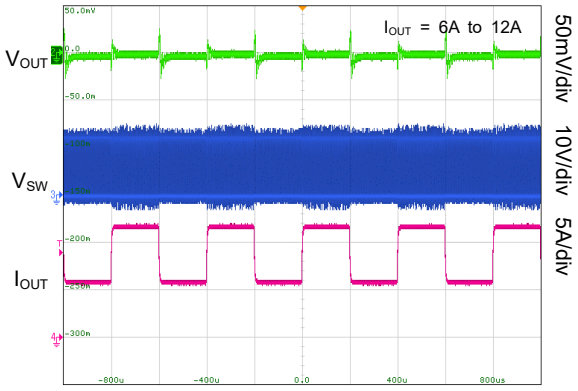
Time (20μs/div)

Load Transient (FCCM)



Time (20μs/div)

Load Transient (PSM)

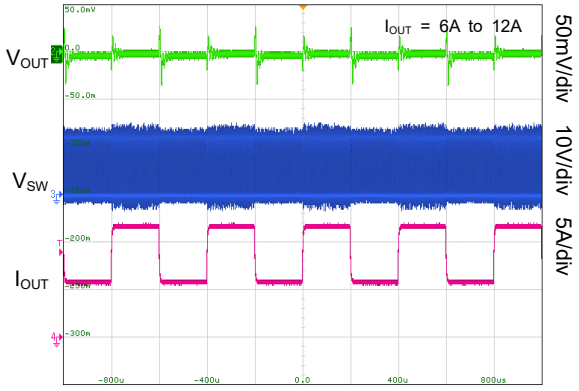


Time (200μs/div)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

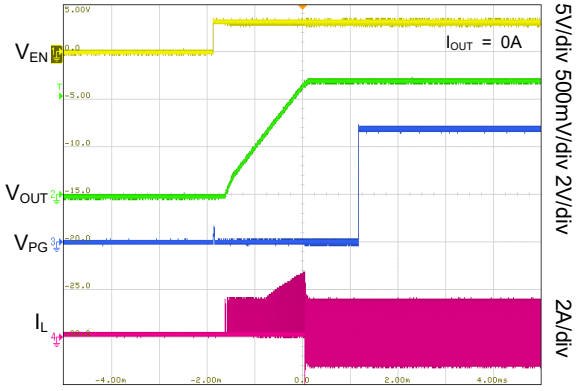
T_A = +25℃, V_{IN} = 12V, V_{OUT} = 1.2V, f_{SW} = 800kHz, unless otherwise noted.

Load Transient (FCCM)



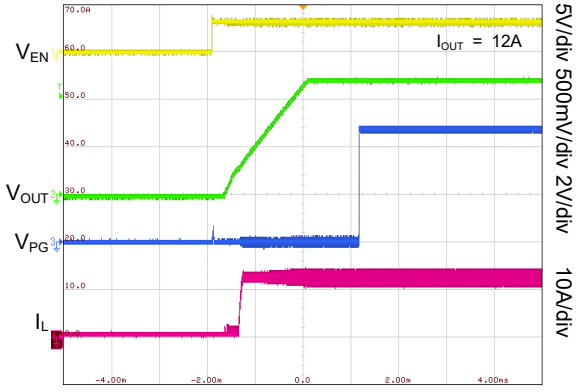
Time (200μs/div)

Startup by EN (FCCM)



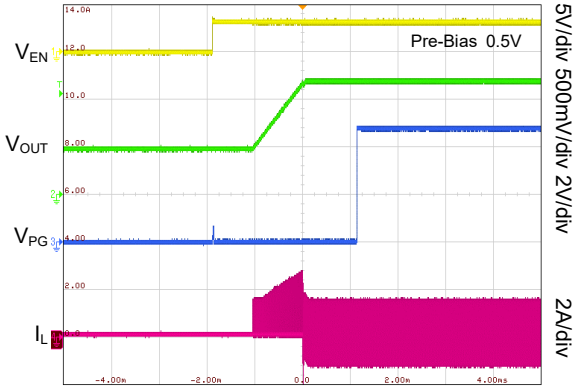
Time (1ms/div)

Startup by EN (FCCM)



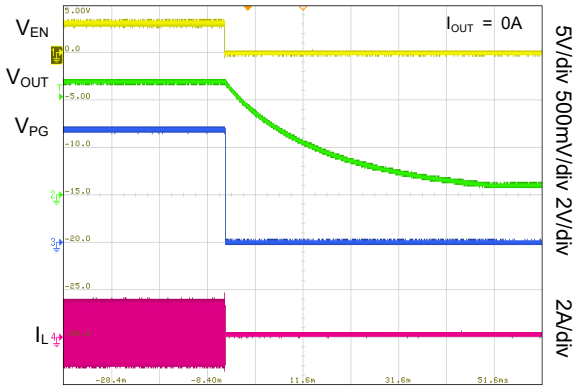
Time (1ms/div)

Startup by EN Pre-Bias (FCCM)



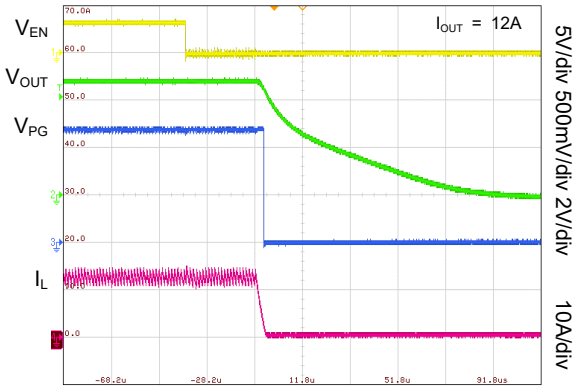
Time (1ms/div)

Shutdown by EN (FCCM)



Time (10ms/div)

Shutdown by EN (FCCM)

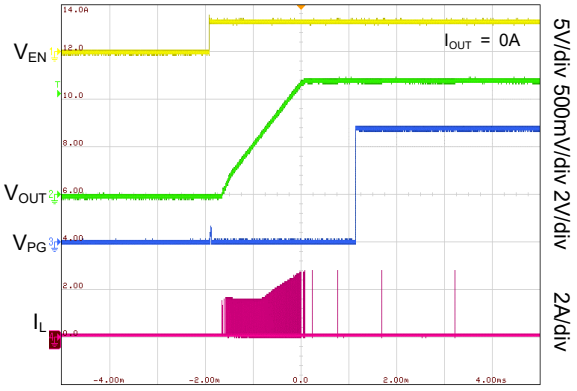


Time (20μs/div)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

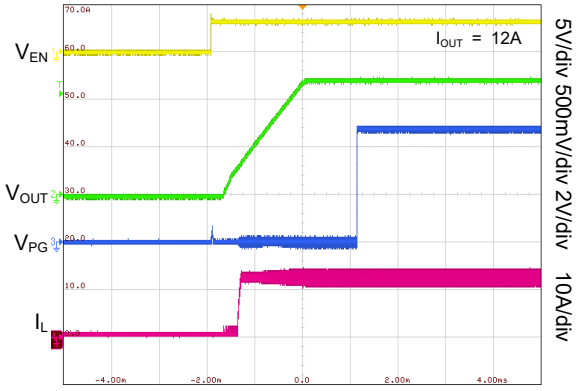
T_A = +25℃, V_{IN} = 12V, V_{OUT} = 1.2V, f_{SW} = 800kHz, unless otherwise noted.

Startup by EN (PSM)



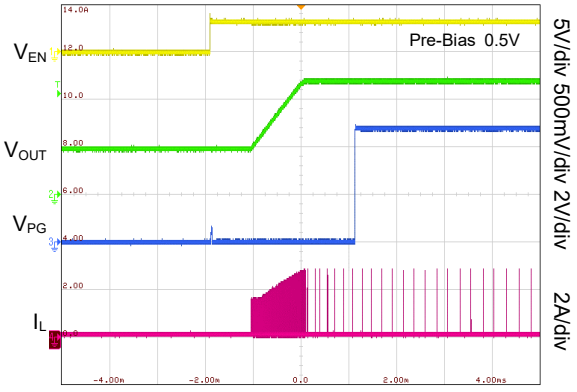
Time (1ms/div)

Startup by EN (PSM)



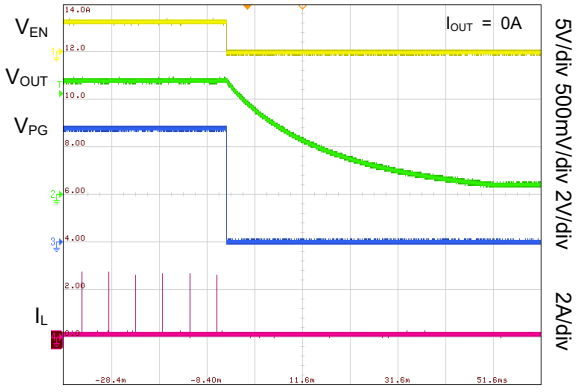
Time (1ms/div)

Startup by EN Pre-Bias (PSM)



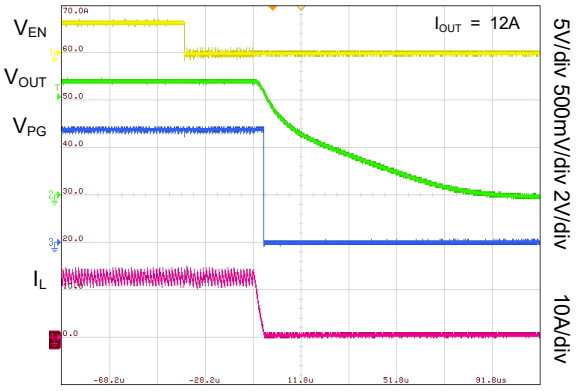
Time (1ms/div)

Shutdown by EN (PSM)



Time (10ms/div)

Shutdown by EN (PSM)



Time (20μs/div)

FUNCTIONAL BLOCK DIAGRAM

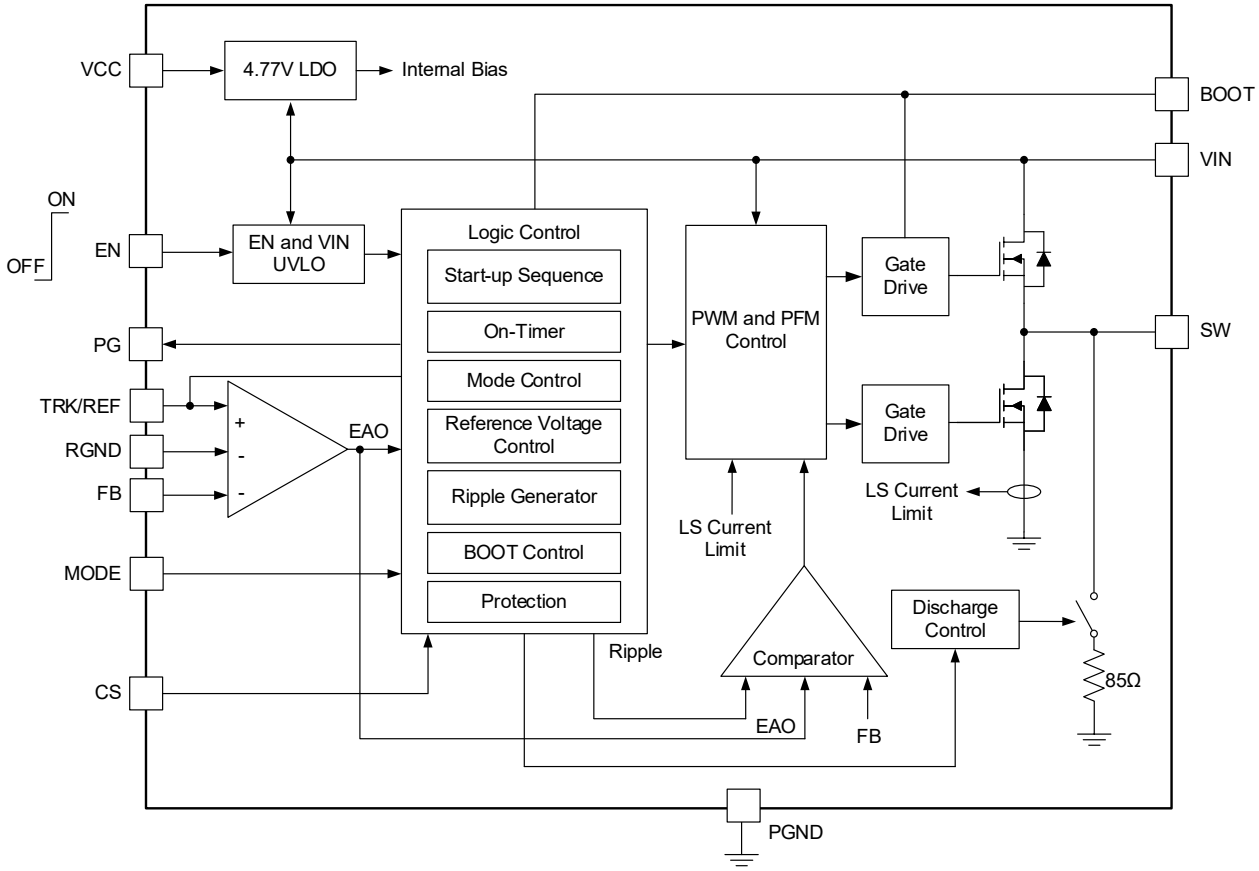


Figure 2. Functional Block Diagram

DETAILED DESCRIPTION

COT Control

The SGM611A13 uses constant-on-time (COT) structure to realize fast transient performance. Figure 3 shows the details of the control stage of SGM611A13. The error amplifier (EA) with a dedicated RGND pin corrects error voltage to achieve accurate remote output no matter in forced continuous conduction mode (FCCM) or pulse saving mode (PSM). The SGM611A13 adds internal ripple injection blocks to support low ESR MLCC output capacitor solution.

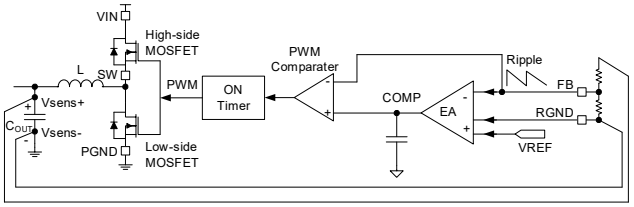


Figure 3. COT Control

PWM Operation

PWM is generated in this way as shown in Figure 4. The EA eliminates the error between FB and REF and creates a smooth DC voltage called EAO. The ripple generated internally is added to the FB. The combined FB is compared with the EAO signal to open the high-side MOSFET when combined FB is lower than EAO.

The high-side MOSFET remains on for a fixed turn-on time which is determined by V_{IN}, V_{OUT} and selected switching frequency. The high-side MOSFET turns off after a constant on-time. It will turn on again when FB + Ripple is lower than EAO. The low-side MOSFET will open after high-side MOSFET turns off. To avoid shoot-through, a dead time (DT) is generated internally between the time when the high-side MOSFET turns off and the low-side MOSFET turns on, or vice versa.

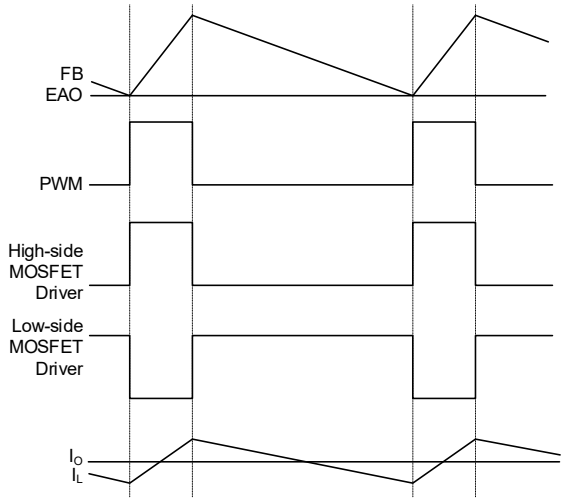


Figure 4. Heavy Load Operation (PWM)

CCM Operation

The device operates under continuous conduction mode (CCM) with a pseudo-constant frequency when the output load is high. The SGM611A13 can also be set up to operate in forced CCM even when the output current is low. For more details, see the Mode Selection section.

Pulse Saving Operation

The SGM611A13 can be set to work in pulse saving mode (PSM) to improve the efficiency. When the inductor current reaches zero as the load decreasing, the device enters the PSM from CCM. For more details, refer to the Mode Selection section.

Mode Selection

The SGM611A13 can be configured the FCCM or PSM under light load output. The SGM611A13 provides three switching frequency selections as shown in Table 1.

Table 1. MODE Selection

MODE	Light Load Mode	Switching Frequency
V_{CC}	Pulse Saving	600kHz
243kΩ (±20%) to GND	Pulse Saving	800kHz
121kΩ (±20%) to GND	Pulse Saving	1000kHz
GND	Forced CCM	600kHz
30.1kΩ (±20%) to GND	Forced CCM	800kHz
60.4kΩ (±20%) to GND	Forced CCM	1000kHz

DETAILED DESCRIPTION (continued)

Soft-Start (SS)

The soft-start time is set by adding SS capacitor to TRK/REF with a 0.91ms limit determined by Equations 1 and 2 as shown below:

$$C_{SS}(ns) = \frac{t_{SS}(ms) \times 36(\mu A)}{0.6(V)} \quad (1)$$

$$C_{SS} = C_{SS1} + C_{SS2} \quad (2)$$

where C_{SS2} is recommended to be minimum of 22nF.

Pre-Bias Startup

The SGM611A13 supports pre-bias voltage startup. If FB voltage is higher than TRK/REF voltage, the IC latches off the bridge. The IC will enable MOSFETs when the TRK/REF voltage ramping up and exceeding FB voltage.

Output Voltage Discharge

When EN shutdown occurs, SGM611A13 turns off the MOSFETs bridge and turns on discharge FET (85Ω) between SW and PGND until the FB is lower than 60mV.

Current Sense and Over-Current Protection (OCP)

The SGM611A13 integrates current sensing and adjustable OCP threshold. When active, the sensed current compares with the reference current programmed by resistor on CS pin. The device limits the low-side current cycle-by-cycle.

Low-side current limit is determined by Equation 3 as shown below:

$$I_{LSCL} = G_{CS} \times R_{CS} \quad (3)$$

where G_{CS} = 2.4A/kΩ.

The SGM611A13 enables hiccup function after EN startup 3ms. The device enters hiccup mode to close high-side MOSFET immediately and close low-side MOSFET after ZCD asserted when triggers OCP 15 times or detects the UVP. The TRK/REF capacitors are also cleared at the same time. The SGM611A13 will try to restart after around 11ms. If OCP persists after restart 3ms, the device repeats the cycle until normal operation resumes.

Negative Inductor Current limit

The SGM611A13 limits the negative current above -10A. It will close low-side MOSFET and open high-side MOSFET to boost the current higher than -10A when detects -10A current.

Output Sinking Mode (OSM)

The SGM611A13 uses output sinking mode (OSM) to maintain output voltage at target reference. OSM is activated when FB voltage exceeds 636mV (1.06 × V_{REF}) but is lower than OVP limit. In OSM, the low-side MOSFET stays on until -5.5A current is reached. It will close low-side MOSFET and open high-side MOSFET and then open low-side MOSFET after a constant on-time. The SGM611A13 exits OSM until FB voltage drops below 618mV (1.03 × V_{REF}). It will generate 15 cycles FCCM pulse after exiting OSM.

Over-Voltage Protection (OVP)

SGM611A13 realizes latch output voltage OVP by the feedback resistor divider.

The FB voltage is higher than 1.16 × V_{REF} triggers OVP. The high-side MOSFET is latches off and PGOOD is de-asserted until VCC/EN power recycle. At the same time, low-side MOSFET stays on until triggered negative current limit (NOCP, -10A). It will close low-side MOSFET and open high-side MOSFET to boost the current higher than -10A when detects -10A current. The SGM611A13 repeats the operation to reduce output voltage. The low-side MOSFET turns off immediately for PSM and remains turning on for FCCM until V_{FB} < 0.5 × V_{REF}.

Over-Temperature Protection (OTP)

The SGM611A13 supports OTP by supervising the junction temperature. If the junction temperature is higher than +160ºC, it shuts down and discharges the TRK/REF capacitors. The device restarts when junction temperature drops below +130℃.

Output Voltage Setting and Remote Output Voltage Sensing

An external resistor divider for feedback is determined as shown in Equation 4:

$$R_{FB1}(k\Omega) = \frac{V_{REF}}{V_{OUT} - V_{REF}} \times R_{FB2}(k\Omega) \quad (4)$$

It is recommended to add a feedforward cap in parallel with R_{FB2} to improve load transient performance. The C_{FF} introduces an additional zero to optimize loop performance. Position this zero at 20kHz ~ 60kHz as shown in Equation 5.

$$f_Z = \frac{1}{2\pi \times R_{FB2} \times C_{FF}} \quad (5)$$

DETAILED DESCRIPTION (continued)

Power Good (PGOOD)

The SGM611A13 supports a PG function with an OD MOS to indicate voltage status. The PG should be pulled up to a power rail (V_{CC} or external rail less than 5.5V) through a resistor (e.g. 10kΩ).

During startup, PG is de-asserted until the FB reaches 0.925 × V_{REF}. The PG will be pulled high after 0.91ms when the FB achieves soft-start end conditions. When the V_{OUT} is lower than UVP threshold or higher than OVP threshold, the PG is pulled low. On the other hand, V_{IN} failure leads to PGOOD low as well.

EN Configuration

EN controls SGM611A13 enable/disable so that it should not be left floating. Users use a resistors tree between VIN and AGND to set the enable input voltage precisely. It is recommended to prevent device turn-on/off oscillation during VIN power on/off by this approach.

The resistor divider for EN control can be calculated by Equation 6:

$$V_{IN\_START}(V) = V_{IHEN} \times \frac{R_{UP} + R_{DOWN}}{R_{DOWN}} \quad (6)$$

V_{IHEN} = 1.22V (TYP)

Choose R_{UP} and R_{DOWN} to ensure V_{EN} ≤ 5.5V at maximum V_{IN}. EN can link to VIN by R_{UP}, with a maximum 50μA current. Equation 7 simplifies R_{UP} calculation.

$$R_{UP}(k\Omega) = \frac{V_{INMAX}(V)}{0.05(mA)} \quad (7)$$

APPLICATION INFORMATION

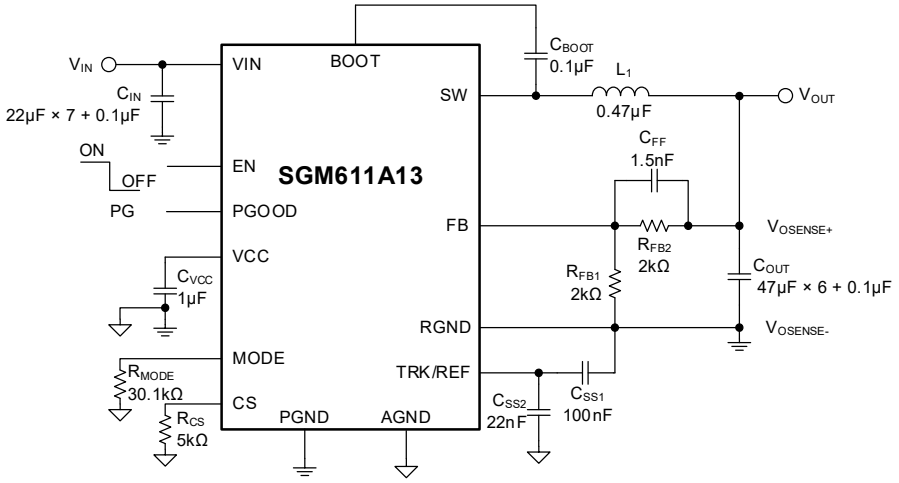


Figure 5. Application Circuit

Design Requirements

Table 2. Design Parameters

Design Parameters	Example Values
Input Voltage	5V to 16V
Output Voltage	1.2V
Output Current	12A

Input Capacitor

Because of the discontinuous input current, the capacitor is needed to provide the AC current to stabilize the DC input voltage for Buck converter. For optimal performance, ceramic capacitors are recommended. In practical design, the input capacitors should be as close as possible to the VIN and PGND pins.

Note that the capacitance is sensitive to temperature, so capacitors with X5R or X7R ceramic dielectrics are preferred due to their stability across a board temperature range and low equivalent series resistance (ESR).

Additionally, the rated ripple current of the selected capacitor should ensure that it is higher than the maximum input ripple current of the converter. The input ripple current can be estimated by Equation 8 and Equation 9:

$$I_{CIN} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (8)$$

The worst-case condition is observed at $V_{IN} = 2V_{OUT}$, as shown in Equation 9:

$$I_{CIN} = \frac{I_{OUT}}{2} \quad (9)$$

For ease of design, select the input capacitor's RMS current rating is at least 50% of the maximum load current. The input capacitance directly influences the Buck converter's input voltage ripple. In systems with ripple specifications, select a capacitor that complies.

Refer to Equation 10 and Equation 11 to calculate the expected input voltage ripple:

$$\Delta V_{IN} = \frac{I_{OUT}}{f_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (10)$$

The worst-case condition is observed at $V_{IN} = 2V_{OUT}$, as shown in Equation 11:

$$\Delta V_{IN} = \frac{1}{4} \times \frac{I_{OUT}}{f_{SW} \times C_{IN}} \quad (11)$$

Output Capacitor

The output capacitor is responsible for maintaining a steady DC output voltage. POSCAP or ceramic capacitors are preferred for optimal performance.

Equation 12 can be used to estimate the output voltage ripple, where:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_{SW} \times C_{OUT}}\right) \quad (12)$$

The impedance of ceramic capacitors at the switching frequency is dominated by their capacitances, which also affects the output voltage ripple. As a simplified approach, Equation 13 can be used to estimate the output voltage ripple, where:

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^{\ 2} \times L \times C_{OUT}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (13)$$

APPLICATION INFORMATION (continued)

The impedance of POSCAP capacitors at the switching frequency is dominated by their ESR. As a simplified approach, Equation 14 can be used to estimate the output voltage ripple, where:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR} \quad (14)$$

Inductor

A constant current is supplied by the switching input voltage to the output load through the inductor. By using larger inductances, the ripple current and output ripple voltage can be reduced, but a larger inductor will cause problems such as a bigger physical size, higher series resistance, and/or lower saturation current. Typically, the inductor value should be selected such that the peak-to-peak ripple current of the inductor falls within the range of 30% to 40% of the maximum switch current limit. Additionally, the design should ensure that the peak inductor current stays below this maximum switch current limit, and Equation 15 can be used to calculate the inductance value.

$$L = \frac{V_{OUT}}{f_{SW} \times \Delta I_L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (15)$$

Where ΔI_L is the peak-to-peak inductor ripple current.

Note that the saturated current of the selected inductor should exceed the maximum peak inductor current, which can be calculated using Equation 16:

$$I_{LP} = I_{OUT} + \frac{V_{OUT}}{2 \times f_{SW} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (16)$$

Table 3. List of Parameters

V_{OUT}	R_{FB1}	R_{FB2}	L	C_{OUT}	f_{SW}
0.6V	2kΩ	0Ω	0.22μH Wurth: 744373460022	47μF × 6	800kHz
1.2V	2kΩ	2kΩ	0.47μH Wurth: 744314047		
3.3V	2kΩ	9kΩ	1μH SPM10040T-1R0M		
5V	2kΩ	15kΩ	1.5μH Wurth: 7443340150		

PCB Layout Guidelines

PCB layout is critical to ensure the stable operation of the system, so refer to Figure 6 and follow the following guidelines to achieve the best performance:

1. The input MLCC capacitors should be placed as close as possible to the VIN and PGND pins, with the major MLCC capacitors on the same layer as the SGM611A13.

2. A 0402 capacitor with a value of 0.1μF is needed to place as close as possible to the VIN pin.

3. The VCC decoupling capacitor should be placed near the device.

4. The BOOT capacitor should be placed as close as possible to the BOOT and SW pins, and the capacitance is recommended a 0.1μF to 1μF.

5. REF capacitors should be placed close to TRK/REF, AGND and RGND pins. Note that capacitances are recommended to be greater than 10nF.

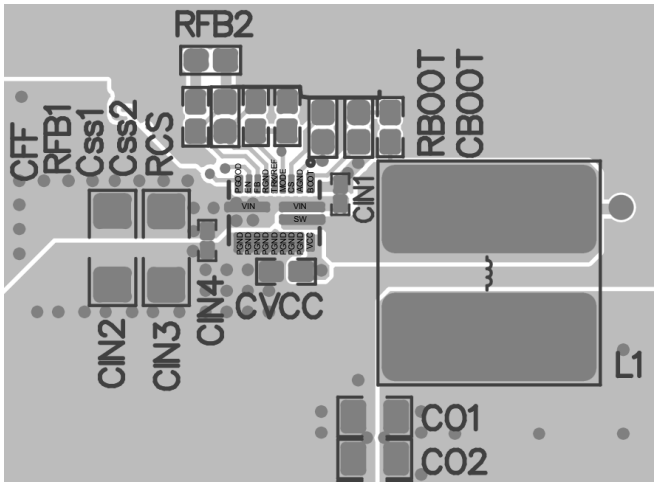


Figure 6. Recommended PCB Layout

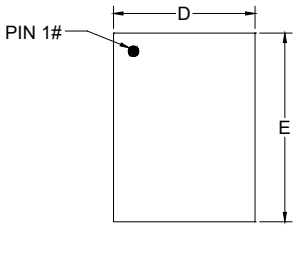
REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

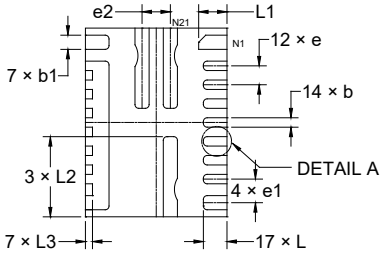
Changes from Original to REV.A (SEPTEMBER 2025)	Page
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

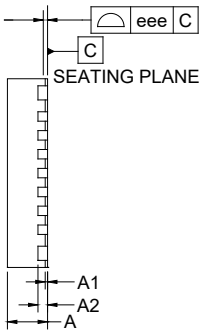
TQFN-3×4-21L



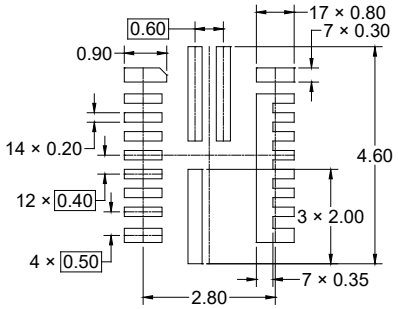
TOP VIEW



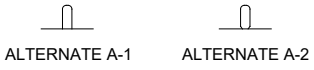
BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN (Unit: mm)



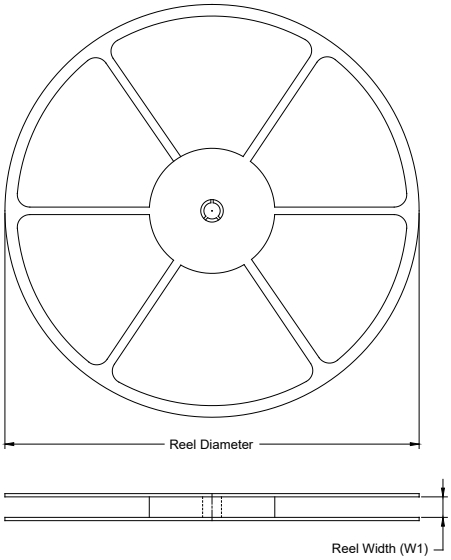
DETAIL A
ALTERNATE TERMINAL CONSTRUCTION

Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	0.800	-	0.900
A1	0.000	-	0.050
A2	0.203 REF		
b	0.150	-	0.250
b1	0.250	-	0.350
D	2.900	-	3.100
E	3.900	-	4.100
e	0.400 BSC		
e1	0.500 BSC		
e2	0.600 BSC		
L	0.400	-	0.600
L1	0.500	-	0.700
L2	1.600	-	1.800
L3	0.150 REF		
eee	0.080		

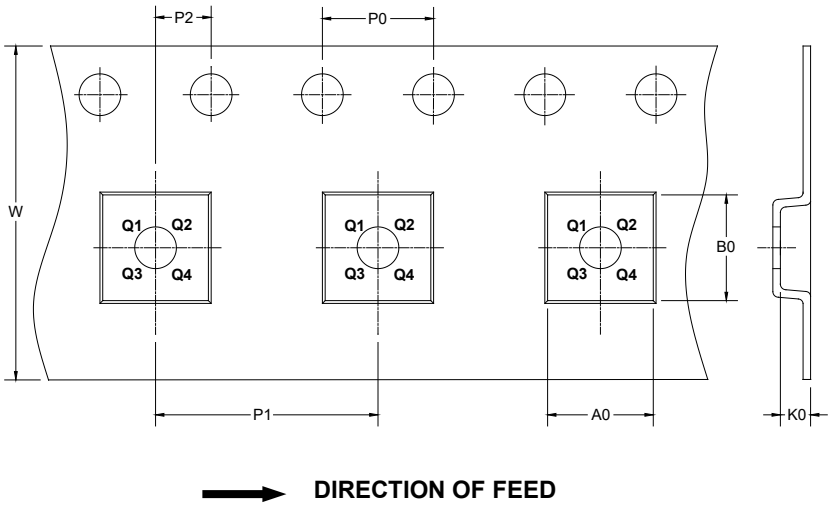
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



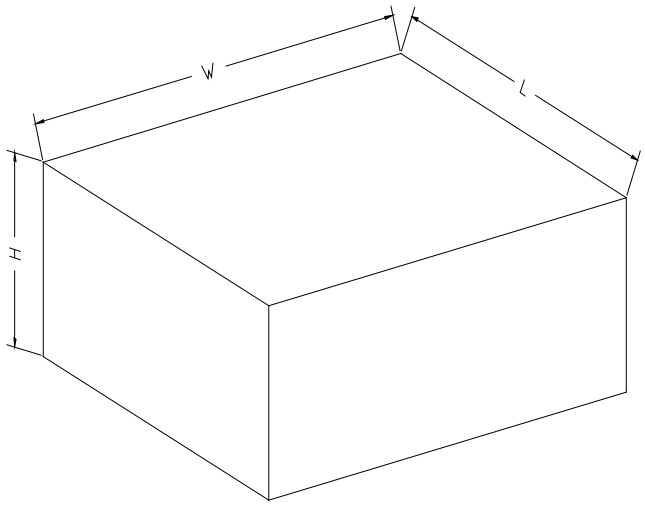
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TQFN-3×4-21L	13"	12.4	3.30	4.30	1.10	4.0	8.0	2.0	12.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002