SGM37380YG
Highly Efficient 8-String White LED Driver

GENERAL DESCRIPTION

The SGM37380YG is a high efficiency 8-string white-LED driver with low-headroom voltage for LED regulation and small on-resistance of switching MOSFET. The SGM37380YG operates from 2.5V to 12V input voltage, and is capable of driving up to 10 LEDs in series for 30mA maximum LED current per string while achieving high conversion efficiency.

An adaptive current-regulated method allows different LED string voltages while LED current remains in regulation. The LED current is programmed through an I^2C interface or through a PWM signal input. These features make it optimized for compact solutions and ideal for LCD display backlighting.

The SGM37380YG features I^2C dimming mode, PWM dimming mode and I^2C × PWM dimming mode setting via brightness control register LED_MOD[1:0] bits.

The SGM37380YG is available in a Green WLCSP-1.7×2.4-20B package. It operates over the -40℃ to +85℃ temperature range.

FEATURES

- **12-Bit Dimming Resolution**
- **Up to 91% Solution Efficiency**
- **Support 1 to 8 LED Strings in Parallel at Typical 31.5V Output**
- **PWM Dimming Interface**
- **Programmable I^2C Interface**
- **Phase Shift Function**
- **Hybrid PWM + Current Dimming for Higher LED Driver Optical Efficiency**
- **1.225MHz/650kHz/350kHz Switching Frequency**
- **LED String Open Detection**
- **LED String Short Detection**
- **LED String Over-Voltage Protection**
- **LED String Over-Current Protection**
- **Programmable Current Limit of Boost**
- **Thermal Shutdown Protection**

APPLICATIONS

Smart Phone
Tablets Backlighting
Small Size LCD Displays

TYPICAL APPLICATION

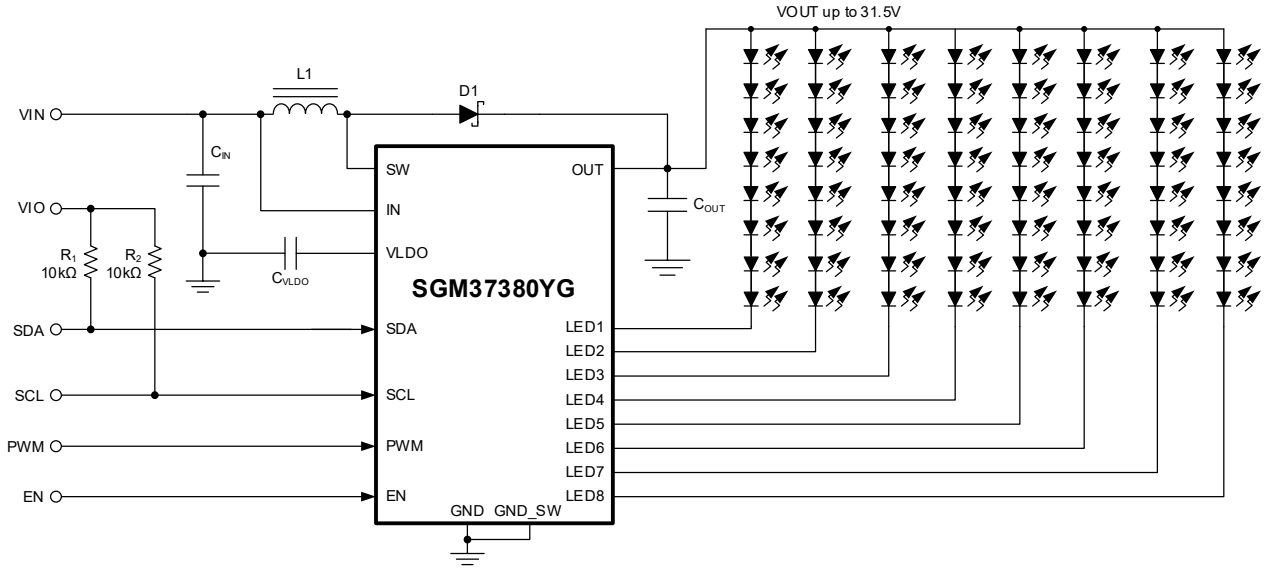


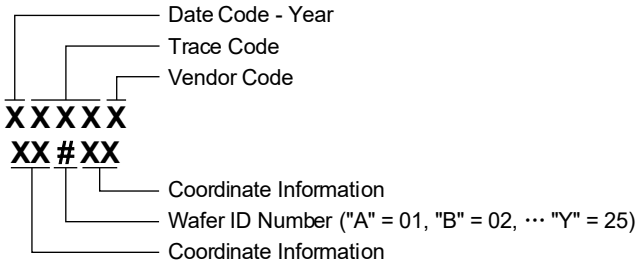
Figure 1. Typical Application Circuit

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM37380YG	WLCSP-1.7×2.4-20B	-40℃ to +85℃	SGM37380YG/TR	37380 XXXXX XX#XX	Tape and Reel, 3000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code. XX#XX = Coordinate Information and Wafer ID Number.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

IN ..... -0.3V to 15V
OUT ..... -0.3V to 33V
SW ..... -0.3V to 33V
LED1, LED2, LED3, LED4, LED5, LED6, LED7, LED8
..... -0.3V to 33V
PWM, SDA, SCL ..... -0.3V to 6V
VLDO ..... -0.3V to 6V
EN ..... -0.3V to 6V
Package Thermal Resistance
WLCSP-1.7×2.4-20B, θ_{JA} ..... 63.4℃/W
WLCSP-1.7×2.4-20B, θ_{JB} ..... 16.7℃/W
WLCSP-1.7×2.4-20B, θ_{JC} ..... 16.7℃/W
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility (1) (2)
HBM ..... ±2000V
CDM ..... ±1000V

NOTES:

1. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.

2. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

RECOMMENDED OPERATING CONDITIONS

IN ..... 2.5V to 12V
OUT ..... 0V to 31.5V
SW ..... 0V to 31.5V
LED1, LED2, LED3, LED4, LED5, LED6, LED7, LED8
..... 0V to 31V
PWM, SDA, SCL ..... 0V to 5.5V
VLDO ..... 0V to 5.5V
EN ..... 0V to 5.5V
Operating Temperature Range ..... -40℃ to +85℃

OVERSTRESS CAUTION

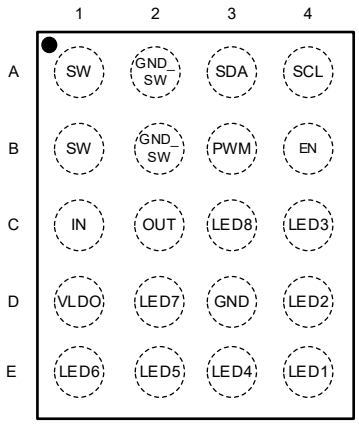
Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

PIN CONFIGURATION

(TOP VIEW)



WLCSP-1.7×2.4-20B

PIN DESCRIPTION

PIN	NAME	I/O	FUNCTION
A1, B1	SW	I	Drain Connection for Internal Low-side NFET N-Channel MOSFET. Connect to the anode of an external Schottky diode.
A2, B2	GND_SW	G	Power Ground.
A3	SDA	I/O	I^2C Data Signal.
A4	SCL	I	I^2C Clock Signal.
B3	PWM	I	PWM Dimming Signal Input.
B4	EN	I	Hardware Enable Input. Drive EN high to enable the device and allow I^2C write commands or PWM control.
C1	IN	I	Input Supply Pin. Connect a at least 2.2μF bypass capacitor from IN to GND.
C2	OUT	O	Output Voltage Sense Pin. It is used for sensing the output voltage for over-voltage protection. Connect to the positive terminal of the output capacitor.
C3	LED8	O	Current Sink Regulation Input. If unused tie to ground.
C4	LED3	O	Current Sink Regulation Input. If unused tie to ground.
D1	VLDO	O	Internal LDO Output Pin. Connect a C_{VLDO} capacitor from this pin to the ground.
D2	LED7	O	Current Sink Regulation Input. If unused tie to ground.
D3	GND	G	Analog Ground.
D4	LED2	O	Current Sink Regulation Input. If unused tie to ground.
E1	LED6	O	Current Sink Regulation Input. If unused tie to ground.
E2	LED5	O	Current Sink Regulation Input. If unused tie to ground.
E3	LED4	O	Current Sink Regulation Input. If unused tie to ground.
E4	LED1	O	Current Sink Regulation Input. If unused tie to ground.

NOTE: I = input, O = output, I/O = input or output, G = ground.

ELECTRICAL CHARACTERISTICS

(V_{IN} = 3.8V, T_A = -40℃ to +85℃, typical values are at T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
VIN						
Input Voltage for IN	V_{IN}		2.5		12	V
Input UVLO Voltage for IN	V_{UVLO}	UVLO_TH = 0		2.3	2.6	V
		UVLO_TH = 1		4.8	5.2	V
Input UVLO Hysteresis	V_{UVLO_HYST}			100		mV
Quiescent Current	I_Q	No switching, PWM duty cycle = 0%		0.65	1.85	mA
Shutdown Current	I_{SHUT}	V_{IN} = 3.8V, EN = 0V		0.5	2	μA
Boost						
LED Current Matching I_{LED1} ~ I_{LED8} (Initialization)	I_{MATCH} (1)	I_{LED} = 12.21μA, V_{LED} = 380mV, T_A = +25℃		3.5	15	%
		I_{LED} = 25mA, V_{LED} = 260mV, T_A = +25℃		0.23	3	
Minimum LED Current (per String) (Initialization)	I_{LED_MIN}	T_A = +25℃	10.38	12.21	14.04	μA
Maximum LED Current (per String) (Initialization)	I_{LED_MAX}	LED_MAX[1:0] = 01, T_A = +25℃	24.25	25	25.75	mA
Regulated Current Sink Headroom Voltage	V_{HR}	I_{LED} = 25mA		260		mV
NMOS Switch On-Resistance	R_{NMOS}	I_{SW} = 500mA		0.085		Ω
NMOS Switch Current Limit	I_{CL}			3.5		A
Output Over-Voltage Protection	V_{OVP}	BOOST_OVP[1:0] = 11	30	31.5		V
OVP Hysteresis	V_{OVP_HYST}			3		V
Switching Frequency	f_{SW}	BOOST_FREQ[1:0] = 10		1225		kHz
		BOOST_FREQ[1:0] = 01		650		kHz
		BOOST_FREQ[1:0] = 00		350		kHz
Maximum Boost Duty Cycle	D_{MAX}			95		%
VLDO Output Voltage	V_{LDO}		4.56	4.8	5.04	V
VLDO Short-Circuit Current	I_{SHORT}			35		mA
Thermal Shutdown	T_{SD}			160		℃
Thermal Shutdown Hysteresis				20		
PWM Input						
PWM Dimming Frequency Range	DFR		5		100	kHz
Turn-Off Delay	t_{STBY}	PWM input low time for turnoff		4		ms
Input Logic High	V_{IH}	EN, SCL, SDA, PWM inputs	0.95			V
Input Logic Low	V_{IL}	EN, SCL, SDA, PWM inputs			0.32	

NOTE:

1. LED current matching depends on the two channels with the largest current difference, and its calculation formula is (I_{LED_MAX} - I_{LED_MIN})/(I_{LED_MAX} + I_{LED_MIN}) × 100%.

I²C TIMING REQUIREMENTS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Maximum I²C Clock Frequency	f_{SC_MAX}	1		1000	kHz
SCL Clock Period	t_1	1			μs
Data in Setup Time to SCL High	t_2	50			ns
Data Out Stable After SCL Low	t_3	0			ns
SDA Low Setup Time to SCL Low (Start)	t_4	260			ns
SDA High Hold Time After SCL High (Stop)	t_5	260			ns

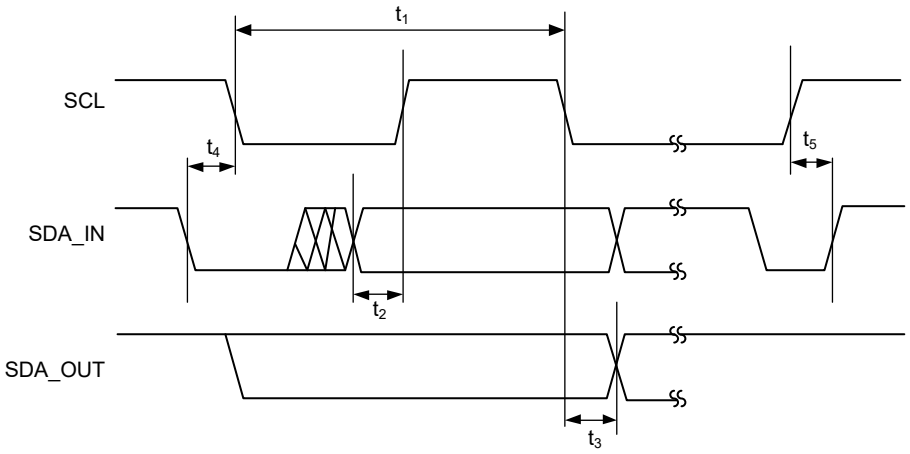
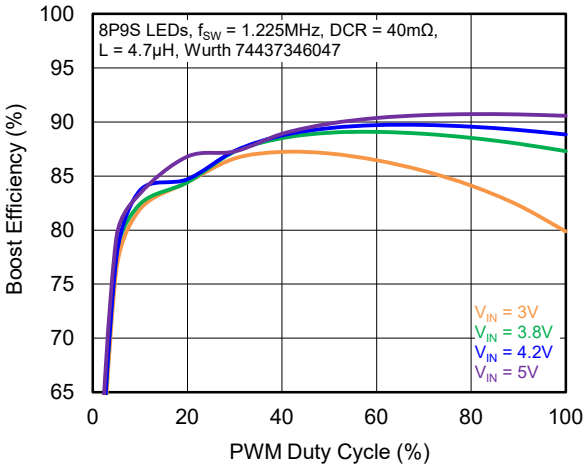


Figure 2. I²C Timing

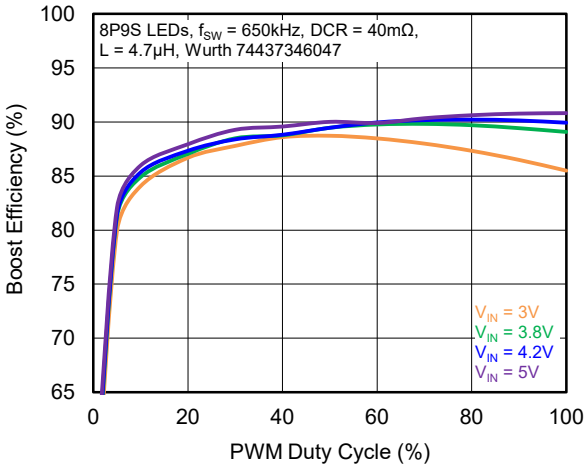
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = +25℃, unless otherwise noted.

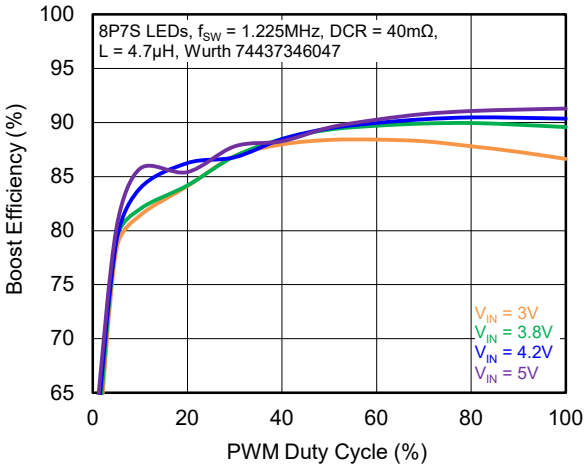
Boost Efficiency vs. PWM Duty Cycle



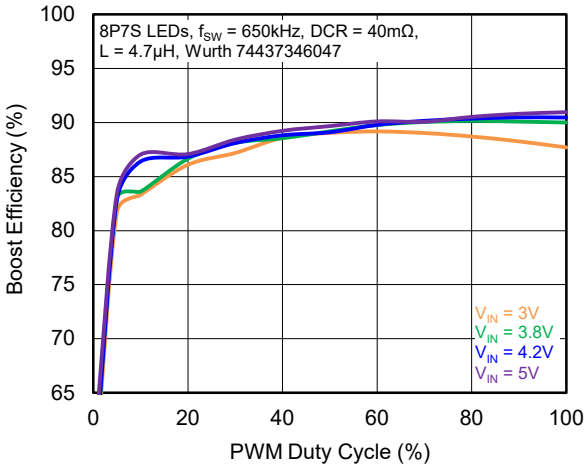
Boost Efficiency vs. PWM Duty Cycle



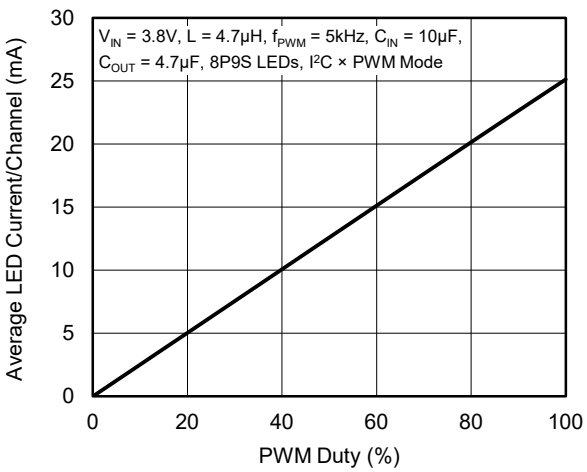
Boost Efficiency vs. PWM Duty Cycle



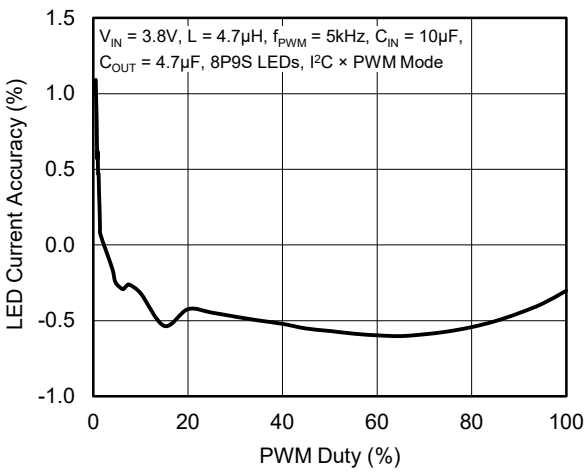
Boost Efficiency vs. PWM Duty Cycle



Average LED Current vs. PWM Duty Cycle



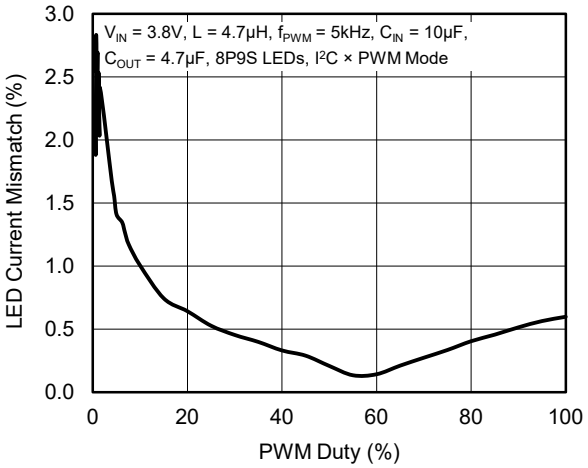
LED Current Accuracy vs. PWM Duty Cycle



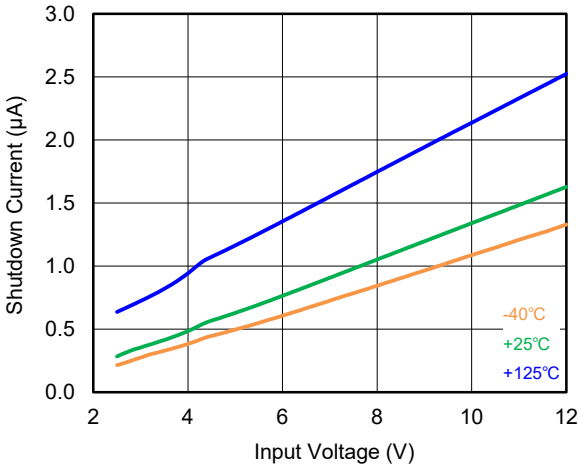
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, unless otherwise noted.

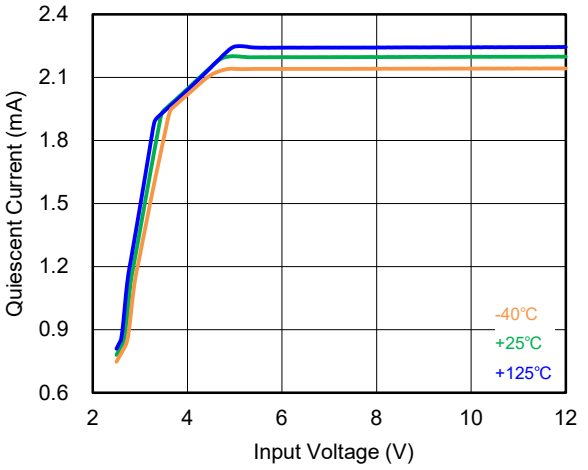
LED Current Mismatch vs. PWM Duty Cycle



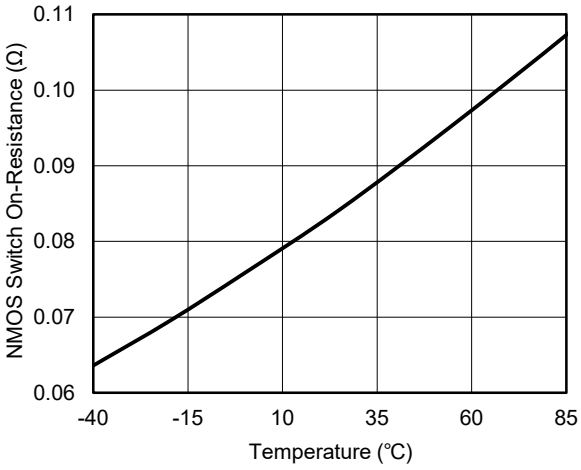
Shutdown Current vs. Input Voltage



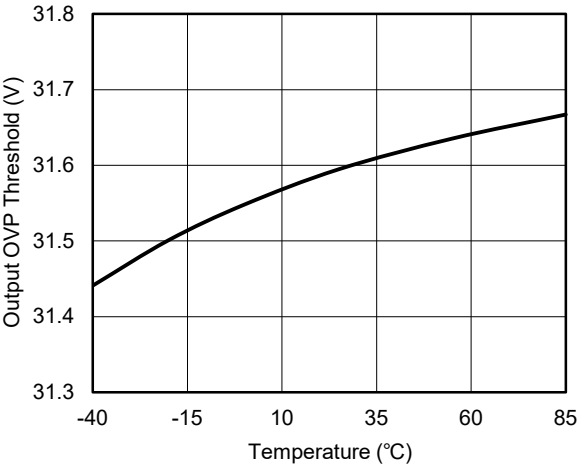
Quiescent Current (Switching) vs. Input Voltage



NMOS Switch On-Resistance vs. Temperature



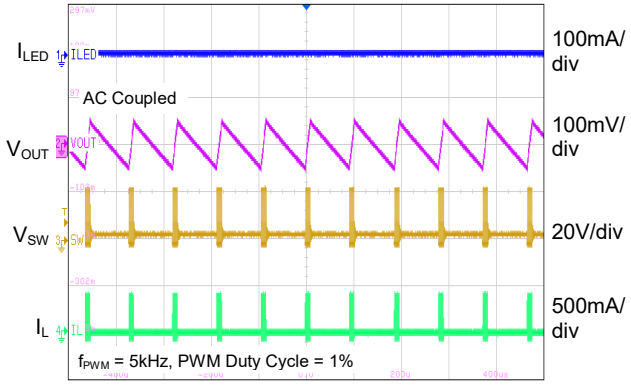
Output Over-Voltage Protection Threshold vs. Temperature



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

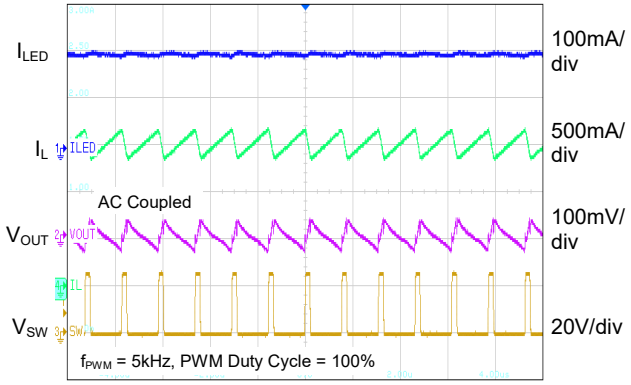
T_A = +25℃, V_{IN} = 3.8V, L = 4.7μH, 8P9S LEDs, I_{LEDx} = 25mA/channel, I^2C × PWM mode, unless otherwise noted.

Output Voltage Ripple



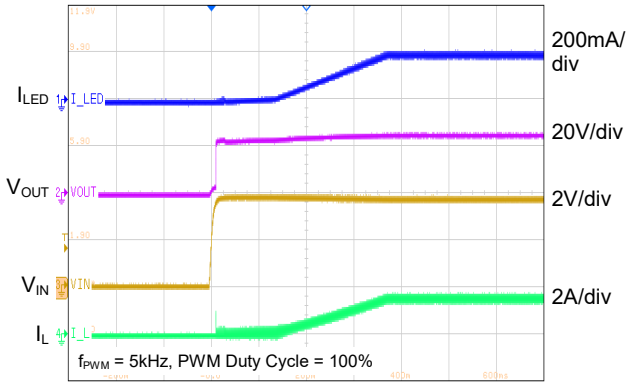
Time (100μs/div)

Output Voltage Ripple



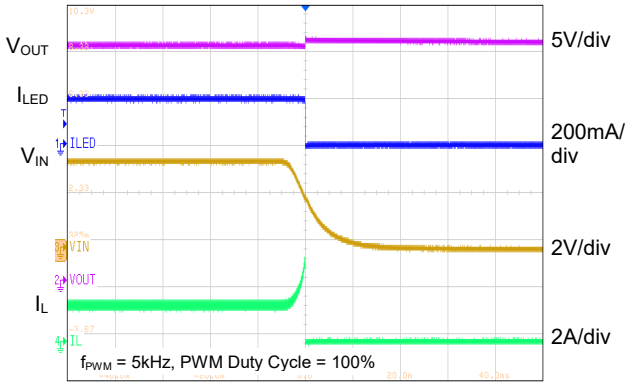
Time (1μs/div)

VIN Start-Up



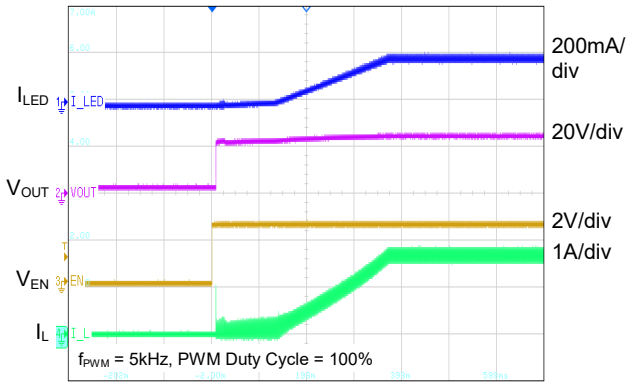
Time (100ms/div)

VIN Shutdown



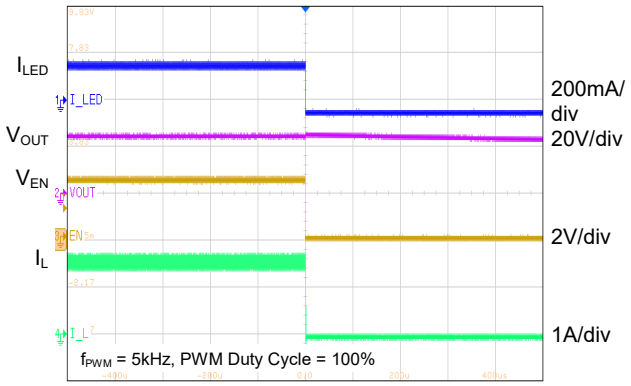
Time (10ms/div)

EN Start-Up



Time (100ms/div)

EN Shutdown

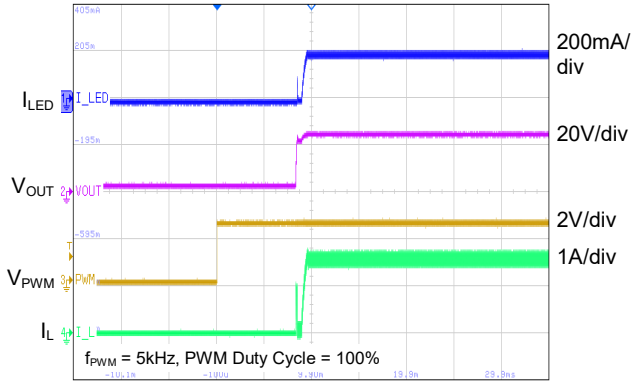


Time (100μs/div)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

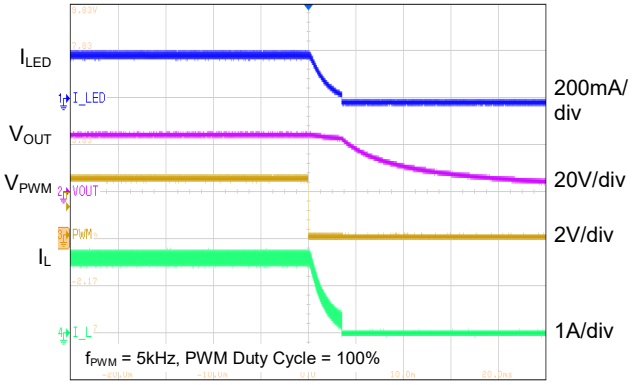
T_A = +25℃, V_{IN} = 3.8V, L = 4.7μH, 8P9S LEDs, I_{LEDx} = 25mA/channel, I^2C × PWM mode, unless otherwise noted.

PWM Start-Up



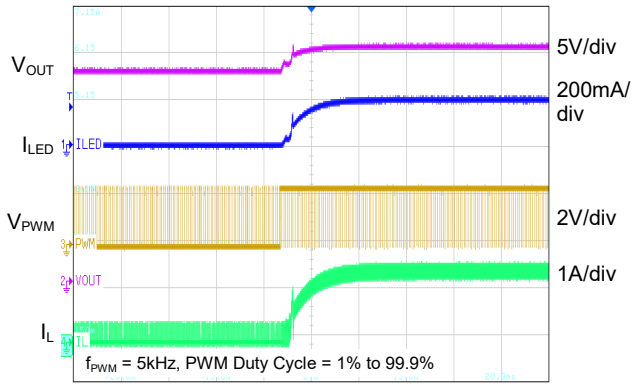
Time (5ms/div)

PWM Shutdown



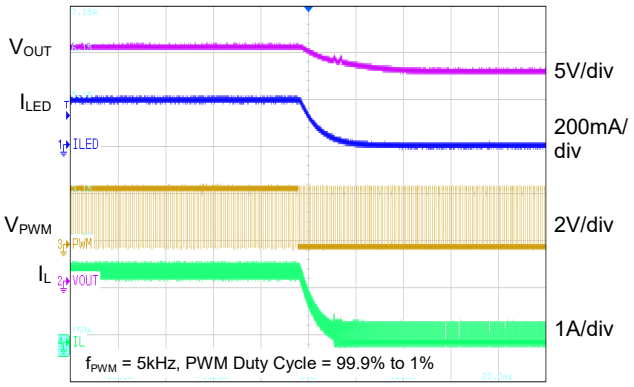
Time (5ms/div)

Brightness Transient



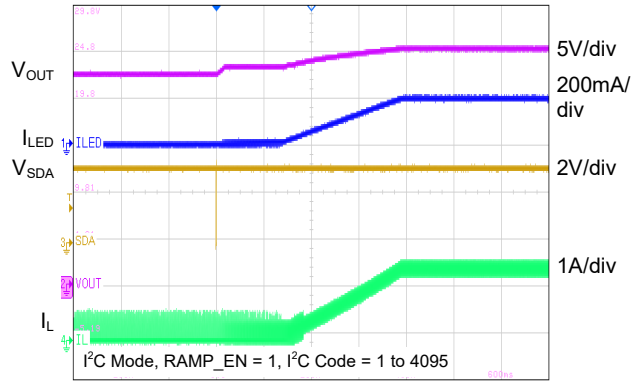
Time (5ms/div)

Brightness Transient



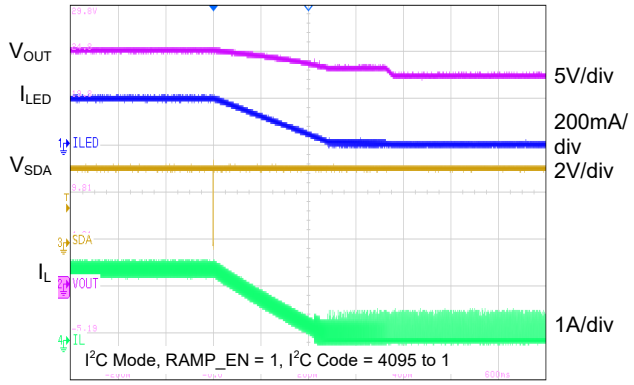
Time (5ms/div)

Brightness Transient



Time (100ms/div)

Brightness Transient

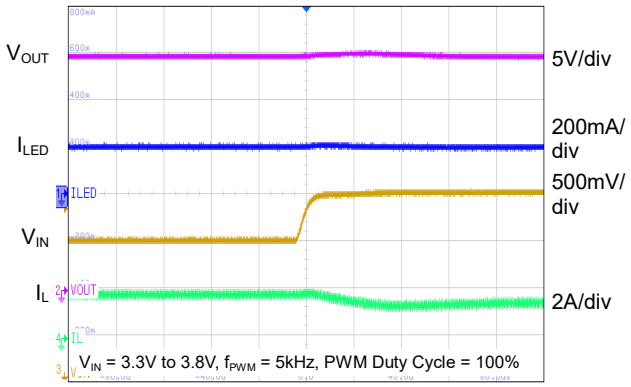


Time (100ms/div)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

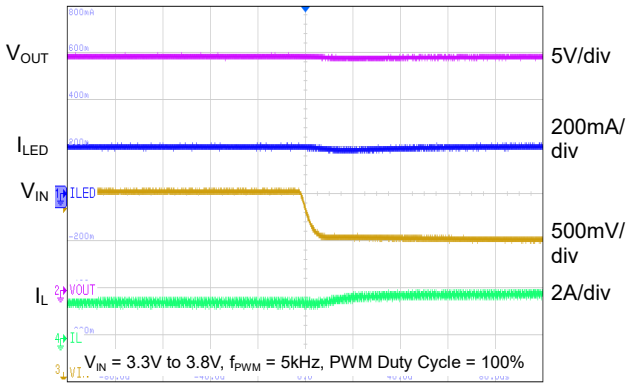
T_A = +25℃, V_{IN} = 3.8V, L = 4.7μH, 8P9S LEDs, I_{LEDx} = 25mA/channel, I^2C × PWM mode, unless otherwise noted.

Line Transient



Time (20μs/div)

Line Transient



Time (20μs/div)

FUNCTIONAL BLOCK DIAGRAM

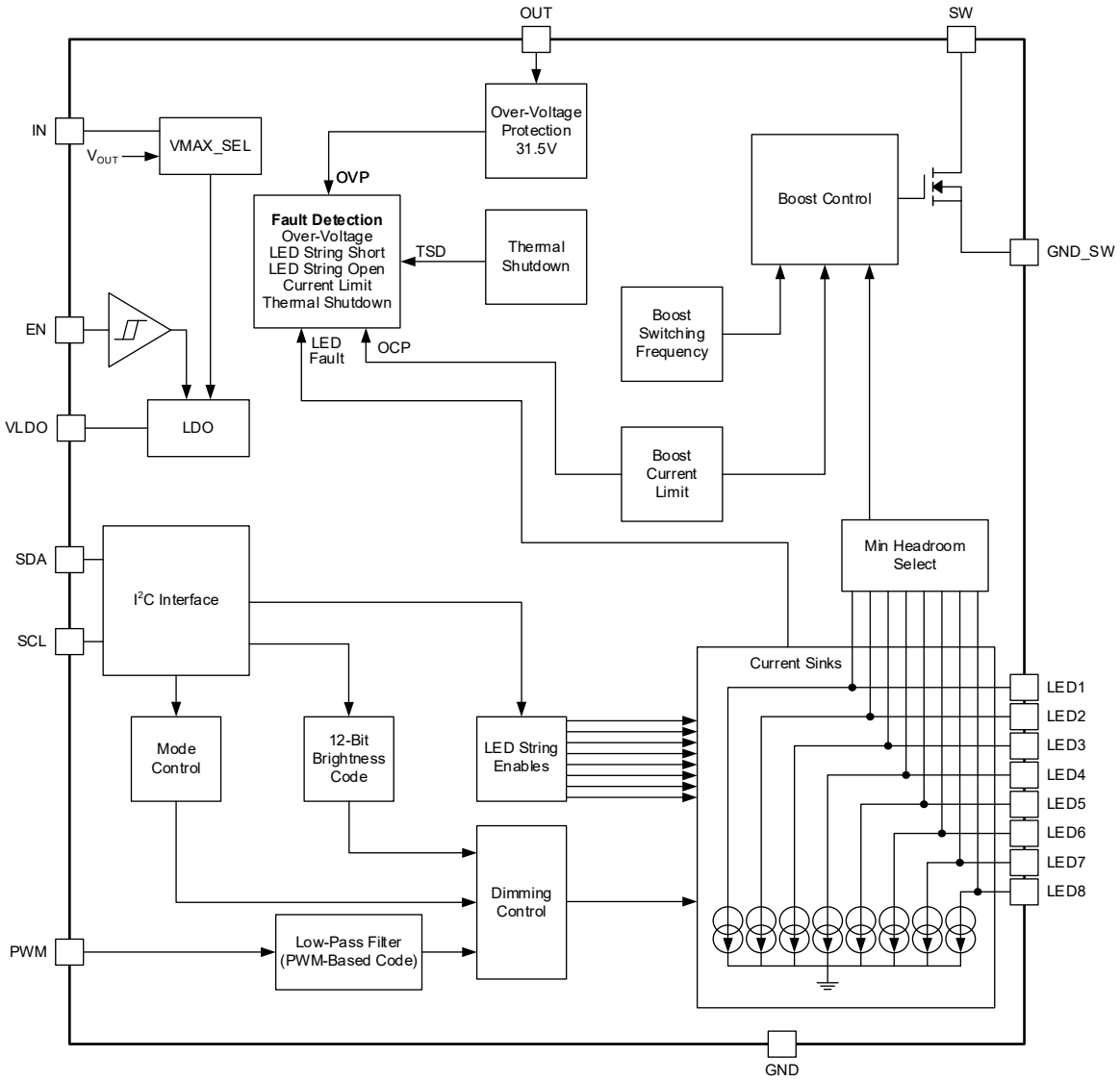


Figure 3. Functional Block Diagram

REGISTER MAPS

All registers are 8-bit and individual bits are named from D[0] (LSB) to D[7] (MSB).

I^2C Slave Address of SGM37380YG is: 0x36 (0b0110110 + R/W)

ADDRESS	REGISTER NAME	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
0x00	Device Code	DEV_COD[7:0]							
0x01	Software Reset	Reserved							SOFT_RST
0x09	Enable Control 0	PS_MODE[2:0]			LED4_EN	LED3_EN	LED2_EN	LED1_EN	DEV_EN
0x10	Enable Control 1	Reserved				LED8_EN	LED7_EN	LED6_EN	LED5_EN
0x11	Brightness Control	UVLO_TH	LED_MOD[1:0]		RAMP_EN	BOOST_FREQ[1:0]		RCOMP[1:0]	
0x1A	Brightness Code 0	Reserved				BRT_COD[3:0]			
0x19	Brightness Code 1	BRT_COD[11:4]							
0x1B	Maximum LED Current	SS_LIM	ISW_LIM[1:0]		LED_SCP	BOOST_OVP[1:0]		ILED_MAX[1:0]	
0x1F	Fault Information	Reserved			SO_FLAG	SC_FLAG	TSD_FLAG	OC_FLAG	OVP_FLAG

Bit Types:
R: Read only
R/W: Read/Write

REG0x00: Device Code Register [Reset = 0x82]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:0]	DEV_COD[7:0]	10000010	R	Reserved

REG0x01: Software Reset Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:1]	Reserved	0000000	R	Reserved
D[0]	SOFT_RST	0	R/W	Software Reset 0 = Normal Operation (default) 1 = Reset the device. It will return 0 automatically.

REGISTER MAPS (continued)

REG0x09: Enable Control 0 Register [Reset = 0xFF]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:5]	PS_MODE[2:0]	111	R/W	Phase Shift Selection 000 = 8-phase, 8 drivers (0°, 45°, 90°, 135°, 180°, 225°,270°, 315°) 001 = 7-phase, 8 drivers (0°, 51°, 102°, 153°, 204°, 255°, 306°, 0°) 010 = 6-phase, 8 drivers (0°, 60°, 120°, 180°, 240°, 300°, 0°, 60°) 011 = 5-phase, 8 drivers (0°, 72°, 144°, 216°, 288° ,0°, 72°, 144°) 100 = 4-phase, 8 drivers (0°, 0°, 90°, 90°, 180°, 180°, 270°, 270°) (12/34/56/78) 101 = 3-phase, 8 drivers (0°, 0°, 120°, 120°, 240°, 240°, 0°, 0°) (1278/34/56) 110 = 2-phase, 8 drivers (0°, 0°, 0°, 0°, 180°, 180°, 180°, 180°) (1234/5678) 111 = 1-phase, 8 drivers (0°, 0°, 0°, 0°, 0°, 0°, 0°, 0°) (12345678) (default) Note: The unused channels need to be disabled according to the LED output string configuration.
D[4]	LED4_EN	1	R/W	LED4 Enable 0 = Disabled 1 = Enabled (default)
D[3]	LED3_EN	1	R/W	LED3 Enable 0 = Disabled 1 = Enabled (default)
D[2]	LED2_EN	1	R/W	LED2 Enable 0 = Disabled 1 = Enabled (default)
D[1]	LED1_EN	1	R/W	LED1 Enable 0 = Disabled 1 = Enabled (default)
D[0]	DEV_EN	1	R/W	Device Enable 0 = Disabled 1 = Enabled (default)

REG0x10: Enable Control 1 Register [Reset = 0x0F]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:4]	Reserved	0000	R/W	Reserved
D[3]	LED8_EN	1	R/W	LED8 Enable 0 = Disabled 1 = Enabled (default)
D[2]	LED7_EN	1	R/W	LED7 Enable 0 = Disabled 1 = Enabled (default)
D[1]	LED6_EN	1	R/W	LED6 Enable 0 = Disabled 1 = Enabled (default)
D[0]	LED5_EN	1	R/W	LED5 Enable 0 = Disabled 1 = Enabled (default)

REGISTER MAPS (continued)

REG0x11: Brightness Control Register [Reset = 0x7B]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	UVLO_TH	0	R/W	IN Input Under-Voltage Lockout Threshold 0 = 2.3V (default) 1 = 4.8V
D[6:5]	LED_MOD[1:0]	11	R/W	LED Brightness Control Mode Selection 00 = I^2C Only 01 = PWM Only 10 = I^2C × PWM 11 = I^2C × PWM (default)
D[4]	RAMP_EN	1	R/W	Ramp Enable 0 = Disabled 1 = Enabled (default)
D[3:2]	BOOST_FREQ[1:0]	10	R/W	Switching Frequency 00 = 350kHz 01 = 650kHz 10 = 1225kHz (default) 11 = 1225kHz
D[1:0]	RCOMP[1:0]	11	R/W	R_{COMP} Selection 00 = 400kΩ 01 = 600kΩ 10 = 800kΩ 11 = 1000kΩ (default)

REG0x1A: Brightness Code 0 Register [Reset = 0xFF]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:4]	Reserved	1111	R	Reserved
D[3:0]	BRT_COD[3:0]	1111	R/W	Lower 4 Bits of the 12-Bit Brightness Code

REG0x19: Brightness Code 1 Register [Reset = 0xFF]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:0]	BRT_COD[11:4]	11111111	R/W	High Byte of the 12-Bit Brightness Code

REG0x1B: Maximum LED Current Register [Reset = 0x7D]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	SS_LIM	0	R/W	Start-Up Current Limit 0 = 0.9A (default) 1 = 1.5A
D[6:5]	ISW_LIM[1:0]	11	R/W	SW Pin Current Limit 00 = 2.6A 01 = 2.9A 10 = 3.2A 11 = 3.5A (default)
D[4]	LED_SCP	1	R/W	LED Short Protection 0 = Disable 1 = Enable (default)
D[3:2]	BOOST_OVP[1:0]	11	R/W	Boost OVP 00 = 21V 01 = 25V 10 = 29V 11 = 31.5V (default)
D[1:0]	ILED_MAX[1:0]	01	R/W	Maximum LED Current Setting 00 = 20mA 01 = 25mA (default) 10/11 = 30mA

REGISTER MAPS (continued)

REG0x1F: Fault Information Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:5]	Reserved	000	R	Reserved
D[4]	SO_FLAG	0	R	LED String Open Fault Flag 0 = No LED open fault (default) 1 = LED open fault
D[3]	SC_FLAG	0	R	Short-Circuit Fault Flag 0 = No short-circuit fault (default) 1 = Short-circuit fault
D[2]	TSD_FLAG	0	R	Thermal Shutdown Fault Flag 0 = No thermal shutdown fault (default) 1 = Thermal shutdown fault
D[1]	OC_FLAG	0	R	Current Limit Fault Flag 0 = No current limit fault (default) 1 = Current limit fault
D[0]	OVP_FLAG	0	R	Output Over-Voltage Fault Flag 0 = No over-voltage fault (default) 1 = Over-voltage fault

DETAILED DESCRIPTION

The SGM37380YG is an LED driver that powers the backlight of the display screen. It can support up to 8 LED backlight channels, and each channel can support up to 30mA of sink current. The device supports three different dimming methods: configuring the internal register via I²C interface, changing the duty cycle of external PWM input, or combining the PWM dimming and I²C dimming.

Enabling the SGM37380YG

The SGM37380YG can be enabled by setting EN to logic high. Conversely, the SGM37380YG can be disabled by setting EN to logic low. When the device is disabled, the device goes into shutdown mode, and the Boost converter and current sink terminate operation. In addition, the register will be reset to the default value.

I²C can be enabled by setting EN to logic high and latching a high PWM pulse internally. VLDO can be powered on by setting both EN high and applying a high PWM pulse. For PWM dimming mode and I²C × PWM hybrid mode, VLDO will be pulled down if the PWM low pulse lasts longer than 4ms. For I²C mode, VLDO will not be pulled down by the PWM signal.

Current Sink Enable

By default, all current channels of the SGM37380YG are enabled. The enable status of each current sink can be controlled through the register, which allows the device to adapt to different LED configurations.

Figure 4 and Figure 5 depict the timing diagrams for enabling the current sink via PWM or I²C. When the enable bit of the current channel inside the device is set to 1, the device enters the standby state and waits for the non-zero PWM input. When the device detects a non-zero PWM input, it converts the PWM input into a brightness dimming code for LED dimming. In applications where I²C function is not used, the LED brightness of the SGM37380YG can be adjusted by changing the PWM duty cycle.

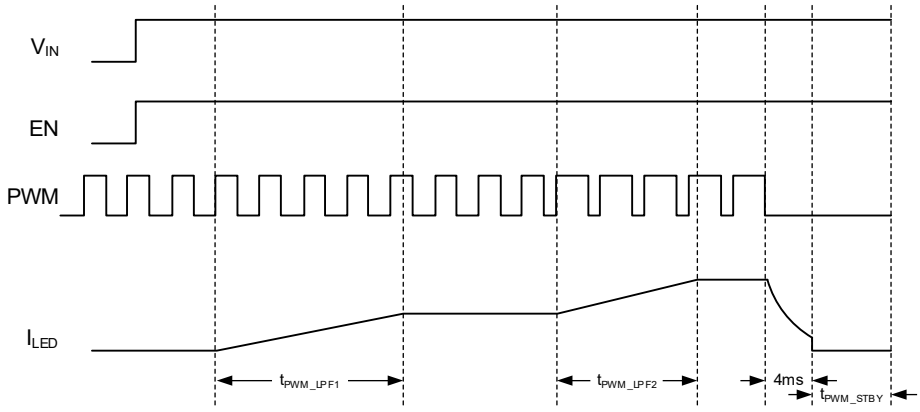


Figure 4. Enabling the SGM37380YG via PWM

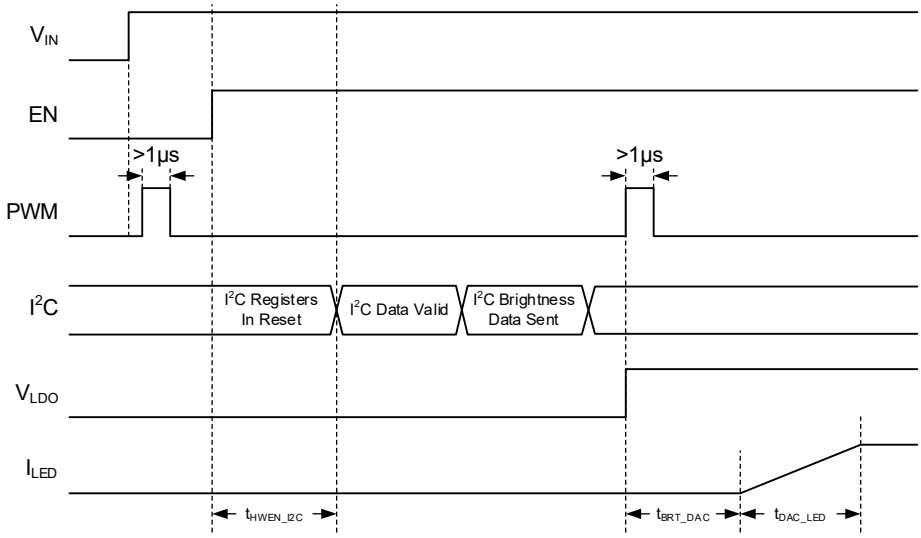


Figure 5. Enabling the SGM37380YG via I²C

DETAILED DESCRIPTION (continued)

SGM37380YG Start-Up

Table 1 shows the operating status of the SGM37380YG in different configurations. When EN is high, the device exits the shutdown state. When the PWM is continuously low or the brightness code in the register is zero, the current sink is disabled and the device is in standby mode.

Regulated Headroom Voltage

Due to the nonlinear differences of LED's forward voltage, the SGM37380YG needs to ensure that the LED string in each channel can reach the specified LED current. If LED8 is enabled to achieve the specified LED current corresponding to the anode voltage that is higher than the other seven channels, the SGM37380YG will use the LED8 channel as the feedback adjustment point of the Boost converter, and the cathode voltage of LED8 is set as V_{HR}.

Table 1. SGM37380YG Operating Modes

Device Enable DEV_EN Bit	LED String Enable LED1_EN/…/LED8_ EN Bits	PWM Input	I^2C Brightness Code BRT_COD[11:0]	Brightness Mode LED_MOD[1:0]	LED Current
0	XXXXXXXX	X	XXX	XX	Off, device disabled
1	00000000	X	XXX	XX	Boost enabled, LED current disabled
1	At least one enabled	X	000	00	Off, device in standby mode
1	At least one enabled	X	Code > 000	00	See (1)
1	At least one enabled	0	XXX	01	Off, device in standby mode
1	At least one enabled	PWM Signal	XXX (2)	01	See (1)
1	At least one enabled	0	XXX	10 or 11	Off, device in standby mode
1	At least one enabled	X	000	10 or 11	Off, device in standby mode
1	At least one enabled	PWM Signal	Code > 000	10 or 11	See (1)

NOTES:

1. I_{LED} is calculated by the equations from Equation 1 to Equation 8 below in Brightness Control Modes.
2. Code is forbidden to set to 0.

Brightness Control Modes

The SGM37380YG has 3 brightness control modes:

1. I^2C Only (brightness mode 00)
2. PWM Only (brightness mode 01)
3. I^2C × PWM (brightness mode 10 or 11)

I^2C Only (Brightness Mode 00)

In brightness control mode 00, only the I^2C brightness registers control the LED current. The brightness data (BRT) consists of the two brightness registers (4 LSBs) and (8 MSBs) (REG0x1A[3:0] and REG0x19[7:0], respectively). The LED current only changes when the MSBs are written, meaning that to do a full 12-bit current change via I^2C, first the 4 LSBs of REG0x1A are written and then the 8 MSBs of REG0x19 are written.

The 12-bit code (0 to 4095) is in control of the LED current as follows:

DETAILED DESCRIPTION (continued)

When the code is from 256 to 4095, the average LED current increases proportionally to the brightness code and follows the below relationship (see Figure 7).

When the code is an odd integer,

$$I_{LED\_AVG} = \frac{I_{LED\_MAX}}{2048} \times 0.5 \times (code - 1) \quad (1)$$

When the code is an even integer,

$$I_{LED\_AVG} = \frac{I_{LED\_MAX}}{2048} \times 0.5 \times code \quad (2)$$

where

I_{LED_AVG} = average LED current

I_{LED_MAX} = maximum LED current per string

When the code is from 16 to 255, the average LED current is calculated by Equation 1 and Equation 2 and the LED current is in current-to-PWM control (see Figure 7) with a constant maximum current, while the duty cycle changes following the code.

When the code is from 1 to 15, the average LED current increases exponentially to the brightness code, and follows the relationship by Equation 3 (see Figure 7). The LED current is also in current-to-PWM control, the duty cycle is 16/256 constantly, and the amplitude of current pulse is 16 times of its corresponding average current.

$$I_{LED\_AVG} = \frac{I_{LED\_MAX}}{2048} \times 1.149^{(code-1)} \quad (3)$$

Code 1 programs the LED current to 12.21μA with 25mA maximum LED current. Code 0 programs 0 current.

When bit[4] in REG0x11 is set to 1, the ramp function is enabled. Then when bits[7:4] in REG0x19 are not all 0 (I^2C code is from 256 to 4095), the ramp rate is 128μs/step. When bits[7:4] in REG0x19 are all 0 (I^2C code is from 1 to 255), the ramp rate is 1024μs/step. For example, if the code is set from 2000 to 4001, I_{LED_AVG} will change from 12.21mA to 24.42mA, the corresponding ramp rate = 128μs/step, so the ramp time for I_{LED_AVG} = [(4001 - 1) × 0.5 - 2000 × 0.5] × 128μs = 128ms.

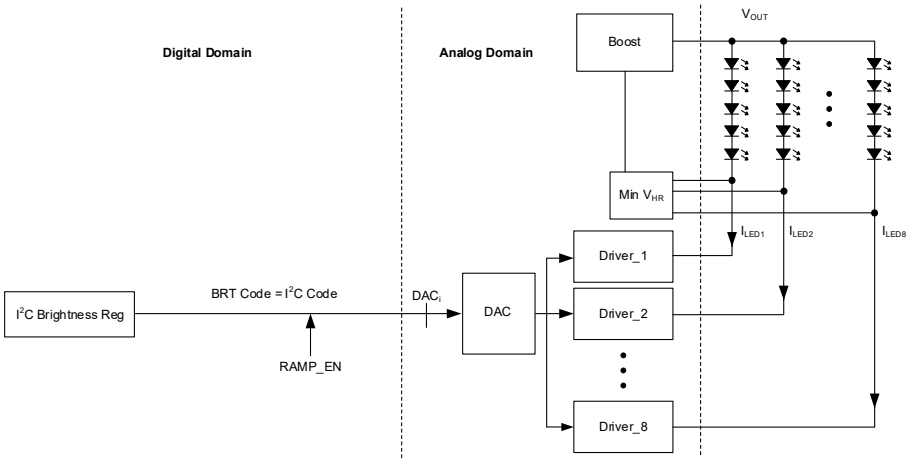


Figure 6. Brightness Control 00 (I^2C Only)

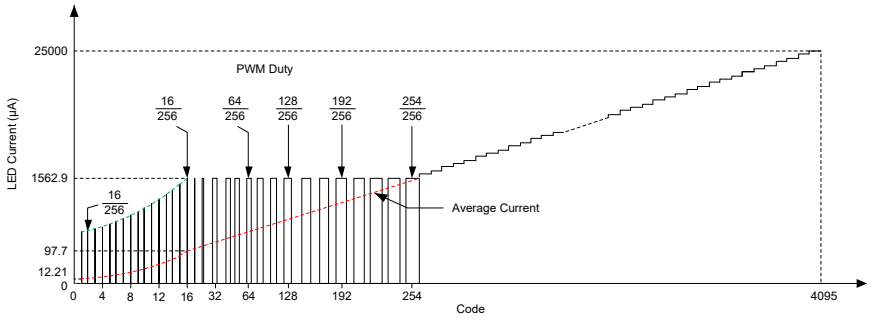


Figure 7. LED Current vs. Brightness Code (Mode 00)

DETAILED DESCRIPTION (continued)

PWM Only (Brightness Mode 01)

In brightness mode 01, only the PWM input sets the brightness. The I^2C code is ignored and forbidden to set to 0. The LED current is proportional with the PWM duty cycle.

When the PWM pin is constantly high, the V_{REF} voltage is regulated to 2048mV typically. When the duty cycle of the input PWM signal is low, the regulation voltage is reduced, and the LED current is reduced; therefore, it achieves LED brightness dimming. The relationship between the duty cycle and V_{REF} regulation voltage is given by Equation 4:

$$V_{REF} = Duty \times 2048mV \quad (4)$$

where
Duty = duty cycle of the PWM signal
2048mV = internal reference voltage

Then the value of V_{REF} is the PWM-based code for brightness dimming. The LED current increases proportionally to input PWM duty and follows the relationship (see Figure 10):

$$I_{LED\_AVG} = I_{LED\_MAX} \times Duty \quad (5)$$

Duty is valid from 1/2048 to 1. There is no ramp function in this mode. The LED current setting time depends on the internal low-pass filter and the bandwidth of the Boost converter.

The user can easily control the WLED brightness by controlling the duty cycle of the PWM signal. The PWM frequency is in the range from 5kHz to 100kHz.

As shown in Figure 8, the IC chops up the internal 2048mV reference voltage at the duty cycle of the PWM signal. The pulse signal is then filtered by an internal low-pass filter. SGM37380YG regulation voltage is independent of the PWM logic voltage level which often has large variations.

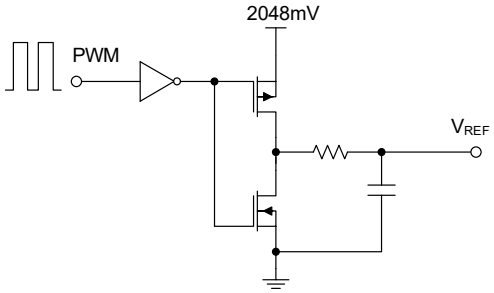


Figure 8. Programmable V_{REF} Using PWM Signal

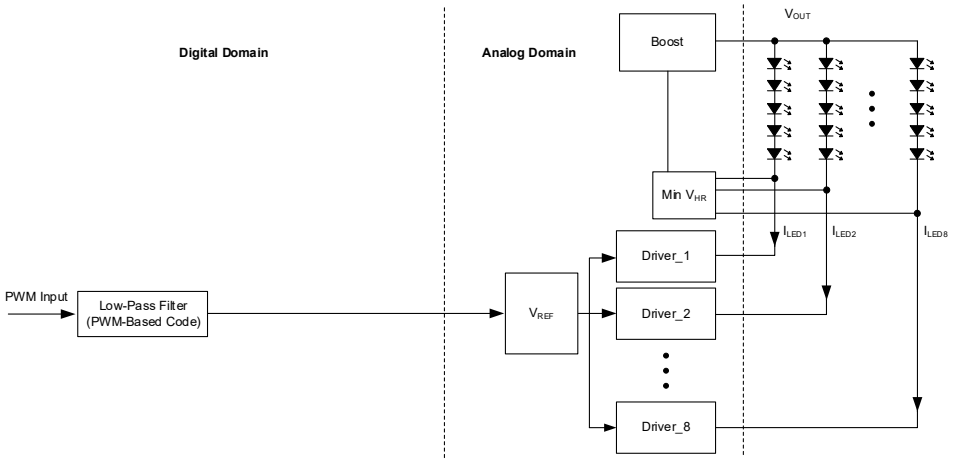


Figure 9. Brightness Control 01 (PWM Only)

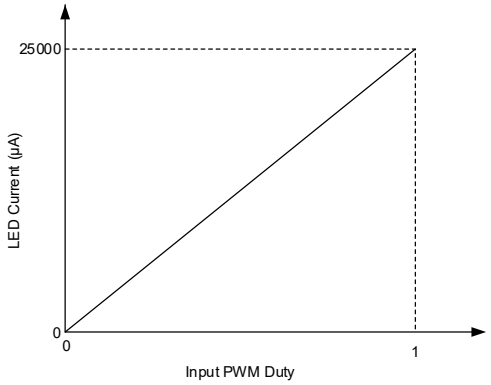


Figure 10. LED Current vs. Input PWM Duty (Mode 01)

DETAILED DESCRIPTION (continued)

I²C × PWM (Brightness Mode 10 or 11)

In brightness control mode 10 or 11 both the I²C code and the PWM duty cycle control the LED current. The brightness code is calculated by PWM duty cycle and the I²C brightness code, and follows the relationship (see Figure 11):

When the I²C code is an odd integer,

BRT_code = (I²C code - 1) × 0.5 × PWM duty cycle (6)

When the I²C code is an even integer,

BRT_code = I²C code × 0.5 × PWM duty cycle (7)

where

BRT_code = the brightness code

I²C code is valid from 0 to 4095. The code should be an integer. In I²C × PWM brightness mode, LED current is disabled when I²C code is 1.

The average LED current increases proportionally to the brightness code and is calculated by Equation 8.

$$I_{LED\_AVG} = \frac{I_{LED\_MAX}}{2048} \times BRT\_code \quad (8)$$

BRT_code is valid from 1 to 2047 and it could be an integer or a decimal. BRT_code 1 programs the LED current to 12.21μA with 25mA maximum LED current. Code 0 programs 0 current.

When bit[4] in REG0x11 is set to 1, the ramp function is enabled. When bits[7:4] in REG0x19 are not all 0 (I²C code is from 256 to 4095), regardless of PWM duty cycle, the ramp rate is 128μs/step. When bits[7:4] in REG0x19 are all 0 (I²C code is from 1 to 255), regardless of PWM duty cycle, the ramp rate is 1024μs/step. For example, if PWM duty cycle is set to 10% and the code is set from 2000 to 4001, when bit[1:0] in REG0x1B is 00, I_{LED_AVG} will change from 1.221mA to 2.442mA, the corresponding ramp rate = 128μs/step, so the ramp time for I_{LED_AVG} = [(4001 - 1) × 0.5 - 2000 × 0.5] × 128μs = 128ms.

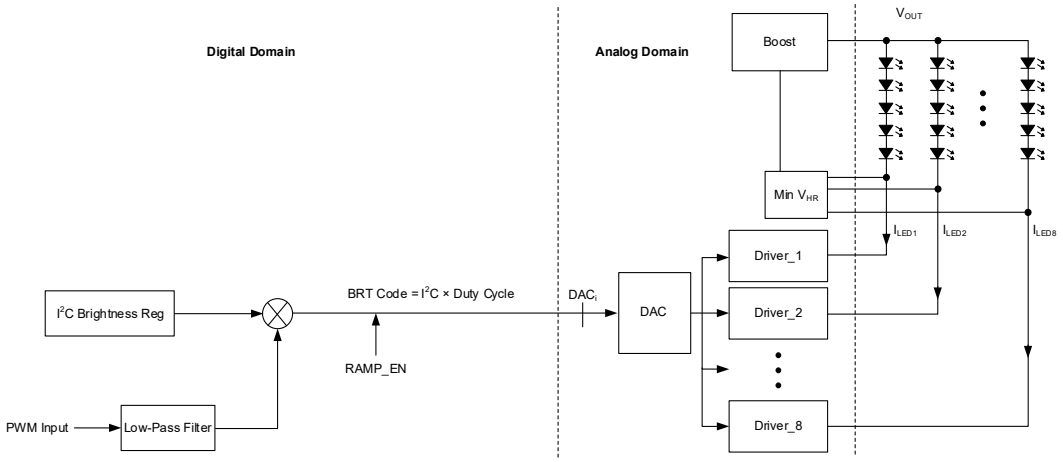


Figure 11. Brightness Control 10 or 11 (I²C × PWM)

DETAILED DESCRIPTION (continued)

Hybrid PWM & I²C Dimming Control

Hybrid PWM & I²C dimming control combines PWM dimming and LED current-dimming control methods. Through this dimming control method, compared to PWM control, better optical efficiency can be achieved. Meanwhile, smooth and accurate control as well as low brightness levels can still be attained. The switch point from current-to-PWM control is set to get the optimal compromise between good matching of the LEDs brightness/white point at low brightness and good optical efficiency. For I²C mode, the LED current enters current-to-PWM control when bits[7:4] in REG0x19 are all 0.

LED Current Transition Time and Ramp

The transition time of two brightness I²C code could be programmed by RAMP_EN. Same ramp time is used for ramp up and ramp down.

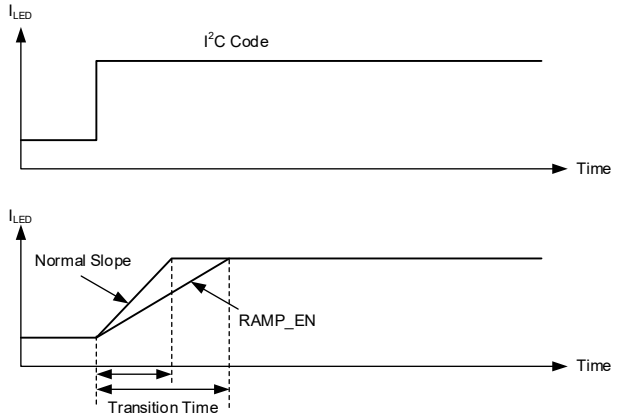


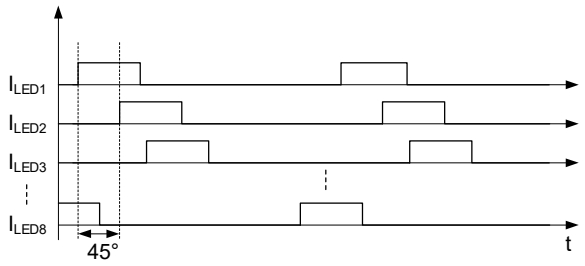
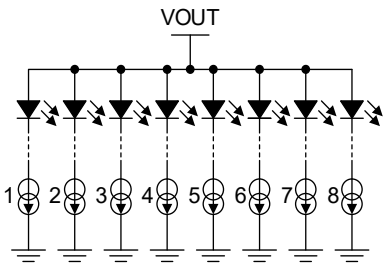
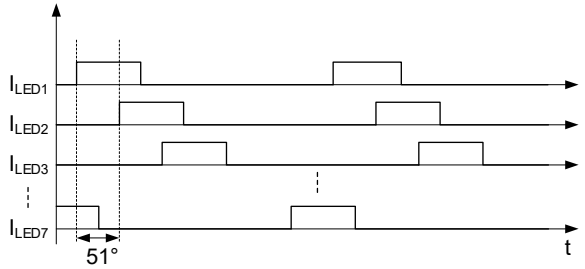
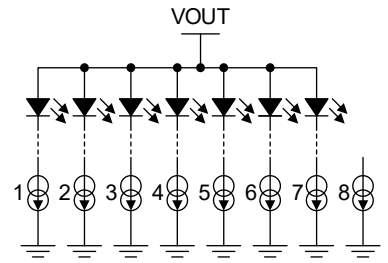
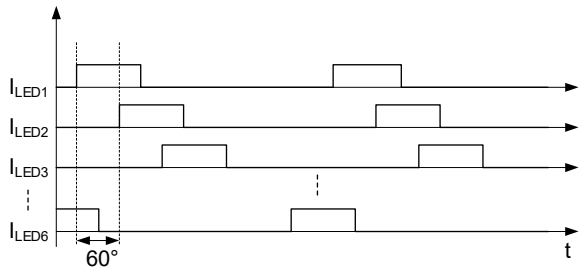
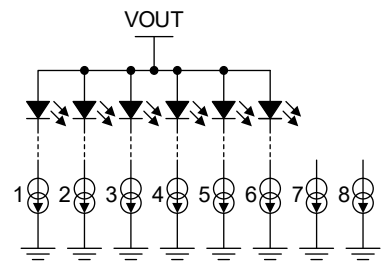
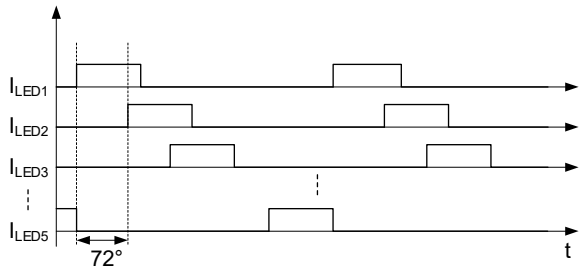
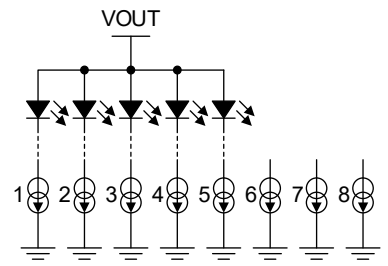
Figure 12. LED Current Transition and Ramp

Phase Shift PWM Scheme

The phase shift PWM (PSPWM) scheme enables an overlapping time when each LED current sink is in an active state. When the LED current sinks are not turned on simultaneously, the peak load current from the Boost output will be significantly reduced. As a result, the ripple on the Boost output is decreased, which makes it possible to use smaller output capacitors. Moreover, the reduction in ripple can also lessen the audible ringing of the output ceramic capacitor. Additionally, the PSPWM scheme can increase the load frequency on the Boost output by as much as eight times, thus shifting the potential audible noise to frequencies that are beyond the audible range.

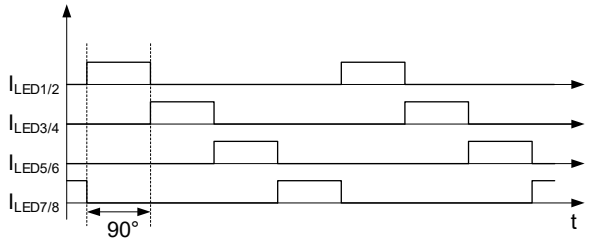
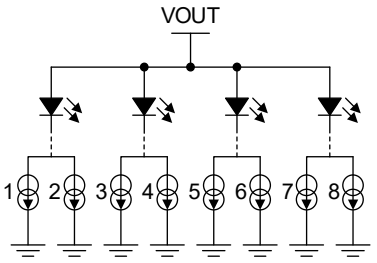
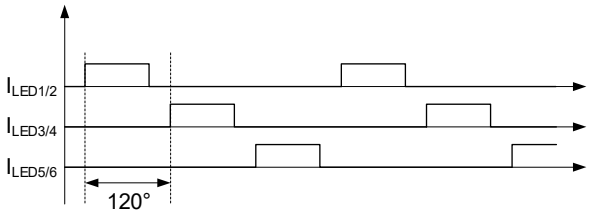
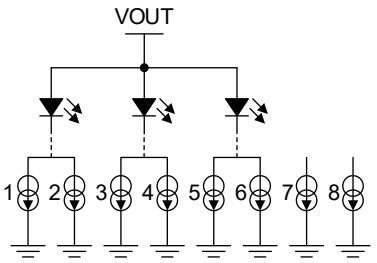
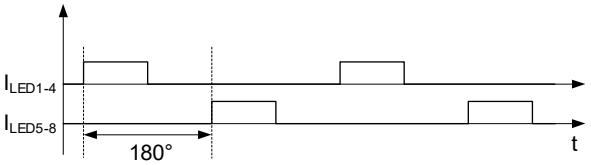
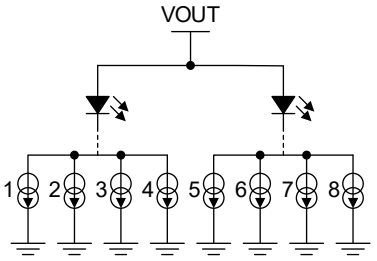
DETAILED DESCRIPTION (continued)

Table 2. Phase Shift PWM Dimming Scheme Diagram

PS_ MODE[2:0]	Typical Waveforms	Connection
000		
	8 LED strings with 45 degree phase shift. One driver for each LED string	
001		
	7 LED strings with 51 degree phase shift. One driver for each LED string	
010		
	6 LED strings with 60 degree phase shift. One driver for each LED string	
011		
	5 LED strings with 72 degree phase shift. One driver for each LED string	

DETAILED DESCRIPTION (continued)

Table 2. Phase Shift PWM Dimming Scheme Diagram (continued)

PS_ MODE[2:0]	Typical Waveforms	Connection
100		
	4 LED strings with 90 degree phase shift. Two drivers for each LED string	
101		
	3 LED strings with 120 degree phase shift. Two drivers for each LED string	
110		
	2 LED strings with 180 degree phase shift. Four drivers for each LED string	
111	No phase shift function	

DETAILED DESCRIPTION (continued)

Fault Protection/Detection

Over-Voltage Protection (OVP)

The OVP function automatically turns off the Boost converter when the output voltage exceeds 31.5V (TYP), thereby protecting the device OUT and SW pins from high voltage damage. The OVP function is usually triggered in two different over-voltage conditions.

Case 1 OVP Fault Only (OVP threshold was triggered and no LED open circuit occurred)

As the number of LEDs per string increases approximately to the maximum number of LEDs per string, the V_{OUT} may approach the OVP threshold in steady state. When the SGM37380YG encounters a fast transient change of V_{IN} or LED current, V_{OUT} may suddenly increase to trigger the OVP threshold. At this point the OVP is triggered and the Boost converter stops working until the output voltage drops to the lower threshold voltage of the OVP. To avoid false triggering, the duration when V_{OUT} is higher than the OVP threshold must be longer than 1ms. In this case, the OVP fault flag (REG0x1F[0]) is set to 1.

Case 2 LED String Open Fault (OVP threshold triggers and an LED open circuit occurs)

When the LED open fault occurs, the Boost converter detects that V_{HR} is lower than 40mV, and the Boost control loop will operate with maximum on-time that results in V_{OUT} to increase, which ultimately results in boost to trigger OVP. At this time, the OVP fault flag (REG0x1F[0]) and the LED open fault flag (REG0x1F[4]) are both set to 1. Then opened LED channel will be disabled internally, and the output voltage is reduced to normal voltage.

Case 3 All LED String Open Fault (OVP threshold triggers and all LED open circuit occurs)

When all LED channels open fault occurs, the Boost converter detects all LED channel V_{HR} is lower than 40mV, and the Boost control loop will operate with maximum on-time that results in V_{OUT} to increase, which ultimately results in boost to trigger OVP. When all LED channels open occurs, the Boost converter is disabled and the output voltage is reduced. At this time, the OVP fault flag (REG0x1F[0]) and the LED open fault flag (REG0x1F[4]) are both set to 1.

LED Short Fault

The SGM37380YG implements LED short fault protection. The device monitors the current sink input voltage. As one channel LED headroom voltage exceeds 4.8V, the device will trigger LED short fault protection. At this time, the fault channel will disable current sinks and other channels work normally. At this time, the short fault flag (REG0x1F[3]) is set to 1.

Over-Current Protection (OCP)

The SGM37380YG has OCP threshold (3.5A, TYP). The device constantly monitors the current flowing through the low-side NFET. When the current exceeds the OCP threshold, the NFET is turned off immediately for the remaining period of the switching period.

When the OCP is continuously triggered, the device sets the OCP fault flag bit (REG0x1F[1]) to 1. The SGM37380YG has a built-in counter that can monitor OCP events over a period of 128μs. If 32 consecutive OCP triggering events occur for 128μs periods, the REG0x1F[1] bit is set to 1, so there is a 4ms blank time more or less.

Over-Temperature Protection (OTP)

When the temperature of the device exceeds +160℃, over-temperature protection (OTP) is triggered, the device stops working, and the OTP Fault flag (REG0x1F[2]) is set to 1. When the temperature of the device drops to +140℃, the device will restart.

LEDx Pin Unused

As shown in Figure 14, user can easily disable the unused channel by connecting its LEDx pin to GND pin or leaving it floating.

DETAILED DESCRIPTION (continued)

I²C Interface

Start and Stop Conditions

A transaction is started by taking control of the bus by master if the bus is free. The transaction is terminated by releasing the bus when the data transfer job is done as shown in Figure 13. All transactions are started by the master which applies a START condition on the bus lines to take over the bus and exchange data. At the end, the master terminates the transaction by applying one (or more) STOP condition. START condition is when SCL is high and a high to low transition on the SDA is generated by master. Similarly, a STOP is defined when SCL is high and SDA goes from low to high. START and STOP are always generated by a master. After a START and before a STOP, the bus is considered busy.

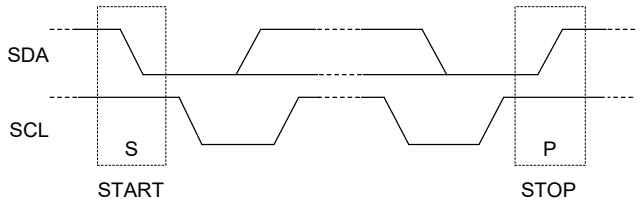


Figure 13. I²C Start and Stop Conditions

I²C Address

The SGM37380YG operates as a slave device with address 0x36 (36H). It has nine 8-bit registers. The first byte sent by master after the START is always the target slave address (7 bits) and an eighth data-direction bit (R/$\overline{W}$). R/$\overline{W}$ bit is 0 for a WRITE transaction and 1 for READ (when master is asking for data). Data direction is the same for all next bytes of the transaction. To reverse it, a new START or repeated START condition must be sent by master (STOP will end the transaction). Usually the second byte is a WRITE sending the register address that is supposed to be accessed in the next byte(s). The third byte contains the data for the selected register.

Byte Format

Data is transmitted in 8-bit packets (one byte at a time). The number of bytes in one transaction is not limited. In each packet, the 8 bits are sent successively with the Most Significant Bit (MSB) first. An acknowledge (or not-acknowledge) bit must come after the 8 data bits. This bit informs the transmitter whether the receiver is ready to proceed for the next byte or not. If the slave is busy and cannot transfer another byte of data, it can hold the SCL line low and keep the master in a wait state. When the slave is ready for another byte of data, it releases the clock line and data transfer can continue with clocks generated by master.

APPLICATION INFORMATION

The SGM37380YG is a high-precision and small-size LED backlight driver solution for consumer applications such as tablet or laptop computers. The device implements the Boost converter plus current sink architecture, which can effectively support multi-string LED backlight panels while supporting high precision dimming.

Component Selection

Inductor

The selection of inductors is mainly concerned with saturation current value and inductance value. The saturation current value of the inductor should be higher than the inductive current peak (I_{PEAK}) under the worst conditions with a 30% margin. The worst case peak inductor current occurs at the minimum input voltage, minimum switching frequency, maximum output voltage and maximum load current. When the application has high transmission efficiency requirements, the peak current should be reduced as much as possible to decrease loss. I_{PEAK} can be estimated using Equation 9:

$$I_{PEAK} = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times \eta} + \frac{V_{IN}}{2 \times f_{SW} \times L} \times (1 - \frac{V_{IN} \times \eta}{V_{OUT}}) \quad (9)$$

In addition, in order to ensure the normal operation of OCP function, the inductance peak current I_{PEAK} should be lower than the OCP threshold. Table 3 lists the recommended inductance that can be used in different applications.

Output Capacitor

To ensure the stability over the entire operating range, the recommended effective output ceramic capacitance should be higher than 0.4μF. Considering the potential tolerance, temperature, and DC derating of the ceramic capacitor, it is recommended to use a 2.2μF to 10μF ceramic capacitor as the output ceramic capacitor.

Table 5 lists possible output capacitors that can be used.

Equation 10 determines the effective output voltage range of the selected capacitor:

$$\text{DC Voltage Derating} \geq \frac{0.38\mu F}{(1 - TOL) \times (1 - TEMP\_CO)} \quad (10)$$

For example, when the tolerance is 10% and the temperature coefficient is 15%, DC voltage derating ≥ 0.5μF. Typically, the capacitors in Table 5 are sufficient to meet the needs of most LED backlight driver applications. When larger capacity capacitors or greater system stability are required, two ceramic capacitors can be connected in parallel.

Input Capacitor

The recommended input capacitor is 2.2μF ceramic capacitor for battery application, which should be placed as close as possible to the IN pin of the device to be used as a filter for the input power supply.

Typical Application

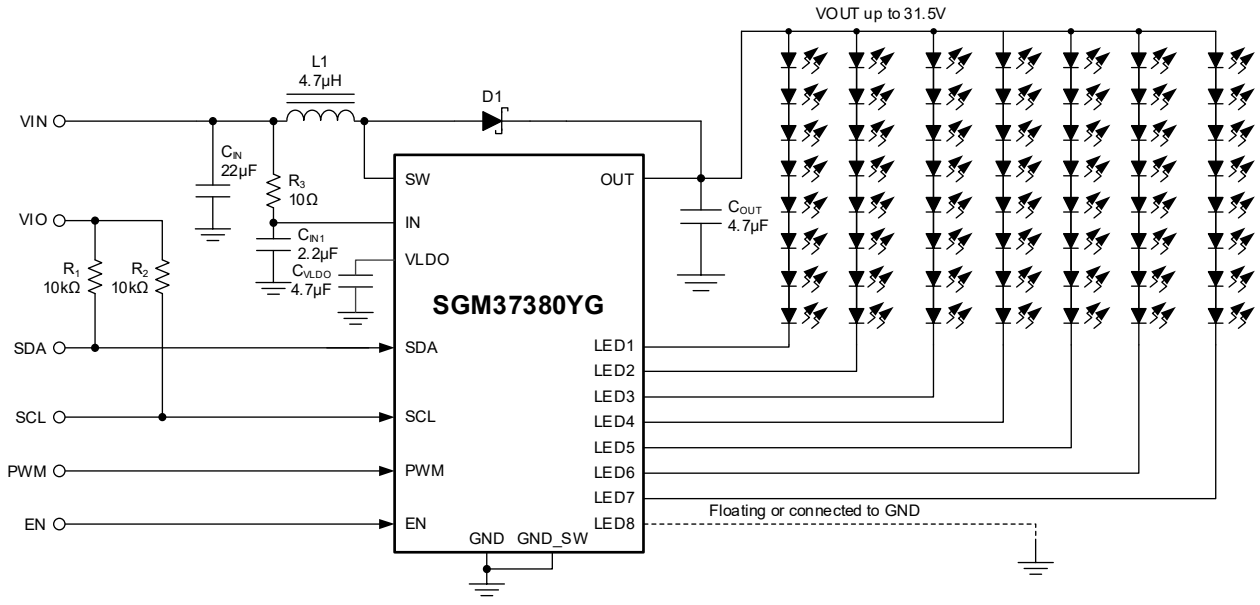


Figure 14. Typical Application for Seven LED Strings

APPLICATION INFORMATION (continued)

Recommended Inductance for the Boost Power Stage

For Boost converter, choosing an inductor with a small size usually results in a higher DCR (DC resistance). The inductor's DCR limits the Boost converter's maximum voltage, and the higher temperature rise caused by the inductor further reduces the output power of the Boost converter. The table below shows the recommended small inductor size solution for 8 LED strings and 9 LEDs per strings. The maximum LED current per string is 25mA by default and the maximum LED forward voltage is 2.9V.

Table 3. Typical Application Component List

Number of LED Strings	Number of LEDs per String	Input Voltage Range	L1		
			f_{SW} = 1225kHz	f_{SW} = 650kHz	f_{SW} = 350kHz
8	10	2.7V ~ 4.4V	4.7μH ~ 6.8μH	6.8μH ~ 10μH	10μH ~ 15μH
		5.4V ~ 8.8V	6.8μH ~ 10μH	8.2μH ~ 10μH	10μH ~ 15μH
8	9	2.7V ~ 4.4V	4.7μH ~ 6.8μH	6.8μH ~ 10μH	8.2μH ~ 10μH
		5.4V ~ 8.8V	6.8μH ~ 10μH	8.2μH ~ 10μH	8.2μH ~ 10μH
6	10	2.7V ~ 4.4V	3.3μH ~ 4.7μH	4.7μH ~ 6.8μH	6.8μH ~ 10μH
		5.4V ~ 8.8V	6.8μH ~ 10μH	6.8μH ~ 10μH	6.8μH ~ 10μH
6	9	2.7V ~ 4.4V	3.3μH ~ 4.7μH	4.7μH ~ 6.8μH	6.8μH ~ 10μH
		5.4V ~ 8.8V	6.8μH ~ 10μH	6.8μH ~ 10μH	6.8μH ~ 10μH

Table 4. Small Size Inductance Application Recommended List

Input Voltage Range	Switch Frequency	Inductance	Part Number	DCR	Size (W*L*H)	Manufacturer
3V ~ 4.4V	1225kHz	4.7μH	HTEQ041B-4R7MSR	85mΩ	4*4*1.2[mm]	CYNTEC
			WCX0412C4R7MT	90mΩ	4*4*1.2[mm]	Sunlord

Recommended Capacitance for the Boost

Table 5. Recommended Capacitors for Battery Application

Switching Frequency	C_{IN}	C_{OUT}	C_{VLDO}
1225kHz	2.2μF	4.7μF	4.7μF
650kHz	2.2μF	4.7μF	4.7μF
350kHz	4.7μF	10μF	4.7μF

LAYOUT

Layout Guidelines

Due to the presence of parasitic inductors and capacitors of the circuit board, SW pin of the Boost converter will exhibit spike voltage, which may cause damage to the device. In addition, parasitic parameters in the layout of the circuit board can also cause a surge in the circuit flowing through the Schottky diode and the output capacitor, which poses a threat to the power device. Figure 15 shows the analysis of the PCB parasitics that generate the undesired voltage spikes. The voltage spike of SW and the high pulse current through the Schottky diode can be effectively suppressed by reasonable circuit board layout design.

The good layout practice of SGM37380YG can follow the conventional Boost converter. The current loop from the Schottky diode to the output capacitor return to the IC's ground pin should be as small as possible. In addition, in order to minimize the radiation of the SW node, the area of the SW node should be reduced as much as possible, while keeping the SW node away from other traces. The input capacitor should be placed as close as possible to the IN pin of the device to provide a stable device power supply.

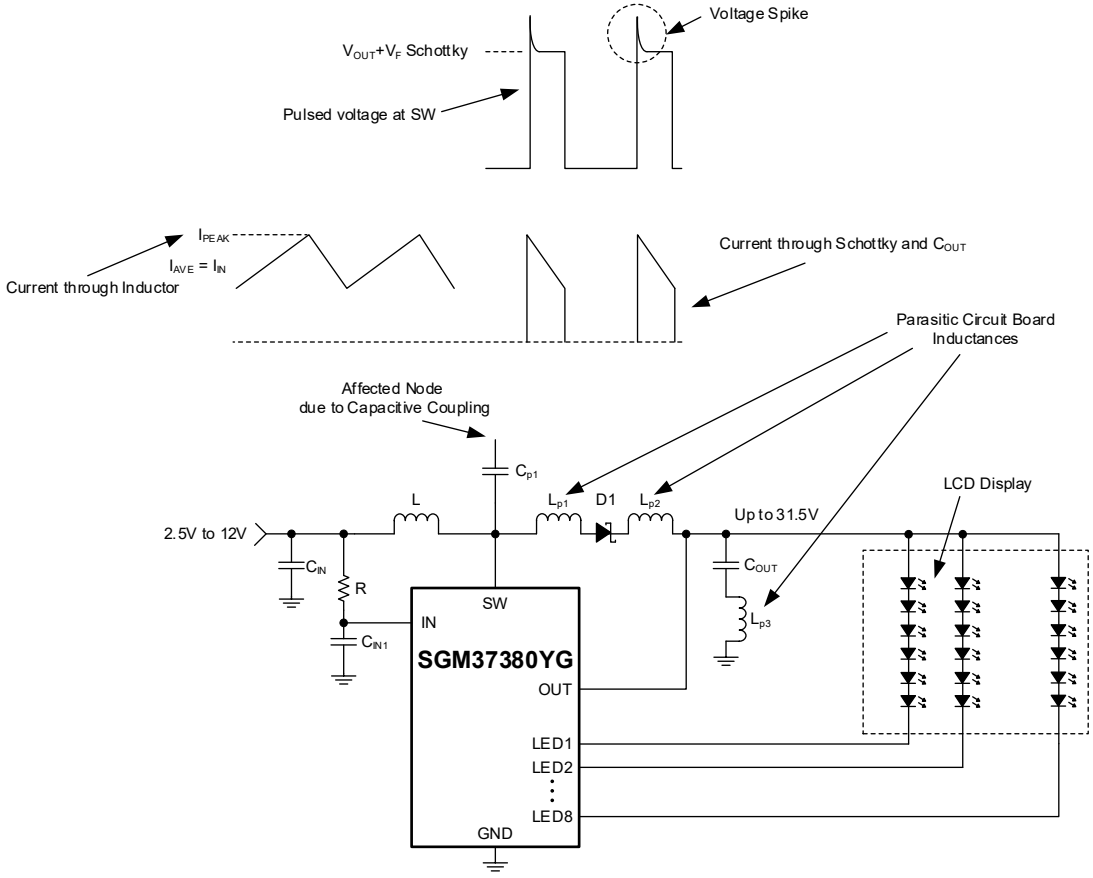


Figure 15. SW Pin Voltage (High Dv/Dt) and Current through Schottky Diode and C_{OUT} (High Di/Dt)

LAYOUT (continued)

Boost Output Capacitor Placement

In the Boost converter, whenever the NMOS is turned off and the Schottky diode is forward biased, both the output capacitor and the Schottky diode detect a high current pulse from 0 to I_{PEAK}. The current path of the output loop starts from the SW node, then passes through the Schottky diode and output capacitor, and finally returns to the GND pin of the SGM37380YG. The circuit board layout parasitic parameter will cause the SW voltage spike and the high current pulsation of the Schottky diode. In order to reduce this effect, the area surrounding the SW pin, Schottky diode and output capacitor should be minimized as much as possible, so as to reduce the influence caused by parasitic parameters. The output capacitor should be placed on the same layer as the SGM37380YG to avoid interference to the output current loop caused by parasitic inductance caused by the through hole.

Schottky Diode Placement

Similar to output capacitors, Schottky diodes are in the current discharge loop. Therefore, parasitic parameters in the board layout can cause SW voltage spike and Schottky diode high current pulsation. The area surrounding the SW pin, Schottky diode and output capacitance of SGM37380YG should be minimized as much as possible to reduce the influence caused by parasitic parameters. Besides, Schottky diodes should be arranged in the same layer as the SGM37380YG.

Inductor Placement

The inductor is an important part of the Boost converter. It is connected to the SGM37380YG at the SW node. The SW node has a large dV/dt, and the SW node voltage will jump between 0 and V_{SW_PEAK} when the NMOS is turned on and off. When the SW voltage is coupled to nearby nodes through parasitic capacitors on the circuit board, it may cause interference to other key traces. For this purpose, the area of the SW node needs to be reduced as much as possible. That is to say, the inductor and the anode of the Schottky diode are as close to the SW node as possible, and the SW node is away from other critical traces. In addition, the inductance flows through a large input current, so any parasitic resistance along the path will cause the SGM37380YG input voltage dropping, which reduces the efficiency and the input operating voltage range. The input capacitor should be as close to the inductor as possible to reduce the parasitic resistance on the input power line.

Boost Input Capacitor Placement

The input capacitor of SGM37380YG is used to filter the input power supply. In order to ensure the stability of the power supply of SGM37380YG, the input capacitor should be as close as possible to the IN pin of the device to avoid voltage spikes in the IN pin caused by parasitic parameters, which may affect the normal operation of SGM37380YG.

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

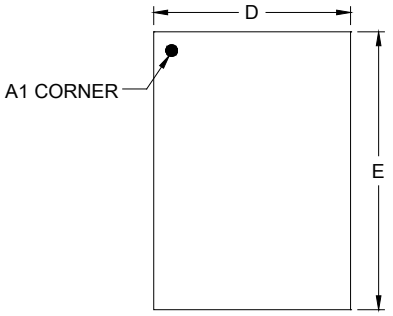
FEBRUARY 2026 – REV.A to REV.A.1	**Page**
Changed and Added Register Maps section	13
Changed and Added Detailed Description section	16

DECEMBER 2025 – REV.A to REV.A.1	**Page**
Changed and Deleted Detailed Description section	18 ~ 21

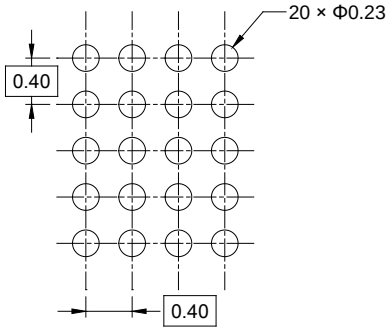
Changes from Original to REV.A (NOVEMBER 2025)	**Page**
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

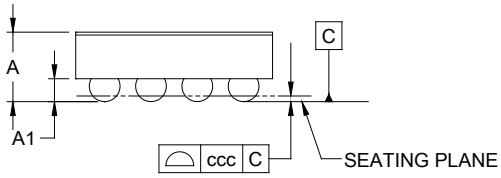
WLCSP-1.7×2.4-20B



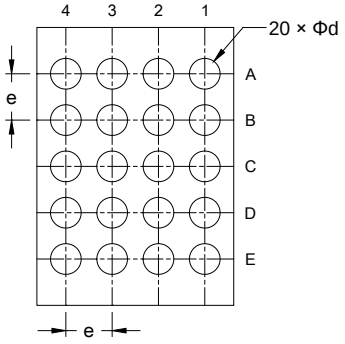
TOP VIEW



RECOMMENDED LAND PATTERN (Unit: mm)



SIDE VIEW



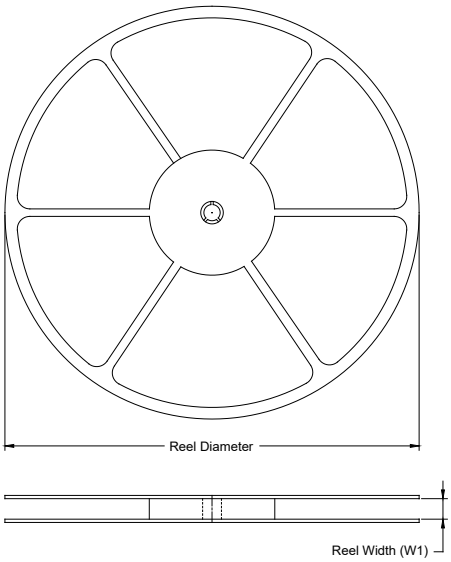
BOTTOM VIEW

Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	-	-	0.645
A1	0.178	-	0.218
D	1.670	-	1.730
E	2.370	-	2.430
d	0.235	-	0.295
e	0.400 BSC		
ccc	0.050		

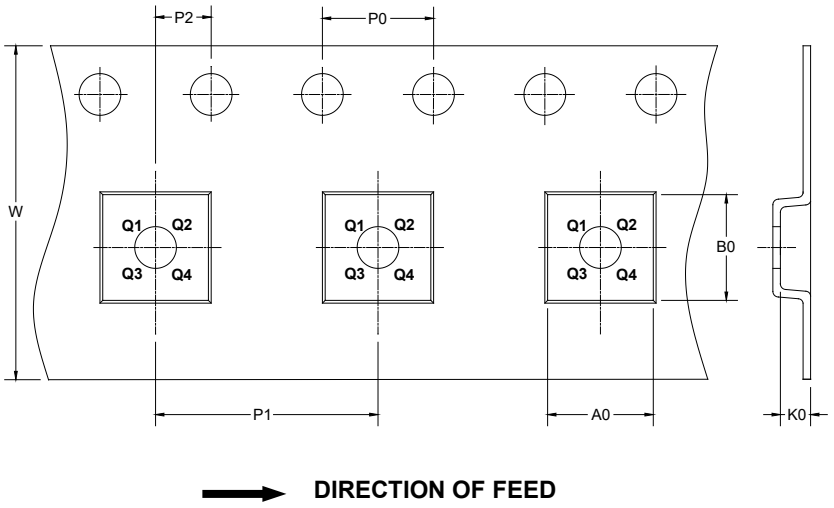
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



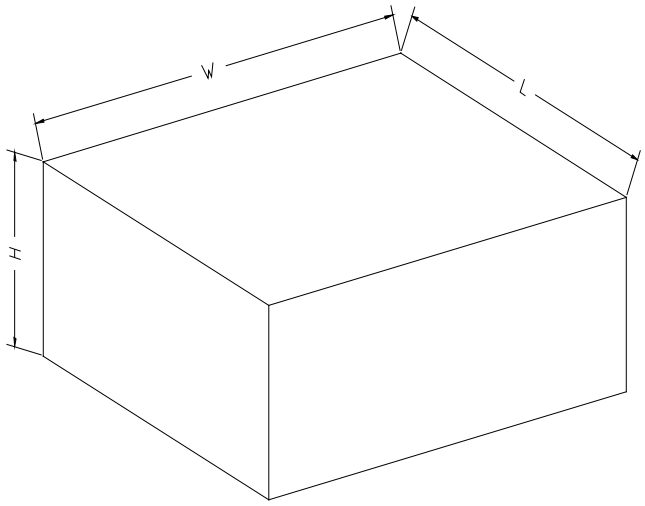
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
WLCSP-1.7×2.4-20B	7"	9.5	1.83	2.49	0.76	4.0	4.0	2.0	8.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18

DD0002