SGM25712Q
Automotive High-side ORing FET Controller

GENERAL DESCRIPTION

The SGM25712Q is a high-side ORing FET controller. This controller, combined with an external MOSFET, can function as an ideal diode rectifier when inserted in series with the power path.

By substituting conventional diode rectifiers within power distribution infrastructure, this controller minimizes energy dissipation and voltage differentials across the circuit.

The SGM25712Q device integrates a charge pump-driven gate driver for external N-MOSFETs alongside a rapid comparator to disable the FET during reverse current events. It operates across a 4V to 72V supply range and accommodates transient voltages as high as 75V.

The device is AEC-Q100 qualified (Automotive Electronics Council (AEC) standard Q100 Grade 1) and it is suitable for automotive applications.

The SGM25712Q is available in a Green SOT-23-6 package.

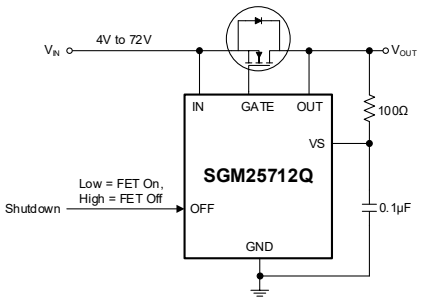
FEATURES

- **AEC-Q100 Qualified for Automotive Applications**
  Device Temperature Grade 1
  T_A = -40℃ to +125℃
- **Functional Safety Capable**
  - **Documentation Available to Aid Functional Safety System Design**
- **Wide Operating Input Voltage Range, V_{IN}: 2V to 72V (V_{BIAS} Required for V_{IN} < 4V)**
- **Transient Capability: 75V**
- **External N-Channel MOSFET Gate Driver with Charge Pump Circuitry**
- **Fast 37ns Response to Current Reversal**
- **1.8A Peak Gate Turn-Off Current**
- **Minimum V_{DS} Clamping Circuit with Enhanced Turn-Off Speed**
- **Available in a Green SOT-23-6 Package**

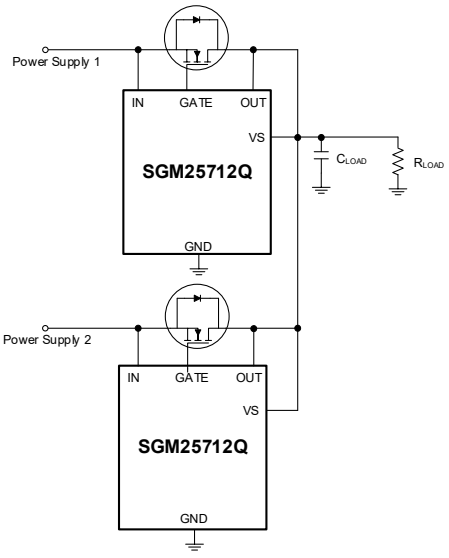
APPLICATIONS

Active ORing of Redundant (N+1)
Power Supplies
Automotive Applications

TYPICAL APPLICATION



Full Application



Typical Redundant Supply Configuration

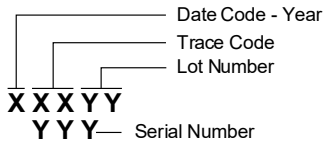
Figure 1. Typical Application Circuit

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE TOP MARKING	PACKING OPTION
SGM25712Q	SOT-23-6	-40℃ to +125℃	SGM25712QN6G/TR	XXXYY 2CJ	Tape and Reel, 3000

MARKING INFORMATION

NOTE: XXX = Date Code and Trace Code. YY = Lot Number.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

IN, OUT Pins to Ground (1) ..... -0.3V to 75V
GATE Pin to Ground (1) ..... -0.3V to 78V
VS Pin to Ground ..... -0.3V to 75V
OFF Pin to Ground ..... -0.3V to 7V
Package Thermal Resistance
SOT-23-6, θ_{JA} ..... 149.7℃/W
SOT-23-6, θ_{JB} ..... 39.1℃/W
SOT-23-6, θ_{JC} ..... 88℃/W
Package Thermal Characterization Parameter
SOT-23-6, ψ_{JT} ..... 19.7℃/W
SOT-23-6, ψ_{JB} ..... 38.1℃/W
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility (2) (3)
HBM ..... ±4000V
CDM ..... ±1000V

NOTES:

1. When the SGM25712Q is active (OFF pin open/low and V_{IN} > V_{OUT}), the GATE pin typically maintains a 12V voltage differential above the IN pin.

2. For human body model (HBM), all pins comply with AEC-Q100-002 specification.

3. For charged device model (CDM), all pins comply with AEC-Q100-011 specification.

RECOMMENDED OPERATING CONDITIONS

IN, OUT, VS Pins (24-Hour) ..... 4V to 72V
IN, OUT, VS Pins ..... 4V to 65V
OFF Pin ..... 0V to 5.5V
Operating Junction Temperature Range ..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

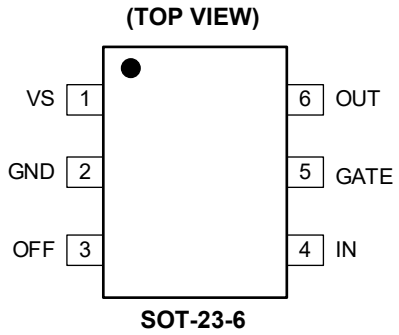
ESD SENSITIVITY CAUTION

This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION



PIN DESCRIPTION

PIN	NAME	FUNCTION
1	VS	The main supply pin delivers primary power for internal biasing and auxiliary power for the gate driver charge pump, typically connected to OUT or IN but adaptable to a dedicated supply when required.
2	GND	Ground.
3	OFF	Shutdown control for the external MOSFET, active high. A high level switches the gate off, so the load current continues through the body diode; a low level leaves the gate under normal drive. Leave the pin open or connect it to GND if the function is not used.
4	IN	The voltage-sensing connection should connect to the external MOSFET's source pin.
5	GATE	The pin interfaces with the external MOSFET's gate, regulating its state to mimic a low-forward voltage diode's behavior.
6	OUT	The voltage-sensing connection should connect to the external MOSFET's drain pin.

ELECTRICAL CHARACTERISTICS

(T_A = -40℃ to +125℃, V_{IN} = 12V, V_S = V_{IN}, V_{OUT} = V_{IN}, V_{OFF} = 0V, C_{GATE} = 47nF, typical values are at T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
VS Pin						
Operating Supply Voltage Range	V_S		4		72	V
Operating Supply Current	I_{VS}	V_S = 4V, V_{IN} = 4V, V_{OUT} = V_{IN} - 100mV		81	140	μA
		V_S = 12V, V_{IN} = 12V, V_{OUT} = V_{IN} - 100mV		98	160	
		V_S = 72V, V_{IN} = 72V, V_{OUT} = V_{IN} - 100mV		106	170	
IN Pin						
Operating Input Voltage Range	V_{IN}		4		72	V
IN Pin Current	I_{IN}	V_{IN} = 4V, V_S = V_{IN}, V_{OUT} = V_{IN} - 100mV, GATE = open	12	20	28	μA
		V_{IN} = 12V to 72V, V_S = V_{IN}, V_{OUT} = V_{IN} - 100mV, GATE = open	12	24	37	
OUT Pin						
Operating Output Voltage Range	V_{OUT}		4		72	V
OUT Pin Current	I_{OUT}	V_{IN} = 4V to 72V, V_S = V_{IN}, V_{OUT} = V_{IN} - 100mV		11	16	μA
GATE Pin						
Gate Pin Source Current	I_{GATE_ON}	V_{IN} = 4V, V_S = V_{IN}, V_{GATE} = V_{IN}, V_{OUT} = V_{IN} - 175mV	12	34	56	μA
		V_{IN} = 12V to 72V, V_S = V_{IN}, V_{GATE} = V_{IN}, V_{OUT} = V_{IN} - 175mV	12	34	56	
V_{GATE} - V_{IN} in Forward Operation (1)	V_{GS}	V_{IN} = 4V, V_S = V_{IN}, V_{OUT} = V_{IN} - 175mV	10	11	12	V
		V_{IN} = 12V to 72V, V_S = V_{IN}, V_{OUT} = V_{IN} - 175mV	11	12	13	
Gate Capacitance Discharge Time at Forward to Reverse Transition	t_{GATE_REV}	C_{GATE} = 0nF (2)		37	85 (3)	ns
		C_{GATE} = 10nF (2)		80		
		C_{GATE} = 47nF (2)		220	450	
Gate Capacitance Discharge Time at OFF Pin Low to High Transition	t_{GATE_OFF}	C_{GATE} = 47nF (4)		378		ns
Gate Pin Sink Current	I_{GATE_OFF}	V_{GATE} = V_{IN} + 3V, V_{OUT} > V_{IN} + 100mV, t ≤ 10ms	1.0	1.8		A
Reverse V_{SD} Threshold	V_{SD_REV}	V_{IN} - V_{OUT}	-48	-26	-3	mV
Reverse V_{SD} Hysteresis	ΔV_{SD_REV}			12		mV
Regulated Forward V_{SD} Threshold V_{IN} > V_{OUT}	V_{SD_REG}	V_{IN} = 4V, V_S = V_{IN}	10	22	37	mV
		V_{IN} = 12V, V_S = V_{IN}	10	22	37	
OFF Pin						
OFF Input High Threshold Voltage	V_{OFF_IH}	V_{OUT} = V_{IN} - 500mV, V_{OFF} rising		1.57	1.75	V
OFF Input Low Threshold Voltage	V_{OFF_IL}	V_{OUT} = V_{IN} - 500mV, V_{OFF} falling	1.1	1.41		V
OFF Threshold Voltage Hysteresis	ΔV_{OFF}	V_{OFF_IH} - V_{OFF_IL}		163		mV
OFF Pin Internal Pull-Down	I_{OFF}	V_{OFF} = 4.5V	2	5	8	μA
		V_{OFF} = 5V		5		

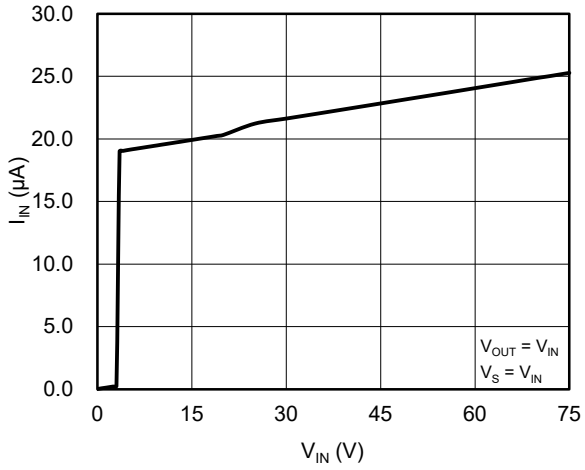
NOTES:

1. Measurement of V_{GS} (V_{GATE} - V_{IN}) includes 1MΩ in parallel with C_{GATE}.
2. The time required for the GATE voltage to drop to V_{IN} + 1V after a (V_{IN} - V_{OUT}) transition from 200mV to -500mV. See Figure 2.
3. Guaranteed by design, not tested in production.
4. The time required for the GATE voltage to reach V_{IN} + 1V after a V_{OFF} transition from 0V to 4V. See Figure 3.

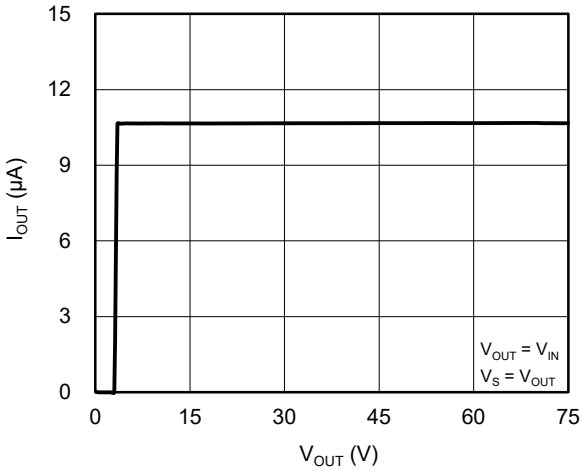
TYPICAL PERFORMANCE CHARACTERISTICS

V_S = 12V, V_{IN} = 12V, V_{OFF} = 0V, and T_A = +25℃, unless otherwise noted.

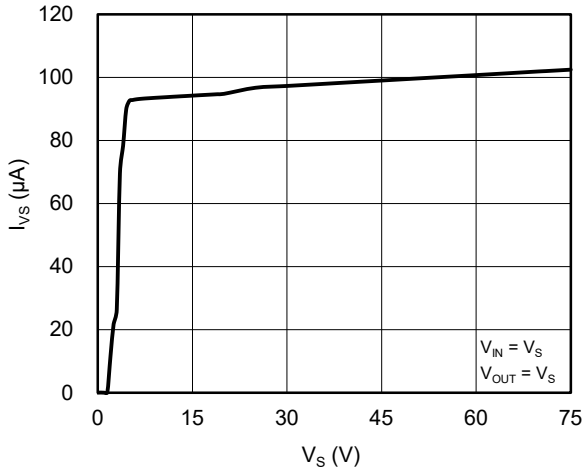
I_{IN} vs. V_{IN}



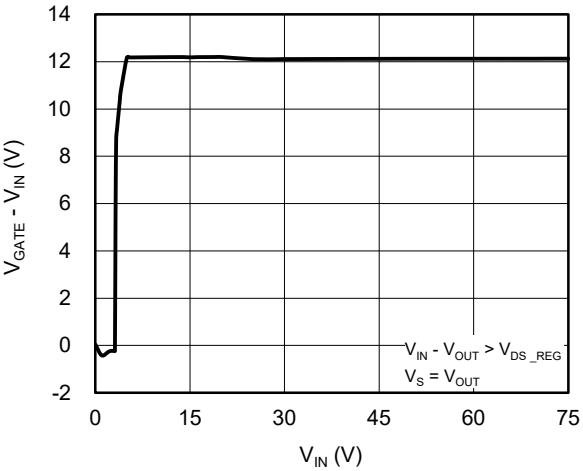
I_{OUT} vs. V_{OUT}



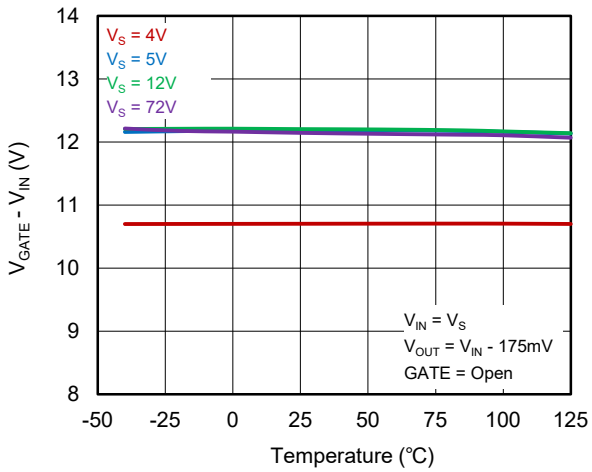
I_{VS} vs. V_S



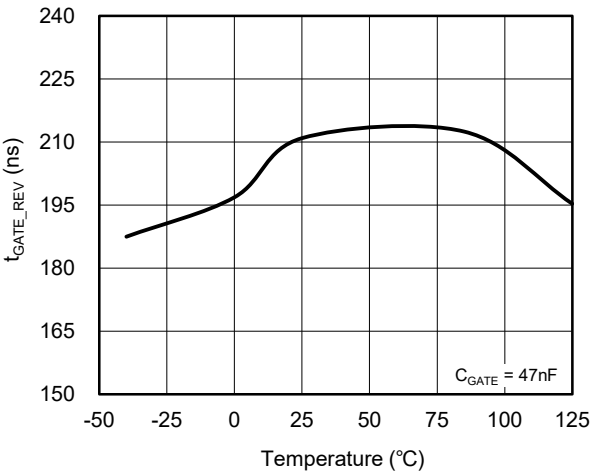
(V_{GATE} - V_{IN}) vs. V_{IN}



V_{GATE} - V_{IN} vs. Temperature



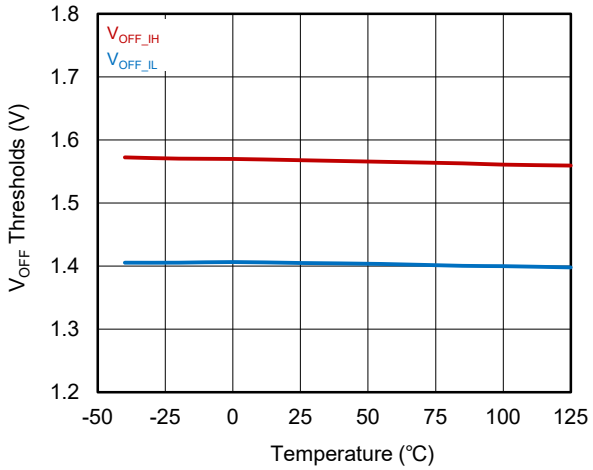
t_{GATE_REV} vs. Temperature



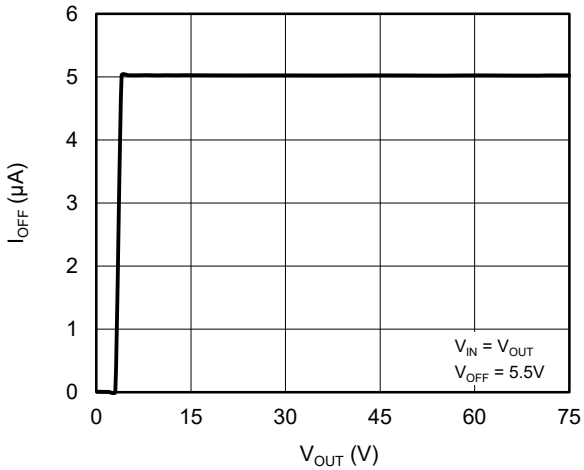
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

V_S = 12V, V_{IN} = 12V, V_{OFF} = 0V, and T_A = +25℃, unless otherwise noted.

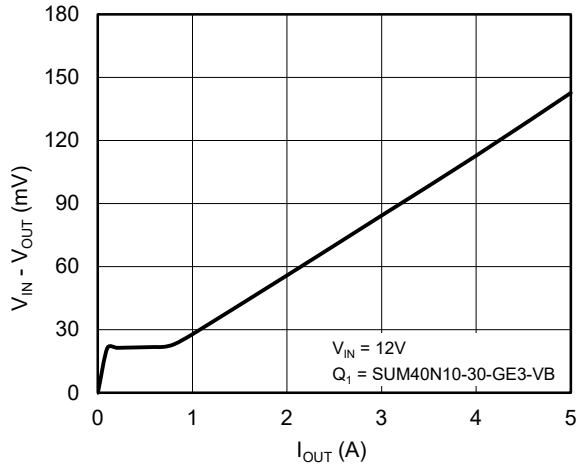
OFF Pin Thresholds vs. Temperature



OFF Pin Internal Pull-Down vs. V_{OUT}



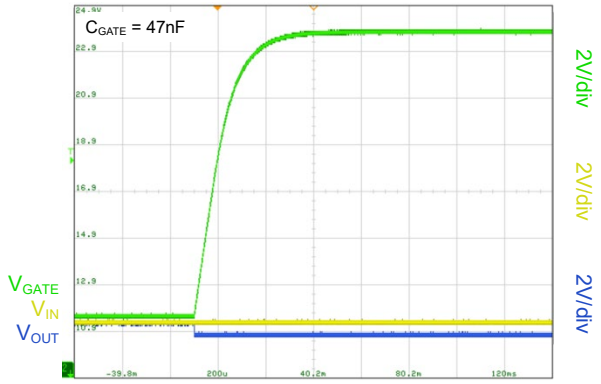
V_{IN} - V_{OUT} vs. I_{OUT}



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

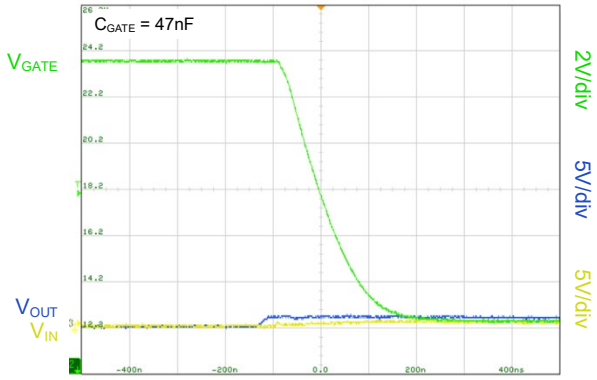
V_S = 12V, V_{IN} = 12V, V_{OFF} = 0V, and T_A = +25℃, unless otherwise noted.

Forward C_{GATE} Charge Time



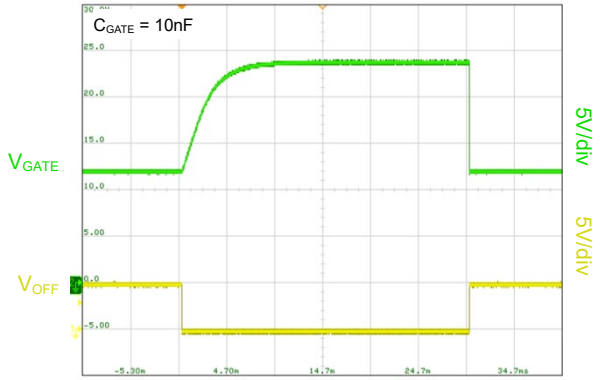
Time (20ms/div)

Reverse C_{GATE} Discharge



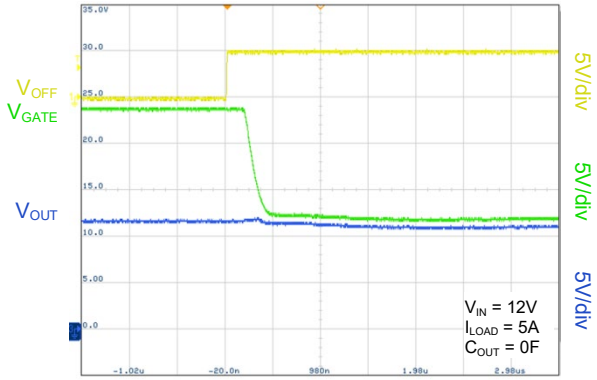
Time (100ns/div)

C_{GATE} Charge and Discharge vs. OFF Pin



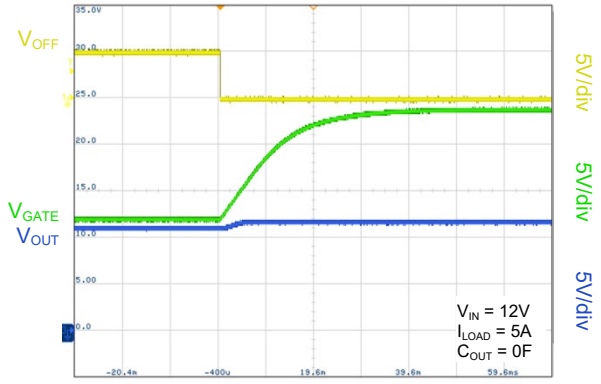
Time (5ms/div)

OFF Pin, On to Off Transition



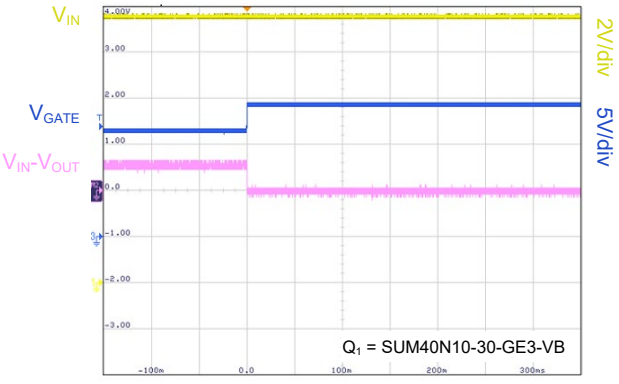
Time (500ns/div)

OFF Pin, Off to On Transition



Time (10ms/div)

Forward Voltage (V_{IN}-V_{OUT}) Drop Reduces When Gate is Enabled (V_{IN} = 12V)

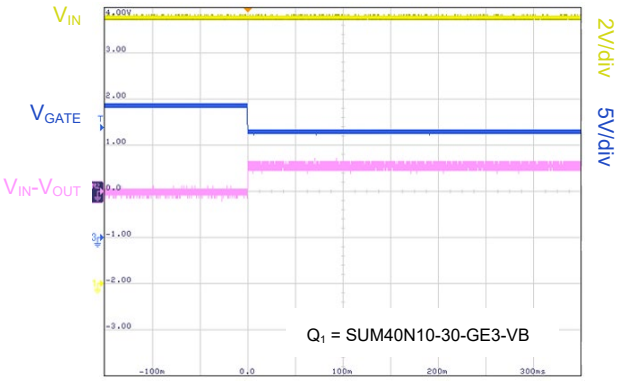


Time (50ms/div)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

V_S = 12V, V_{IN} = 12V, V_{OFF} = 0V, and T_A = +25℃, unless otherwise noted.

Forward Voltage (V_{IN}-V_{OUT}) Drop Increases
When Gate is Disabled (V_{IN} = 12V)



Time (50ms/div)

TIMING DIAGRAMS

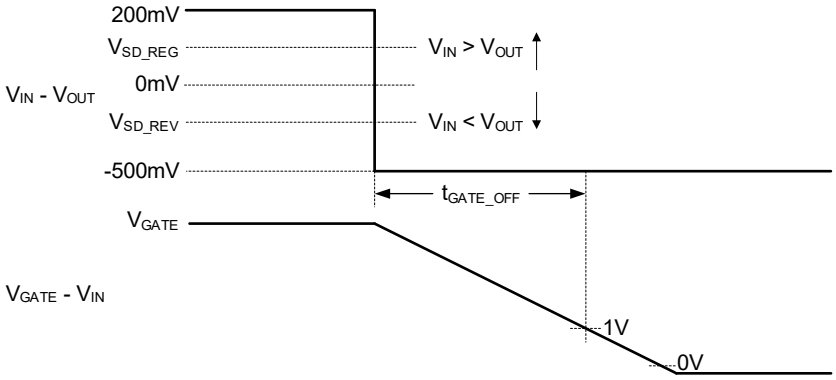


Figure 2. Forward to Reverse Transition Gate Off Timing Diagram

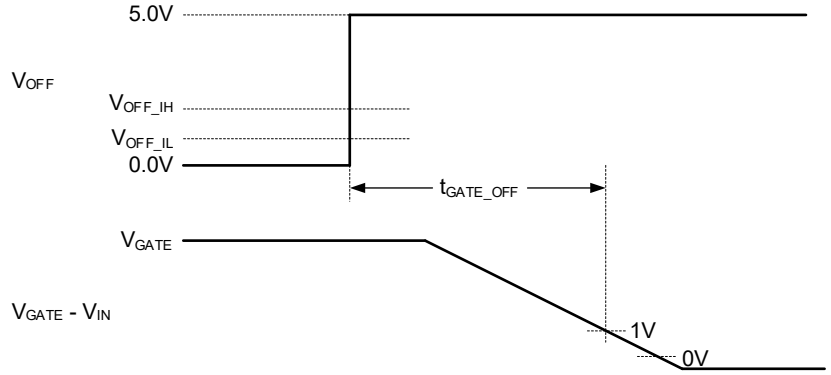


Figure 3. OFF Pin Low to High Transition Gate Off Timing Diagram

FUNCTIONAL BLOCK DIAGRAM

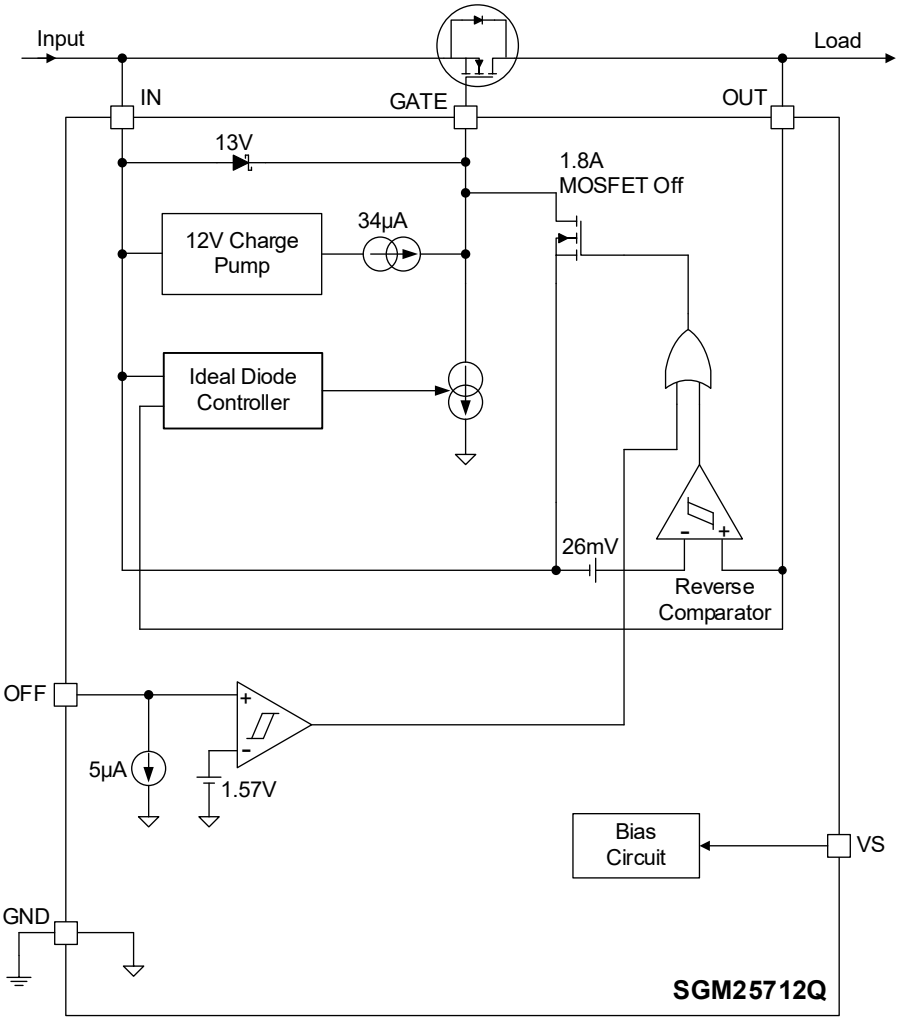


Figure 4. Block Diagram

DETAILED DESCRIPTION

Overview

Blocking diodes are typically series-connected to power supply inputs to enable redundant power source "ORing" and prevent reverse polarity faults. The SGM25712Q substitutes these diodes with an N-MOSFET, lowering both voltage drop and power loss compared to passive solutions. This advantage is particularly significant in low-voltage applications where minimized forward voltage drop becomes critical. The device functions between 4V and 72V and can withstand an absolute maximum of 75V without being damaged. A typical 12V/15A ideal diode configuration is illustrated in Figure 8. Beyond the main MOSFET (Q_1), additional external components are required to address inherent challenges of ideal diode operation. Like traditional diodes, ideal diodes exhibit reverse-recovery behavior, which, when combined with parasitic or intentional inductance, can induce voltage spikes during reverse-current shutdown. Diodes D_1/D_2 and resistor R1 form a protection circuit to suppress these spikes, which could otherwise exceed the SGM25712Q's 75V voltage rating. The output capacitor (COUT) further dissipates energy from reverse-recovery events. Comprehensive analysis of spike mitigation strategies and short-circuit scenarios is provided in the Short-Circuit Failure of an Input Supply" part of the datasheet.

Feature Description

IN, GATE, and OUT Pins

Upon initial power application, the load current passes via the MOSFET's body diode from source to drain. As soon as the voltage over the body diode (V_{SD}) exceeds the V_{SD_REG} threshold, the SGM25712Q activates a 34μA charge pump current source to initiate MOSFET gate charging. During forward operation, the gate voltage is raised until it attains the clamping voltage set by the internal 12V Zener diode between the GATE and IN pins of the SGM25712Q.

The SGM25712Q is intended to control the gate-to-source voltage (V_{GS}) of the MOSFET. If the current through the MOSFET drops, such that the source-to-drain voltage drops below the 22mV (TYP) V_{SD_REG} threshold, the voltage at the GATE pin will decrease until V_{SD} stabilizes at 22mV. Conversely, if V_{SD} exceeds the V_{SD_REG} regulation point, V_{GS} increases until it reaches the 12V Zener clamp voltage, set by the internal Zener diode between the GATE and IN pins of the SGM25712Q.

When the MOSFET current reverses (e.g., due to input supply failure), causing the voltage between SGM25712Q's IN and OUT pins to drop below the V_{SD_REV} threshold (-26mV TYP), the SGM25712Q activates a strong internal GATE-to-IN discharge transistor to rapidly discharge the MOSFET gate.

In cases of abrupt input supply failure (e.g., shorted to ground), a temporary reverse current flows via the MOSFET until the gate discharges completely. This current originates from parallel power supplies as well as load capacitance.

The SGM25712Q detects voltage reversal conditions within 37ns (TYP) and initiates gate discharge. Turn-off time depends on the MOSFET's gate capacitance (C_{GS}); for example, a 47nF C_{GS} allows full turn-off within 220ns (TYP). This rapid response suppresses transient voltage and current effects at the output, reducing disturbances from redundant power supplies.

DETAILED DESCRIPTION (Continued)

VS Pin

The SGM25712Q's VS pin serves as the primary power input for internal biasing circuits and also provides auxiliary power to the internal gate-drive charge pump.

In typical SGM25712Q applications, if the input voltage exceeds 4V, the VS pin can be directly connected to the OUT pin. When input voltage is near but still above the 4V minimum threshold, an RC low-pass filter is recommended between VS and the OUT pins to prevent erratic behavior caused by unwanted voltage spikes on the OUT or IN pin. The series resistor should be kept low to minimize voltage drop (e.g., 100Ω). The capacitor should use the smallest value that effectively suppresses noise.

With VS powered while IN is left open or tied to ground, roughly 0.23mA flows from VS into the part, and about 9μA flows back out of the OUT pin. Of that leakage, some 33μA leaves through the IN pin and the remainder is diverted to ground. This leakage has no effect on long-term reliability, but the circuit design has to allow for it if the part is to operate as intended.

Refer to the Reverse Input Voltage Protection with IQ Reduction section for guidance on eliminating this leakage current. Alternatively, the SGM25712Q can operate with a V_{IN} as low as 2V when the VS pin is supplied independently. This external VS supply must be within the voltage range of 4V to 72V. See Figure 9 for details.

OFF Pin

The OFF pin serves as a logic-level input that governs the gate driving of the external MOSFET, with a maximum voltage rating of 5.5V. When asserted high, this pin disables the MOSFET's conduction path, independently of the IN/OUT voltages, making the load current to flow through the MOSFET's body diode. During normal diode conduction, the voltage drop (V_{IN} - V_{OUT}) across the terminals is approximately 700mV. The OFF pin incorporates an internal 5μA pull-down current (TYP). If unused, the pin may be left floating or connected to GND.

Device Functional Modes

ON/OFF Control Mode

Asserting the OFF pin high disables the MOSFET, but the load current continues to flow through its body diode, thereby maintaining V_{OUT} availability.

External Power Supply Mode

The VS pin of the SGM25712Q can operate as the bias supply input over a voltage range of 4V to 72V. Under this configuration, the input voltage can be as low as 2V, as illustrated in Figure 9.

APPLICATION INFORMATION

High-availability systems frequently employ multiple parallel-connected redundant power supplies to enhance system reliability. Schottky ORing diodes are generally used to connect these redundant sources to a common load connection point. However, a key drawback of this approach is the inherent forward voltage drop across the diodes, which diminishes available voltage and increases power losses as load currents rise. By replacing ORing diodes with N-channel MOSFETs, designers can mitigate these issues while introducing only marginal additional complexity. This substitution reduces or removes the requirement for diode heat sinks and large thermal copper areas on printed circuit boards in high-power applications.

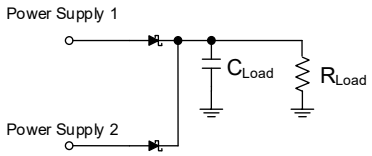


Figure 5. ORing with Diodes

The SGM25712Q is a high-side ORing controller designed to drive an external N-channel MOSFET, thereby supplanting conventional ORing diodes. It monitors the source-drain voltage via the IN and OUT pins, and modulates the MOSFET's gate signal (via the GATE pin) to regulate its operation dynamically. This configuration enables diode-like rectification behavior, where the MOSFET's source and drain terminals function analogously to a diode's anode and cathode respectively, but with idealized low-forward-voltage characteristics.

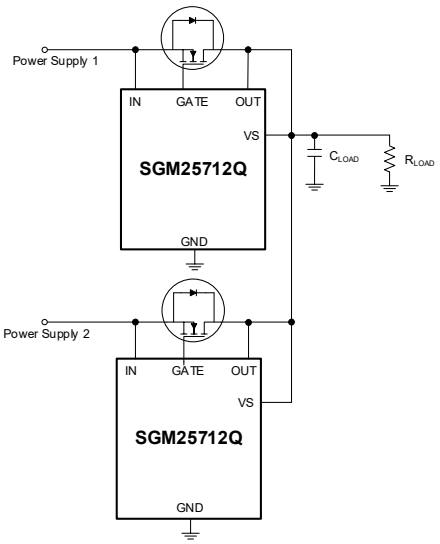


Figure 6. ORing with MOSFETs

MOSFET Selection

The critical electrical parameters of the MOSFET include the maximum continuous drain current (I_D), maximum source current (I_S, body diode rating), maximum drain-source voltage (V_{DS_MAX}), threshold voltage (V_{GS_TH}), drain-source reverse breakdown voltage (V_{BR_DSS}) and on-state resistance (R_{DSON}).

Drain current (I_D): The rated I_D must exceed system load current to prevent thermal overstress.

Body diode current (I_S): I_S is normally equal to, or a little above, the drain current rating, although that current only flows while the gate is being charged towards V_{GS_TH}.

Gate Charge Time (t_Q): Defined by the equation $t_Q = Q_G / I_{GATE_ON}$, where Q_G represents total gate charge and I_{GATE_ON} is the drive current during MOSFET turn-on.

1. Drain-source voltage (V_{DS_MAX}): Must exceed the peak application voltage (including fault conditions) to prevent breakdown.
2. Reverse breakdown voltage (V_{BR_DSS}): In low-voltage applications, this parameter provides transient protection for the OUT pin by enabling a conduction path from OUT to IN during positive voltage spikes on the OUT pin.
3. The threshold voltage (V_{GS_TH}) between gate and source has to be compatible with what the SGM25712Q driver can deliver. Logic-level MOSFETs, with R_{DSON} quoted at a 4V gate-source threshold, are the usual choice. Sub-logic-level devices quoted at 2.5V V_{GS_TH} are also usable, provided their other ratings are checked against the output capability of the driver.
4. The dominant loss in the MOSFET of an SGM25712Q active ORing arrangement is conduction loss, set by the source-to-drain current flowing into the load and by the R_{DSON} of the device. Lowering R_{DSON} is the obvious way to cut that loss, but choosing the lowest available R_{DSON} does not always give a good result, which is the opposite of the usual expectation. Several factors are behind this.

APPLICATION INFORMATION (continued)

(1) Reverse transition detection is crucial for system reliability. Increased on-state resistance (R_{DSON}) enhances voltage signal amplification to the SGM25712Q's reverse comparator even under reduced reverse current conditions. This enables faster MOSFET shutdown triggering if the input voltage path is grounded, thereby minimizing potential disruptions to the redundant power bus.

(2) Reverse conduction leakage. When multiple input power sources exhibit voltage levels closely aligned, a minor current might persistently traverse the MOSFET's drain-source path (reverse conduction) without triggering the SGM25712Q's reverse detection circuitry. However, elevated on-resistance (R_{DSON}) reduces this reverse conduction current magnitude by increasing impedance in the leakage pathway.

(3) There is an inverse relationship between MOSFET cost and on-state resistance (R_{DSON}): lower R_{DSON} values generally correlate with higher component costs. This arises because reducing R_{DSON} typically requires larger die sizes, thicker metal layers, or advanced process technologies to maintain low resistance, all of which increase fabrication expenses.

5. The primary loss mechanism in the SGM25712Q's MOSFET-based active ORing configuration is conduction loss, which scales with the square of the source-to-drain current (I_{DS}^2) multiplied by the MOSFET's on-resistance (R_{DSON}). Reducing R_{DSON} directly minimizes this loss but introduces critical trade-offs that must be evaluated holistically:

(1) A MOSFET with an oversized R_{DSON} value may cause substantial power losses. Additionally, during regulation toward the V_{SD_REG} threshold of 22mV, the SGM25712Q driver will fully charge the MOSFET gate to its maximum capacity while attempting to drive the drain-source voltage to this target. Higher gate charge lengthens the turn-off discharge time because the gate discharge current remains constant.

(2) R_{DSON} selection is advised to maintain a voltage drop between 22mV and 100mV under nominal load conditions to adhere to the recommended operational guidelines. Formula: $(22mV / I_D) \leq R_{DSON} \leq (100mV / I_D)$.

(3) When designing MOSFET packages, thermal resistance must be assessed alongside expected power loss to keep the junction temperature (T_J) within acceptable operational boundaries, as elevated T_J values directly elevate the on-state resistance (R_{DSON}), thereby compromising device efficiency under thermal loading.

6. $P_D = I_D^2 \times (R_{DSON})$

7. To ensure junction temperatures (T_J) remain below +100℃ under operating conditions defined by T_{A_MAX} = +35℃, I_{LOAD} = 10A, and R_{DSON} = 10mΩ, the maximum permissible junction-to-ambient thermal resistance (θ_{JA}) is calculated through the following derivation. First, compute power dissipation (P_D): $P_D = I_D^2 \times R_{DSON} = (10A)^2 \times 10m\Omega = 1W$. The thermal resistance θ_{JA} is then determined via the equation $T_J = T_A + P_D \times \theta_{JA}$. Rearranging for θ_{JA} gives $\theta_{JA} \leq (T_J - T_{A_MAX}) / P_D = (100℃ - 35℃) / 1W = 65℃/W$.

APPLICATION INFORMATION (continued)

Short-Circuit Failure of an Input Supply

An abrupt short-circuit (0Ω) across the input voltage source induces the maximum possible backflow current during the discharge phase of the MOSFET gate by the SGM25712Q's internal controller. This reverse current magnitude is constrained solely by the MOSFET's on-state resistance (R_{DSON}), combined with resistive losses and inductive effects from parasitic wiring elements. The peak instantaneous reverse current under worst-case conditions would thus be determined by:

$$I_{D_REV} = (V_{OUT} - V_{IN}) / R_{DSON}$$

The internal reverse comparator will activate and begin discharging the gate terminal as soon as reverse current reaches:

$$I_{D_REV} = V_{SD_REV} / R_{DSON}$$

Upon complete MOSFET deactivation, the energy accumulated in parasitic wiring inductances is dissipated into the remaining circuitry. Consequently, the IN pin of the SGM25712Q experiences a negative voltage surge, whereas the OUT pin undergoes a positive voltage surge. To safeguard the IN pin, a diode clamp connected to ground can be applied to counteract negative excursions. For the OUT pin, protection measures include employing a TVS diode, implementing a nearby bypass capacitor, or combining both solutions. In low-voltage applications, the MOSFET's drain-source breakdown voltage (V_{BR_DSS}) might suffice for OUT pin protection, provided V_{IN} + $V_{BR_DSS_MAX}$ remains below 72V. However, since datasheets typically do not guarantee the maximum breakdown thresholds, reliance on this approach is advisable only under careful evaluation.

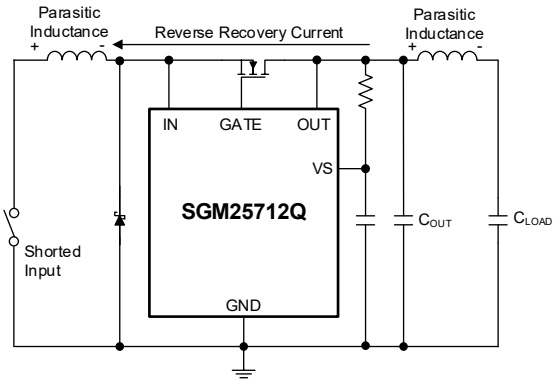


Figure 7. Reverse Recovery Current Generates Inductive Spikes at V_{IN} and V_{OUT}

TYPICAL APPLICATIONS

Typical Application with Input and Output Transient Protection

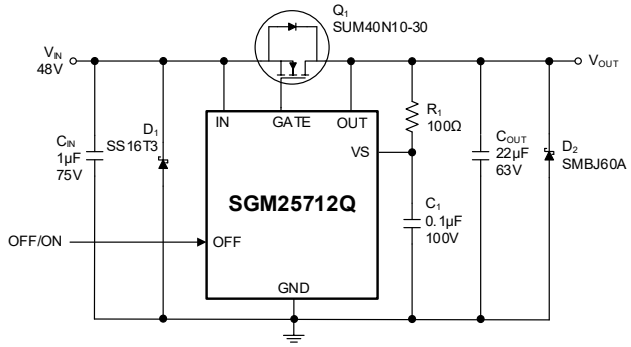


Figure 8. Typical Application with Input and Output Transient Protection Schematic

Design Requirements

Table 1 presents the various parameters of Figure 8.

Table 1. Design Parameters

Design Parameter	Example Value
Minimum Input Voltage, V_{IN_MIN}	6V
Maximum Input Voltage, V_{IN_MAX}	50V
Output Current Range, I_{OUT}	0A to 15A
Ambient Temperature Range, T_A	0℃ to +50℃

Detailed Design Procedure

This outlined procedure enables the determination of component parameters for the SGM25712Q's circuit design.

Power Supply Components (R_1, C_1) Selection

The SGM25712Q's VS pin serves as the primary power source for internal biasing circuits and acts as a secondary power source for the gate driver charge pump's operation. The series resistor (R1) should be selected with a sufficiently low resistance to minimize voltage drop across the VS pin. A nominal resistor value of 100Ω is commonly employed. Regarding the capacitor (0.1μF, TYP), the minimal capacitance value that achieves adequate filtering of voltage noise should be chosen to balance performance and efficiency.

MOSFET (Q_1) Selection

The methodology for selecting the MOSFET (Q_1) is elaborated in the MOSFET Selection section. For the design case study, the SUM40N10-30-E3 MOSFET was specifically implemented as the chosen device.

D_1 and D_2 Selection for Inductive Kick-Back Protection

The diodes D_1/D_2 and capacitors C_2 in Figure 9 function as protective elements against inductive kickback, mitigating negative transient voltage spikes induced on the input terminal when the supply voltage is abruptly shorted to ground. Consequently, the IN pin of the SGM25712Q experiences a negative voltage surge, whereas the OUT pin encounters a positive surge. To safeguard the IN pin, a Schottky diode (D_1) clamps the negative excursion to ground; complementary protection measures are required for the OUT pin, such as a TVS diode (e.g., D_2), a localized bypass capacitor, or a combined solution. The Schottky Barrier Rectifier (SS16T3G) for D_1 is rated at 1A/60V, while D_2 employs a 60V TVS diode (SMBJ60A-13F).

Using a Separate VS Supply for Low V_{IN} Operation

To enable operation at V_{IN} voltages as low as 2V, the SGM25712Q requires its VS pin to be biased to a voltage between 4V and 72V. This configuration allows the device to function reliably under low input voltages while maintaining proper internal biasing. Figure 9 illustrates this implementation, where the VS supply ensures stable operation despite reduced V_{IN}, minimizing power loss in the low-voltage regime.

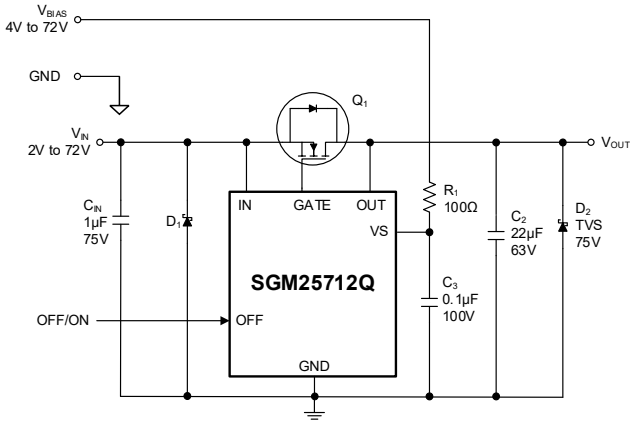


Figure 9. Using a Separate VS Supply for Low V_{IN} Operation Schematic

TYPICAL APPLICATION (Continued)

ORing of Two Power Sources

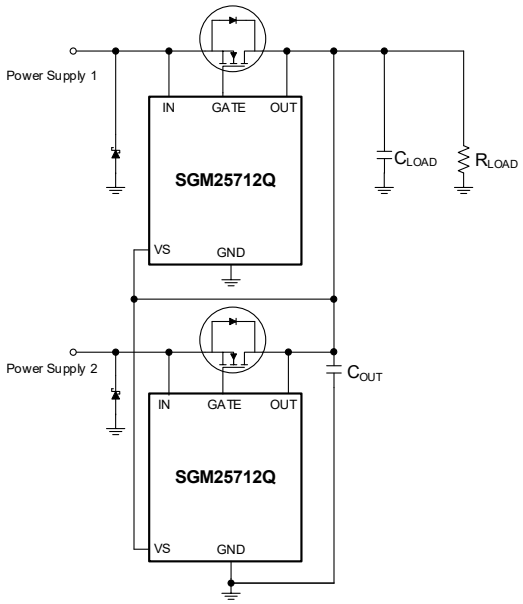


Figure 10. ORing of Two Power Sources

Reverse Input Voltage Protection with I_Q Reduction

When the VS supply is active with the IN terminal in a floating or grounded state, the IC draws 0.23mA of quiescent current through the VS pin and exhibits 9μA leakage current from the OUT pin into the IC. Of this leakage, approximately 33μA exits via the IN pin, while the remainder flows to ground. Though these leakage paths do not degrade the IC's long-term reliability, they should be accounted for during circuit design to prevent unintended behavior. In battery-powered systems, disconnecting the SGM25712Q's ground connection via Q_2 (OFF state, per Figure 11) isolates the IC from the system, thereby eliminating parasitic current drain from the battery.

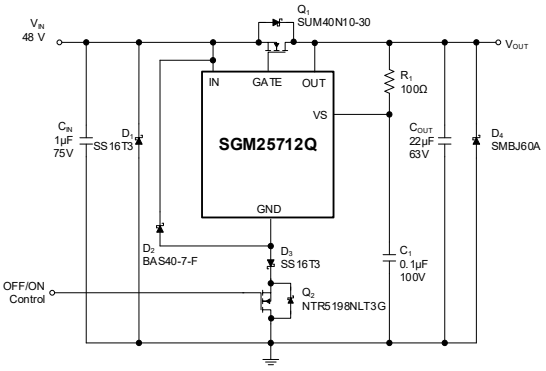


Figure 11. Reverse-Voltage Blocking Topology Integrating Low-I_Q Biasing Networks

Basic Application with Input Transient Protection

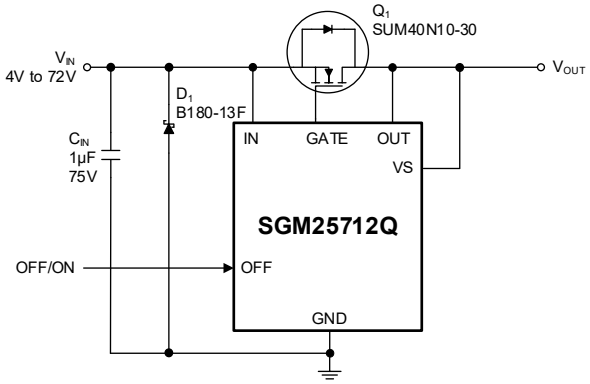


Figure 12. Basic Application Circuit Diagram with Input Transient Protection Function

48V Application with Reverse Input Voltage (V_{IN} = -48V) Protection

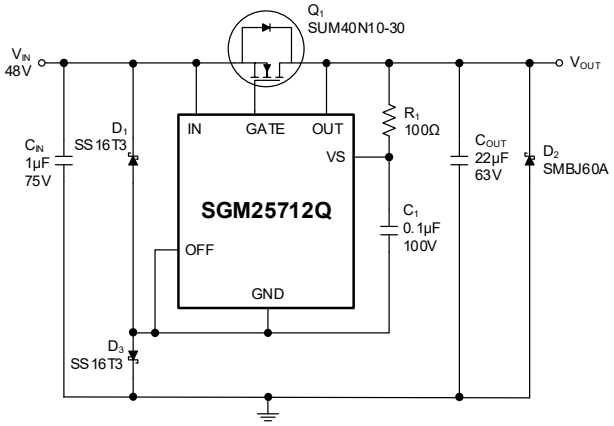


Figure 13. 48V Reverse-Polarity Protected Power Input Circuit with -48V Withstand Capability

Power Supply Recommendations

Upon deactivating the external MOSFET, the SGM25712Q generates transient voltage spikes at its input/output terminals due to reverse recovery effects, as described in Short-Circuit Failure of an Input Supply. To safeguard the device and peripheral components during direct input short-circuit events, negative voltage transients at the IN and OUT pins must be suppressed via TVS diodes.

TYPICAL APPLICATION (Continued)

Layout Guidelines

A standard PCB configuration for the SGM25712Q is illustrated in Figure 14. To ensure optimal performance, it is recommended that the IN, GATE, and OUT terminals be placed adjacent to the source and drain terminals of the MOSFET. Maintain conductors for the MOSFET drain in a wide and short configuration to reduce resistive losses and parasitic inductance. Transient voltage suppressors (TVS) D_1 and D_4 should be positioned according to the placement depicted in the schematic referenced in the Figure 14 of SGM25712Q's design guidelines.

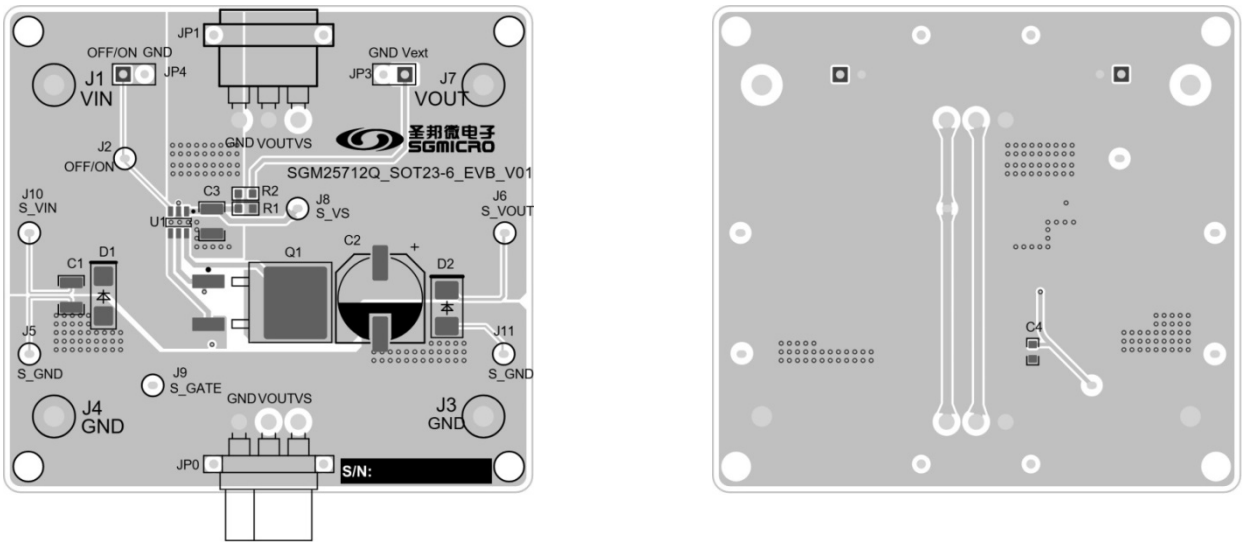


Figure 14. Layout Example

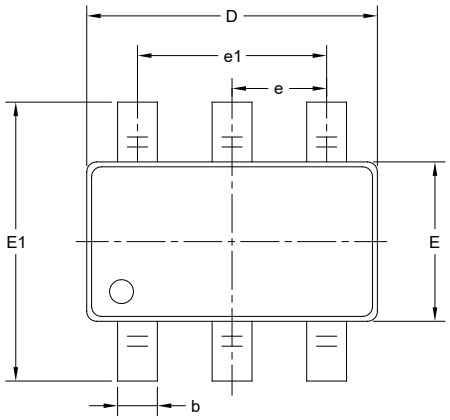
REVISION HISTORY

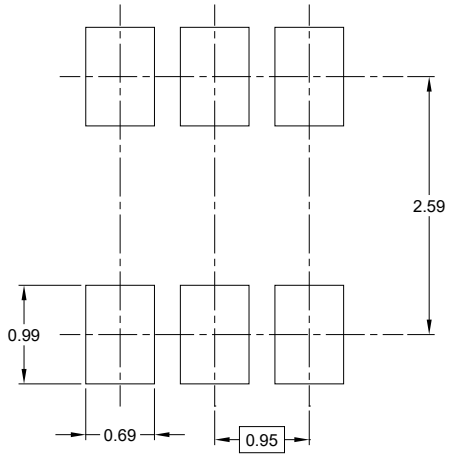
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original to REV.A (OCTOBER 2026)	Page
Changed from product preview to production data	All

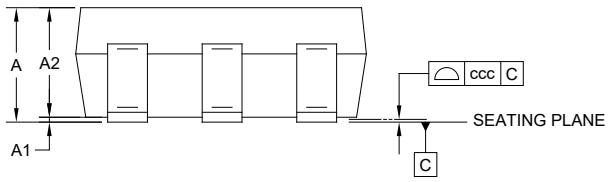
PACKAGE OUTLINE DIMENSIONS

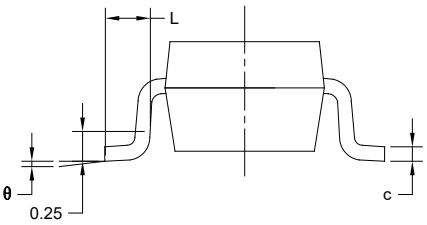
SOT-23-6





RECOMMENDED LAND PATTERN (Unit: mm)



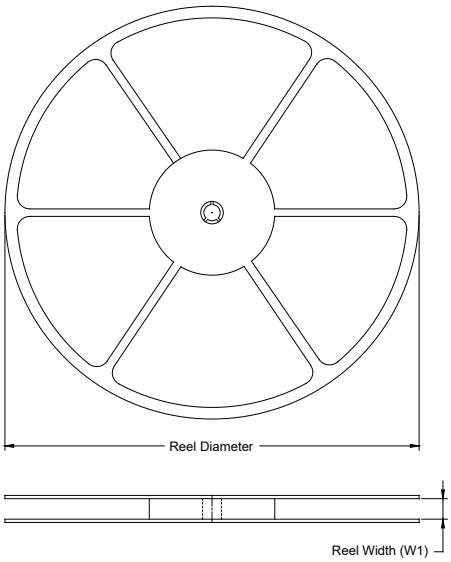


Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	-	-	1.450
A1	0.000	-	0.150
A2	0.900	-	1.300
b	0.300	-	0.500
c	0.080	-	0.220
D	2.750	-	3.050
E	1.450	-	1.750
E1	2.600	-	3.000
e	0.950 BSC		
e1	1.900 BSC		
L	0.300	-	0.600
θ	0°	-	8°
ccc	0.100		

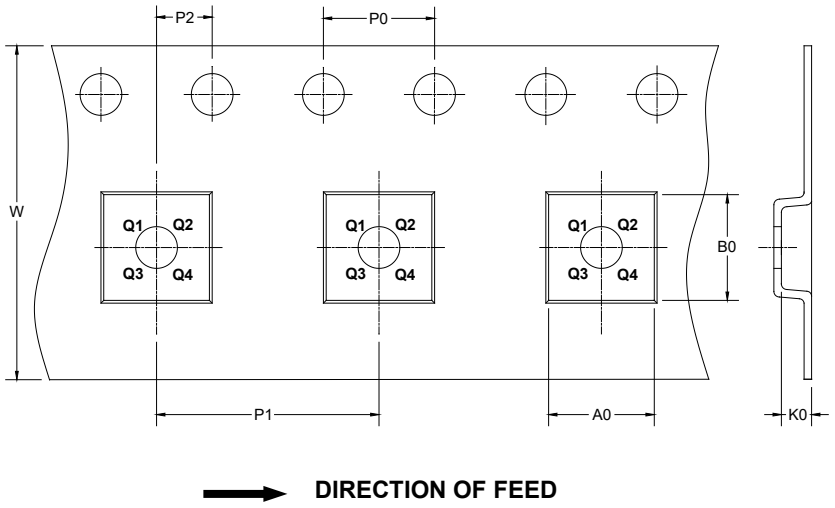
NOTES:
1. This drawing is subject to change without notice.
2. The dimensions do not include mold flashes, protrusions or gate burrs.
3. Reference JEDEC MO-178.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



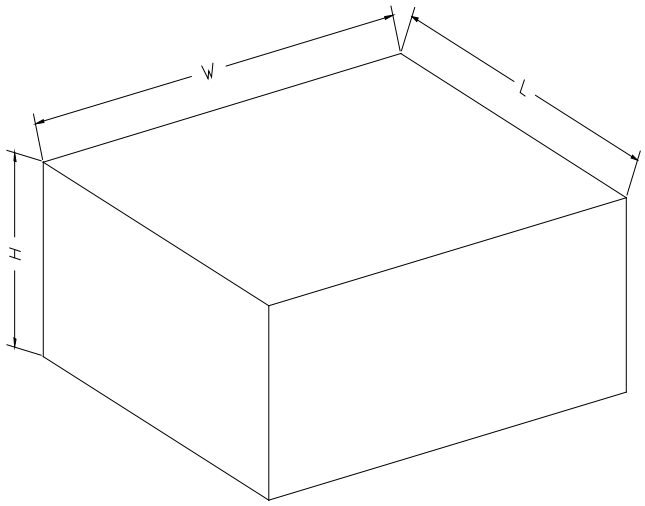
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
SOT-23-6	7"	9.5	3.23	3.17	1.37	4.0	4.0	2.0	8.0	Q3

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18

DD0002