SGM25716L
High Voltage Hot-Swap Controller and Digital Voltage, Current and Power Monitor with PMBus Interface

GENERAL DESCRIPTION

The SGM25716L is a high-performance hot-swap controller for 10V to 90V system with an SMBus/I^{2}C interface compliant with PMBus standards. The SGM25716L provides continuous real-time monitoring of power, voltage, current, temperature, and fault conditions through the SMBus/I^{2}C interface, reporting all data to the system management host.

The SGM25716L delivers current and power limiting capabilities, which safeguards sensitive circuitry when boards are inserted into a live system backplane or any other active power source. Additionally, a rapid-response circuit breaker prevents damage if a short circuit occurs at the output. Key parameters such as input under-voltage and over-voltage levels, hysteresis, insertion delay time, and fault detection time are all configurable. The SGM25716L also features a temperature monitoring module that interfaces with a low-cost external diode. This diode is used to monitor the temperature of external MOSFETs or other thermally sensitive components. The power good output serves as a quick indicator whenever input or output voltages deviate from their programmed ranges.

The monitoring module of the SGM25716L calculates two types of values for subsystem operating parameters (V_{IN}, I_{IN}, P_{IN}, V_{OUT}): real-time values and average values. It also computes the peak power of the subsystem. Accurate power averaging is achieved by calculating the average of the product derived from input voltage and input current.

The SGM25716L features enhanced telemetry accuracy and supports for the READ_EIN command for energy monitoring.

The SGM25716L is available in a Green TSSOP-28 (Exposed Pad) package.

FEATURES

- **10V to 90V Operation**
- **100V Continuous Absolute Maximum**
- **26mV or 51mV ILIM Threshold**
- **Programmable FET SOA Protection**
- **User-Configurable UV, OV, and t_{FAULT} Thresholds**
- **External FET Temperature Sensing**
- **Failed FET Detection**
- **I^{2}C/SMBus Interface**
- **PMBus Compliant Command Structure**
- **High-Accuracy Monitoring of V_{IN}, V_{OUT}, I_{IN}, P_{IN}, and V_{AUX}**
- **Programmable I/V/P Averaging Interval**
- **12-Bit ADC with 1kHz Sampling Rate**
- **Available in a Green TSSOP-28 (Exposed Pad) Package**

APPLICATIONS

48V Servers
Base Station Power Distribution
Networking Routers and Switchers
PLC Power Management
24V to 28V Industrial Systems

SIMPLIFIED SCHEMATIC

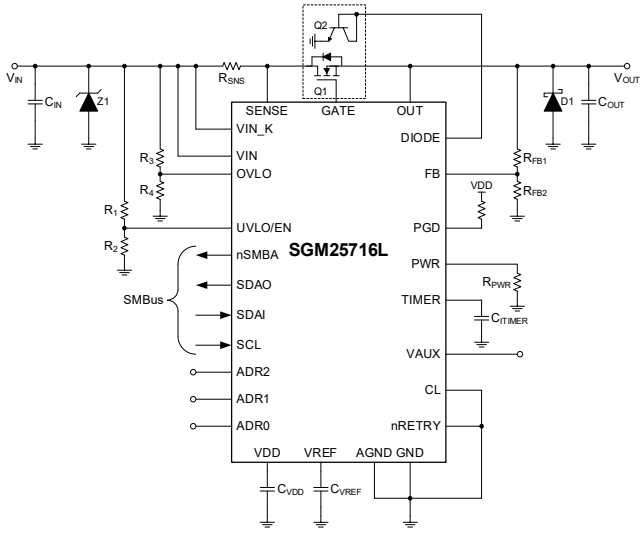


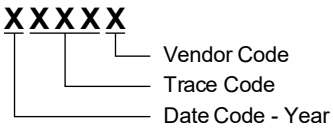
Figure 1. Simplified Schematic

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM25716L	TSSOP-28 (Exposed Pad)	-40℃ to +125℃	SGM25716LXPTS28G/TR	SGM25716L XPTS28 XXXXX	Tape and Reel, 4000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Input Voltage

VIN, VIN_K, GATE, UVLO/EN, SENSE, PGD to GND ..... -0.3V to 100V

OVLO, FB, TIMER, PWR to GND ..... -0.3V to 7V

OUT to GND ..... -0.3V to 100V

OUT to GND (1ms Transient) ..... -1V to 100V

SCL, SDAI, SDAO, CL, ADR0, ADR1, ADR2, VDD, VAUX, DIODE, nRETRY, nSMBA to GND ..... -0.3V to 6V

SENSE to VIN_K, VIN to VIN_K, AGND to GND ..... -0.3V to 0.3V

Package Thermal Resistance

TSSOP-28 (Exposed Pad), θ_{JA} ..... 26℃/W

TSSOP-28 (Exposed Pad), θ_{JB} ..... 7.9℃/W

TSSOP-28 (Exposed Pad), $\theta_{JC\ (TOP)}$ ..... 16.4℃/W

TSSOP-28 (Exposed Pad), $\theta_{JC\ (BOT)}$ ..... 1.2℃/W

Junction Temperature ..... +150℃

Storage Temperature Range ..... -65℃ to +150℃

Lead Temperature (Soldering, 10s) ..... +260℃

ESD Susceptibility (1) (2)

HBM ..... ±2000V

CDM ..... ±1000V

NOTES:

1. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.
2. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

RECOMMENDED OPERATING CONDITIONS

VIN, SENSE, OUT Voltage ..... 10V to 90V

Operating Junction Temperature Range ..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

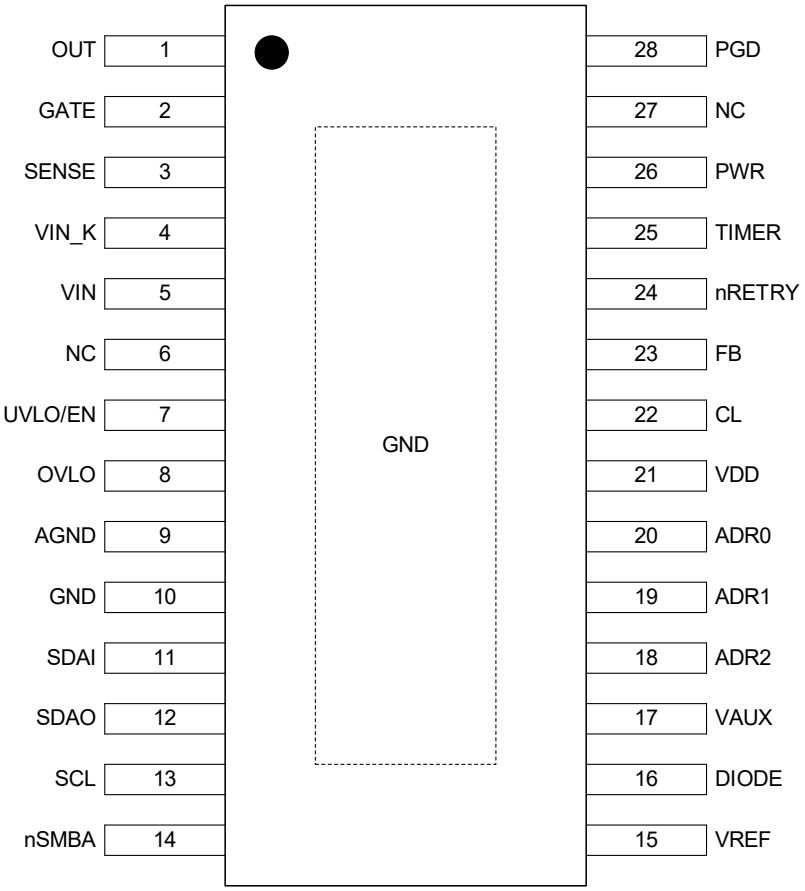
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

(TOP VIEW)



TSSOP-28 (Exposed Pad)

PIN DESCRIPTION

PIN	NAME	FUNCTION
1	OUT	Output Pin. Connect this pin to the source of the external MOSFET. It is utilized to calculate the V_{DS} of the external MOSFET for power limiting purposes and to keep track of the output voltage.
2	GATE	Gate Drive Output. This pin is the gate drive of an external MOSFET.
3	SENSE	Current-Sense Input. This pin, along with VIN_K, detects the voltage across the external current-sense resistor (R_{SNS}). Once that voltage exceeds the over-current threshold, the output current is clamped and the fault timer is triggered.
4	VIN_K	Positive Supply Kelvin Pin. It is utilized to measure the input voltage for current sensing and keep track of the input voltage.
5	VIN	Positive Supply Input. Connect a small ceramic bypass capacitor near this pin to suppress transients generated upon load current deactivation.
6	NC	No Connection.
7	UVLO/EN	Under-Voltage Lockout. The under-voltage turn-on threshold is configured by an external resistor divider connected to the system input voltage. Hysteresis is provided by an internal 20μA current source. The enabled threshold voltage of this pin is specified as 2.47V.
8	OVLO	Over-Voltage Lockout. The over-voltage turn-off threshold is configured by an external resistor divider referenced to the system input voltage. An internal current source rated at 21μA delivers hysteresis. The disabled threshold voltage for this pin is specified as 2.45V.
9	AGND	Analog Ground.
10	GND	Circuit Ground.
11	SDAI	SMBus Data Input Pin. This pin serves as the data input for the SMBus interface. If unidirectional isolation components are not required for the application, connect the circuit to the SDAO pin.
12	SDAO	SMBus Data Output Pin. This pin serves as the data output for the SMBus interface. If unidirectional isolation components are not required for the application, connect the circuit to the SDAI pin.
13	SCL	SMBus Clock. Clock pin for SMBus.
14	nSMBA	SMBus Alert Line. Alert pin for SMBus, active low. This is an open-drain output that requires an external pull-up resistor connected to VDD or another voltage supply.
15	VREF	Internal Reference. A precision 2.97V reference generated inside the IC is used for ADC operation. Place a 1μF bypass capacitor from this pin to ground.
16	DIODE	External Diode. Connect this pin to MMBT3904 NPN transistor configured as a diode for temperature sensing. Ground the pin if it is not in use.
17	VAUX	Auxiliary Voltage Input. This pin provides voltage telemetry sourced externally, with a full-scale input of 2.97V.
18	ADR2	SMBUS Address Line 2. Tri-state address line. Connect this pin to VDD, GND, or leave it floating.
19	ADR1	SMBUS Address Line 1. Tri-state address line. Connect this pin to VDD, GND, or leave it floating.
20	ADR0	SMBUS Address Line 0. Tri-state address line. Connect this pin to VDD, GND, or leave it floating.
21	VDD	Internal Sub-Regulator Output. Internally sub-regulated 4.85V bias supply. Connect a 1μF capacitor between this pin and ground.
22	CL	Current Limit Range. The over-current threshold is set to 51mV when this pin is tied to GND or left floating, and to 26mV when connected to VDD.
23	FB	Power Good Feedback. An external resistor divider connected to the OUT pin defines the output voltage that triggers the switching of the PGD pin. The pin's threshold voltage is specified as 2.45V. Hysteresis is added by an internal current source rated at 20μA.
24	nRETRY	Fault Retry Input. The power-up fault retry feature is configured via this pin. When the pin is connected to GND, the device repeatedly attempts power engagement if a fault occurs. When this pin is connected to VDD, the device latches off upon fault detection.
25	TIMER	Timing Capacitor. Insertion delay, fault timeout, and restart timing are all programmed by the external capacitor connected to this pin.
26	PWR	Power Limit Set. The maximum allowable power dissipation of the external power MOSFET is set by an external resistor on this pin, which works with the current-sense resistor (R_{SNS}).
27	NC	No Connection.
28	PGD	Power Good Indicator. This is an open-drain output. It goes high when the FB pin voltage exceeds V_{FBTH} (typically 2.45V). This pin can be connected to the output rail (external MOSFET source) or other voltage nodes that need to be monitored.
Exposed Pad	GND	Connect to Ground.

ELECTRICAL CHARACTERISTICS

(V_{IN} = 48V, T_J = -40℃ to +125℃, typical values are measured at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input (VIN Pin)						
Input Current, Enabled	I_{IN-EN}	V_{UVLO} = 3V and V_{OVLO} = 2V		2.5	4.5	mA
VIN Power-On Reset Threshold for Insertion Timer Activation	POR_{IT}	V_{IN} increasing		7.5	8.5	V
VIN Power-On Reset Threshold for All Function Enabled	POR_{EN}	V_{IN} increasing		8.3	9.5	V
POR_{EN} Hysteresis	POR_{HYS}	V_{IN} decreasing		120		mV
V_{DD} Regulator (VDD Pin)						
VDD Regulate Voltage	V_{DD}	I_{VDD} = 0A	4.60	4.90	5.15	V
		I_{VDD} = 10mA		4.85		
VDD Current Limit	V_{DDILIM}		-38	-30	-22	mA
VDD Voltage Reset Threshold	V_{DDPOR}	V_{DD} rising		4.1		V
UVLO/EN, OVLO Pins						
UVLO Threshold	$UVLO_{TH}$	V_{UVLO} falling	2.40	2.47	2.54	V
UVLO Hysteresis Current	$UVLO_{HYS}$	V_{UVLO} = 1V	13	20	26	μA
UVLO Bias Current	$UVLO_{BIAS}$	V_{UVLO} = 3V			1	μA
OVLO Threshold	$OVLO_{TH}$	V_{OVLO} rising	2.38	2.45	2.52	V
OVLO Hysteresis Current	$OVLO_{HYS}$	V_{OVLO} = 1V	-26	-21	-13	μA
OVLO Bias Current	$OVLO_{BIAS}$	V_{OVLO} = 1V			1	μA
Power Good (PGD Pin)						
Output Low Voltage	PGD_{VOL}	I_{SINK} = 2mA		80	200	mV
Off Leakage Current	PGD_{IOH}	V_{PGD} = 80V			1	μA
FB Pin						
FB Threshold	FB_{TH}	V_{UVLO} = 3V and V_{OVLO} = 2V	2.38	2.45	2.52	V
FB Hysteresis Current	FB_{HYS}		-25	-20	-15	μA
Off Leakage Current	FB_{LEAK}	V_{FB} = 2.3V			1	μA
Power Limit (PWR Pin)						
Power Limit Sense Voltage ($V_{IN-SENSE}$)	PWR_{LIM}	$V_{SENSE-OUT}$ = 48V, R_{PWR} = 60kΩ	7.5	9.5	11.5	mV
		$V_{SENSE-OUT}$ = 48V, R_{PWR} = 20kΩ	1.2	3.2	5.2	
		$V_{SENSE-OUT}$ = 24V, R_{PWR} = 60kΩ	15.55	19.3	23.05	
		$V_{SENSE-OUT}$ = 24V, R_{PWR} = 20kΩ	4.7	6.7	8.7	
PWR Pin Current	I_{PWR}	V_{PWR} = 2.5V		-20		μA
PWR Pin Impedance under Disabled Condition	R_{SAT_PWR}	V_{UVLO} = 2V		147		Ω
Gate Control (GATE Pin)						
Source Current	I_{GATE}	Normal operation	-26	-20	-10	μA
Fault Sink Current		V_{UVLO} = 2V	3.4	4.4	5.3	mA
POR Circuit Breaker Sink Current		$V_{IN-SENSE}$ = 150mV or V_{IN} < POR_{IT}, V_{GATE} = 5V	80	125	170	mA
Reverse Bias Voltage for GATE-to-OUT Zener Diode	V_{GATEZ}	GATE to OUT	12	16	18	V
Peak Charge Pump Voltage Under Normal Operating Condition (V_{IN} = V_{OUT})	V_{GATECP}	GATE to OUT		12		V

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 48V, T_J = -40℃ to +125℃, typical values are measured at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
OUT Pin						
OUT Bias Current, Enabled	I_{OUT-EN}	V_{OUT} = V_{IN}, normal operation		38		μA
OUT Bias Current, Disabled (1)	$I_{OUT-DIS}$	Disabled, V_{OUT} = 0V, V_{SENSE} = V_{IN}		-34		μA
Current Limit						
Current Limit Threshold Voltage (V_{IN} - V_{SENSE})	V_{CL}	CL = VDD	23	26	29	mV
		CL = GND	46	51	56	
SENSE Input Current	I_{SENSE}	Enabled, V_{SENSE} = V_{OUT}		40		μA
		Disabled, V_{OUT} = 0V		75		
		Enabled, V_{OUT} = 0V		110		
Circuit Breaker						
Circuit Breaker to Current Limit Ratio: (V_{IN} - V_{SENSE})$_{CB}$/V_{CL}	RT_{CB}	CB/CL ratio bit = 0, V_{ILIM} = 51mV	1.60	1.92	2.24	V/V
		CB/CL ratio bit = 1, V_{ILIM} = 51mV	3.30	3.88	4.46	
		CB/CL ratio bit = 0, V_{ILIM} = 26mV		1.85		
		CB/CL ratio bit = 1, V_{ILIM} = 26mV		3.77		
Circuit Breaker Threshold Voltage: (V_{IN} - V_{SENSE})	V_{CB}	CB/CL ratio bit = 0, V_{ILIM} = 51mV	83	98	113	mV
		CB/CL ratio bit = 1, V_{ILIM} = 51mV	170	198	226	
		CB/CL ratio bit = 0, V_{ILIM} = 26mV	39	48	57	
		CB/CL ratio bit = 1, V_{ILIM} = 26mV	83	98	113	
Timer (TIMER Pin)						
Upper Threshold	V_{TMRH}		3.74	3.9	4.07	V
Lower Threshold	V_{TMRL}	Restart cycles	0.98	1.1	1.24	V
		End of eighth cycle		0.3		
		Re-enabled threshold		0.3		
Insertion Time Current	I_{TIMER}	TIMER pin = 2V	-5.9	-4.8	-3.3	μA
Sink Current, End of Insertion Time			1.2	1.6	2.0	mA
Fault Detection Current			-95	-75	-50	μA
Fault Sink Current			1.7	2.5	3.2	μA
Fault Restart Duty Cycle	DC_{FAULT}			0.5		%
Internal Reference						
Reference Voltage	V_{REF}		2.93	2.97	3.02	V
ADC and MUX						
Resolution				12		bits
Integral Non-Linearity	INL	ADC only		±4		LSB
Acquisition + Conversion Time	$t_{ACQUIRE}$	Any channel		120		μs
Acquisition Round Robin Time	t_{RR}	Cycle all channels		1		ms

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 48V, T_J = -40℃ to +125℃, typical values are measured at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Telemetry Accuracy						
Current Input Full-Scale Range	I_{INFSR}	CL = GND		54.4		mV
		CL = VDD		27.0		
Current Input LSB	I_{INLSB}	CL = GND		13.3		μV
		CL = VDD		6.7		
VAUX Input Full-Scale Range	V_{AUXFSR}			2.97		V
VAUX Input LSB	V_{AUXLSB}			725		μV
Input Voltage Full-Scale Range	V_{INFSR}			88.9		V
Input Voltage LSB	V_{INLSB}			21.7		mV
Output Voltage Full-Scale Range	V_{OUTFSR}			88.9		V
Output Voltage LSB	V_{OUTLSB}			21.7		mV
Input Current Accuracy (2)	I_{INACC}	$V_{IN-SENSE}$ = 22mV (80% IINFSR), CL = VDD	-1.55		1.55	%
		$V_{IN-SENSE}$ = 5mV (19% IINFSR), CL = VDD	-5.00		5.00	
		$V_{IN-SENSE}$ = 44mV (80% IINFSR), CL = GND	-3.10		3.10	
V_{IN}, V_{OUT} Absolute Accuracy (2)	V_{ACC}	V_{IN}, V_{OUT} = 48V, 80V	-1.20		1.20	%
		V_{IN}, V_{OUT} = 10V	-2.25		2.25	
V_{AUX} Absolute Accuracy (2)		V_{AUX} = 2.8V	-1.20		1.20	%
Input Power Accuracy (2)	P_{INACC}	V_{IN} = 48V, $V_{IN-SENSE}$ = 22mV (80% IINFSR), CL = VDD	-2.25		2.25	%
		V_{IN} = 48V, $V_{IN-SENSE}$ = 5mV (19% IINFSR), CL = VDD	-6.00		6.00	
		V_{IN} = 48V, $V_{IN-SENSE}$ = 44mV (80% IINFSR), CL = GND	-4.00		4.00	
Remote Diode Temperature Sensor						
Temperature Accuracy Using Local Diode (3)	T_{ACC}			2	10	℃
Remote Diode Resolution				9		bits
External Diode Current Source	I_{DIODE}	High level		260	325	μA
		Low level		10		
Diode Current Ratio				26		
PMBus Pin Thresholds (nSMBA, SDA, SCL)						
Data, Clock Input Low Voltage	V_{IL}				0.9	V
Data, Clock Input High Voltage	V_{IH}		2.1		5.5	V
Data Output Low Voltage	V_{OL}	I_{SINK} = 3mA	0		0.4	V
Input Leakage Current	I_{LEAK}	SDAI, nSMBA, SCL = 5V			1	μA
Configuration Pin Thresholds (CL, nRETRY)						
Threshold Voltage	V_{IH}		3			V
Input Leakage Current	I_{LEAK}	CL, nRETRY = 5V		5		μA

NOTES:

1. OUT bias current (disabled): originates from leakage current flowing through the internal 1MΩ resistor between SENSE and OUT.

2. Initial accuracy.

3. This parameter is guaranteed by design and characterization; not production.

TIMING REQUIREMENTS

PARAMETER	SYMBOL	MIN	MAX	UNITS
SMBus Operating Frequency	f_{SMB}	10	400	kHz
Bus Free Time from Stop to Start Condition	t_{BUF}	1.3		μs
Start Hold Time	t_{HD_STA}	0.6		μs
Repeated Start Condition Setup Time	t_{SU_STA}	0.6		μs
Stop Condition Setup Time	t_{SU_STO}	0.6		μs
Data Hold Time	t_{HD_DAT}	85		ns
Data Setup Time	t_{SU_DAT}	100		ns
Clock Low Time-Out (1)	$t_{TIMEOUT}$	25	35	ms
Clock Low Period	t_{LOW}	1.5		μs
Clock High Period (2)	t_{HIGH}	0.6		μs
Cumulative Clock Low Extend Time (Slave Device) (3)	t_{LOW_SEXT}		25	ms
Cumulative Low Extend Time (Master Device) (4)	t_{LOW_MEXT}		10	ms
Clock or Data Signal Fall Time (5)	t_F	20	300	ns
Clock or Data Signal Rise Time (5)	t_R	20	300	ns

NOTES:

1. Device involved in a data transfer will trigger a timeout if the clock remains low for longer than the minimum timeout value ($t_{TIMEOUT_MIN}$) of 25ms. Upon detecting a timeout, devices must reset the communication process no later than the maximum timeout threshold ($t_{TIMEOUT_MAX}$) of 35ms. Both master and slave devices shall comply with this maximum limit, which covers the combined stretch limits of the master (10ms) and slave (25ms).

2. The maximum high time (t_{HIGH_MAX}) serves as a straightforward means for devices to identify bus idle states.

3. t_{LOW_SEXT}: the maximum cumulative time a slave may stretch the clock within a single message, spanning from the start condition to the stop condition. A slave device that exceeds this limit shall release both the clock and data lines and perform a self-reset.

4. t_{LOW_MEXT}: the maximum cumulative clock-stretching time permitted for a master per byte of a message, covering the intervals of start-to-acknowledge, acknowledge-to-acknowledge, or acknowledge-to-stop.

5. Rise time (t_R) and fall time (t_F) are defined as follows: t_R spans from (V_{ILMAX} - 0.15V) to (V_{IHMIN} + 0.15V), and t_F ranges from 0.9 × V_{DD} to (V_{ILMAX} - 0.15V).

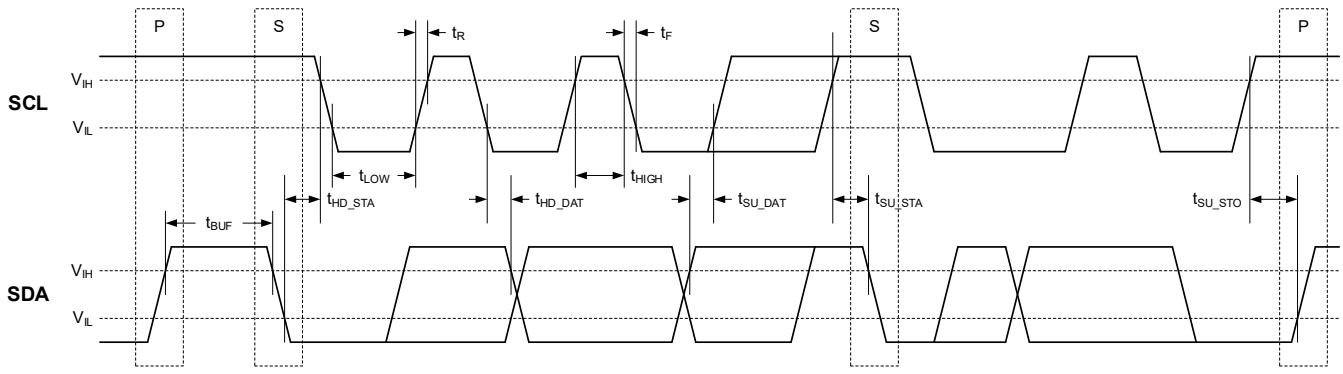


Figure 2. SMBus Timing Diagram

SWITCHING CHARACTERISTICS

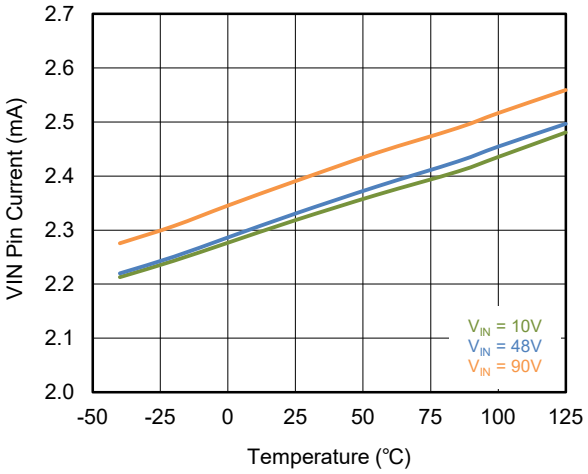
(V_{IN} = 48V, V_{UVLO} = 3V, V_{OVLO} = 0V, R_{PWR} = 20kΩ, typical values are measured at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
UVLO/EN, OVLO Pins						
UVLO Delay	$UVLO_{DEL}$	Delay to GATE high		15		μs
		Delay to GATE low		9		
OVLO Delay	$OVLO_{DEL}$	Delay to GATE high		15		μs
		Delay to GATE low		9		
FB Pin						
FB Delay	FB_{DEL}	Delay to PGD high		7		μs
		Delay to PGD low		9.3		
Current Limit						
Response Time	t_{CL}	$V_{IN-SENSE}$ stepped from 0V to 80mV, CL = GND		22		μs
Circuit Breaker						
Response Time	t_{CB}	$V_{IN-SENSE}$ stepped from 0V to 150mV, time to GATE low, no load		0.33	0.80	μs
Timer (TIMER Pin)						
Fault to GATE Low Delay	t_{FAULT_DELAY}	The TIMER pin attains the upper threshold level		12		μs

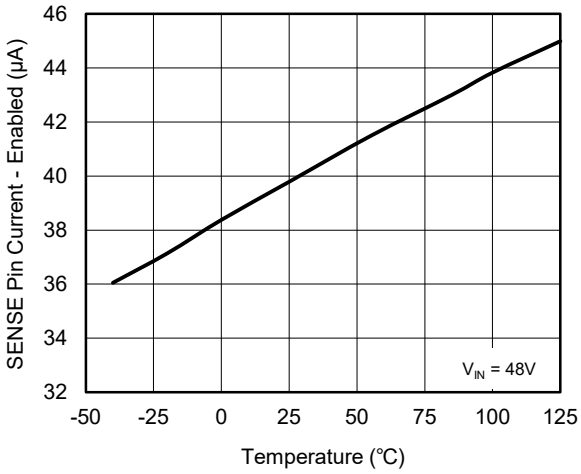
TYPICAL PERFORMANCE CHARACTERISTICS

T_J = +25℃, unless otherwise noted.

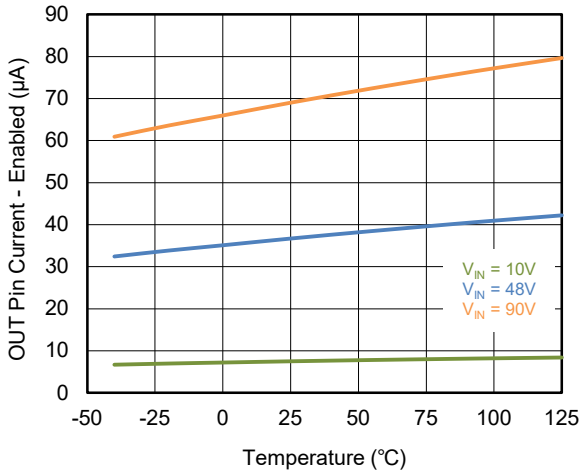
VIN Pin Current vs. Temperature



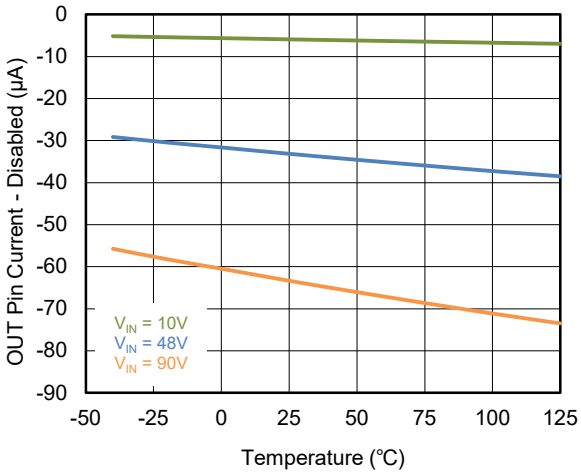
SENSE Pin Current - Enabled vs. Temperature



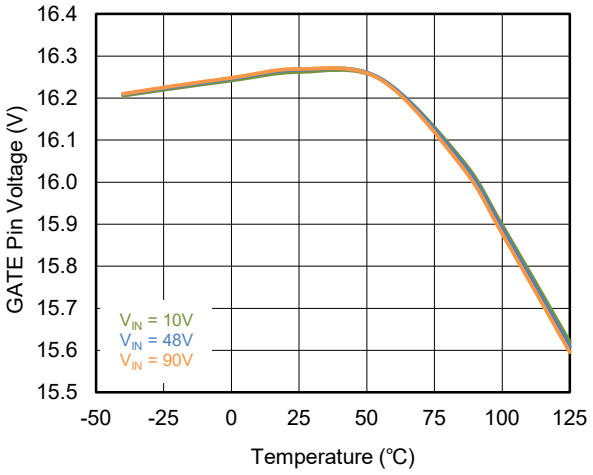
OUT Pin Current - Enabled vs. Temperature



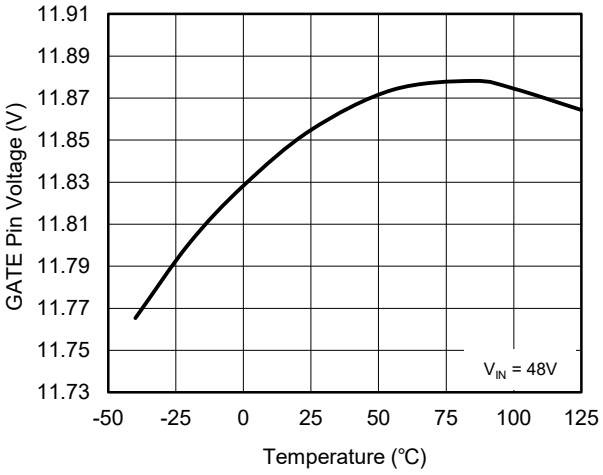
OUT Pin Current - Disabled vs. Temperature



GATE Zener Reverse Bias Voltage (V_{GATE} - V_{OUT}) vs. Temperature



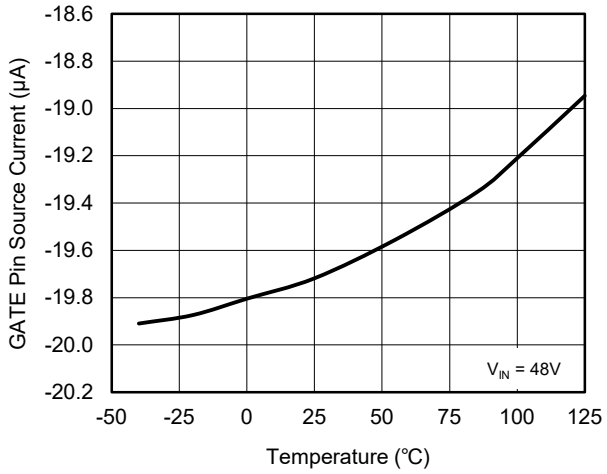
GATE Peak Charge Pump Voltage (V_{GATE} - V_{OUT}) vs. Temperature



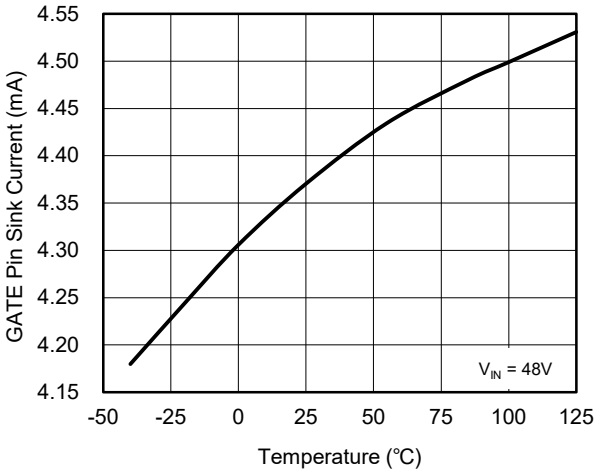
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_J = +25℃, unless otherwise noted.

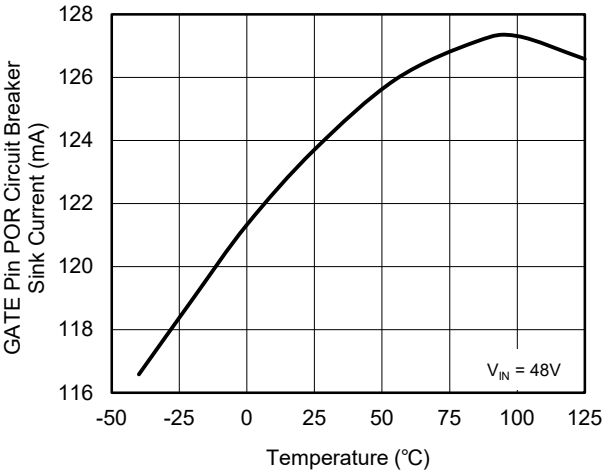
GATE Pin Source Current vs. Temperature



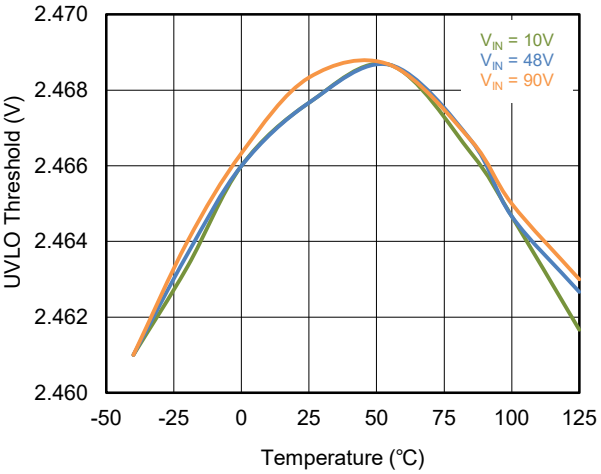
GATE Pin Sink Current vs. Temperature



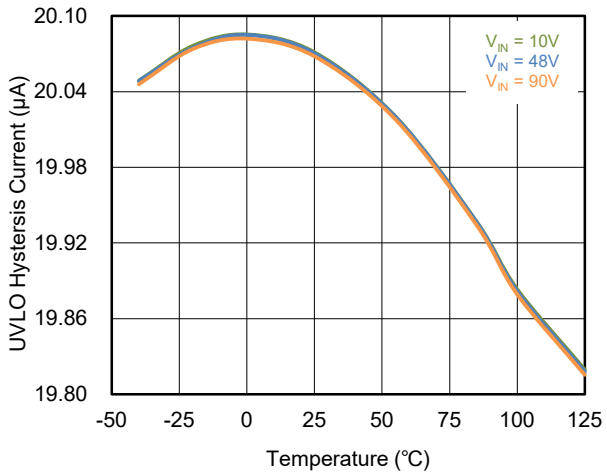
GATE Pin POR Circuit Breaker Sink Current vs. Temperature



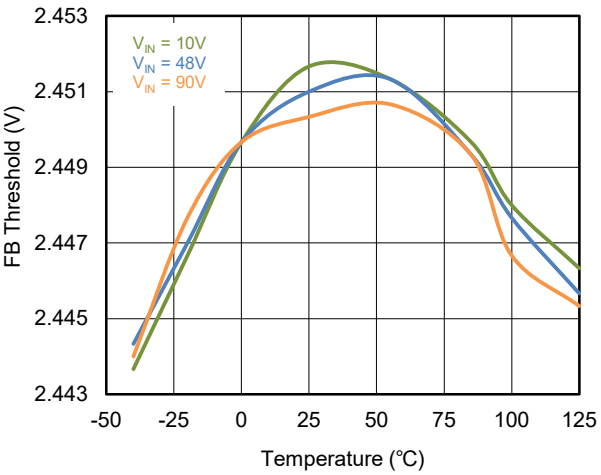
UVLO Threshold vs. Temperature



UVLO Hysteresis Current vs. Temperature



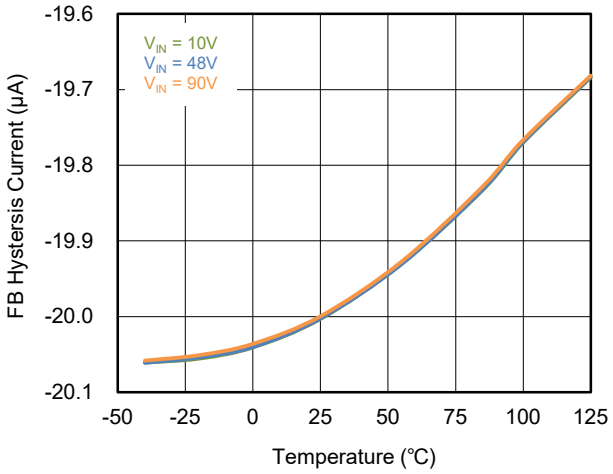
FB Threshold vs. Temperature



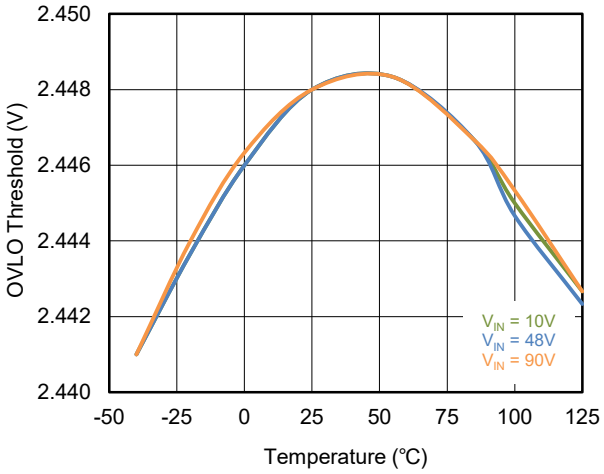
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_J = +25℃, unless otherwise noted.

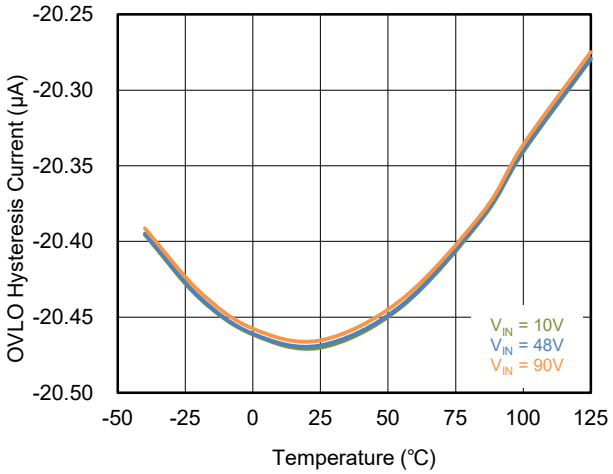
FB Hysteresis Current vs. Temperature



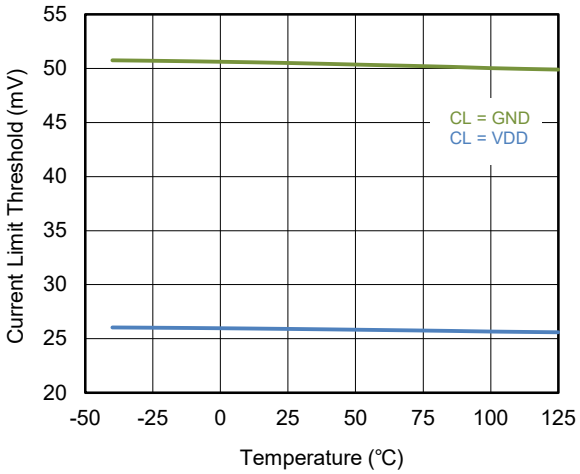
OVLO Threshold vs. Temperature



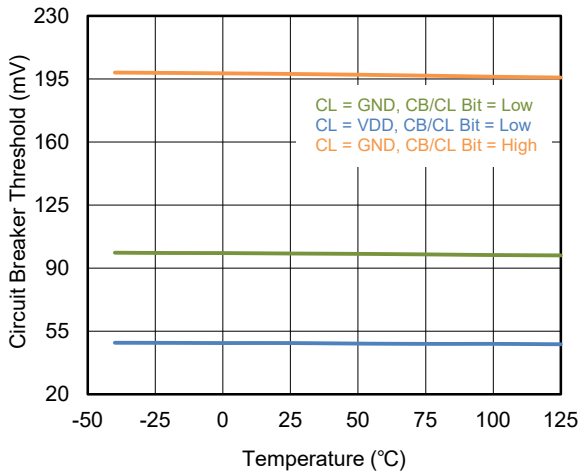
OVLO Hysteresis Current vs. Temperature



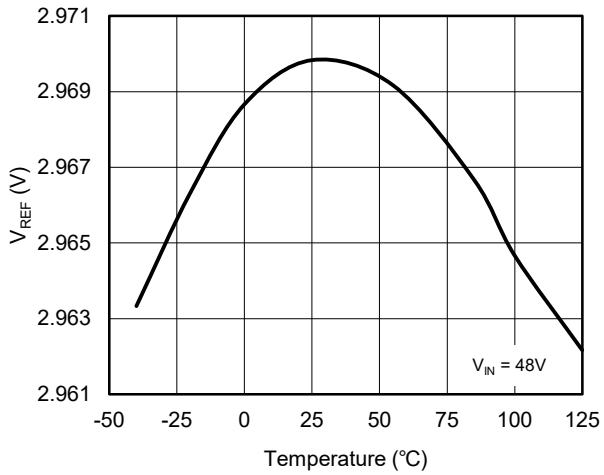
Current Limit Threshold vs. Temperature



Circuit Breaker Threshold vs. Temperature

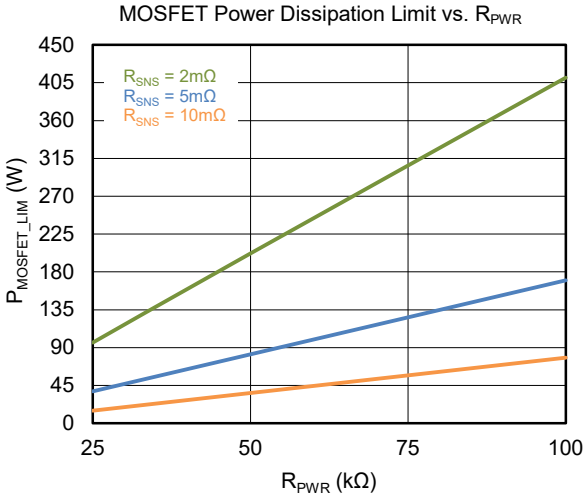


Reference Voltage vs. Temperature



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

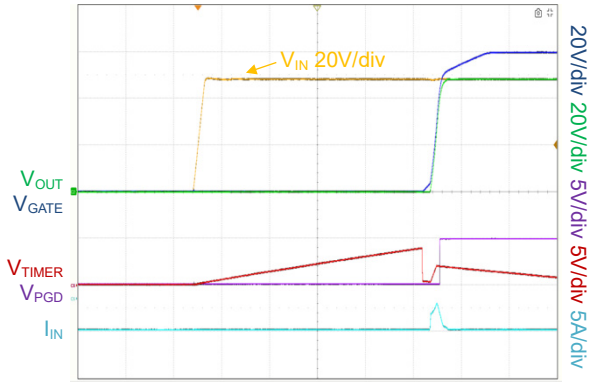
T_J = +25℃, unless otherwise noted.



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

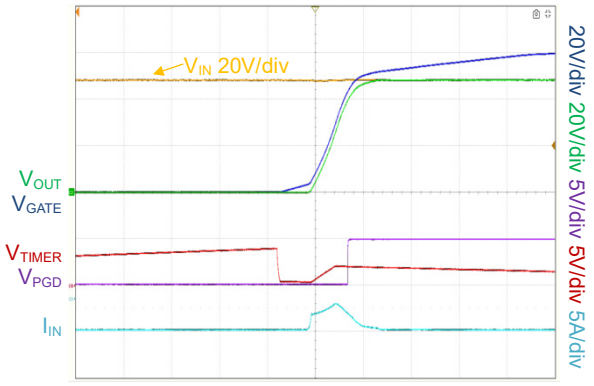
T_J = +25℃, V_{IN} = 48V, unless otherwise noted.

Insertion Delay



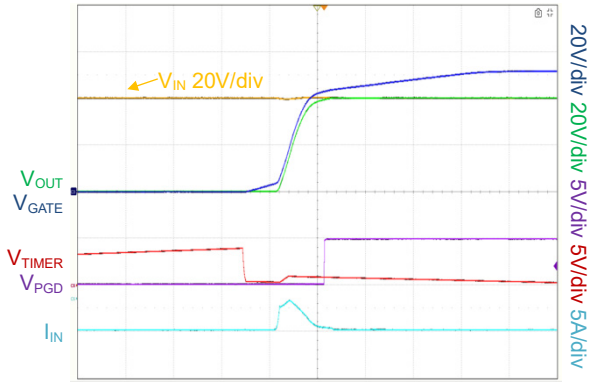
Time (20ms/div)

Start-Up



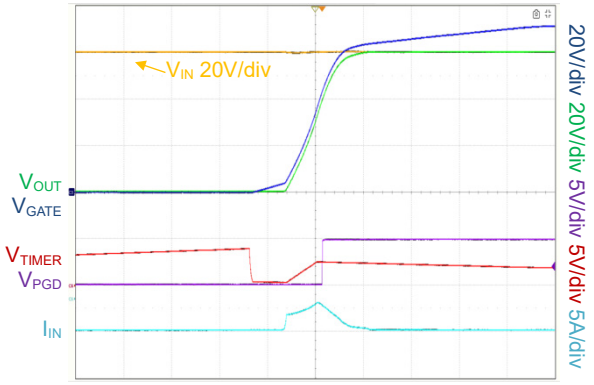
Time (5ms/div)

Start-Up (V_{IN} = 40V)



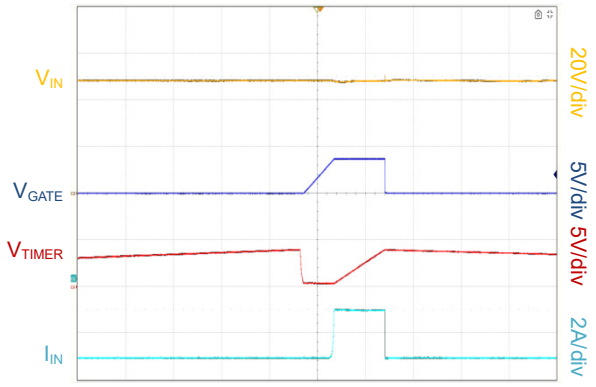
Time (5ms/div)

Start-Up (V_{IN} = 60V)



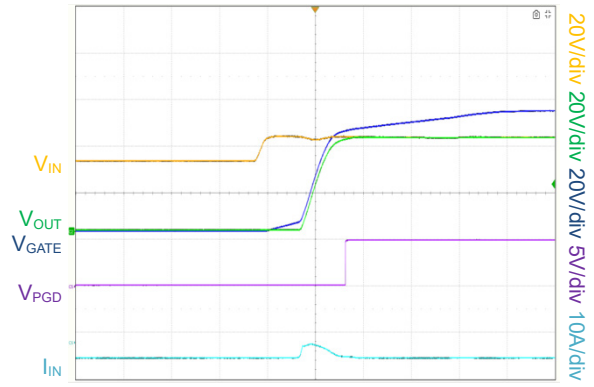
Time (5ms/div)

Start-Up into Short-Circuit



Time (5ms/div)

Under-Voltage

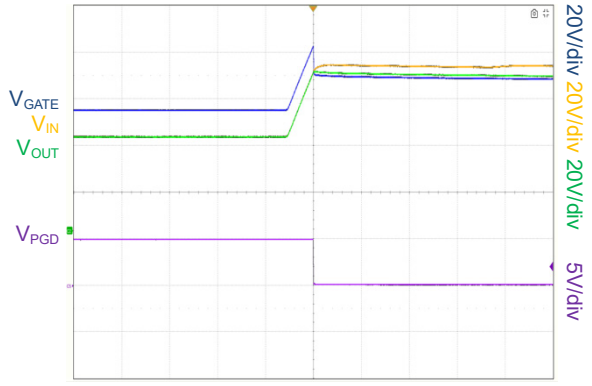


Time (5ms/div)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

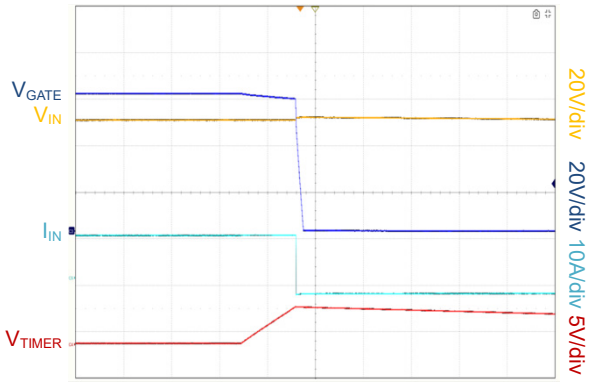
T_J = +25℃, V_{IN} = 48V, unless otherwise noted.

Over-Voltage



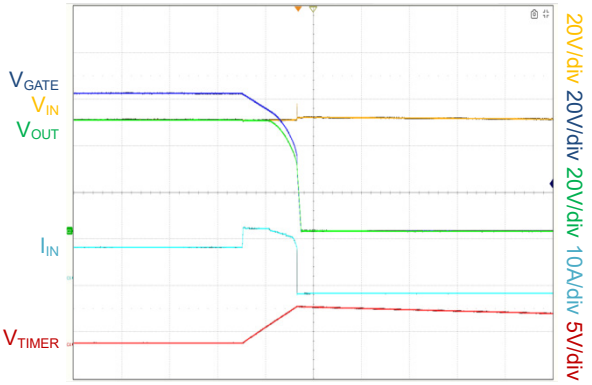
Time (5ms/div)

Gradual Over-Current



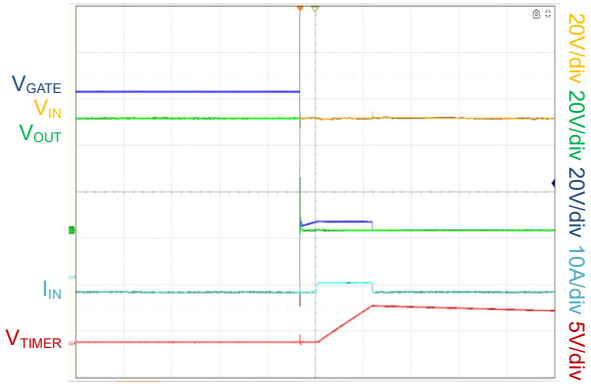
Time (5ms/div)

Loadstep



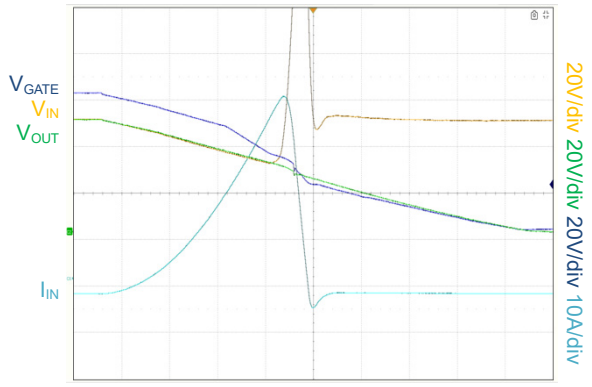
Time (5ms/div)

Hot-Short on Output (Zoomed Out)



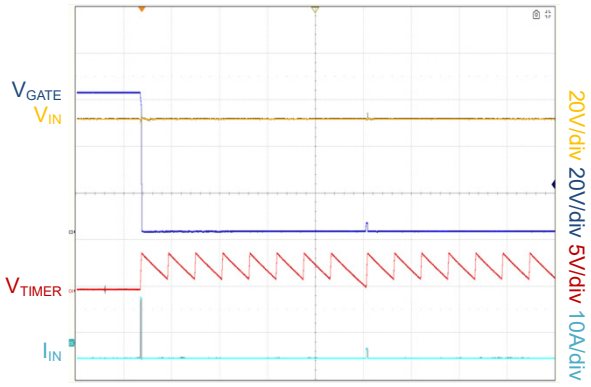
Time (5ms/div)

Hot-Short on Output (Zoomed In)



Time (2μs/div)

Auto-Retry



Time (200ms/div)

FUNCTIONAL BLOCK DIAGRAM

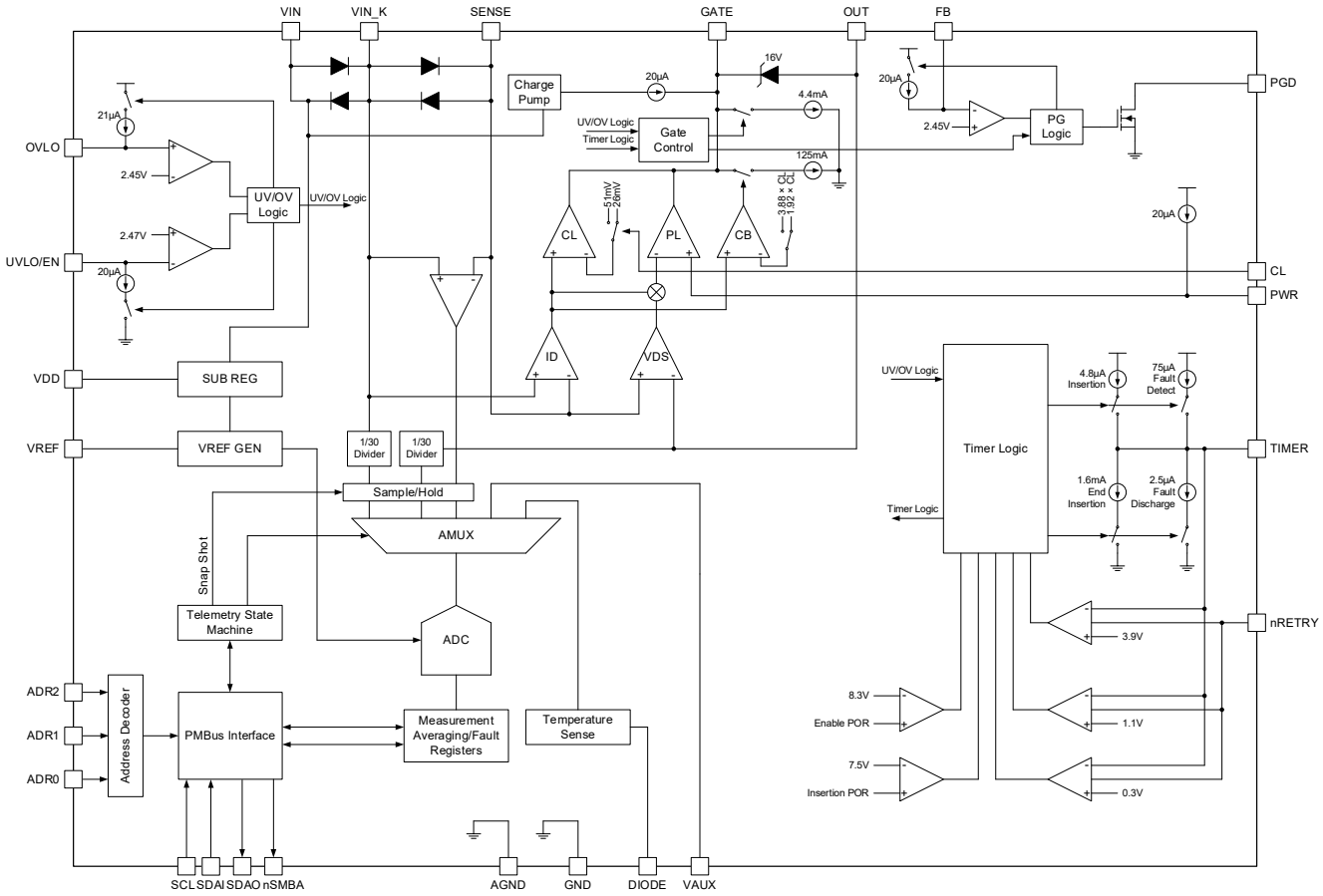


Figure 3. Block Diagram

DETAILED DESCRIPTION

Overview

The SGM25716L is a high-performance hot-swap controller for 10V to 90V system with an SMBus/I^2C interface compliant with PMBus standards. Via the SMBus interface, the SGM25716L provides continuous real-time monitoring of power, voltage, current, temperature, and fault conditions through the SMBus/I^2C interface, reporting all data to the system management host.

SGM25716L delivers current and power limiting capabilities, which safeguards sensitive circuitry when boards are inserted into a live system backplane or any other active power source. Additionally, a rapid-response circuit breaker prevents damage if a short circuit occurs at the output. Key parameters such as input under-voltage and over-voltage levels, hysteresis, insertion delay time, and fault detection time are all configurable. The SGM25716L also features a temperature monitoring module that interfaces with a low-cost external diode. This diode is used to monitor the temperature of external MOSFETs or other thermally sensitive components. The Power Good output serves as a quick indicator whenever input or output voltages deviate from their programmed ranges.

The monitoring module of the SGM25716L calculates two types of values for subsystem operating parameters (V_{IN}, I_{IN}, P_{IN}, and V_{OUT}), real-time values and average values. It also computes the peak power of the subsystem. Accurate power averaging is achieved by calculating the average of the product derived from input voltage and input current.

The SGM25716L features enhanced telemetry accuracy and supports for the READ_EIN command for energy monitoring.

Feature Description

Current Limit

The current-limit threshold is triggered when the voltage across sense resistor R_{SNS} (between VIN_K and SENSE) exceeds the ILIM level which is 26mV when CL is tied to VDD and 51mV when CL is tied to GND. Under current-limiting operation, the GATE voltage is regulated to limit the current through MOSFET Q_1, and the fault timer operates as defined within the Fault Timer and Restart section. Upon completion of the fault timeout period programmed by C_{TIMER}, one of the two states is reached. If the load current has fallen below the current-limit threshold by then, the SGM25716L returns to normal operation. If current-limit is still in effect, the STATUS_INPUT[2] bit, the READ_DIAGNOSTIC_WORD[3] bit, and the STATUS_WORD[13] bit are set high and the nSMBA pin is asserted. Assertion of nSMBA can be masked via the ALERT_MASK register (0xD8). For reliable operation, R_{SNS} must not exceed 200mΩ. It is possible for bigger resistance values to cause unstable behavior of the current-limit control loop. The current-limit threshold set by pin may be superseded by programming the associated bits of register DEVICE_SETUP (0xD9).

Circuit Breaker

When load current rises sharply, such as during a load short-circuit fault, the current through sense resistor R_{SNS} is capable of exceeding the current-limit threshold before the control loop responds. If the current reaches 1.92 times the current-limit threshold, or 3.88 times the threshold when the CL pin is tied to GND, the GATE 125mA pull-down current rapidly turns off Q_1 and initiates the fault timeout period. After the R_{SNS} voltage drops under the CB trigger level, the 125mA GATE pull-down path turns off, and the Q_1 gate voltage gets controlled via either the current-limit or power-limit mechanism. Should the TIMER pin hit 3.9V before the limit operation ends, the 4.4mA GATE pull-down current switches Q_1 off (see the Fault Timer and Restart section). Upon a circuit breaker event, the STATUS_OTHER[5], STATUS_MFR_SPECIFIC[7], and READ_DIAGNOSTIC_WORD[0] bits is set high, and the nSMBA pin is asserted. This alert action can be disabled by programming the ALERT_MASK (0xD8) register. The hardware pin-defined circuit breaker setting can be overwritten by configuring corresponding bits within the DEVICE_SETUP (0xD9) register.

DETAILED DESCRIPTION (continued)

Power Limit

MOSFET power limiting constitutes a key function of the SGM25716L. The power limit feature keeps the maximum power dissipation of MOSFET Q_1 inside the SOA rating of the device. The SGM25716L calculates Q_1 power dissipation from its drain-source voltage (SENSE to OUT) and drain current (via R_{SNS}, VIN_K to SENSE), and compares the V × I product against the power-limit threshold set by the resistor connected to the PWR pin. When the power-limit threshold is crossed, modulation of the GATE potential serves to stabilize the current flowing across Q_1. With the power-limiting circuit enabled, the fault timer runs per the Fault Timer and Restart section. If power limiting persists beyond the fault timeout period defined by C_{TIMER}, the STATUS_INPUT[2] bit, the STATUS_WORD[13] bit, and the READ_DIAGNOSTIC_WORD[3] bit are set high and the nSMBA pin is asserted. This alert can be masked via the ALERT_MASK (0xD8) register.

UVLO

Q_1, the series-pass MOSFET, turns on only while V_{IN} stays within the operating window bounded by the programmable UVLO and OVLO thresholds. The V_{IN} UVLO level is normally set by a resistor divider network. As Figure 3 shows, the internal 20μA UVLO current source is active and the OVLO current source stays off when V_{IN} sits below the UVLO threshold, and the 4.4mA GATE pulldown keeps Q_1 off. When V_{IN} climbs and the UVLO pin voltage passes its threshold, the 20μA source switches off, pulling the UVLO pin voltage up and providing threshold hysteresis. Once the UVLO/EN pin voltage exceeds the threshold and the insertion delay elapses, the 20μA GATE current source turns Q_1 on.

Refer to the APPLICATION INFORMATION section for the calculation method of threshold-setting resistors. Tying the UVLO/EN pin directly to VIN achieves the minimum V_{IN} UVLO level, and Q_1 is enabled after the insertion delay once V_{IN} reaches the POR threshold. After power-up, a UVLO fault sets the STATUS_WORD[13] bit, the STATUS_INPUT[4] bit, and the READ_DIAGNOSTIC_WORD[5] bit high, and pulls the nSMBA pin low. This alert function can be masked by programming the ALERT_MASK (0xD8) register.

OVLO

The series-pass MOSFET Q_1 turns on while the input supply voltage V_{IN} stays within the operating window set by programmable UVLO and OVLO thresholds. When V_{IN} makes the voltage at the OVLO pin surpass its threshold, the 4.4mA GATE pulldown current turns off Q_1 and cuts off power supply to the load. When the OVLO voltage rises above the threshold, the internal 21μA current source turns on and pulls the pin voltage up, providing threshold hysteresis. Q_1 will be re-enabled once V_{IN} drops below the OVLO threshold. When an OVLO fault occurs, the STATUS_INPUT[7] bit, the STATUS_WORD[13] bit, and the READ_DIAGNOSTIC_WORD[4] bit are latched high. The ALERT_MASK register (0xD8) can mask this alert, otherwise, the nSMBA pin will be driven to a low state.

Refer to the APPLICATION INFORMATION section for the calculation procedure of threshold-setting resistors.

Power Good Pin

The PGD output is the drain of an internal N-channel MOSFET. This transistor blocks up to 80V in the off-state and survives transients up to 100V. A pull-up resistor must bias PGD to a suitable rail so that downstream logic can read the power status. In the off-state, the PGD level may rest above or below both V_{IN} and V_{OUT}. PGD is driven high when the FB pin voltage crosses the PGD threshold. A resistor divider from the output to the feedback network usually defines the output threshold, but the monitored signal needs not to be the output voltage. Any node can be sensed as long as the FB pin voltage stays below its absolute maximum rating. Per Figure 3, the internal 20μA FB current source stays off while FB sits below the threshold. Once the rising output voltage pushes FB above the threshold, the current source turns on and sources current out of the FB pin, raising the FB pin voltage to create threshold hysteresis. PGD is pulled low if UVLO/EN drops below its threshold or OVLO climbs above its threshold. The PGD state is readable over PMBus from the STATUS_WORD (0x79) or READ_DIAGNOSTIC_WORD (0xE1) register.

DETAILED DESCRIPTION (continued)

VDD Sub-Regulator

The SGM25716L integrates an internal linear sub-regulator. It steps down the input voltage to create a 4.9V power rail that supplies the chip's low-voltage internal circuits. When CL, nRETRY, ADR2, ADR1 and ADR0 pins require a high-level tie-up, the VDD sub-regulator shall serve as their pull-up supply. This rail can also supply pull-up bias for PGD and SMBus interface signals including SDA, SCL and nSMBA. The VDD sub-regulator is intended only for low-current use and must not be loaded with additional integrated circuits. The VDD pin implements 30mA current limiting to safeguard the SGM25716L under short-circuit conditions. A ceramic bypass capacitor of 1μF or higher is mandatory for this sub-regulator. Place the capacitor near to the VDD pin as PCB layout permits.

Remote Temperature Sensing

The SGM25716L supports remote temperature sensing using an MMBT3904 NPN transistor. Connect the MMBT3904's base and collector to the DIODE pin, and tie its emitter to the SGM25716L ground. For hot-swap MOSFET Q_1 temperature sensing, place the MMBT3904 near to Q_1 as the PCB layout allows. Parasitic resistance in the path from the DIODE pin to the MMBT3904 must be minimized in the PCB layout to avoid degrading the measurement. SGMICRO recommends a Kelvin trace from the MMBT3904 emitter back to the IC ground to preserve measurement accuracy. A 1000pF small bypass capacitor shall be fitted in parallel with the MMBT3904 to suppress noise impact. The measured temperature is accessible via the PMBus READ_TEMPERATURE_1 command (0x8D). According to factory default settings, the nSMBA pin is pulled low once the measured temperature rises above +125℃, and Q_1 will be disabled when temperature exceeds +150℃. Users can reconfigure these thresholds over the PMBus interface with OT_WARN_LIMIT (0x51) and OT_FAULT_LIMIT (0x4F). The DIODE pin must be tied to ground if the SGM25716L's temperature sensing and protection functions are not required.

If the device input voltage falls below the minimum operating voltage of 10V, the VREF reference voltage will drop beneath its nominal 2.97V level, which may produce incorrect temperature readings. Under high ambient temperature conditions, such faulty readings may exceed the OT_FAULT_LIMIT threshold, triggering a fault response and turning off Q_1. To clear the fault status and reset the chip in this scenario, write 0x00 then 0x80 sequentially to the OPERATION register (0x01).

Damaged MOSFET Detection

The SGM25716L provides fault detection for damage of the external MOSFET Q_1 under specific operating conditions. When the GATE voltage is low, or internal logic commands GATE to stay low, a voltage higher than 4mV across the sense resistor will set READ_DIAGNOSTIC_WORD[8], STATUS_MFR_SPECIFIC[6] bits high, and assert the nSMBA pin. This alert function can be masked by configuring the ALERT_MASK (0xD8) register. This detection scheme reliably identifies Q_1 short-circuit failures caused by drain-gate and/or drain-source damage.

Device Functional Modes

Power-Up Sequence

The SGM25716L operates with V_{IN} from 10V to 90V and supports voltage transients up to 100V. As illustrated in Figure 4, while V_{IN} rises from zero, an internal 125mA pulldown current on the GATE pin keeps the external N-channel MOSFET Q_1 off. This strong GATE pulldown avoids unintended turn-on during charging of the MOSFET's gate-drain Miller capacitance. The TIMER pin is initially pulled to ground. When V_{IN} crosses the POR threshold, the insertion delay sequence begins. During the insertion delay, the capacitor C_{TIMER} on the TIMER pin is charged by a 4.8μA current source. Regardless of V_{IN} level, a 4.4mA GATE pulldown current keeps Q_1 off. This insertion delay lets V_{IN} ringing and transients decay before Q_1 is enabled. The insertion delay ends when the TIMER pin voltage reaches 3.9V, and C_{TIMER} is then rapidly discharged via an internal 1.6mA pulldown current. Q_1 is turned on by the GATE pin only when V_{IN} exceeds the UVLO threshold. If V_{IN} remains above the UVLO threshold after insertion delay expires, the GATE charge pump supplies 20μA to charge Q_1's gate capacitance. An internal 16V Zener diode clamps the maximum gate-source voltage of Q_1.

DETAILED DESCRIPTION (continued)

While the OUT pin voltage rises, the SGM25716L senses the drain current and power dissipation of Q_1 on a continuous basis. The inrush current limiter, power limiter, or both circuits operate together to dynamically regulate the current supplied to the load. During the inrush limiting phase (t_2 in Figure 4), C_{TIMER} is charged by an internal 75μA fault-timer current source. If both Q_1 power dissipation and input current fall beneath their limit thresholds before the TIMER voltage reaches 3.9V, the charging source is disabled and C_{TIMER} is discharged by an internal 2.5μA current sink (t_3 in Figure 4). The inrush limiting function will not activate again until another current-limit event takes place.

Should the TIMER pin reach 3.9V while inrush current limiting or power limiting is still active within interval t_2, the device registers a fault and turns off Q_1. See the Fault Timer and Restart section for the complete fault behavior.

Once the input voltage rises above the POR threshold, the SGM25716L activates the nSMBA pin to signal that volatile memory and device parameters are restored to factory defaults. The STATUS_MFR_SPECIFIC[4] bit signifies that warning thresholds and device operating settings are loaded with default values. This bit stays high until the chip receives a CLEAR_FAULTS command.

Gate Control

A charge pump supplies the GATE pin voltage to drive the gate of N-channel MOSFET Q_1. Under normal operating conditions (t_3 in Figure 4), an internal 20μA current source keeps Q_1's gate node charged. The charge pump delivers a peak voltage of approximately 12V, establishing a 12V V_{GS} for Q_1 during steady-state operation. When the system supply is first applied, a 125mA pulldown current pulls the GATE pin low. This prevents unintended turn-on of Q_1 caused by charging of the drain-gate capacitance while the system voltage rises.

During the insertion time (t_1 in Figure 4), a 4.4mA pulldown current holds the GATE pin low. Q_1 remains off for the entire t_1 interval, independent of V_{IN} or UVLO status. After insertion time completes, in interval t_2 shown in Figure 4, Q_1 gate voltage is dynamically modulated to prevent current or power dissipation from exceeding user-programmed limits. The capacitor on the TIMER pin charges while current limiting or power limiting is active. If current and power limiting end before the TIMER voltage reaches 3.9V, C_{TIMER} discharges and the circuit returns to normal operation. If the inrush limiting condition persists and TIMER pin reaches 3.9V within t_2, the 4.4mA pulldown current pulls GATE low. GATE stays low until either a power-up sequence is triggered (nRETRY tied to VDD) or an automatic retry is performed (nRETRY grounded or left floating). See the Fault Timer and Restart section for more details. When the system input voltage drops below UVLO threshold or rises above OVLO threshold, the 4.4mA pulldown current pulls GATE low to turn off Q_1.

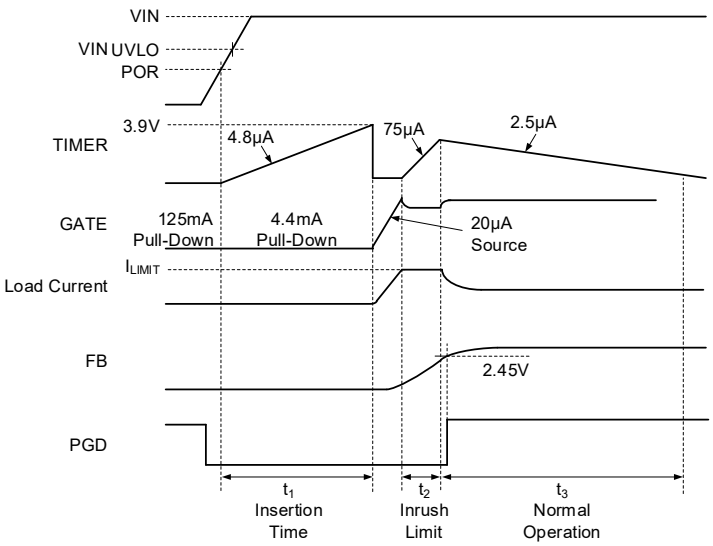


Figure 4. Power-Up Sequence (Current Limit Only)

DETAILED DESCRIPTION (continued)

Fault Timer and Restart

If the current-limit or power-limit threshold is tripped during turn-up or by a fault event, the Q_1 gate-source voltage is modulated to regulate load current and Q_1 power dissipation. Whenever either limiting function is enabled, a 75μA fault timer current source charges the external capacitor C_{TIMER} connected to the TIMER pin, corresponding to the fault timeout interval illustrated in Figure 4. If the fault clears within the timeout window before the TIMER pin voltage rises to 3.9V, the SGM25716L reverts to normal operation, and C_{TIMER} is discharged via a 1.6mA current sink. If the TIMER pin reaches 3.9V before the fault subsides, the 4.4mA GATE pulldown current turns off Q_1. The following restart sequence is determined by the configured retry mode.

When the nRETRY pin is tied high, the SGM25716L latches the GATE pin low upon expiration of the fault timeout interval. The C_{TIMER} capacitor is then discharged to GND via a 2.5μA fault current sink. The 4.4mA pulldown current keeps the GATE pin low until an external power-up sequence is triggered. This can be accomplished by cycling the input supply V_{IN}, or by briefly pulling the UVLO/EN pin below its threshold using an open-collector or open-drain driver as illustrated in Figure 5. The restart sequence will only work when the TIMER pin voltage is less than 0.3V. The READ_DIAGNOSTIC_WORD[9] bit stays asserted as long as the latched shutdown state remains active.

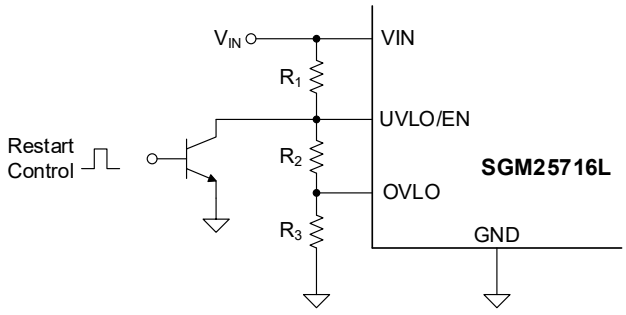


Figure 5. Latched Fault Restart Control

The SGM25716L implements an automatic restart sequence. After fault timeout expires, the TIMER pin swings between 3.9V and 1.1V for seven cycles, as depicted in Figure 6. The cycle time is defined by the 75μA charge current, 2.5μA discharge current and capacitance value of C_{TIMER}. On the 8th high-to-low voltage ramp, once the TIMER pin voltage falls to 0.3V, the 20μA GATE current source activates Q_1. If the fault persists, the fault timeout and restart sequence will repeat. The nRETRY pin offers two coarse options: no retry or infinite retries. Users can configure retry behavior with higher granularity via the DEVICE_SETUP register (0xD9). By programming the corresponding bits in DEVICE_SETUP (0xD9), available retry counts include 0, 1, 2, 4, 8, 16, or infinite retries.

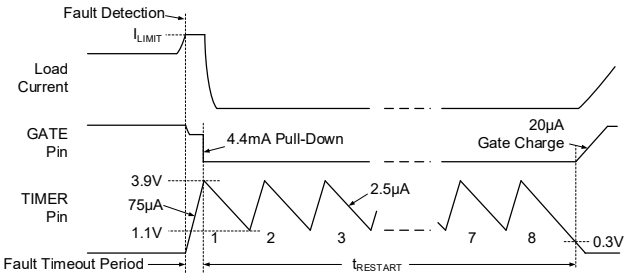


Figure 6. Restart Sequence

Shutdown Control

Remote load current shutdown is achievable by pulling the UVLO/EN pin below its threshold using an open-collector or open-drain driver, illustrated in Figure 7. Once the UVLO/EN pin is released, the SGM25716L turns on the external FET with inrush current limiting and power limiting active.

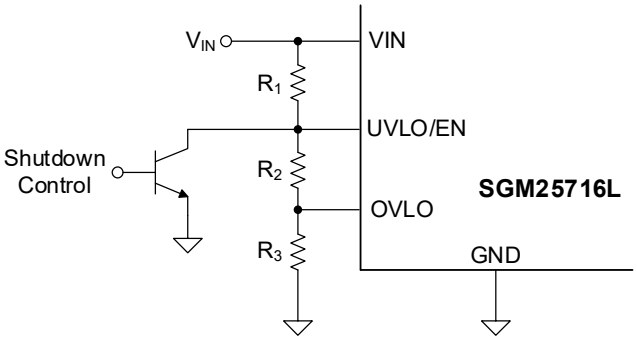


Figure 7. Shutdown Control

DETAILED DESCRIPTION (continued)

Enabling/Disabling and Resetting

During normal operation, the output can be disabled by pulling the UVLO/EN pin below its threshold or driving the OVLO pin above its threshold. This forces the GATE voltage low via a 4.4mA pulldown current. Toggling UVLO/EN can also release the SGM25716L from latched shutdown triggered by overcurrent or overpower faults once the maximum retry count has been exhausted. Although UVLO/EN and OVLO pins are capable of disabling the output, they do not alter the volatile memory or device address of the SGM25716L. As long as the chip remains powered, SMBus programmed parameters including device address, operating mode, warning and fault thresholds will be retained, independent of UVLO/EN and OVLO pin status. The output can also be turned on or off by writing 0x80 or 0x00 to the OPERATION register (0x01). To re-enable the output after a fault event, clear the fault status by sequentially writing 0x00 followed by 0x80 into OPERATION (0x01).

At power-up, the SGM25716L samples its SMBus address from the logic levels on ADR0, ADR1 and ADR2 (GND, NC or VDD). The sampled address is stored in a volatile register once V_{DD} crosses the 4.1V POR threshold. Grounding the VREF pin lets users reassign or postpone address capture. Pulling VREF low also resets the internal logic and wipes the volatile memory of the SGM25716L. After VREF is released, its voltage ramps to its final level, and the address is latched into the volatile register once the VREF voltage passes 2.55V.

TYPICAL APPLICATION

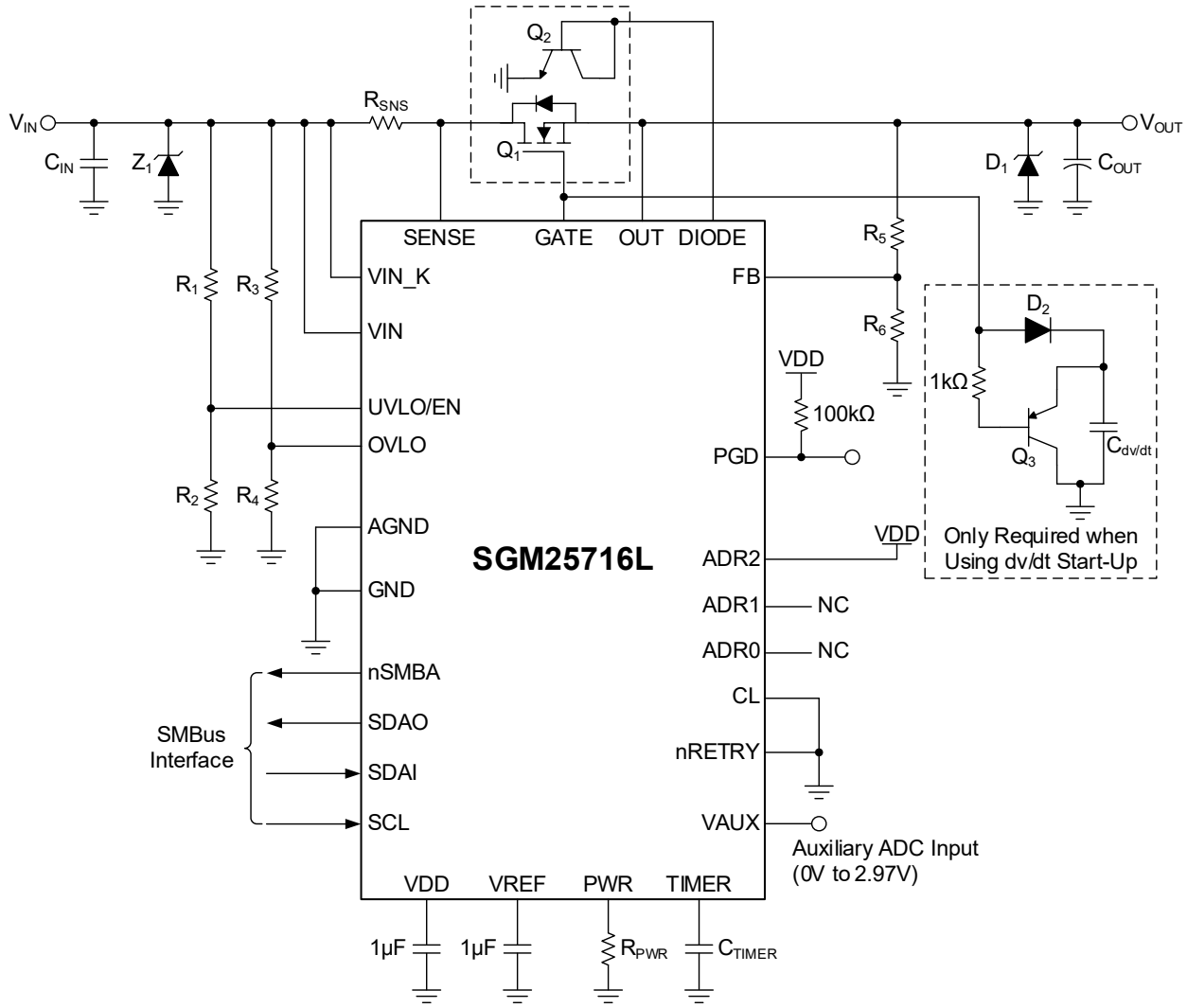


Figure 8. Typical Application Circuit

APPLICATION INFORMATION

The SGM25716L is a hot-swap controller equipped with a PMBus interface. It reports current, voltage, power and status data to the host system. As a hot-swap device, it controls inrush current and implements fault protection. Three critical operating cases must be evaluated during hot-swap design:

- Start-up.
- The hot-swap output is shorted to ground while the hot-swap controller remains enabled. This condition is commonly known as a hot-short event.
- Board power-up occurs while its output node is shorted to ground. This operating condition is generally referred to as start-into-short.

All these operating conditions impose heavy stress on the hot-swap MOSFET. Special design considerations are required to ensure that the MOSFET operates inside its SOA. Detailed design examples are presented in subsequent sections. Manual calculation of all equations is tedious and prone to mistakes. Manual calculation of all equations is tedious and prone to mistakes. Instead, SGMICRO recommends using the SGM25716L design calculator provided on the product page.

Design Requirements

Table 1 lists the design parameters required prior to hot-swap circuit development. When the hot-swap MOSFET charges the output capacitor, the energy it dissipates equals to the energy stored in the output capacitor (1/2CV²). The stress on the MOSFET is thus set by both the input voltage and the output capacitance. Maximum load current dictates the current limit setting and the choice of sense resistor. Furthermore, maximum load current, peak ambient temperature and PCB thermal characteristic $R_{\theta CA}$ govern selection of MOSFET $R_{DS(ON)}$ and parallel MOSFET quantity. $R_{\theta CA}$ is heavily affected by PCB layout and the copper area attached to the MOSFET drain. Keep in mind that the drain node has no electrical connection to the ground plane; the ground plane therefore cannot serve as a heat sink. This design example adopts $R_{\theta CA}$ = 30℃/W, matching the performance of the SGM25716L EVM. It is recommended to measure $R_{\theta CA}$ for the actual design once prototype PCBs are fabricated.

Lastly, it is critical to define the test requirements that the hot-swap circuit must satisfy. Typically, the hot-swap controller is designed to withstand both hot-short and start-into-short events introduced in the preceding section. SGMICRO further advises that the load remains disabled until the hot-swap completes its power-up sequence. Enabling the load prematurely introduces extra stress to the MOSFET, which may result in MOSFET damage or failed startup.

Table 1. Design Parameters

PARAMETER	EXAMPLE VALUE
Input voltage range	40V to 60V
Maximum load current	10A
Maximum output capacitance of the hot-swap	220μF
Maximum ambient temperature	85℃
MOSFET $R_{\theta CA}$ (function of layout)	30℃/W
Pass hot-short on output?	Yes
Pass a start into short?	Yes
Is the load off until PG asserted?	Yes
Can a hot board be plugged back in?	Yes

Detailed Design-In Procedure

Select R_{SNS} and CL Setting

The SGM25716L supports two V_{CL} options: 26mV and 51mV. The 26mV threshold yields a smaller R_{SNS} and reduced I²R conduction loss. By contrast, the 51mV option improves current and power telemetry accuracy and permits a lower minimum power-limit setting. This design picks the 26mV option by connecting the CL pin to VDD straightly. SGMICRO recommends setting the target current limit no less than 10% higher than the maximum load current, to accommodate the tolerance of the SGM25716L current limit circuit. With a target current limit of 11A, the sense resistance is calculated below:

$$R_{SNS,CLC} = \frac{I_{LIM}}{V_{CL}} = \frac{26mV}{11A} = 2.36m\Omega \quad (1)$$

Sense resistors are generally offered in standard discrete values. Where high precision of current limit is required, a sense resistor combined with a resistor divider network may be adopted, as illustrated in Figure 9.

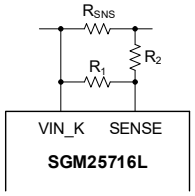


Figure 9. SENSE Resistor Divider

APPLICATION INFORMATION (continued)

Select the next higher standard value for the sense resistor (3mΩ for this example). The ratio between R_1 and R_2 can be calculated as below:

$$\frac{R_1}{R_2}=\frac{R_{SNS,CLC}}{R_{SNS}-R_{SNS,CLC}}=\frac{2.36m\Omega}{3m\Omega-2.36m\Omega}=3.69 \quad (2)$$

It should be noted that the SENSE pin sinks 40μA current and generates an offset voltage over R_2. SGMICRO recommends limiting R_2 to less than 10Ω to minimize this offset. Furthermore, 1% tolerance resistors contribute additional error to current measurement. When the resistor divider topology is adopted, users shall calculate the effective sense resistance $R_{SNS,EFF}$ via Equation 3 and substitute $R_{SNS,EFF}$ for R_{SNS} in all calculations.

$$R_{SNS,EFF}=\frac{R_{SNS}\times R_1}{R_1+R_2} \quad (3)$$

It should be noted that high-precision current limit is unnecessary for numerous applications. Under such circumstances, selecting the next lower standard sense resistor provides a simpler solution. For this design, a 2mΩ resistor yields a 13A current limit.

Selecting the Hot-Swap FETs

Proper MOSFET selection is critical in hot-swap design. The chosen device shall satisfy the following criteria:

- The V_{DS} voltage rating must withstand the maximum system voltage plus ringing induced by transient events. A 100V FET is recommended for most 48V systems.
- The FET SOA must fully cover all operating conditions: power-up, hot-short and start-into-short.
- The $R_{DS(ON)}$ value shall be low enough to keep junction and case temperatures under the device maximum absolute ratings. SGMICRO further recommends limiting the steady-state FET temperature below +125℃ to preserve thermal margin for transient stress.
- The maximum continuous drain current rating shall exceed the maximum load current, and the pulsed drain current must be higher than the circuit-breaker current threshold. Most MOSFETs satisfying the preceding three criteria also meet these two specifications.
- A ±20V V_{GS} rating is mandatory, since the SGM25716L is capable of driving the gate up to 16V above the source node.

The PSMN4R8-100BSE is chosen for this design due to its low $R_{DS(ON)}$ and excellent SOA characteristic. Once the MOSFET is selected, the maximum steady-state case temperature can be calculated as shown below:

$$T_{C,MAX}=T_{A,MAX}+R_{\theta CA}\times I_{LOAD,MAX}{}^2\times R_{DS(ON)}(T_J) \quad (4)$$

Junction temperature exerts a significant influence on $R_{DS(ON)}$. For the majority of D2PACK packaged MOSFETs, junction temperature closely tracks case temperature. Multiple calculation cycles using the earlier equations can be applied to converge the final $R_{DS(ON)}$ and $T_{C,MAX}$ results. As documented in the PSMN4R8-100BSE datasheet, the device's $R_{DS(ON)}$ increases twofold at +110℃. This $R_{DS(ON)}$ parameter is adopted in Equation 5 to solve for $T_{C,MAX}$. The calculated $T_{C,MAX}$ aligns well with the assumed junction temperature for $R_{DS(ON)}$ estimation, hence, further iteration is unnecessary.

$$T_{C,MAX}=85℃+\frac{30℃}{W}\times(10A)^2\times(2\times4.8m\Omega)=114℃ \quad (5)$$

Select Power Limit

A lower power-limit setting is generally recommended to minimize stress imposed on the MOSFET. Nevertheless, when the SGM25716L is configured with an extremely low power limit, the device regulates the FET current, and accordingly the sense resistor voltage (V_{SNS}), down to a minimal level. V_{SNS} can be calculated using Equation 6.

$$V_{SNS}=\frac{P_{LIM}\times R_{SNS}}{V_{DS}} \quad (6)$$

To prevent notable performance degradation in power limiting operation, SGMICRO advises not to set V_{SNS} below 4mV. Using this criterion, the minimum permissible power limit can be calculated as shown below:

$$P_{LIM,MIN}=\frac{V_{SNS,MIN}\times V_{IN,MAX}}{R_{SNS}}=\frac{4mV\times60V}{2m\Omega}=120W \quad (7)$$

APPLICATION INFORMATION (continued)

Equation 8 allows designers to configure the power limit to $P_{LIM,MIN}$ for most application scenarios. A 1.5mV systematic offset causes the SGM25716L's P_{LIM} to deviate as the MOSFET V_{DS} changes. Equation 8 defines the R_{PWR} value such that the real power limit matches the programmed target when $V_{IN} = V_{IN,MAX}$ and V_{OUT} = 0V.

$$R_{PWR} = \frac{P_{LIM} \times R_{SNS} - 0.043}{7 \times 10^{-6}} = \frac{120 \times 0.002 - 0.043}{7 \times 10^{-6}} = 28143\Omega \quad (8)$$

Select the standard resistor value nearest to the calculated result. For this design example, a 21kΩ resistor is selected.

Set Fault Timer

The fault timer activates while the hot-swap circuit operates under power limit or current limit conditions, a scenario that occurs during start-up. Therefore, the timer must be configured with a sufficiently long timeout period to avoid timeout events at start-up. When the device starts up directly in current limit (ILIM × V_{DS} < P_{LIM}), Equation 9 can be used to calculate the maximum start-up duration.

$$t_{START,MAX} = \frac{C_{OUT} \times V_{IN,MAX}}{I_{LIM}} \quad (9)$$

For the majority of designs, including this design example, I_{LIM} × V_{DS} > P_{LIM}. The hot-swap therefore begins operation under power limit and then transitions to current limit. Under this operating condition, Equation 10 may be used to calculate the maximum start-up time.

$$t_{START,MAX} = \frac{C_{OUT}}{2} \times \left[\frac{V_{IN,MAX}^2}{P_{LIM}} + \frac{P_{LIM}}{I_{LIM}^2} \right] = \frac{220\mu F}{2} \times \left[\frac{(60V)^2}{120W} + \frac{120W}{(13A)^2} \right] = 3.38ms \quad (10)$$

The start-up time calculated above uses typical values of current limit and power limit. To guarantee that no timer timeout occurs during start-up, SGMICRO recommends configuring the fault time (t_{FLT}) as 2 × $t_{START,MAX}$, equals to 6.76ms. This margin accommodates variations of power limit, timer current and timer capacitance. Accordingly, C_{TIMER} can be calculated as shown below:

$$C_{TIMER} = \frac{t_{FLT} \times I_{TIMER}}{V_{TIMER}} = \frac{6.76ms \times 75\mu A}{3.9V} = 130nF \quad (11)$$

The next higher standard capacitor value is selected for C_{TIMER}, which is 150nF. Once the C_{TIMER} component is selected, the resulting programmed fault time may be calculated as shown below:

$$t_{FLT} = \frac{C_{TIMER} \times V_{TIMER}}{I_{TIMER}} = \frac{150nF \times 3.9V}{75\mu A} = 7.8ms \quad (12)$$

Check MOSFET SOA

After configuring power-limit and fault timer parameters, it is essential to confirm that FET operation stays inside its SOA across all test scenarios. A hot-short incident activates the circuit breaker, and the SGM25716L then restarts within power limit mode until timer timeout. Under worst-case operating conditions, MOSFET V_{DS} matches $V_{IN,MAX}$, I_{DS} is defined as $P_{LIM}/V_{IN,MAX}$, and stress lasts for t_{FLT}. This reference design subjects the MOSFET to 60V and 2A over a 7.8ms interval.

Per the SOA characteristics of the PSMN4R8-100BSE, the device withstands 60V at 30A for 1ms and 60V at 6A for 10ms. To obtain the SOA limit for 7.8ms, the relationship between SOA rating and time can be approximated as a power function for extrapolation, as illustrated below:

$$I_{SOA}(t) = a \times t^m$$

$$m = \frac{\ln(I_{SOA}(t_1)/I_{SOA}(t_2))}{\ln(t_1/t_2)} = \frac{\ln(\frac{30A}{6A})}{\ln(\frac{1ms}{10ms})} = -0.7$$

$$a = \frac{I_{SOA}(t_1)}{t_1^m} = \frac{30A}{(1ms)^{-0.7}} = 30A \times (1ms)^{0.7} \quad (13)$$

$$I_{SOA}(7.8ms) = 30A \times (ms)^{0.7} \times (7.8ms)^{-0.7} = 7.12A$$

MOSFET SOA data is measured with the device case held at 25℃, but case temperature increases sharply when a hot-short fault occurs. The SOA must be de-rated according to $T_{C,MAX}$ via Equation 14:

$$I_{SOA}(7.8ms, T_{C,MAX}) = I_{SOA}(7.8ms, 25℃) \times \frac{T_{J,ABSMAX} - T_{C,MAX}}{T_{J,ABSMAX} - 25℃} = 7.12A \times \frac{175℃ - 114℃}{175℃ - 25℃} = 2.90A \quad (14)$$

From this calculation, the MOSFET survives 60V at 2.85A for 7.8ms at elevated case temperature, while the hot-short scenario needs only 2A. The resulting margin makes the design robust. SGMICRO typically calls for a MOSFET capability 1.3 times the hot-short requirement, a margin that absorbs variation in power limit and fault time.

APPLICATION INFORMATION (continued)

Set UVLO and OVLO Thresholds

With programmed UVLO and OVLO thresholds, the SGM25716L turns on the series-pass device Q_1 when the input supply voltage (V_{IN}) stays within the intended operating window. If V_{IN} drops under the UVLO threshold or climbs over the OVLO threshold, Q_1 turns off and power to the load is cut. Both thresholds include hysteresis.

Option A

The Figure 10 setup employs three resistors R_1-R_3 for threshold setting.

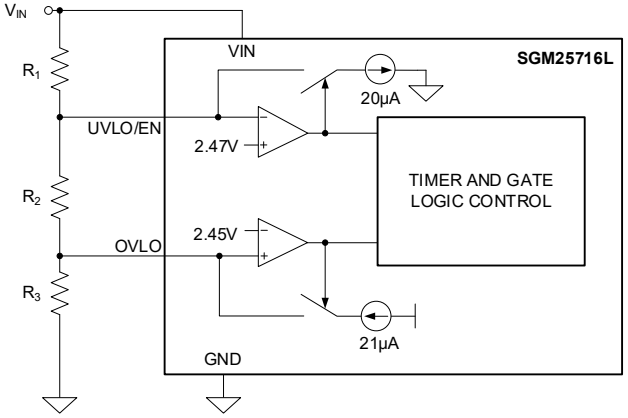


Figure 10. UVLO and OVLO Thresholds Set By R_1-R_3

Calculate the resistor values by the following procedure:

- Set the upper UVLO trigger level (V_{UVH}) and lower UVLO trigger level (V_{UVL}).
- Define the upper OVLO threshold (V_{OVH}).
- This configuration does not support predefining the lower OVLO threshold (V_{OVL}). Its value can only be calculated once R_1 through R_3 are assigned fixed values. Choose Option B when tight precision for V_{OVL} is required together with the other three threshold settings. The resistor values are obtained from the equations below:

$$R_1 = \frac{V_{UVH} - V_{UVL}}{20\mu A} = \frac{V_{UV(HYS)}}{20\mu A}$$
$$R_3 = \frac{R_1 \times V_{UVL} \times 2.45V}{V_{OVH} \times (V_{UVL} - 2.47V)} \quad (15)$$
$$R_2 = \frac{2.47V \times R_1}{V_{UVL} - 2.47V} - R_3$$

The lower OVLO threshold is given by:

$$V_{OVL} = \left[(R_1 + R_2) \times \left(\left(\frac{2.45V}{R_3} \right) - 21\mu A \right) \right] + 2.45V \quad (16)$$

After R_1 to R_3 are fixed, the threshold voltages and hysteresis are computed with the equations below:

$$V_{UVH} = 2.47V + R_1 \times (\frac{2.47V}{R_2 + R_3} + 20\mu A)$$
$$V_{UVL} = \frac{2.47V \times (R_1 + R_2 + R_3)}{R_2 + R_3} \quad (17)$$

Option B

When precise definition of all four thresholds is required, the circuit configuration shown in Figure 11 may be adopted.

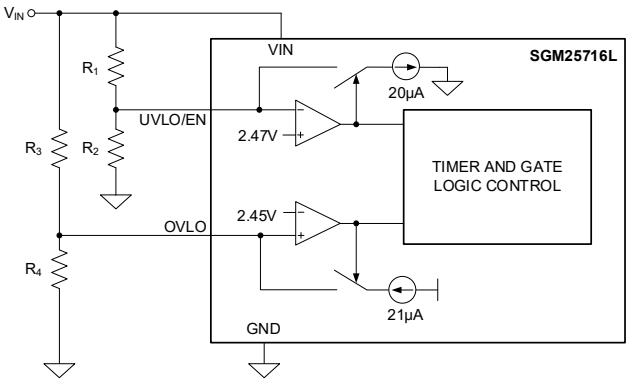


Figure 11. Programming the Four Thresholds

The four resistor values are calculated as follows:

- Select the upper and lower UVLO thresholds (V_{UVH}) and (V_{UVL}).

$$R_1 = \frac{V_{UVH} - V_{UVL}}{20\mu A} = \frac{V_{UV(HYS)}}{20\mu A}$$
$$R_2 = \frac{2.47V \times R_1}{V_{UVL} - 2.47V} \quad (18)$$

- Select the upper and lower OVLO threshold (V_{OVH}) and (V_{OVL}).

$$R_3 = \frac{V_{OVH} - V_{OVL}}{21\mu A}$$
$$R_4 = \frac{2.45V \times R_3}{V_{OVH} - 2.45V} \quad (19)$$

APPLICATION INFORMATION (continued)

- After R_1 to R_3 are fixed, the threshold voltages and hysteresis are computed with the equations below:

$$V_{UVH} = 2.47V + \left[R_1 \times \left(\frac{2.47V}{R_2} + 20\mu A \right) \right]$$
$$V_{UVL} = \frac{2.47V \times (R_1 + R_2)}{R_2}$$
$$V_{UV(HYS)} = R_1 \times 20\mu A \quad (20)$$
$$V_{OVH} = \frac{2.45V \times (R_3 + R_4)}{R_4}$$
$$V_{OVL} = 2.45V + \left[R_3 \times \left(\frac{2.45V}{R_4} - 21\mu A \right) \right]$$

Option C

The minimum UVLO level is achieved by tying the UVLO/EN pin to VIN, illustrated in Figure 12. Q_1 turns on once V_{IN} rises to the POR_{EN} threshold (approximately 8.3V). Resistors R_3 and R_4 set the OVLO thresholds, and their values are computed following the procedure described in Option B.

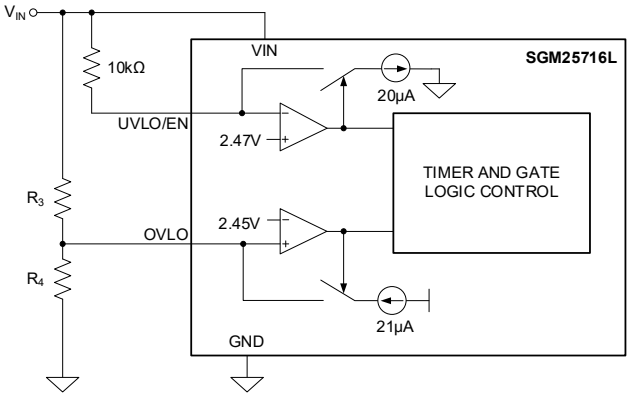


Figure 12. UVLO = POR_{EN}

Option D

The OVLO function may be disabled by connecting the OVLO pin to ground. UVLO thresholds are configured following the procedures defined in Option B or Option C.

This design example uses Option B with target thresholds V_{UVH} = 38V, V_{UVL} = 35V, V_{OVH} = 65V, and V_{OVL} = 63V. V_{UVH} and V_{OVL} are placed 5% below and above the 40V to 60V input range, respectively, to absorb device threshold tolerance. R_1 through R_4 are computed with the equations below:

$$R_1 = \frac{V_{UVH} - V_{UVL}}{20\mu A} = \frac{38V - 35V}{20\mu A} = 150k\Omega$$
$$R_2 = \frac{2.47V \times R_1}{V_{UVL} - 2.47V} = \frac{2.47V \times 150k\Omega}{35V - 2.47V} = 11.39k\Omega$$
$$R_3 = \frac{V_{OVH} - V_{OVL}}{21\mu A} = \frac{65V - 63V}{21\mu A} = 95.24k\Omega \quad (21)$$
$$R_4 = \frac{2.45V \times R_3}{V_{OVH} - 2.45V} = \frac{2.45V \times 95.24k\Omega}{65V - 2.45V} = 3.73k\Omega$$

Select the nearest available 1% resistor values. Set R_1 = 150kΩ, R_2 = 11.5kΩ, R_3 = 95.3kΩ, and R_4 = 3.74kΩ.

Power Good Pin

The Power Good indicator pin (PGD) connects to the drain of an internal N-channel MOSFET. This transistor withstands 80V under off-state condition and transient voltages up to 100V. An external pull-up resistor must be connected to PGD and biased to a suitable supply, so that downstream circuits can receive the status signal. In the off-state, the voltage on PGD can rest above or below both V_{IN} and V_{OUT}. PGD is driven high when the FB pin voltage rises above the PGD threshold. A resistor divider connected between the output and feedback pin is commonly used to set the output voltage threshold. However, the monitored signal is not limited to the output voltage. Other voltage signals may be monitored provided that the FB pin voltage never exceeds its maximum absolute rating. According to the Figure 3, the 20μA current source at FB is disabled when FB voltage stays below the threshold. Once the output voltage rises and pushes FB above the threshold, the current source turns on and sources current out of the pin, raising the FB pin voltage and creating threshold hysteresis. If UVLO/EN drops below its threshold or OVLO exceeds its threshold, PGD is pulled low. The PGD state is readable over PMBus through the READ_DIAGNOSTIC_WORD (0xE1) or the STATUS_WORD (0x79) registers.

APPLICATION INFORMATION (continued)

When the FB pin voltage rises above its threshold, the internal pull-down device on the PGD pin is disabled. PGD can then rise to V_{PGD} via a pull-up resistor R_{PG}, as illustrated in Figure 14. The pull-up supply V_{PGD} can reach up to 80V, and may be higher or lower than V_{IN} and the output voltage. Using VDD for V_{PGD} is a practical option, which supports low-voltage logic interfacing and prevents PGD glitches during power-up. If PGD signal delay is needed, refer to the example circuits in Figure 15, Figure 16 and Figure 17. In Figure 15, capacitor C_{PG} introduces delay only on the rising edge with no effect on the falling edge. For Figure 16, the rising edge delay is determined by R_{PG1} + R_{PG2} and C_{PG}, while the falling edge has a shorter delay formed by R_{PG2} and C_{PG}. Placing a diode across R_{PG2} (Figure 17) enables either equal delay for both edges, or a short rising-edge delay paired with a long falling-edge delay.

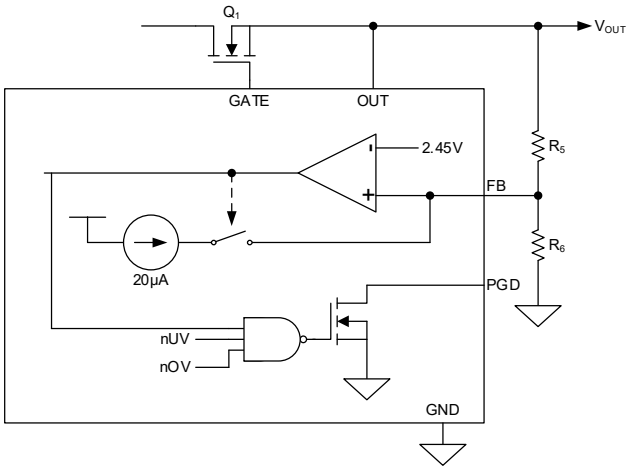


Figure 13. Programming the PGD Threshold

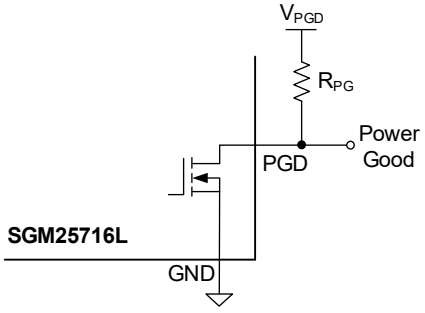


Figure 14. Power Good Output

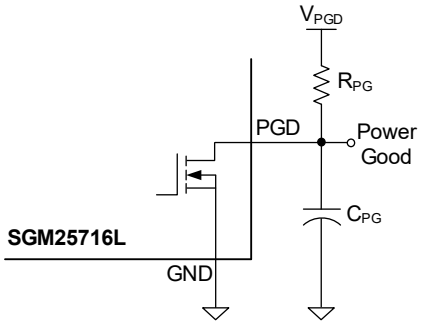


Figure 15. Adding Delay to the Power Good Output Pin - Delay at Rising Edge Only

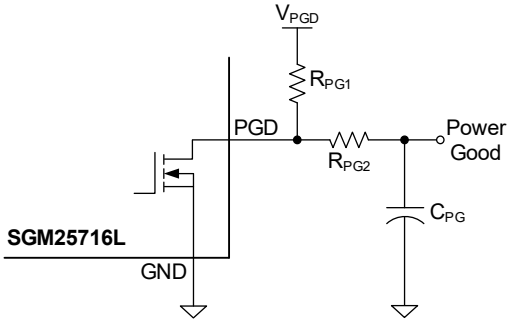


Figure 16. Adding Delay to the Power Good Output Pin - Long Delay at Rising Edge, Short Delay at Falling Edge

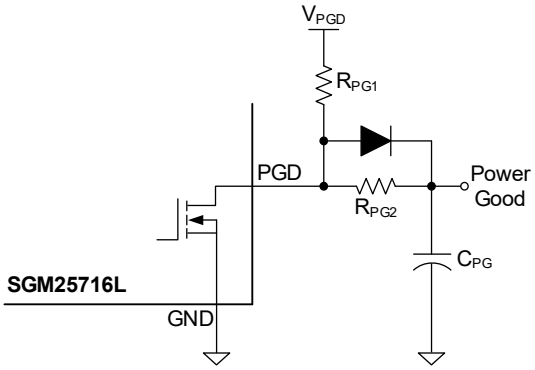


Figure 17. Adding Delay to the Power Good Output Pin - Short Delay at Rising Edge and Long Delay at Falling Edge or Equal Delays

SGMICRO suggests setting the PG threshold 5% under the minimum input voltage. This ensures that the PG signal is asserted across all input operating conditions. For this design example, target values are V_{PGDH} = 38V and V_{PGDL} = 35V. Resistors R_5 and R_6 are calculated via the equations below:

$$R_5 = \frac{V_{PGDH} - V_{PGDL}}{20\mu A} = \frac{38V - 35V}{20\mu A} = 150k\Omega$$
$$R_6 = \frac{2.45V \times R_5}{V_{PGDH} - 2.45V} = \frac{2.45V \times 150k\Omega}{38V - 2.45V} = 10.34k\Omega \quad (22)$$

Select the nearest available 1% resistor values. Set R_5 = 150kΩ and R_6 = 10.5kΩ.

APPLICATION INFORMATION (continued)

Input and Output Protection

For dependable operation of the SGM25716L hot-swap circuit, a voltage-clamping component must be placed on the supply side of the mating connector where the board is inserted. A TVS device is the recommended choice, as shown in the Figure 18. The TVS must absorb the voltage transients produced when the hot-swap circuit interrupts load current. This effect is most severe during hot-short events, when a large current is cut abruptly at FET turn-off. The chosen TVS should draw low leakage at $V_{IN,MAX}$ and hold the voltage below 100V during hot-short faults. The 5.0SMDJ60A fits most high-power applications.

When the load supplied by the SGM25716L hot-swap circuit exhibits inductive behavior, a Schottky diode must be placed across the output terminals of SGM25716L together with load capacitance. The capacitor and diode serve to restrain the negative voltage excursion on the OUT pin when load current is disabled.

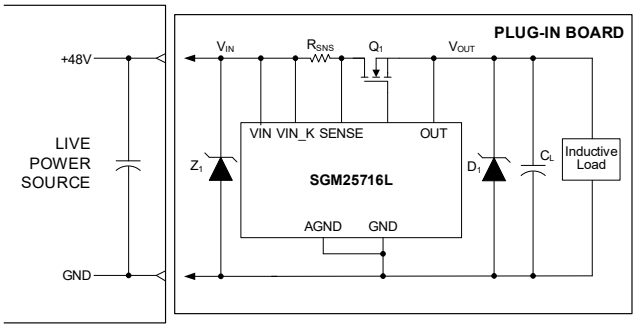


Figure 18. Output Diode Required for Inductive Loads

Final Schematic and Component Values

Figure 8 illustrates the schematic diagram fulfilling the specifications covered in the preceding section. Table 2 lists the finalized component values selected to satisfy the design targets of this 48V, 10A hot-swap solution. The application characteristic curves presented in the subsequent section are derived from these component parameters.

Table 2. Final Component Values (48V, 10A Design)

COMPONENT	VALUE
R_{SNS}	2mΩ
R_1	150kΩ
R_2	11.5kΩ
R_3	95.3kΩ
R_4	3.74kΩ
R_5	150kΩ
R_6	10.5kΩ
R_{PWR}	21kΩ
Q_1	PSMN4R8-100BSEJ
Q_2	MMBT3904
D_1	B380-13-F
Z_1	5.0SMDJ60A
C_{TIMER}	150nF
Optional dv/dt circuit	DNP

APPLICATION INFORMATION (continued)

PMBus Address Lines (ADR0, ADR1, ADR2)

The SGM25716L offers 27 possible I²C addresses, determined by setting each of its three address pins to either VDD (high), GND (low), or left open (floating). Table 3 provides the resulting 7-bit addresses, with the eighth bit used for the read/write control.

Table 3. Device Addressing

ADR2	ADR1	ADR0	DECODED ADDRESS
Z	Z	Z	0x40
Z	Z	0	0x41
Z	Z	1	0x42
Z	0	Z	0x43
Z	0	0	0x44
Z	0	1	0x45
Z	1	Z	0x46
Z	1	0	0x47
Z	1	1	0x10
0	Z	Z	0x11
0	Z	0	0x12
0	Z	1	0x13
0	0	Z	0x14
0	0	0	0x15
0	0	1	0x16
0	1	Z	0x17
0	1	0	0x50
0	1	1	0x51
1	Z	Z	0x52
1	Z	0	0x53
1	Z	1	0x54
1	0	Z	0x55
1	0	0	0x56
1	0	1	0x57
1	1	Z	0x58
1	1	0	0x59
1	1	1	0x5A

nSMBA Response

The nSMBA effectively has two masks:

- The Alert Mask Register at 0xD8.
- The ARA Automatic Mask.

The ARA Automatic Mask is a feature that activates automatically when a device successfully answers an Alert Response Address (ARA) read request. During an ARA transaction, the PMBus master retrieves the address of the lowest-numbered device on the bus whose nSMBA pin is currently active. If this device's address is returned, it confirms that it was the one that responded. In response, the device releases its nSMBA signal. Once all devices with asserted nSMBA have reported their addresses through ARA, the common nSMBA line returns to an inactive state.

In the SGM25716L, this release is achieved by internally masking all fault conditions present at the time of the ARA read via the ARA Automatic Mask bit. While these faults remain visible in the status registers, they will not reassert nSMBA unless the mask is cleared, typically by the host issuing a CLEAR_FAULTS command. As a best practice, this clear operation should be performed whenever servicing an nSMBA event, regardless of whether an actual ARA read took place. A schematic overview of this process is shown in Figure 19.

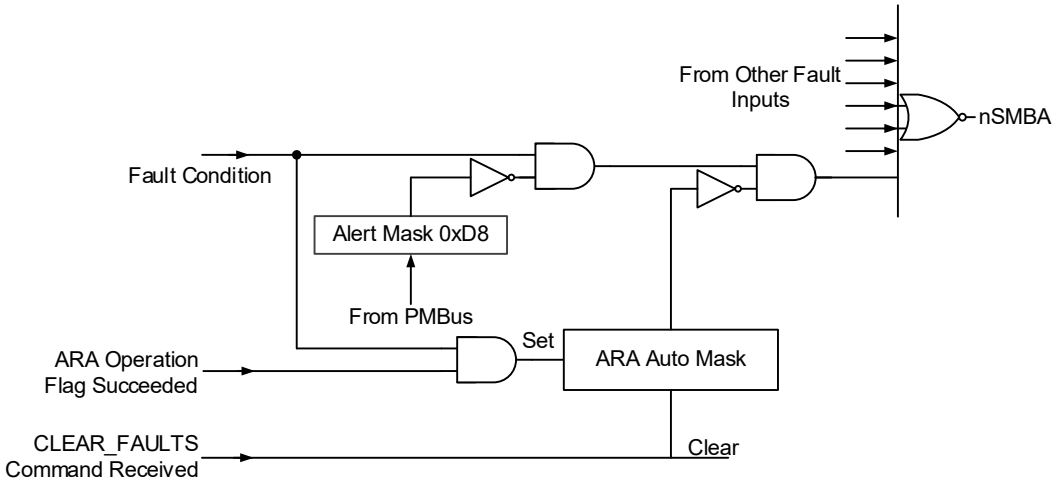


Figure 19. Typical Flow Schematic for nSMBA Fault

REGISTER MAPS

PMBus Command Support

The device provides an SMBus interface with PMBus command support. Warning thresholds and error masks can be configured, and telemetry data such as V_{IN}, V_{OUT}, I_{IN}, V_{AUX}, and P_{IN} can be retrieved. See Table 4 for the full list of supported PMBus commands.

Table 4. Supported PMBus Commands

CODE	NAME	FUNCTION	R/W	NUMBER OF DATA BYTES	DEFAULT VALUE
0x01	OPERATION	Used to read or write the operational status.	R/W	1	0x80
0x03	CLEAR_FAULTS	Clears status registers and re-enables black box registers to accept new updates.	Send byte	0	-
0x19	CAPABILITY	Retrieves the device capability.	R	1	0xB0
0x43	VOUT_UV_WARN_LIMIT	Enables retrieval and configuration of the output under-voltage warning limit.	R/W	2	0x0000
0x4F	OT_FAULT_LIMIT	Enables retrieval and configuration of the over-temperature fault limit.	R/W	2	0x0960 (+150℃)
0x51	OT_WARN_LIMIT	Enables retrieval and configuration of the over-temperature warning limit.	R/W	2	0x07D0 (+125℃)
0x57	VIN_OV_WARN_LIMIT	Enables retrieval and configuration of the input over-voltage warning limit.	R/W	2	0x0FFF
0x58	VIN_UV_WARN_LIMIT	Enables retrieval and configuration of the input under-voltage warning limit.	R/W	2	0x0000
0x5D	IIN_OC_WARN_LIMIT	Reads or writes the input current warn limit threshold (mirrored at 0xD3).	R/W	2	0x0FFF
0x78	STATUS_BYTE	Reads the operating status information of the device.	R	1	0x49
0x79	STATUS_WORD	Reads the operating status information of the device.	R	2	0x3849
0x7A	STATUS_VOUT	Reads output voltage status information.	R	1	0x00
0x7C	STATUS_INPUT	Reads input status information.	R	1	0x20
0x7D	STATUS_TEMPERATURE	Reads temperature status information.	R	1	0x00
0x7E	STATUS_CML	Reads communication status information.	R	1	0x00
0x7F	STATUS_OTHER	Retrieves other status information.	R	1	0x00
0x80	STATUS_MFR_SPECIFIC	Retrieves the state of circuit breaker and MOSFET short-circuit faults.	R	1	0x10
0x86	READ_EIN	Retrieves energy meter measurement.	R	7	0x00000000000006
0x88	READ_VIN	Retrieves input voltage measurement.	R	2	0x0000
0x89	READ_IIN	Retrieves input current measurement (mirrors at 0xD1).	R	2	0x0000
0x8B	READ_VOUT	Retrieves output voltage measurement.	R	2	0x0000
0x8D	READ_TEMPERATURE_1	Retrieves temperature measurement.	R	2	0x0000
0x97	READ_PIN	Reads the averaged input power measurement (mirrored at 0xDF).	R	2	0x0000
0x99	MFR_ID	Gets the manufacturer identification expressed in ASCII characters (MGS).	R	4	0x4D475303
0x9A	MFR_MODEL	Gets the part identification represented by ASCII characters. (SGM25716L).	R	9	0x00000036313735320 5
0x9B	MFR_REVISION	Reads the device revision character or number, encoded in ASCII (e.g., 00).	R	3	0x303002
0xD0	MFR_SPECIFIC_00 READ_VAUX	Retrieves auxiliary voltage measurement.	R	2	0x0000
0xD1	MFR_SPECIFIC_01 MFR_READ_IIN	Retrieves input current measurement.	R	2	0x0000
0xD2	MFR_SPECIFIC_02 MFR_READ_PIN	Retrieves input power measurement.	R	2	0x0000
0xD3	MFR_SPECIFIC_03 MFR_IIN_OC_WARN_LIMIT	Reads or writes the warning threshold of input current limit.	R/W	2	0x0FFF
0xD4	MFR_SPECIFIC_04 MFR_PIN_OP_WARN_LIMIT	Reads or writes the warning threshold for input power limit.	R/W	2	0x0FFF
0xD5	MFR_SPECIFIC_05 READ_PIN_PEAK	Reads the measured peak input power value.	R	2	0x0000

REGISTER MAPS (continued)

Table 4. Supported PMBus Commands (continued)

CODE	NAME	FUNCTION	R/W	NUMBER OF DATA BYTES	DEFAULT VALUE
0xD6	MFR_SPECIFIC_06 CLEAR_PIN_PEAK	Peak input power register reset to zero.	Send byte	0	-
0xD7	MFR_SPECIFIC_07 GATE_MASK	Enables users to suppress MOSFET gate shutdown under different fault conditions.	R/W	1	0x00
0xD8	MFR_SPECIFIC_08 ALERT_MASK	Retrieves or stores user nSMBA fault mask.	R/W	2	0x0820
0xD9	MFR_SPECIFIC_09 DEVICE_SETUP	Reads or writes configuration data for the retry attempt count.	R/W	1	0x00
0xDA	MFR_SPECIFIC_10 BLOCK_READ	Reads the latest diagnostic and telemetry information within a single transaction.	R	12	0x08E00000000000000000000
0xDB	MFR_SPECIFIC_11 SAMPLES_FOR_AVG	AVGN is the exponent used to define the quantity of samples for averaging (N = 2^{AVGN}), range = 0x00 to 0x0C.	R/W	2	0x0000
0xDC	MFR_SPECIFIC_12 READ_AVG_VIN	Retrieves averaged input voltage measurement.	R	2	0x0000
0xDD	MFR_SPECIFIC_13 READ_AVG_VOUT	Retrieves averaged output voltage measurement.	R	2	0x0000
0xDE	MFR_SPECIFIC_14 READ_AVG_IIN	Reads the averaged input current measurement value.	R	2	0x0000
0xDF	MFR_SPECIFIC_15 READ_AVG_PIN	Reads the averaged input power measurement value.	R	2	0x0000
0xE0	MFR_SPECIFIC_16 BLACK_BOX_READ	It captures diagnostic and telemetry data, which get latched upon the first nSMBA event after fault clearance.	R	12	0x08E00000000000000000000
0xE1	MFR_SPECIFIC_17 READ_DIAGNOSTIC_WORD	A manufacturer-defined counterpart to STATUS_WORD, used to transmit all fault and warning data in one transaction.	R	2	0x08E0
0xE2	MFR_SPECIFIC_18 AVG_BLOCK_READ	Captures the latest averaged telemetry and diagnostic data within one single transaction.	R	12	0x08E00000000000000000000

Reading and Writing Telemetry Data and Warning Thresholds

All telemetry and user-programmed warning threshold data use 12-bit two's complement binary numbers, sent two bytes at a time and formatted in the DIRECT format defined in the PMBus Power System Management Protocol Specification 1.1 (Part II), Section 8.3.3. Table 5 shows the bit layout of each telemetry or warning word, with D[11] as the most significant bit (MSB) and D[0] as the least significant bit (LSB). Except for temperature, every warning and telemetry word falls in the decimal range 0 to 4095, and the temperature word may take any decimal value from 0 to 65535.

Table 5. Telemetry and Warning Word Format

Byte	B7	B6	B5	B4	B3	B2	B1	B0
1	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
2	0	0	0	0	D[11]	D[10]	D[9]	D[8]

The coefficients in Section 7.2.1 of the PMBus Power System Management Protocol Specification 1.1 (Part II) convert DIRECT-format data into real-world current, voltage, power, and temperature values. The host expresses the received values in volts, amperes, watts, or other units according to the following relationship:

$$X = \frac{1}{m}\left(Y \times 10^{-R} - b\right) \quad (23)$$

where:

X is the resulting real-world quantity in volts, amperes, watts, or similar units.

m is the slope coefficient.

Y is the 2-byte two's complement integer read from the device.

b is the offset, a 2-byte two's complement integer.

R is the exponent, a 1-byte two's complement integer.

REGISTER MAPS (continued)

R is required only in systems that demand an integer value for m (for instance, when m is held in an integrated-circuit register). In these situations, R only has to be large enough to deliver the accuracy required.

Table 6. Telemetry and Warning Conversion Coefficients

Commands	Condition	Format	Number of Data Bytes	m	b	R	Unit
READ_VIN, READ_AVG_VIN, VIN_OV_WARN_LIMIT, VIN_UV_WARN_LIMIT		DIRECT	2	4617	-140.0	-2	V
READ_VOUT, READ_AVG_VOUT, VOUT_UV_WARN_LIMIT		DIRECT	2	4602	500.0	-2	V
READ_VAUX		DIRECT	2	13774	73.0	-1	V
READ_IIN, READ_AVG_IIN (1), MFR_IIN_OC_WARN_LIMIT	CL = VDD	DIRECT	2	15076	-503.9	-2	A
READ_IIN, READ_AVG_IIN (1), MFR_IIN_OC_WARN_LIMIT	CL = GND	DIRECT	2	7645	100	-2	A
READ_PIN, READ_AVG_PIN (1), READ_PIN_PEAK, MFR_PIN_OP_WARN_LIMIT	CL = VDD	DIRECT	2	1701	-4000	-3	W
READ_PIN, READ_AVG_PIN (1), READ_PIN_PEAK, MFR_PIN_OP_WARN_LIMIT	CL = GND	DIRECT	2	860.6	-965	-3	W
READ_TEMPERATURE_1, OT_WARN_LIMIT, OT_FAULT_LIMIT		DIRECT	2	16000	0	-3	℃

Table 7. Current and Power Telemetry and Warning Conversion Coefficients (R_{SNS} in mΩ)

Commands	Condition	Format	Number of Data Bytes	m	b	R	Unit
READ_IIN, READ_AVG_IIN (1), MFR_IIN_OC_WARN_LIMIT	CL = VDD	DIRECT	2	15076 × R_{SNS}	-503.9	-2	A
READ_IIN, READ_AVG_IIN (1), MFR_IIN_OC_WARN_LIMIT	CL = GND	DIRECT	2	7645 × R_{SNS}	100.0	-2	A
READ_PIN, READ_AVG_PIN (1), READ_PIN_PEAK, MFR_PIN_OP_WARN_LIMIT	CL = VDD	DIRECT	2	1701 × R_{SNS}	-4000	-3	W
READ_PIN, READ_AVG_PIN (1), READ_PIN_PEAK, MFR_PIN_OP_WARN_LIMIT	CL = GND	DIRECT	2	860.6 × R_{SNS}	-965.0	-3	W

NOTE:

1. The current/power measurement and warning-threshold coefficients listed here are normalized to a sense resistor (R_{SNS}) of 1mΩ. Table 6 gives the general relationships from which the current or power coefficients may be derived.

R should be selected to keep m within -32768 to 32767. As an illustration, use a 5mΩ sense resistor, READ_IIN with CL = VDD takes m = 5359, b = -120, R = -1.

REGISTER MAPS (continued)

Standard PMBus Commands

REG0x01: OPERATION [Reset = 0x80]

The OPERATION command is a standard PMBus instruction designed to control MOSFET switching functions. It allows the host system to remotely turn the MOSFET on or off. Additionally, this command serves to reactivate the MOSFET after it shuts down due to a fault condition. Transmitting an off command succeeded by an on command will wipe out every fault status and bring the IC back to regular operating conditions. Conversely, delivering nothing but an on command posts a fault-triggered shutdown failed to reset fault registers or re-activate the device. Such commands are delivered via the write-byte communication protocol.

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	ON/OFF_STATE	1	R/W	0: The MOSFET is off. 1: The MOSFET is on.
D[6:0]	RESERVED	000 0000	R/W	Reserved.

REG0x03: CLEAR_FAULTS

As a standardized PMBus operation, CLEAR_FAULTS resets every retained warning and fault flag and also clears the nSMBA signal. Should an active fault or warning condition persist upon transmission of this command, the nSMBA signal may either fail to clear or reassert immediately. Importantly, issuing CLEAR_FAULTS alone does not turn the MOSFET back on after a fault-induced shutdown; restoring the output requires sending an OPERATION command once the underlying fault has been resolved. The PMBus byte-send protocol is utilized for sending this particular command.

REG0x19: CAPABILITY [Reset = 0xB0]

CAPABILITY is a PMBus-standard command that reports which PMBus functions the SGM25716L device supports. The PMBus byte-read protocol governs access to this command.

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	PACKET_ERROR_CHECKING	1	R	Packet Error Checking is supported.
D[6:5]	MAXIMUM_BUS_SPEED	01	R	Maximum supported bus speed is 400kHz.
D[4]	SMBALERT#	1	R	The device does have an nSMBA pin and does support the SMBus Alert Response protocol.
D[3]	DATA_TYPE	0	R	Numeric data is in LINEAR11, ULINEAR16 or DIRECT format.
D[2]	AVSBUS_SUPPORT	0	R	AVSBus not supported.
D[1]	CML	0	R	A communication fault occurred.
D[0]	RESERVED	0	R	Reserved.

REG0x43: VOUT_UV_WARN_LIMIT [Reset = 0x0000]

VOUT_UV_WARN_LIMIT is a PMBus-standard command that sets the value of the output voltage at the sense or output pins that causes an output voltage low warning. This warning is masked until the unit reaches the programmed output voltage. This warning is also masked when the unit is disabled. This command shall be accessed via either the PMBus Read Word or Write Word protocol. The coefficients specified in Table 6 shall be adopted for read and write operations on this register. If the measured output voltage (V_{OUT}) drops below the threshold stored within this register, the V_{OUT} under-voltage warning flags will be triggered, and the nSMBA interrupt signal will be asserted.

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[15:0]	VOUT_UV_WARN_LIMIT	0000 0000 0000 0000	R/W	0001h ~ 0FFFh: V_{OUT} under-voltage warning detection threshold. 0000h: V_{OUT} under-voltage warning disabled.

REGISTER MAPS (continued)

REG0x4F: OT_FAULT_LIMIT [Reset = 0x0960]

OT_FAULT_LIMIT is a PMBus-standard command that configures or reads the threshold for over-temperature fault detection. Conversion coefficients shown in Table 6 need to be applied for all read and write actions targeting this register. PMBus Read Word or Write Word protocol is required for any access to this command. Should the measured temperature surpass this pre-set threshold, an over-temperature fault is triggered. This fault turns off the power MOSFET, sets OT FAULT flags, and asserts the nSMBA signal. Following a drop in measured temperature below the register setting, the OPERATION command can be run to re-enable the MOSFET. Each temperature sample undergoes averaging over 16 round-robin cycles, meaning the shortest possible over-temperature fault detection time equals 16ms.

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[15:0]	OT_FAULT_LIMIT	0000 1001 0110 0000	R/W	0000h ~ 0FFEh: Threshold value for over-temperature fault. 0FFFh: Over-temperature fault detection has been disabled.

REG0x51: OT_WARN_LIMIT [Reset = 0x07D0]

OT_WARN_LIMIT serves as a PMBus-standard command for setting and reading back the over-temperature warning detection threshold. Conversion coefficients specified in Table 6 shall be adopted for every read or write operation on this register. Access to this command shall use the PMBus Read Word or Write Word protocol. Should the measured temperature surpass this preset threshold, the device generates an over-temperature warning, sets OT WARN status flags, and asserts the nSMBA alert signal. Each temperature reading is averaged over 16 consecutive round-robin sampling cycles; therefore, the minimum response time for over-temperature warning detection is 16ms.

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[15:0]	OT_WARN_LIMIT	0000 0111 1101 0000	R/W	0000h ~ 0FFEh: Threshold value for over-temperature warning. 0FFFh: Over-temperature warning detection has been disabled.

REG0x57: VIN_OV_WARN_LIMIT [Reset = 0x0FFF]

The VIN_OV_WARN_LIMIT command represents a standard PMBus instruction used for setting or retrieving the threshold value associated with V_{IN} over-voltage warning detection. When reading from or writing to this register, the coefficient values specified in Table 6 must be applied. Access to this command is allowed exclusively through the PMBus read-word or write-word protocol. In cases where the sensed V_{IN} measurement exceeds the value stored in this register, the corresponding V_{IN} over-voltage warning flags will be triggered in the relevant registers, and the nSMBA signal will be activated.

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[15:0]	VIN_OV_WARN_LIMIT	0000 1111 1111 1111	R/W	0000h ~ 0FFEh: V_{IN} over-voltage warning detection threshold. 0FFFh: V_{IN} over-voltage warning disabled.

REG0x58: VIN_UV_WARN_LIMIT [Reset = 0x0000]

VIN_UV_WARN_LIMIT serves as a PMBus-standard command designed for configuring and reading the threshold level for V_{IN} under-voltage warning monitoring. The coefficients provided in Table 6 shall be applied for both read and write operations to this register. All operations on this command shall be carried out according to the PMBus read-word or write-word protocol. If the sensed V_{IN} level falls beneath the threshold programmed into this register, the matching V_{IN} under-voltage warning flags within the relevant register will be set, and the nSMBA signal is asserted.

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[15:0]	VIN_UV_WARN_LIMIT	0000 0000 0000 0000	R/W	0001h ~ 0FFFh: V_{IN} under-voltage warning detection threshold. 0000h: V_{IN} under-voltage warning disabled.

REGISTER MAPS (continued)

REG0x5D: IIN_OC_WARN_LIMIT [Reset = 0x0FFF]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[15:0]	IIN_OC_WARN_LIMIT	0000 1111 1111 1111	R/W	0000h ~ 0FFEh: Value for input over-current warn limit. 0FFFh: Input over-current warning disabled.

REG0x78: STATUS_BYTE [Reset = 0x49]

The STATUS_BYTE command is a standard PMBus instruction that outputs a set of flag bits reflecting the operating status of the SGM25716L. Access to this command shall use the PMBus byte-read protocol. For resetting the bits contained in this register, the relevant system fault condition must be resolved first, followed by the issuance of a CLEAR_FAULTS command.

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	BUSY	0	R	Not supported, always 0.
D[6]	OFF	1	R	This bit asserts when the MOSFET cannot be turned on for any reason.
D[5]	VOUT_OV	0	R	Not supported, always 0.
D[4]	IOUT_OC	0	R	Not supported, always 0.
D[3]	VIN_UV_FAULT	1	R	A V_{IN} under-voltage fault has occurred.
D[2]	TEMPERATURE	0	R	A temperature-related fault or warning event is triggered.
D[1]	CML	0	R	A communication fault event is detected.
D[0]	NONE_OF_THE_ABOVE	1	R	A fault or warning event other than those defined in bits [7:1] is detected.

REG0x79: STATUS_WORD [Reset = 0x3849]

The STATUS_WORD is a PMBus-standard command that outputs a series of status flags reflecting the operating condition of the SGM25716L device. Access to this command shall adhere to the PMBus word-read protocol. Clearing the bits within this register is required to remove the originating fault condition followed by execution of the CLEAR_FAULTS command. Notably, the INPUT and V_{IN} UV flags are set to logic 1 by default at power-on and UVLO is below the threshold; these bits are automatically reset to 0 once the input voltage first rises above the resistor configured UVLO threshold.

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[15]	VOUT	0	R	An output voltage fault or warning event has been detected.
D[14]	IOUT/POUT	0	R	Not supported, always 0.
D[13]	INPUT	1	R	An input voltage or current fault event is detected.
D[12]	MFR	1	R	A manufacturer-specific fault or warning occurred.
D[11]	nPOWER_GOOD	1	R	Power Good signal deasserted.
D[10]	FANS	0	R	Not supported, always 0.
D[9]	CB_FAULT	0	R	Circuit breaker fault triggered.
D[8]	UNKNOWN	0	R	Not supported, always 0.
D[7]	BUSY	0	R	Not supported, always 0.
D[6]	OFF	1	R	This bit is set whenever the MOSFET fails to turn on for any cause.
D[5]	VOUT_OV	0	R	Not supported, always 0.
D[4]	IOUT_OC	0	R	Not supported, always 0.
D[3]	VIN_UV	1	R	A V_{IN} under-voltage fault has occurred.
D[2]	TEMPERATURE	0	R	A temperature-related fault or warning event is detected.
D[1]	CML	0	R	A communication fault event is detected.
D[0]	NONE_OF_THE_ABOVE	1	R	A fault or warning event outside the definitions of bits [7:1] is detected.

REGISTER MAPS (continued)

REG0x7A: STATUS_VOUT [Reset = 0x00]

The STATUS_VOUT command represents a standard PMBus instruction designed to report the status of the V_{OUT} under-voltage warning flag. All access operations for this command shall comply with the PMBus byte-read protocol. In order to reset the bits within this register, the relevant fault condition must be resolved first, followed by the transmission of a CLEAR_FAULTS command.

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	VOUT_OV_FAULT	0	R	Not supported, always 0.
D[6]	VOUT_OV_WARN	0	R	Not supported, always 0.
D[5]	VOUT_UV_WARN	0	R	A V_{OUT} under-voltage warning has occurred.
D[4]	VOUT_UV_FAULT	0	R	Not supported, always 0.
D[3]	VOUT_MAX	0	R	Not supported, always 0.
D[2]	TON_MAX_FAULT	0	R	Not supported, always 0.
D[1]	TOFF_MAX_FAULT	0	R	Not supported, always 0.
D[0]	VOUT_TRACKING_ERROR	0	R	Not supported, always 0.

REG0x7C: STATUS_INPUT [Reset = 0x20]

STATUS_INPUT serves as a PMBus-standard command that provides status values for multiple flags associated with input voltage, current, and power. Reads of this command follow the PMBus byte-read protocol. To reset the bits in this register, first eliminate the related fault condition, and then send a CLEAR_FAULTS command. The V_{IN} under-voltage warning flag is initialized to 1 at input power-on; it will be cleared to 0 when the input voltage rises above the resistor-set UVLO threshold for the first time.

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	VIN_OV_FAULT	0	R	A V_{IN} over-voltage fault has occurred.
D[6]	VIN_OV_WARN	0	R	A V_{IN} over-voltage warning has occurred.
D[5]	VIN_UV_WARN	1	R	A V_{IN} under-voltage warning has occurred.
D[4]	VIN_UV_FAULT	0	R	A V_{IN} under-voltage fault has occurred.
D[3]	INSUFFICIENT_VOLTAGE	0	R	Not supported, always 0.
D[2]	IIN_OC_FAULT	0	R	An I_{IN} over-current fault has occurred.
D[1]	IIN_OC_WARN	0	R	An I_{IN} over-current warning has occurred.
D[0]	PIN_OP_WARN	0	R	An input power overpower warning event is detected.

REG0x7D: STATUS_TEMPERATURE [Reset = 0x00]

STATUS_TEMPERATURE is a PMBus-standard command providing multiple status flags associated with temperature telemetry readings. The PMBus byte-read protocol shall be adopted to access this command. The register's bits are cleared by eliminating the relevant fault condition and subsequently issuing CLEAR_FAULTS.

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	OVERTEMP_FAULT	0	R	An over-temperature fault has occurred.
D[6]	OVERTEMP_WARN	0	R	An over-temperature warning has occurred.
D[5]	UNDERTEMP_WARN	0	R	Not supported, always 0.
D[4]	UNDERTEMP_FAULT	0	R	Not supported, always 0.
D[3]	RESERVED	0	R	Not supported, always 0.
D[2]	RESERVED	0	R	Not supported, always 0.
D[1]	RESERVED	0	R	Not supported, always 0.
D[0]	RESERVED	0	R	Not supported, always 0.

REGISTER MAPS (continued)

REG0x7E: STATUS_CML [Reset = 0x00]

STATUS_CML is a PMBus-standard command that provides various status flags indicative of communication-related faults. The PMBus byte-read protocol shall be used to read this command. Issuing a CLEAR_FAULTS command is required to clear the bits within this register.

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	STATUS_CML[7]	0	R	The device has received an invalid or unsupported command.
D[6]	STATUS_CML[6]	0	R	Received data is invalid or unsupported.
D[5]	STATUS_CML[5]	0	R	Packet error check failed.
D[4]	STATUS_CML[4]	0	R	Not supported, always 0.
D[3]	STATUS_CML[3]	0	R	Not supported, always 0.
D[2]	STATUS_CML[2]	0	R	Not supported, always 0.
D[1]	STATUS_CML[1]	0	R	Miscellaneous communication error is detected.
D[0]	STATUS_CML[0]	0	R	Not supported, always 0.

REG0x7F: STATUS_OTHER [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	RESERVED	0	R	Always 0.
D[6]	RESERVED	0	R	Always 0.
D[5]	CIRCUITBREAKER_FAULT	0	R	CB Fault.
D[4]	STATUS_OTHER[4]	0	R	Not supported, always 0.
D[3]	STATUS_OTHER[3]	0	R	Not supported, always 0.
D[2]	STATUS_OTHER[2]	0	R	Not supported, always 0.
D[1]	STATUS_OTHER[1]	0	R	Not supported, always 0.
D[0]	STATUS_OTHER[0]	0	R	Not supported, always 0.

REG0x80: STATUS_MFR_SPECIFIC [Reset = 0x10]

The STATUS_MFR_SPECIFIC command serves as a standardized PMBus instruction used to store status data unique to individual manufacturers. This command is read-only via the PMBus byte-read protocol. To reset its bits, the relevant fault condition must be resolved first, followed by issuing a CLEAR_FAULTS command.

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	STATUS_MFR_SPECIFIC[7]	0	R	Circuit breaker fault.
D[6]	EXT_MOSFET_SHORTED	0	R	External MOSFET shorted fault.
D[5]	STATUS_MFR_SPECIFIC[5]	0	R	Not supported, always 0.
D[4]	STATUS_MFR_SPECIFIC[4]	1	R	Defaults loaded.
D[3]	STATUS_MFR_SPECIFIC[3]	0	R	Not supported, always 0.
D[2]	STATUS_MFR_SPECIFIC[2]	0	R	Not supported, always 0.
D[1]	STATUS_MFR_SPECIFIC[1]	0	R	Not supported, always 0.
D[0]	STATUS_MFR_SPECIFIC[0]	0	R	Not supported, always 0.

REGISTER MAPS (continued)

REG0x86: READ_EIN [Reset = 0x00000000000006]

The READ_EIN command is a PMBus-standard command that returns information the host can use to calculate average input power consumption. Accesses to this command should use the PMBus multi-byte block-read protocol. The information provided by this command is independent of any device-specific averaging period. Six data bytes are returned by this command (excluding the first byte, which indicates the number of bytes). The first two bytes are the two's complement signed output of an accumulator that continuously sums samples of the instantaneous input power. The accumulator value is the summation of the instantaneous power measurement. These two data bytes are formatted in the DIRECT format. The next data byte is a rollover count for the accumulator. This byte is an unsigned integer that indicates the number of times the accumulator has rolled over from its maximum positive unsigned integer (0x7FFF) to 0. The last three data bytes are a 24-bit unsigned integer that counts the number of samples of the instantaneous input power. This value also rolls periodically from its maximum positive value to 0. It is up to the host to keep track of the sample count and account for the rollovers.

The combination of the accumulator and the roller count may overflow after a period of several seconds. Similarly, the sample count value overflows, but this event only occurs once every few hours.

To convert the data obtained from two separate READ_EIN commands into average power, first convert the accumulator and rollover count to an unsigned integer (see Equation 24).

$$Accumulator_23 = (rollover_count << 15) + accumulator \quad (24)$$

Note that the overflow of this variable needs to be monitored and properly accounted for. Data from the previous calculation, along with the sample count values from the corresponding register access, can be used to get the unscaled average power:

$$\frac{Accumulator_23[n] - Accumulator_23[n-1]}{Sample_count[n] - Sample_count[n-1]} \quad (25)$$

where:

Accumulator_23[n] = Overflow corrected, 23-bit accumulator data from this read.
Sample_count[n] = Sample count data from this read.
Accumulator_23[n - 1] = Overflow corrected, 23-bit accumulator data from previous read.
Sample_count[n - 1] = Sample count data from previous read.
Unscaled average power is now in the same units as the data from the READ_PIN command. Coefficients from Table 6 are used to convert the unscaled average power to Watts.

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[55:48]	READ_EIN[55:48]	0000 0000	R	Sample count high byte.
D[47:40]	READ_EIN[47:40]	0000 0000	R	Sample count mid byte.
D[39:32]	READ_EIN[39:32]	0000 0000	R	Sample count low byte.
D[31:24]	READ_EIN[31:24]	0000 0000	R	Power accumulator rollover count.
D[23:16]	READ_EIN[23:16]	0000 0000	R	Power accumulator high byte.
D[15:8]	READ_EIN[15:8]	0000 0000	R	Power accumulator low byte.
D[7:0]	READ_EIN[7:0]	0000 0110	R	Number of bytes.

REGISTER MAPS (continued)

REG0x88: READ_VIN [Reset = 0x0000]

READ_VIN is a PMBus-standard command that provides a 12-bit digital result representing the measured input voltage. Retrieval of this register requires the use of the coefficients specified in Table 6 and must follow the PMBus word-read protocol. Internally, this measured value is also employed to detect over-voltage and under-voltage warning conditions for the input voltage.

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[15:0]	READ_VIN	0000 0000 0000 0000	R	0000h ~ 0FFFh: Measured V_{IN} value.

REG0x89: READ_IIN [Reset = 0x0000]

The READ_IIN command is a PMBus-standard command that returns the 12-bit measured value of the input current. The Table 6 coefficients apply when reading this register. Accesses to this command should use the PMBus word-read protocol. This value is also mirrored at 0xD1.

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[15:0]	READ_IIN	0000 0000 0000 0000	R	0000h ~ 0FFFh: Measured I_{IN} value.

REG0x8B: READ_VOUT [Reset = 0x0000]

The READ_VOUT command represents a standard PMBus instruction that outputs a 12-bit sampled measurement of the output voltage. When reading this register, the coefficient values provided in Table 6 shall be applied. All access operations for this command shall comply with the PMBus word-read protocol. Internally, this measured value is additionally utilized for detecting V_{OUT} under-voltage warning events.

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[15:0]	READ_VOUT	0000 0000 0000 0000	R	0000h ~ 0FFFh: Measured V_{OUT} value.

REG0x8D: READ_TEMPERATURE_1 [Reset = 0x0000]

READ_TEMPERATURE_1 command is a PMBus-standard command that provides a signed reading of the temperature detected by an external temperature sensing diode. When reading this register, the coefficients listed in Table 6 must be used, and all transactions must follow the PMBus word-read protocol. Internally, this temperature value is also used to identify over-temperature faults and warning conditions. After coefficient conversion, the valid range of this data spans from -256℃ to +255℃.

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[15:0]	READ_TEMPERATURE_1	0000 0000 0000 0000	R	0000h ~ 0FFFh: Measured TEMPERATURE value.

REG0x97: READ_PIN [Reset = 0x0000]

The READ_PIN command is a PMBus-standard command that returns the 12-bit measured value of the input power. The Table 6 coefficients apply when reading this register. Accesses to this command should use the PMBus word-read protocol. This value is also mirrored at 0xDF.

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[15:0]	READ_PIN	0000 0000 0000 0000	R	0000h ~ 0FFFh: Measured P_{IN} value.

REGISTER MAPS (continued)

REG0x99: MFR_ID [Reset = 0x4D475303]

The MFR_ID command functions as a PMBus-standard command that reports the manufacturer's identification code. The PMBus multi-byte block-read protocol shall be used to obtain MFR_ID information.

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[31:24]	'M'	0100 1101	R	MFR ID-3.
D[23:16]	'G'	0100 0111	R	MFR ID-2.
D[15:8]	'S'	0101 0011	R	MFR ID-1.
D[7:0]	MFR_ID[7:0]	0000 0011	R	Number of bytes.

REG0x9A: MFR_MODEL [Reset = 0x000000363137353205]

MFR_MODEL is a PMBus-standard command used to retrieve the device part number. PMBus multi-byte block-read protocol shall be applied when reading this command.

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[71:64]	MFR_MODEL[71:64]	0000 0000	R	MFR ID-8.
D[63:56]	MFR_MODEL[63:56]	0000 0000	R	MFR ID-7.
D[55:48]	MFR_MODEL[55:48]	0000 0000	R	MFR ID-6.
D[47:40]	'6'	0011 0110	R	MFR ID-5.
D[39:32]	'1'	0011 0001	R	MFR ID-4.
D[31:24]	'7'	0011 0111	R	MFR ID-3.
D[23:16]	'5'	0011 0101	R	MFR ID-2.
D[15:8]	'2'	0011 0010	R	MFR ID-1.
D[7:0]	MFR_MODEL[7:0]	0000 0101	R	Number of bytes.

REG0x9B: MFR_REVISION [Reset = 0x303002]

As a PMBus-standard command, MFR_REVISION returns the component's hardware or firmware revision level. PMBus multi-byte block-read protocol shall be adopted to access this command.

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[23:16]	'0'	0011 0000	R	MFR ID-2.
D[15:8]	'0'	0011 0000	R	MFR ID-1.
D[7:0]	MFR_VERSION[7:0]	0000 0010	R	Number of bytes.

REGISTER MAPS (continued)

Manufacturer Specific PMBus Commands

REG0xD0: MFR_SPECIFIC_00 READ_VAUX [Reset = 0x0000]

The READ_VAUX command outputs a 12-bit ADC measurement of the auxiliary voltage. Any voltage at or above 2.97V relative to ground is reported as full-scale value 0FFFh. Voltages at or below 0V with respect to ground are indicated as 0000h. The PMBus word-read protocol shall be used when retrieving data via the READ_VAUX command.

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[15:0]	READ_VAUX	0000 0000 0000 0000	R	0000h ~ 0FFFh: Measured VAUX input value.

REG0xD1: MFR_SPECIFIC_01 MFR_READ_IIN [Reset = 0x0000]

The MFR_READ_IIN command provides a 12-bit ADC measurement of the current sense voltage. Data from this command must be read using the PMBus word-read protocol, and the conversion coefficients specified in Table 6 should be applied when interpreting this register. See the Reading and Writing Telemetry Data and Warning Thresholds section for how to perform the calculation correctly.

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[15:0]	MFR_READ_IIN	0000 0000 0000 0000	R	0000h ~ 0FFFh: Measured input current sense voltage value.

REG0xD2: MFR_SPECIFIC_02 MFR_READ_PIN [Reset = 0x0000]

The upper 12 bits of V_{IN} × I_{IN}, as captured by a 12-bit ADC, are output by the MFR_READ_PIN command. Access follows the PMBus word-read protocol, and reads of this register shall use the coefficients in Table 6. Instructions for deriving the corresponding values are given in the Reading and Writing Telemetry Data and Warning Thresholds section.

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[15:0]	MFR_READ_PIN	0000 0000 0000 0000	R	0000h ~ 0FFFh: VALUE for input current × input voltage.

REG0xD3: MFR_SPECIFIC_03 MFR_IIN_OC_WARN_LIMIT [Reset = 0x0FFF]

The MFR_IIN_OC_WARN_LIMIT is a PMBus command used to configure the input over-current warning threshold. If the input current exceeds the threshold programmed in this register, the corresponding I_{IN} over-current warning flags will be set in the relevant registers, and the nSMBA signal will be asserted. This register can be accessed using the PMBus word read/write protocol, and the coefficients provided in Table 6 should be applied for both read and write operations.

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[15:0]	MFR_IIN_OC_WARN_LIMIT	0000 1111 1111 1111	R/W	0000h ~ 0FFEh: Value for input over-current warn limit. 0FFFh: Input over-current warning disabled.

REG0xD4: MFR_SPECIFIC_04 MFR_PIN_OP_WARN_LIMIT [Reset = 0x0FFF]

MFR_PIN_OP_WARN_LIMIT is the PMBus command used to program the input over-power warning threshold. When input power goes beyond the limit programmed in this register, the corresponding PIN over-power flags in the associated registers become set, and the nSMBA signal is driven. This register is accessed via the PMBus word read/write protocol, and the coefficients listed in Table 6 shall be applied for both read and write operations.

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[15:0]	MFR_PIN_OP_WARN_LIMIT	0000 1111 1111 1111	R/W	0000h ~ 0FFEh: Input over-power warn limit setting. 0FFFh: Input over-power warning detection is disabled.

REGISTER MAPS (continued)

REG0xD5: MFR_SPECIFIC_05 READ_PIN_PEAK [Reset = 0x0000]

The highest input power value captured after a power-on reset or the latest CLEAR_PIN_PEAK execution is returned by the READ_PIN_PEAK command. The PMBus word-read protocol should be utilized to access data from this command, and the coefficients defined in Table 6 shall be adopted for calculation.

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[15:0]	READ_PIN_PEAK	0000 0000 0000 0000	R	0000h ~ 0FFFh: The maximum input current × input voltage since reset or the most recent clear.

REG0xD6: MFR_SPECIFIC_06 CLEAR_PIN_PEAK

The CLEAR_PIN_PEAK instruction is designed to reset the PIN PEAK register. This command shall be operated via the PMBus byte-send protocol.

REG0xD7: MFR_SPECIFIC_07 GATE_MASK [Reset = 0x00]

The GATE_MASK register provides hardware masking, preventing fault events from triggering MOSFET turn-off. If a specific bit is set, the corresponding fault condition ceases to control the MOSFET gate. All status registers, including STATUS and DIAGNOSTIC, continue to update normally, and the nSMBA signal is still asserted as required. Read and write operations on this register follow the PMBus byte read/write protocol.

NOTE: Preventing the MOSFET from shutting down during over-current or circuit-breaker fault events may lead to permanent damage of the MOSFET. This function must be employed with extreme care and proper oversight.

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	RESERVED	0	R/W	Not used, always 0.
D[6]	RESERVED	0	R/W	Not used, always 0.
D[5]	VIN_UV_FAULT	0	R/W	If turning off the MOSFET when V_{IN} under-voltage fault happened. 0: Turning off (default) 1: No
D[4]	VIN_OV_FAULT	0	R/W	If turning off the MOSFET when V_{IN} over-voltage fault happened. 0: Turning off (default) 1: No
D[3]	IIN/PFET_FAULT	0	R/W	If turning off the MOSFET when over-current or over power fault happened. 0: Turning off (default) 1: No
D[2]	OVERTEMP_FAULT	0	R/W	If turning off the MOSFET when over-temperature fault happened. 0: Turning off (default) 1: No
D[1]	RESERVED	0	R/W	Not used, always 0.
D[0]	CIRCUIT_BREAKER_FAULT	0	R/W	If turning off the MOSFET when circuit breaker fault happened. 0: Turning off (default) 1: No

I_{IN}/PFET faults consist of the input current fault and the MOSFET power dissipation fault. The IC offers no input power fault detection; it supports input power warning monitoring only.

REGISTER MAPS (continued)

REG0xD8: MFR_SPECIFIC_08 ALERT_MASK [Reset = 0x0820]

The ALERT_MASK command masks the nSMBA signal upon the occurrence of a specified fault or warning event. Each bit maps to one out of 14 separate analog and digital fault/warning events that normally cause nSMBA to assert. When the relevant bit is high, the associated condition leaves the nSMBA signal deasserted. Even if such a condition occurs, the registers that record the event (including STATUS registers and DIAGNOSTIC_WORD) are still updated, and for fault events of VIN_OV_FAULT, VIN_UV_FAULT, IIN/PFET_FAULT, CB_FAULT and OT_FAULT, the external MOSFET gate control function continues operation. Register access follows the PMBus word read/write protocol. The V_{IN} under-voltage fault flag defaults to logic 1 on power-up and is cleared to 0 after the input voltage crosses the resistor-programmed UVLO threshold for the first time.

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[15]	VOUT_UNDERVOLTAGE_WARN	0	R/W	If masking nSMBA signal pulled down when V_{OUT} under-voltage warning happened. 0: No mask (default) 1: Mask
D[14]	IIN_LIMIT_WARN	0	R/W	If masking nSMBA signal pulled down when input current exceeds current limit threshold. 0: No mask (default) 1: Mask
D[13]	VIN_UNDERVOLTAGE_WARN	0	R/W	If masking nSMBA signal pulled down when V_{IN} under-voltage warning happened. 0: No mask (default) 1: Mask
D[12]	VIN_OVERVOLTAGE_WARN	0	R/W	If masking nSMBA signal pulled down when V_{IN} over-voltage warning happened. 0: No mask (default) 1: Mask
D[11]	nPOWER_GOOD	1	R/W	If masking nSMBA signal pulled down when power good signal is low voltage. 0: No mask 1: Mask (default)
D[10]	OVERTEMP_WARN	0	R/W	If masking nSMBA signal pulled down when over-temperature warning happened. 0: No mask (default) 1: Mask
D[9]	RESERVED	0	R	Not used.
D[8]	OVERPOWER_LIMIT_WARN	0	R/W	If masking nSMBA signal pulled down when over power limit warning happened. 0: No mask (default) 1: Mask
D[7]	RESERVED	0	R	Not used.
D[6]	EXT_MOSFET_SHORTED	0	R/W	If masking nSMBA signal pulled down when external MOSFET shorted. 0: No mask (default) 1: Mask.
D[5]	VIN_UNDERVOLTAGE_FAULT	1	R/W	If masking nSMBA signal pulled down when V_{IN} under-voltage fault happened. 0: No mask 1: Mask (default)
D[4]	VIN_OVERVOLTAGE_FAULT	0	R/W	If masking nSMBA signal pulled down when V_{IN} over-voltage fault happened. 0: No mask (default) 1: Mask
D[3]	IIN/PFET_FAULT	0	R/W	If masking nSMBA signal pulled down when over-current or power fault happened. 0: No mask (default) 1: Mask
D[2]	OVERTEMPERATURE_FAULT	0	R/W	If masking nSMBA signal pulled down when over-temperature fault happened. 0: No mask (default) 1: Mask
D[1]	CML_FAULT	0	R/W	If masking nSMBA signal pulled down when communication fault happened. 0: No mask (default) 1: Mask
D[0]	CIRCUIT_BREAKER_FAULT	0	R/W	If masking nSMBA signal pulled down when circuit breaker fault happened. 0: No mask (default) 1: Mask

REGISTER MAPS (continued)

REG0xD9: MFR_SPECIFIC_09 DEVICE_SETUP [Reset = 0x00]

The DEVICE_SETUP command allows the host to override the pin configurations and define the operating mode of the SGM25716L. This command is accessed using the PMBus byte read/write protocol.

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:5]	RETRY_SETTING	000	R/W	111: Unlimited retries 110: 16 retries 101: 8 retries 100: 4 retries 011: 2 retries 010: 1 retries 001: No retries 000: Pin configured retries (default)
D[4]	CURRENT_LIMIT_SETTING	0	R/W	0: High setting (51mV, default) 1: Low setting (26mV)
D[3]	CB/CL_RATIO	0	R/W	0: Low setting (1.92 times, default) 1: High setting (3.88 times)
D[2]	CURRENT_LIMIT_CONFIGURATION	0	R/W	0: Use pin settings (default) 1: Use SMBus settings
D[1]	RESERVED	0	R/W	Unused.
D[0]	RESERVED	0	R/W	Unused.

To configure the current limit via this register, the current limit configuration D[2] must be set to 1, enabling register-based control of current limit function. Meanwhile, D[4] is used to select the target current limit level. If current limit configuration bit is disabled, device uses hardware pin settings.

The ratio of circuit breaker threshold to current-limit threshold is set via the D[3] (CB/CL ratio). Be aware that updates to the current-limit setting will not reset sampling data used by the telemetry averaging function. SGMICRO recommends waiting for one full averaging refresh cycle with the new current-limit setting prior to reading averaged measurement results.

It should also be noted that the current limit configuration influences the scaling coefficients applied to current and power measurements as well as the corresponding warning registers.

REG0xDA: MFR_SPECIFIC_10 BLOCK_READ [Reset = 0x08E000000000000000000000]

The BLOCK_READ command aggregates the DIAGNOSTIC_WORD, input and output telemetry data (I_{IN}, V_{OUT}, V_{IN}, P_{IN}), and temperature measurements. This allows retrieval of all operating parameters of the SGM25716L within one SMBus transaction. This data block has a length of 12 bytes, and the telemetry values are transmitted in the same format as individual READ_XXX commands (as illustrated in the table below). The contents of this block-read register are refreshed every clock cycle of 1μs. The BLOCK_READ function also ensures that measurements for V_{IN}, V_{OUT}, I_{IN}, and P_{IN} are fully time-synchronized.

When using separate read commands, individual samples may lose time alignment due to inherent communication delays in the protocol. This block read operation is performed using the PMBus multi-byte block-read protocol.

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[95:80]	DIAGNOSTIC_WORD	0000 1000 1110 0000	R	Report all of the SGM25716L faults and warnings.
D[79:64]	IIN_BLOCK	0000 0000 0000 0000	R	Report measured with the 12-bit ADC current sense voltage.
D[63:48]	VOUT_BLOCK	0000 0000 0000 0000	R	Report measured with the 12-bit ADC output voltage.
D[47:32]	VIN_BLOCK	0000 0000 0000 0000	R	Report measured with the 12-bit ADC input voltage.
D[31:16]	PIN_BLOCK	0000 0000 0000 0000	R	Report measured with the 12-bit ADC $V_{IN} \times I_{IN}$.
D[15:0]	TEMP_BLOCK	0000 0000 0000 0000	R	Report measured with the 12-bit ADC temperature.

REGISTER MAPS (continued)

REG0xDB: MFR_SPECIFIC_11 SAMPLES_FOR_AVG [Reset = 0x0000]

The SAMPLES_FOR_AVG command is a manufacturer-specific PMBus command that sets the quantity of sampling samples utilized for averaging calculations of I_{IN}, V_{IN}, V_{OUT} and P_{IN}. The decimal value corresponding to the AVGN nibble represents the exponent of 2 that determines the sample count; for instance, AVGN = 12 corresponds to an averaging window of 4096 samples. The SGM25716L supports the following sample counts: 1, 2, 4, 8, 16, 32, 64, 128, 256, 512, 1024, 2048, and 4096. The programmed sample count is applied equally to the averaging calculations of I_{IN}, V_{IN}, V_{OUT} and P_{IN} at the same time.

The device implements straightforward arithmetic averaging: consecutive sampled results are accumulated up to the programmed number of samples, and the sum is then divided by the sample count. The averaging process follows the formula below:

$$Y = (X_N + X_{N-1} + ... + X_0) / N \quad (26)$$

Once an averaging cycle is completed (e.g. after 4096 samples), a new averaging cycle restarts from scratch. The same number of new samples must be acquired before the updated average value becomes valid.

Table 8. SAMPLES_FOR_AVG Register

AVGN (b)	$N = 2^{AVGN}$	Averaging/Register Update Period (ms)
0000	1	1
0001	2	2
0010	4	4
0011	8	8
0100	16	16
0101	32	32
0110	64	64
0111	128	128
1000	256	256
1001	512	512
1010	1024	1024
1011	2048	2048
1100	4096	4096

Be aware that updates written to the SAMPLES_FOR_AVG register do not apply to averaged telemetry data until the ongoing averaging cycle completes. The PMBus byte read/write protocol shall be used for accesses to the SAMPLES_FOR_AVG register.

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[15:0]	SAMPLES_FOR_AVG	0000 0000 0000 0000	R/W	0000h ~ 000Ch: Exponent (AVGN) defining the quantity of samples used for averaging.

REG0xDC: MFR_SPECIFIC_12 READ_AVG_VIN [Reset = 0x0000]

The READ_AVG_VIN command provides the 12-bit ADC measurement of the averaged input voltage. In cases where new data is not available, the previously stored averaged value will be returned as the result. Should no prior averaged data exist, a default value of 0000h is provided instead. This register is accessed via the PMBus word-read protocol, and the coefficients specified in Table 6 shall be applied for data conversion.

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[15:0]	READ_AVG_VIN	0000 0000 0000 0000	R	0000h ~ 0FFFh: Averaged input voltage measurement.

REGISTER MAPS (continued)

REG0xDD: MFR_SPECIFIC_13 READ_AVG_VOUT [Reset = 0x0000]

The READ_AVG_VOUT command retrieves the average voltage value of the current sense signal sampled with the 12-bit ADC. When averaged data remains unavailable, the system will return the default value (0x0000) or the most recent valid data stored previously. Access to this command uses the PMBus word-read protocol, and the coefficients presented in Table 6 shall be utilized for data interpretation.

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[15:0]	READ_AVG_VOUT	0000 0000 0000 0000	R	0000h ~ 0FFFh: Averaged output voltage measurement.

REG0xDE: MFR_SPECIFIC_14 READ_AVG_IIN [Reset = 0x0000]

The READ_AVG_IIN command outputs the averaged current sense voltage acquired with the 12-bit ADC. If the averaged measurement is not yet valid, the device returns either the default value 0x0000 or the last valid set of data. This parameter is read using the PMBus word-read protocol, and the coefficients listed in Table 6 apply to this register.

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[15:0]	READ_AVG_IIN	0000 0000 0000 0000	R	0000h ~ 0FFFh: Averaged current sense voltage measurement.

REG0xDF: MFR_SPECIFIC_15 READ_AVG_PIN [Reset = 0x0000]

The READ_AVG_PIN command returns the upper 12 bits derived from the averaged V_{IN} × I_{IN} product sampled with the 12-bit ADC. When averaged data remains unavailable, the register outputs either the default value 0000h or the previously calculated result. Data is retrieved via the PMBus word-read protocol, and the coefficients provided in Table 6 must be used for this register.

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[15:0]	READ_AVG_PIN	0000 0000 0000 0000	R	0000h ~ 0FFFh: Averaged input voltage measurement × input current sense voltage.

REG0xE0: MFR_SPECIFIC_16 BLACK_BOX_READ [Reset = 0x08E000000000000000000000]

The BLACK BOX READ command obtains the BLOCK READ data latched by the SGM25716L when the nSMBA signal is first asserted. The function is reactivated via the CLEAR_FAULTS command. Format is identical to the BLOCK_READ registers, except for that the contents refresh at the nSMBA edge, not the internal clock edge. The command is read using the PMBus block-read protocol.

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[95:80]	DIAGNOSTIC_WORD	0000 1000 1110 0000	R	Report all of the SGM25716L faults and warnings.
D[79:64]	IIN_ALERT	0000 0000 0000 0000	R	Reports the current sense voltage sampled with the 12-bit ADC at the time of alert assertion.
D[63:48]	VOUT_ALERT	0000 0000 0000 0000	R	Reports the output voltage sampled with the 12-bit ADC at the time of alert assertion.
D[47:32]	VIN_ALERT	0000 0000 0000 0000	R	Reports the input voltage sampled with the 12-bit ADC at the time of alert assertion.
D[31:16]	PIN_ALERT	0000 0000 0000 0000	R	Reports the V_{IN} × I_{IN} value sampled with the 12-bit ADC at the time of alert assertion.
D[15:0]	TEMP_ALERT	0000 0000 0000 0000	R	Reports the temperature sampled with the 12-bit ADC at the time of alert assertion.

REGISTER MAPS (continued)

REG0xE1: MFR_SPECIFIC_17 READ_DIAGNOSTIC_WORD [Reset = 0x08E0]

The PMBus READ_DIAGNOSTIC_WORD command reports all faults and warning events of the SGM25716L within one read transaction. Instead of sending multiple read accesses to different status registers as the conventional handling method upon nSMBA assertion, users may perform a single word read on the DIAGNOSTIC_WORD register. The PMBus word-read protocol shall be adopted to read the READ_DIAGNOSTIC_WORD command. The READ_DIAGNOSTIC_WORD value is also provided in BLOCK_READ, BLACK_BOX_READ, and AVG_BLOCK_READ operations.

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[15]	VOUT_UNDERVOLTAGE_WARN	0	R	A V_{OUT} under-voltage warning has occurred.
D[14]	IIN_OP_WARN	0	R	An I_{IN} over-current or over power warning has occurred.
D[13]	VIN_UNDERVOLTAGE_WARN	0	R	A V_{IN} under-voltage warning has occurred.
D[12]	VIN_OVERVOLTAGE_WARN	0	R	A V_{IN} over-voltage warning has occurred.
D[11]	nPOWER GOOD	1	R	The Power Good signal has been deasserted.
D[10]	OVER_TEMPERATURE_WARN	0	R	An over-temperature warning has occurred.
D[9]	TIMER_LATCHED_OFF	0	R	Communication time out has occurred.
D[8]	EXT_MOSFET_SHORTED	0	R	An external MOSFET shorted has occurred.
D[7]	CONFIG_PRESET	1	R	Defaults loaded.
D[6]	DEVICE_OFF	1	R	Failure of MOSFET turn-on.
D[5]	VIN_UNDERVOLTAGE_FAULT	1	R	A V_{IN} under-voltage fault has occurred.
D[4]	VIN_OVERVOLTAGE_FAULT	0	R	A V_{IN} over-voltage fault has occurred.
D[3]	IIN_OC/PFET_OP_FAULT	0	R	An I_{IN} over-current or over power fault has occurred.
D[2]	OVER_TEMPERATURE_FAULT	0	R	An over-temperature fault has occurred.
D[1]	CML_FAULT	0	R	A bus communication fault occurred.
D[0]	CIRCUIT_BREAKER_FAULT	0	R	A circuit breaker fault has occurred.

REG0xE2: MFR_SPECIFIC_18 AVG_BLOCK_READ [Reset = 0x08E000000000000000000000]

The AVG_BLOCK_READ command merges DIAGNOSTIC_WORD, averaged input and output telemetry readings (I_{IN}, V_{OUT}, V_{IN} and P_{IN}), together with temperature data. This enables retrieval of all device operating parameters within one single PMBus transaction. This data block is 12 bytes in length, and the telemetry values are transmitted in the same format as individual READ_AVG_XXX commands, as detailed in Table 9. The AVG_BLOCK_READ function also ensures time alignment among V_{IN}, V_{OUT} and I_{IN} measurements, which may not be guaranteed when reading these values through separate PMBus commands. The SMBus multi-byte block-read protocol is used to access data from the AVG_BLOCK_READ command.

Table 9. AVG_BLOCK_READ Register Format

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[95:80]	DIAGNOSTIC_WORD	0000 1000 1110 0000	R	Report all of the SGM25716L faults and warnings.
D[79:64]	AVG_IIN	0000 0000 0000 0000	R	Report the 12-bit ADC sampled average current sense voltage.
D[63:48]	AVG_VOUT	0000 0000 0000 0000	R	Report the 12-bit ADC sampled average output voltage.
D[47:32]	AVG_VIN	0000 0000 0000 0000	R	Report the 12-bit ADC sampled average input voltage.
D[31:16]	AVG_PIN	0000 0000 0000 0000	R	Report the 12-bit ADC sampled average $V_{IN} \times I_{IN}$.
D[15:0]	TEMPERATURE	0000 0000 0000 0000	R	Report the 12-bit ADC sampled average temperature.

REGISTER MAPS (continued)

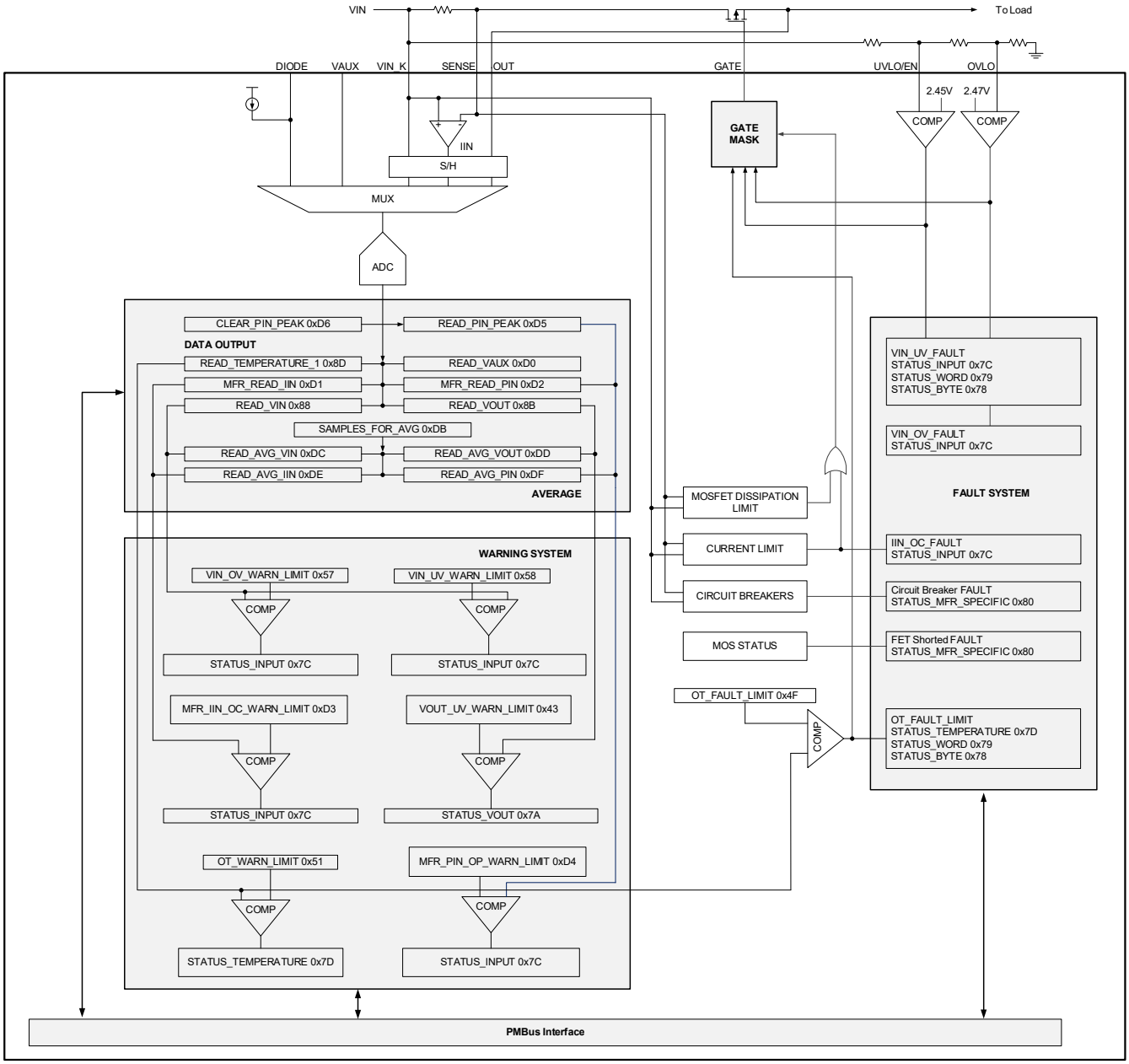


Figure 20. Command/Register and Alert Flow Diagram

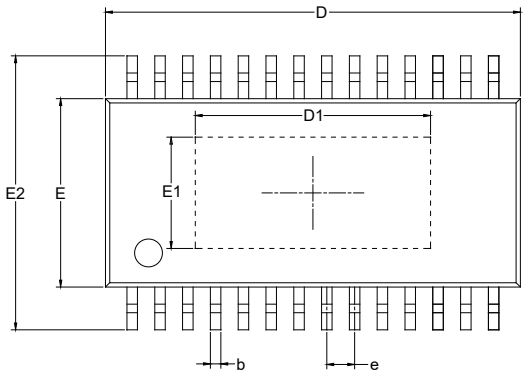
REVISION HISTORY

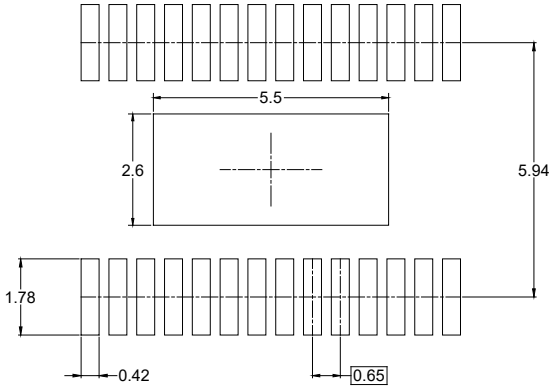
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original to REV.A (NOVEMBER 2026)	Page
Changed from product preview to production data	All

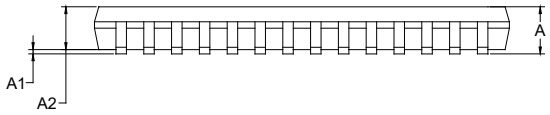
PACKAGE OUTLINE DIMENSIONS

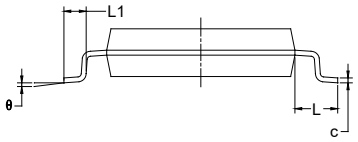
TSSOP-28 (Exposed Pad)





RECOMMENDED LAND PATTERN (Unit: mm)





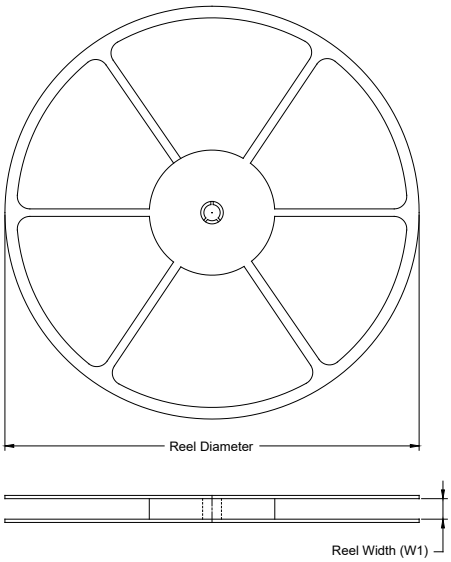
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A		1.200		0.047
A1	0.050	0.150	0.002	0.006
A2	0.800	1.050	0.031	0.041
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
D	9.600	9.800	0.378	0.386
D1	4.700	5.700	0.185	0.224
E	4.300	4.500	0.169	0.177
E1	2.400	2.800	0.094	0.110
E2	6.200	6.600	0.244	0.260
e	0.650 BSC		0.026 BSC	
L	1.000 BSC		0.039 BSC	
L1	0.450	0.750	0.018	0.030
θ	0°	8°	0°	8°

NOTES:

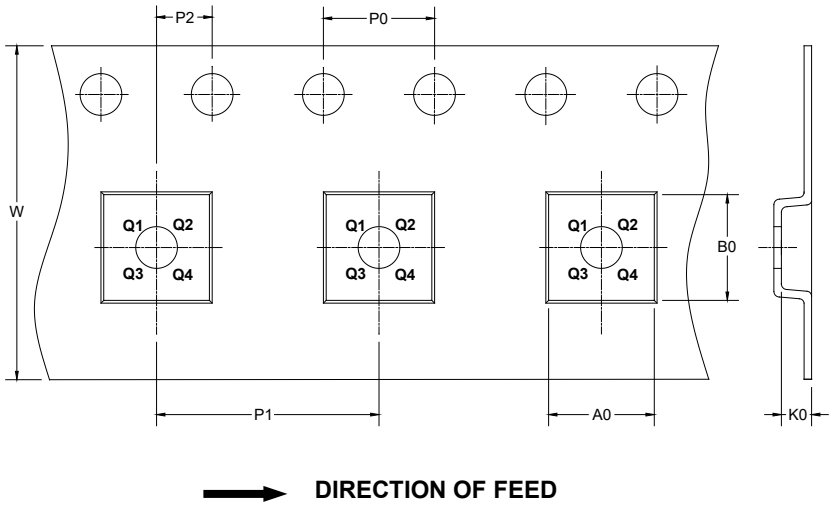
1. Body dimensions do not include mold flash or protrusion.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-153.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



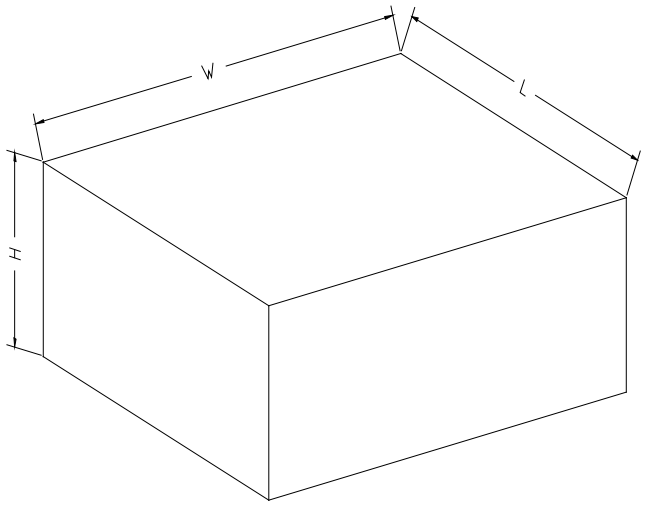
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TSSOP-28 (Exposed Pad)	13"	16.4	6.80	10.25	1.60	4.0	8.0	2.0	16.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002