

GENERAL DESCRIPTION

The SGM61264 is a high efficiency synchronous Buck converter with integrated 25mΩ high-side and 11mΩ low-side power MOSFETs and a wide 4.5V to 28V input range suitable for 12V, 19V, 24V power rails. It supports a wide output range from 0.6V to 13V with up to 6A current load.

With adaptive constant on-time (ACOT) control, the SGM61264 provides the very fast load transient response and excellent output regulation. It also does not require external compensation and supports low equivalent series resistance (ESR) output capacitors.

The SGM61264 supports three operating modes at light load by configuring the resistor R_{MODE} connected between the MODE pin and AGND. The SGM61264 operates in FCCM mode with the MODE pin floating or a $R_{MODE} \geq 500k\Omega$ connected to AGND, which provides a low output voltage ripple at light load. To maintain high efficiency at very low load condition, SGM61264 provides PFM mode with MODE pin short to AGND or $R_{MODE} \leq 10k\Omega$ connected to AGND. SGM61264 is set to USM (Ultra-Sonic Mode) to eliminate audible noise in light load with R_{MODE} between 100kΩ and 150kΩ range.

Protection features of the SGM61264 include the cycle by cycle current limit, under-voltage lockout (UVLO), over-voltage protection (OVP), output under-voltage protection (UVP) and over-temperature protection (OTP). The SGM61264 provides power good (PG) indicator to monitor the output and IC status and it also supports the output discharge function.

The SGM61264 is available in a Green TQFN-3×3-10L package.

FEATURES

- Wide 4.5V to 28V Input Voltage Range
- 0.6V to 13V Output Voltage Range
- 65μA Quiescent Current and 3.5μA Shutdown Supply Current
- 6A Maximum Continuous Output Current
- Low $R_{DS(on)}$ MOSFETs (HS 25mΩ and LS 11mΩ)
- 0.6V Reference Voltage and $\pm 1.5\%$ accuracy from -40°C to $+150^{\circ}\text{C}$
- Adaptive Constant On-Time (ACOT) Control Mode for Fast Transient Response
- PFM, USM and FCCM Selectable for Light Load Operation
- Internal 2ms Soft-Start
- Built-in Output Discharge Function
- 540kHz Switching Frequency
- Power Good Indicator
- Input Under-Voltage Lockout (UVLO)
- Cycle-by-Cycle Over-Current Limit Protection
- Hiccup Mode Protection for OVP and UVP
- Over-Voltage Protection (OVP)
- Output Under-Voltage Protection (UVP)
- Over-Temperature Protection (OTP)
- Available in a Green TQFN-3×3-10L Package

APPLICATIONS

Multi-Function Printer
TV

Factory Automation and Control

General Purposes for 12V, 19V, 24V Power-Bus Supply

SIMPLIFIED SCHEMATIC

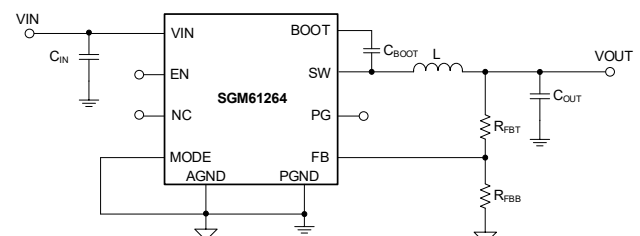


Figure 1. Simplified Schematic

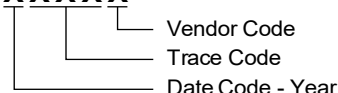
PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM61264	TQFN-3×3-10L	-40°C to +150°C	SGM61264TTUS10G/TR	61264 TTUS10 XXXXXX	Tape and Reel, 4000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.

XXXXXX



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

VIN Voltage	-0.3V to 32V
BOOT Voltage	-0.3V to SW + 6V
BOOT-SW Voltage	-0.3V to 6V
EN, FB, MODE Voltage	-0.3V to 6V
PGND, AGND	-0.3V to 0.3V
SW Voltage	-0.3V to 32V
SW (Less than 10ns) Voltage	-4V to 34V
VOOUT Voltage	-0.3V to 16V
PG Voltage	-0.3V to 6V
Package Thermal Resistance	
TQFN-3×3-10L, θ_{JA}	64.5°C/W
TQFN-3×3-10L, θ_{JB}	6.1°C/W
TQFN-3×3-10L, θ_{JC}	49.1°C/W
Junction Temperature	+150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 10s)	+260°C
ESD Susceptibility ^{(1) (2)}	
HBM	±2000V
CDM	±1000V

NOTES:

1. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.
2. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

RECOMMENDED OPERATING CONDITIONS

VIN Voltage	4.5V to 28V
BOOT Voltage	4.5V to 33.5V
BOOT-SW Voltage	-0.1V to 5.5V
EN, FB, MODE Voltage	-0.1V to 5.5V
PGND, AGND	-0.1V to 0.1V
SW Voltage	-0.1V to 28V
PG Voltage	-0.1V to 5.5V
VOOUT Voltage	-0.1V to 13V
Operating Junction Temperature Range	-40°C to +150°C

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

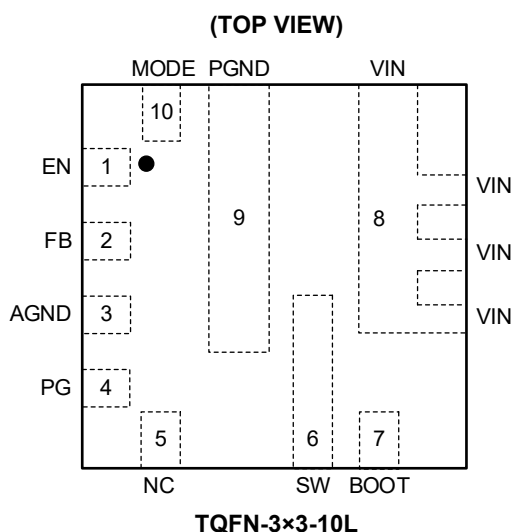
ESD SENSITIVITY CAUTION

This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION



PIN DESCRIPTION

PIN	NAME	TYPE	FUNCTION
1	EN	AI	Enable Input Control. Driving EN high or leaving this pin floating enables the converter. A resistor divider can be used to imply an UVLO function.
2	FB	AI	Output Feedback Input. Connect FB to the tap of an external resistor divider from the output to AGND to set the output voltage.
3	AGND	P	Ground of Internal Analog Circuitry. Connect AGND to PGND plane at a single point.
4	PG	AO	Open-Drain Power Good Indicator. It is asserted low if output voltage is out of PG threshold due to over-voltage, under-voltage, thermal shutdown, EN shutdown or during soft-start. Pull up PG pin to a DC voltage ($\leq 5V$) through a 100k Ω pull-up resistor, such as V_{OUT} or an external DC supply.
5	NC	—	Not Connected. Keep this pin floating.
6	SW	P	Switching Node Terminal. Connect the output inductor to this pin with wide and short tracks and act as the return path for the high-side switch high bootstrap circuit.
7	BOOT	P	Supply Input for the Gate Drive Voltage of the High-side MOSFET. Connect a 0.1 μF bootstrap capacitor between BOOT and SW.
8	VIN	P	Input Voltage Supply Pin. Drain terminal of high-side MOSFET. Connect the input decoupling capacitors of 100nF between VIN and PGND.
9	PGND	P	Power GND Terminal. Source terminal of low-side MOSFET.
10	MODE	AI	Operation Mode Selection Pin. Leaving this pin floating or connecting a resistor $R_{MODE} \geq 500k\Omega$ between MODE pin and AGND forces the SGM61264 into FCCM. Connecting this pin to AGND or connecting a resistor $R_{MODE} \leq 10k\Omega$ forces the SGM61264 into PFM under light load. Connecting a resistor R_{MODE} (100k Ω to 150k Ω) from this pin to AGND enables Ultra-Sonic Mode (USM), which ensures at least 33kHz switching frequency at light load.

NOTE: AI = analog input, AO = analog output, P = power or ground.

ELECTRICAL CHARACTERISTICS

(V_{IN} = 4.5V to 28V and T_J = -40°C to +150°C, all typical values are measured at T_J = +25°C and V_{IN} = 12V, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current						
Quiescent Current, Operating at PFM Mode	I _Q	V _{FB} = 0.7V, MODE = AGND		65		μA
Shutdown Supply Current	I _{SD}	V _{EN} = 0V		3.5		μA
Under-Voltage Lockout						
V _{IN} Under-Voltage Lockout	V _{UVLO_RISING}	V _{IN} rising	3.9	4.2	4.5	V
	V _{UVLO_FALLING}	V _{IN} falling	3.4	3.7	4.0	V
	V _{UVLO_HYS}	Hysteresis V _{IN} voltage		500		mV
Enable (EN Pin)						
EN Input Current	I _{EN_INPUT}	V _{EN} = 1.1V		1		μA
EN Hysteresis Current	I _{EN_HYS}	V _{EN} = 1.3V		4		μA
Enable Threshold	V _{EN_ON}	EN rising		1.2	1.3	V
	V _{EN_OFF}	EN falling	1.0	1.1		V
Voltage Reference (FB Pin)						
Voltage Reference	V _{REF}	Continuous mode operation	0.592	0.600	0.608	V
Input Leakage Current at FB Pin	I _{LKG_FB}	V _{FB} = 0.6V	-1		1	μA
MOSFET						
High-side Switch Resistance	R _{DSON_H}	V _{IN} = 12V, V _{BOOT} - V _{SW} = 5V		25		mΩ
Low-side Switch Resistance	R _{DSON_L}	V _{IN} = 12V		11		mΩ
Current Limit						
Valley Current Limit	I _{OCL}	V _{IN} = 12V, V _{OUT} = 5V, L = 3.3μH, close loop	6.3	8.5	10.6	A
Reverse Current Limit for FCCM Mode	I _{OC_REV}	V _{IN} = 12V, V _{OUT} = 5V, L = 3.3μH, close loop	2.3	3.8	5.4	A
Power Good						
PG Lower Threshold (Falling) ⁽¹⁾	V _{PG_LOW_DN}	V _{FB} falling, % of V _{REF}		85		%
PG Lower Threshold (Rising) ⁽¹⁾	V _{PG_LOW_UP}	V _{FB} rising, % of V _{REF}		90		
PG Upper Threshold (Falling)	V _{PG_HIGH_DN}	V _{FB} falling, % of V _{REF}	102	110	118	
PG Upper Threshold (Rising)	V _{PG_HIGH_UP}	V _{FB} rising, % of V _{REF}	107	115	123	
PG Sink Current	I _{PGSINK}	V _{FB} = 0.5V, V _{PG} = 0.5V		1.6		mA
PG Leakage Current	I _{PGLK}	V _{PG} = 5.5V	-1		1	μA
Frequency						
Switching Frequency	f _{SW}	V _{OUT} = 5V, continuous mode operation		540		kHz
Output Under-Voltage and Over-Voltage Protection						
Output OVP Threshold	V _{OVP}	OVP detect (V _{FB} rising)		125		%
Output OVP Threshold Hysteresis ⁽¹⁾	V _{OVP_HYS}			3.5		
Output UVP Threshold ⁽¹⁾	V _{UVP}	Hiccup detect (V _{FB} falling)		65		%
Thermal Shutdown						
Thermal Shutdown Threshold	T _{SD}	Temperature rising		165		°C
Thermal Shutdown Threshold Hysteresis	T _{HYS}			30		
SW Discharge Resistance						
V _{OUT} Discharge Resistance	R _{DIS}	V _{EN} = 0V, V _{SW} = 0.5V		192	250	Ω

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 4.5V to 28V and T_J = -40°C to +150°C, all typical values are measured at T_J = +25°C and V_{IN} = 12V, unless otherwise noted.)

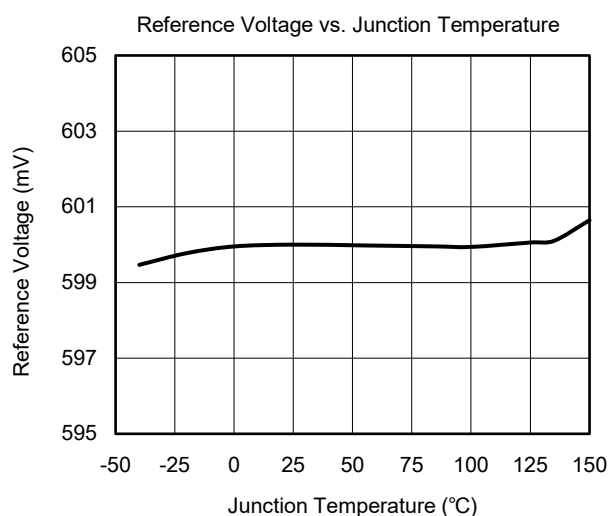
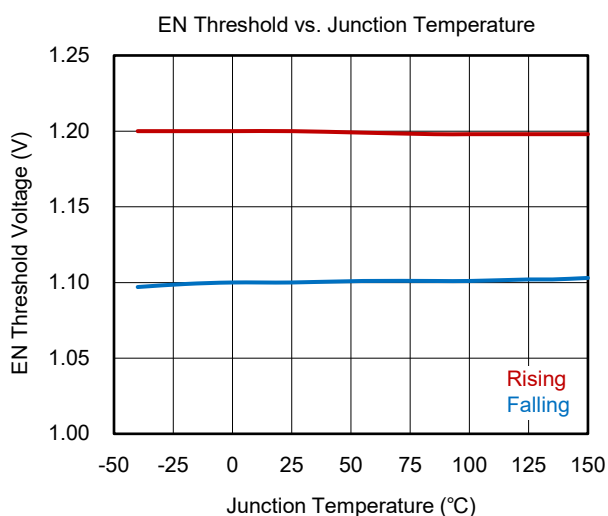
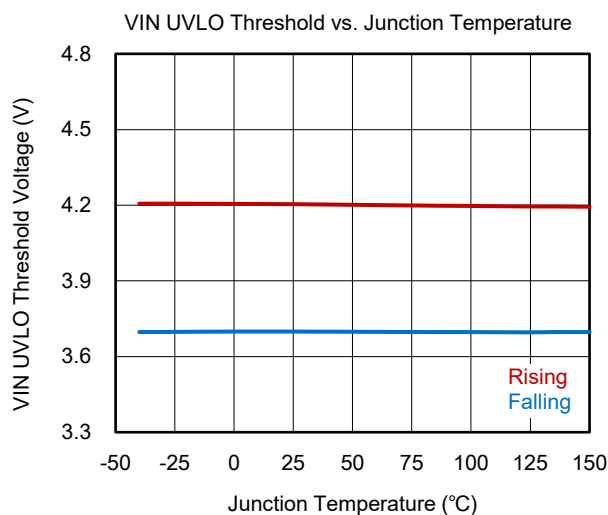
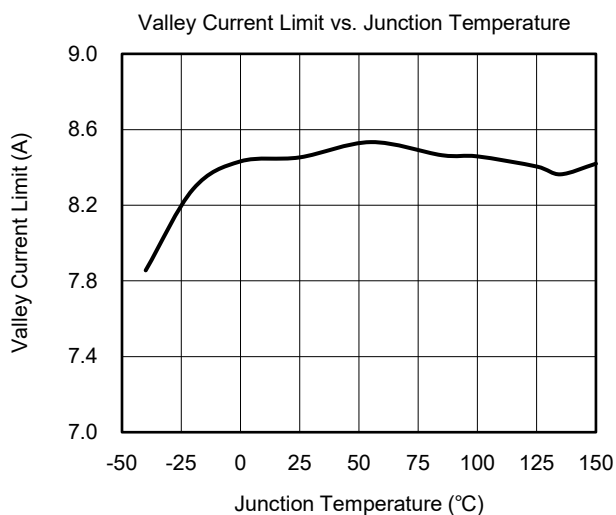
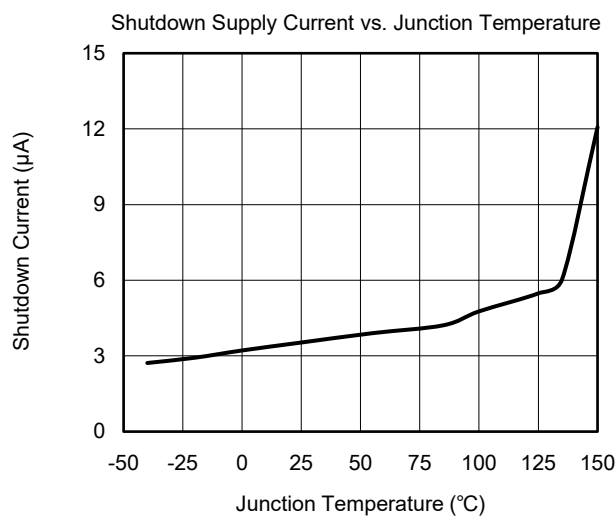
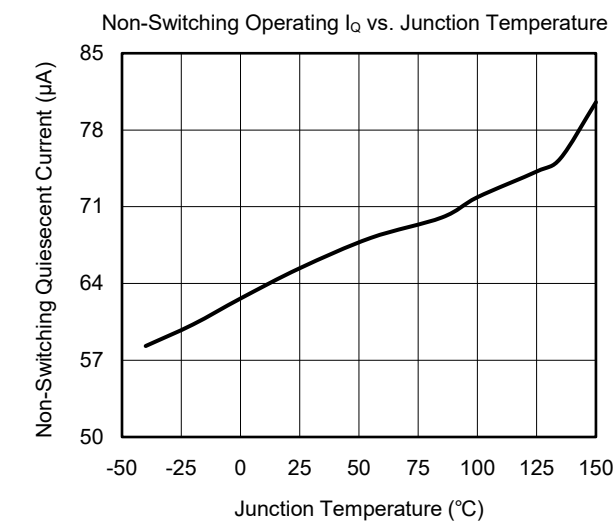
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
On-Time Timer Control						
Minimum On-Time ⁽¹⁾	t_{ON_MIN}			50		ns
Minimum Off-Time ⁽¹⁾	t_{OFF_MIN}	$V_{FB} = 0.5V$, measure SW at $V_{IN} = 12V$		200		ns
Soft-Start						
Soft-Start Time ⁽¹⁾	t_{SS}	Regulation range from 0% to 100%		2		ms
Output Under-Voltage Protection						
UV Protection Deglitch Time ⁽¹⁾	t_{UVP_WAIT}	UV triggered (V_{FB} lower than 65% V_{REF})		0.25		ms
UV Protection Hiccup Time before Recovery ⁽¹⁾	t_{UVP_HICCUP}			25		ms

NOTE:

1. Not production tested. Ensured by design and engineering sample correlation.

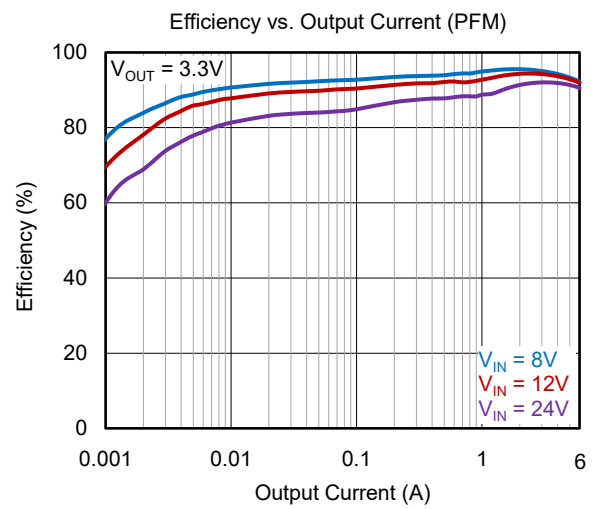
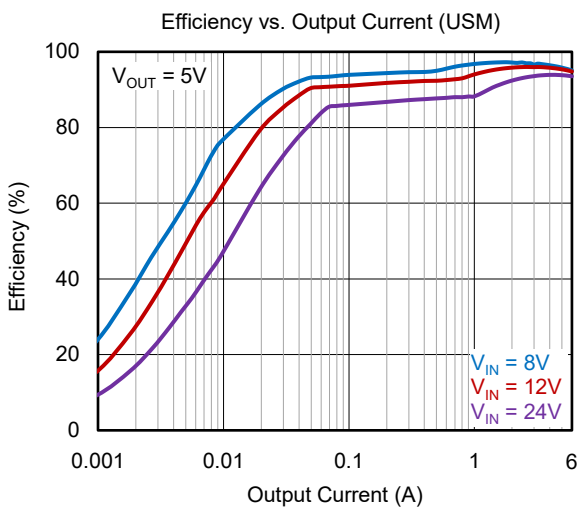
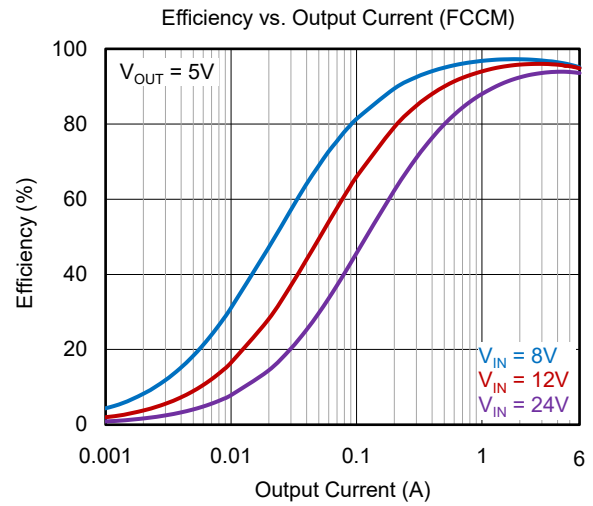
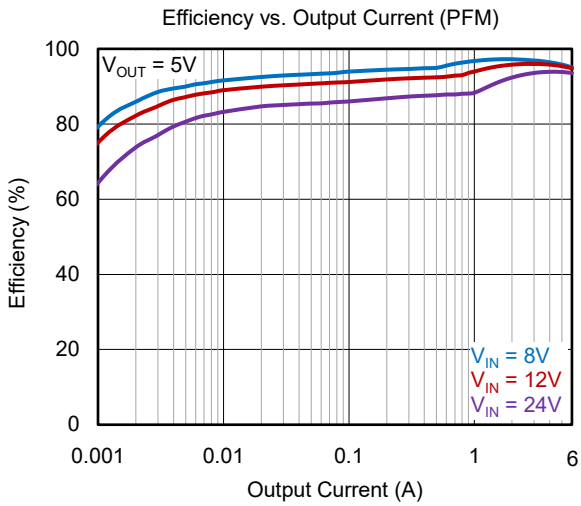
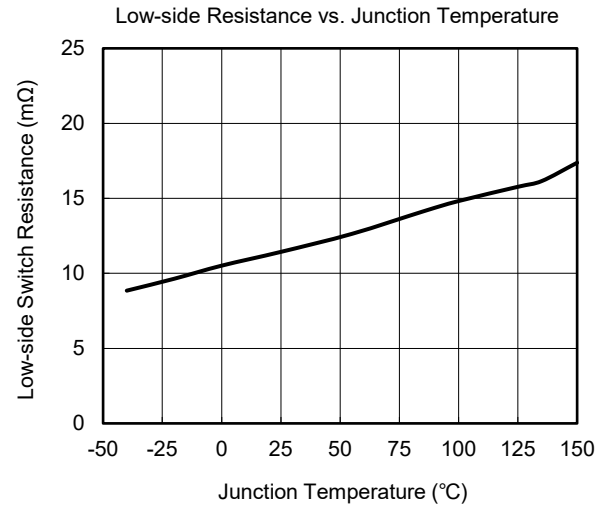
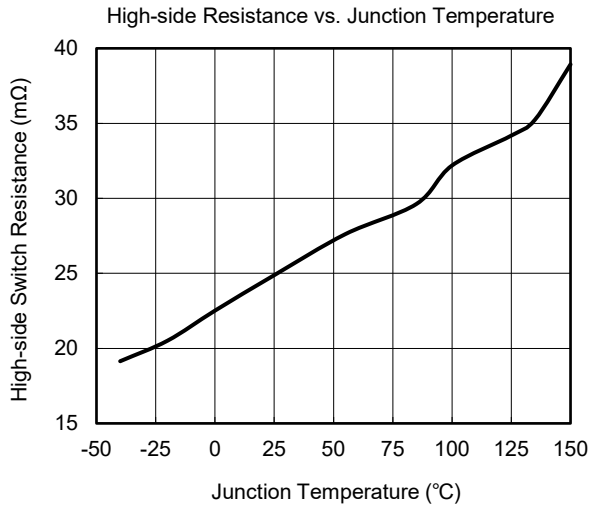
TYPICAL PERFORMANCE CHARACTERISTICS

$T_A = +25^\circ\text{C}$, $V_{IN} = 12\text{V}$, $V_{OUT} = 5\text{V}$, $L = 3.3\mu\text{H}$ (DCR = $5.2\text{m}\Omega$), EN = floating, $f_{SW} = 540\text{kHz}$, and $C_{OUT} = 22\mu\text{F} \times 2$, unless otherwise noted.



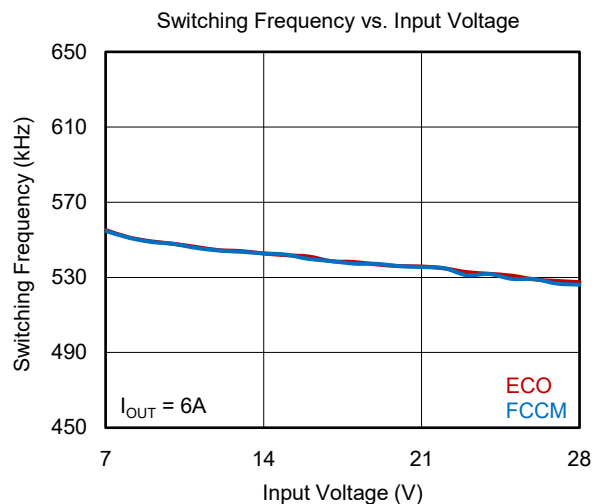
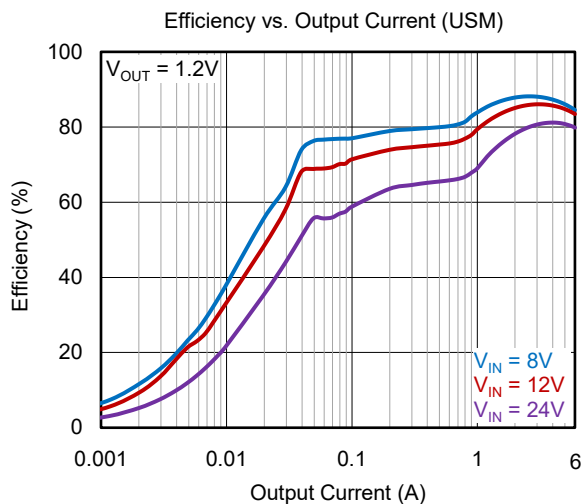
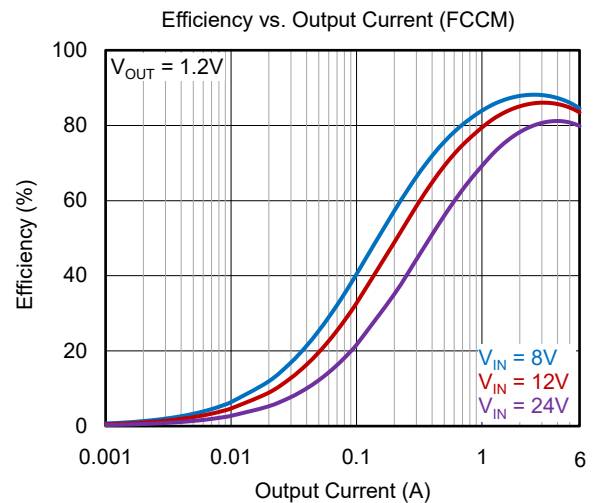
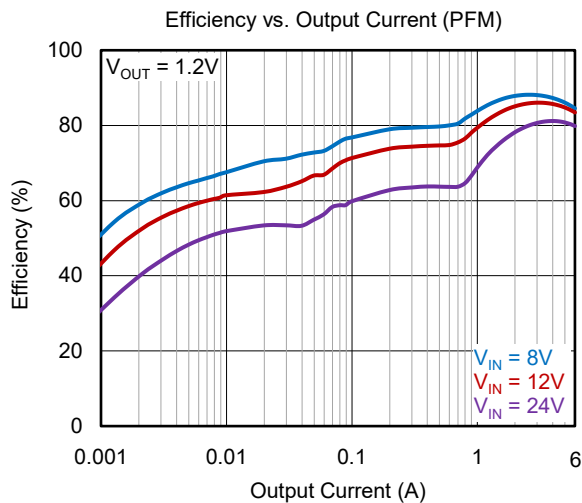
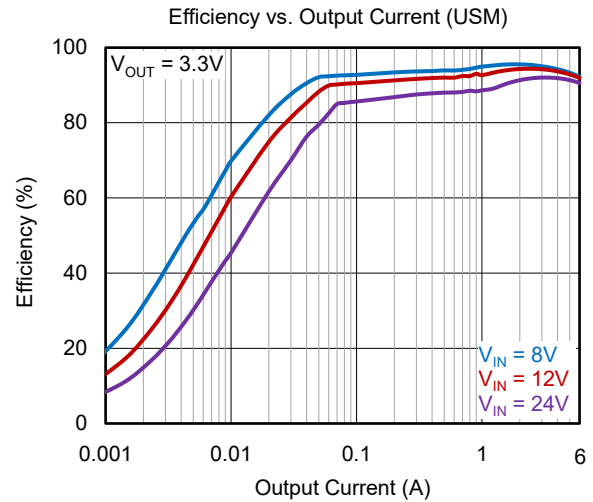
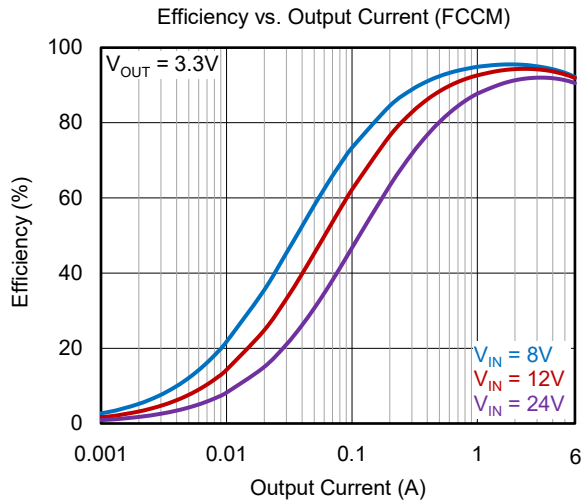
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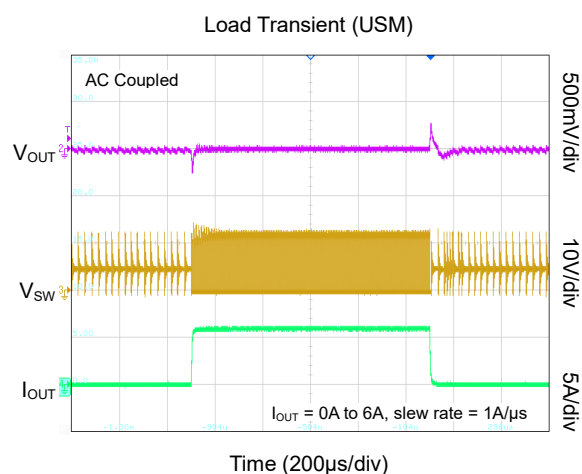
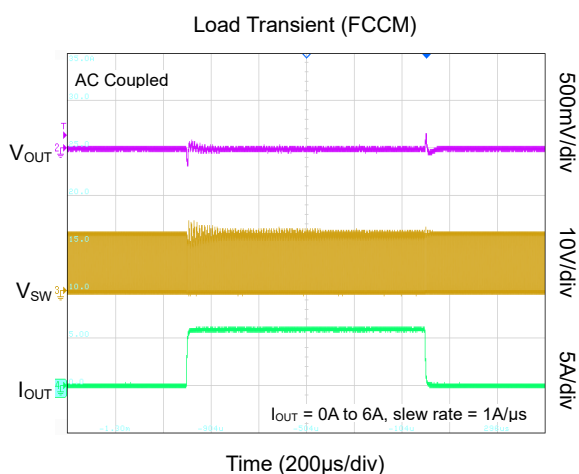
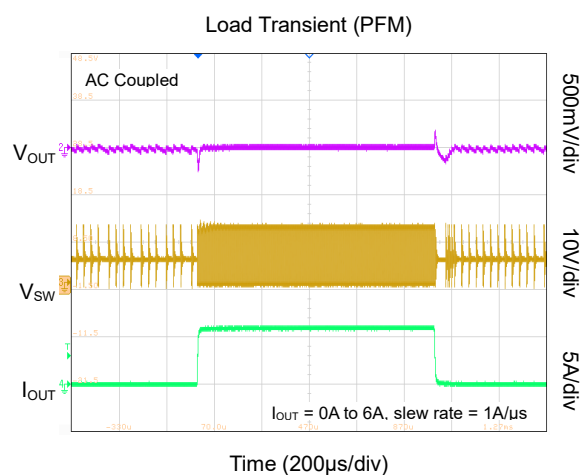
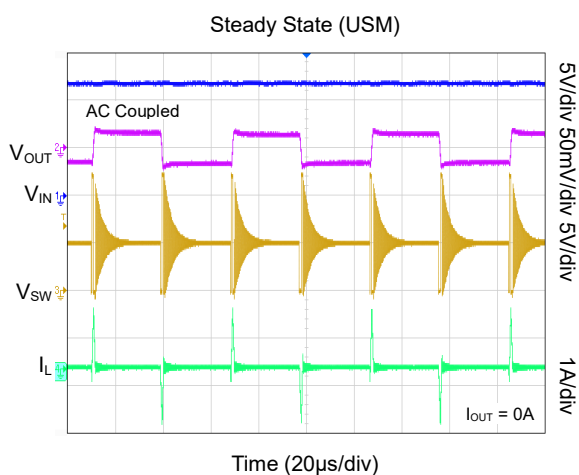
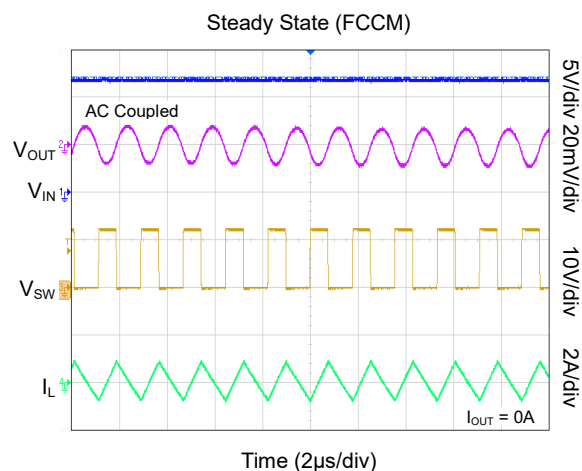
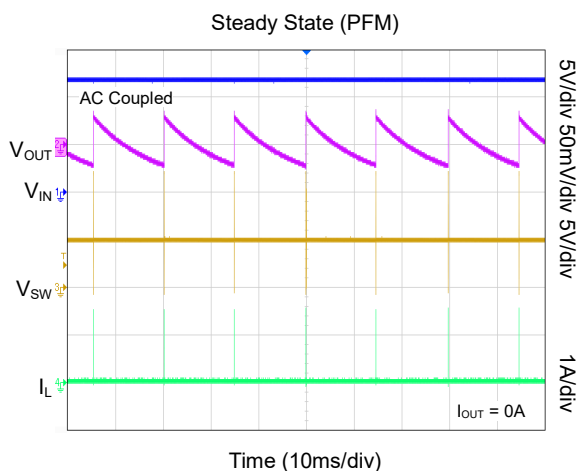
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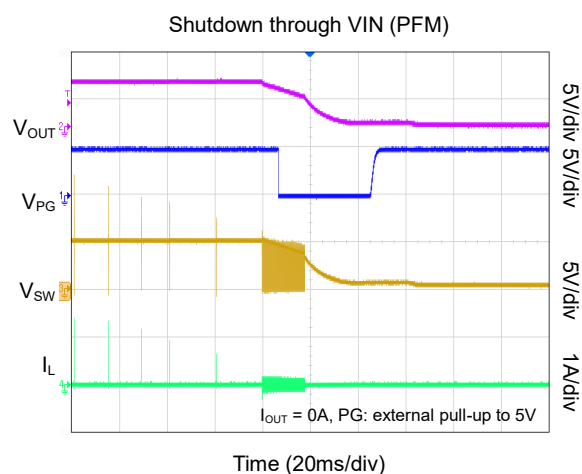
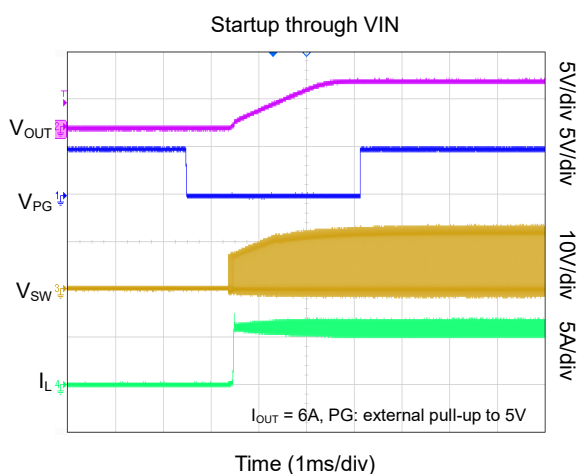
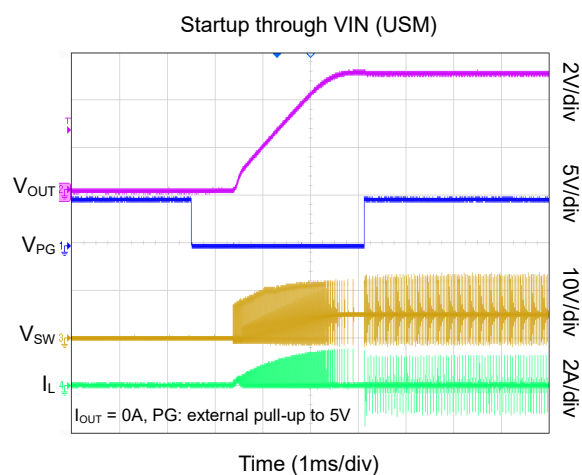
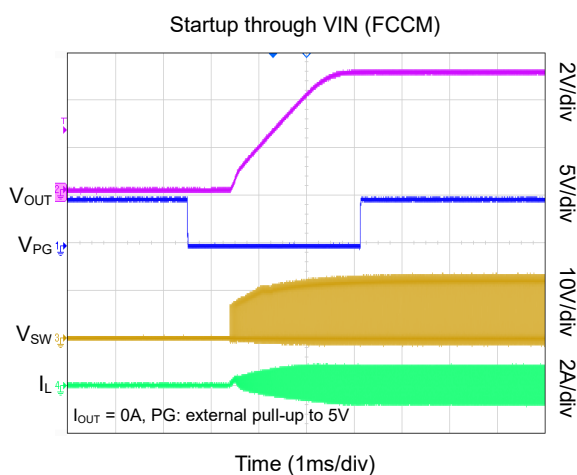
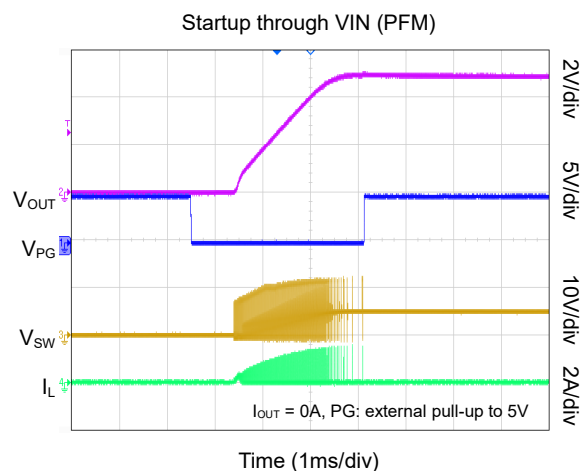
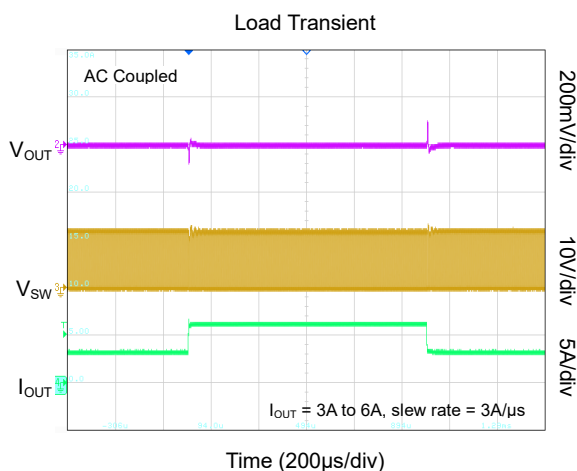
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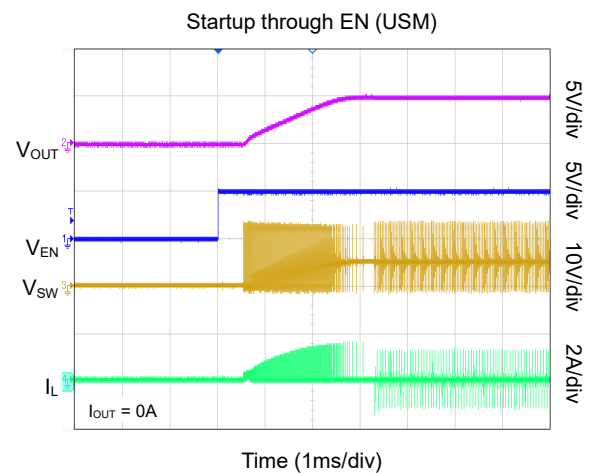
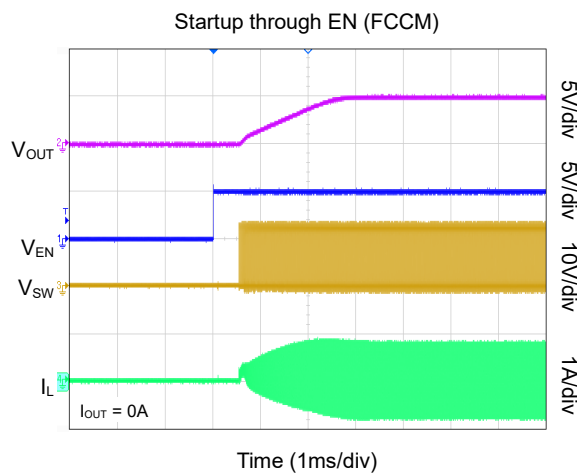
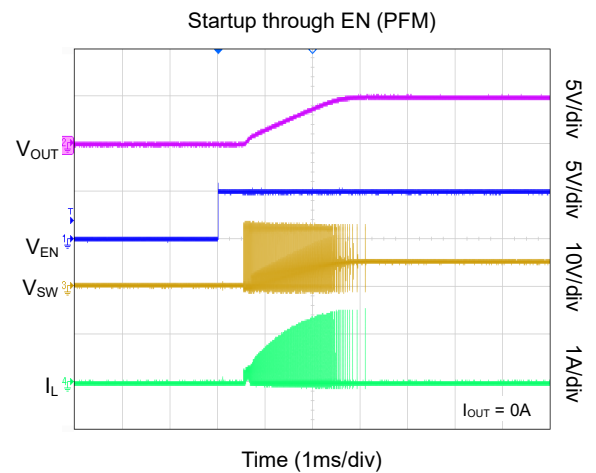
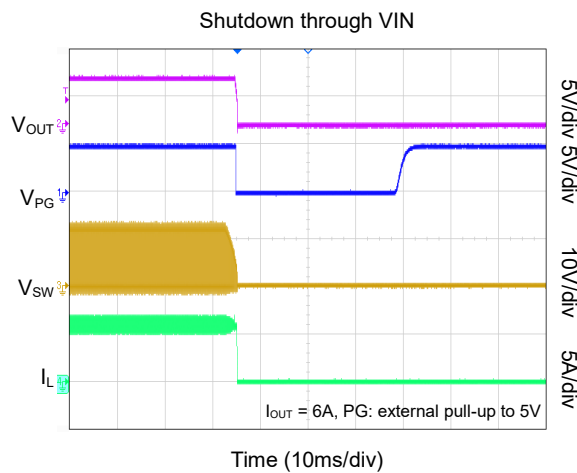
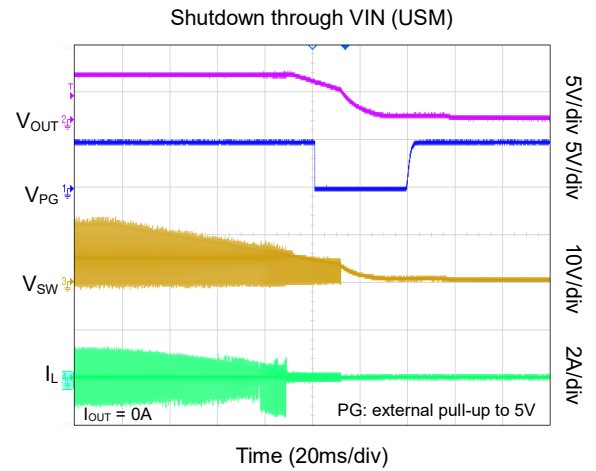
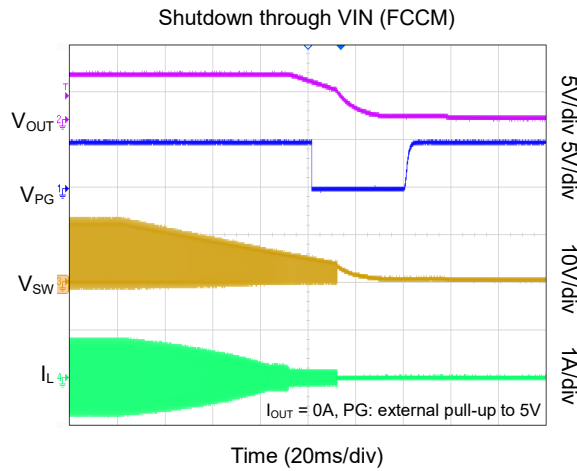
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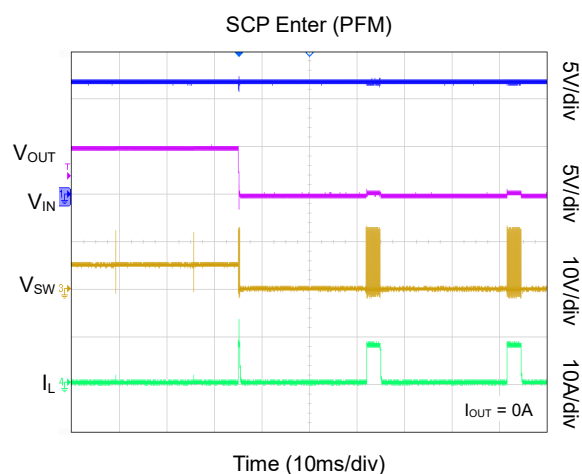
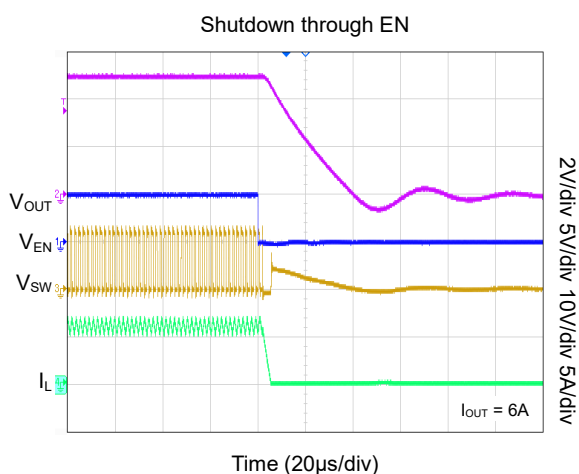
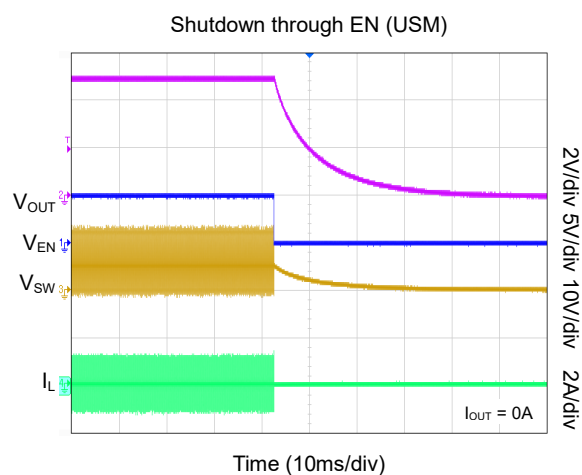
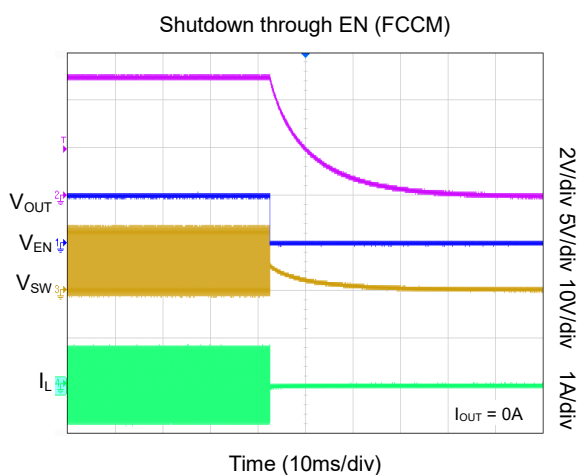
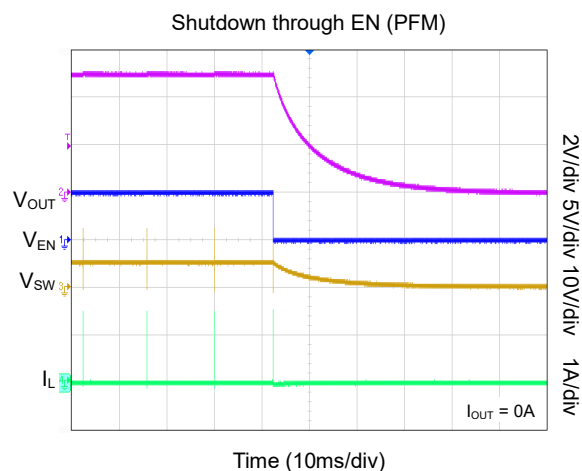
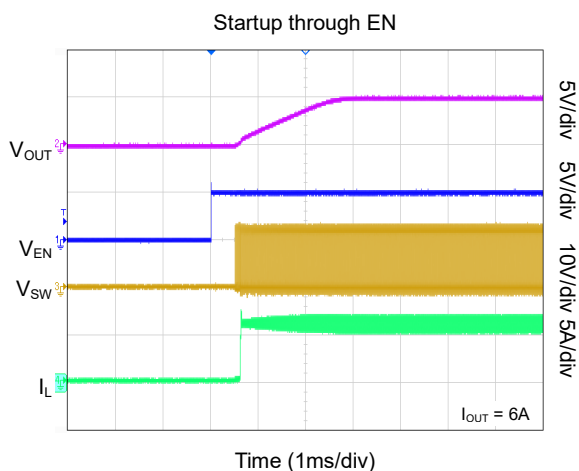
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$T_A = +25^\circ\text{C}$, $V_{IN} = 12\text{V}$, $V_{OUT} = 5\text{V}$, $L = 3.3\mu\text{H}$ (DCR = $5.2\text{m}\Omega$), $EN = \text{floating}$, $f_{SW} = 540\text{kHz}$, and $C_{OUT} = 22\mu\text{F} \times 2$, unless otherwise noted.



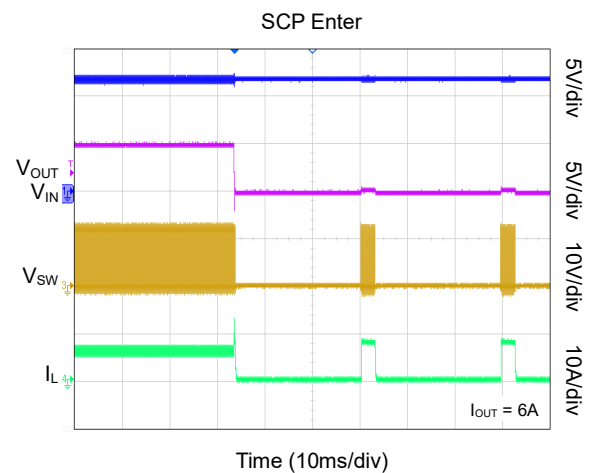
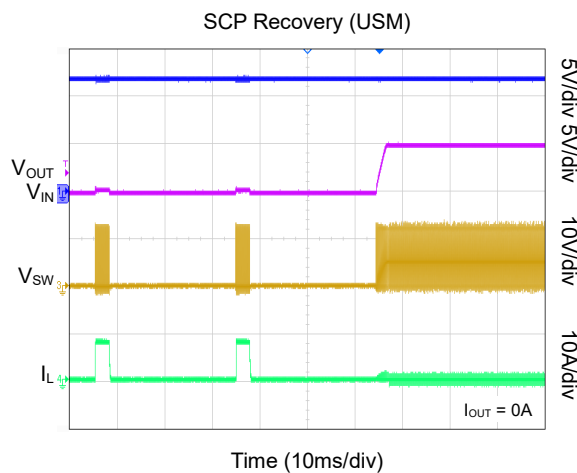
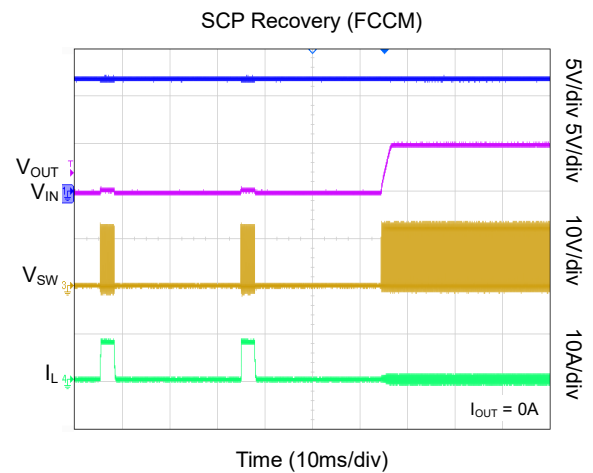
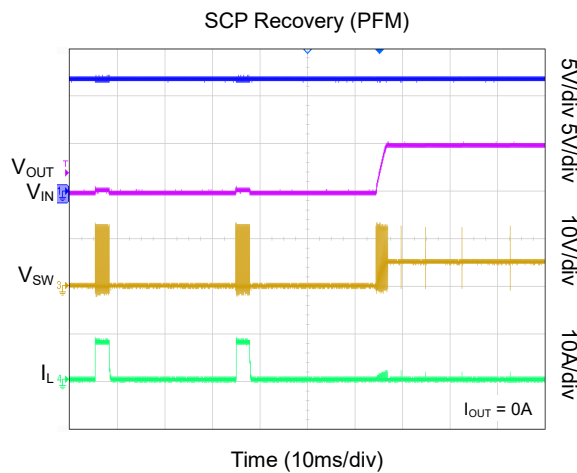
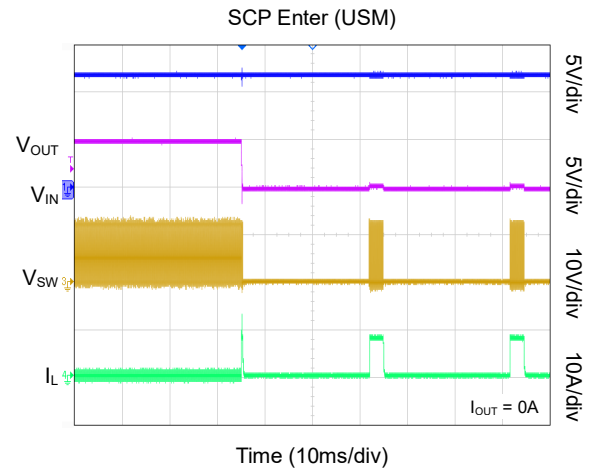
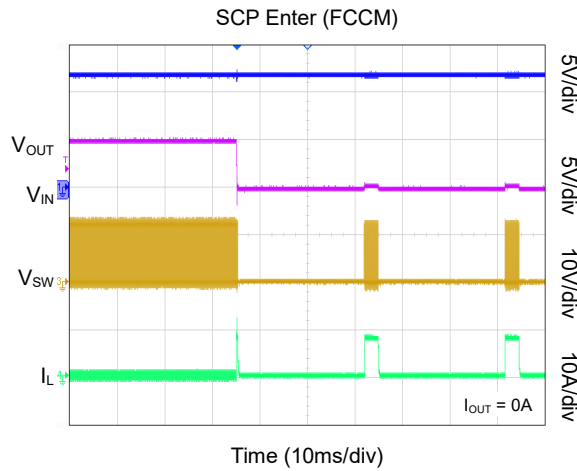
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$T_A = +25^\circ\text{C}$, $V_{IN} = 12\text{V}$, $V_{OUT} = 5\text{V}$, $L = 3.3\mu\text{H}$ (DCR = $5.2\text{m}\Omega$), $EN = \text{floating}$, $f_{SW} = 540\text{kHz}$, and $C_{OUT} = 22\mu\text{F} \times 2$, unless otherwise noted.



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$T_A = +25^\circ\text{C}$, $V_{IN} = 12\text{V}$, $V_{OUT} = 5\text{V}$, $L = 3.3\mu\text{H}$ (DCR = $5.2\text{m}\Omega$), EN = floating, $f_{SW} = 540\text{kHz}$, and $C_{OUT} = 22\mu\text{F} \times 2$, unless otherwise noted.



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$T_A = +25^\circ\text{C}$, $V_{IN} = 12\text{V}$, $V_{OUT} = 5\text{V}$, $L = 3.3\mu\text{H}$ (DCR = $5.2\text{m}\Omega$), EN = floating, $f_{SW} = 540\text{kHz}$, and $C_{OUT} = 22\mu\text{F} \times 2$, unless otherwise noted.

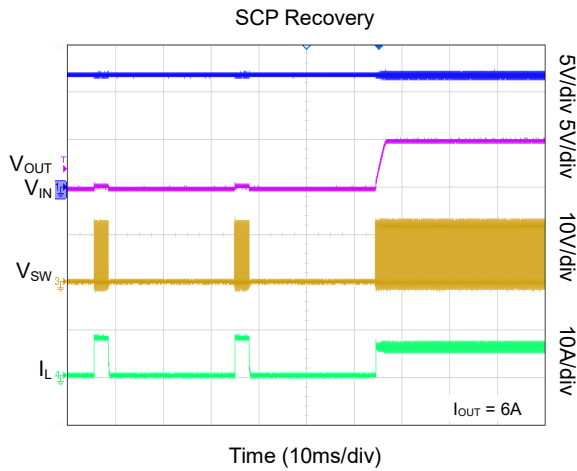
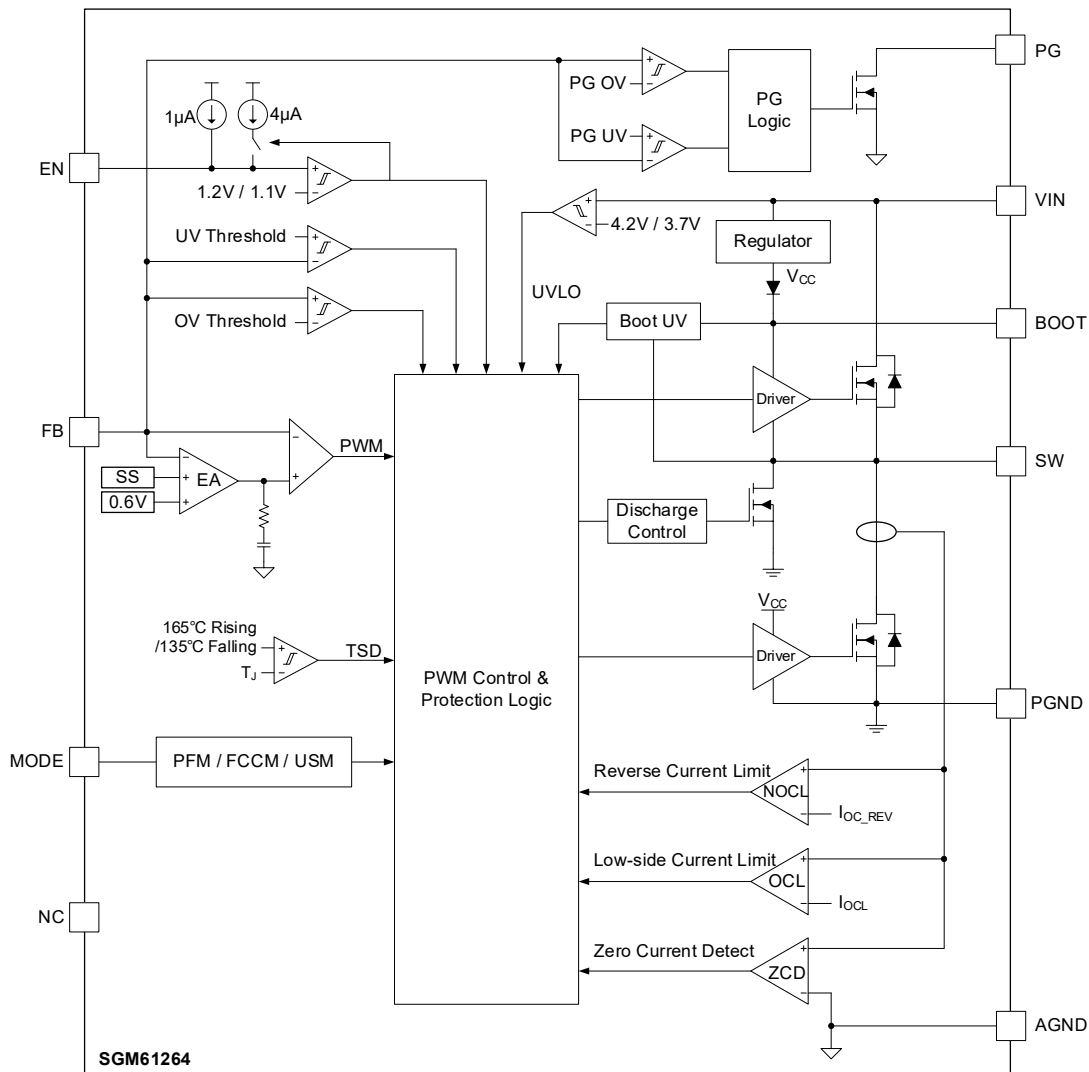
**FUNCTIONAL BLOCK DIAGRAM**

Figure 2. Block Diagram

DETAILED DESCRIPTION

Overview

The SGM61264 is a 28V synchronous Buck converter with 6A continuous output current capability, it can provide adjustable output voltage in range of 0.6V to 13V. It adopts adaptive constant on-time (ACOT) control, enabling fast transient response and precise feedback voltage without the external compensation components.

The ACOT control achieves seamless switching between CCM under heavy load conditions and DCM under light load conditions. The operating mode at light load can be selected via the external MODE pin. PFM mode can improve the efficiency under light load. FCCM mode can decrease the output ripple and maintain fixed switching frequency. USM mode can eliminate audible noise at light load.

The SGM61264 supports ultra-low ESR ceramic capacitors. It can use small-size MLCCs to achieve a compact layout, effectively reducing PCB area, simplifying routing, and lowering parasitic inductance.

Feature Description

UVLO

The SGM61264 implements internal under-voltage lockout (UVLO) circuitry on the VIN pin. It can operate above the VIN rising UVLO threshold (4.2V TYP). If falls below the falling UVLO voltage, the device will stop switching. If the EN pin is pulled high or floating and VIN exceeds the rising UVLO threshold, the device will start up with a soft-start.

Enable and Adjusting Under-Voltage Lockout

The EN pin control the power on/off of the device. The device will enable, if the EN pin voltage exceeds the enable threshold voltage of 1.20V (TYP). The device will disable, if the EN voltage is externally pulled low or the VIN pin voltage falls below its UVLO threshold.

The EN pin has an internal current source pull-up that keeps the EN pin voltage at high state by default, it allows the user to leave the pin floating to enable the device. If the EN pin is pulled low externally, the SGM61264 will enter standby mode with a typical shutdown current of 3.5μA.

If an application requires a higher VIN UVLO threshold, an external VIN UVLO adjustment circuit is recommended in Figure 3. The hysteresis is preferably higher than 500mV if the external VIN UVLO function is used.

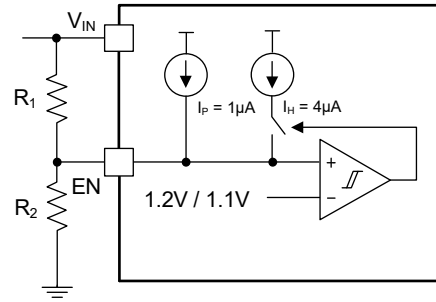


Figure 3. Adjustable VIN Under-Voltage Lockout

Figure 3 shows how UVLO and hysteresis are increased using R1 and R2. The EN pin has a pull-up current of 1μA. When EN pin voltage exceeds VEN_ON (1.2V TYP), a 4μA additional current is injected to the divider to provide hysteresis, and it will be removed when EN pin voltage is below VEN_OFF (1.1V TYP).

Use Equation 1 and 2 to calculate the values of R1 and R2 for a specified UVLO threshold. VSTART is the input start (turn-on) threshold voltage and VSTOP is the input stop (turn-off) threshold voltage. VEN_HYS is the hysteresis of VEN_ON and VEN_OFF. The VEN voltage can be calculated by Equation 3 and it must be lower than 5.5V with VIN (MAX).

$$R_1 = \frac{(V_{START} - V_{STOP}) - V_{EN_HYS} \times \frac{V_{START}}{V_{EN_ON}}}{I_H + V_{EN_HYS} \times \frac{I_P}{V_{EN_ON}}} \quad (1)$$

$$R_2 = \frac{V_{EN_ON}}{I_P + \frac{V_{START} - V_{EN_ON}}{R_1}} \quad (2)$$

$$V_{EN} = \frac{R_2 \times V_{IN} + R_1 \times R_2 \times (I_P + I_H)}{R_1 + R_2} \quad (3)$$

Soft-Start and Pre-Biased Soft-Start

The SGM61264 integrates an internal 2ms soft-start (SS) function to control the output voltage ramp rate during power up. It makes the output voltage rise up smoothly and avoids excessive over-current.

When EN pin enables the device to operate, the internal soft-start circuit voltage rises slowly from 0V to 0.6V and replaces the VREF during startup for the output voltage regulation. If a pre-bias voltage already exists on the output capacitor during startup, the device will not switch until the internal soft-start circuit voltage exceeds the feedback voltage VFB, it ensures a smooth rise of the converter to the regulation point.

DETAILED DESCRIPTION (continued)

The Adaptive On-Time Control and PWM Operation

The SGM61264 features adaptive constant on-time (ACOT) pulse width modulation (PWM) controller. ACOT is a hysteretic mode control without clock signal. When the internal comparator senses that the FB voltage drops below the reference voltage, the switching cycle will start with a relative constant on-time pulse. The adaptive constant on-time control with an internal compensation circuit is able to dynamically adjust the on-time duration based on the input voltage and output voltage to realize quasi-fixed frequency. It maintains stability even at virtually no output ripple. The SGM61264 features an integrated error amplifier (EA) to avoid the average value of output voltage above the target voltage, ensure high output voltage accuracy. This control requires no external current sensing network or loop compensation.

When the FB voltage falls below the reference voltage, the internal on-timer is triggered, then the high-side MOSFET will turn on. As the on-time expires, the high-side will turn off. The on-time depends on the input voltage and output voltage which is proportional to V_{OUT} and inversely proportional to V_{IN} . The on-timer will reset at the next switching cycle. An internal ramp is added to reference voltage to simulate output ripple, so it enables to use both low-ESR and ceramic output capacitors.

Bootstrap Voltage

To drive the high-side MOSFET, a voltage higher than V_{IN} is needed. This voltage is provided via the bootstrap technique, which uses a $0.1\mu\text{F}$ bootstrap capacitor between the SW and BOOT pins, and an internal bootstrap diode to derive power. The bootstrap capacitor is refreshed when the high-side MOSFET is off and the low-side MOSFET conducts.

When the bootstrap voltage falls below the UVLO threshold, the high-side switch is turned off, and the low-side switch is turned on to recharge the BOOT capacitor. After the recharge, the high-side switch is turned on again to regulate the output.

It is recommended to use X5R or X7R ceramic capacitors for the bootstrap capacitor, and the capacitor must have a voltage rating of 10V or higher.

Mode Selection

The SGM61264 offers a MODE pin to choose different states of operations under light load condition. The operating mode is configured by the resistor R_{MODE} value between the MODE pin and AGND. If MODE pin is short to AGND or the $R_{MODE} \leq 10\text{k}\Omega$, SGM61264 works under PFM control scheme. If MODE pin is floating or the $R_{MODE} \geq 500\text{k}\Omega$, SGM61264 works under FCCM mode. If the value of R_{MODE} is between $100\text{k}\Omega$ and $150\text{k}\Omega$, SGM61264 works under USM mode.

Table 1. MODE Pin Settings

MODE Pin	Light Load Operation Mode
Short to AGND or $R_{MODE} \leq 10\text{k}\Omega$	PFM
$100\text{k}\Omega \leq R_{MODE} \leq 150\text{k}\Omega$	USM
Floating or $R_{MODE} \geq 500\text{k}\Omega$	FCCM

Figure 4 below shows the typical power-up sequence. Once the EN voltage exceeds the EN rising threshold, the internal VCC voltage increases. It takes about $100\mu\text{s}$ to cross the VCC UVLO, then the device will detect the MODE pin, it takes about $64\mu\text{s}$ to read and set the operating mode. After MODE detection, the operating mode is latched and will not change until V_{IN} or EN restart. Then after a delay of around $650\mu\text{s}$, the soft-start function begins to ramp up the reference voltage to the PWM comparator. And then the PG will be pulled up if the PG pin is connected to external VCC.

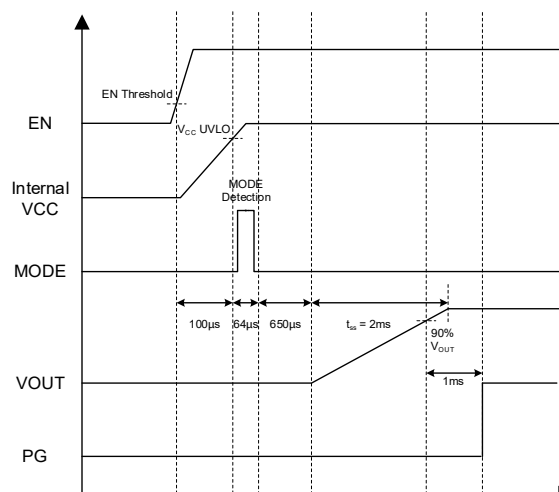


Figure 4. Power-Up Sequence

DETAILED DESCRIPTION (continued)

PFM Control Scheme

When MODE pin is short to AGND or the $R_{MODE} \leq 10k\Omega$, the SGM61264 is set to PFM control scheme to maintain high light load efficiency. Under light load condition, the on-time is still determined by the input voltage and output voltage. After the high-side MOSFET is turned on once, the output voltage rises during a switching cycle, it takes a longer time to discharge the output capacitor to the reference voltage level, resulting in fewer switching actions and a lower operating frequency. If the SGM61264 works at PFM and the load current is ultra-light, the switch remains inactive for a long time, it will enter sleep mode that some internal circuits are disabled to further improve light load efficiency.

At light load, once the inductor current drops to zero is detected, the low-side MOSFET is turned off. The power switches remain off for an extended period, and the converter operates in discontinuous conduction mode (DCM). As the load current increases, the inductor current rises accordingly, and the switching frequency increases as well. The point at which the valley of the inductor current ripple touches zero is the boundary between discontinuous conduction mode (DCM) and continuous conduction mode (CCM). The load current corresponding to this boundary point can be calculated by Equation 4.

$$I_{OUT(LL)} = \frac{1}{2L \times f_{SW}} \times \frac{(V_{IN} - V_{OUT})V_{OUT}}{V_{IN}} \quad (4)$$

USM Control Scheme

When MODE pin is connected to AGND through a resistor with a value between $100k\Omega$ and $150k\Omega$, the SGM61264 is set to USM control scheme to eliminate audible noise in light load. In PFM mode, the low switching frequency under light load conditions generates audible noise. The ultra-sonic mode (USM) fixes this by maintaining a minimum switching frequency of 33kHz. In USM mode, the low-side switch is forced to open for discharging the output capacitor during light load. The high-side switch is turned on again when the feedback voltage hits the reference voltage. This rendering the noise inaudible to humans. Compared to PFM mode, USM exhibits lower efficiency due to increased switching.

FCCM Control Scheme

When MODE pin is floating or the $R_{MODE} \geq 500k\Omega$, the SGM61264 is set to operate in forced continuous conduction mode (FCCM) in light load conditions. In FCCM mode, the low-side MOSFET is forced to conduct continuously, allowing the inductor current to become negative. The switching frequency is maintained at a quasi-fixed level over the entire load range, resulting in low output voltage ripple. Due to the continuous conduction of the low-side MOSFET and high switching frequency, the light load efficiency is lower than that in PFM and USM modes. However, this mode can avoid audible noise.

Power Good

The SGM61264 features a power good (PG) pin to indicate whether the output voltage is at the desired level. This pin is an open-drain output that requires a resistor pulled up to a DC voltage (not exceeds 5.5V). It is recommended to use a $100k\Omega$ pull-up resistor connected to 5V. An internal 1.6mA sink current ensures a valid logic low level. As shown in Figure 5, when the FB voltage is within the 90% and 110% of the reference voltage (V_{REF}), the internal open-drain switch is turned off and the PG pin is pulled up to high. When the FB voltage is outside the power-good range, or in events of thermal shutdown, EN shutdown, UVLO conditions, the internal open-drain switch is turned on and the PG pin is pulled down to low. The PG pin can only be held low as long as V_{IN} is continuously present.

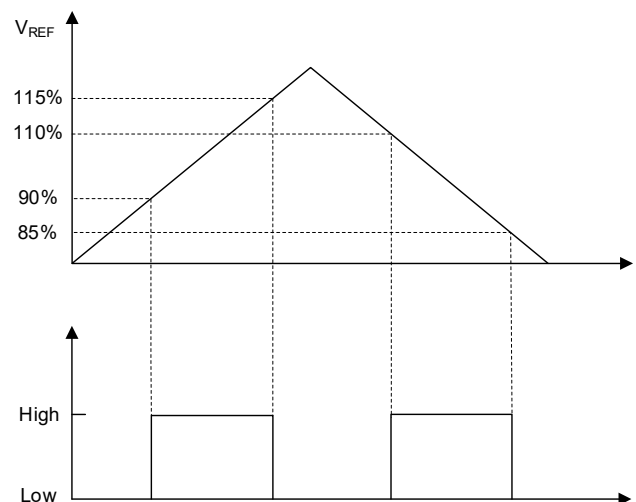


Figure 5. Power Good Flag

DETAILED DESCRIPTION (continued)**Output Over-Current Limit and Under-Voltage Protection**

Cycle-by-cycle valley current detect control circuit is used to realized output over-current limit (OCL). The switching current is monitored during off state by measuring the low-side MOSFET drain to source voltage. This voltage is proportional to the switching current, and temperature compensation is applied to improve sensing accuracy.

During the on-time of the high-side MOSFET, the inductor current rises linearly, with the slope determined by the input voltage, output voltage, and inductance. During the on-time of the low-side MOSFET, the inductor current falls linearly, with the slope determined by the output voltage and inductance. If the on-timer clock is ready and the inductor current exceeds the over-current limit (OCL) threshold during the off-time, the low-side MOSFET remains on until the current drops to or below the OCL threshold, at which point a new on-time pulse is generated.

When the device keeps in cycle-by-cycle limit to obtain the system's power request, the OCL is triggered and the current is being limited. As the load increases continuously, the output voltage decreases. If SS is ready and the FB voltage drops to 65% of V_{REF} , the UVP comparator detects it and shuts down the device after a deglitch wait time of 0.25ms and then re-starts after the hiccup time of 25ms. If over-current or a short-circuit fault condition still exists, the hiccup mode

will repeat until the fault condition is removed. Hiccup mode can help to reduce power dissipation and prevent overheating and potential damage to the device.

Over-Voltage Protection

If V_{FB} exceeds 125% of the V_{REF} threshold, the high-side switch will turn off after a deglitch time of 256 μ s. The low-side switch will turn off when the inductor current crosses zero for PFM. The low-side switch turns off when the inductor current hits the negative current limit for FCCM. Then the output will be discharged. When it returns below 121.5% of the V_{REF} , the discharge path will still be on for a hiccup time of 25ms and then the device will re-soft-start to recover the output voltage.

Output Voltage Discharge

The SGM61264 integrates a discharge MOSFET with $R_{DIS} = 192\Omega$ between the SW pin and PGND. This MOSFET turns on to discharge the output voltage when the device shuts down due to UVP, OVP, OTP or EN disable conditions. Due to the limited current capability of the MOSFET, the discharge is relatively slow.

Thermal Shutdown

If the junction temperature (T_J) exceeds +165°C (TYP), the device goes into thermal shutdown. The device will stop switching to protect the device from overheating, and the discharge path is turned on. When T_J decreases below the threshold of 135°C, the device will soft-start and resume normal operation.

APPLICATION INFORMATION

Typical Application

The design method and component selection are explained in this section. Figure 6 shows the typical schematic of SGM61264. It is used for converting a 6V to 28V supply voltage to a lower 5V output voltage with a maximum output current of 6A.

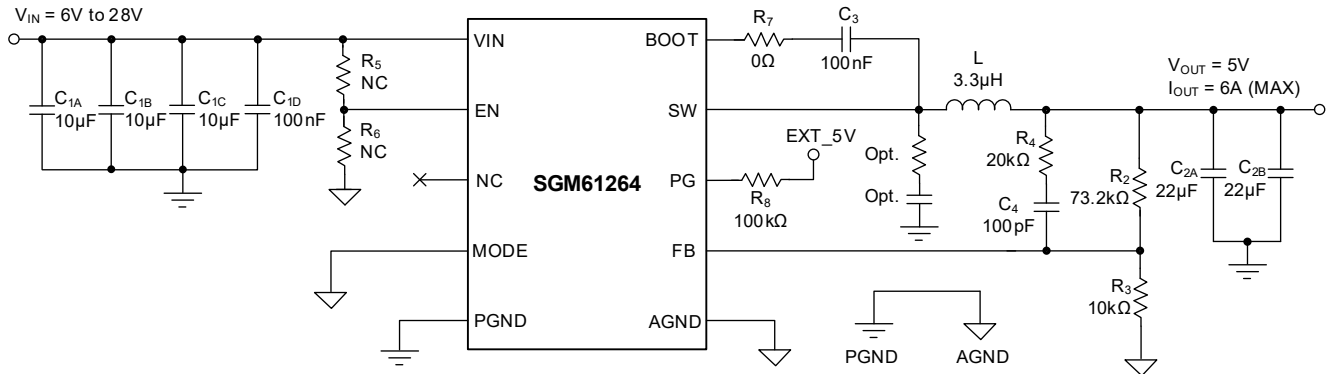


Figure 6. SGM61264 5V, 6A Reference Design

The external components are designed based on the application requirements and device stability. Some suitable output filters (L and C_{OUT}) along with C₄ and divider resistor values are provided in Table 2 to simplify component selection.

Table 2. Recommended Component Values

V _{OUT} (V)	L (μH)	C _{2A} + C _{2B} ⁽¹⁾ (μF)	R ₂ (kΩ)	R ₃ (kΩ)	R ₄ ⁽²⁾ (kΩ)	C ₄ ⁽²⁾ (pF)
0.6	1	47 × 2	0	—	—	—
1.2	1	47 × 2	10	10	—	—
3.3	2.2	22 × 2	45.3	10	20	100
5	3.3	22 × 2	73.2	10	20	100
13	5.6	22 × 2	206	10	20	100

NOTES:

- The output capacitance values specified herein are nominal ratings, not effective capacitances.
- R₄ and C₄ can be used to improve the load transient response or improve the loop-phase margin.

Design Requirements

The design parameters given in Table 3 are used for this design example.

Table 3. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUES
Input Voltage Range	24V nominal, 6V to 28V
Output Voltage	5V
Transient Response, 6A Load Step	ΔV _{OUT} = ±5%
Output Ripple Voltage	< 30mV at CCM
Output Current Rating	6A
Operating Frequency	540kHz

Input Capacitor Selection

A high-quality ceramic capacitor (X5R or X7R or better dielectric grade) must be used for input decoupling of the SGM61264. In some applications, additional bulk capacitance may also be required for the V_{IN} input. SGMICRO recommends a ceramic capacitor over 10μF for the input capacitor. An additional small size 0.1μF ceramic capacitor (C_{1D}) right beside V_{IN} and PGND pins is recommended for high frequency filtering.

For this design, a ceramic capacitor with at least 50V voltage rating is required to support the maximum input voltage. Three 10μF/50V capacitors are selected for V_{IN} to cover all DC bias, thermal and aging de-ratings. The input capacitance determines the regulator input voltage ripple. Use 540kHz for f_{sw}. This ripple can be calculated from Equation 5.

$$\Delta V_{IN} = \frac{I_{OUT} \times D \times (1-D)}{C_{IN} \times f_{SW}} \quad (5)$$

The capacitor's ripple current rating must exceed the maximum input ripple current in the application, which can be calculated using Equation 6.

$$I_{CIN_RMS} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \frac{V_{IN} - V_{OUT}}{V_{IN}}} = I_{OUT} \times \sqrt{D \times (1-D)} \quad (6)$$

When the input power supply is located far from the chip circuit, it is recommended to add input bulk capacitance to ensure stability.

APPLICATION INFORMATION (continued)

Inductor Selection

The LC filter used as the output filter has double pole at:

$$f_p = \frac{1}{2\pi\sqrt{L \times C_{OUT}}} \quad (7)$$

Low-frequency gain is determined by the output set-point resistor divider network and the internal gain of the device, with a phase of 180°. The ACOT control architecture introduces a high-frequency zero, reducing the gain attenuation rate to -20dB per decade and boosting the phase to 90 degrees at one decade above the zero frequency.

To ensure system stability, the inductor and capacitor of the output filter must be properly selected. The double-pole frequency defined by Equation 7 should be lower than the high-frequency zero and close enough to it, so that the phase boost from the high-frequency zero can provide sufficient phase margin for the circuit.

Equation 8, Equation 9, and Equation 10 are used to calculate the inductor's peak-to-peak ripple current, peak current, and RMS current, respectively. To ensure reliable operation, the inductor must have a saturation current rating exceeding the calculated peak current, as well as an RMS (heating) current rating that is higher than the calculated RMS current.

Use 540kHz for f_{SW} . The selected inductor must be able to withstand the peak current calculated by Equation 9 and the RMS current calculated by Equation 10, with sufficient margin.

$$\Delta I_L = \frac{V_{OUT}}{V_{IN}} \times \frac{V_{IN} - V_{OUT}}{L \times f_{SW}} \quad (8)$$

$$I_{L_PEAK} = I_{OUT} + \frac{\Delta I_L}{2} \quad (9)$$

$$I_{L_RMS} = \sqrt{I_{OUT}^2 + \frac{\Delta I_L^2}{12}} \quad (10)$$

Note that during startup, load transients or fault conditions, the peak inductor current may exceed the calculated I_{L_PEAK} . Therefore, it is always safer to choose the inductor saturation current higher than the switch current limit.

Output Capacitor Selection

The output voltage ripple is determined by the capacitance and its ESR. The voltage rating of the output capacitors should be selected with enough margins to ensure that capacitance drop (voltage and temperature de-rating) is not significant.

SGM61264 is designed for use with ceramic or other low-ESR capacitors, the ESR and ESL are virtually zero, so the output voltage ripple will be dominated by the following Equation 11.

$$\Delta V_{OUT} = \frac{\Delta I_L}{8 \times f_{SW} \times C_{OUT}} \quad (11)$$

The C_{OUT} is recommended values ranging from 20μF to 100μF for ceramic output capacitors. To reduce the voltage ripple, using parallel capacitors can help reduce the output ripple in a design using electrolytic output capacitors. Use Equation 12 to calculate the required RMS current rating for the output capacitor.

$$I_{CO_RMS} = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{\sqrt{12} \times V_{IN} \times L \times f_{SW}} \quad (12)$$

Bootstrap Capacitor Selection

SGMICRO recommends to use a 0.1μF high-quality ceramic capacitor (X7R or X5R) with 10V or higher voltage rating between BOOT and SW for the bootstrap capacitor.

Divider Resistors Selection

The output voltage is set with a resistor divider from the output node to the VFB pin. SGMICRO recommends using 1% tolerance or better divider resistors. Start by using Equation 13 to calculate V_{OUT} .

To improve efficiency under ultra-light load conditions, it is recommended to use voltage-dividing resistors with higher resistance values. However, excessively high resistance will degrade the device's noise immunity and significantly increase voltage errors caused by the V_{FB} input current. Please note that dynamically adjusting output voltage is not recommended.

$$V_{OUT} = 0.6 \times \left(1 + \frac{R_2}{R_3} \right) \quad (13)$$

APPLICATION INFORMATION (continued)

Layout Guidelines

1. A four-layer PCB is recommended to provide excellent thermal performance, effective noise shielding, and low impedance for power and ground paths.
2. Use one of the mid-layers as ground plane for noise shielding and additional heat dissipation especially for heavy load applications.
3. Place C_{IN} and C_{OUT} as close to the device as possible to minimize trace impedance and connected on the top layer PGND pin/plane and PAD.
4. Place small size high frequency decoupling capacitors on input capacitors.
5. Wide V_{IN} and PGND traces help reduce impedance,

lower conduction loss, and improve heat dissipation, ensuring stable and reliable operation.

6. Keep the BOOT-SW voltage path as short as possible.
7. Use a short and wide path for routing the SW pin to minimize radiated emissions.
8. Keep the SW area minimal and away from sensitive signals like FB input.
9. Minimize FB trace length and keep both feedback resistors close to the FB pin. Place C_4 right beside R_2 .
10. Bring the V_{OUT} sense trace from the point where V_{OUT} accuracy is important.
11. PGND and AGND are connected at a single point.

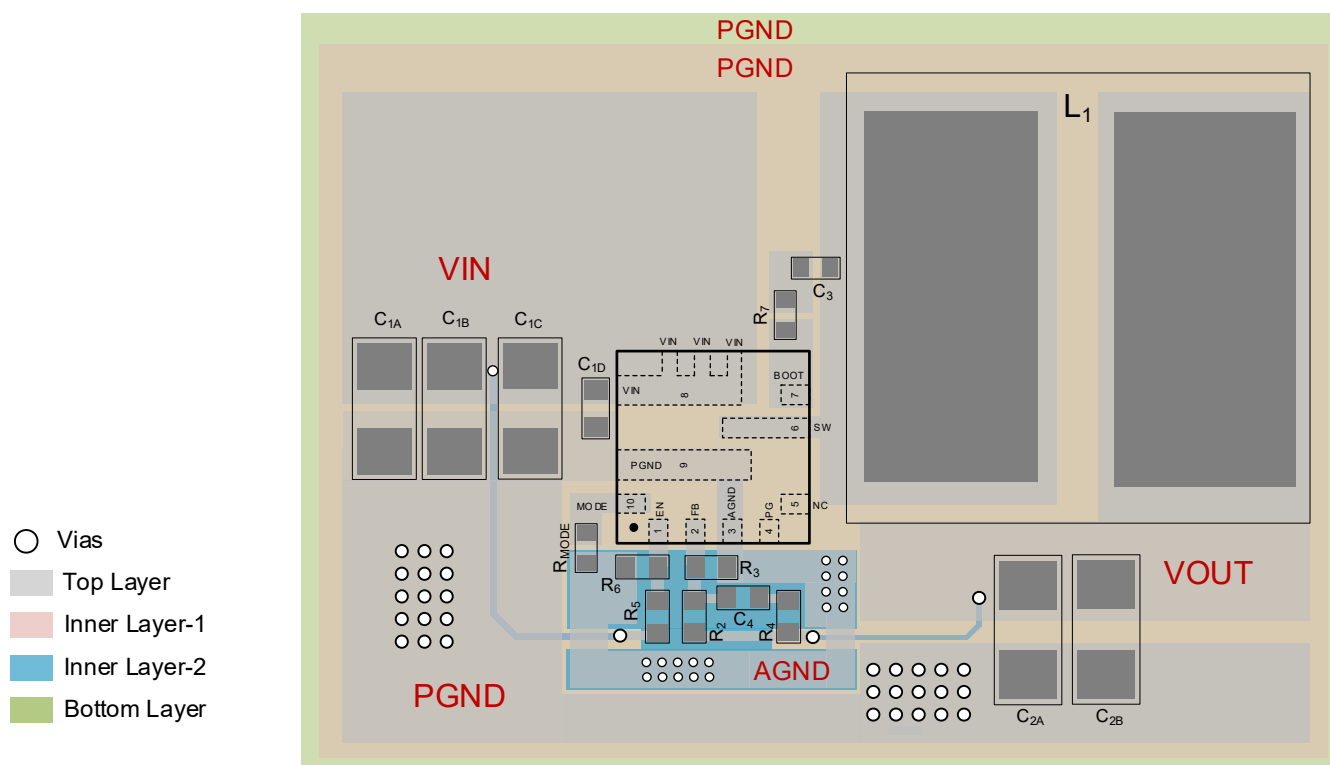


Figure 7. SGM61264 PCB Layout Example

REVISION HISTORY

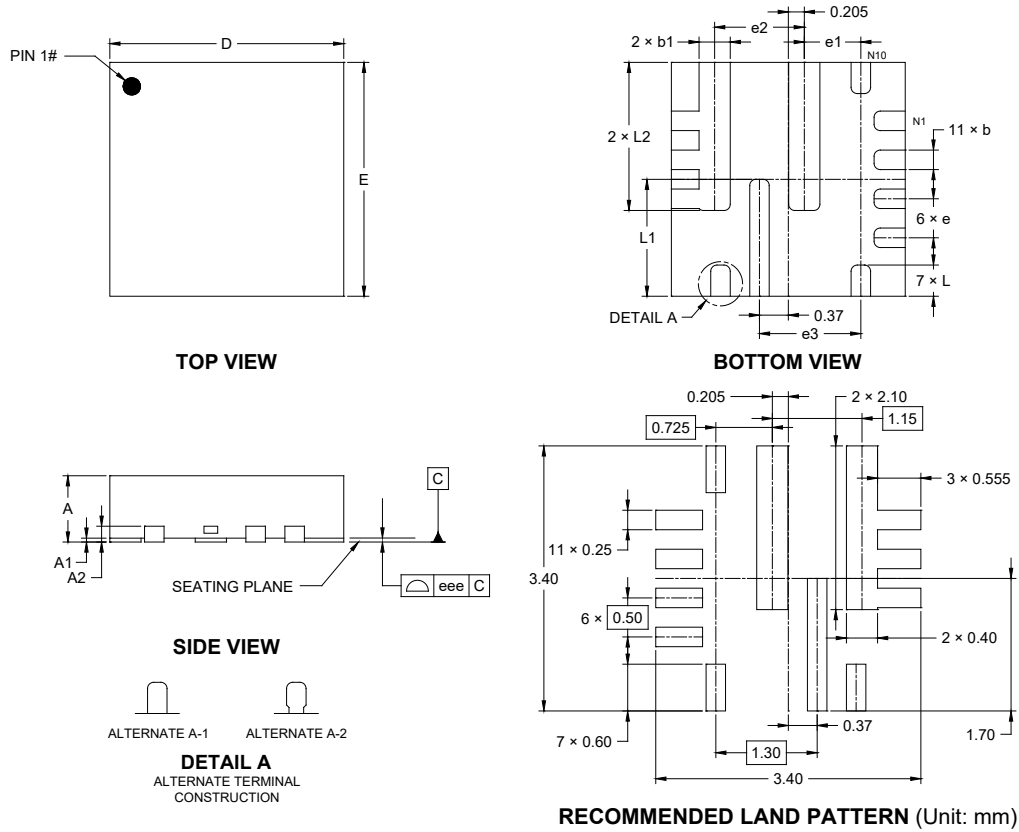
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original to REV.A (SEPTEMBER 2026)

Changes from Original to REV.A (SEPTEMBER 2026)	Page
Changed from product preview to production data.....	All

PACKAGE OUTLINE DIMENSIONS

TQFN-3×3-10L



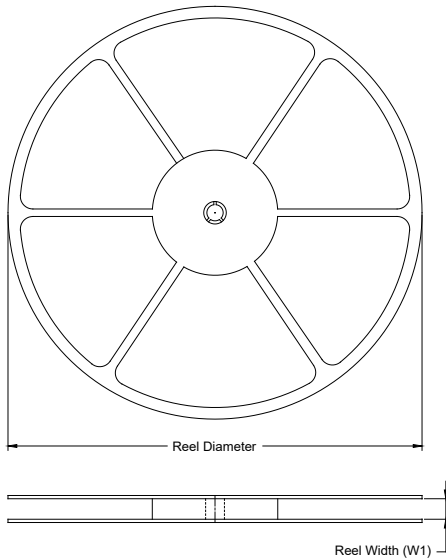
Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	0.800	-	0.900
A1	0.000	-	0.050
A2	0.203 REF		
b	0.200	-	0.300
b1	0.350	-	0.450
D	2.900	-	3.100
E	2.900	-	3.100
e	0.500 BSC		
e1	0.725 BSC		
e2	1.150 BSC		
e3	1.300 BSC		
L	0.300	-	0.500
L1	1.400	-	1.600
L2	1.800	-	2.000
eee	0.080		

NOTE: This drawing is subject to change without notice.

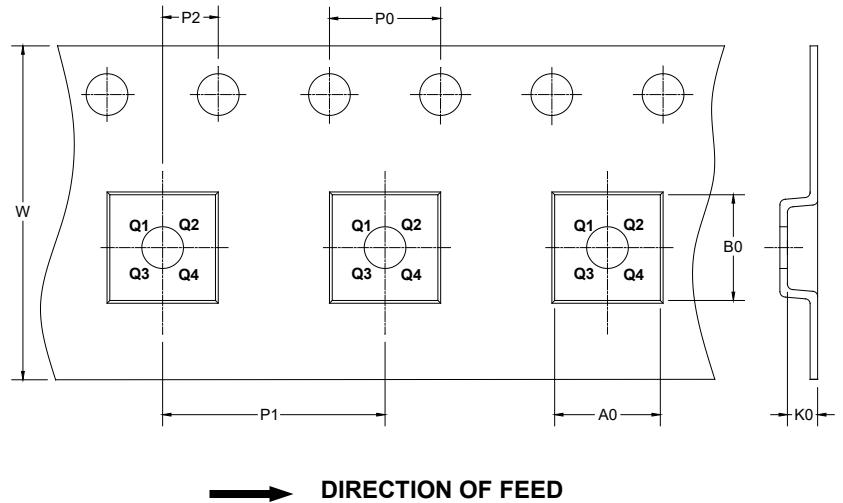
PACKAGE INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

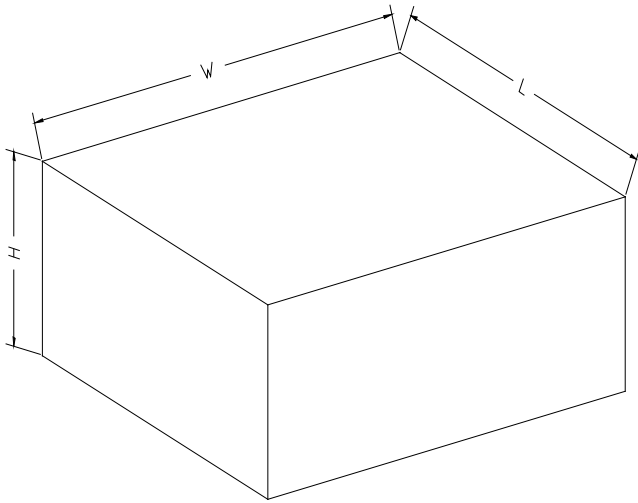
KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TQFN-3×3-10L	13	12.4	3.30	3.30	1.10	4.0	8.0	2.0	12.0	Q2

DD0001

PACKAGE INFORMATION

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13"	386	280	370	5

DD0002