TD24C256-C1
256-Kbit I²C Serial EEPROM 4-Ball WLCSP

GENERAL DESCRIPTION

The TD24C256-C1 is a 256-Kbit I²C-compatible serial EEPROM organized as 512 pages of 64 bytes each, totaling 32768 × 8 bits. The data integrity is improved with an embedded Error Correction Code (ECC) logic. The device is designed to operate in a supply voltage range of 1.7V to 5.5V, with a maximum of 1MHz transfer rate, over an operating temperature range of -40℃ to +105℃.

The TD24C256-C1 offers an additional 8-bit Chip Enable register for the Device Address Configuration (DAC) and Software Write Protection (SWP) feature. The device address is configurable through software, allowing up to eight devices on the bus at the same time. Write Protection of the whole memory array is software programmable by setting the SWP bit value. In order to protect this register from unexpected Write operation, the device allows the user to lock it in Read-only mode or unlock it by sending specific Write commands. The device also offers a separate memory block (in Read-only mode) containing a factory programmed 128-bit Unique ID.

The TD24C256-C1 is delivered in a WLCSP-0.65×1.11-4B package.

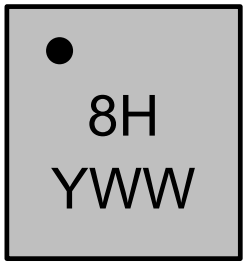
FEATURES

- **Supply Voltage Range: 1.7V to 5.5V**
- **2-Wire Serial Interface I²C Compatible**
  - **400kHz and High Speed 1MHz Transfer Rate Compatibility**
- **Byte and Page (up to 64 bytes) Write Mode**
  - **Partial Page Write Allowed**
- **Software Write Protection on the Whole Memory Array**
- **Software Programmable Device Address Configuration**
- **Additional 128-bit Unique ID**
- **Self-timed Write Cycle (3ms MAX)**
- **Schmitt Trigger, Filtered Inputs for Noise Suppression**
- **High Reliability**
  - **Endurance: 1,000,000 Write Cycles at T_A = +25℃**
  - **Data Retention: 100 Years at T_A = +25℃**
  - **ESD Protection (HBM): 6000V**
- **Low Operating Current**
  - **Write Current: 1mA (MAX)**
  - **Read Current: 0.5mA (MAX)**
  - **Standby Current: 1μA (MAX)**
- **Operating Temperature Range: -40℃ to +105℃**
- **RoHS Compliant and Halogen Free**
- **Available in a Green WLCSP-0.65×1.11-4B Package**

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
TD24C256-C1	WLCSP-0.65×1.11-4B	-40℃ to +105℃	TD24C256-C2LP1TR	8H YWW	Tape and Reel, 4000

MARKING INFORMATION



8H: TD24C256-C2LP1TR
YWW: Date Code, Y = year, WW = week
Example: 310 = year 2023, week 10

Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC} ..... -0.5V to 4V
Voltage on Input Pins, V_{IN} ..... -0.5V to 4V
Ambient Temperature with Power Applied ... -55℃ to +130℃
Storage Temperature Range ..... -65℃ to +150℃
ESD Susceptibility
HBM..... 6000V

RECOMMENDED OPERATING CONDITIONS

Operating Ambient Temperature Range..... -40℃ to +105℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

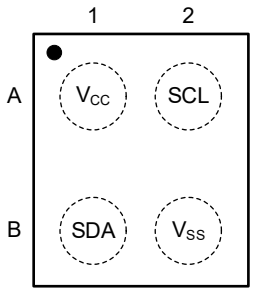
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

(TOP VIEW)



WLCSP-0.65×1.11-4B

PIN DESCRIPTION

NAME	TYPE	FUNCTION
SDA	Input/Output	Serial Data. The SDA pin is an open-drain bidirectional input/output pin used to serially transfer data to and from the device.
SCL	Input	Serial Clock. The SCL pin is used to provide a clock to the device and is used to control the flow of data to and from the device. Command and input data present on the SDA pin is always latched in on the rising edge of SCL, while output data on the SDA pin is always clocked out on the falling edge of SCL.
V_{CC}	Power	Device Power Supply. The V_{CC} pin is used to supply the source voltage to the device. Operations at invalid V_{CC} voltages may produce spurious results and should not be attempted.
V_{SS}	Ground	Ground. The ground reference for the power supply. GND should be connected to the system ground.

ELECTRICAL CHARACTERISTICS

DC Characteristics

(Operating range: T_A = -40℃ to +105℃, V_{CC} = 1.7V to 5.5V, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
Supply Voltage	V_{CC}		1.7	5.5	V
Supply Current (Read)	I_{CC1}	V_{CC} = 1.7V, Read at 1MHz		0.1	mA
		V_{CC} = 1.8V, Read at 400kHz		0.1	mA
		V_{CC} = 5.5V, Read at 400kHz		0.4	mA
		V_{CC} = 5.5V, Read at 1MHz		0.5	mA
Supply Current (Write)	I_{CC2}	V_{CC} = 1.8V, Write at 400kHz		0.4	mA
		V_{CC} = 5.5V, Write at 400kHz		1	mA
Standby Current	I_{SB}	V_{CC} = 1.7V, V_{IN} = V_{CC} or V_{SS}		0.5	μA
		V_{CC} = 5.5V, V_{IN} = V_{CC} or V_{SS}		1	μA
Input Leakage Current	I_{LI}	V_{IN} = V_{CC} or V_{SS}		1	μA
Output Leakage Current	I_{LO}	V_{OUT} = V_{CC} or V_{SS}		1	μA
Input Low-Level Voltage (SDA, SCL)	V_{IL}		-0.5	0.3 × V_{CC}	V
Input High-Level Voltage (SDA, SCL)	V_{IH}		0.7 × V_{CC}	V_{CC} + 0.5	V
Low-Level Output Voltage	V_{OL1}	V_{CC} > 2V, I_{OL}= 3mA		0.4	V
Low-Level Output Voltage	V_{OL2}	V_{CC} ≤ 2V, I_{OL}= 2mA		0.2	V

AC Characteristics

(Operating range: T_A = -40℃ to +105℃, V_{CC} = 1.7V to 5.5V, C_L = 100pF. Measurement conditions: input rise and fall time ≤ 50ns, input pulse voltages: 0.2 × V_{CC} to 0.8 × V_{CC}; input and output timing reference voltages: 0.3 × V_{CC} to 0.7 × V_{CC}, unless otherwise noted.)

PARAMETER	SYMBOL	FAST MODE V_{CC} = 1.7V to 5.5V		HIGH SPEED MODE V_{CC} = 1.7V to 5.5V		UNITS
		MIN	MAX	MIN	MAX	
Clock Frequency, SCL	f_{SCL}		400		1000	kHz
Clock Pulse Width Low	t_{LOW}	1300		600		ns
Clock Pulse Width High	t_{HIGH}	600		260		ns
SDA Rise Time	t_R (1)		300		300	ns
SDA (Out) Fall Time	t_F (1)		300		100	ns
Start Hold Time	$t_{HD.STA}$	600		250		ns
Start Setup Time	$t_{SU.STA}$	600		250		ns
Stop Setup Time	$t_{SU.STO}$	600		250		ns
Bus Free Time between Stop and Next Start	t_{BUF}	1300		500		ns
Data In Hold Time	$t_{HD.DI}$	0		0		ns
Data In Setup Time	$t_{SU.DAT}$	100		50		ns
Data Out Hold Time	$t_{HD.DAT}$	50		50		ns
SCL Low to Data Out Valid	t_{AA}	100	900	50	500	ns
Write Cycle Time	t_{WR}		3		3	ms
Noise Suppression Time	t_I		50		50	ns

NOTE: 1.This parameter is ensured by characterization only.

ELECTRICAL CHARACTERISTICS (continued)

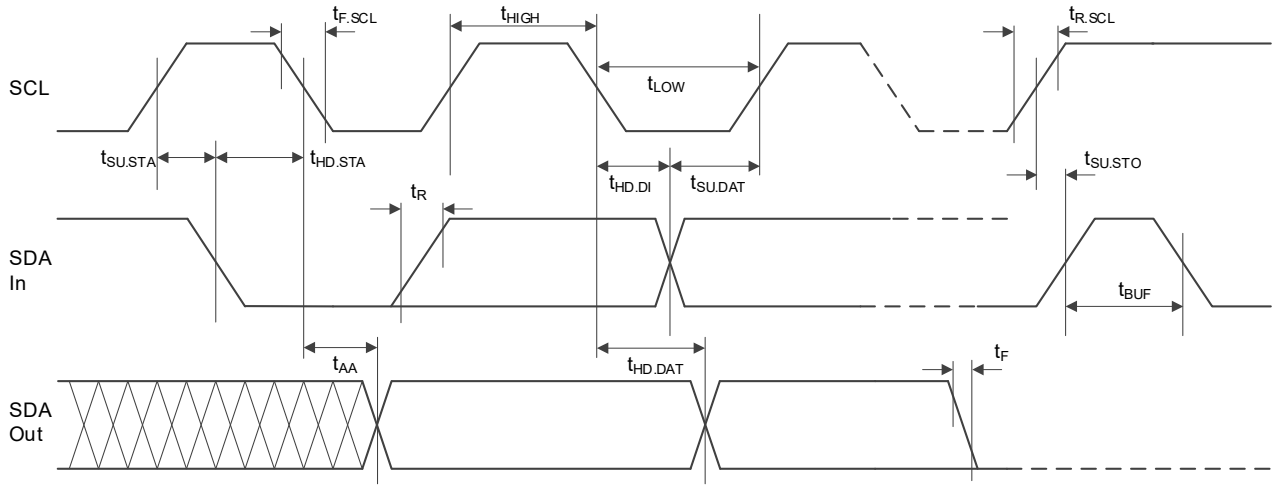


Figure 1. Bus Timing

Pin Capacitance

(Operating range for pin capacitance: T_A = +25℃, f_C = 1MHz, V_{CC} = 1.7V to 5.5V.)

PARAMETER (1)	SYMBOL	CONDITIONS	MAX	UNITS
Input/output Capacitance (SDA)	$C_{I/O}$	$V_{I/O}$ = 0V	8	pF
Input Capacitance (SCL)	C_{IN}	V_{IN} = 0V	6	pF

NOTE: 1. These parameters are ensured by characterization only.

Reliability Characteristics

PARAMETER	SYMBOL	CONDITIONS	MIN	UNITS
Write Cycle Endurance (1)	N_W	T_A = +25℃, Page mode	1×10^6	cycle
		T_A = +105℃, Page mode	1×10^5	
Data Retention	D_R	T_A = +25℃	100	year

NOTE: 1. The write cycle endurance is defined for group of four bytes located at addresses [4 × N, 4 × N + 1, 4 × N + 2, 4 × N + 3], where N is an integer. The Write cycle endurance is defined by characterization and qualification.

FUNCTIONAL BLOCK DIAGRAM

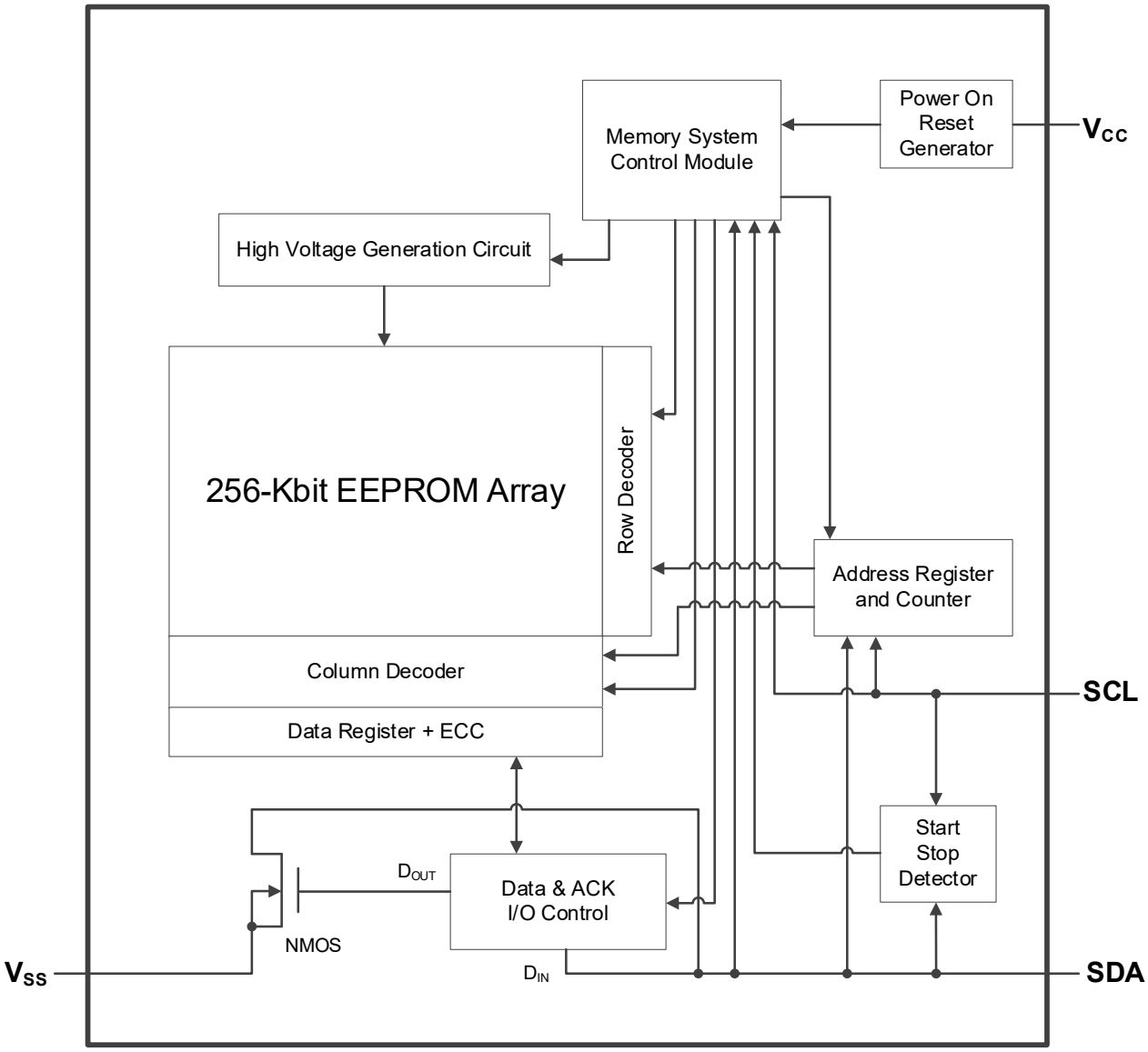


Figure 2. Block Diagram

FEATURES FOR WLCSP PACKAGE DEVICE

Chip Enable Register

As the TD24C256-C1 is delivered in 4-Ball WLCSP without Device Address inputs and Write Protection pin, the device provides a non-volatile 8-bit register, called Chip Enable register, allowing users to define a configurable device address by Device Address Configuration (DAC) feature and write-protect the whole memory array by Software Write Protection (SWP) feature. This register can be written and read with the device type identifier of '1010' at a specific word address. The description of the Chip Enable register is given in Table 1.

Table 1. Chip Enable Register (Address 111x_xxxx_xxxx_xxxxb)

REGISTER DATA BYTE							
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3 (2)	BIT 2 (2)	BIT 1 (2)	BIT 0
X (1)	X	X	X	Device Address Configuration E2 (bit 3), E1(bit 2), E0 (bit1)			Software Write Protect Activation 0: the whole memory can be written 1: the whole memory is write-protected

NOTES:

1. X = Bit is Don't Care.
2. Bits 3:1 Device Address Configuration:

(b3,b2,b1) = (0,0,0): the device address is 000 (factory default state).
(b3,b2,b1) = (0,0,1): the device address is 001.
(b3,b2,b1) = (0,1,0): the device address is 010.
(b3,b2,b1) = (0,1,1): the device address is 011.
(b3,b2,b1) = (1,0,0): the device address is 100.
(b3,b2,b1) = (1,0,1): the device address is 101.
(b3,b2,b1) = (1,1,0): the device address is 110.
(b3,b2,b1) = (1,1,1): the device address is 111.

Device Address Configuration

Bit 3, bit 2 and bit 1 define the device address bits E2, E1 and E0 in the Device Address Byte, respectively. These three bits can be written and reconfigured with a Write command (see ***Write Chip Enable Register*** section). Factory default state of the bit 3, bit 2 and bit 1 is Logic 0.

Note that the software device address bits (E2, E1 and E0) must match the corresponding address data (bit 3, bit 2 and bit 1). After the values of bit 3, bit 2 and bit 1 are reconfigured, the Master should send new device address bits for the subsequent instructions, otherwise the device responds with an NACK.

Software Write Protection

In order to prevent unwanted Write operations, the TD24C256-C1 offers a SWP bit (bit 0 in Chip Enable register), which makes it possible to protect the content in the whole 256-Kbit memory array. Updating the SWP bit to a new value is a reversible action with a Write command (see ***Write Chip Enable Register*** section). The SWP bit can be updated from 0 to 1 and from 1 to 0. Write operations are disabled (Read-only memory) when the SWP bit is set to Logic 1, while Write operations are enabled when the SWP bit is set to Logic 0. Upon a certain instruction send by the Master, the device will automatically load the last configuration of the SWP bit.

Write Protection on Chip Enable Register

In order to protect the Chip Enable register from unexpected Write operation, the TD24C256-C1 offers a feature for users to lock this register in Read-only mode or unlock it by sending specific Write commands (see ***Lock and Unlock Chip Enable Register*** section for details).

DEVICE COMMUNICATION

The TD24C256-C1 operates as a slave device and utilizes a 2-Wire serial interface to communicate with the Master. The Master initiates and controls all Read and Write operations to the slave devices on the serial bus, and both the Master and the slave devices can transmit and receive data on the bus.

The serial interface is comprised of just two signal lines: the Serial Clock (SCL) and the Serial Data (SDA). Data is always latched into the TD24C256-C1 on the rising edge of SCL and is always output from the device on the falling edge of SCL. Both the SCL pin and SDA pin incorporate integrated spike suppression filters and Schmitt Triggers to minimize the effects of input spikes and bus noise.

All command and data information is transferred with the Most Significant Bit (MSB) first. During the bus communication, one data bit is transmitted every clock cycle, and after eight bits of data has been transferred, the receiving device must respond with an acknowledge or a no-acknowledge response bit during a ninth clock cycle generated by the Master. Therefore, nine clock cycles are required for every one byte of data transferred. There is no unused clock cycle during any Read or Write operation, so there must not be any interruptions or breaks during the data stream.

During data transfers, data on the SDA pin must only change while SCL is low, and the data must remain stable while SCL is high. If data on the SDA pin changes while SCL is high, then either a Start or a Stop condition will occur. The number of data bytes transferred between a Start and a Stop condition is not limited and is determined by the Master.

Start Condition

A Start condition occurs when there is a high-to-low transition on the SDA pin while the SCL pin is stable in Logic 1 state. The Start condition must precede any command as the Master uses a Start condition to initiate any data transfer sequence (see Figure 3). The TD24C256-C1 will continuously monitor the SDA and SCL pins for a Start condition, and the device will not respond unless one is given.

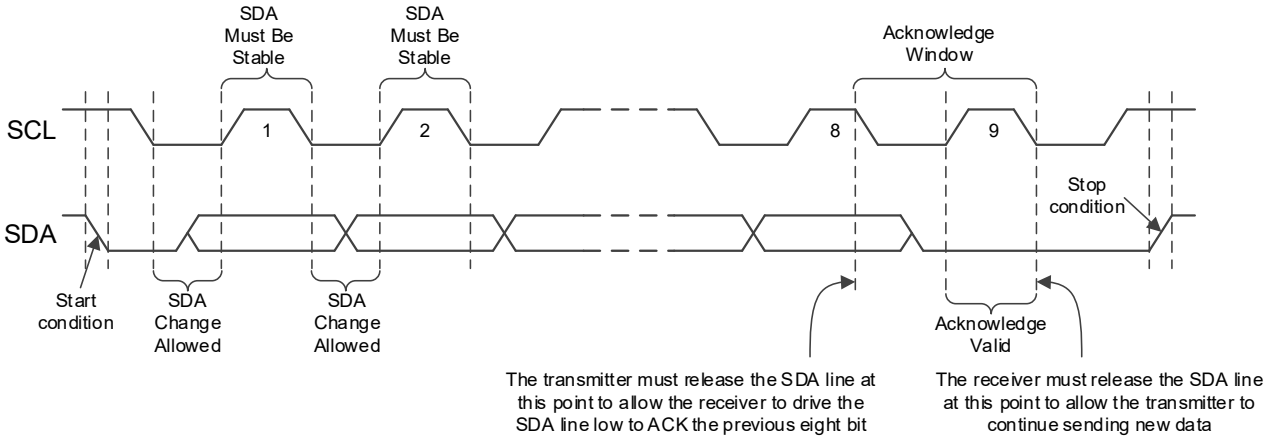


Figure 3. Start, Stop, and ACK

Stop Condition

A Stop condition occurs when there is a low-to-high transition on the SDA pin while the SCL pin is stable in Logic 1 state (see Figure 3). A stop condition terminates communication between the TD24C256-C1 and the Master. A Stop condition at the end of a Write command triggers the EEPROM internal write cycle. Otherwise, the TD24C256-C1 subsequently returns to Standby mode after receiving a Stop condition.

Acknowledge (ACK)

After each byte of data is received, the TD24C256-C1 should acknowledge to the Master that it has received the data byte successfully. This is accomplished by the Master first releasing the SDA line and providing the ACK/NACK clock cycle (a ninth clock cycle for every byte). During the ACK/NACK clock cycle, the TD24C256-C1 must output Logic 0 as ACK for the entire clock cycle so that the SDA line must be stable in Logic 0 state during the entire high period of the clock cycle (see Figure 3).

DEVICE COMMUNICATION (continued)

Standby Mode

The TD24C256-C1 features a low-power Standby mode which is enabled:

(1) Upon power-up;

(2) After the receipt of a Stop condition in Read operation;

(3) The completion of any internal operations.

Software Reset

After an interruption in protocol, power loss, or system reset, any 2-Wire part can be reset by following these steps: (1) Create a Start condition; (2) Clock nine cycles; (3) Create another Start condition followed by a Stop condition (see Figure 4).

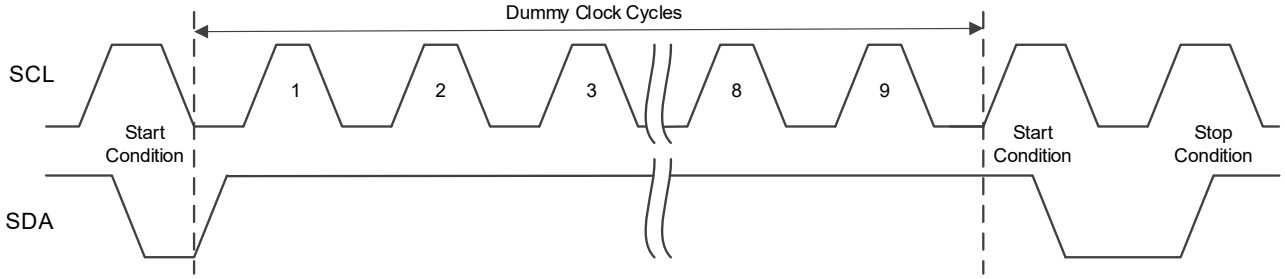


Figure 4. 2-Wire Software Reset

DEVICE COMMUNICATION (continued)

Device Reset and Initialization

The TD24C256-C1 incorporates a Power-On Reset (POR) circuit to prevent inadvertent operations during power-up. On a cold power-up, the device does not respond to any instructions until the supply voltage reaches the internal power-on reset threshold voltage (V_{POR}). The supply voltage must rise continuously between V_{POR} and V_{CC} (MIN) without any ring back to ensure a proper power-up. Once the supply voltage passes V_{POR}, the device is reset and enters Standby mode. However, no protocol should be issued to the device until a valid and stable supply voltage is applied for the time specified by the t_{INIT} parameter. The supply voltage must remain stable and valid until the end of the protocol transmission, and for a Write instruction, until the end of the internal write cycle (see Figure 5).

This POR behavior is bi-directional. It protects the TD24C256-C1 against brown-out failure caused by a temporary loss of power. In a similar way, as soon as the supply voltage drops below the internal brown-out reset threshold voltage (V_{BOR}), the device is reset and stops responding to any instructions. The V_{BOR} level is set below the V_{POR} level.

Parameters related to power-up and power-down conditions are listed in Table 2.

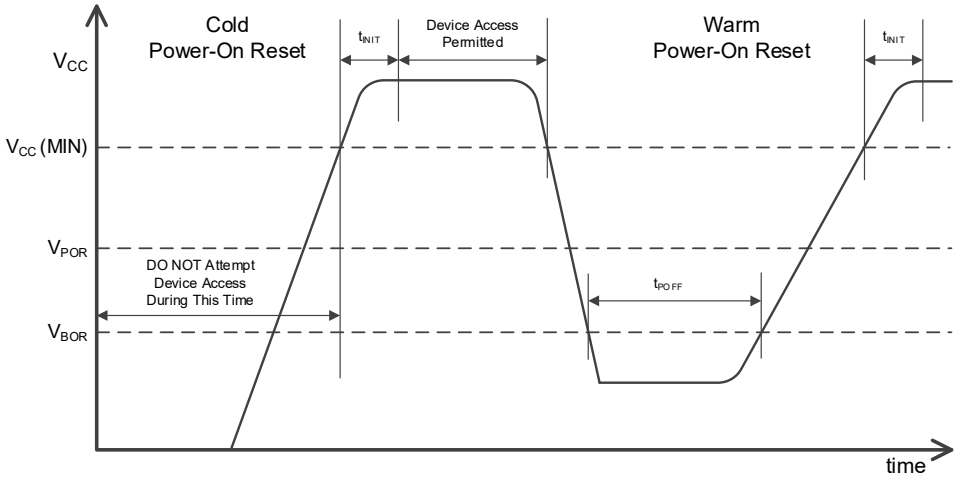


Figure 5. Power-Up and Power-Down Timing

Table 2. Power-Up and Power-Down Conditions

PARAMETER	SYMBOL	MIN	MAX	UNITS
Power-On Reset Voltage	V_{POR}		1.5	V
Brown-Out Reset Voltage	V_{BOR}	1.2		V
Time from V_{CC} (MIN) to First Command	t_{INIT}	100		μs
Warm Power Cycle Off Time	t_{POFF}	100		μs

Data Security

The TD24C256-C1 offers a Software Write Protection (SWP) feature that allows users to write protect the whole memory array when the internal non-volatile SWP bit is set to Logic 1 (see ***Software Write Protection*** section for details).

DEVICE ADDRESSING

The TD24C256-C1 requires a 7-bit device address and a Read/Write select bit following a Start condition from the Master to initiate communication with the serial EEPROM. The device address byte is comprised of a 4-bit device type identifier followed by three device address bits (E2, E1, and E0) and a R/W select bit and is clocked by the Master on the SDA pin with the most significant bit (bit 7) first.

The TD24C256-C1 will only respond to the device type identifier of '1010' to select the device 256-Kbit memory for normal Read or Write operation, or the Chip Enable register for Read or Write operation, or the Unique ID block (see Table 3).

Table 3. TD24C256-C1 Device Address Byte

FUNCTION	DEVICE TYPE IDENTIFIER				DEVICE ADDRESS			READ/WRITE
	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
When accessing the 256-Kbit memory array	1	0	1	0	E2	E1	E0	R/W
When accessing the Chip Enable register	1	0	1	0	E2	E1	E0	R/W
When lock/unlock the Chip Enable register	1	0	1	0	E2	E1	E0	0
When accessing the Unique ID	1	0	1	0	E2	E1	E0	1

The software device address bits (E2, E1 and E0) must match the corresponding device address data stored in the Chip Enable register, allowing up to eight devices on the bus at the same time. The eighth bit of the address byte is the R/W operation selection bit. A Read operation is selected if this bit is Logic 1, and a Write operation is selected if this bit is Logic 0. Upon a compare of the device address byte, the TD24C256-C1 outputs an ACK or an NACK during the ninth clock cycle if the compare is true or not true, respectively. The device will return to the low-power Standby mode after an NACK.

Once the TD24C256-C1 has acknowledged the device address byte, the device waits for the Master to send two word address bytes (first word address byte sent first, followed by the second word address byte) for a certain Read or Write instruction according to Table 4. The TD24C256-C1 responds to each address byte with an ACK.

Table 4. TD24C256-C1 Word Address Bits

FUNCTION	FIRST WORD ADDRESS BYTE								SECOND WORD ADDRESS BYTE							
	BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Random Read	0	A14 (1)	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Byte/Page Write	0	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Write Chip Enable Register	1	1	1	X (2)	X	X	X	X	X	X	X	X	X	X	X	X
Read Chip Enable Register	1	1	1	X	X	X	X	X	X	X	X	X	X	X	X	X
Lock Chip Enable Register	1	0	1	X	X	X	X	X	X	X	X	X	X	X	X	X
Unlock Chip Enable Register	1	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X
Read Unique ID	1	0	0	X	X	X	X	X	X	X	X	X	A3	A2	A1	A0

NOTES:

1. A = Significant address bit.

2. X = Bit is Don't Care.

READ AND WRITE OPERATIONS

Write Operations

Byte Write

For a Byte Write operation, the Master sends a Start condition followed by the device type identifier of '1010', the device address bits and the R/$\overline{W}$ select bit set to Logic 0. The TD24C256-C1 responds with an ACK during the ninth clock cycle and waits for the Master to send two word address bytes (first word address byte and second word address byte). Then the device responds to each word address byte with an ACK. After receiving ACKs from the device, the Master transmits one data byte. If the addressed location has been Write-protected, the device responds with an NACK, and the addressed location will not be modified. If the addressed location is not Write-protected, the device responds with an ACK. The Master ends the Byte Write sequence with a Stop condition during the 10th clock cycle to initiate the internally self-timed write cycle (see Figure 6). A Stop condition issued during any other clock cycle during the Write operation will not trigger the internal write cycle.

Once the write cycle begins, the preloaded data word will be programmed in the amount of time not to exceed the t_{WR} specification (see Figure 8). During the time, the Master should wait a fixed time by the t_{WR} specification, or for time sensitive applications, an ACK polling routine can be implemented. All inputs are ignored by the device during the write cycle and the device will not respond until the write cycle is completed. The serial EEPROM will increment its internal address counter each time a byte is written.

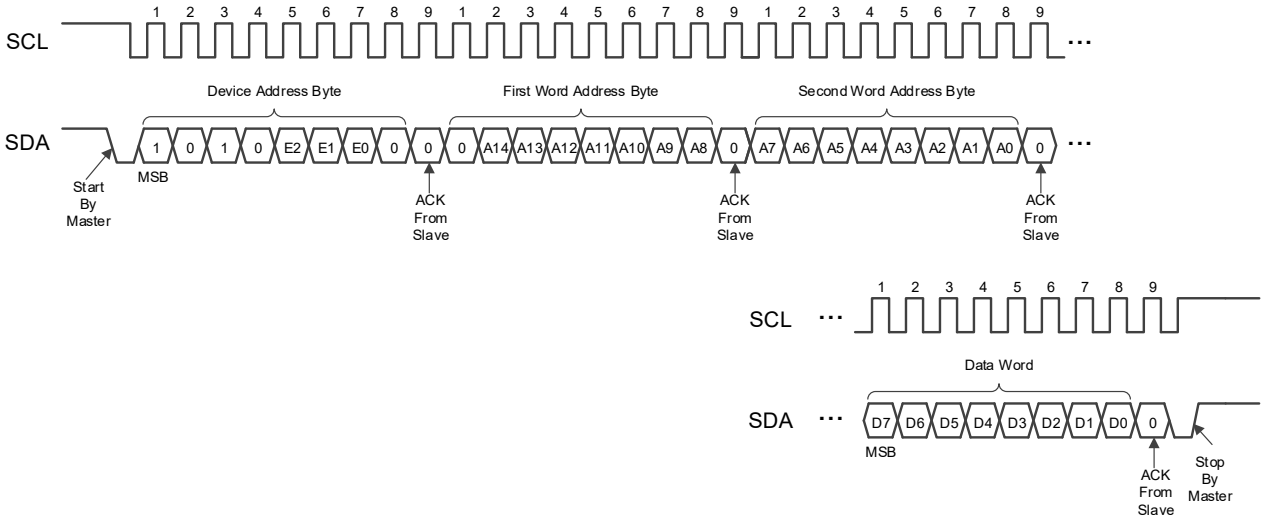


Figure 6. Byte Write

READ AND WRITE OPERATIONS (continued)

Page Write

The 256-Kbit serial EEPROM is capable of writing up to 64 data bytes at a time by executing the Page Write protocol sequence. A partial or full Page Write operation is initiated the same as a Byte Write operation except that the Master does not send a Stop condition after the first data word is clocked in. Instead, after the device has acknowledged to the first data word, the Master can transmit up to 63 more data words. The device responds with an ACK after each data word is received if the addressed locations are not Write-protected. If the addressed locations have been Write-protected by the SWP bit set to Logic 1, the device responds with an NACK to each data word and the addressed locations will not be modified. After the device acknowledges to the last data word, the Master should terminate the Page Write sequence with a Stop condition to start the internal write cycle (see Figure 7). A Stop condition issued at any other clock cycle will not initiate the internally self-timed write cycle and the Write sequence will have to be repeated again. Once the write cycle begins, the data words should be programmed in the amount of time not exceeding the t_{WR} specification (see Figure 8). During this time, the Master should wait a fixed time by the t_{WR} specification, or for time sensitive applications, an ACK polling routine can be implemented.

The lower six bits of the word address are internally incremented following the receipt of each data word. The higher word address bits are not incremented, retaining the memory page row location. When the internally generated word address reaches the page boundary, the following data word will be placed at the beginning of the same page. If more than sixty-four data words are transmitted to the device, the data word address will roll over and the previous data will be overwritten. The address roll-over during a Write sequence is from the last byte of the current page to the first byte of the same page.

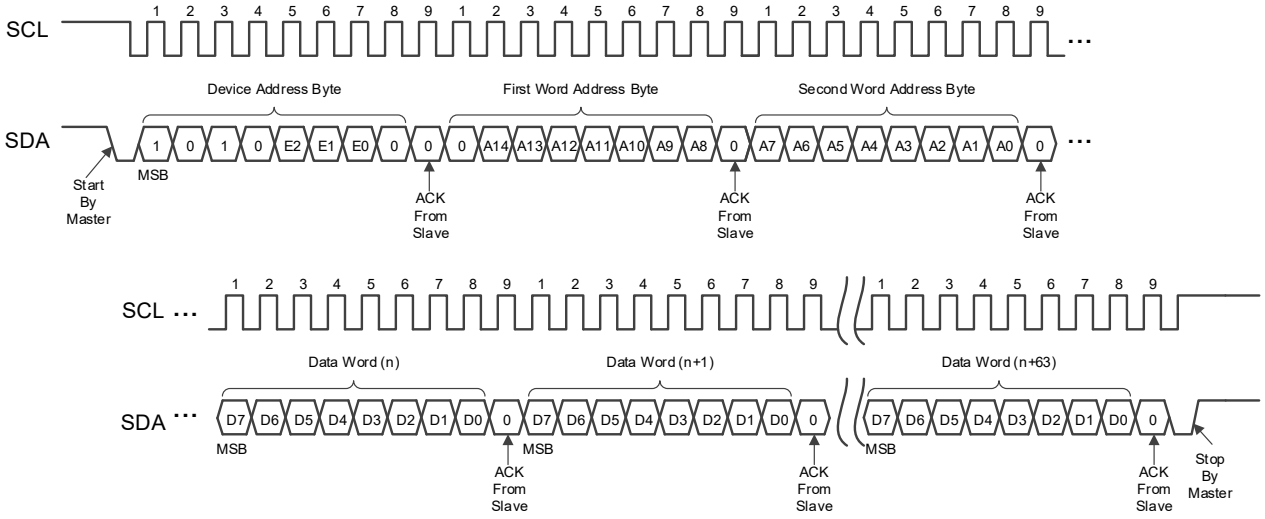


Figure 7. Page Write

READ AND WRITE OPERATIONS (continued)

Write Cycle Timing

The length of the self-timed write cycle, or t_{WR}, is defined as the amount of time from a valid Stop condition that begins the internal write sequence to the Start condition of the first device address byte sent to the TD24C256-C1 that it subsequently responds to with an ACK (see Figure 8).

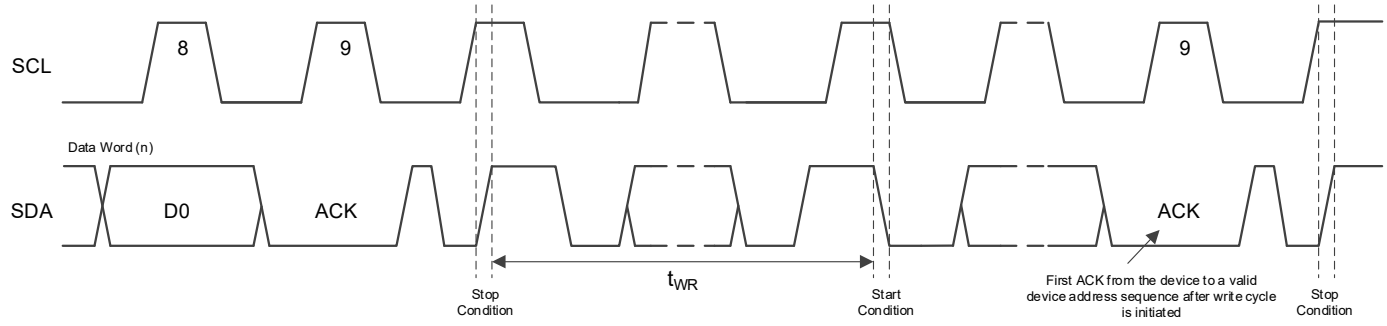


Figure 8. Write Cycle Timing

Error Correction Code (ECC) and Write Cycling

The Error Correction Code (ECC) is an internal logic function which is transparent for the I²C communication protocol.

The ECC logic is implemented on each group of four EEPROM bytes. A group of four bytes is located at addresses [4 × N, 4 × N + 1, 4 × N + 2, 4 × N + 3], where N is an integer. Inside a group, if a single bit out of the four bytes happens to be erroneous during a Read operation, the ECC detects this bit and replaces it with the correct value. The data reliability is therefore much improved.

Even if the ECC function is performed on groups of four bytes, a single byte can be written/cycled independently. In this case, the ECC function also writes/cycles the three other bytes located in the same group. As a consequence, the maximum cycling budget is defined at group level and the cycling can be distributed over the 4 bytes of the group: the sum of the cycles seen by byte 0, byte 1, byte 2 and byte 3 of the same group must remain below the maximum value defined in ***Reliability Characteristics*** section.

READ AND WRITE OPERATIONS (continued)

Acknowledge (ACK) Polling

An ACK polling routine can be implemented to optimize time sensitive applications that would not prefer to wait the fixed maximum write cycle time but would prefer to know immediately when the serial EEPROM write cycle has completed to start a subsequent operation. Once the internally self-timed write cycle has started, the device inputs are disabled and ACK polling can be initiated. An ACK polling routine involves sending a valid Start condition followed by the device address byte. While the write cycle is in progress, the device will not respond with an ACK, indicating the device is busy writing data. Once completed, the device returns an ACK and the next device operation can be started (see Figure 9).

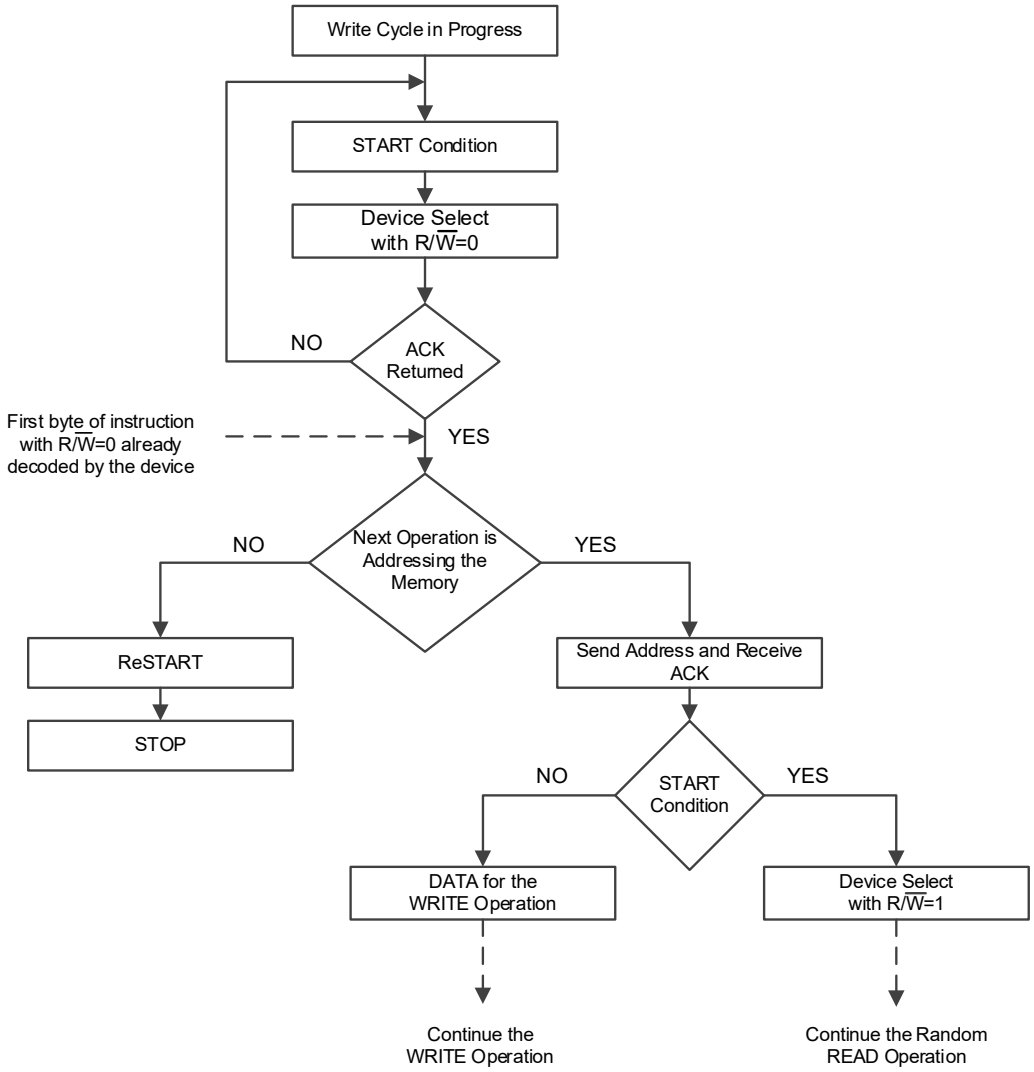


Figure 9. Acknowledge Polling Flow Chart

In case of writing Chip Enable register when E2, E1 and E0 are reconfigured, the device will return ACK only if:

- three device address bits of the Device Address Byte is equal to the new E2, E1 and E0 values;
- internal write cycle is completed (new E2, E1 and E0 values have been programmed in the Chip Enable register).

READ AND WRITE OPERATIONS (continued)

Write Chip Enable Register

The TD24C256-C1 provides a non-volatile 8-bit register for users to achieve Device Address Configuration (DAC) and Software Write Protection (SWP) feature. Writing in the Chip Enable register can be performed with a Byte Write instruction at address 111x_xxxx_xxxx_xxxxb (where 'x' is Don't Care), as shown in Figure 10. The data word byte is defined in Table 1.

Write Chip Enable register is performed independently of the state of SWP bit. Writing more than one byte will discard the write cycle and the content in the Chip Enable register will not be changed.

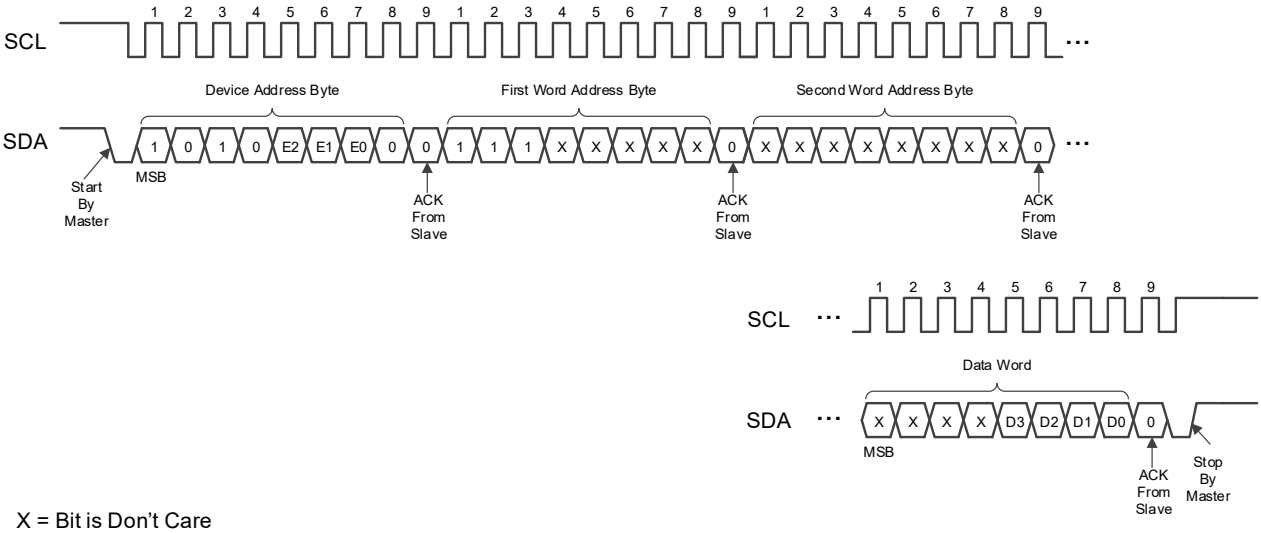


Figure 10. Write Chip Enable Register

Lock and Unlock Chip Enable Register

The Chip Enable register can be locked or unlocked via command. This feature provides more additional protection for the device. The Lock Chip Enable Register instruction locks the Chip Enable register in Read-only mode. This instruction is similar to Byte Write, except that:

- The word address bits A15:A13 must be '101' and other word address bits are Don't Care;
- The data byte must be equal to FFh (see Figure 11).

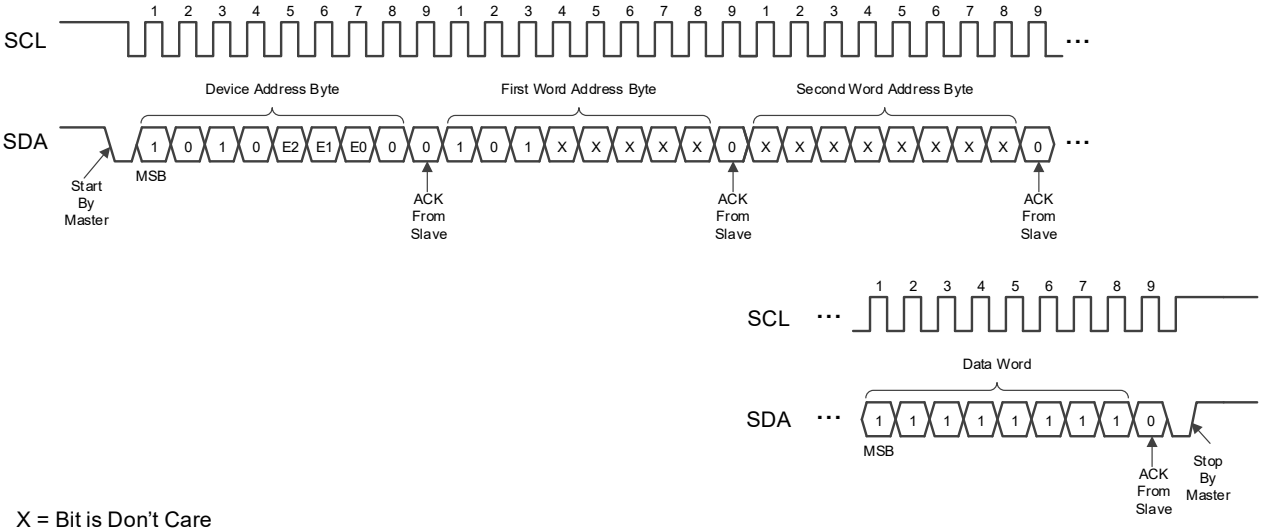


Figure 11. Lock Chip Enable Register

READ AND WRITE OPERATIONS (continued)

The Unlock Chip Enable Register instruction unlocks the Chip Enable register in write mode. This instruction is similar to Byte Write, except that:

- The word address bits A15:A13 must be '110' and other word address bits are Don't Care;
- The data byte must be equal to 00h (see Figure 12).

The factory default state of the Chip Enable register is unlocked.

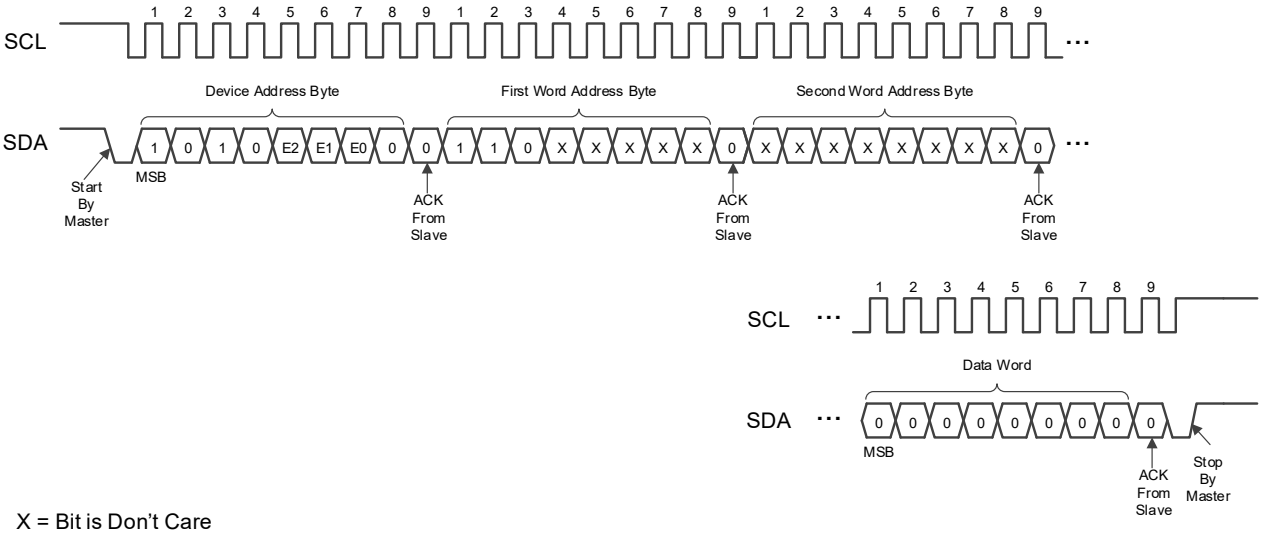


Figure 12. Unlock Chip Enable Register

READ AND WRITE OPERATIONS (continued)

Read Operations

All Read operations are initiated by the Master transmitting a Start condition, a device type identifier of '1010' or '1011', three software device address bits (E2, E1, E0) that match corresponding values in Chip Enable register, and the R/W select bit with Logic 1 state. In the following clock cycle, the TD24C256-C1 should respond with an ACK. The subsequent protocol depends on the type of Read operation desired. There are three Read operations for memory array: Current Address Read, Random Address Read, and Sequential Read with the device type identifier of '1010'; two Read operations for functional registers: Read Chip Enable register and Read Write Protection Status with the device type identifier of '1010'; three Read operations for Identification Page and Unique ID: Read Identification Page, Read the Lock Status, and Read Unique ID with the device type identifier of '1011'.

Current Address Read

For a Current Address Read operation, the Master sends a Start condition followed by transmitting the device address byte with the R/W bit set to Logic 1 (see Figure 13). The TD24C256-C1 should respond with an ACK and then serially transmits the data word addressed by the internal address counter. This address maintained by the internal address counter is the last address accessed during the last Read or Write operation. The counter is then incremented by one and the address will stay valid between operations as long as power to the device is supplied. The address roll-over during a Read operation is from the last byte of the last page to the first byte of the first page. To end the command, the Master responds with an NACK followed by a Stop condition.

Note that the address counter value is defined by instructions accessing the memory or the Chip Enable register or the ID Page or the Unique ID. For example, when accessing the ID Page, the counter value is loaded with the byte location in the ID Page. Therefore the next Current Address Read in the memory uses this new address counter value. When accessing the memory, it is recommended to always use the Random Read instruction (see ***Random Read*** section) instead of the Current Address Read instruction.

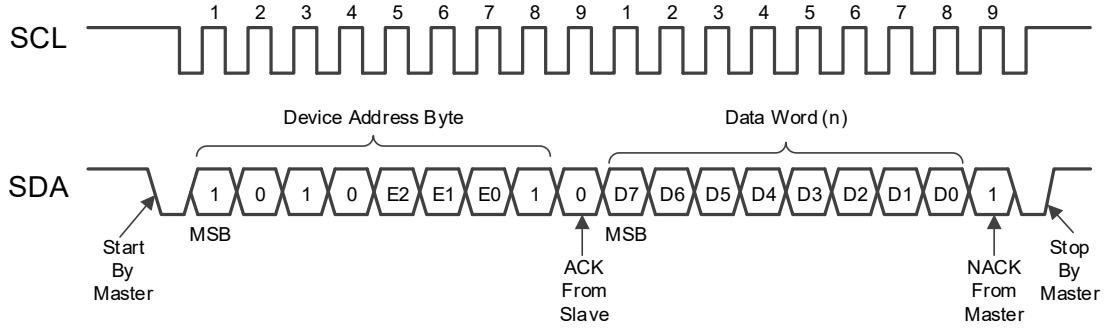


Figure 13. Current Address Read

READ AND WRITE OPERATIONS (continued)

Random Read

A Random Read operation allows the Master to access any memory location in a random manner and requires a dummy write sequence to preload the starting data word address. To perform a Random Read, the device address byte and the word address bytes are transmitted to the TD24C256-C1 as part of the dummy write sequence (see Figure 14). Once the device address byte and word address bytes are clocked in and acknowledged by the TD24C256-C1, the Master must generate another Start condition. The Master initiates a Current Address Read by sending another device address byte with the R/$\overline{W}$ bit set to Logic 1. The TD24C256-C1 responds with an ACK to the device address byte and serially clocks out the first data word and increments its internal address counter. The device will continue to transmit sequential data words as long as the Master continues to acknowledge each data word. To end the sequence, the Master responds with an NACK followed by a Stop condition.

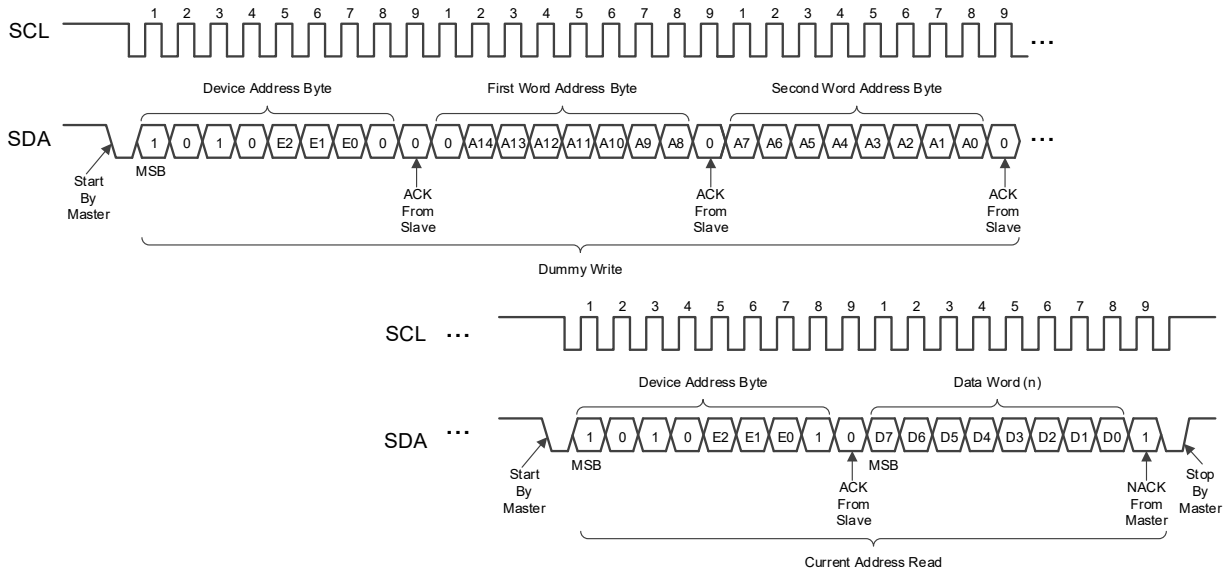


Figure 14. Random Read

Sequential Read

A Sequential Read operation is initiated in the same way as either a Current Address Read or a Random Read, except that after the TD24C256-C1 transmitting the first data word, the Master responds with an ACK instead of an NACK. As long as the TD24C256-C1 receives an ACK, it will continue to increment the data word address and serially clock out the sequential data words (see Figure 15). When the internal address counter is at the last byte of the last page, the word address will roll over to the beginning of the memory array and the Sequential Read operation will continue. The Sequential Read operation is terminated by the Master responding with an NACK followed by a Stop condition.

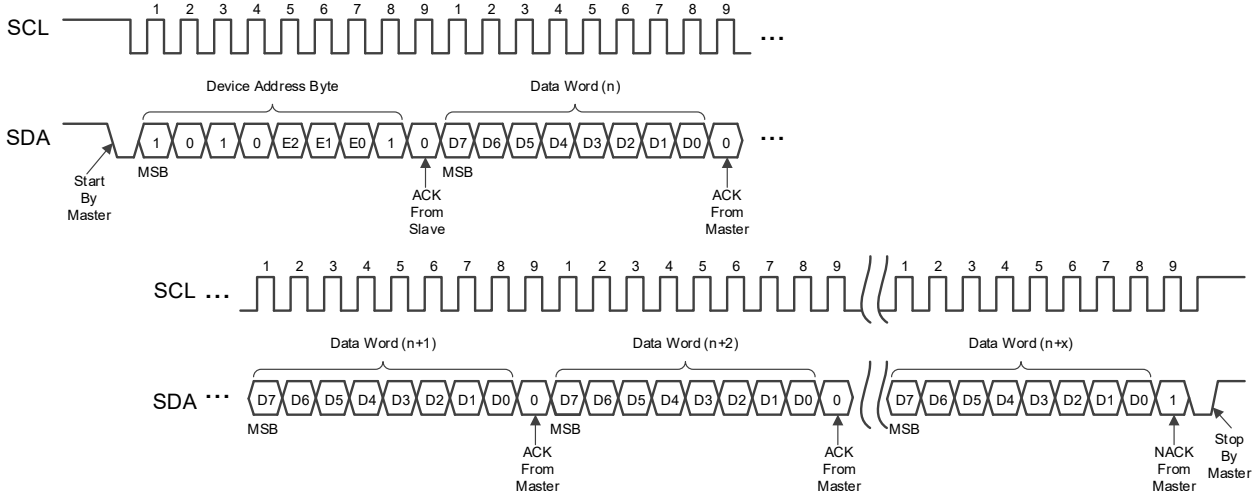


Figure 15. Sequential Read

READ AND WRITE OPERATIONS (continued)

Read Chip Enable Register

Reading the Chip Enable register is performed with a Random Read at address 111x_xxxx_xxxx_xxxxb (where 'x' is Don't Care). The higher four bits of the Chip Enable register content are read as '0000' (see Figure 16). The lower four bits (bit 3, bit 2, bit 1, and bit 0) are defined in ***Chip Enable Register*** section. Reading more than one byte will loop on reading the Chip Enable register value.

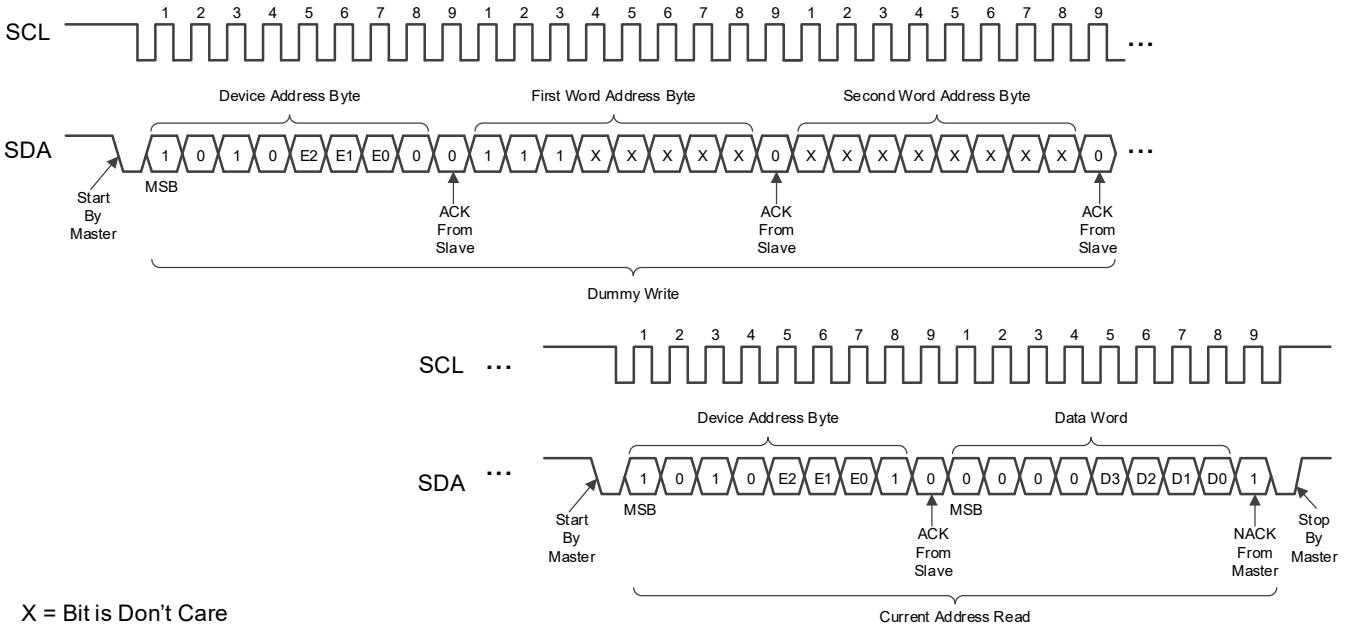


Figure 16. Read Chip Enable Register

READ AND WRITE OPERATIONS (continued)

Read Unique ID

The TD24C256-C1 offers a separate memory block containing a factory programmed 128-bit Unique ID (UID), or Serial Number. Reading the Serial Number is similar to Sequential Read, except that:

- The word address bits A15:A13 must be '100', bits A12:A4 are Don't Care;
- The word address bits A3:A0 define the byte locations inside the Unique ID (see Table 4).

In order to guarantee a unique number, the entire 128-bit value must be read from the starting address of the Serial Number block. To read the first byte of the Serial Number, the word address bits A3:A0 need to be '0000'. Writing or altering the 128-bit Unique ID is not allowed. When the end of the 128-bit UID block is reached (16 bytes of data), the word address will roll over to the beginning of the 128-bit UID block. The Read Unique ID operation is terminated when the Master responds with an NACK to the data byte followed by a Stop condition (see Figure 17).

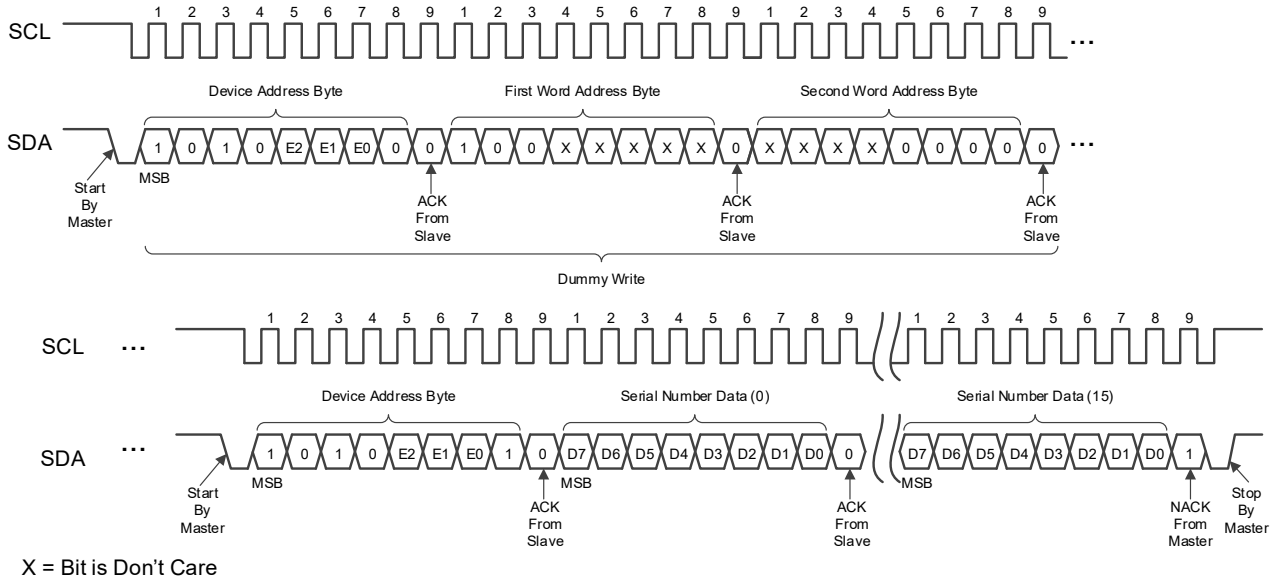


Figure 17. Read Unique ID

INITIAL DELIVERY STATE

The TD24C256-C1 serial EEPROM is delivered as follows:

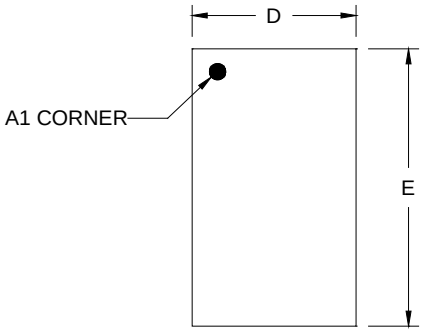
- All bits in the memory array are set to ‘1’ (each byte contains FFh).
- All bits in the Chip Enable register are set to ‘0’ (00h).

REVISION HISTORY

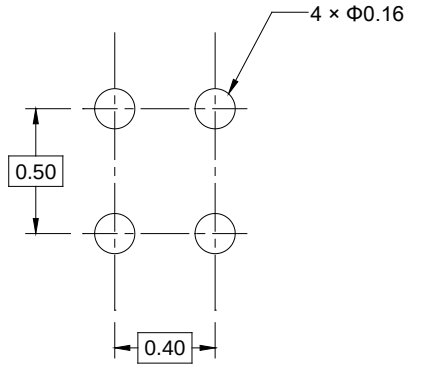
REVISION	DATE	COMMENTS
REV.A	Jun. 2023	Initial version release
REV.A.1	Mar. 2023	Added: — 4-Ball 400 x 400μm WLCSP Package Information
REV.A.2	Dec. 2025	Updated: — Figure 16 and Figure 17
REV.A.3	Oct. 2026	Updated: — Package Outline Dimensions Deleted: — 4-Ball WLCSP (ball pitch 400μm × 400μm) package Added: — N_W at T_A = +105℃, Page mode — Tape and Reel Information

PACKAGE OUTLINE DIMENSIONS

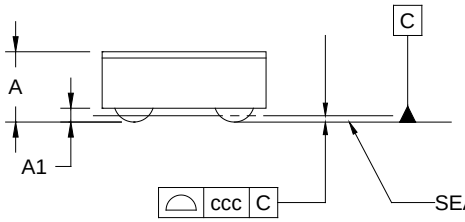
WLCSP-0.65×1.11-4B



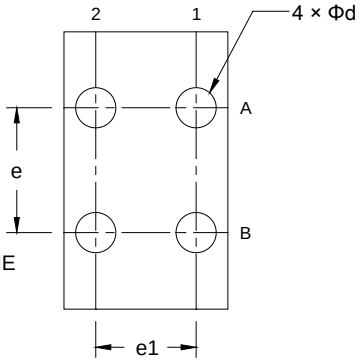
TOP VIEW



RECOMMENDED LAND PATTERN (Unit: mm)



SIDE VIEW



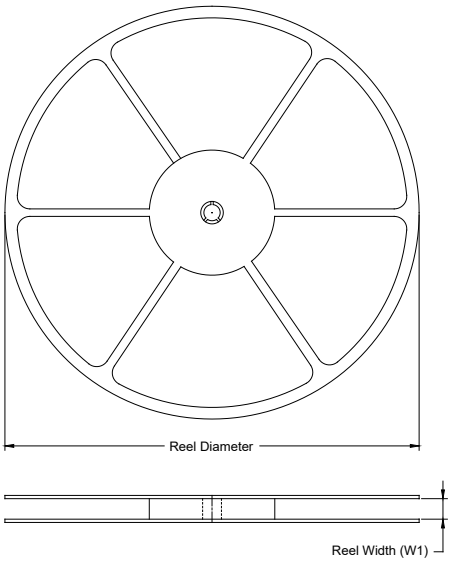
BOTTOM VIEW

Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	-	-	0.302
A1	0.050	-	0.061
D	0.623	-	0.683
E	1.075	-	1.135
d	0.130	-	0.190
e	0.500 BSC		
e1	0.400 BSC		
ccc	0.050		

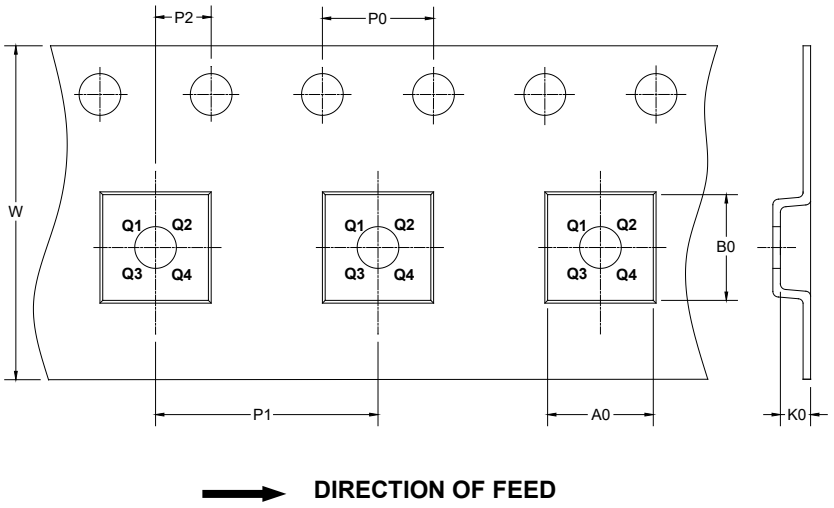
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



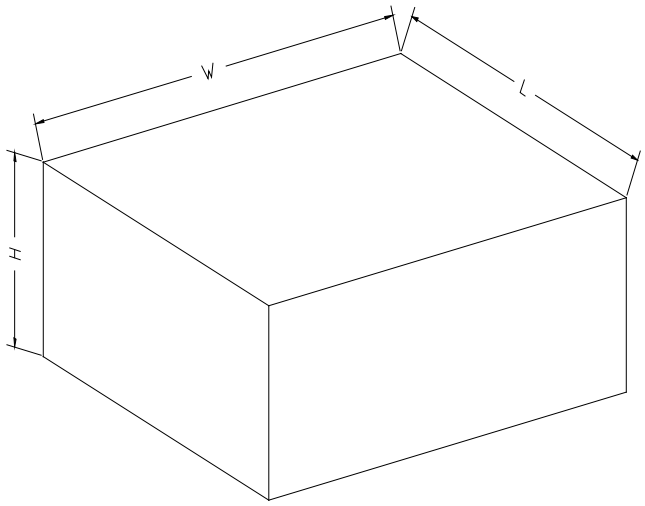
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
WLCSP-0.65×1.11-4B	7"	8.6	0.78	1.21	0.38	4.0	4.0	2.0	8.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18

DD0002