SGM71632H4
4-Channel, 16-Bit, High-Accuracy, ±16V Output, Digital-to-Analog Converter

GENERAL DESCRIPTION

The SGM71632H4 stands as a highly precise, 4-channel, 16-bit digital-to-analog converter (DAC). It functions across a supply voltage range of ±5V to ±18V when in bipolar output mode, and within ±5V to 24V/-12V in unipolar mode. Through utilization of a 5V reference, the SGM71632H4 can be conveniently configured to produce outputs such as ±10V, ±5V, 0V to 20V, or 0V to 10V. Noteworthy attributes of the SGM71632H4 encompass its provision of 16-bit monotonic behavior, exceptional integral nonlinearity (INL) error control within ±1LSB, minimal glitch and noise characteristics throughout an operational temperature span ranging from -40℃ to +125℃. The manufacturing process includes precision trimming to minimize zero and gain errors. Moreover, the SGM71632H4 introduces a user-configurable system-level calibration function that enables the attainment of ±0.125LSB zero error and ±1LSB gain error.

Embedded within the SGM71632H4 are integrated reference buffers and output buffers. Its key features encompass a standard high-speed 1.8V, 3V, or 5V serial peripheral interface (SPI) capable of functioning at clock frequencies of up to 50MHz for seamless interaction with a DSP or microprocessor. Addressing the four DAC channels and auxiliary registers involves employing four address bits. The device incorporates double-buffered interface logic to enable concurrent updates for all DACs. Introducing an asynchronous load input (nLDAC) that facilitates the transfer of data from the input data register to the DAC latch, the content residing in the DAC latch establishes the resultant output voltage. Furthermore, the asynchronous nRST input serves to reset the output of all four DACs to 0V. The V_{MON} pin serves as an analog monitoring output that offers multiplexing capabilities for the individual DAC outputs or the AIN pin.

FEATURES

- **16-Bit Monotonic**
- **Analog Output Ranges:**
  - **Outputs in Bipolar: Up to ±16V**
  - **Outputs in Unipolar: 0V to +20V**
- **INL: ±1LSB (MAX)**
- **Low Zero Error and Gain Error**
  - **Before User Calibration**
    Zero Error: ±6LSB (MAX)
    Gain Error: ±12LSB (MAX)
  - **After User Calibration:**
    Zero Error: ±0.125LSB (TYP)
    Gain Error: ±1LSB (TYP)
- **Configurable Gain: ×2/×4**
- **Settling Time: 6μs (TYP)**
- **Low Noise: 85nV/$\sqrt{Hz}$ (TYP)**
- **Analog Output Monitor**
- **SPI: Up to 50MHz, 1.8V/3V/5V Logic**
- **Support Power-Down Mode**
- **Support Daisy-Chain Mode**
- **Operating Temperature Range: -40℃ to +125℃**
- **Available in Green TQFP-7×7-48L and TQFN-6×6-40FL Packages**

APPLICATIONS

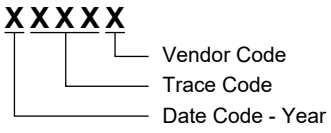
ATE (Automatic Test Equipment)
Precision Instrumentation
PCTL (Industrial Process Control Automation)
Communications

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM71632H4	TQFP-7×7-48L	-40℃ to +125℃	SGM71632H4XTFJ48G/TR	SGM17R XTFJ48 XXXXX	Tape and Reel, 3000
			SGM71632H4XTFJ48SG/TR	SGM17R XTFJ48 XXXXX	Tape and Reel, 500
	TQFN-6×6-40FL	-40℃ to +125℃	SGM71632H4XTVG40G/TR	SGM71632H4 XTVG40 XXXXX	Tape and Reel, 3000
			SGM71632H4XTVG40SG/TR	SGM71632H4 XTVG40 XXXXX	Tape and Reel, 500

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Voltage Range
- AV_{DD} to AV_{SS} (1) ..... -0.3V to 38V
- AV_{DD} to AGND (1) ..... -0.3V to 25V
- AV_{SS} to AGND, DGND (1) ..... -19V to 0.3V
- DV_{DD} to DGND ..... -0.3V to 6V
- IOV_{DD} to DGND ..... -0.3V to DV_{DD}+0.3V
- Digital Input Voltage to DGND ..... -0.3V to DV_{DD}+0.3V
- SDO to DGND ..... -0.3V to DV_{DD}+0.3V
- SGND-x, REFGND-x, AGND to DGND ..... -0.3V to 0.3V
- V_{OUT}-x, R_{FB1}-x, R_{FB2}-x, V_{MON}, AIN to AV_{SS} ..... -0.3V to AV_{DD}+0.3V
- REF-x to REFGND-x, AGND ..... -0.3V to MIN (AV_{DD}/2, -AV_{SS}/2)
- GPIO-x to DGND ..... -0.3V to 6V

GPIO-x Input Current 5mA

Package Thermal Resistance
- TQFP-7×7-48L, θ_{JA} ..... 69.9℃/W
- TQFP-7×7-48L, θ_{JB} ..... 49.9℃/W
- TQFP-7×7-48L, θ_{JC} ..... 15.6℃/W
- TQFN-6×6-40FL, θ_{JA} ..... 23.5℃/W
- TQFN-6×6-40FL, θ_{JB} ..... 5.9℃/W
- TQFN-6×6-40FL, $\theta_{JC\ (TOP)}$ ..... 11.3℃/W
- TQFN-6×6-40FL, $\theta_{JC\ (BOT)}$ ..... 0.9℃/W

Junction Temperature ..... +150℃

Storage Temperature Range ..... -65℃ to +150℃

Lead Temperature (Soldering, 10s) ..... +260℃

ESD Susceptibility (2) (3)

HBM ..... ±4000V

CDM ..... ±1000V

NOTES: 1. AV_{SS} must be < -3.5V when AV_{DD} ≥ 1V.

2. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.

3. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

RECOMMENDED OPERATING CONDITIONS

Operating Temperature Range ..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

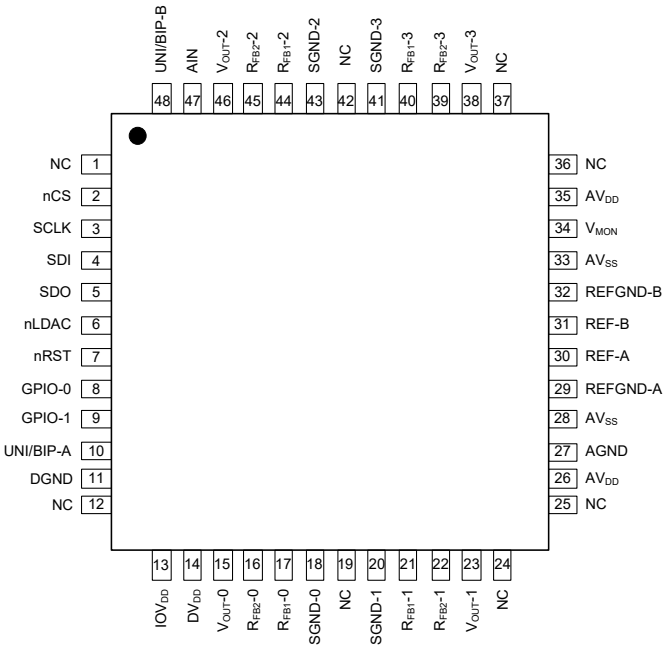
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

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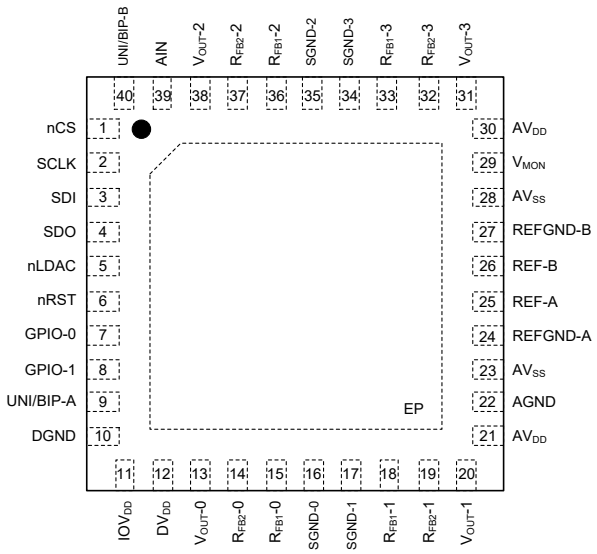
PIN CONFIGURATIONS

(TOP VIEW)



TQFP-7×7-48L

(TOP VIEW)



TQFN-6×6-40FL

PIN DESCRIPTION

PIN		NAME	TYPE	FUNCTION
TQFP-7×7-48L	TQFN-6×6-40FL			
1, 12 19, 24, 25, 36, 37, 42	—	NC	—	No Connection.
2	1	nCS	I	SPI Bus Chip Select Input Pin. Active low. The data is only loaded into the SPI shift register when nCS is at a low logic level. When nCS is at a high logic level, the SDO enters a high-impedance state.
3	2	SCLK	I	Serial Interface Clock Pin.
4	3	SDI	I	Serial Interface Data Input Pin.
5	4	SDO	O	Serial Interface Data Output Pin.
6	5	nLDAC	I	Load DAC Latch Control Input Pin. Active low. When the nLDAC signal is in a low state, the DAC latch is rendered transparent, enabling the transfer of data from the input data register into it. The DAC output undergoes an immediate transition to the corresponding level upon the update of the DAC latch.
7	6	nRST	I	Reset Input Pin. Active low. Applying a logic low signal to this pin initiates a reset operation on the input registers and DACs, restoring them to the values established by the UNI/BIP-x pins. Additionally, it configures the gain register and zero register to their default settings.
8	7	GPIO-0	I/O	General-Purpose Digital Input/Output Pin. This pin serves as a bidirectional digital input/output with an open-drain output configuration. When utilizing this pin as an output, it is essential to incorporate a 10kΩ pull-up resistor connected to IOV_{DD}. Refer to the General-Purpose Input/Output Pins section for comprehensive information.
9	8	GPIO-1		
10	9	UNI/BIP-A	I	Group A Output Mode Selection (DAC-0 and DAC-1). When UNI/BIP-A pin is connected to IOV_{DD}, the group A operates in unipolar output mode. Conversely, when UNI/BIP-A pin is linked to DGND, the group A functions in bipolar output mode. For the unipolar output mode, the input data written to the DAC is in straight binary format, whereas for the bipolar output mode, it employs two's complement representation.

PIN DESCRIPTION (continued)

PIN		NAME	TYPE	FUNCTION
TQFP-7×7-48L	TQFN-6×6-40FL			
11	10	DGND	I	Digital Ground.
13	11	IOV_{DD}	I	Interface Power Supply Pin.
14	12	DV_{DD}	I	Digital Power Supply Pin.
15	13	V_{OUT}-0	O	DAC-0 Output Pin.
16	14	R_{FB2}-0 (1)	O	DAC-0 R_{FB2} Feedback Pin.
17	15	R_{FB1}-0 (1)	O	DAC-0 R_{FB1} Feedback Pin.
18	16	SGND-0	I	DAC-0 Signal Ground. Connect it to REFGND-A.
20	17	SGND-1	I	DAC-1 Signal Ground. Connect it to REFGND-A.
21	18	R_{FB1}-1 (1)	O	DAC-1 R_{FB1} Feedback Pin.
22	19	R_{FB2}-1 (1)	O	DAC-1 R_{FB2} Feedback Pin.
23	20	V_{OUT}-1	O	DAC-1 Output Pin.
26, 35	21, 30	AV_{DD}	I	Positive Analog Power Supply Pin.
27	22	AGND	I	Analog Ground.
28, 33	23, 28	AV_{SS}	I	Negative Analog Power Supply Pin.
29	24	REFGND-A	I	Reference REF-A Ground. Connect to AGND.
30	25	REF-A	I	Group A (DAC-0, DAC-1) Reference Input Pin.
31	26	REF-B	I	Group B (DAC-2, DAC-3) Reference Input Pin.
32	27	REFGND-B	I	Reference REF-B Ground. Connect to AGND.
34	29	V_{MON}	O	Analog Monitor Output Pin. It is either in a Hi-Z state or can be connected to one of the four DAC outputs or AIN, contingent on the settings within the monitor register.
38	31	V_{OUT}-3	O	DAC-3 Output Pin.
39	32	R_{FB2}-3 (1)	O	DAC-3 R_{FB2} Feedback Pin.
40	33	R_{FB1}-3 (1)	O	DAC-3 R_{FB1} Feedback Pin.
41	34	SGND-3	I	DAC-3 Signal Ground. Connect it to REFGND-B.
43	35	SGND-2	I	DAC-2 Signal Ground. Connect it to REFGND-B.
44	36	R_{FB1}-2 (1)	O	DAC-2 R_{FB1} Feedback Pin.
45	37	R_{FB2}-2 (1)	O	DAC-2 R_{FB2} Feedback Pin.
46	38	V_{OUT}-2	O	DAC-2 Output Pin.
47	39	AIN	I	Auxiliary Analog Input Pin. Connect it to the analog monitor mux.
48	40	UNI/BIP-B	I	Group B Output Mode Selection (DAC-2 and DAC-3).When UNI/BIP-B pin is connected to IOV_{DD}, the group B operates in unipolar output mode. Conversely, when UNI/BIP-B pin is connected to DGND, the group B functions in bipolar output mode. For the unipolar output mode, the input data written to the DAC is in straight binary format, while for the bipolar output mode, it employs two's complement representation.
—	Exposed Pad	EP	—	Exposed Pad.

NOTE:

1. To configure DAC-x with a gain of 2, connect R_{FB1}-x and R_{FB2}-x to V_{OUT}-x, and set the corresponding gain bit in the command register to '0'. For a DAC-x gain of 4, connect R_{FB1}-x to V_{OUT}-x, leave R_{FB2}-x open, and set the corresponding gain bit in the command register to '1'. Following a power-on reset or user-initiated reset, the gain bit defaults to '1'. In order to achieve the gain of 2, the gain bit must be cleared to '0'.

FUNCTIONAL BLOCK DIAGRAM

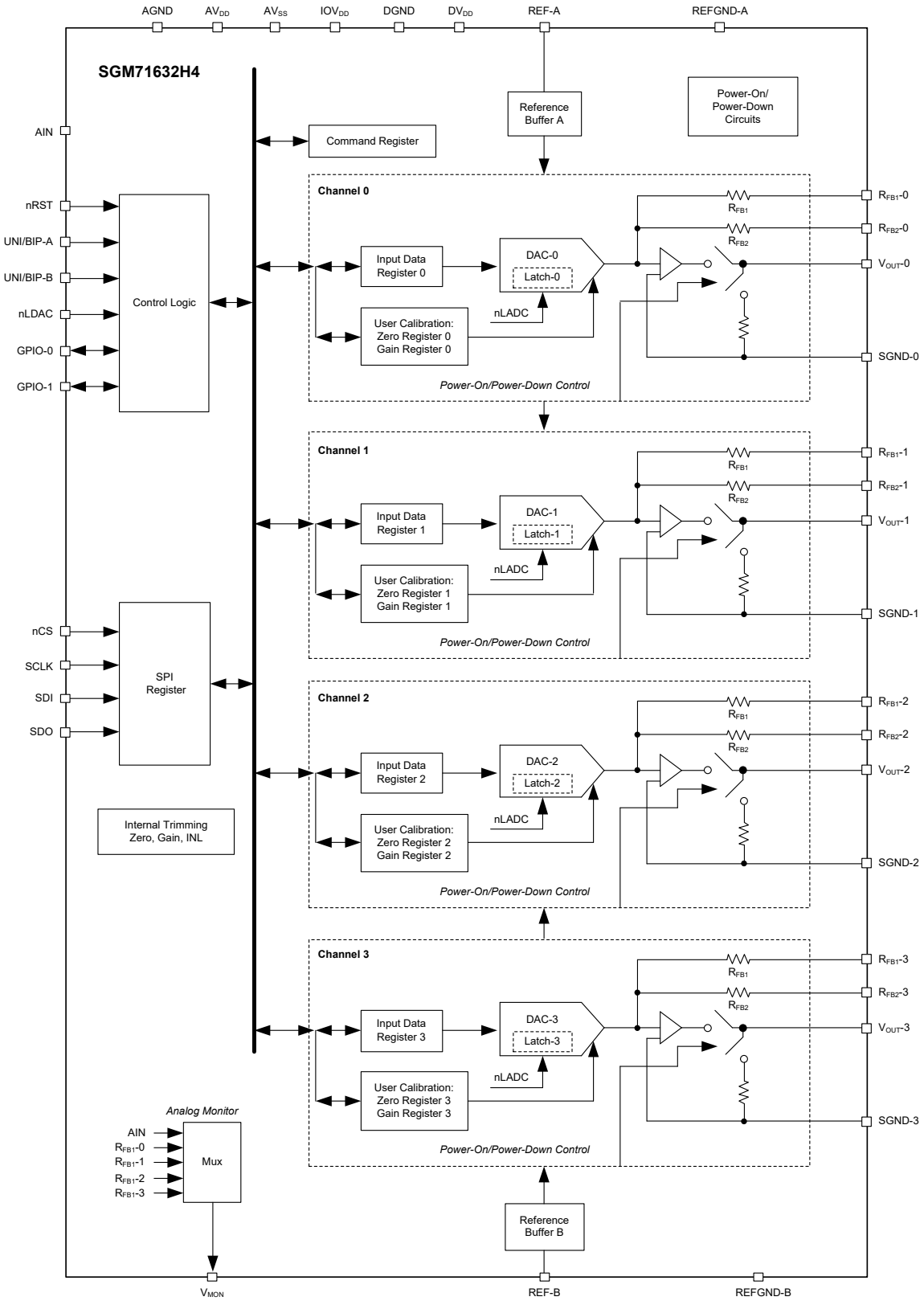
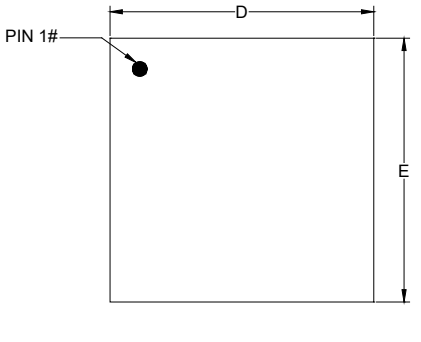


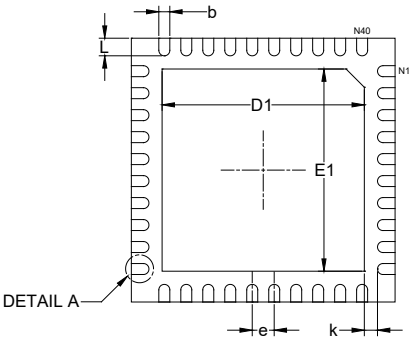
Figure 1. Block Diagram

PACKAGE OUTLINE DIMENSIONS

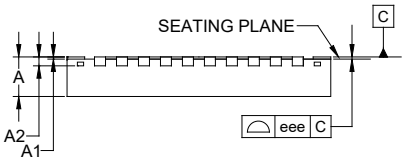
TQFN-6×6-40FL



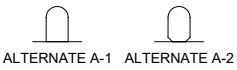
TOP VIEW



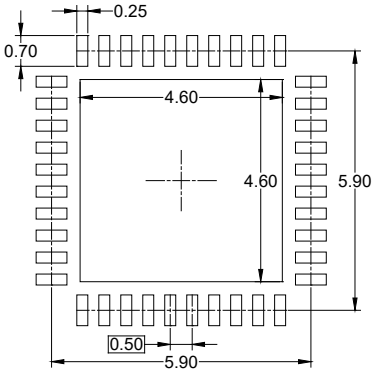
BOTTOM VIEW



SIDE VIEW



DETAIL A
ALTERNATE TERMINAL CONSTRUCTION



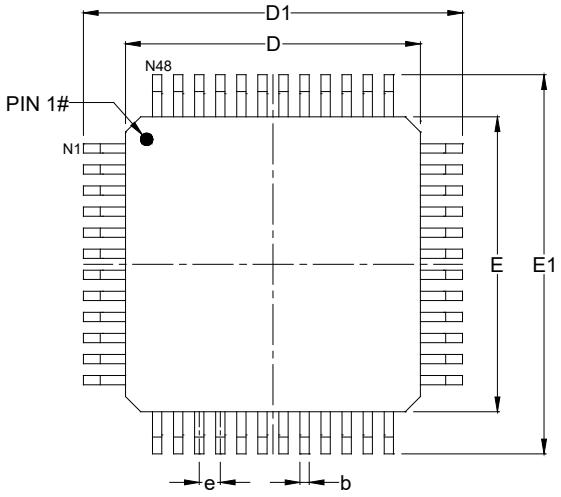
RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	0.800	-	1.000
A1	0.000	-	0.050
A2		0.203 REF	
b	0.200	-	0.300
D	5.900	-	6.100
E	5.900	-	6.100
D1	4.500	-	4.700
E1	4.500	-	4.700
k	0.200	-	-
L	0.300	-	0.500
e		0.500 BSC	
eee		0.080	

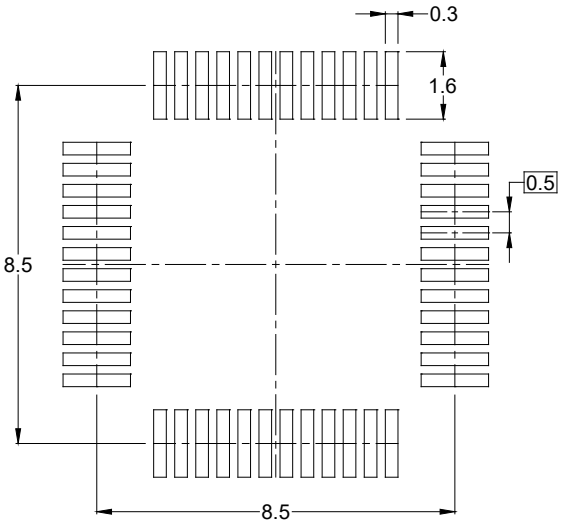
NOTE: This drawing is subject to change without notice.

PACKAGE OUTLINE DIMENSIONS

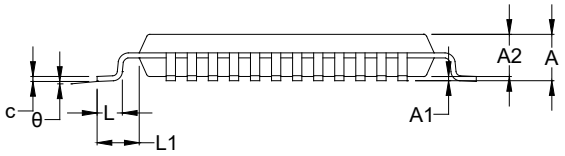
TQFP-7×7-48L



TOP VIEW



RECOMMENDED LAND PATTERN (Unit: mm)



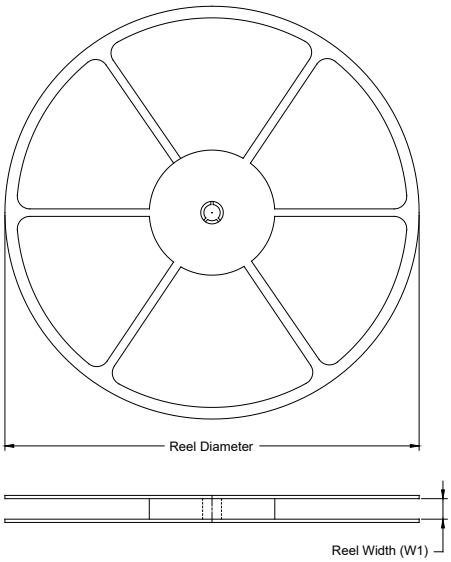
SIDE VIEW

Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	-	-	1.200
A1	0.050	-	0.150
A2		1.000 REF	
b	0.170	-	0.270
c	0.090	-	0.200
D	6.900	-	7.100
D1	8.800	-	9.200
E	6.900	-	7.100
E1	8.800	-	9.200
e		0.500 BSC	
L	0.450	-	0.750
L1		1.000 REF	
θ	0°	-	7°

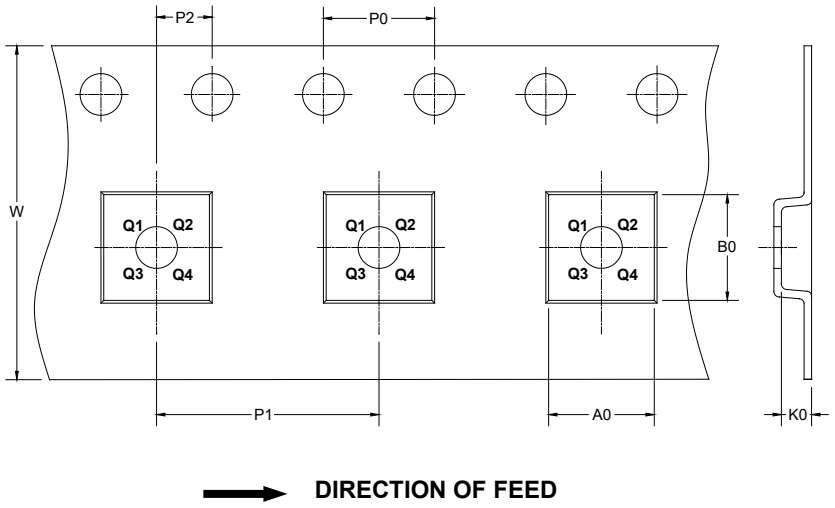
NOTES:
1. This drawing is subject to change without notice.
2. The dimensions do not include mold flashes, protrusions or gate burrs.
3. Reference JEDEC MS-026.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



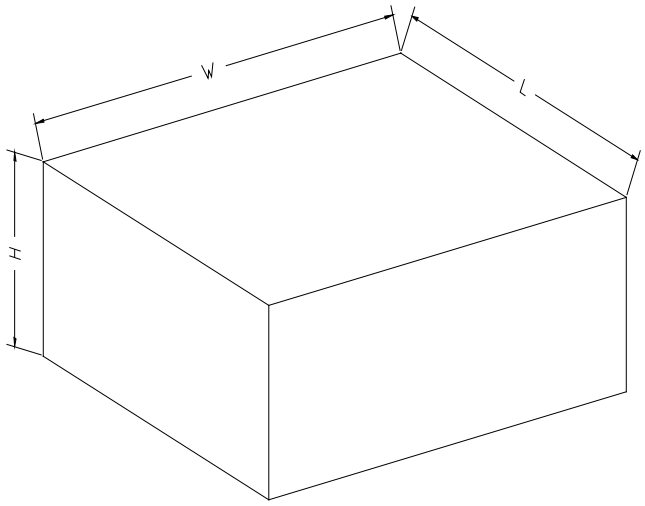
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TQFN-6×6-40FL	13″	16.4	6.30	6.30	1.10	4.0	8.0	2.0	16.0	Q2
TQFP-7×7-48L	13″	16.4	9.40	9.40	1.35	4.0	12.0	2.0	16.0	Q2

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002