SGM25702
High-side Protection Controller with Low Quiescent Current

GENERAL DESCRIPTION

The SGM25702 high-side protection controller intelligently manages a high-side N-channel MOSFET during standard on/off transitions and fault conditions. It controls in-rush current through a constant rise time of the output voltage. A power good output indicates when the output voltage matches the input voltage and the MOSFET is fully conducting. The controller includes input UVLO with hysteresis and programmable input OVP. It features a remote on/off control via an enable input and a second safety redundancy enable through programmable UVLO. A single capacitor configures the delay time for initial start-up V_{GS} fault detection, transition V_{DS} fault detection and continuous over-current V_{DS} fault detection. When a fault persists beyond the set delay, the MOSFET is deactivated until either the enable input or UVLO input is toggled low and then high again, restoring operation.

The SGM25702 is available in a Green MSOP-10 package.

FEATURES

- **Wide Operating Input Voltage Range: 5.5V to 65V**
- **Less than 11μA Quiescent Current in Disabled Mode**
- **Controlled Output Rise Time for Safe Capacitive Loads Connection**
- **Charge Pump Gate Driver for External N-Channel MOSFET**
- **Adjustable Under-Voltage Lockout (UVLO) with Hysteresis**
- **UVLO Serves as Second Enable Input for Systems Requiring Safety Redundancy**
- **Programmable Fault Detection Delay Time**
- **MOSFET Latched Off after Load Fault Detection**
- **Power Good (nPG) Output is Active Low Open-Drain**
- **Adjustable Input Over-Voltage Protection (OVP)**
- **Immediate Restart after Over-Voltage Shutdown**
- **Available in a Green MSOP-10 Package**

APPLICATIONS

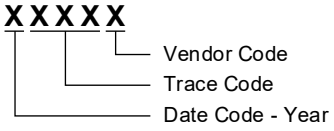
Industrial Body Electronics

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM25702	MSOP-10	-40℃ to +125℃	SGM25702XMS10G/TR	SGM1FU XMS10 XXXXX	Tape and Reel, 4000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

IN Pin (1) ..... -0.3V to 70V
SENSE, OUT Pins ..... -0.3V to 70V
GATE Pin (1) ..... -0.3V to 80V
EN, UVLO Pins ..... -0.3V to 70V
nPG, OVP Pins ..... -0.3V to 70V
TIMER Pin ..... -0.3V to 6V
Package Thermal Resistance
MSOP-10, θ_{JA} ..... 142.4℃/W
MSOP-10, θ_{JB} ..... 91.8℃/W
MSOP-10, θ_{JC} ..... 47.9℃/W
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility (2) (3)
HBM ..... ±4000V
CDM ..... ±1000V

NOTES:

1. When the device is enabled, the voltage of the GATE pin is 12.2V (TYP) higher than that of the IN pin. Considering the Absolute Maximum Rating of the GATE pin is 80V, only when the device is disabled or under an instantaneous surge condition, IN can be applied a voltage of 70V.

2. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.

3. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

RECOMMENDED OPERATING CONDITIONS

Supply Voltage, V_{IN} ..... 5.5V to 65V
GATE Pin Voltage ..... 0V to 80V
Enable Voltage, V_{EN} ..... 0V to 65V
Under-Voltage Lockout Voltage, V_{UVLO} ..... 0V to 65V
nPG Pin Voltage ..... 0V to 65V
nPG Pin Sink Current ..... 0mA to 5mA
Operating Ambient Temperature, T_A ..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

DISCLAIMER

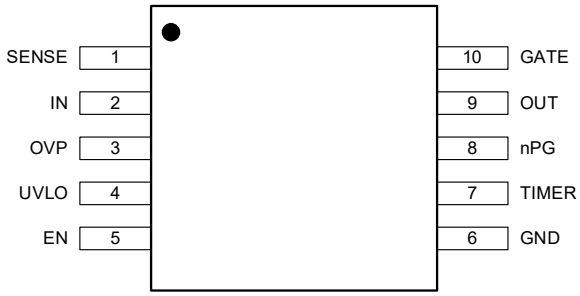
SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

ESD SENSITIVITY CAUTION

This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

PIN CONFIGURATION

(TOP VIEW)



MSOP-10

PIN DESCRIPTION

PIN	NAME	I/O	FUNCTION
1	SENSE	I	Input Voltage Sense. The fault detection threshold is determined by an external resistor multiplying a constant current sink (16μA TYP) at the SENSE pin.
2	IN	P	Supply Voltage Input. Operating voltage ranges from 5.5V to 65V. The internal power-on reset (POR) circuit typically activates when the IN pin exceeds 5.1V. It is advisable to place a small ceramic bypass capacitor near this pin to mitigate noise.
3	OVP	I	Over-Voltage Protection Comparator Input. An external resistor divider connected to the input supply voltage determines the over-voltage turn-off threshold. When the OVP exceeds the typical 2.0V threshold, the GATE pin is pulled low, but the controller does not latch off. Normal operation resumes once the OVP pin drops below typical 1.76V.
4	UVLO	I	Under-Voltage Lockout Comparator Input. The UVLO pin serves as the input for under-voltage lockout by interfacing this pin with a resistor divider network between the input supply voltage and the ground. The UVLO comparator is activated when the EN signal is in high state. Once the voltage at the UVLO pin exceeds 1.6V (TYP), the pull-down components on the GATE pin are deactivated, thereby permitting the output to incrementally ascend. A constant current sink (5.5μA TYP) is incorporated to guarantee that the UVLO pin stays low during an open circuit situation.
5	EN	I	Enable Input. When the voltage on the EN pin falls below 0.8V, the device transitions into a low-current shutdown state. Conversely, if the voltage surpasses 2.0V, the internal bias circuitry and UVLO comparator are activated. The pull-up bias on the GATE pin is activated only when both EN and UVLO are high. A constant current sink (5μA TYP) is incorporated to guarantee that the EN pin stays low during an open circuit situation.
6	GND	G	Ground Pin.
7	TIMER	I/O	Timing Capacitor. The V_{DS} and V_{GS} fault detection waiting time is determined by an external capacitor connected to this pin. If the voltage at this pin surpasses 2.0V, the external MOSFET will be deactivated by SGM25702 and stay in latch off state. Once EN, UVLO or VIN (POR) input is toggled low and then high, the external MOSFET is released.
8	nPG	O	Fault Status. This output is an open-drain output. If the external MOSFET voltage drop (V_{DS}) falls to the point, where the voltage at the OUT pin surpasses the SENSE pin, the nPG indicator is activated, indicating a fault-free condition with a low signal.
9	OUT	I	Output Voltage Sense. Connect to the output rail, which is the external MOSFET source. It is internally utilized to detect V_{DS} and V_{GS} conditions.
10	GATE	O	Gate Drive Output. Connect to the external MOSFET to provide a constant current source (25μA TYP) generated by the internal charge pump to charge the GATE of external MOSFET. The voltage difference between the GATE and the OUT will be clamped at 17.2V by an internal Zener diode. A capacitor can be connected from the GATE pin to GND in order to reduce the ΔV/Δt of the output voltage.

NOTE: I = input, P = power, G = ground, I/O = input/output, O = output.

ELECTRICAL CHARACTERISTICS

(T_J = -40℃ to +125℃, V_{IN} = 14V, V_{EN} = V_{UVLO} = 2V, V_{OVP} = 1.5V, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
IN Pin						
Input Current, Enabled Mode	I_{IN_EN}			0.34	0.60	mA
Input Current, Disabled Mode	I_{IN_DIS}	V_{EN} = 0V		7.3	11	μA
Input Current, Standby Mode	I_{IN_STB}	V_{UVLO} = 0V		0.37	0.60	mA
Power-On Reset Threshold at IN	POR_{EN}	V_{IN} rising		5.1	5.4	V
POR_{EN} Hysteresis	POR_{HYS}	V_{IN} falling		500		mV
OUT Pin						
OUT Pin Bias Current, Enabled	I_{OUT_EN}	V_{OUT} = V_{IN}	6	8	10	μA
OUT Pin Leakage Current, Disabled (1)	I_{OUT_DIS}	Disabled, V_{OUT} = 0V, V_{SENSE} = V_{IN}		0		μA
SENSE Pin						
Threshold Programming Current	I_{SENSE}	SENSE pin bias current	14	16	18	μA
V_{DS} Comparator Offset Voltage	V_{OFFSET}	SENSE to OUT voltage for fault detection	-7	0	7	mV
Current Ratio of I_{SENSE} and I_{OUT_EN}	I_{RATIO}	I_{SENSE}/I_{OUT_EN}	1.8	2.0	2.2	
OVP Input						
OVP Threshold	OVP_{TH}	Voltage rising	1.88	2.0	2.12	V
OVP Hysteresis	OVP_{HYS}			240		mV
OVP Delay Time	OVP_{DEL}	Delay from OVP pin > OVP_{TH} to GATE low		12		μs
OVP Pin Bias Current	OVP_{BIAS}	V_{OVP} = 1.9V		0	0.5	μA
UVLO Input						
UVLO Threshold	$UVLO_{TH}$	Voltage rising	1.45	1.6	1.75	V
UVLO Hysteresis	$UVLO_{HYS}$		130	180	230	mV
UVLO Pin Pull-Down Current	$UVLO_{BIAS}$		3.8	5.5	7.2	μA
EN Input						
EN Threshold	EN_{THH}		2.0			V
	EN_{THL}				0.8	
EN Threshold Hysteresis	EN_{HYS}			200		mV
EN Pin Pull-Down Current	EN_{BIAS}			5	7	μA

ELECTRICAL CHARACTERISTICS (continued)

(T_J = -40℃ to +125℃, V_{IN} = 14V, V_{EN} = V_{UVLO} = 2V, V_{OVP} = 1.5V, typical values are at T_J = +25℃, unless otherwise noted.)

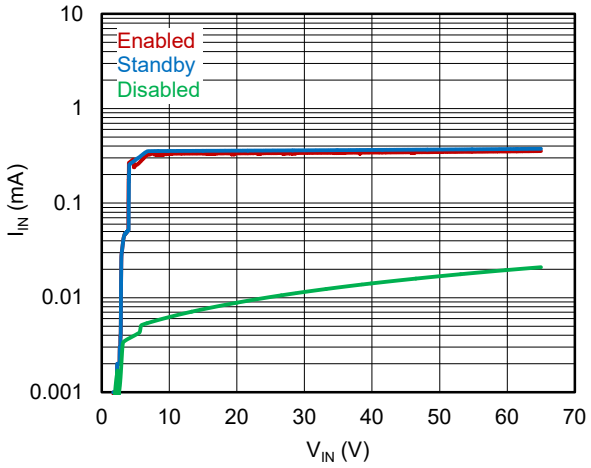
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Gate Control (GATE Pin)						
Gate Charge (Sourcing) Current, On State	I_{GATE}	On-state	16	25	34	μA
Gate Discharge (Sinking) Current, Off State	I_{GATE_OFF}	V_{UVLO} = 0V		2		mA
Gate Discharge (Sinking) Current, Fault State	I_{GATE_FLT}	V_{OUT} < V_{SENSE}		60		mA
Gate Output Voltage in Normal Operation	V_{GATE}	GATE to IN voltage, GATE pin open	10.0	12.2	14.4	V
V_{GS} Status Comparator Threshold Voltage	V_{GATE_TH}	GATE to OUT threshold voltage for TIMER voltage reset and TIMER current change	5.3	6.4	7.5	V
Zener Clamp between GATE Pin and OUT Pin	V_{GATE_CLAMP}	I_{GATE_CLAMP} = 0.1mA		17.2		V
Timer (TIMER Pin)						
Timer Fault Threshold	V_{TMRH}	Voltage rising		2.00		V
Timer Re-Enable Threshold	V_{TMRL}	Voltage falling		0.30		V
Timer Charge Current for V_{DS} Fault	I_{TMRH}	TIMER charge current after start-up, V_{GS} = 7.5V	8.5	11.0	13.5	μA
Timer Start-Up Charge Current	I_{TMRL}	TIMER charge current during start-up, V_{GS} = 5.3V	4.5	6.0	7.5	μA
Timer Reset Discharge Current	I_{TMRR}	TIMER pin = 1.5V	4.5	6.0	7.5	mA
Fault to GATE Low Delay	t_{FAULT}	TIMER pin > 2V, no load on GATE pin		6.5		μs
Power Good (nPG Pin)						
Output Low Voltage	PG_{VOL}	I_{SINK} = 2mA		80	200	mV
Off Leakage Current	PG_{IOH}	V_{nPG} = 10V		0	1.00	μA

NOTE: 1. When the device is enabled, the voltage of the GATE pin is 12.2V (TYP) higher than that of the IN pin. Considering the Absolute Maximum Rating of the GATE pin is 80V, only when the device is disabled or under an instantaneous surge condition, IN can be applied a voltage of 70V.

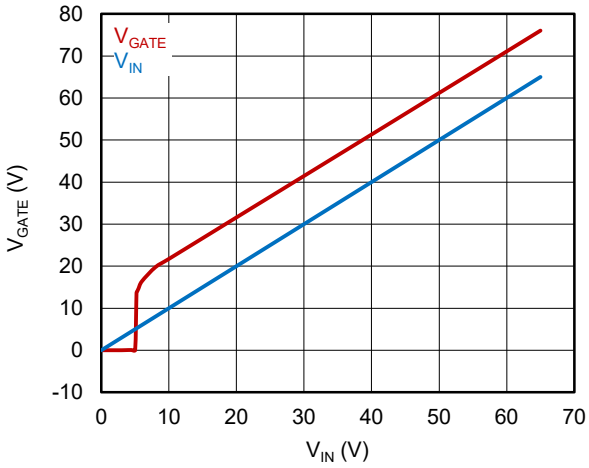
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = -40℃ to +125℃, V_{IN} = 14V, V_{EN} = V_{UVLO} = 2V, V_{OVP} = 1.5V, unless otherwise noted.

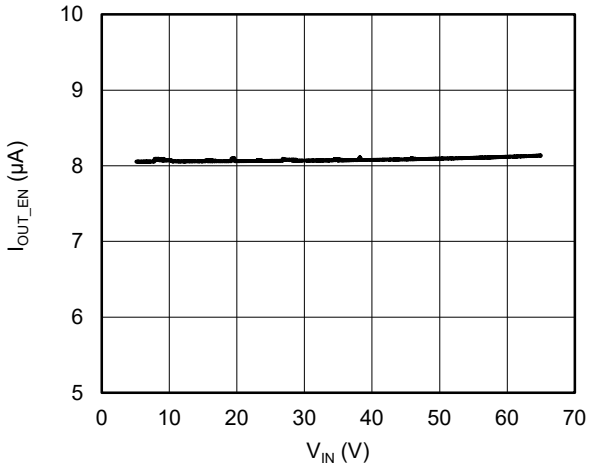
I_{IN} vs. V_{IN}



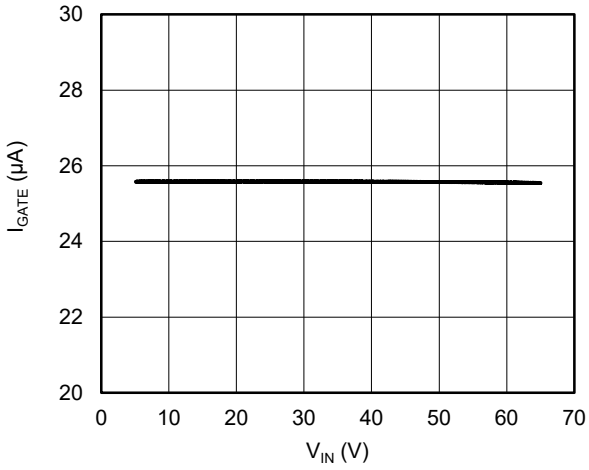
V_{GATE} vs. V_{IN}



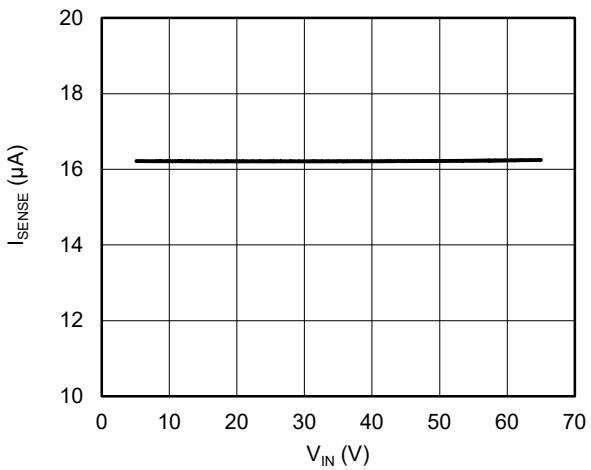
I_{OUT_EN} vs. V_{IN}



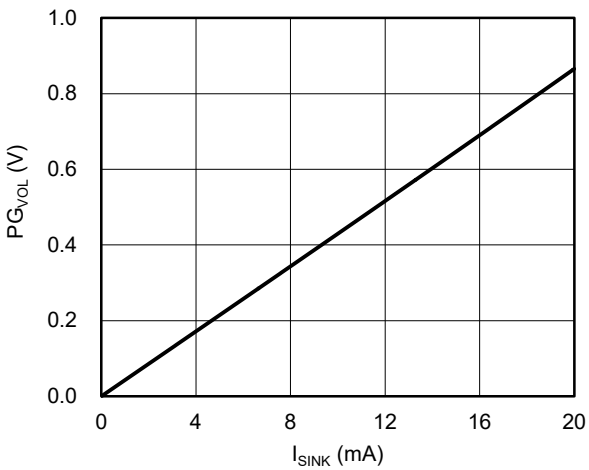
I_{GATE} vs. V_{IN}



I_{SENSE} vs. V_{IN}



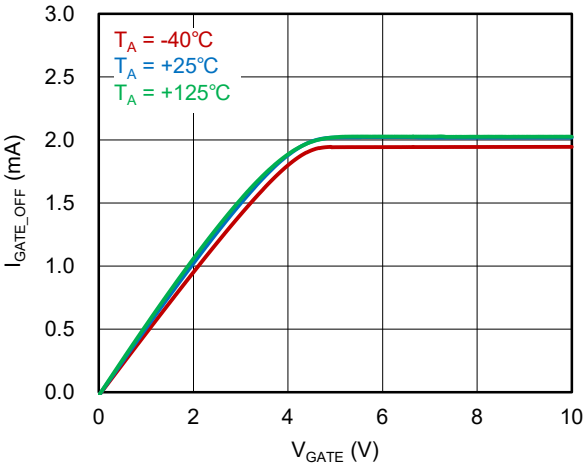
PG_{VOL} vs. I_{SINK}



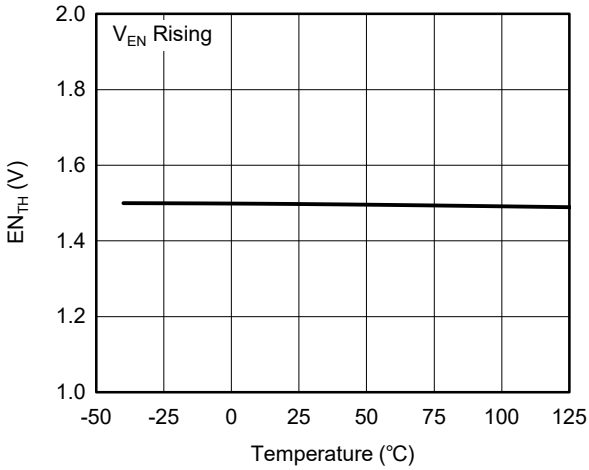
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = -40℃ to +125℃, V_{IN} = 14V, V_{EN} = V_{UVLO} = 2V, V_{OVP} = 1.5V, unless otherwise noted.

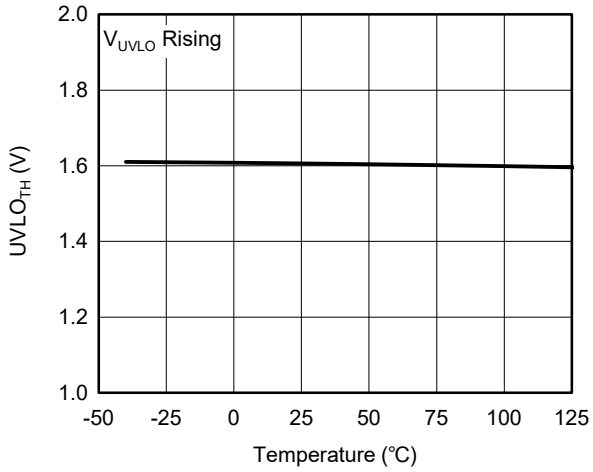
I_{GATE_OFF} vs. V_{GATE}



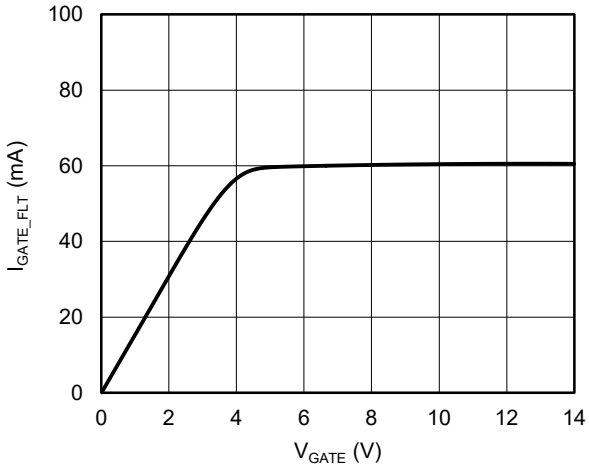
EN_{TH} vs. Temperature



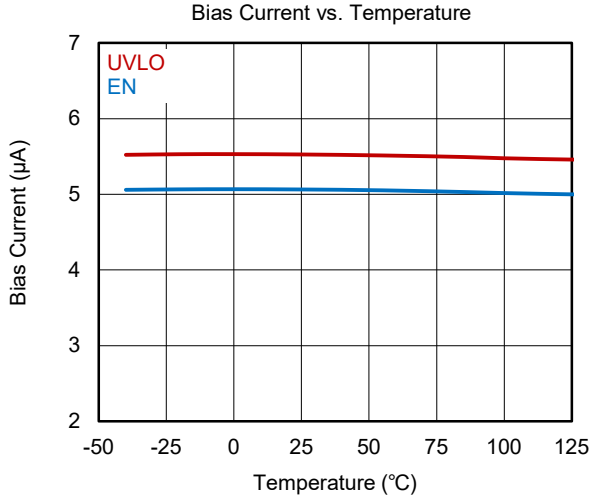
$UVLO_{TH}$ vs. Temperature



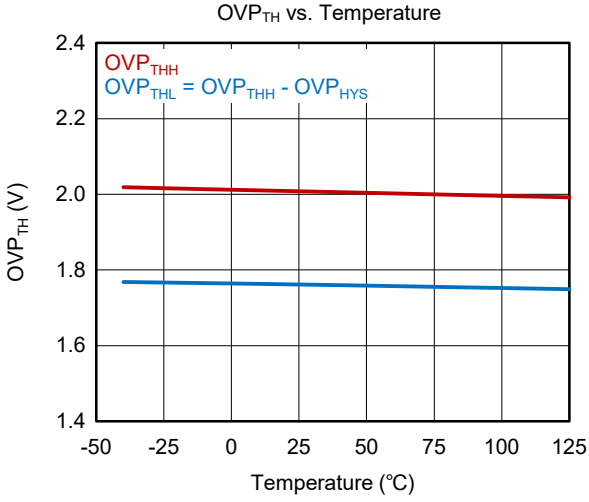
I_{GATE_FLT} vs. V_{GATE}



Bias Current vs. Temperature



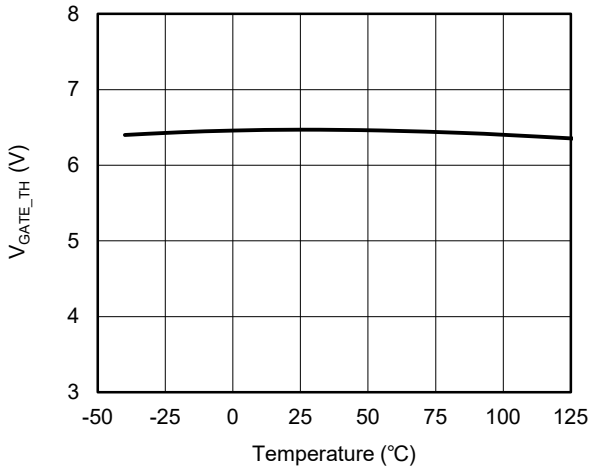
OVP_{TH} vs. Temperature



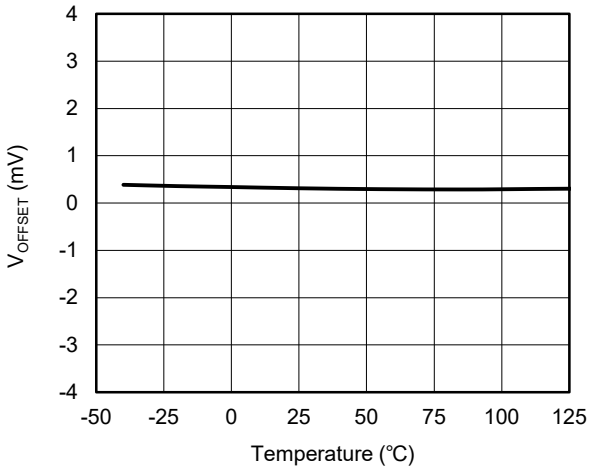
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = -40℃ to +125℃, V_{IN} = 14V, V_{EN} = V_{UVLO} = 2V, V_{OVP} = 1.5V, unless otherwise noted.

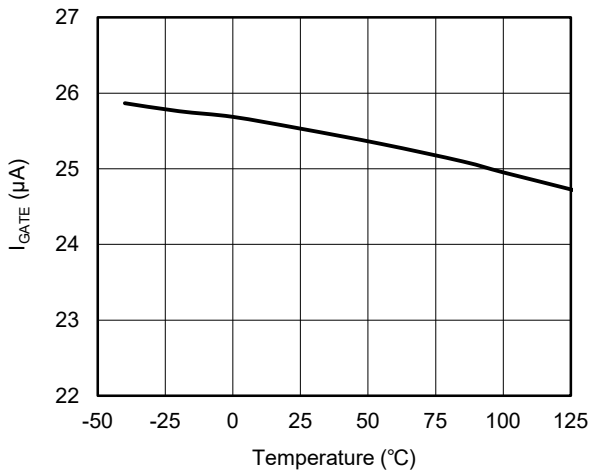
V_{GATE_TH} vs. Temperature



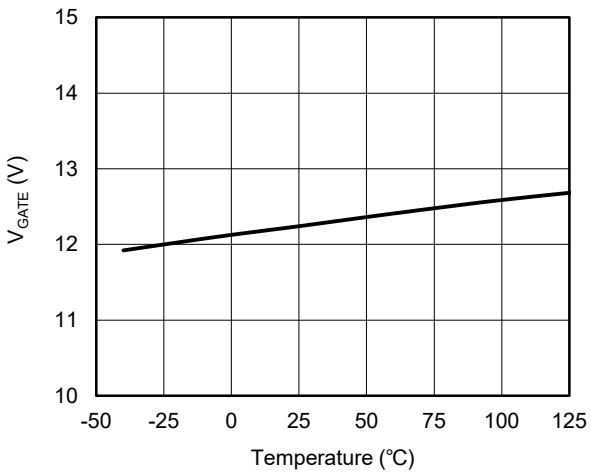
V_{OFFSET} vs. Temperature



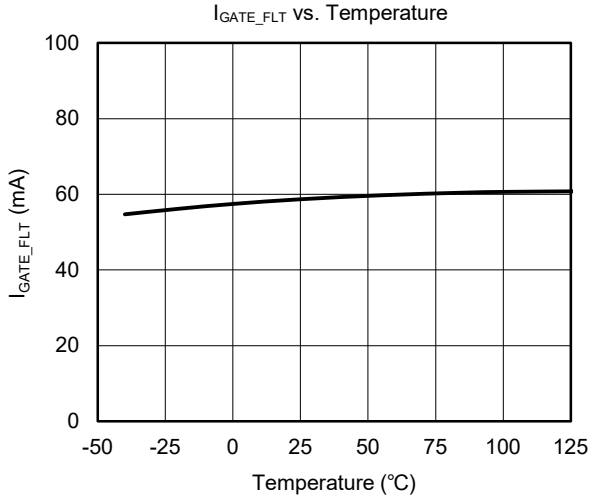
I_{GATE} vs. Temperature



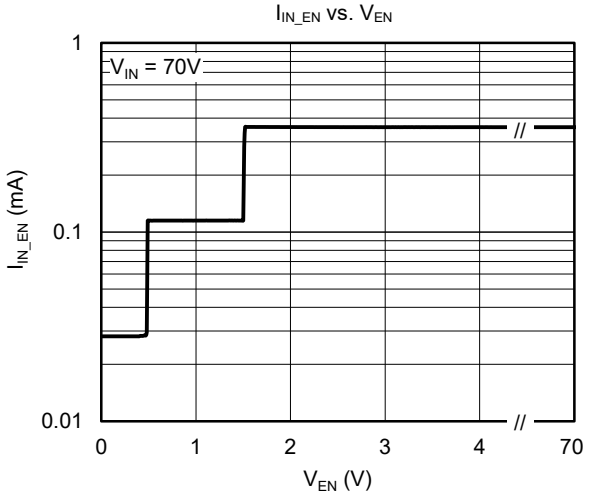
V_{GATE} vs. Temperature



I_{GATE_FLT} vs. Temperature

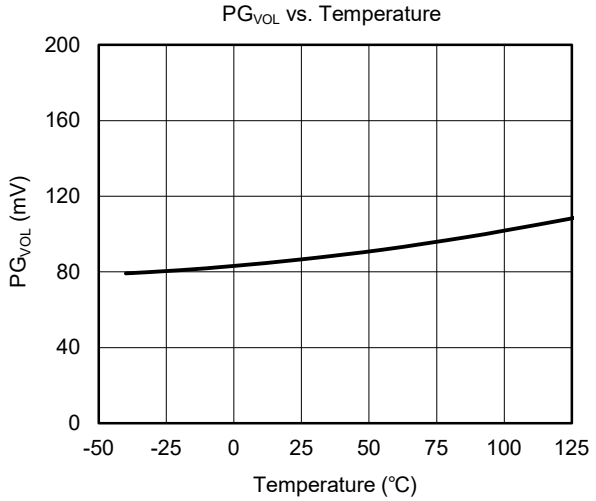


I_{IN_EN} vs. V_{EN}



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = -40℃ to +125℃, V_{IN} = 14V, V_{EN} = V_{UVLO} = 2V, V_{OVP} = 1.5V, unless otherwise noted.



FUNCTIONAL BLOCK DIAGRAM

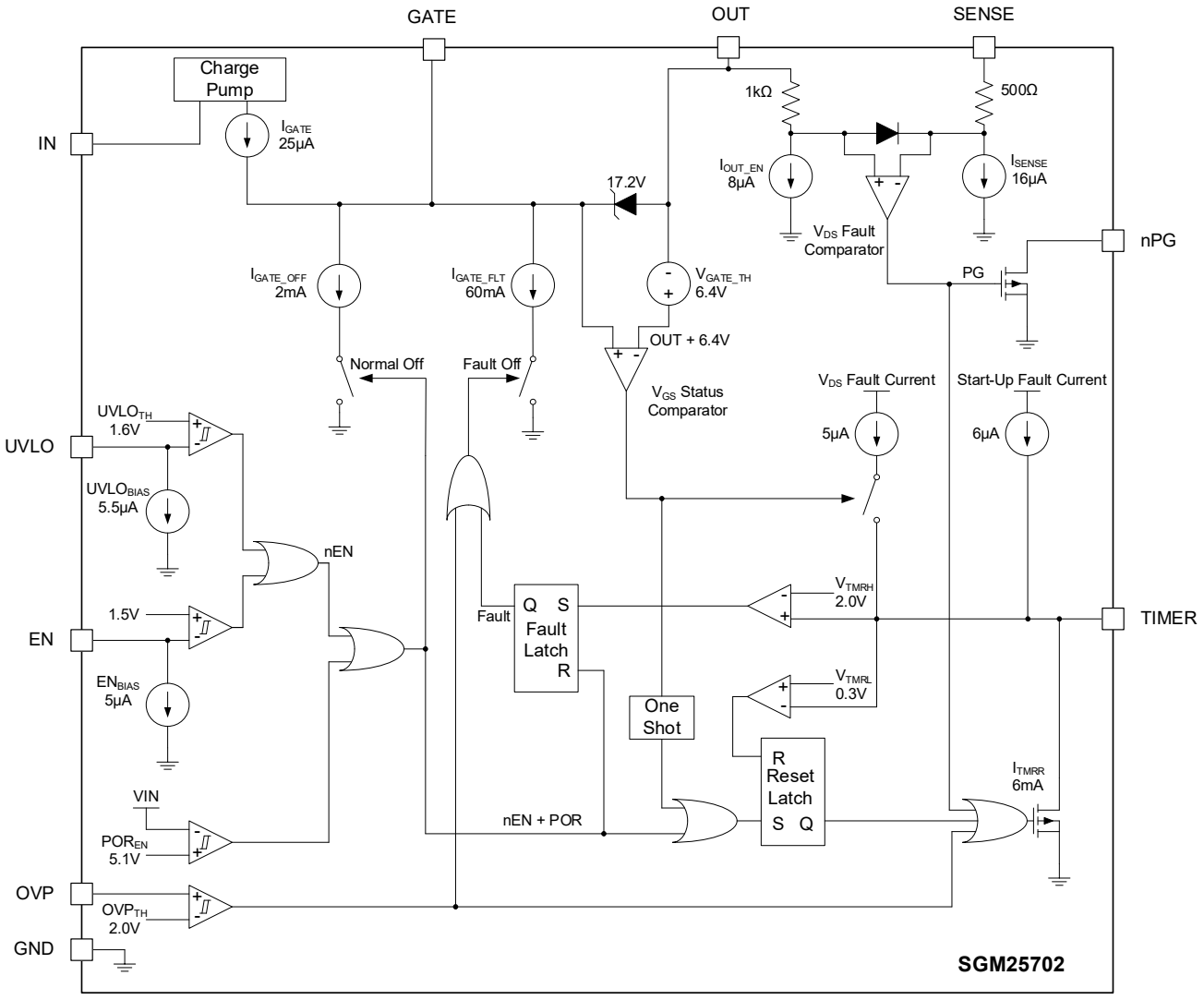


Figure 1. Block Diagram

DETAILED DESCRIPTION

Overview

The SGM25702 is a high-side controller with low quiescent current, which is designed to drive a high-side N-MOSFET. The device provides complete protection for on/off events and various faults, including over-current, start-up, adjustable under-voltage lockout (UVLO) and adjustable input over-voltage protection (OVP). Remote control can be implemented by EN pin, and the external N-MOSFET will be turned off when the EN is low, where the SGM25702 is switched into a quite low quiescent current off mode. The power good indication is provided to report whether the external N-MOSFET is in normal status. An external timer capacitor is used to adjust the waiting time from detecting the fault condition to turning off the N-MOSFET. The start-up time can be adjusted by placing an external capacitor between GATE and GND because of the current source in the gate driver is constant.

Start-Up Sequence

The SGM25702 has an input voltage range of 5.5V to 65V. Please refer to Figure 2 and Figure 3 for details of the typical application circuit and the start-up sequence, respectively. The device is enabled through EN pin exceed the EN_{THH} threshold (2.0V).

When the device begins to start up, a 25μA (TYP) current source inside the GATE pin is used to charge the gate of the external N-MOSFET, and the timer capacitor is charged by a 6μA (TYP) current source. Furthermore, the TIMER pin is pulled low to 0.3V by internal 6mA current source when the gate-to-source voltage (V_{GS}) reaches the V_{GATE_TH} threshold (6.4V TYP) before the C_{TIMER} voltage value reaches 2V which means the V_{GS} sequence is completed, and the internal 5μA current source is enabled. Then the C_{TIMER} is charged by the internal 11μA current source at the TIMER pin until either the drain-to-source voltage (V_{DS}) of the N-MOSFET decrease below the limit threshold (i.e. no V_{DS} fault) or the C_{TIMER} voltage value reaches the V_{TMRH} threshold (2V TYP) (i.e. fault). The drain-to-source voltage (V_{DS}) of the N-MOSFET is indicated by the V_{DS} comparator, which detects the voltage difference between the SENSE and OUT pins. The voltage of SENSE pin can be programmed by the voltage drop across the selected appropriate external resistor. When the OUT voltage is above the SENSE voltage, the active low nPG pin is asserted low (i.e. no fault) and the C_{TIMER} is discharged.

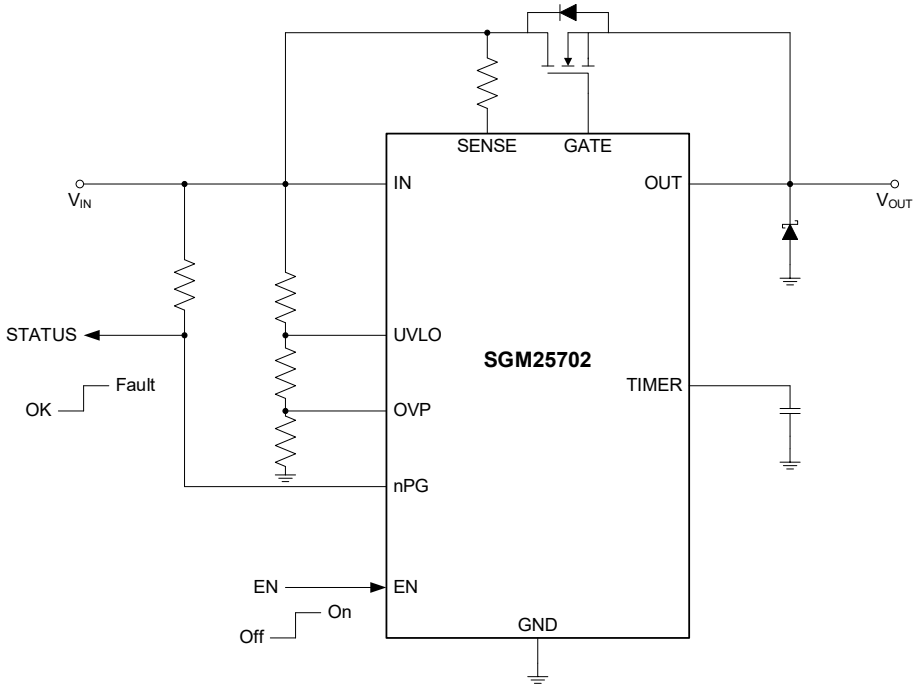


Figure 2. Basic Application Circuit

DETAILED DESCRIPTION (continued)

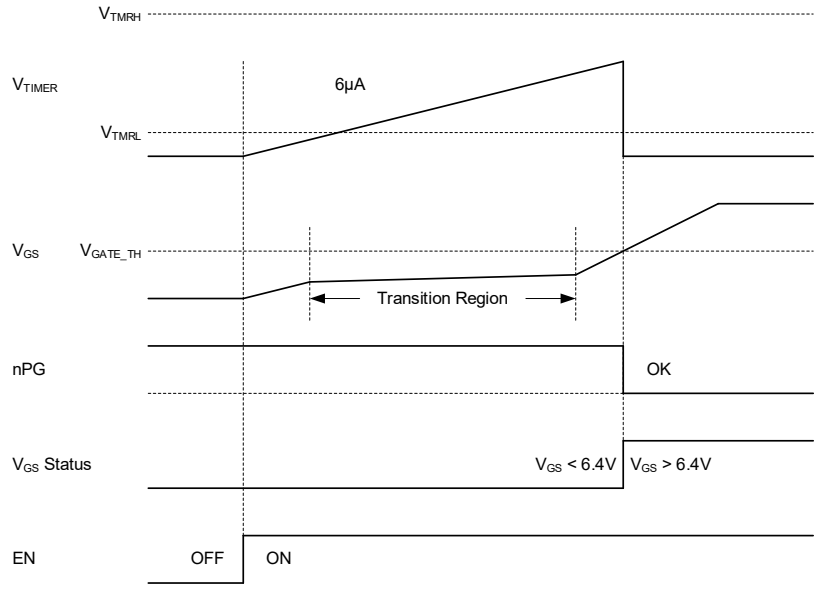


Figure 3. Voltages during Normal Start-Up Sequence

Gate Control

An internal charge pump can provide an internal bias higher than the output voltage to boost the gate of the N-MOSFET. The V_{GS} of external N-MOSFET is limited to 17.2V by an internal Zener diode. During normal operation, the GATE pin is charged to approximately 12.2V above the OUT pin by the internal 25μA current source. A pull-down current source of 2mA can prevent crosstalk caused by the drain-to-gate capacitance of N-MOSFET when UVLO or EN is low, thus avoiding misleading conduction.

The GATE pin is pulled down by the 60mA current source when the C_{TIMER} is charged up to threshold of 2V or an over-voltage fault is indicated by OVP voltage exceeding OVP_{TH} threshold.

Status Conditions

Output responses of the SGM25702 to various input conditions is shown in Table 1.

Table 1. Overview of Operating Conditions

INPUTS						OUTPUTS					STATUS
EN	UVLO	OVP (TYP)	VIN (TYP)	SENSE-OUT	GATE-OUT	IN Current (TYP)	GATE Current (TYP)	TIMER	GATE after TIMER > 2V	nPG	
L	L	-	> 5.1V	-	-	0.009mA	2mA Sink	Low	-	-	Disabled
L	H	-	> 5.1V	-	-	0.009mA	2mA Sink	Low	-	-	Disabled
H	L	< 2V	> 5.1V	SENSE > OUT	-	0.37mA	2mA Sink	Low	-	H	Standby
				SENSE < OUT						L	
H	L	> 2V	> 5.1V	SENSE > OUT	-	0.37mA	60mA Sink	Low	-	H	Standby
				SENSE < OUT						L	
H	H	< 2V	> 5.1V	SENSE > OUT	< 6.4V	0.34mA	25μA Source	6μA Source	60mA Sink	H	Enabled
				SENSE < OUT				Low	-	L	
H	H	< 2V	> 5.1V	SENSE > OUT	> 6.4V	0.34mA	25μA Source	11μA Source	60mA Sink	H	Enabled
				SENSE < OUT				Low	-	L	
H	H	> 2V	> 5.1V	SENSE > OUT	-	0.34mA	60mA Sink	Low	-	H	Over-Voltage
				SENSE < OUT						L	
H	H	< 2V	< 5.1V	-	-	0.34mA	2mA Sink	Low	-	H	Power-On Reset

DETAILED DESCRIPTION (continued)

Fault Timer

The fault waiting time can be set by the C_{TIMER}, which is connected between TIMER and GND, and the capacitor will be charged up to V_{TMRH} threshold to indicate a fault condition by internal current source. When a fault is indicated, the SGM25702 will turn off the N-MOSFET by discharging the GATE pin with a 60mA current source until the EN, UVLO or IN pin is power cycled.

There are 3 current sources to charge or discharge the timer capacitor. When EN, UVLO, and IN are all in high level, a constant 6μA (TYP) current source charging the TIMER pin is active. When the V_{GS} sequence has been completed, another constant 5μA (TYP) current source charging the TIMER pin is active, and the total charge current is 11μA (TYP). A 6mA pull-down current source is activated to discharge the timer capacitor and reset the timer when EN, UVLO, or IN pin is low, or when OVP is high. Note that when a V_{DS} fault is declared, the 6mA pull-down current source is disabled and the total charge current is 11μA (TYP) to set the fault waiting time. The timer capacitor voltage waveform during start-up is shown in Figure 3, Figure 4 and Figure 5.

An adequate timer capacitor should be selected to ensure the gate charging and output voltage rising completely, or the TIMER pin voltage will arrive the V_{TMRH} threshold prematurely and the SGM25702 will latch off.

It is not recommended to disable the timer function by connecting the TIMER pin to GND, although the nPG can still indicate the V_{DS} fault condition, because the TIMER pin voltage will never reach the threshold and the fault latch-off function is disabled.

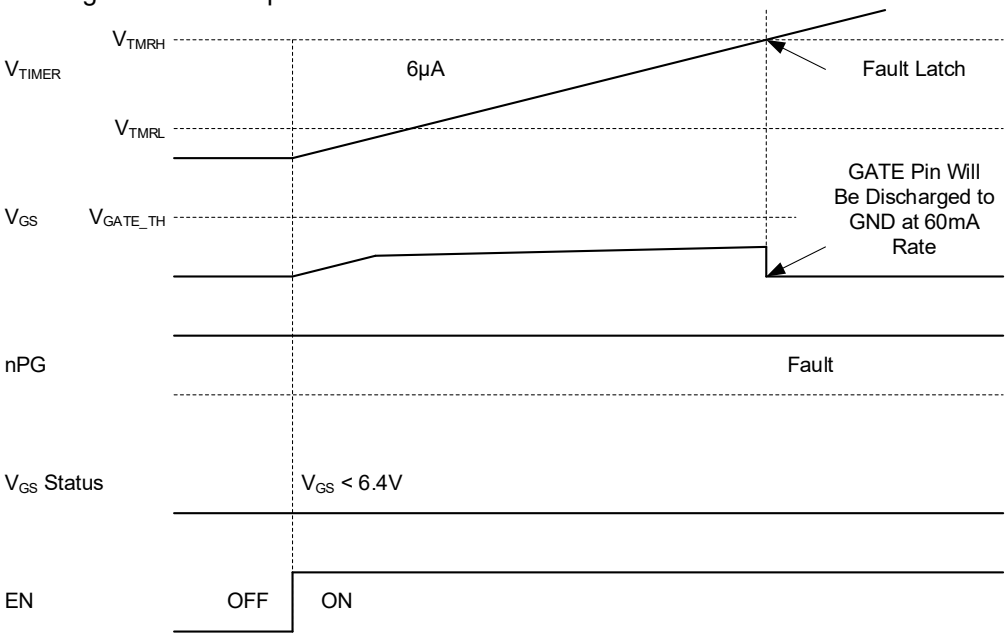


Figure 4. Voltages during Start-Up with V_{GS} Gate Leakage Condition

DETAILED DESCRIPTION (continued)

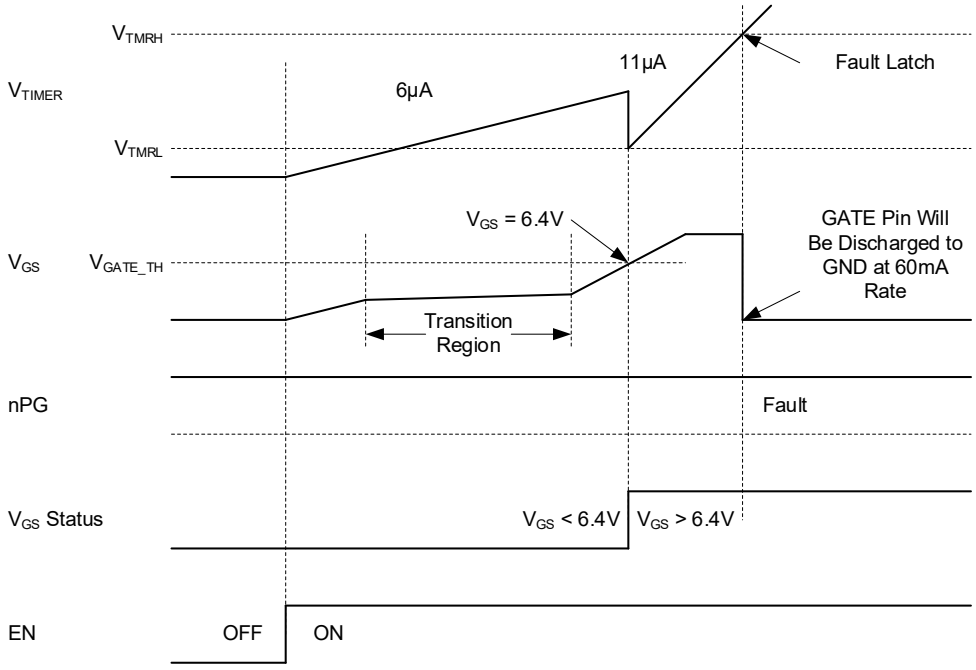


Figure 5. Voltages during Start-Up with V_{DS} Fault Condition

Restart

There are two different restart conditions including restart after over-current fault (V_{DS} fault) and restart after OVP event.

When a V_{DS} fault has been declared, the SGM25702 latches off and turns off the external N-MOSFET until the EN, UVLO or IN pin is toggled low and then high.

Another condition is the OVP function activated, the GATE and OUT pin has been pulled low. Since the timer capacitor is discharged and the SGM25702 will not latch off during an OVP event, the device will restart as mentioned in the start-up sequence once the OVP pin voltage falls below the lower threshold (1.76V, typically). The EN, UVLO or IN pin power cycle is not necessary to restart the external N-MOSFET.

V_{DS} Fault Condition

As mentioned above, the drain-to-source voltage (V_{DS}) of the N-MOSFET is indicated by the V_{DS} Comparator. When the SENSE voltage exceeds the OUT voltage, the V_{DS} comparator will trip and the open-drain output nPG will be in high-impedance state. Then the C_{TIMER} will be charged by either a 6μA (TYP) current source if the V_{GS} sequence is not completed or an 11μA (TYP) current source if the V_{GS} sequence is completed. As is shown in Figure 5, a V_{DS} fault occurs during start-up, where the nPG maintains high level due to the excessive V_{DS} voltage is detected by the V_{DS} comparator during the whole period.

Over-Current Detection

The over-current detection can be implemented by using the V_{DS} fault comparator. Since the comparator monitors the voltage difference between SENSE and OUT pins, the V_{DS} fault threshold is:

$$V_{DSTH} = (R_S \times I_{SENSE}) - V_{OFFSET} \quad (1)$$

The MOSFET drain-to-source current threshold is:

$$I_{DSTH} = \frac{V_{DSTH}}{R_{DSON}} \quad (2)$$

where

- R_{DSON} is the drain-to-source resistance of Q1 in Figure 8.
- V_{OFFSET} is the offset voltage of the V_{DS} comparator.
- I_{SENSE} (16μA TYP) is the threshold programming current.

DETAILED DESCRIPTION (continued)

Therefore, the over-current threshold of the external N-MOSFET can be set through the series resistance on the SENSE pin. During start-up, the chip allows the MOSFET to conduct excessive current within a certain time, which is jointly determined by the external C_{TIMER}, the source current of the TIMER and the fault threshold (V_{TMRH}). When the voltage of the C_{TIMER} arrives at the fault threshold (V_{TMRH}), the waiting time expires, and the gate is discharged at a 60mA rate.

The SGM25702 is recommended to be applied for the applications where the accurate current sensing is not necessary, and the inductance or impedance in the power path makes the current rise slowly in a short circuit condition.

Considering the external N-MOSFET needs to conduct the excessive current during the fault waiting time, it is necessary to carefully consider the Safe Operating Area (SOA) of the N-MOSFET. Besides, the value of the over-current threshold will be affected by the R_{DSON} variations.

Enable

The SGM25702 is suitable for the applications where the remote on/off control is needed. When the EN pin is forced low, the external N-MOSFET is remotely turned off. When the EN pin is forced high, the external N-MOSFET is remotely turned on. The threshold levels of the EN pin is shown in Figure 6.

A low quiescent current mode can be entered when EN pin falls below 0.5V (TYP), and the quiescent current of IN pin falls down to 7.3μA (TYP).

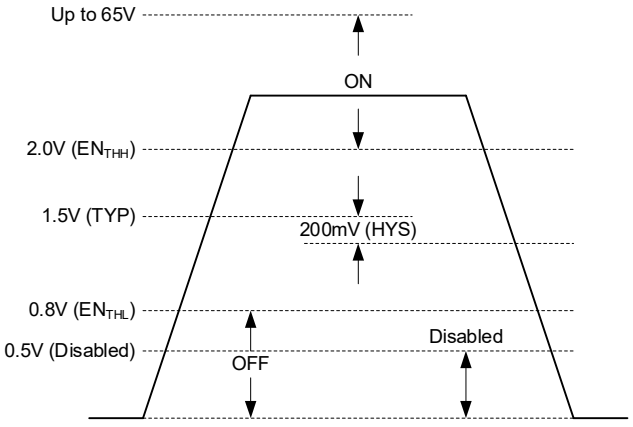


Figure 6. Enable Function Threshold Levels

UVLO

When the voltage of the UVLO pin falls below the threshold, the external N-MOSFET will be turned off with a 2mA (TYP) current sink at the GATE pin. The input voltage threshold can be adjusted by a resistor divider as shown in Figure 2. Besides, the UVLO pin can also be used as a redundant, or secondary EN remote control without a quite low quiescent current off mode.

It is suggested to connect the UVLO pin to the IN pin if the UVLO function is not needed rather than leave the UVLO pin floating, because an internal pull-down exists in the UVLO pin. In addition, there is an additional Power-On Reset (POR) whose threshold is typically 5.1V to monitor the input voltage.

OVP

When the voltage of the OVP pin rises above the OVP_{TH} threshold (2.0V TYP) lasting longer than typically 12μs, the external N-MOSFET will be turned off with a 60mA (TYP) current sink at the GATE pin, and the C_{TIMER} will be discharged. The input OVP threshold can be adjusted by a resistor divider as shown in Figure 2. It is suggested to connect the OVP pin to GND if the OVP function is not needed rather than leave the OVP pin floating.

nPG Indication

The nPG pin is an open-drain output pin to indicate a V_{DS} fault condition. The nPG pin will be high impedance when the over-current fault is detected. As is shown in Figure 2, the nPG pin voltage will be high during a V_{DS} fault condition, regardless of the fault timer function. It is recommended that the pull-up resistance should be large enough to limit the sink current below 5mA during the nPG pin low state.

APPLICATION INFORMATION

This section introduces three applications, including SGM25702 demo board design, reverse polarity protection and reverse current blocking.

SGM25702 Demo Board Design

This section illustrates the design process for the normal applications using SGM25702. The schematic of the SGM25702 demo board is shown in Figure 7.

Application Circuit

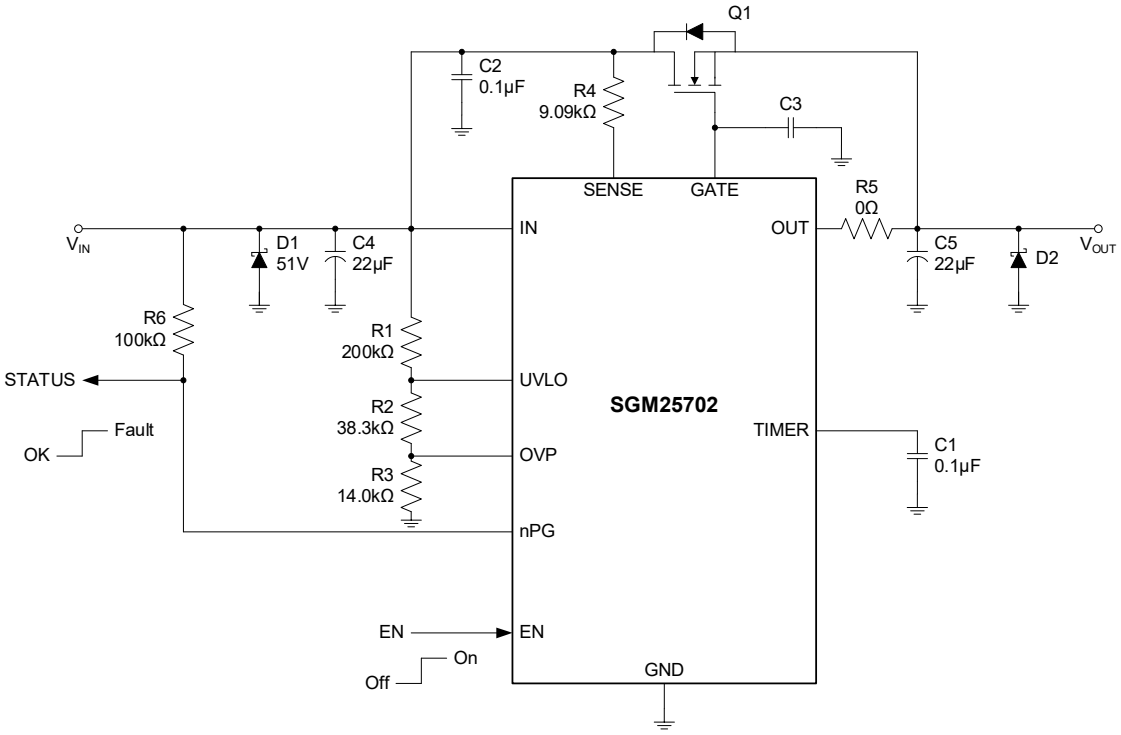


Figure 7. Schematic Diagram

Design Requirements

Table 2 shows the design specifications of the SGM25702 demo board.

Table 2. Example Number 1 Circuit Specifications

DESIGN PARAMETER	EXAMPLE VALUE
Maximum Input Voltage (OVP)	37V
Minimum Input Voltage (UVLO)	9V
Output Current Range	0A to 5A
Ambient Temperature Range	0℃ to 50℃

Selecting Sense Pin Series Resistor R_S

As described in the section Over-Current Detection and Figure 8, the appropriate SENSE pin resistor R_S can be selected based on the desired over-current threshold and R_{DSON} of the external N-MOSFET.

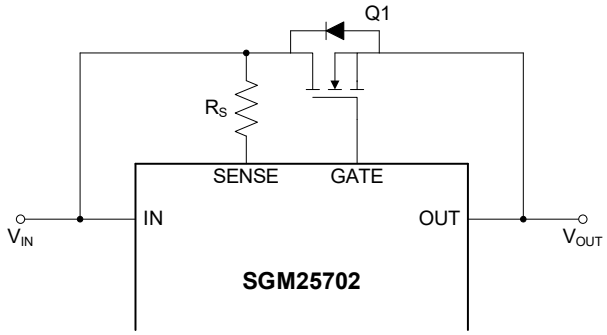


Figure 8. Setting the V_{DS} Threshold

APPLICATION INFORMATION (continued)

Output Rise Time

In applications where there is a large output capacitor or downstream load that is sensitive to the output voltage, the rise time of the output voltage can be slowed down by placing a capacitor between GATE and GND. The output rise time is determined by the threshold level of the MOSFET, the gate capacitance of the MOSFET, and the external capacitance between GATE and GND shown in Figure 9. It is necessary to carefully consider the Safe Operating Area (SOA) of the MOSFET if it slowly turns on, or the power losses may damage the device.

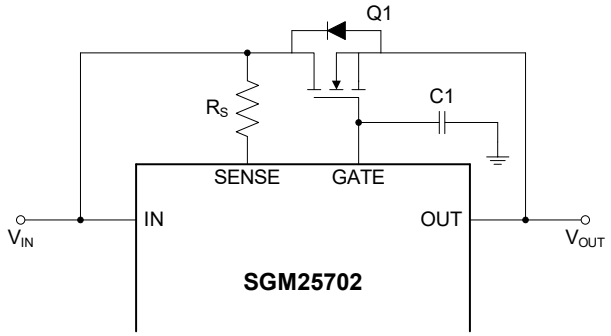


Figure 9. Turn-On Time Extension

Fault Detection Waiting Time

In order to provide sufficient start-up time for MOSFET and enable MOSFET to conduct current exceeding the over-current threshold in a short period of time, SGM25702 provides a fault detection waiting time function, which makes SGM25702 suitable for applications such as lamps and motors that may require a certain amount of surge current during start-up or normal operation. The waiting time for the V_{GS} detection or the over-current detection can be set through a low leakage capacitor C_{TIMER} connected between TIMER and GND.

When the SGM25702 enters the normal operating state, the internal charge pump will be turned on to provide a constant 25μA current source to the gate of the external MOSFET. Meanwhile, the C_{TIMER} will be charged by a constant current source of 6μA.

Before the V_{GS} voltage reaches the 6.4V threshold (V_{GATE_TH}), the V_{DS} start-up fault waiting time can be calculated according to the following formula.

$$V_{DS}\ \text{Fault Waiting Time} = \frac{V_{TMRH} \times C_{TIMER}}{I_{TMRL}} \quad (3)$$

Where the I_{TMRL} is typically 6μA and V_{TMRH} is typically 2V.

The TIMER pin is pulled low to 0.3V by internal 6mA current source when the gate-to-source voltage (V_{GS}) reaches the V_{GATE_TH} threshold (6.4V TYP) before the C_{TIMER} voltage value reaches 2V. It means the V_{GS} sequence is completed, and the internal 5μA current source is enabled, and the total C_{TIMER} charge current is increased to 11μA (TYP) while the GATE pin is still charged by the 25μA current source. After the V_{GS} sequence ends, the external MOSFET may still not be fully conductive, so additional time is required to wait for the V_{GS} to charge to a higher voltage. If the V_{DS} voltage of the external MOSFET continues to exceed the threshold, causing the timer capacitor voltage to exceed the threshold V_{TMRH}, the chip will latch off.

After the V_{GS} voltage reaches the 6.4V threshold (V_{GATE_TH}), the V_{DS} transition fault waiting time can be calculated according to the following formula.

$$V_{DS}\ \text{Fault Waiting Time} = \frac{(V_{TMRH} - V_{TMRL}) \times C_{TIMER}}{I_{TMRH}} \quad (4)$$

Where the I_{TMRH} is typically 11μA, V_{TMRH} is typically 2V and V_{TMRL} is typically 300mV.

APPLICATION INFORMATION (continued)

If the surge current of the load exceeds the over-current threshold, the current source used to discharge the timer capacitor is disabled, and the 11μA current source charges the timer capacitor. When the surge current lasts long enough to charge the timer capacitor to the threshold (V_{TMRH}) of 2V, the device will immediately latch off. The V_{DS} fault waiting time can be calculated via the following formula.

$$V_{DS}\ \text{Fault Waiting Time} = \frac{V_{TMRH} \times C_{TIMER}}{I_{TMRH}} \quad (5)$$

Where the I_{TMRH} is typically 11μA and V_{TMRH} is typically 2V.

As mentioned above, since only one single capacitor is used to set the delay time for multiple faults, some trade-offs should be required between the desired waiting time and the actual waiting time.

MOSFET Selection

The selection of external MOSFET should consider the following aspects:

1. BVDSS should be greater than the maximum input voltage of the system and leave a certain margin to cope with voltage ringing caused by line or load transients.

2. The maximum drain current of MOSFET should be greater than the over-current threshold set by the SENSE series resistor.

3. It is recommended to choose MOSFET with lower threshold voltages, which reaches ohmic region sooner under the same gate capacitance conditions, thereby keep MOSFET operating within SOA during start-up.

4. It is necessary to carefully consider the SOA and thermal characteristics of MOSFET at maximum power consumption possible during start-up and shutdown period.

5. Try to keep the R_{DSON} as small as possible to avoid excessive temperature rise. It recommends a steady state of less than +125℃ for MOSFET.

6. If the maximum rated V_{GS} of the selected external MOSFET is less than 16V, a Zener diode must be placed between the gate and source to clamp V_{GS}. In addition, the forward current rating of the external Zener diode should exceed 60mA to meet the requirement of conducting pull-down current under fault conditions.

Input and Output Capacitors

In an ideal situation, input and output capacitors are not necessary. However, in practical situations, parasitic inductance is inevitable in power circuits, mainly caused by the routing of wires and printed circuit boards. All trace inductance can cause positive spikes on the input side and negative spikes on the output side when the MOSFET rapidly turns off. Therefore, it is necessary to use capacitors or clamp circuits at the input and output terminals to limit the impact of these voltage spikes. The selection of capacitor value is mainly related to the input voltage level, load current level, trace parasitic inductance and MOSFET switching speed. Besides, it is necessary to place a bypass capacitor between IN and GND in order to filter noise and voltage spikes.

Considering the difficulty in accurately predicting the value of trace parasitic inductance, optimizing the layout of the circuit board and carefully evaluation are effective methods for determining appropriate input or output capacitance values or clamp circuits.

UVLO and OVP

UVLO and OVP can both be used to detect whether the input voltage is within a suitable operating range through resistor dividers. When the input voltage is too low, the voltage at the UVLO pin is below the threshold, which will cause the MOSFET to be turned off by the 2mA current sink at the GATE pin. The UVLO threshold has a hysteresis of 180mV. When the input voltage is too high, the voltage at the OVP pin is higher than the threshold, which will cause the MOSFET to be turned off by the 60mA current sink at the GATE pin. The OVP threshold has a hysteresis of 240mV.

There are several ways to set the under-voltage and over-voltage thresholds for the input voltage. The first method, as shown in Figure 10, sets the threshold through three resistors. The second method, as shown in Figure 11, adjusts the UVLO and OVP thresholds separately through two resistor dividers. Another way is to ground the OVP to disable its function.

APPLICATION INFORMATION (continued)

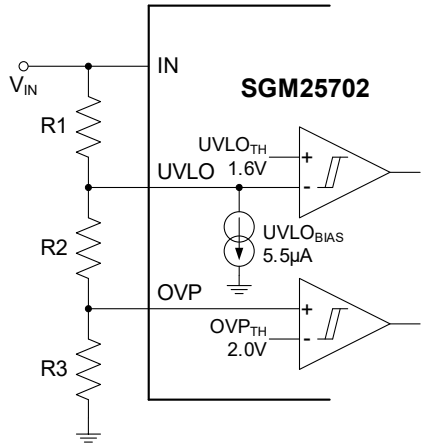


Figure 10. UVLO and OVP Thresholds Set by R1, R2 and R3

Here are the design procedures for separately setting UVLO and OVP thresholds as shown in Figure 11.

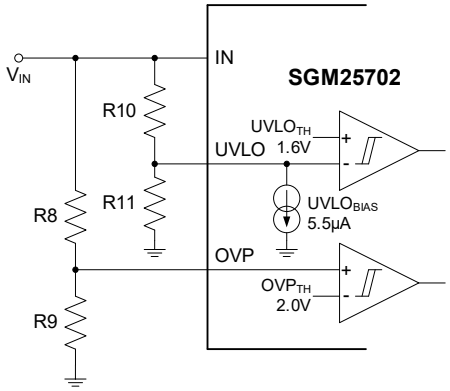


Figure 11. Programming the Thresholds with Resistors R8-R11

1. Select the rising threshold for UVLO and ensure that the device can still operate normally under the minimum required input voltage conditions. It is recommended to choose a resistor lower than 100kΩ for R11, as a smaller resistor is beneficial for improving immunity to $UVLO_{BIAS}$. The value of R10 can be calculated according to Equation 6. All other variables can be found in the Electrical Characteristics table of this document.

$$R10 = \frac{V_{INMIN} - UVLO_{TH}}{(UVLO_{BIAS} + \frac{UVLO_{TH}}{R11})} \quad (6)$$

2. As for the calculation of the falling threshold of UVLO, it can be obtained by replacing $UVLO_{TH}$ in Equation 6 with ($UVLO_{TH}$ - $UVLO_{HYS}$).

3. Select the falling threshold for OVP and ensure that the device can still operate normally under the maximum required input voltage conditions. It is recommended to choose a resistor lower than 100kΩ for R9. The value of R8 can be calculated according to Equation 7. All other variables can be found in the Electrical Characteristics table of this document.

$$R8 = R9 \times (\frac{V_{INMAX} - OVP_{TH}}{OVP_{TH}}) \quad (7)$$

4. As for the calculation of the falling threshold of OVP, it can be obtained by replacing OVP_{TH} in Equation 7 with (OVP_{TH} - OVP_{HYS}).

Therefore, the maximum and minimum rising values of IN can be calculated using the following equations after values of R9-R11 are determined.

$$V_{INMAX} = OVP_{TH} + \frac{R8 \times OVP_{TH}}{R9} \quad (8)$$

$$V_{INMIN} = UVLO_{TH} + \left[R10 \times (UVLO_{BIAS} + \frac{UVLO_{TH}}{R11}) \right] \quad (9)$$

Similarly, the falling threshold which including the hysteresis can be calculated by replacing $UVLO_{TH}$ in Equation 6 with ($UVLO_{TH}$ - $UVLO_{HYS}$) and OVP_{TH} in Equation 7 with (OVP_{TH} - OVP_{HYS}).

APPLICATION INFORMATION (continued)

Power Good Indicator

When nPG is in a logic low state, it is recommended to limit the current into the pin through a pull-up resistor within the range of 1mA to 5mA. As shown in Figure 12, the pull-up resistor R4 is connected between IN and nPG. In fact, any positive voltage not exceeding 65V can be used as a pull-up power supply.

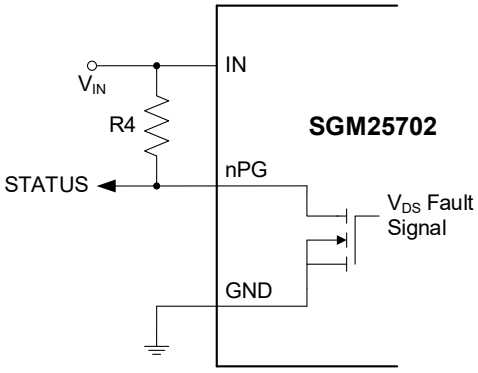


Figure 12. Circuitry at the nPG Pin

Light Load with Large Load Capacitor

Assuming a scenario where a large output capacitor is connected in parallel with a light load, if the device latches off due to a fault, there is a 60mA current sink inside the GATE pin. Due to the light load or high impedance load path, the charge on the load capacitor is mostly dissipated internally by SGM25702, as shown in Figure 13. The power dissipated by SGM25702 in this scenario can be calculated according to the following equation.

$$P = I_{GATE\_FLT} \times V_{OUT} \quad (10)$$

Where the I_{GATE_FLT} is the sink current of the SGM25702 gate control.

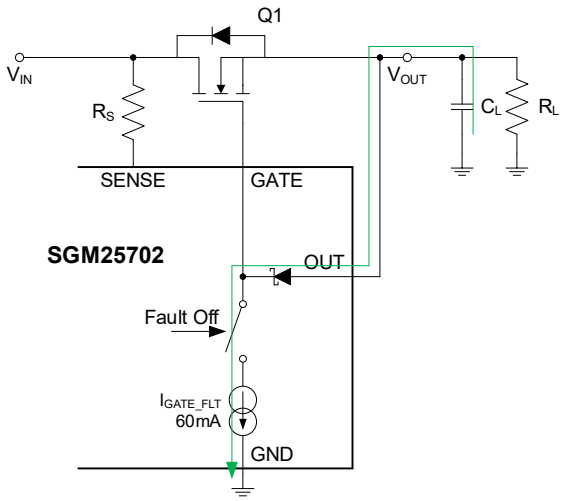


Figure 13. Discharge Path of Possible Load Capacitor

If the limit of the discharge current on the load capacitor is needed, you can connect a discharge resistor R_O in series with the OUT pin, as shown in Figure 14. However, it should be noted that this resistor will affect the over-current threshold, so the value of R_S needs to be adjusted with the change of R_O. For more information on the calculation procedures and precautions of R_O, R_S, and over-current threshold, please refer to Reverse Polarity Protection section.

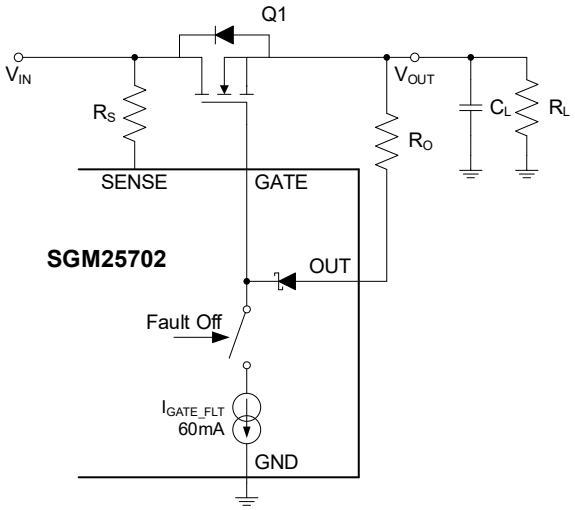
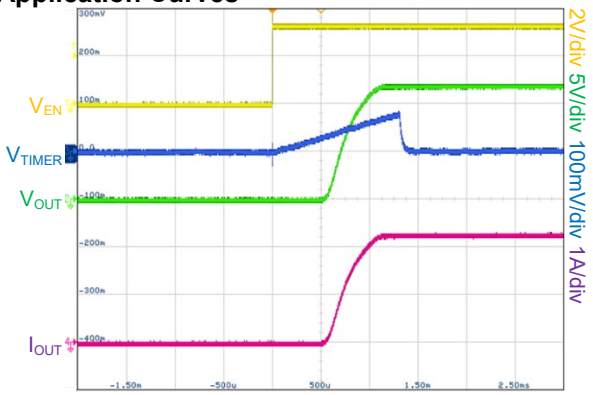


Figure 14. Current Limiting Resistor R_O for Special Cases

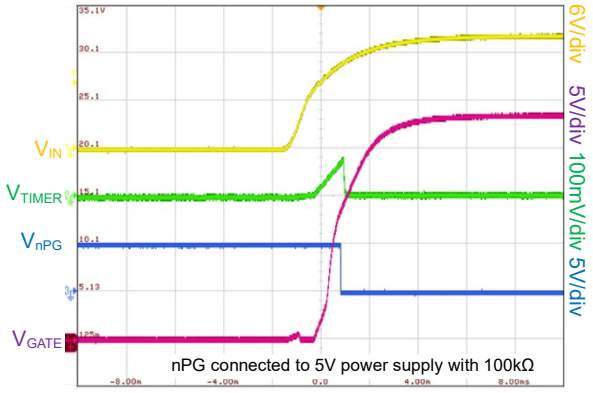
APPLICATION INFORMATION (continued)

Application Curves



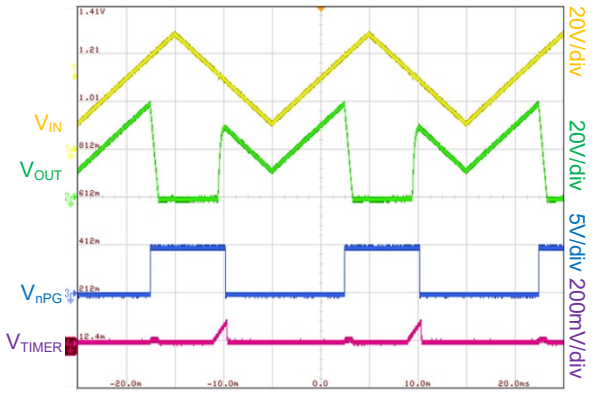
Time (500μs/div)

Figure 15. Start-Up Waveform



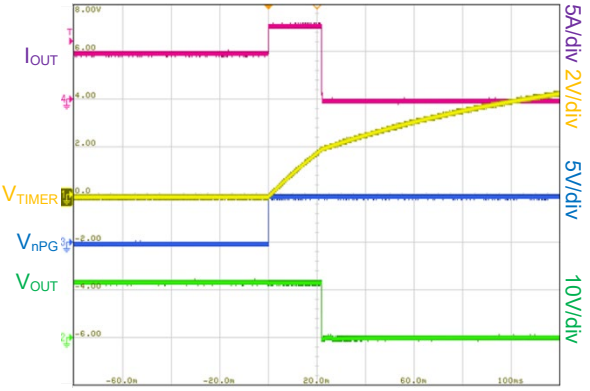
Time (2ms/div)

Figure 16. Start-Up Waveform



Time (5ms/div)

Figure 17. OVP Behavior



Time (20ms/div)

Figure 18. Fault Behavior

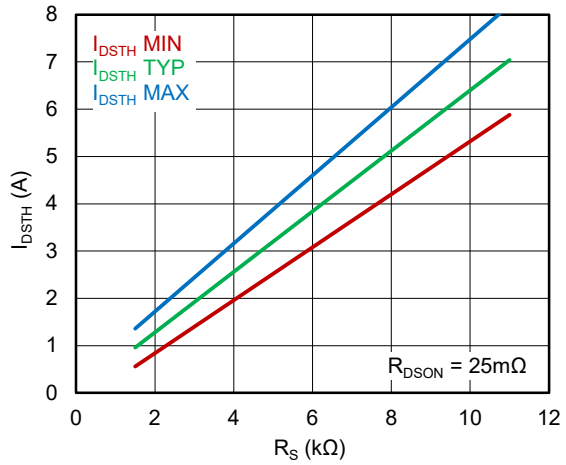


Figure 19. I_{DSTH} vs. R_S for R_{DSON} = 25mΩ

APPLICATION INFORMATION (continued)

Reverse Polarity Protection

This section illustrates the principle and application curve of the reverse polarity protection using SGM25702.

Application Circuit

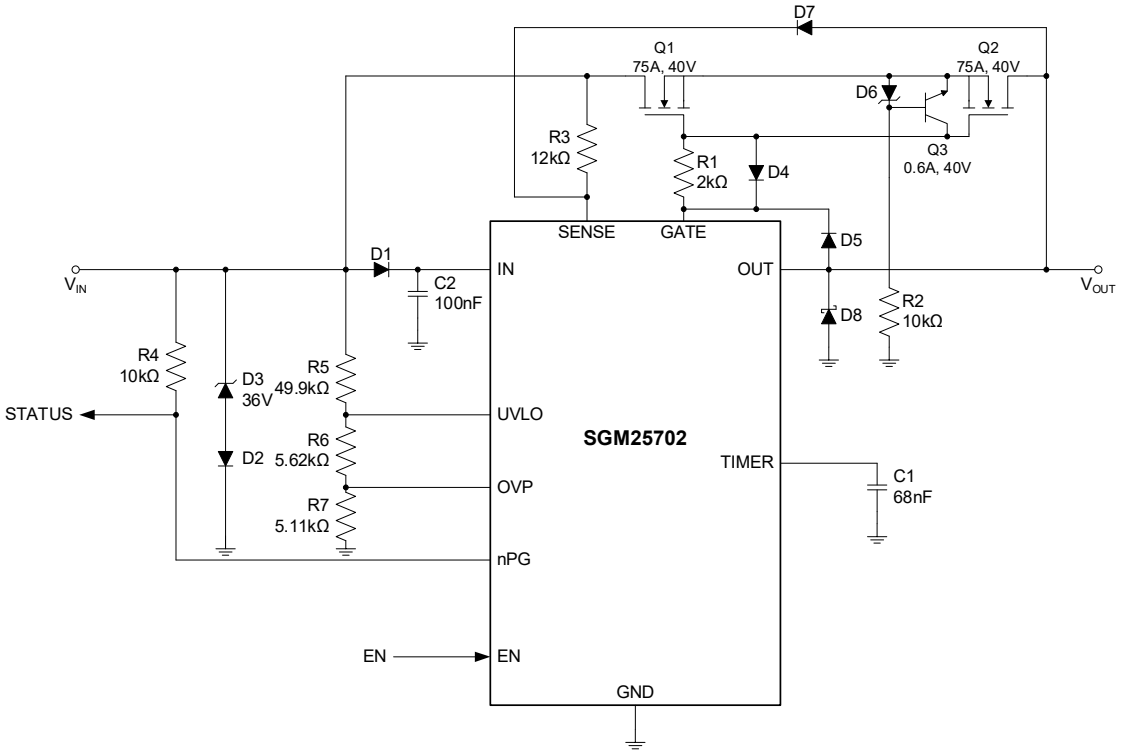


Figure 20. Application with Reverse Polarity Protection with Diodes for OUT Pin Protection

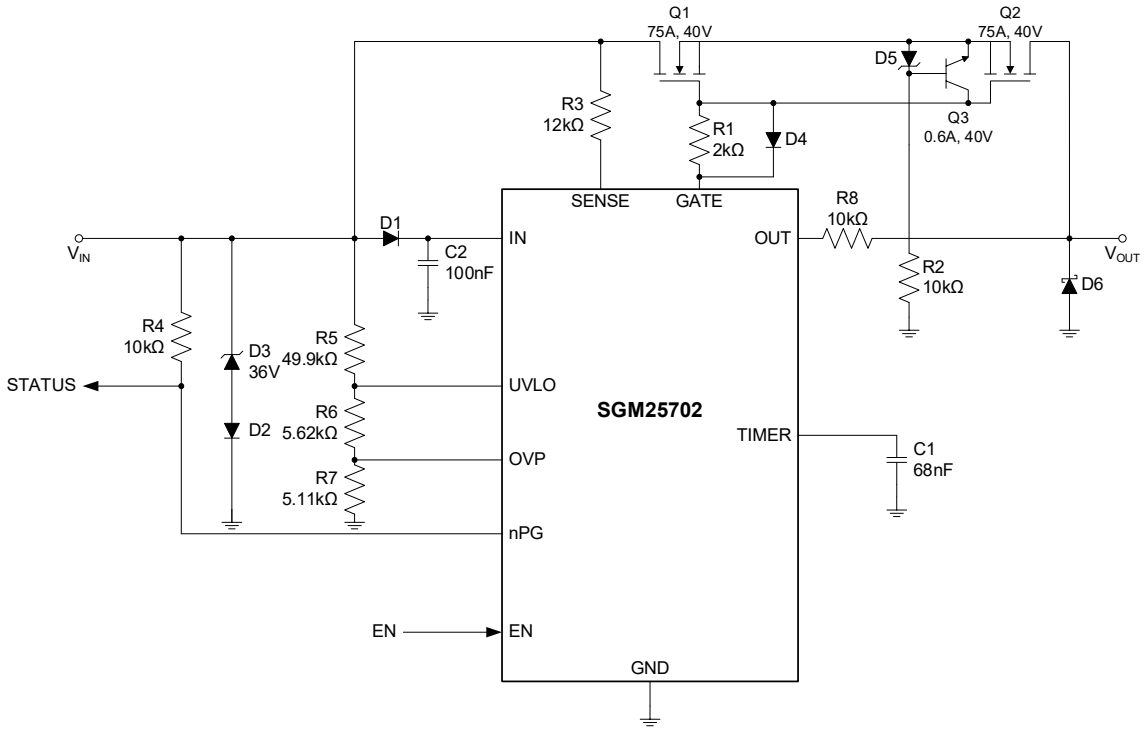


Figure 21. Application with Reverse Polarity Protection with a Resistor for OUT Pin Protection

APPLICATION INFORMATION (continued)

Figure 20 and Figure 21 respectively show the reverse polarity protection, which is important in industrial applications, function achieved by SGM25702 using diodes and resistors.

In Figure 20, two MOSFETs of Q1 and Q2, whose sources are connected, are used to avoid reverse current in a IN reverse polarity condition. Zener diode D3 is used to protect the device from input voltage transient damage caused by the quickly turn off of MOSFET. When the input capacitance is large enough to absorb voltage transients, D3 can be ignored. To avoid the conduction of D3 in the case of input reverse polarity, D3 can be connected in series with a diode D2. Diode D1 is used to protect the IN pin and prevent reverse current through the ESD diode. The resistor R1 is used to protect the GATE pin. Due to the constant current source inside GATE is active when Q1 and Q2 are turned on, R1 will not affect the turn-on speed of MOSFET. In order to avoid R1 slowing down the shutdown speed when Q1 and Q2 are shut down due to faults, an additional D5 is used to bypass current limiting resistor R1. D6, Q3 and R2 protect Q2 from V_{GS} damage in the event of reverse input polarity. Diodes D5 and D7 protect the Zener diode inside SGM25702 when the output load is a large capacitor.

Another reverse polarity protection circuit is shown in Figure 21, which uses resistors instead of diodes to implement reverse polarity protection.

The design procedures of reverse polarity protection circuit with diodes shown in Figure 20 are almost the same with SGM25702 Demo Board Design section. However, the design procedures of reverse polarity protection circuit with resistors is more complicated because of the existence of R8.

The following section will demonstrate the design procedures of a protection circuit using the resistance scheme shown in Figure 21.

Design Requirements

The design requirements of the reverse polarity protection circuit with resistors are shown in Table 3.

Table 3. Application Specifications

DESIGN PARAMETER	EXAMPLE VALUE
Operating Voltage Range	9V to 24V
Current MAX	30A
OVP Setting	27V TYP
UVLO Setting	9V TYP

Current Limiting Resistors in Reverse Polarity Protection

As mentioned above, adding a resistor at OUT pin can not only limit the current flowing through the diode between OUT and GATE but also the current flowing through the diode between OUT and SENSE. However, the appearance of OUT pin resistor will require modification of SENSE pin resistor to ensure the accuracy of over-current threshold. The selection of OUT pin resistors is mainly based on limiting the current flowing through the diode of the V_{DS} comparator to no more than 4mA. The simplified internal circuit is shown in Figure 22, where the internal current source of 8μA and 16μA can be ignored for simplified analysis.

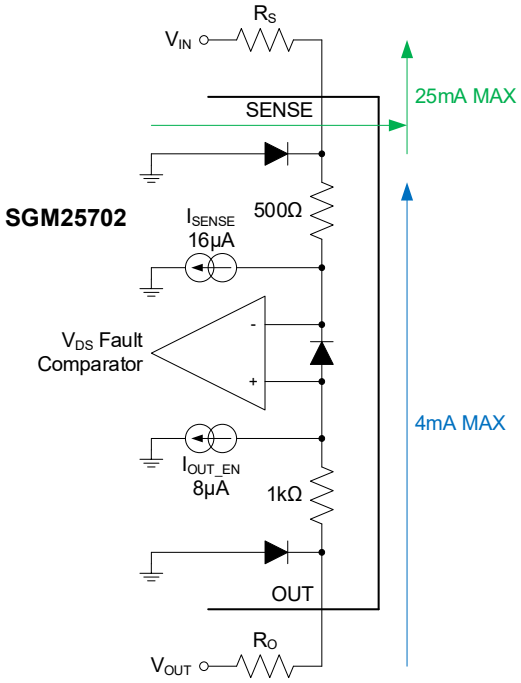


Figure 22. Current Limiting Resistor for Negative SENSE Condition

Case 1: $V_{OUT} > V_{IN}$, and V_{IN} is in reverse polarity. Due to V_{IN} being negative and SENSE pin being pulled up to near GND by an internal diode, the OUT pin resistor can be calculated as shown in Equation 11.

$$R_{O(MIN)} = \frac{V_{OUT} - (4mA \times 1.5k\Omega)}{4mA} \quad (11)$$

APPLICATION INFORMATION (continued)

In addition, the reverse current flowing out of the SENSE pin needs to be limited to below 25mA, so the minimum value of the SENSE pin resistor can be derived as follows.

$$R_{S(MIN)} = \frac{V_{IN}}{25mA} \quad (12)$$

Case 2: $V_{OUT} > V_{IN}$, and V_{IN} is positive, which is shown in Figure 23. The OUT pin resistor can be calculated as shown in Equation 13. Note that OUT, SENSE and IN pin voltage should not exceed 65V.

$$R_{O(MIN)} = \frac{(V_{OUT} - V_{IN})}{4mA} - (R_S + 1.5k\Omega) \quad (13)$$

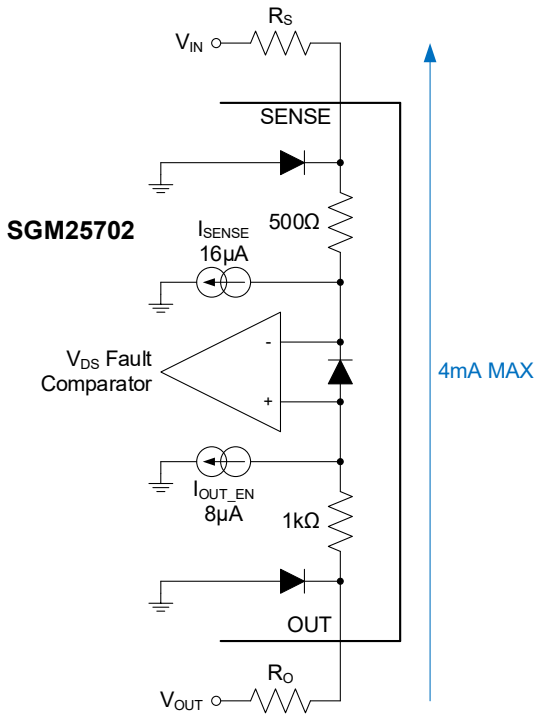


Figure 23. Current Limiting Resistor in the OUT Path for OUT > SENSE Condition

Case 3: $V_{OUT} < V_{IN}$, and V_{OUT} is positive. This is a normal working state, so there is no risk of excessive current in the OUT pin. Note that OUT, SENSE and IN pin voltage should not exceed 65V.

Case 4: $V_{OUT} < V_{IN}$, V_{OUT} is negative and V_{IN} is positive, which is shown in Figure 24. Due to V_{OUT} being negative and OUT pin being pulled up to near GND by an internal diode, the OUT pin resistor can be calculated as shown in Equation 14.

$$R_{O(MIN)} = \frac{V_{OUT}}{25mA} \quad (14)$$

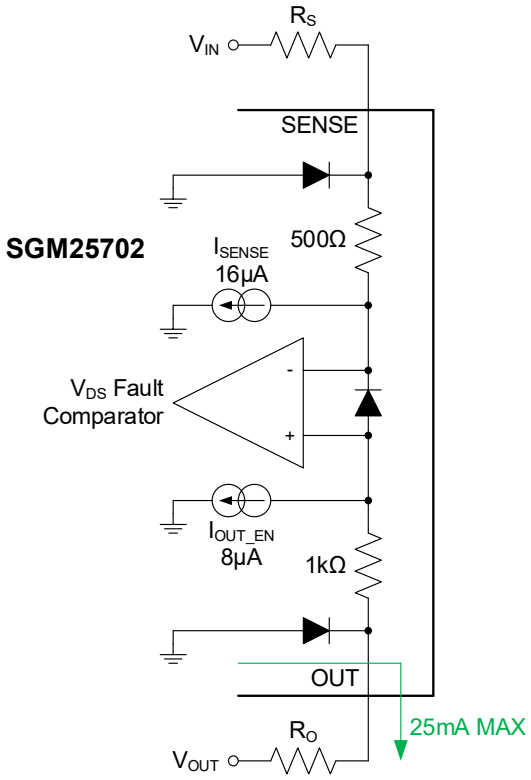


Figure 24. Current Limiting Resistor for Negative OUT Conditions

APPLICATION INFORMATION (continued)

V_{DS} Fault Detection with R_O and R_S

As mentioned several times before, when the OUT pin resistor R_O is present, R_S needs to be modified in order to obtain the desired V_{DS} fault threshold V_{DSTH}, which is the drain-to-source voltage threshold of the external MOSFET. The following equation is the resistance value of R_S calculated based on the voltage drop on R_O and the desired V_{DSTH}.

$$R_S = \frac{V_{DSTH}}{I_{SENSE}} + \frac{R_O \times I_{OUT\_EN}}{I_{SENSE}} - \frac{V_{OFFSET}}{I_{SENSE}} \quad (15)$$

Where, V_{OFFSET} means the offset voltage between OUT and SENSE, I_{SENSE} is the SENSE pin bias current (16μA TYP) and the I_{OUT_EN} is the OUT pin bias current (8μA TYP). Once the R_S and R_O are selected, the V_{DSTH} can be calculated as follows.

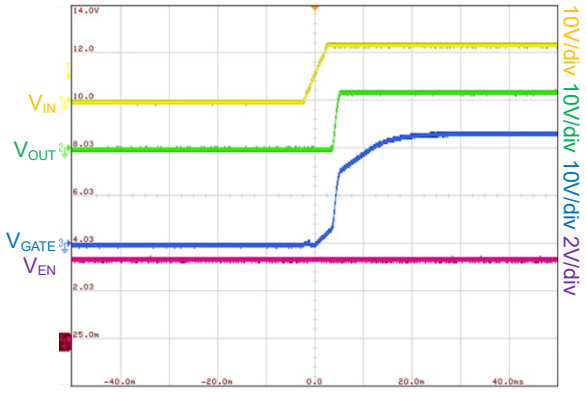
$$V_{DSTH} = I_{SENSE} \times (R_S - \frac{R_O}{I_{RATIO}}) + V_{OFFSET} \quad (16)$$

Thus, the threshold of MOSFET current flowing from drain-to-source can be obtained by R_{DSON} of MOSFET as Equation 17.

$$I_{DSTH} = \frac{V_{DSTH}}{R_{DSON}} \quad (17)$$

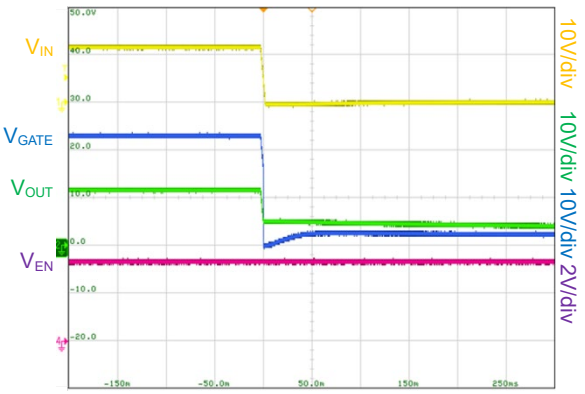
Application Curves

Note that all the curves are based on the reverse polarity protection circuit with resistors shown in Figure 21.



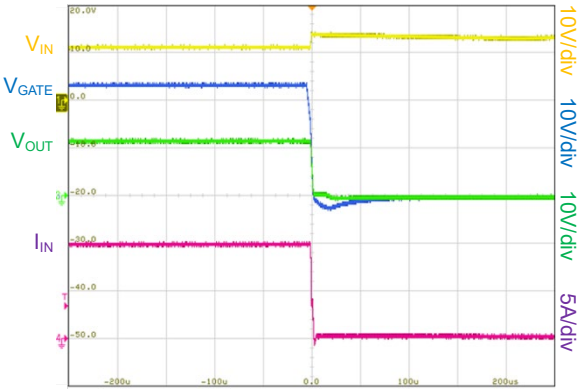
Time (10ms/div)

Figure 25. Start-Up at No Load



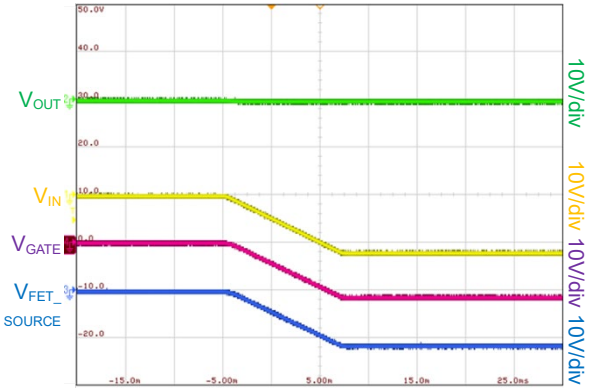
Time (50ms/div)

Figure 26. Shutdown



Time (50μs/div)

Figure 27. Over-Current Shutdown with Gate Diode



Time (5ms/div)

Figure 28. Reverse Input Voltage Polarity

APPLICATION INFORMATION (continued)

Reverse Current Blocking

This section illustrates the principle and application curves of the reverse current blocking using SGM25702.

Application Circuit

As shown in Figure 29, the reverse current blocking function can be implemented by a circuit similar to reverse polarity protection circuit. The main difference is that R2 is connected between the base of Q3 and OUT instead of GND. Note that the reverse current blocking function is active only when SGM25702 is shut down (EN = low).

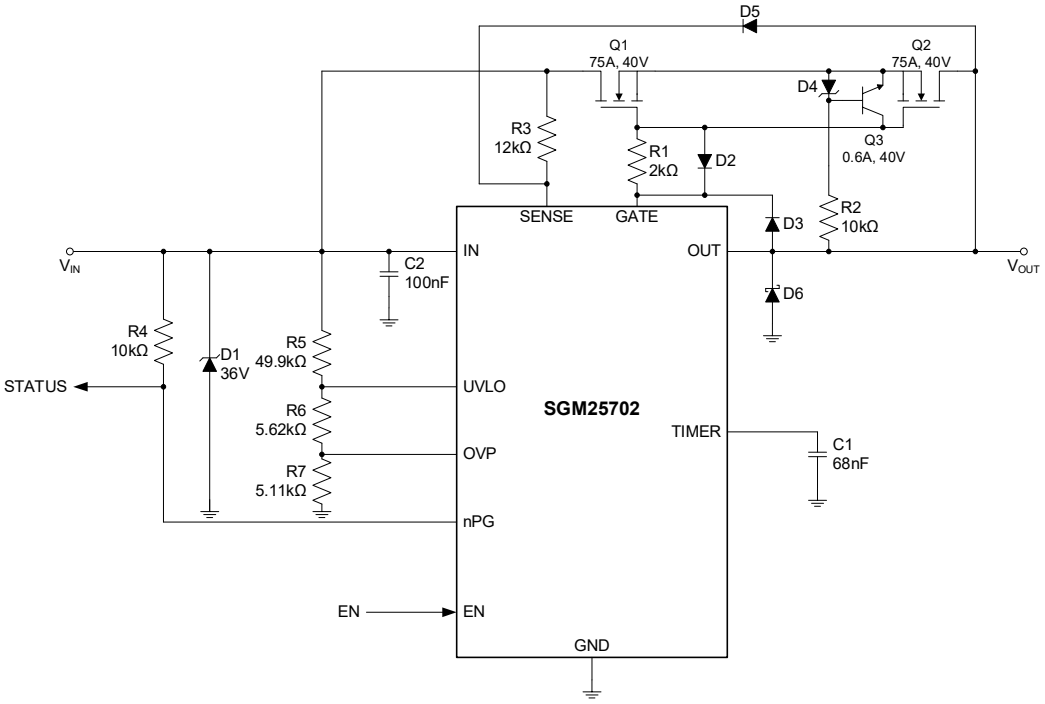


Figure 29. Application Circuit with Reverse Current Blocking Implemented by Diodes

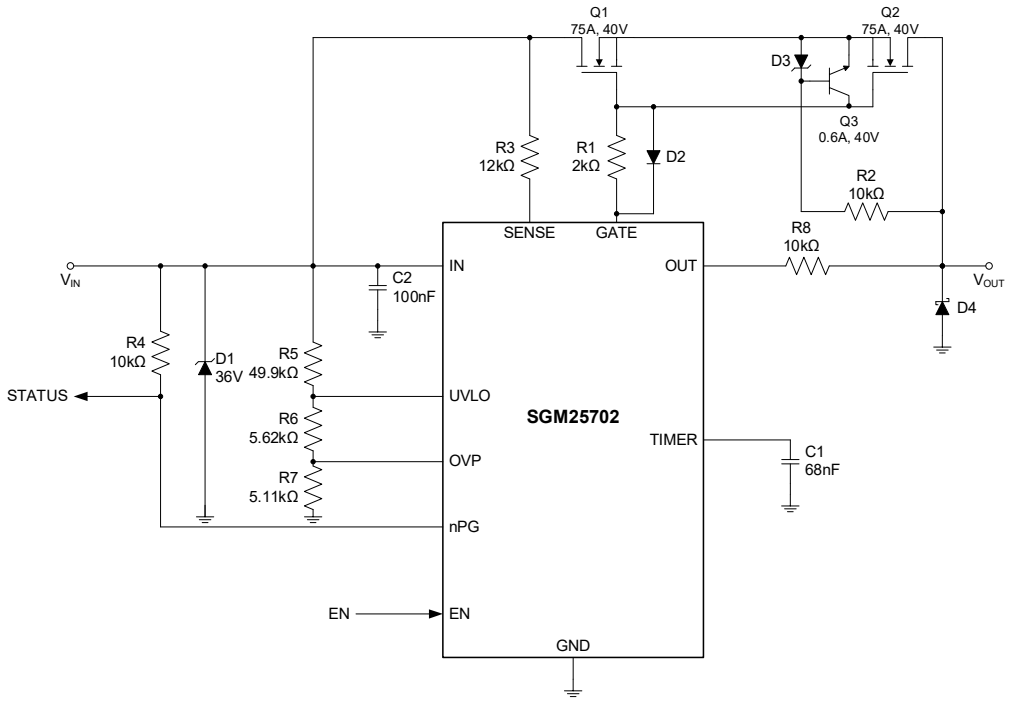


Figure 30. Application Circuit with Reverse Current Blocking implemented by resistors

APPLICATION INFORMATION (continued)

Application Curve

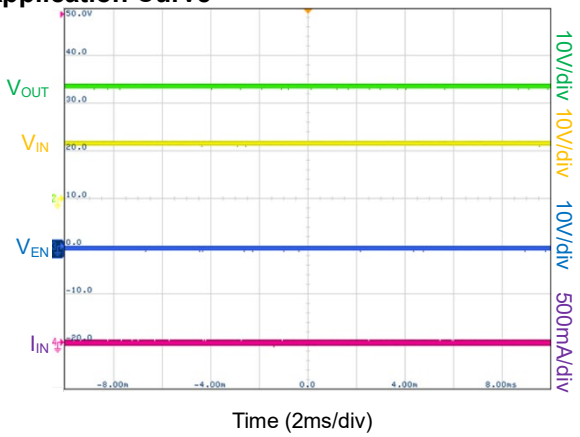


Figure 31. Reverse Current Blocking

Power Supply Recommendations

Generally speaking, SGM25702 can provide stable power supply with reliable performance. It is recommended to place a capacitor of 10nF or 100nF near the IN pin, in order to keep the SGM25702 operation stable.

System Considerations

If the input capacitor is not large enough, TVS needs to be placed in the input to prevent large voltage generated during voltage transient from exceeding the maximum rated value of IN pin.

When the output of SGM25702 is inductive load, it is necessary to reverse parallel diode on the load side. When the load is cut off, a flowing path is provided for the current of the inductive load to prevent negative voltage on OUT pin from damaging the device.

Layout Guidelines

SGM25702 should observe the following principles during PCB layout:

- The bypass capacitor of IN should be placed as close as possible to IN pin.
- The TIMER capacitor should be placed as close as possible to TIMER pin.
- The current path and return path from the input to the load side should be parallel and close to each other to reduce the loop inductance.
- GND of components around SGM25702 can be connected with each other and connected with GND pin of SGM25702. Then connect GND to the system ground uniformly. Do not separately connect the ground of the devices around the chip to the ground of the system with high current.

PCB layout provides good heat dissipation conditions for MOSFET to reduce the junction temperature when it is turned on and off.

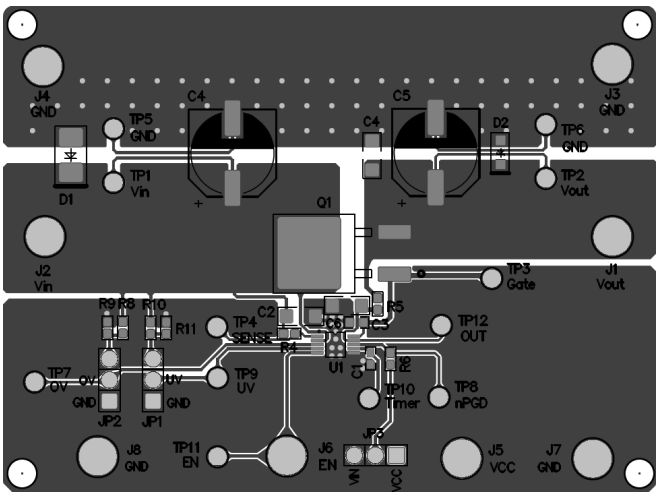


Figure 32. Top Layer

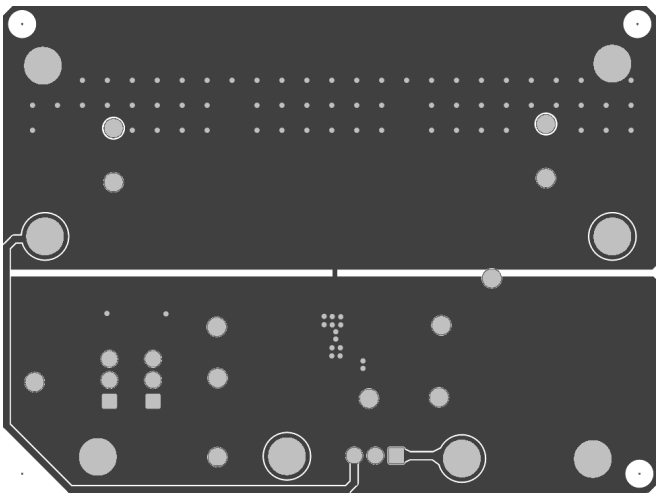


Figure 33. Bottom Layer

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

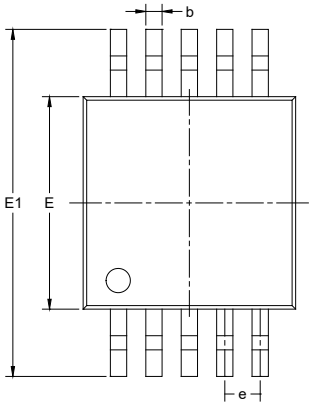
MAY 2025 – REV.A.1 to REV.A.2	Page
Updated Absolute Maximum Ratings, Recommended Operating Conditions, Electrical Characteristics and Typical Performance Characteristics	2, 5, 6, 7, 8, 9

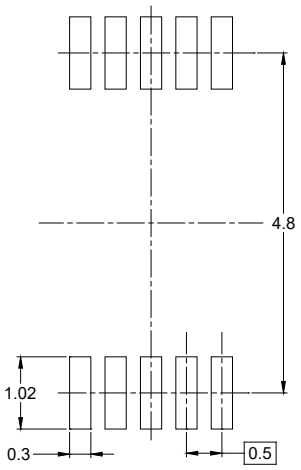
APRIL 2025 – REV.A to REV.A.1	Page
Updated Detailed Description and Application Information	11, 12, 14, 19, 20, 22, 24, 26

Changes from Original (DECEMBER 2024) to REV.A	Page
Changed from product preview to production data	All

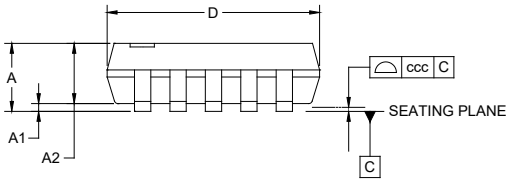
PACKAGE OUTLINE DIMENSIONS

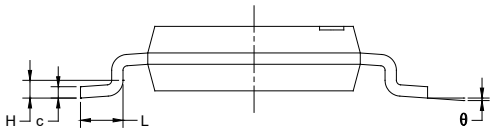
MSOP-10





RECOMMENDED LAND PATTERN (Unit: mm)



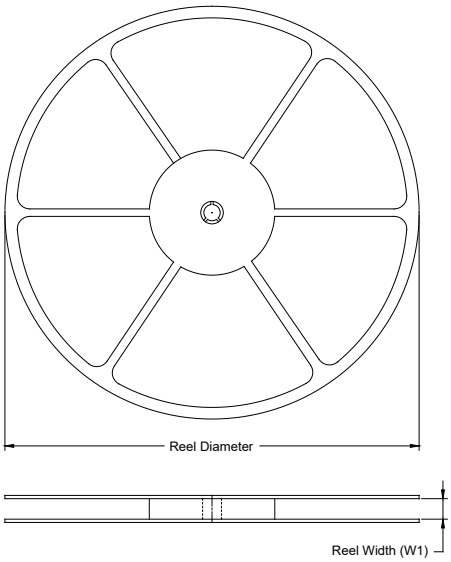


Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	-	-	1.100
A1	0.000	-	0.150
A2	0.750	-	0.950
b	0.170	-	0.330
c	0.080	-	0.230
D	2.900	-	3.100
E	2.900	-	3.100
E1	4.750	-	5.050
e	0.500 BSC		
H	0.250 TYP		
L	0.400	-	0.800
θ	0°	-	8°
ccc	0.100		

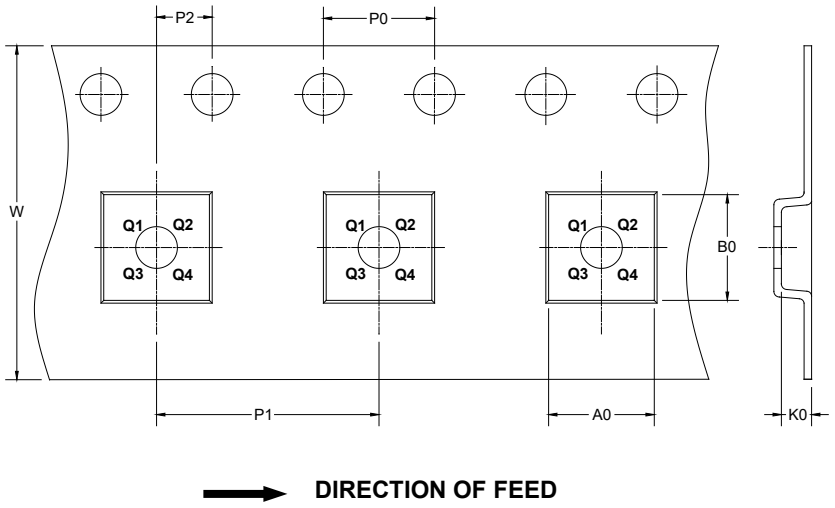
NOTES:
1. This drawing is subject to change without notice.
2. The dimensions do not include mold flashes, protrusions or gate burrs.
3. Reference JEDEC MO-187.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



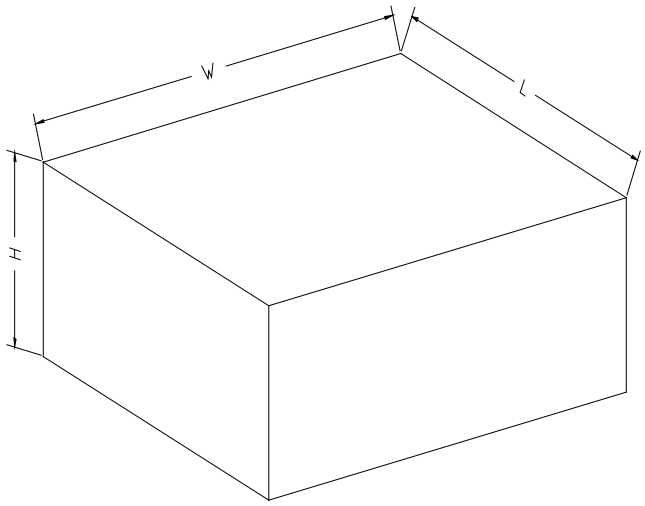
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
MSOP-10	13"	12.4	5.20	3.30	1.50	4.0	8.0	2.0	12.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002