SGMM2130
3V to 17V Input, 3A Synchronous 3D Buck PowerSoC

GENERAL DESCRIPTION

The SGMM2130 is a high frequency synchronous Buck PowerSoC. It integrates a synchronous Buck converter and an inductor to simplify design, reduce external components, and save PCB area. High output voltage accuracy and fast transient response along with low-ESR ceramic capacitors are easily achievable with the AHP-COT control.

The 3V to 17V input voltage range makes this device a suitable choice for both 12V input power rails and the battery powered applications including Li-Ion batteries. It supports 100% duty cycle operation and can provide 3A continuous current. The SGMM2130 can operate as a standalone power supply with adjustable soft-start ramp or as a tracking power supply using the SS/TR input pin. The enable input (EN) and power good output (PG) pins provide power sequencing capability.

In power-save mode (PSM), the VIN quiescent current is reduced to 31μA (TYP). Operation mode is seamlessly changed between PWM and PSM to keep the efficiency high in entire load range. Mode changing is automatically decided based on the load current at the DCM/CCM changeover level.

In the shutdown mode, the device is completely turned off and the current consumption drops to 3μA typically.

The SGMM2130 is available in a Green EMSIP-2.8×3-10L package.

FEATURES

- **Integrated Power IC and Power Inductor**
- **AHP-COT Topology**
- **3V to 17V Input Voltage Range**
- **Up to 3A Output Current**
- **0.9V to 5.5V Adjustable Output Voltage**
- **Internal Compensation**
- **Adjustable Soft-Start and Tracking Function**
- **Pre-biased Startup**
- **Power-Save Mode with Seamless Transition**
- **31μA (TYP) Quiescent Current**
- **1.95MHz PWM Frequency**
- **Power Good Output**
- **100% Duty Cycle Mode**
- **Under-Voltage Lockout (UVLO)**
- **Current Limit Protection**
- **Short-Circuit Protection**
- **Over-Temperature Protection**
- **Available in a Green EMSIP-2.8×3-10L Package**

APPLICATIONS

12V Rail Supplies
POL Supply from Single or Multi-Cell Li-Ion Battery
Solid-State Disk Drives
Embedded Systems
LDO Replacement
Mobile PCs, Tablets, Modems, Cameras
Servers, Micro Servers
Data Terminal, Point of Sales (ePOS)

TYPICAL APPLICATION

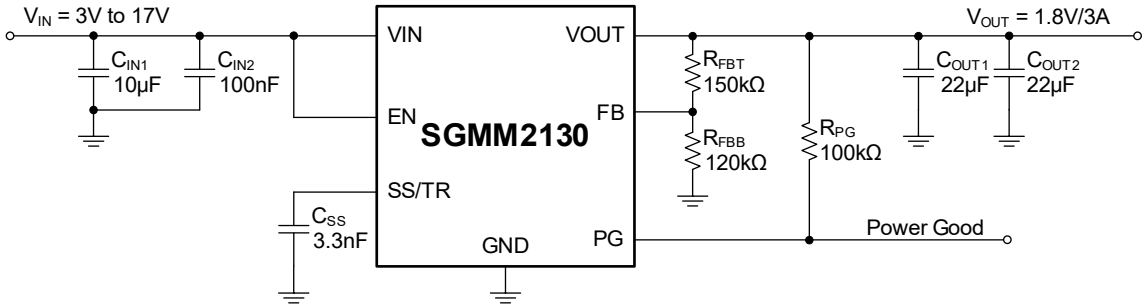


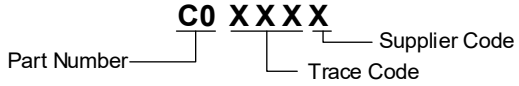
Figure 1. Typical Application Circuit

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGMM2130	EMSIP-2.8×3-10L	-40℃ to +125℃	SGMM2130XESAC10G/TR	C0XXXX	Tape and Reel, 3000

MARKING INFORMATION

NOTE: XXXX = Trace Code and Supplier Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

VIN ..... -0.3V to 20V
EN, SS/TR ..... -0.3V to V_{IN} + 0.3V
FB, PG, VOUT ..... -0.3V to 6V
Power Good Sink Current, PG 10mA
Package Thermal Resistance
EMSIP-2.8×3-10L, θ_{JA} ..... 49.6℃/W
EMSIP-2.8×3-10L, θ_{JB} ..... 10.9℃/W
EMSIP-2.8×3-10L, $\theta_{JC\ (TOP)}$ ..... 22℃/W
EMSIP-2.8×3-10L, $\theta_{JC\ (BOT)}$ ..... 10.8℃/W
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility (1) (2)
HBM ..... ±4000V
CDM ..... ±1000V

NOTES:

1. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.

2. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

RECOMMENDED OPERATING CONDITIONS

V_{IN} ..... 3V to 17V
V_{PG} ..... 5.5V (MAX)
V_{OUT} ..... 0.9V to 5.5V
I_{OUT} ..... 3A (MAX)
Module Operating Temperature Range for 100,000 hours Lifetime ..... -40℃ to +110℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

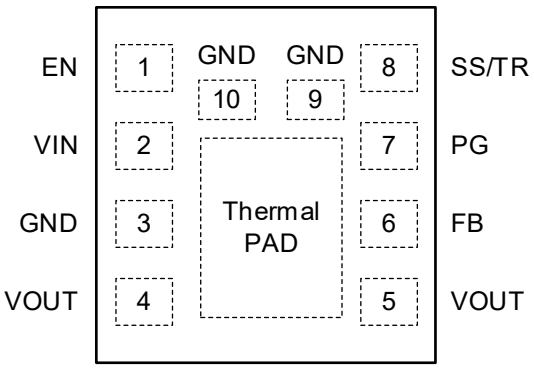
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

(TOP VIEW)



EMSIP-2.8×3-10L

PIN DESCRIPTION

PIN	NAME	TYPE	FUNCTION
1	EN	I	Active High Enable Input. Connect a temporary internal pull-down resistor. Applying a logic high voltage to this pin enables the chip. Pulling EN low will shut down the device.
2	VIN	P	Supply Voltage for Power Stage.
3, 9, 10	GND	G	Power Ground. The GND, exposed thermal pad and the common system ground plane must be connected directly.
4, 5	VOUT	O	Output Voltage Pin.
6	FB	I	Voltage Feedback of Adjustable Output Voltage. Connect an external resistor divider from the output to this pin to program the desired output voltage.
7	PG	O	Open-Drain Power Good Output. A pull-up resistor to a logic high rail is needed. The PG pin goes low when the output voltage is below regulation and will be in high-impedance state when the output is in regulation.
8	SS/TR	I	Soft-Start/Tracking Input Pin. A minimum 1nF capacitor is required for this pin to avoid overshoot during the charge of soft-start capacitor. To set the soft-start ramp, place a capacitor (C_{SS}) between this pin and GND. If an external voltage is applied to this pin, the output voltage will track it. This feature is useful for voltage tracking and radiometric sequencing.
Thermal PAD	Thermal PAD	—	Thermal Pad. It must be directly connected to GND and the PCB common ground plane. Solder this pad such that a good heat transfer path is created from the junction to the ambient. Thermal vias will help.

NOTE: I = input, O = output, P = power, G = ground.

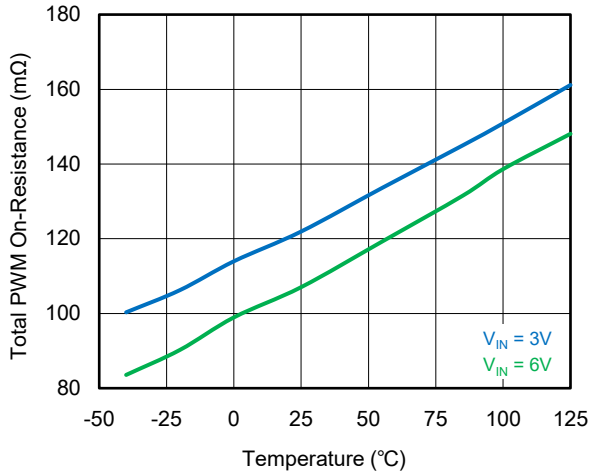
ELECTRICAL CHARACTERISTICS

(V_{IN} = 3V to 17V, T_J = -40℃ to +125℃. Typical values are at T_J = +25℃ and V_{IN} = 12V, unless otherwise noted.)

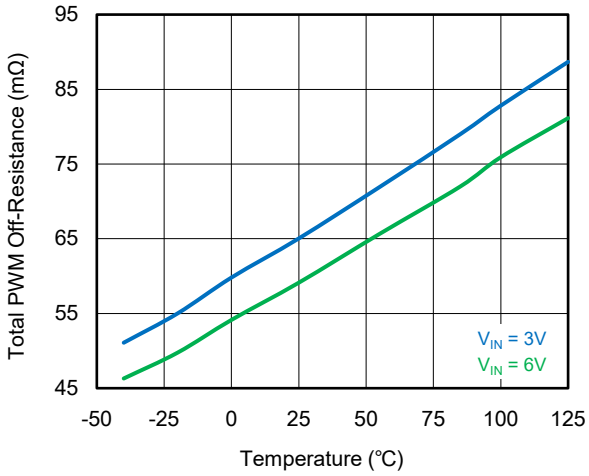
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply							
Quiescent Current into VIN	I_Q	EN = high, no load, device not switching, V_{IN} = 12V			31	48	μA
Shutdown Current into VIN	I_{SD}	EN = low, V_{IN} = 12V			3	4.8	μA
Under-Voltage Lockout Threshold	V_{UVLO}	V_{IN} falling		2.62	2.73	2.84	V
	V_{UVLO_HYS}	V_{IN} rising			160		mV
Thermal Shutdown Threshold	T_{SD}	Temperature rising			160		℃
		Temperature falling			140		℃
Logic Interface (EN)							
High Level Input Threshold Voltage	V_{IH}			0.9	0.66		V
Low Level Input Threshold Voltage	V_{IL}				0.44	0.25	V
Input Leakage Current into the EN pin	I_{LKG_EN}	EN = V_{IN}			0.01	0.4	μA
Control (SS/TR, PG)							
SS/TR Pin Source Current	$I_{SS/TR}$			2.1	2.5	2.9	μA
Power Good Threshold Voltage	V_{TH_PG}	V_{PG} rising, V_{FB} referenced to V_{REF}		91	95	98	%
		V_{PG} falling, V_{FB} referenced to V_{REF}		85	89	92	
Power Good Output Low	V_{OL_PG}	I_{SINK} = 2mA			0.1	0.3	V
Input Leakage Current into the PG pin	I_{LKG_PG}	V_{PG} = 1.8V			50	400	nA
Output							
Feedback regulation voltage	V_{FB}	PWM mode	$V_{IN} \geq V_{OUT}$ + 1V, T_J = +25℃	793	800	807	mV
			$V_{IN} \geq V_{OUT}$ + 1V	790	800	810	
FB Input Leakage Current	I_{LKG_FB}	V_{FB} = 0.8V			1	10	nA
Line Regulation		V_{IN} = 3V to 17V, I_{OUT} = 1A, V_{OUT} = 1.8V			0.004		%/V
Load Regulation		I_{OUT} = 0.5A to 3A, V_{OUT} = 1.8V			0.15		%/A
Power Switch and Inductor							
Total PWM-On Resistance	R_{PWM_ON}	PWM on, resistance from V_{IN} to V_{OUT}, V_{IN} = 6V			107	180	mΩ
		PWM on, resistance from V_{IN} to V_{OUT}, V_{IN} = 3V			122		
Total PWM-Off Resistance	R_{PWM_OFF}	PWM off, resistance from V_{OUT} to GND, $V_{IN} \geq$ 6V			59	100	
		PWM off, resistance from V_{OUT} to GND, V_{IN} = 3V			65		
High-side MOSFET Current Limit	I_{LIMF}	V_{IN} = 12V		3.9	4.6	5.3	A
PWM Switching Frequency	f_{SW}	I_{OUT} = 1A, V_{OUT} = 1.8V			1950		kHz
Inductance of the integrated Inductor	L	At 1MHz, 1V			1000		nH

TYPICAL PERFORMANCE CHARACTERISTICS

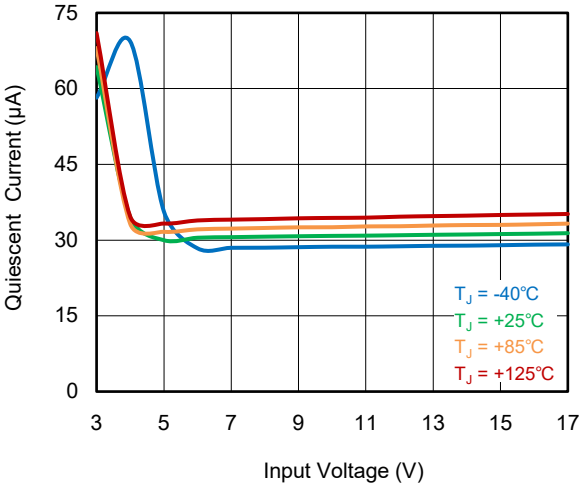
Total PWM-On Resistance vs. Temperature



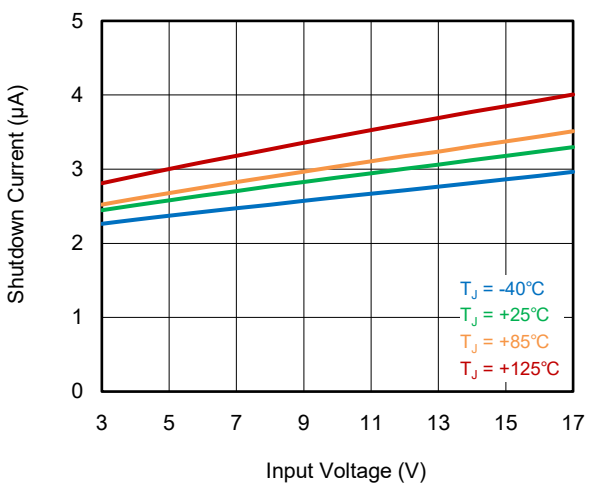
Total PWM-Off Resistance vs. Temperature



Quiescent Current vs. Input Voltage



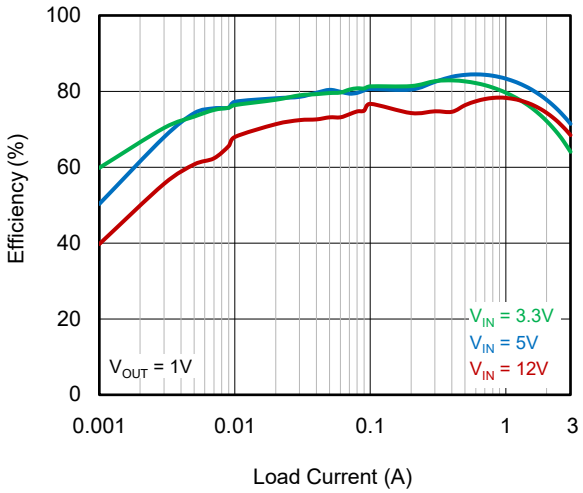
Shutdown Current vs. Input Voltage



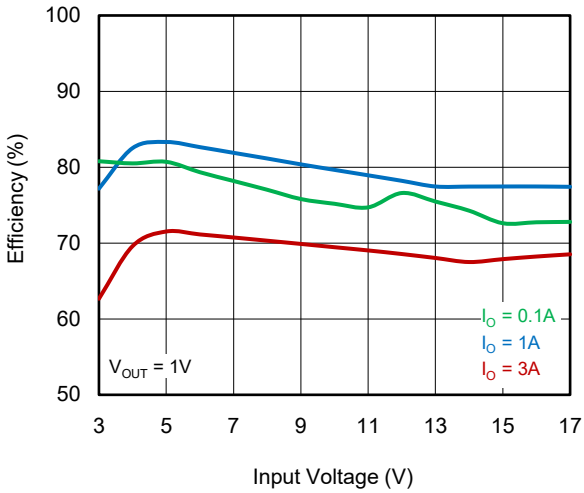
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, V_{IN} = 12V, V_{OUT} = 1.8V, C_{IN} = 10μF + 0.1μF, and C_{OUT} = 2 × 22μF, unless otherwise noted.

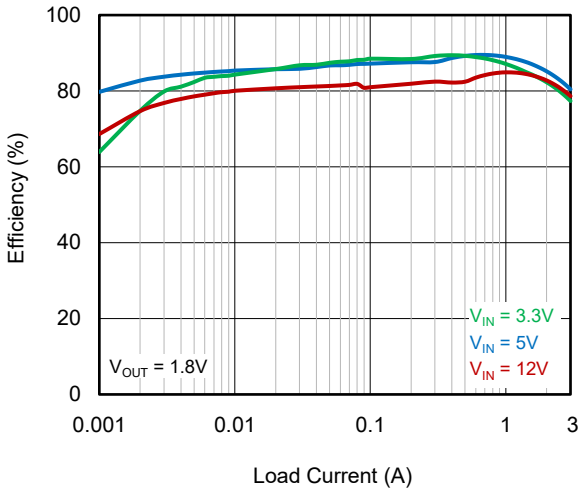
Efficiency vs. Load Current



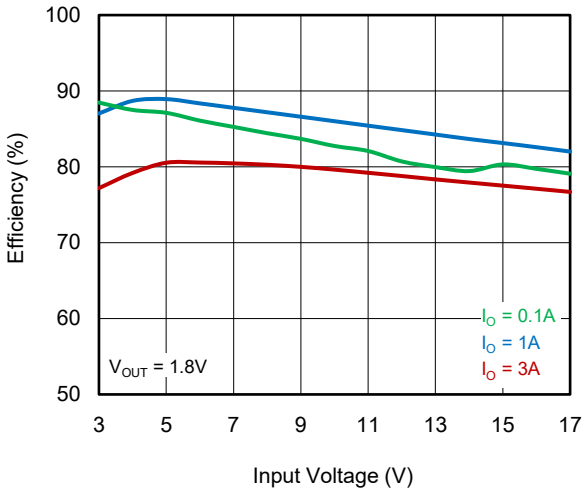
Efficiency vs. Input Voltage



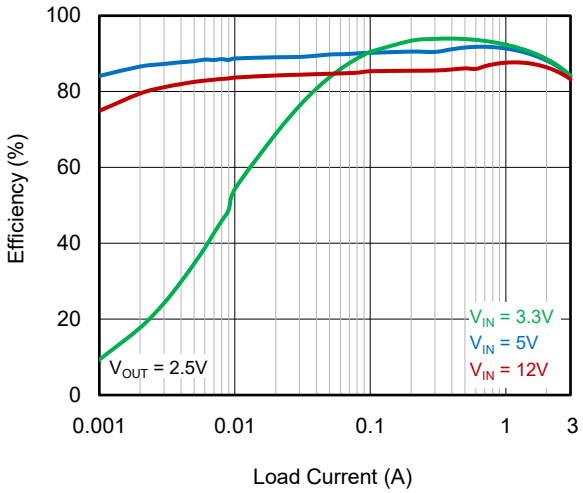
Efficiency vs. Load Current



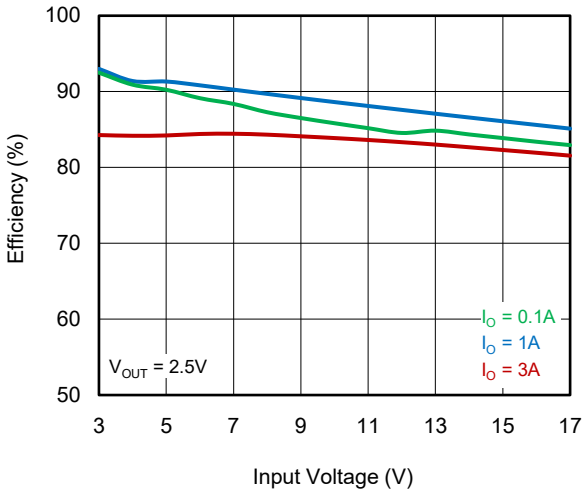
Efficiency vs. Input Voltage



Efficiency vs. Load Current



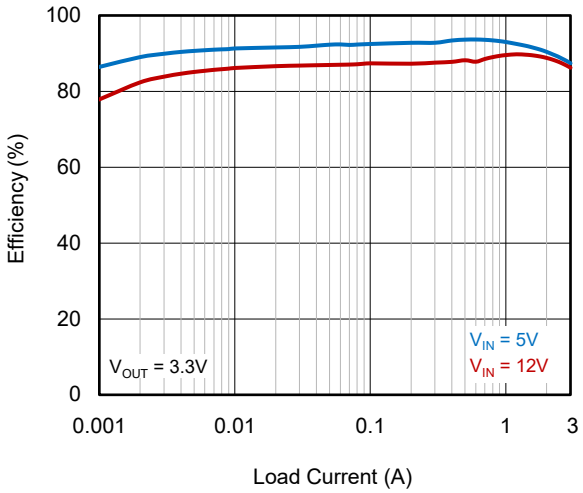
Efficiency vs. Input Voltage



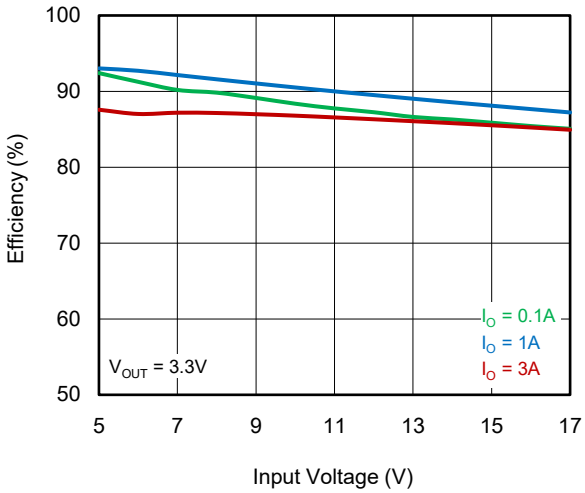
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, V_{IN} = 12V, V_{OUT} = 1.8V, C_{IN} = 10μF + 0.1μF, and C_{OUT} = 2 × 22μF, unless otherwise noted.

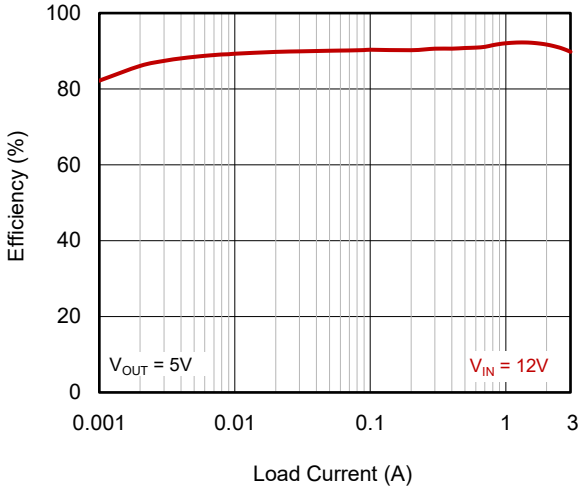
Efficiency vs. Load Current



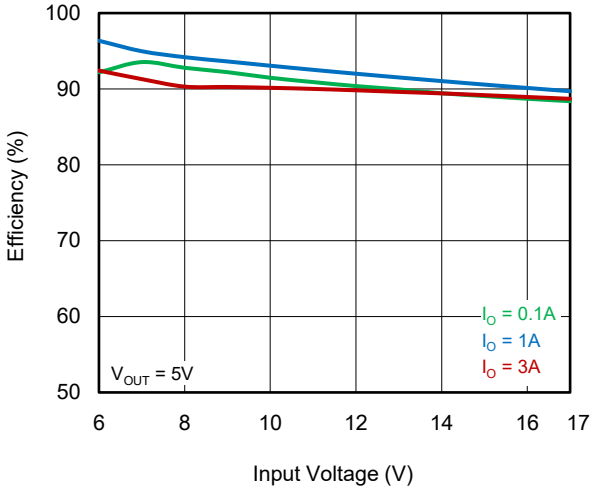
Efficiency vs. Input Voltage



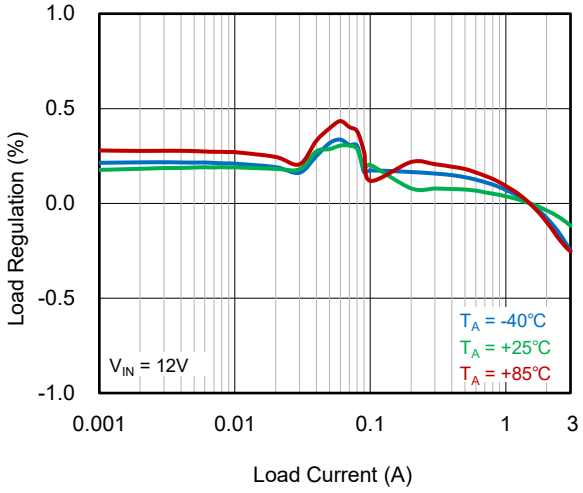
Efficiency vs. Load Current



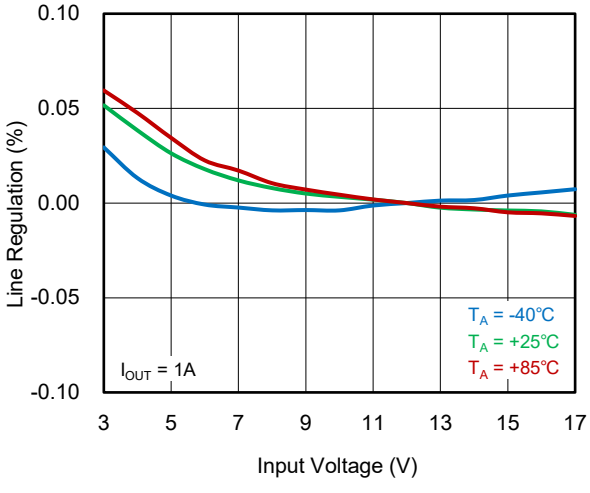
Efficiency vs. Input Voltage



Load Regulation



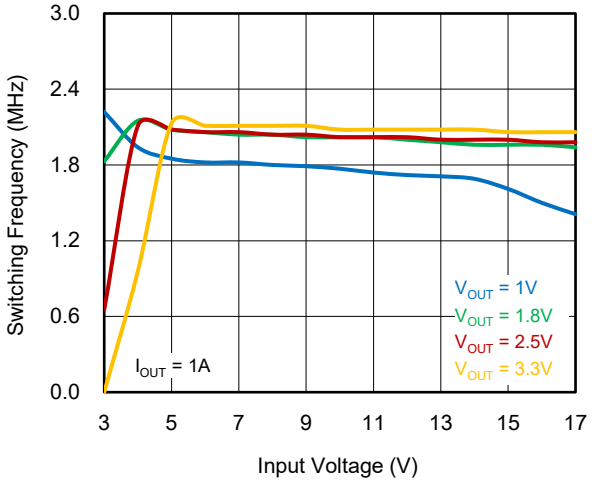
Line Regulation



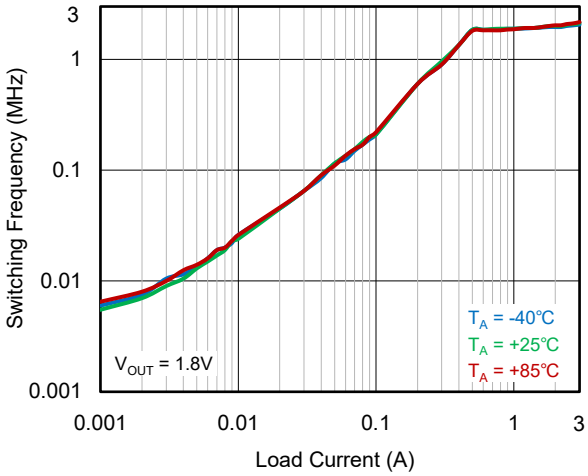
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, V_{IN} = 12V, V_{OUT} = 1.8V, C_{IN} = 10μF + 0.1μF, and C_{OUT} = 2 × 22μF, unless otherwise noted.

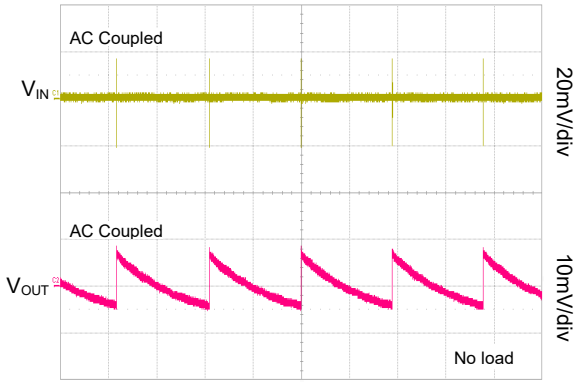
Switching Frequency vs. Input Voltage



Switching Frequency vs. Load Current

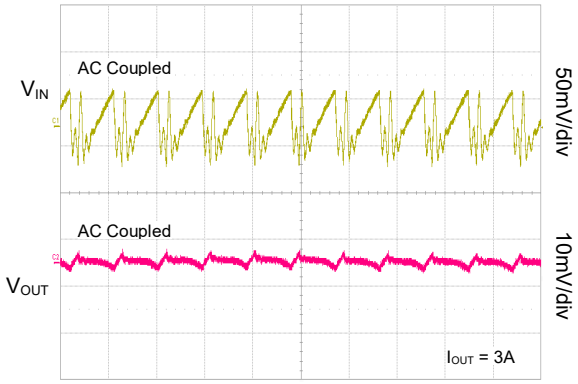


Input and Output Ripple in PSM Mode



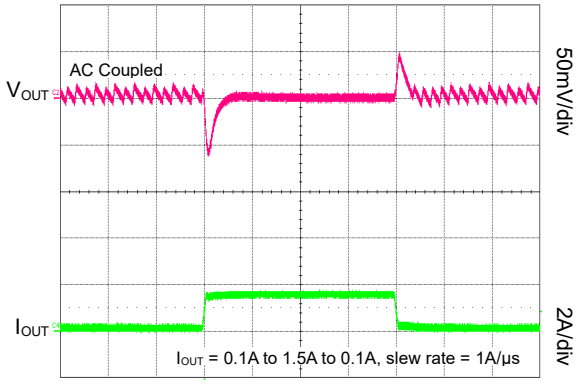
Time (20ms/div)

Input and Output Ripple in PWM Mode



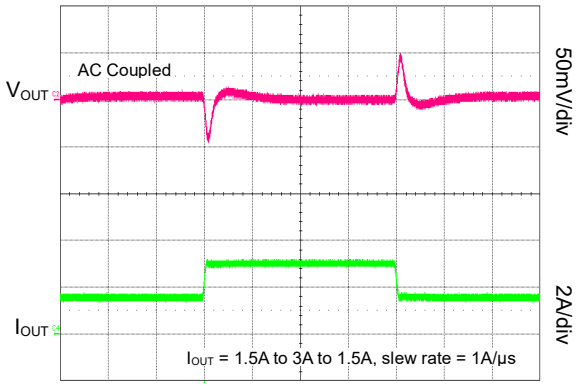
Time (500ns/div)

Load Transient



Time (20μs/div)

Load Transient

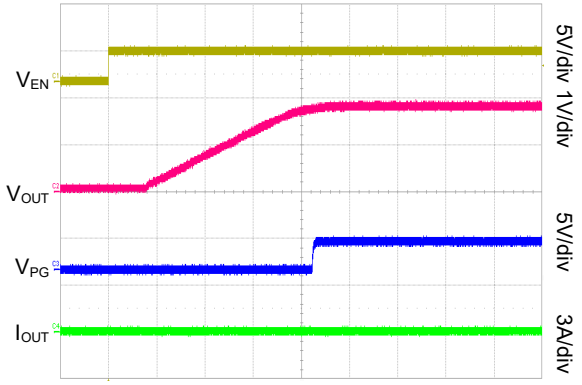


Time (20μs/div)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

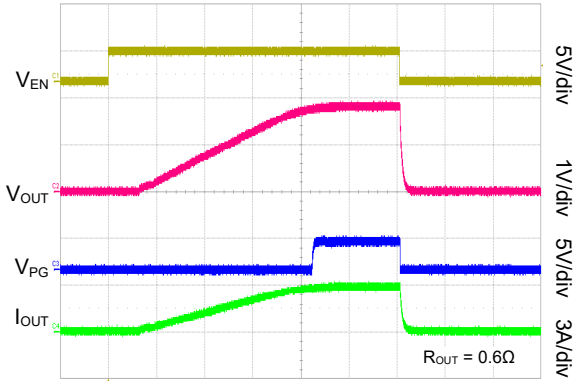
T_A = +25℃, V_{IN} = 12V, V_{OUT} = 1.8V, C_{IN} = 10μF + 0.1μF, and C_{OUT} = 2 × 22μF, unless otherwise noted.

Startup without Load



Time (500μs/div)

Startup / Shutdown with Resistance Load



Time (500μs/div)

FUNCTIONAL BLOCK DIAGRAM

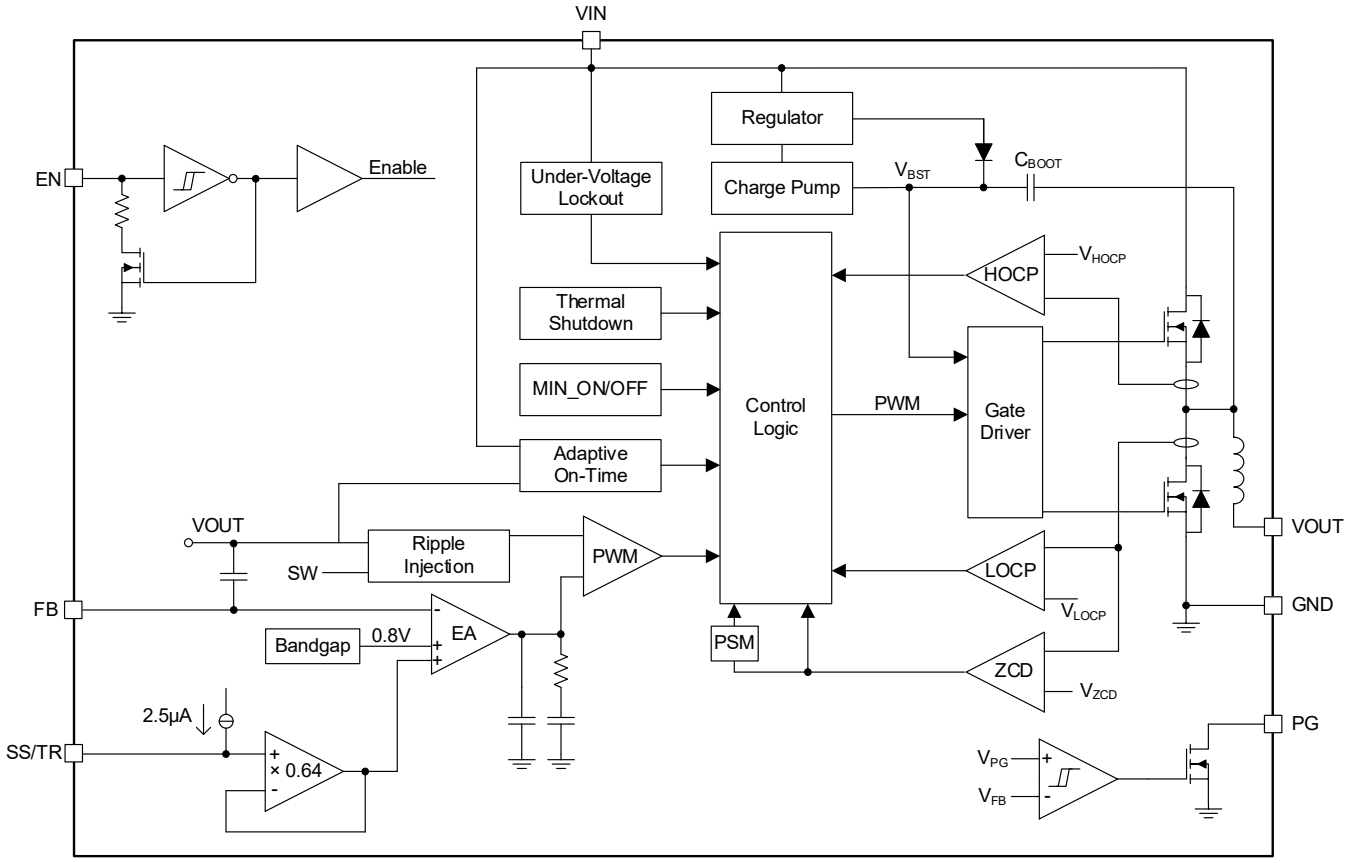


Figure 2. Block Diagram

DETAILED DESCRIPTION

Overview

SGMM2130 is a series of high-frequency synchronous Buck PowerSoC with AHP-COT architecture and advanced regulation topology. The device works in pulse width modulation (PWM) mode at medium to heavy loads. When the load current falls, it goes into PSM to achieve high efficiency with reducing switching frequency and minimizing quiescent current. Operation mode is seamlessly changed between PWM and PSM to keep the efficiency high in entire load range. In PWM mode, the module operates with its nominal switching frequency of 1.95MHz having a controlled frequency variation over the input voltage range.

Under-Voltage Lockout (UVLO)

To avoid mis-operation of the device at low input voltages, under-voltage lockout is implemented to shut down the device when input voltage is lower than V_{UVLO} (when V_{IN} voltage falls). When the input voltage is higher than V_{UVLO}, the device will recover to normal operation with a 160mV hysteresis.

Device Enable and Disable (EN)

The SGMM2130 is enabled by setting the EN pin input to higher than 0.66V. It is disabled when EN pin falls lower than 0.44V. If the device is enabled, the internal power stage starts switching and regulates the output voltage to the setting point voltage. In shutdown mode, the internal power switches as well as the entire control circuitry are turned off to reduce the device current to 3μA. The EN pin is connected with a pull-down resistor to ensure that it remains at the appropriate level. When the EN is connected to a high level, the pull-down circuit is disconnected. If it keeps floating after a low level is connected, the internal pull-down resistance will remain low until the pin is connected to a high level, so the EN pin must be reliably connected to a high or low level.

Soft-Start and Tracking (SS/TR)

An internal soft-start circuit is included to prevent input inrush current and input voltage drops during startup. This circuit slowly ramps up to the error amplifier reference voltage (V_{REF} = 0.8V) after exiting the shutdown state or under-voltage lockout (UVLO). Slow increase of the output voltage prevents the excessive inrush current for charging the output capacitors and creates a smooth output voltage rise. The other advantage of a soft-start is avoiding supply voltage drops especially on the high internal impedance sources such as the primary cells and rechargeable batteries.

The slope of output voltage is controlled by the external capacitor (C_{SS}) connected to the SS/TR pin, and the starting wave form is shown in Figure 3. Reducing the capacitor will obtain a faster starting speed. In order to avoid capacitor voltage overshoot, it is recommended that the C_{SS} capacitor is not less than 1nF. If the device is set to shutdown (EN = GND), UVLO, or thermal shut down, the SS/TR pin is grounded through a pull-down resistor. The SS/TR connection will restart after exiting the above states.

If an external voltage is applied to the SS/TR pin, the output voltage tracking function can be achieved. This feature is useful for voltage tracking and ratio sequencing. If the given voltage is between 0.2V (TYP) and 1V (TYP). The following relationship exists between the FB pin voltage and the tracking voltage.

$$V_{FB} \approx 0.64 \times V_{SS/TR} \quad (1)$$

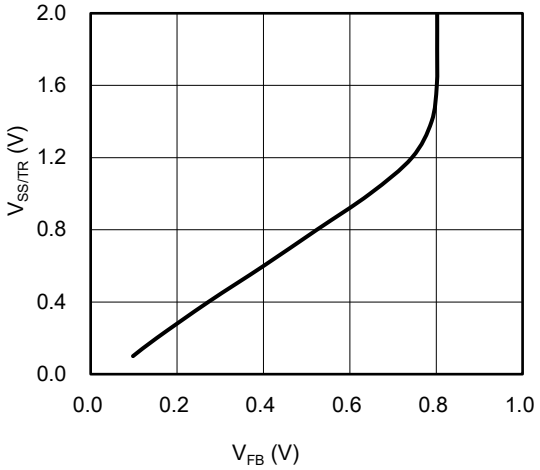


Figure 3. Voltage Tracking Curve

NOTES:

1. When $V_{SS/TR}$ exceeds 1.6V, V_{FB} is clamped to the internal feedback voltage and no longer tracks the given voltage.

2. When the tracking voltage is for external power supply, the voltage value cannot exceed V_{IN} + 0.3V.

The SGMM2130 is also capable of starting with a pre-biased output capacitor when it is powered up or enabled. When the device is turning on, a bias on the output is likely to exist due to the other sources connected to the load(s) such as multi-voltage ICs or simply because of residual charges on the output capacitors. For example, when a device with light load is disabled and re-enabled, the output voltage cannot drop too much during the off period and the device must restart under pre-biased output condition. Without the pre-biased capability, the device cannot be able to start up properly. During the pre-biased start, when the internal set ramp voltage is higher than the pre-biased voltage, the switch is allowed to operate, and then start normally until the output voltage reaches the given value.

DETAILED DESCRIPTION (continued)

Power Good (PG)

The device has PG function inside. PG is an open-drain output with a maximum sinking capacity of 2mA. Connect the pin to GND or keep it floating when it is not in use, otherwise this pin should be pulled to a logical high rail not exceeding 5.5V with an external resistor.

For the SGMM2130, the PG pin is driven to a low level during shutdown, UVLO, and thermal shutdown states. At this time, the PG circuit can be used as an active discharge circuit of V_{OUT} in the presence of power supply voltage. Table 1 respectively shows the PG state changes of SGMM2130 under different conditions. By connecting the PG signal to the EN pins of other converters, it can be used for sequencing of multiple tracks.

Table 1. PG Output State in Different Conditions

Device Information		PG State	
		Hi-Z	Low
Enable (EN = High)	$V_{FB} \geq V_{TH\_PG}$	√	
	$V_{FB} \leq V_{TH\_PG}$		√
Shutdown by EN (EN = Low)			√
Thermal Shutdown	$T_J > T_{SD}$		√
UVLO	$0.85V < V_{IN} < V_{UVLO}$		√
Power Supply Removal	$V_{IN} < 0.85V$	√	

Pulse Width Modulation (PWM) Operation

In the condition of continuous conduction mode (CCM) which occurs at medium to heavy loads, the device works in pulse width modulation (PWM) operation. Then a fixed on-time architecture is activated. The device operates at a nominal switching frequency of 1.95MHz.

Power-Save Mode (PSM)

As the load current decreases, the inductor current will change from continuous mode (CCM) to discontinuous mode (DCM). At this time, the on-time t_{ON} of the switch in COT mode is unchanged, and the turn-off time becomes longer, so the switching frequency decreases. When the load current is further reduced, the SGMM2130 series will enter the power saving mode. The device then maintains high efficiency by reducing the switching frequency and operating at a minimum static current. In PSM mode, the inductor current is discontinuous and the output voltage is slightly higher than the nominal output voltage. This effect can be mitigated by a larger output capacitance. The switching frequency is greatly reduced as the load current decreases in PSM mode.

When the duty cycle is small, the minimum on-time is set to limit the switching loss, in which case the circuit frequency is below the nominal value. When the input and output voltages are close, the device will remain in CCM, no matter how the load changes, and no longer enter PSM mode.

100% Duty Cycle

When the input voltage gradually drops to the regulation output voltage, the device can operate at 100% duty cycle and keep the high-side MOSFET continuously on for minimal input-to-output voltage difference. The low side MOSFET is kept off. In this mode, the lowest input voltage for keeping the output regulated is determined by load current and the resistive drops from the input to the output as given in Equation 2:

$$V_{IN\_MIN} = V_{OUT} + I_{OUT\_MAX} \times R_{PWM\_ON} \quad (2)$$

where:

V_{IN_MIN} is the minimum input voltage to maintain output voltage in regulation.

I_{OUT_MAX} is the maximum output current.

R_{PWM_ON} is Resistance from V_{IN} to V_{OUT}, which includes the high-side MOSFET on-resistance and DC resistance of the inductor.

Switch Current Limits and Short-Circuit Protection

Limiting switch current protects the switch itself and also prevents over-current sources and the inductor. When the high-side (HS) switch current exceeds high-side MOSFET current limit (4.6A), the HS switch is off and the low-side (LS) switch is on to reduce the inductive current and limit the peak current. The switch on the high-side (HS) can be turned on again only when the switch current on the low-side (LS) is lower than low-side MOSFET current limit (3.6A). If the V_{OUT} is detected to be lower than 0.5V (TYP), the high-side MOSFET current limit is reduced to 2.1A (TYP), and the current limit returns to normal when the output voltage is higher than 0.5V (TYP).

Thermal Protection and Shutdown

Thermal protection is included to protect the die against overheating damage. If the junction temperature exceeds T_{SD} threshold, the switching is stopped and the device is shut down. An automatic recovery with a soft-start begins when the junction cools down for 20℃ below the T_{SD} limit.

APPLICATION INFORMATION

In this section, power supply design with the SGMM2130 synchronous Buck PowerSoC and selection of the external component will be explained based on the typical application that is applicable for various input and output voltage combinations.

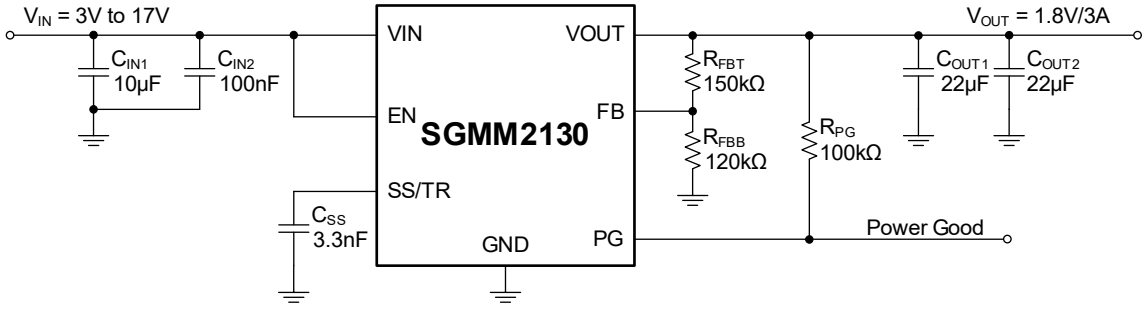


Figure 4. 1.8V Output Voltage Application of SGMM2130

Design Requirements

Table 2 summarizes the requirements for this example as shown in Figure 4. The selected components are given in Table 3.

Table 2. Design Parameters for the Application Example

Design Parameter	Example Value
Input Voltage	3V to 17V
Output Voltage	1.8V
Maximum Output Current	3A
Switching Frequency	1.95MHz

Table 3. Selected Components for the Design Example

Ref	Description	Manufacturer
C_{IN1}	10μF, ceramic capacitor, 25V, size 1210	Standard
C_{IN2}	100nF, ceramic capacitor, 25V, size 0603	Standard
C_{SS}	3.3nF, ceramic capacitor, 25V, size 0603	Standard
C_{OUT1}	22μF, ceramic capacitor, 6.3V, size 0805	Standard
C_{OUT2}		
R_{FBT}	150kΩ, chip resistor, 1/16W, 1%, size 0603	Standard
R_{FBB}	120kΩ, chip resistor, 1/16W, 1%, size 0603	Standard
R_{PG}	100kΩ, chip resistor, 1/16W, 1%, size 0603	Standard

Input Capacitor Selection (C_{IN})

The input capacitor is the low impedance energy source for the device that helps provide stable operation. A low ESR multilayer ceramic capacitor is recommended for best filtering. In most cases, a 10μF input capacitor is recommended, a larger value reduces input voltage ripple and improves system stability. Usually a 100nF low ESR ceramic capacitor is recommended to be connected between the VIN and GND pins as closely as possible.

Output Capacitor Selection (C_{OUT})

The architecture of the SGMM2130 allows use of tiny ceramic-type output capacitors with low equivalent series resistance (ESR). These capacitors are recommended due to the low output voltage ripple. To keep the resistance up to high frequencies and to achieve narrow capacitance variation with temperature, it is recommended to use X7R or X5R dielectric. The bias voltage can cause the capacitance of the ceramic capacitor to decrease significantly, and the degree of decrease depends on the specification of the capacitor (size, nominal voltage, temperature standard).

The effective deviation of a ceramic capacitor can be as high as -50% to +20% of the nominal value. C_{OUT} = 2 × 22μF is the recommended values for the typical application. If the switching frequency is seriously reduced due to the decrease of the input voltage, it is recommended to increase the output capacitance to ensure system stability.

Soft-Start Capacitor Selection (C_{SS})

The slope of soft-start output voltage can be changed through the selection of SS/TR external capacitor, and the external capacitor can be charged through 2.5μA (TYP) constant current source inside the chip. The relationship between soft-start time and capacitance is shown in the following Equation 3:

$$C_{SS} = t_{SS} \times \frac{2.5\mu A}{1.25V} \quad (3)$$

where:

C_{SS} is the capacitance (F) required at the SS/TR pin.

t_{SS} is the desired soft-start ramp time (s).

APPLICATION INFORMATION (continued)

Output Voltage Adjustment

Use Equation 4 for selecting the feedback resistors (R_{FBT} and R_{FBB}) in Figure 4 to set the desired output voltage. There is a 20pF feedforward capacitance inside the device. It forms a set of zero-pole pair with R_{FBT} and R_{FBB}. The position of the zero-pole pair will affect the dynamic characteristics and stability of the system. Therefore, for different output voltages please refer to the R_{FBT}/R_{FBB} values of similar output voltages in Figure 4 to Figure 6.

$$R_{FBT} = R_{FBB} \times \left(\frac{V_{OUT}}{V_{FB}} - 1 \right) = R_{FBB} \times \left(\frac{V_{OUT}}{0.8V} - 1 \right) \quad (4)$$

Additional Typical Application Circuits

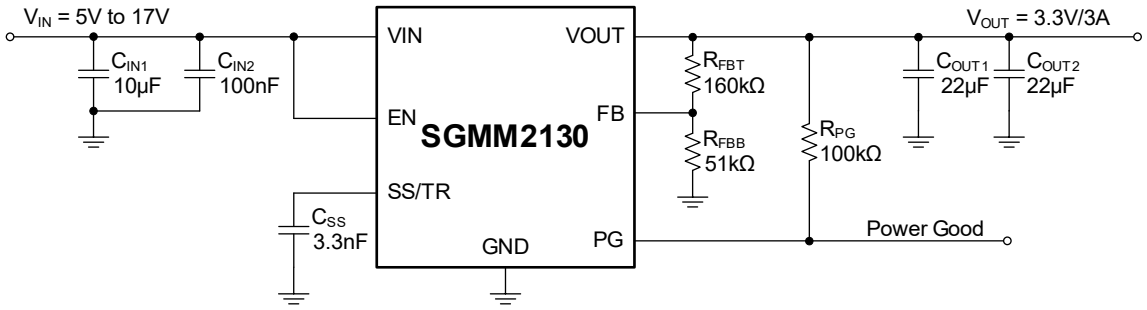


Figure 5. 3.3V Output Voltage Application of SGMM2130

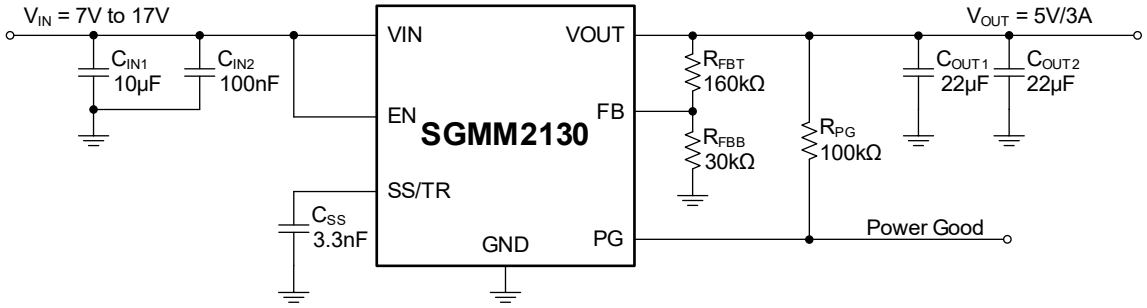


Figure 6. 5V Output Voltage Application of SGMM2130

Layout Guidelines

A critical component of a high frequency switching power supply is the PCB layout. A good layout can improve the overall performance of the system and a poor layout can result in stability issues and EMI problems. The following guidelines are provided for designing a power supply layout with the SGMM2130.

• Place the input/output capacitors as close as possible to the device pins and keep the power traces short. Use direct and wide traces for routing power paths to assure low trace parasitic resistance and inductance.

• Connect the ground returns of the input and output capacitors close to the GND pin and at the same point to avoid a ground potential shift and to minimize high frequency current path.

• Use GND planes in mid-layers for shielding and minimizing the ground potential drifts.

• Connect the thermal pad of the device to the bottom or internal ground planes using multiple vias placed directly under or adjacent to the pad to enhance heat dissipation and improve device reliability.

APPLICATION INFORMATION (continued)

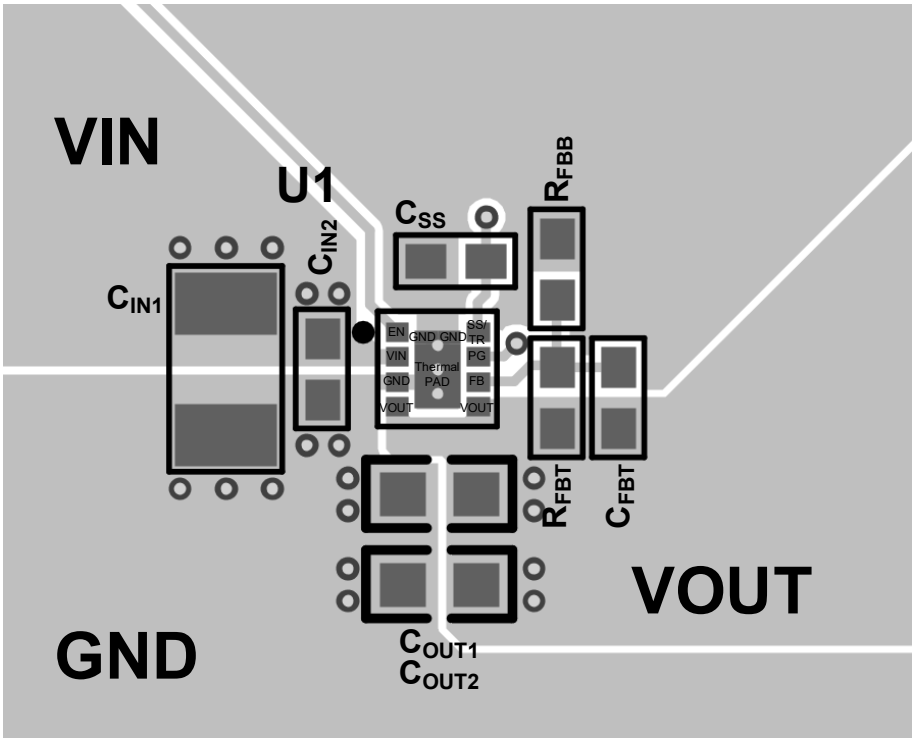


Figure 7. PCB Layout Example

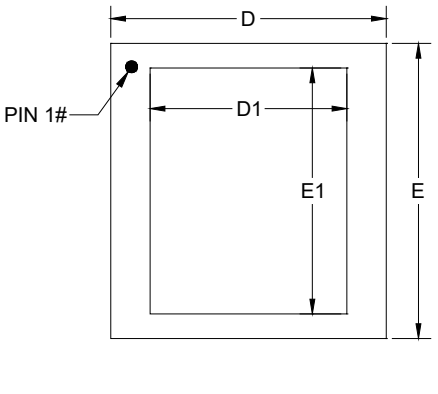
REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

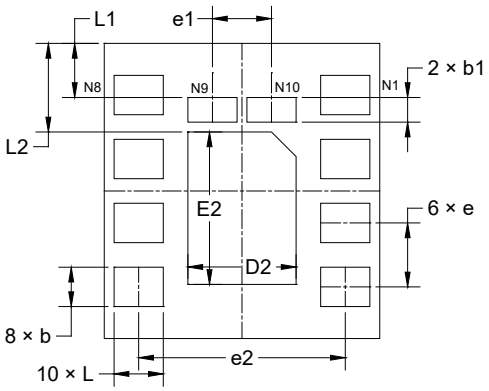
Changes from Original to REV.A (JULY 2026)	Page
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

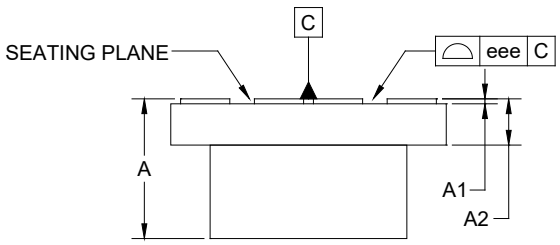
EMSIP-2.8×3-10L



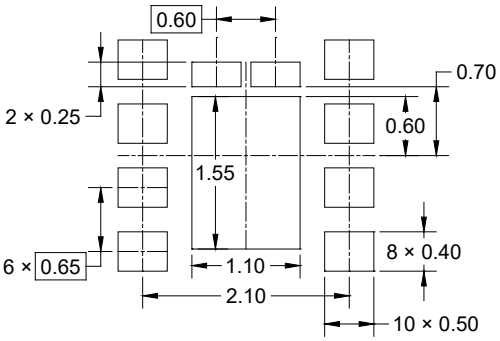
TOP VIEW



BOTTOM VIEW



SIDE VIEW



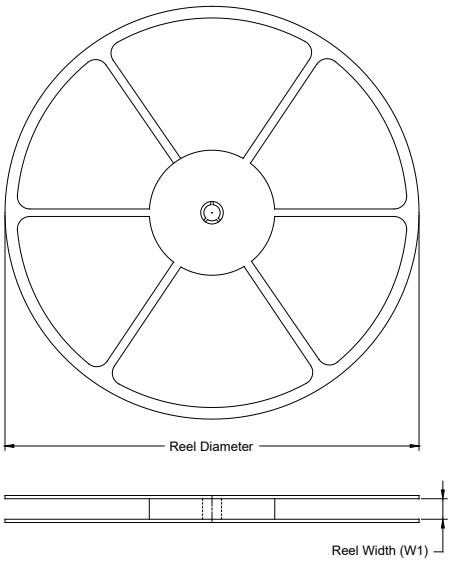
RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	1.320	-	1.520
A1		0.050 REF	
A2		0.420 REF	
b	0.350	-	0.450
b1	0.200	-	0.300
D	2.700	-	2.900
D1		2.000 REF	
D2	1.050	-	1.150
E	2.900	-	3.100
E1		2.500 REF	
E2	1.500	-	1.600
e		0.650 BSC	
e1		0.600 BSC	
e2		2.100 BSC	
L	0.450	-	0.550
L1		0.550 REF	
L2		0.900 REF	
eee		0.100	

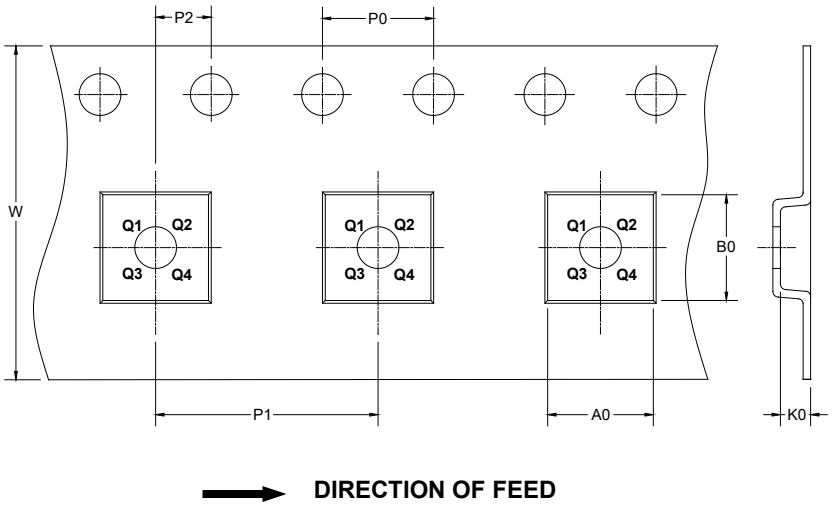
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



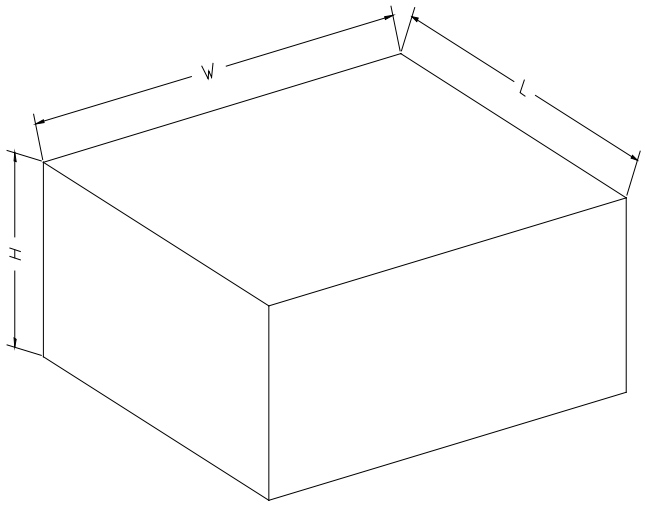
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
EMSIP-2.8×3-10L	13"	12.4	3.10	3.30	1.62	4.0 0	8.00	2.00	12.00	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002