SGM61061S
6A Continuous (8A Peak), High Efficiency, Synchronous Buck Converter

GENERAL DESCRIPTION

The SGM61061S device is a 2.7V to 5.5V synchronous Buck converter with AHP-COT architecture that is an optimized solution for high efficiency and compact size. The device integrates switches capable of delivering an output current up to 8A.

When MODE input voltage is lower than 0.4V or floating, SGM61061S enters into power-save-mode (PSM) mode. At medium to heavy loads, it operates in pulse width modulation (PWM) state with 1.2MHz (TYP) switching frequency. At light loads, the device automatically enters in pulse frequency modulation (PFM) state to maintain high efficiency over the entire load current range. When MODE input voltage is more than 1.2V, SGM61061S enters into a forced pulse width modulation (FPWM) mode over the entire load current range. In shutdown state, the current consumption is reduced to 0.03μA (TYP).

The SGM61061S is available in a Green TQFN-2×3-12L package.

FEATURES

- **AHP-COT Control**
- **6A Continuous Output Current**
- **8A Peak Output Current**
- **2.7V to 5.5V Input Voltage Range**
- **Low R_{DSON} Internal Switches: 19mΩ/9mΩ**
- **44μA (TYP) Quiescent Current (V_{IN} = 3.6V)**
- **1.2MHz (TYP) Switching Frequency**
- **Low Dropout with 100% Duty Cycle**
- **External Control of Operation Mode**
- **Adjustable Output Voltage from 0.6V to V_{IN}**
- **Output Discharge Function**
- **1.3ms (TYP) Internal Soft-Start Time and Pre-Biased Startup**
- **Cycle-by-Cycle Over-Current Protection**
- **Hiccup Mode OCP/Short-Circuit Protection**
- **Stable with Low ESR Output Ceramic Capacitors**
- **Thermal Shutdown Protection**
- **Available in a Green TQFN-2×3-12L Package**

APPLICATIONS

Battery Powered Applications
Point-of-Load
Processor Power Supplies
Hard Disk Drives (HDD)/Solid State Drives (SSD)

TYPICAL APPLICATION

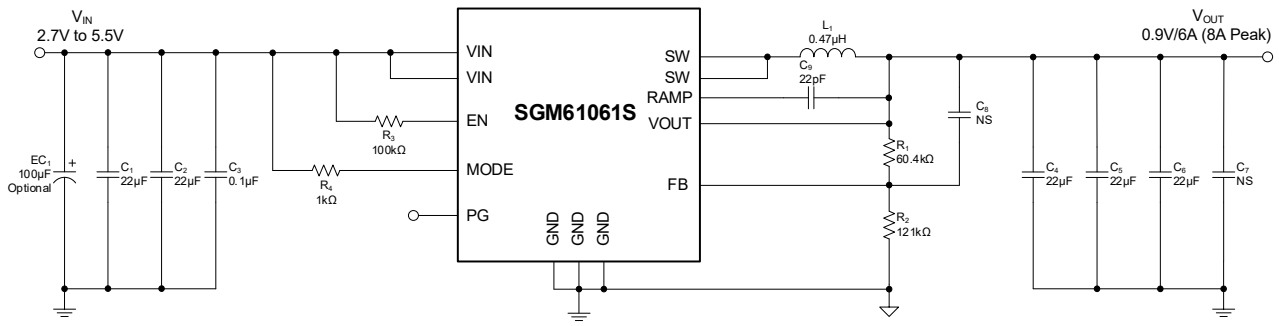


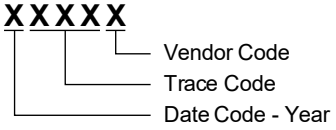
Figure 1. Typical Application Circuit

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM61061S	TQFN-2×3-12L	-40℃ to +125℃	SGM61061SXTSS12G/TR	1UOSS XXXXX	Tape and Reel, 3000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Pin Voltages Referred to GND
VIN, FB, EN, PG, MODE, VOUT, RAMP ..... -0.3V to 6V
SW (DC) .....-0.3V to V_{IN} + 0.3V
SW (AC, Less than 10ns) while Switching..... -3V to 8V
Package Thermal Resistance
TQFN-2×3-12L, θ_{JA} ..... 47.9℃/W
TQFN-2×3-12L, θ_{JB} ..... 6.1℃/W
TQFN-2×3-12L, $\theta_{JC\ (TOP)}$..... 54℃/W
TQFN-2×3-12L, $\theta_{JC\ (BOT)}$..... 8℃/W
Junction Temperature Range .....-40℃ to +150℃
Storage Temperature Range .....-65℃ to +150℃
Lead Temperature (Soldering, 10s).....+260℃
ESD Susceptibility (1) (2)
HBM.....±4000V
CDM .....±1000V

NOTES:

1. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.

2. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

RECOMMENDED OPERATING CONDITIONS

Input Voltage Range, V_{IN} .....2.7V to 5.5V
Output Voltage Range, V_{OUT}..... 0.6V to V_{IN}
Maximum V_{PG} 5.5V
Output Current Range, I_{OUT} .....0A to 6A (8A Peak)
Operating Junction Temperature Range.....-40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

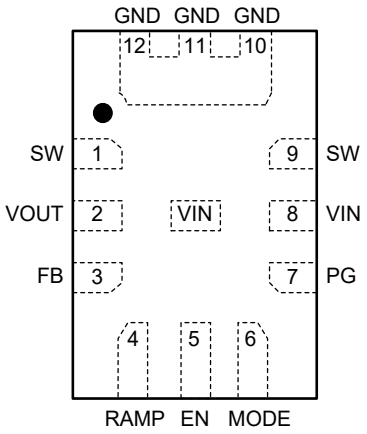
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

(TOP VIEW)



TQFN-2×3-12L

PIN DESCRIPTION

PIN	NAME	TYPE	FUNCTION
1, 9	SW	P	Switching Node Output of the Converter. Switch pin connected to the internal FET switches and inductor terminal. Connect the inductor of the output filter to this pin.
2	VOUT	I	Output Voltage Pin. Connect this pin to output capacitor directly.
3	FB	I	Feedback Pin for Internal Control Loop. Connect this pin to an external feedback divider.
4	RAMP	I	RAMP Pin. Connect a capacitor from this pin to VOUT to optimize the transient performance.
5	EN	I	Device Enable Input. Enable: pull this pin to high voltage level.
6	MODE	I	FPWM and PSM Mode Selection. When MODE voltage is more than 1.2V, the device enters FPWM mode. When MODE voltage is lower than 0.4V or floating, the device enters PSM mode.
7	PG	O	Power Good Open-Drain Output Pin. The output of this pin is an open-drain with an internal 570kΩ (TYP) pull-up resistor to VIN. PG is pulled up to VIN when the FB voltage is within 10% of the regulation level, otherwise it is low. There is a 105μs delay between the time V_{FB} reaches PG threshold and the time PG pin goes high.
8, Exposed Pad	VIN	P	Power Supply Voltage Input. A decoupling capacitor is required to ground to reduce switching spikes. The input capacitor should be placed as close as possible to the IC pins.
10, 11, 12	GND	G	Ground Pin. Connect these pins to larger copper areas to the negative terminals of the input and output capacitors.

NOTE: I = input, O = output, P = power, G = ground.

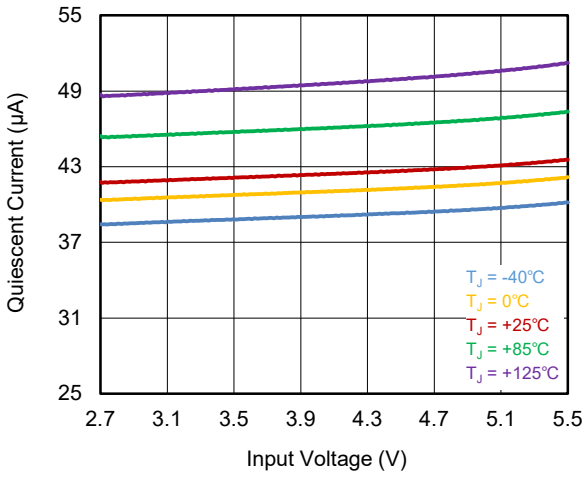
ELECTRICAL CHARACTERISTICS

(V_{IN} = 3.6V and T_J = -40℃ to +125℃, and all typical values are measured at T_J = +25℃, unless otherwise noted.)

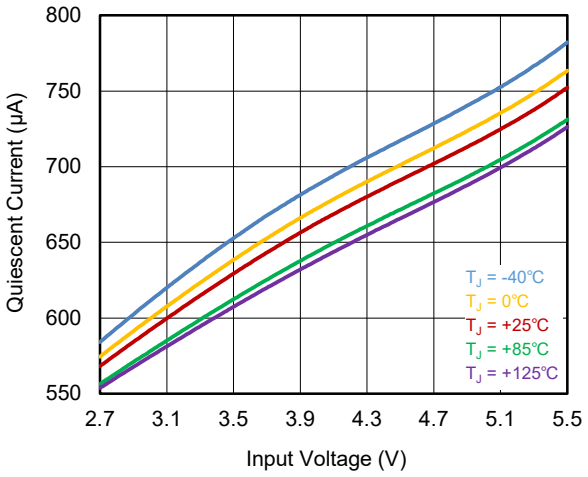
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply							
Quiescent Current into VIN Pin	I_Q	Not switching, V_{IN} = 2.7V to 5.5V, V_{EN} = 2V, V_{FB} = 0.62V	T_J = +25℃		44	60	μA
			T_J = -40℃ to +125℃			70	
Shutdown Current into VIN Pin	I_{SD}	V_{IN} = 2.7V to 5.5V, V_{EN} = 0V	T_J = +25℃		0.03	2	μA
			T_J = -40℃ to +125℃			14.5	
Input Under-Voltage Lockout Threshold	V_{UVLO}	V_{IN} rising, no load		2.45	2.55	2.65	V
Input Under-Voltage Lockout Hysteresis	V_{UVLO_HYS}	V_{IN} falling hysteresis, no load			300		mV
Thermal Shutdown	T_{SD}	Junction temperature rising			165		℃
		Junction temperature falling			135		
EN Input							
High-Level Threshold at EN Pin	V_{IH}	V_{IN} = 2.7V to 5.5V		1.2			V
Low-Level Threshold at EN Pin	V_{IL}	V_{IN} = 2.7V to 5.5V				0.4	V
EN Input Leakage Current	I_{EN_LKG}	V_{EN} = 3.6V			3.6		μA
Soft-Start, Power Good							
Soft-Start Time	t_{SS}	Time from the first pulse to 95% of V_{OUT} nominal			1.3		ms
Power Good Threshold	V_{PG}	V_{FB} rising, referenced to V_{FB} nominal			90		% × V_{FB_NOM}
		V_{FB} falling, referenced to V_{FB} nominal			85		
Power Good Over-Voltage Threshold	V_{PG_OV}	PG OV threshold rising			115		
		PG OV threshold falling			110		
Power Good Low-Level Output Voltage	V_{PG_OL}	I_{SINK} = 1mA			0.1	0.3	V
PG Internal Pull-up Resistor	R_{PG}				570		kΩ
Power Good Delay Time	t_{PG_DLY}	PG rising edge			105		μs
Output and Feedback							
Feedback Regulation Voltage (ADJ)	V_{FB_NOM}	V_{IN} = 2.7V to 5.5V	T_J = +25℃	0.596	0.600	0.604	V
			T_J = -40℃ to +125℃	0.591	0.600	0.609	
Feedback Input Leakage Current	I_{FB_LKG}	V_{FB} = 0.65V			1	50	nA
Output Discharge Resistor	R_{DIS}	V_{EN} = low, V_{OUT} = 1.2V			140		Ω
Power Switch							
High-side FET On-Resistance	R_{DSON}	V_{IN} = 2.7V			24		mΩ
		V_{IN} = 3.6V			19	33	
Low-side FET On-Resistance		V_{IN} = 2.7V			12		mΩ
		V_{IN} = 3.6V			9	18	
PMOS SW Leakage Current	I_{SW_LKG}	V_{IN} = 5.5V			0.4	13.5	μA
NMOS SW Leakage Current		V_{IN} = 5.5V		-3.5	-0.08		
High-side Peak Current Limit	I_{LIM_H}	T_J = -40℃ to +125℃		10.3	13	14.8	A
Low-side Valley Current Limit	I_{LIM_L}	T_J = -40℃ to +125℃		7.2	11	14.6	
Low-side Negative Current Limit	I_{LIM_LN}	FPWM mode, OVP			-5		A
Low-side ZCD Threshold	I_{ZCD}	PSM mode, V_{OUT} = 1.8V			200		mA
Switching Frequency	f_{SW}	FPWM mode, V_{IN} = 3.6V, V_{OUT} = 1.2V, I_{OUT} = 1A		0.9	1.2	1.5	MHz
Controller							
Minimum Off-Time	t_{OFF_MIN}	V_{IN} = 3.4V, V_{OUT} = 3.3V			45		ns
FPWM Mode Threshold	V_{M_FPWM}	V_{IN} = 3.6V, V_{EN} = 2V		1.2			V
PSM Mode Threshold	V_{M_PSM}	V_{IN} = 3.6V, V_{EN} = 2V				0.4	V

TYPICAL PERFORMANCE CHARACTERISTICS

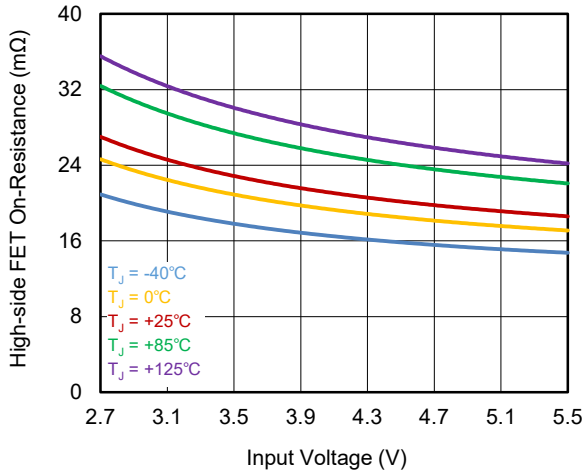
Quiescent Current vs. Input Voltage (PSM)



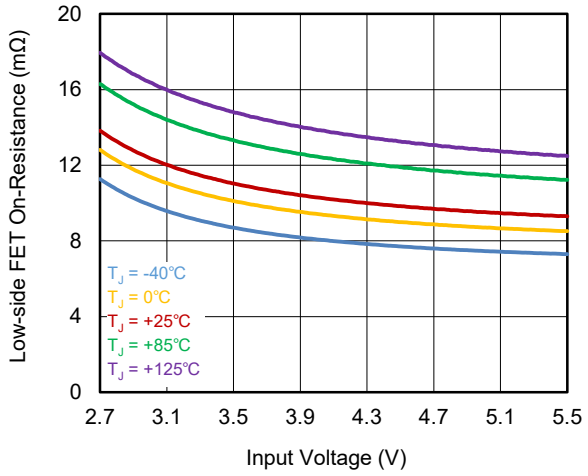
Quiescent Current vs. Input Voltage (FPWM)



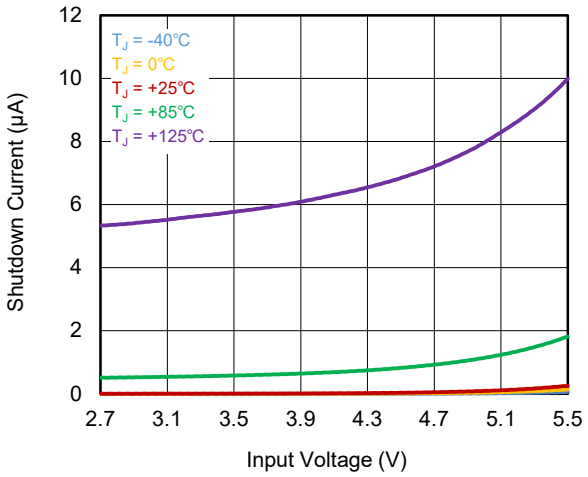
High-side FET On-Resistance vs. Input Voltage



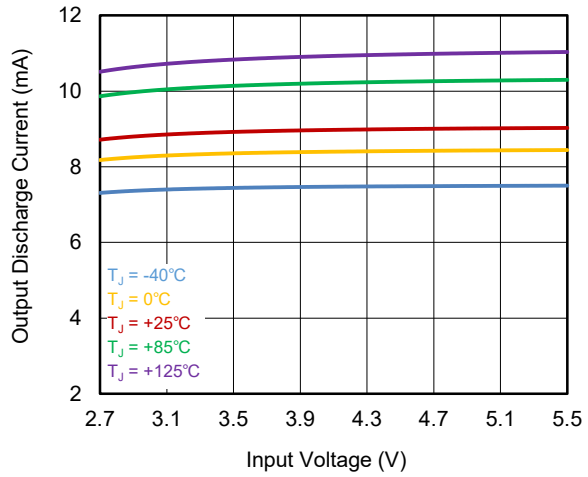
Low-side FET On-Resistance vs. Input Voltage



Shutdown Current vs. Input Voltage



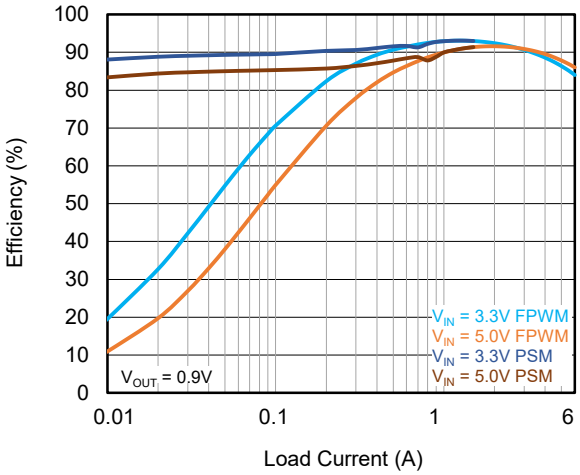
Output Discharge Current vs. Input Voltage



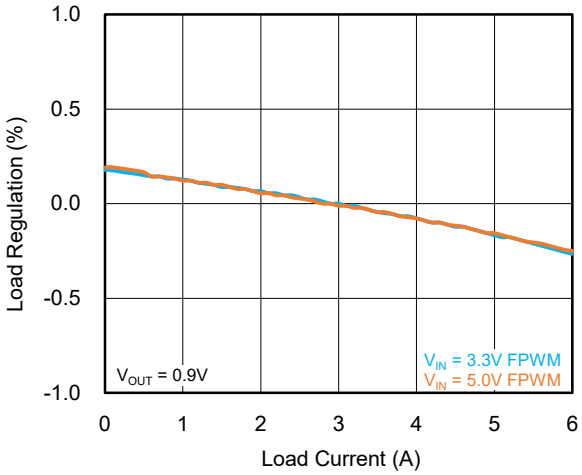
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

V_{IN} = 5V, V_{OUT} = 0.9V, L_1 = 0.47μH (DCR = 4.1mΩ), and C_{OUT} = 3 × 22μF, T_A = +25℃, unless otherwise noted.

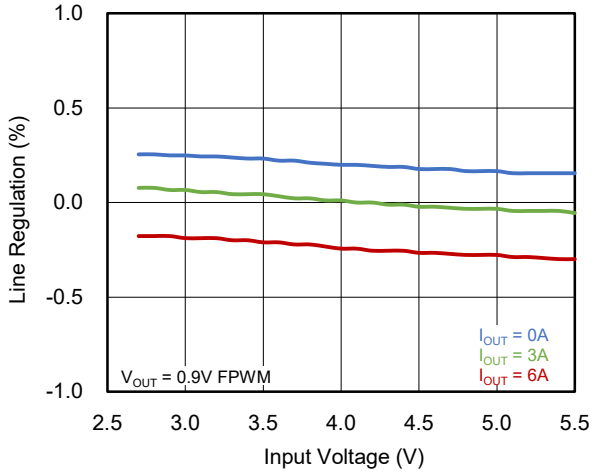
Efficiency vs. Load Current



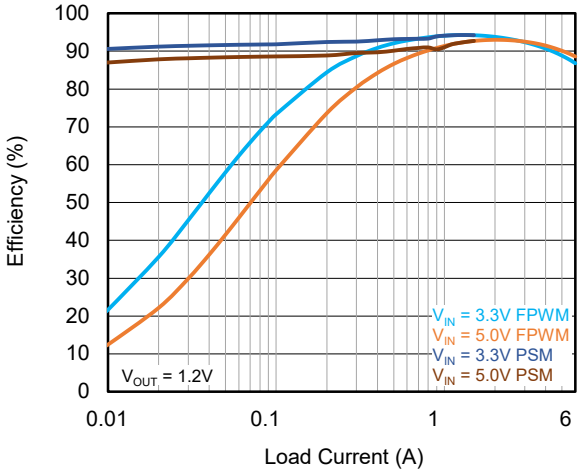
Load Regulation vs. Load Current



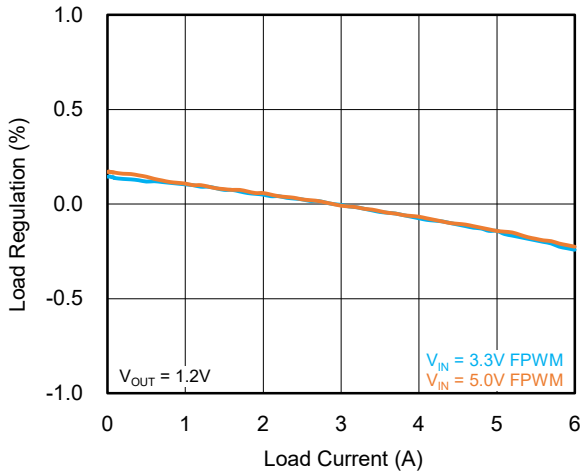
Line Regulation vs. Input Voltage



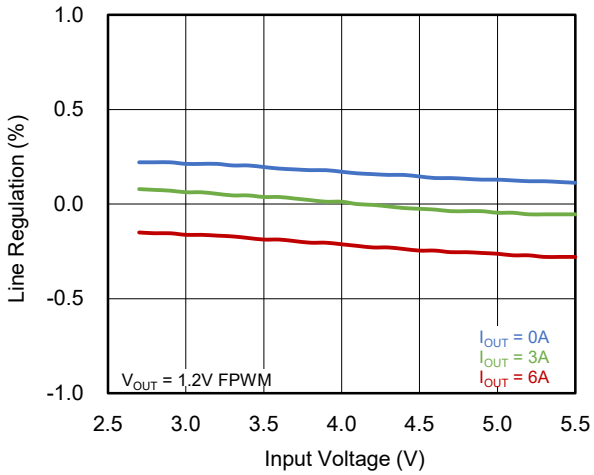
Efficiency vs. Load Current



Load Regulation vs. Load Current



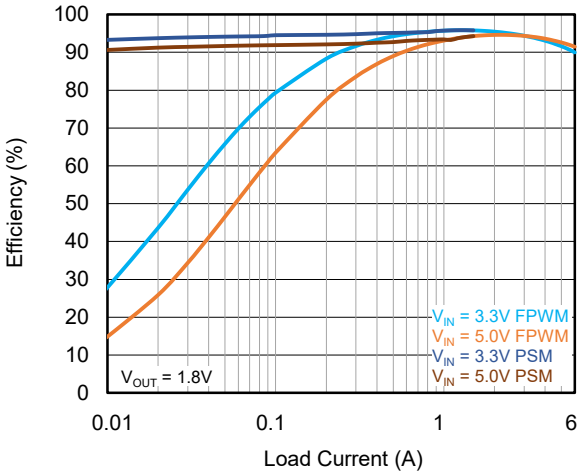
Line Regulation vs. Input Voltage



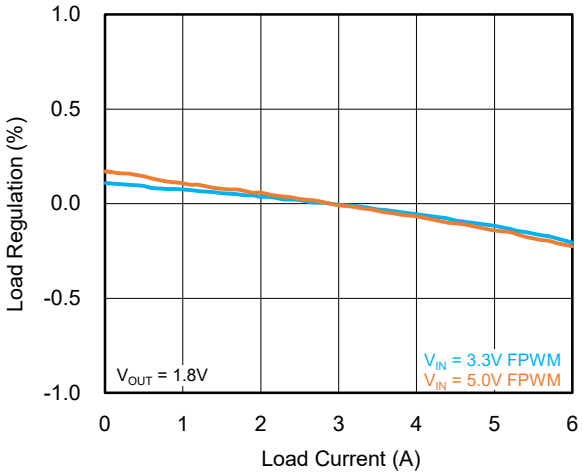
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

V_{IN} = 5V, V_{OUT} = 0.9V, L_1 = 0.47μH (DCR = 4.1mΩ), and C_{OUT} = 3 × 22μF, T_A = +25℃, unless otherwise noted.

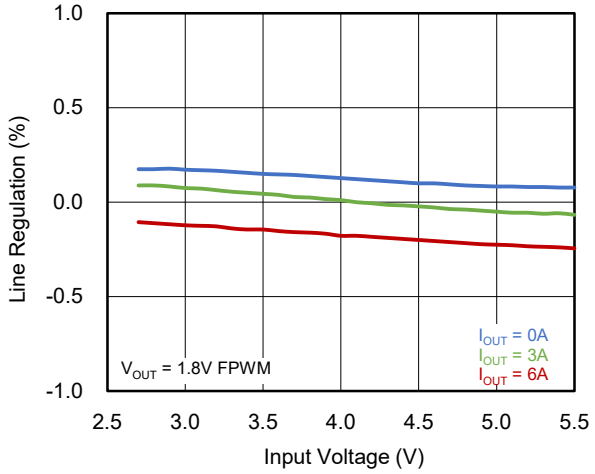
Efficiency vs. Load Current



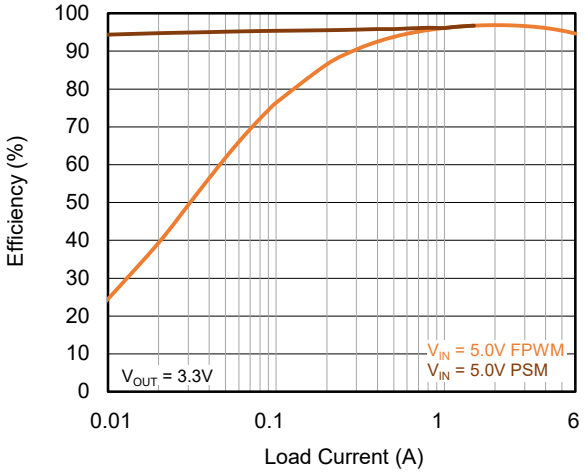
Load Regulation vs. Load Current



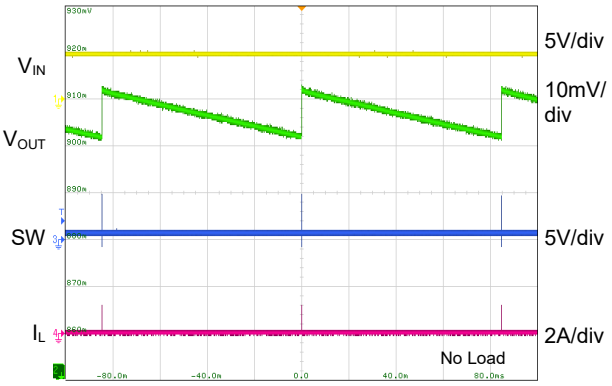
Line Regulation vs. Input Voltage



Efficiency vs. Load Current

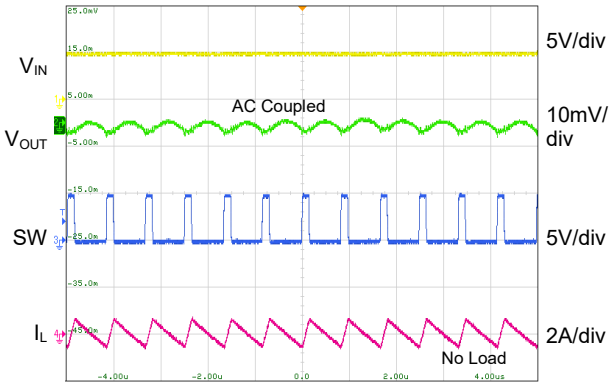


Steady State (PSM)



Time (20ms/div)

Steady State (FPWM)

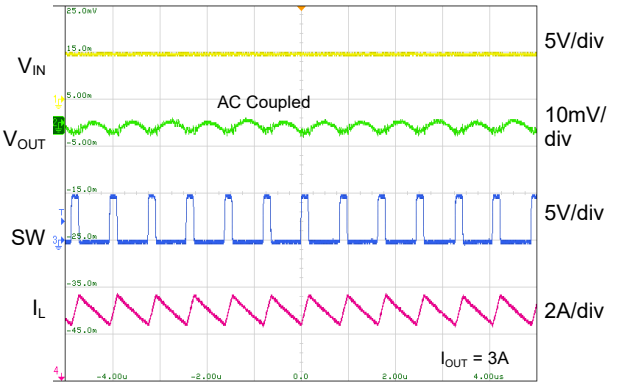


Time (1μs/div)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

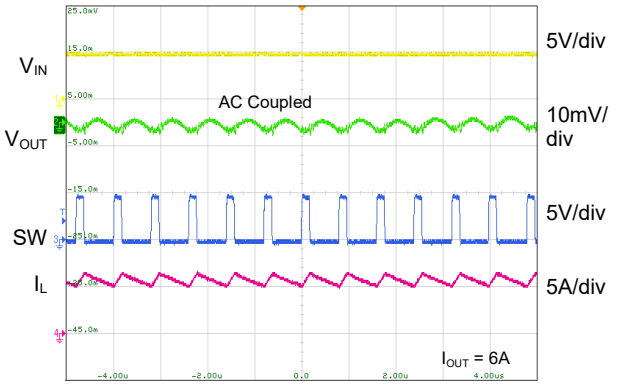
V_{IN} = 5V, V_{OUT} = 0.9V, L_1 = 0.47μH (DCR = 4.1mΩ), and C_{OUT} = 3 × 22μF, T_A = +25℃, unless otherwise noted.

Steady State (FPWM)



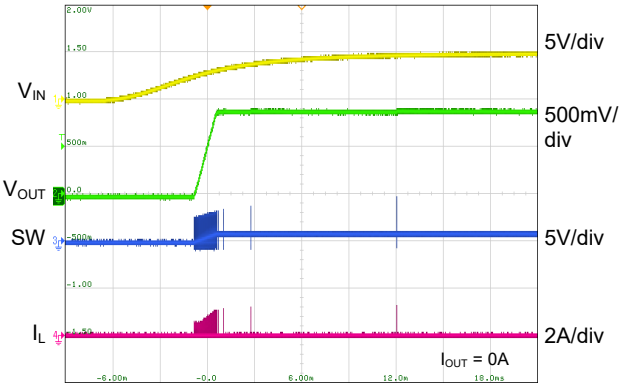
Time (1μs/div)

Steady State (FPWM)



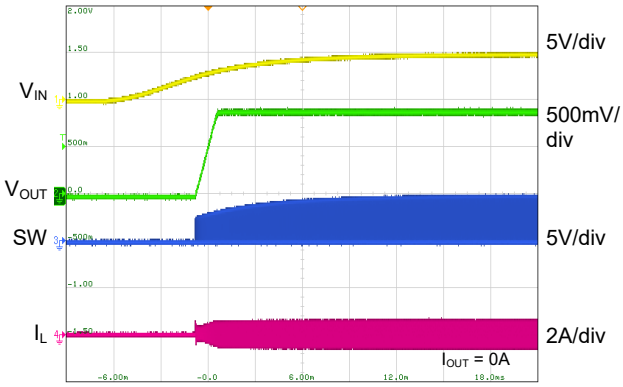
Time (1μs/div)

Power Up (PSM)



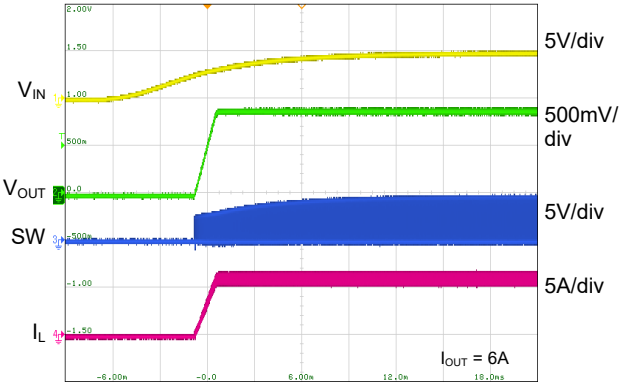
Time (3ms/div)

Power Up (FPWM)



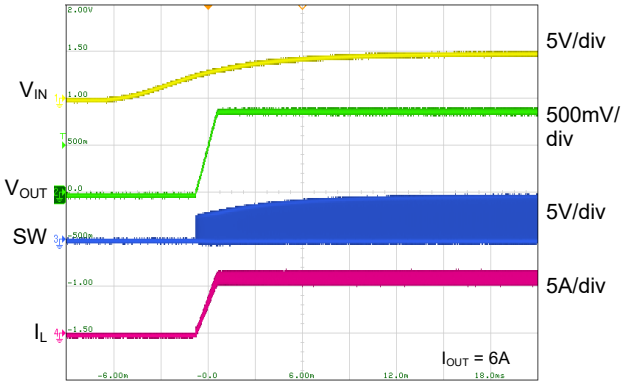
Time (3ms/div)

Power Up (PSM)



Time (3ms/div)

Power Up (FPWM)

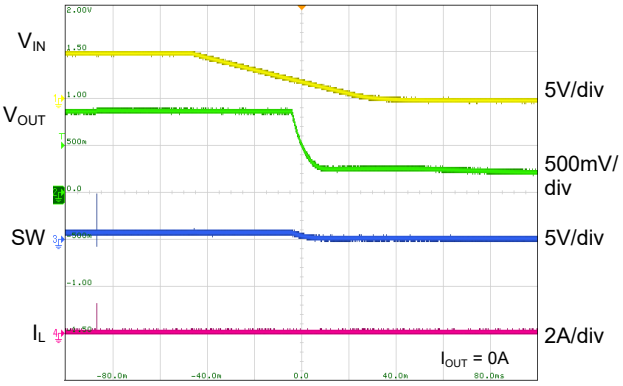


Time (3ms/div)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

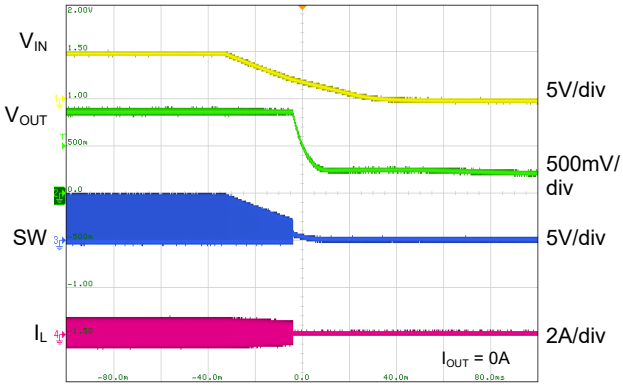
V_{IN} = 5V, V_{OUT} = 0.9V, L_1 = 0.47μH (DCR = 4.1mΩ), and C_{OUT} = 3 × 22μF, T_A = +25℃, unless otherwise noted.

Power Off (PSM)



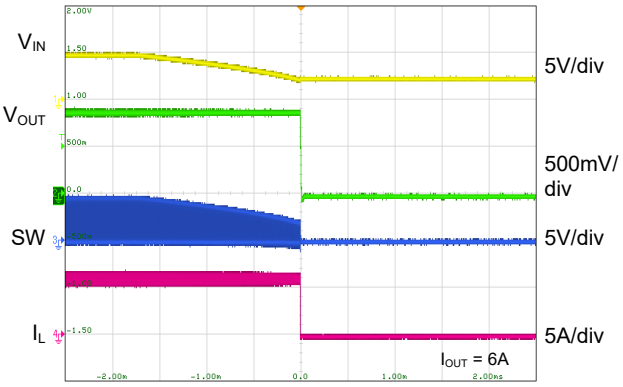
Time (20ms/div)

Power Off (FPWM)



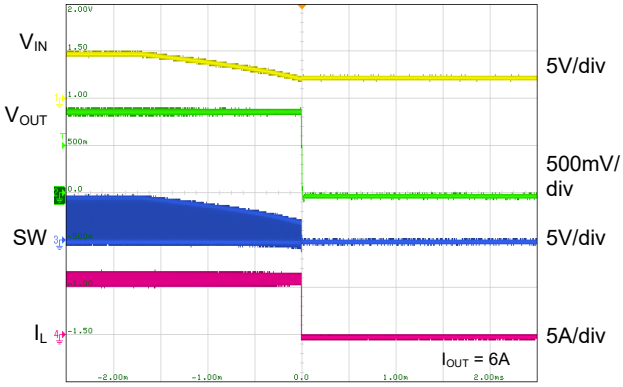
Time (20ms/div)

Power Off (PSM)



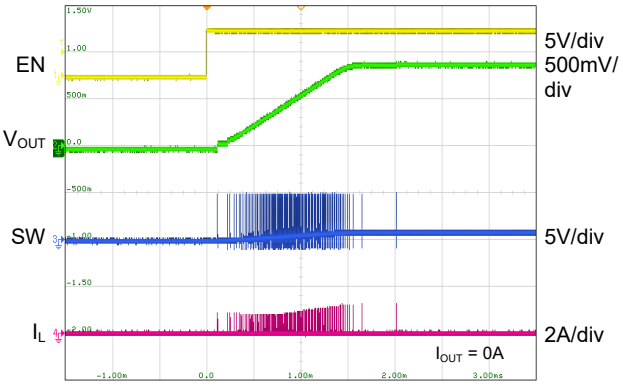
Time (500μs/div)

Power Off (FPWM)



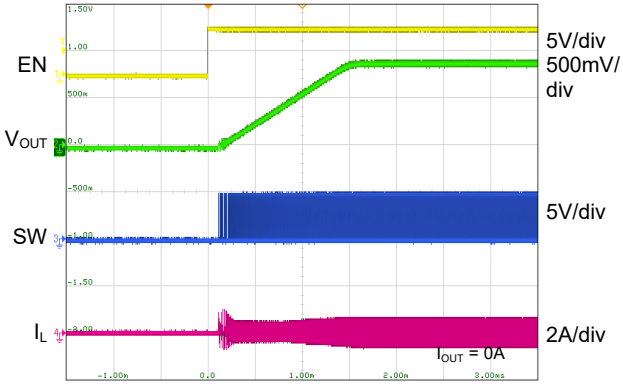
Time (500μs/div)

Enable On (PSM)



Time (500μs/div)

Enable On (FPWM)

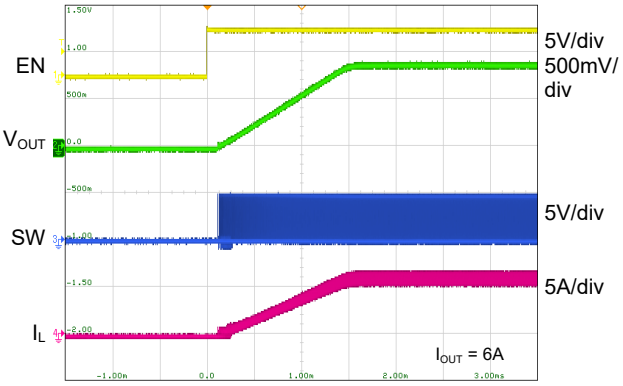


Time (500μs/div)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

V_{IN} = 5V, V_{OUT} = 0.9V, L_1 = 0.47μH (DCR = 4.1mΩ), and C_{OUT} = 3 × 22μF, T_A = +25℃, unless otherwise noted.

Enable On (PSM)



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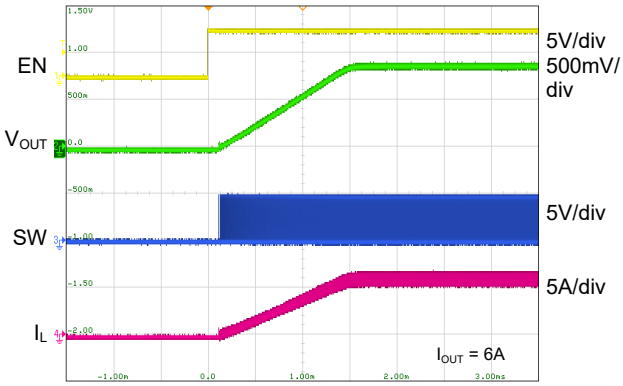
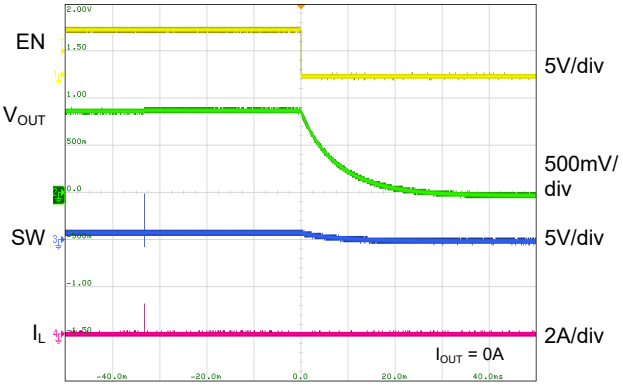
Enable On (FPWM)



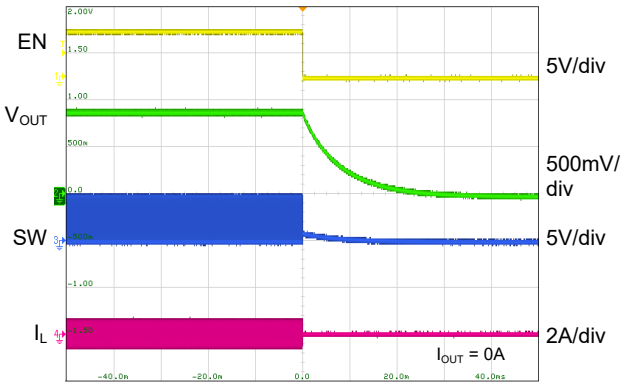
Time (500μs/div)

Enable Shutdown (PSM)



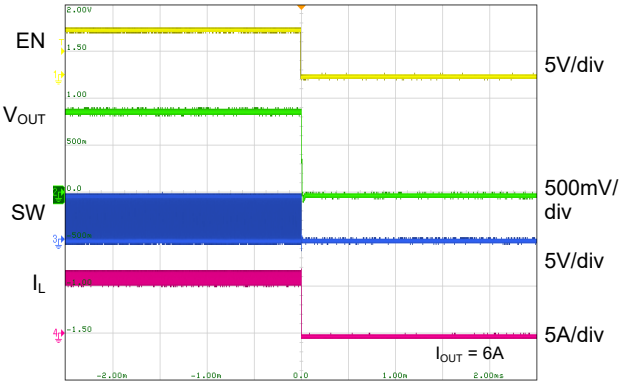
Time (10ms/div)

Enable Shutdown (FPWM)



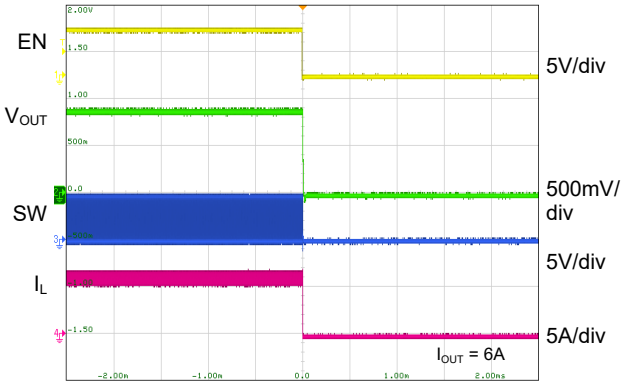
Time (10ms/div)

Enable Shutdown (PSM)



Time (500μs/div)

Enable Shutdown (FPWM)

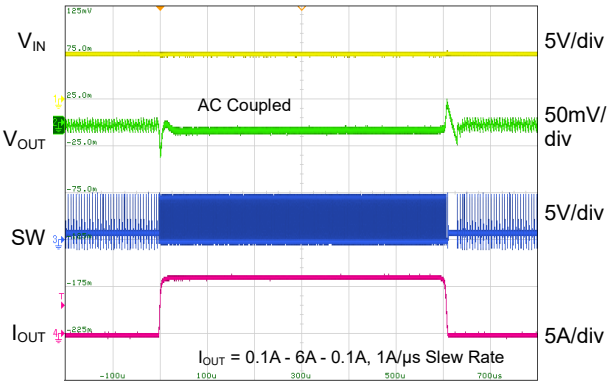


Time (500μs/div)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

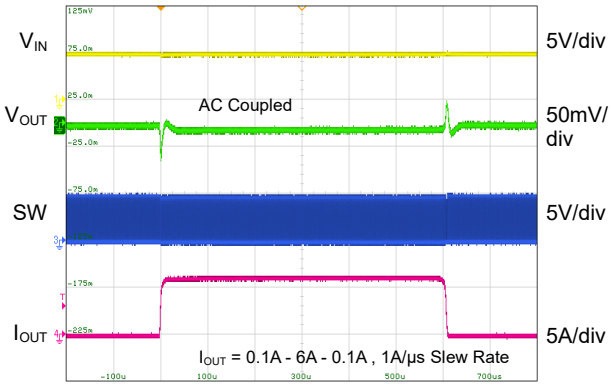
V_{IN} = 5V, V_{OUT} = 0.9V, L_1 = 0.47μH (DCR = 4.1mΩ), and C_{OUT} = 3 × 22μF, T_A = +25℃, unless otherwise noted.

Load Transient Response (PSM)



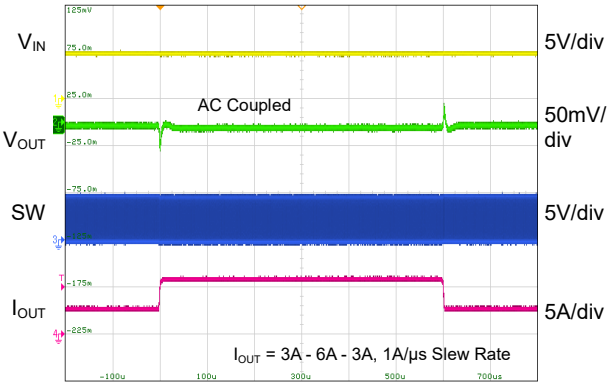
Time (100μs/div)

Load Transient Response (FPWM)



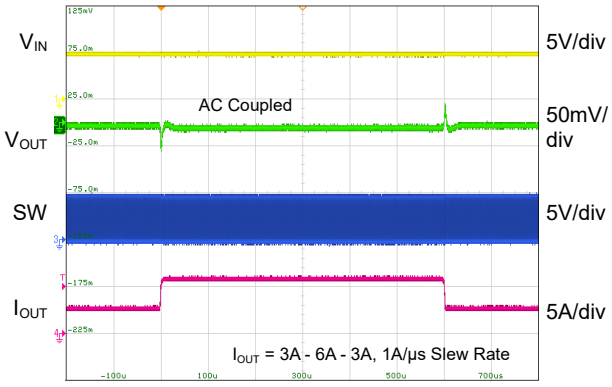
Time (100μs/div)

Load Transient Response (PSM)



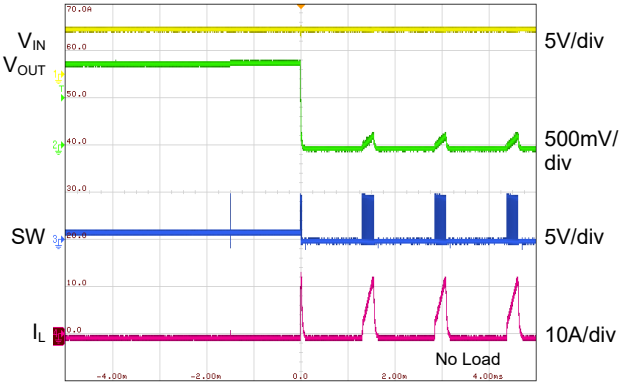
Time (100μs/div)

Load Transient Response (FPWM)



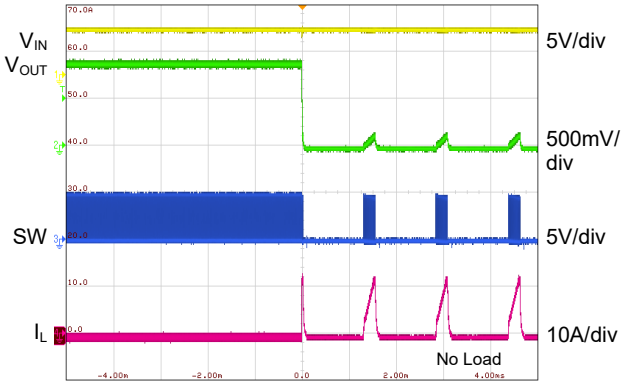
Time (100μs/div)

Hiccup with Output Short (PSM, Entry)



Time (1ms/div)

Hiccup with Output Short (FPWM, Entry)

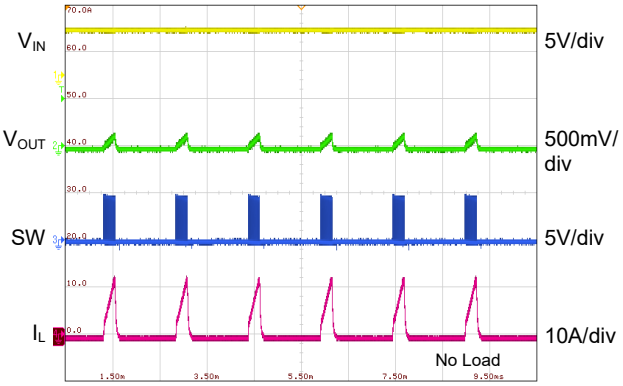


Time (1ms/div)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

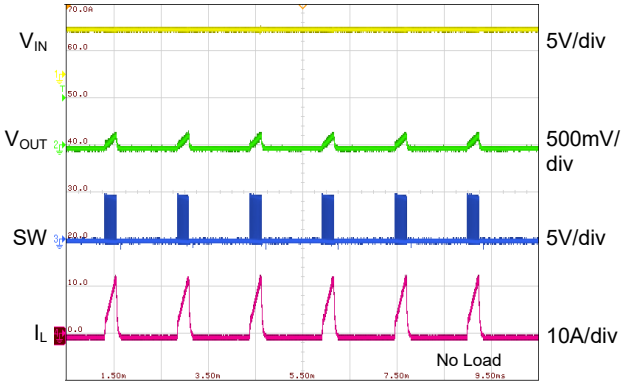
V_{IN} = 5V, V_{OUT} = 0.9V, L_1 = 0.47μH (DCR = 4.1mΩ), and C_{OUT} = 3 × 22μF, T_A = +25℃, unless otherwise noted.

Hiccup with Output Short (PSM, Steady)



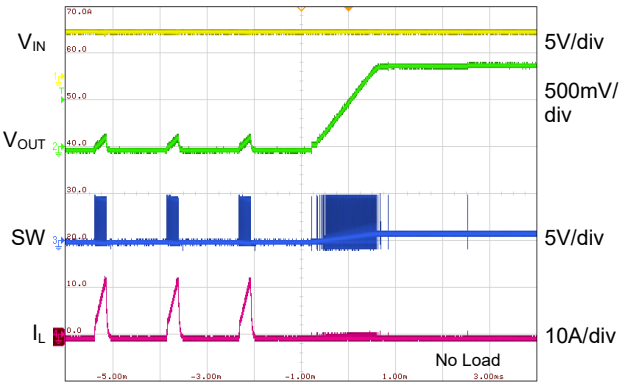
Time (1ms/div)

Hiccup with Output Short (FPWM, Steady)



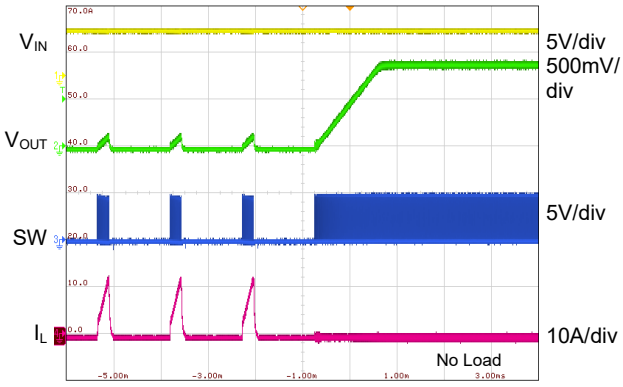
Time (1ms/div)

Hiccup with Output Short (PSM, Recovery)



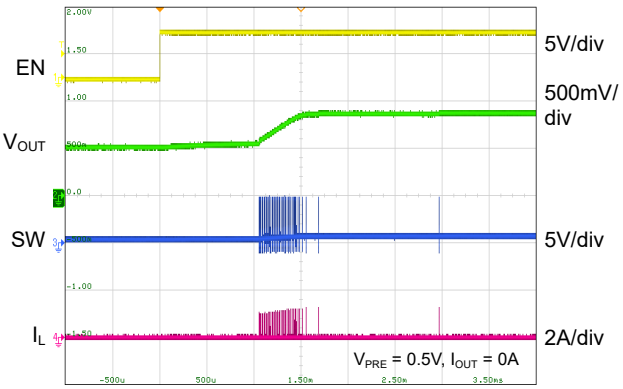
Time (1ms/div)

Hiccup with Output Short (FPWM, Recovery)



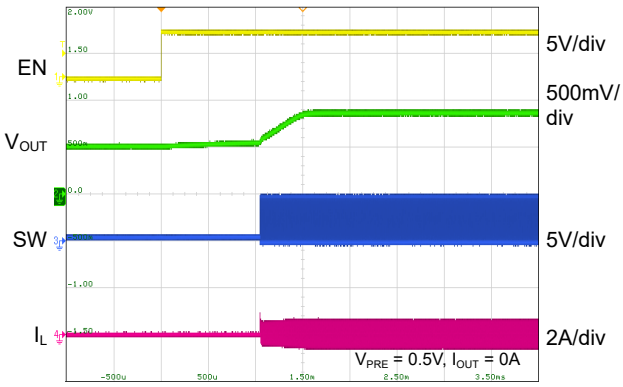
Time (1ms/div)

V_{OUT} Pre-bias Start Up (PSM)



Time (500μs/div)

V_{OUT} Pre-bias Start Up (FPWM)



Time (500μs/div)

FUNCTIONAL BLOCK DIAGRAM

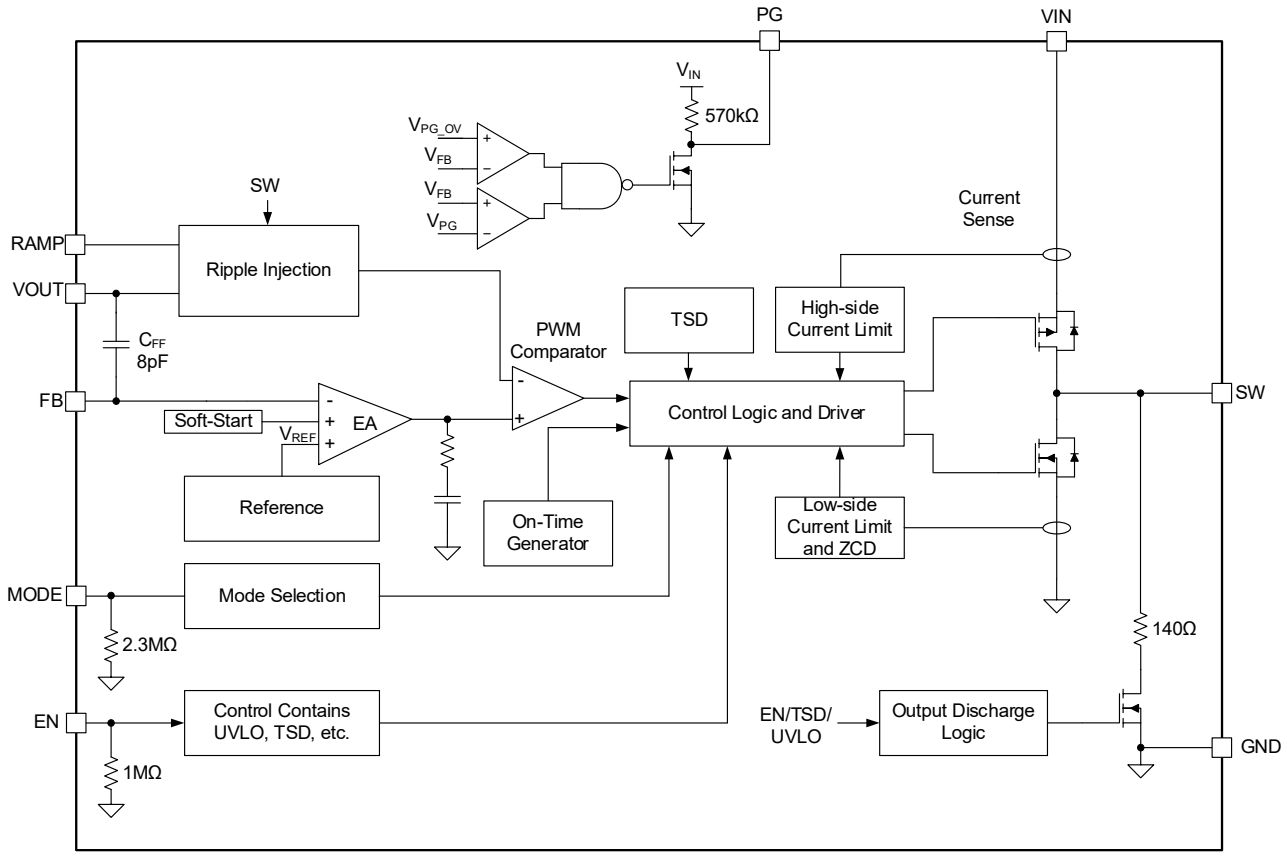


Figure 2. Block Diagram

DETAILED DESCRIPTION

Overview

The SGM61061S is a high efficiency synchronous Buck switching converter. The device operates in an AHP-COT control scheme. The device operates at a typically 1.2MHz switching frequency in FPWM mode. Based on the V_{IN}/V_{OUT} ratio, a simple circuit sets the required on-time for the high-side MOSFET. It makes the switching frequency relatively constant regardless of the variation of input voltage, output voltage, and load current at PWM state.

Under-Voltage Lockout (UVLO)

To avoid mis-operation of the device at low input voltages, under-voltage lockout is implemented that shuts down the device when input voltage lower than V_{UVLO} (when V_{IN} voltage falls) with 300mV (TYP) hysteresis. When the input voltage is higher than 2.55V (TYP), the device will recover to normal operation.

Soft-Start and Pre-Biased Output

A 1.3ms internal soft-start circuit is included to prevent input inrush current and input voltage drops during startup. This circuit slowly ramps up the error amplifier reference voltage (V_{REF} = 0.6V) after exiting the shutdown state or under-voltage lockout (UVLO). Slow increase of the output voltage prevents the excessive inrush current for charging the output capacitors and creates a smooth output voltage rise. The other advantage of a soft-start is avoiding supply voltage drops especially on the high internal impedance sources such as the primary cells and rechargeable batteries.

The SGM61061S is also capable of starting with a pre-biased output capacitor when it is powered up or enabled. When the device is turning on, a bias on the output is likely to exist due to other sources connected to the load(s) such as multi-voltage ICs or simply because of residual charges on the output capacitors. For example, when a device with light load is disabled and re-enabled, the output voltage cannot drop too much during the off period and the device must restart under pre-biased output condition. Without the pre-biased capability, the device cannot be able to start up properly. The output ramp is automatically initiated to the bias voltage and ramps up to the nominal output value.

Device Enable and Disable

The SGM61061S is enabled by setting the EN pin input to higher than 1.2V. It is disabled when EN pin falls lower than 0.4V. If the device is enabled, the internal power stage starts switching and regulates the output voltage to the setting point voltage. In shutdown mode, the internal power switches as well as the entire control circuitry are turned off. The output discharge FET is turned on.

Power Good Output (PG)

SGM61061S has a power good output. The PG pin is pulled to high-level once FB voltage reaches 90% (TYP) of the reference voltage, and is driven low once FB voltage falls below 85% (TYP) of the reference voltage. If the FB voltage is higher than 115% (TYP) of the reference voltage, the PG pin becomes low, then the FB voltage is reduced to 110% (TYP) of the reference voltage, and the PG pin is pulled to the high-level. The PG pin is an open-drain output with internal pull-up resistor connected to V_{IN}. It is recommended that the sink current should not exceed 1mA. There is a 105μs delay between when V_{FB} reaches PG threshold to when the PG pin is pulled to high. The PG signal can be used for sequencing of multiple rails by connecting it to the EN pin of other converters. Leave the PG pin unconnected when not used.

Table 1. PG Output State in Different Conditions

Reason	Conditions	PG State	
		High	Low
FB Voltage	EN = High, $V_{PG\_OV} \geq V_{FB} \geq V_{PG}$	√	
	EN = High, $V_{FB} < V_{PG}$		√
	EN = High, $V_{FB} > V_{PG\_OV}$		√
Shutdown by EN	EN = Low		√
Thermal Shutdown	$T_J > T_{SD}$		√
UVLO (1)	$1.4V < V_{IN} < V_{UVLO}$		√
Power Supply Removal (1)	$V_{IN} \leq 1.4V$	Uncertainty	

NOTE: 1. PG pin is connected to VIN pin with an external 570kΩ resistor.

DETAILED DESCRIPTION (continued)

Low Dropout Operation (100% Duty Cycle)

When the input voltage gradually drops to the regulation output voltage, the SGM61061S can operate at 100% duty cycle and keep the high-side MOSFET continuously on for minimal input-to-output voltage difference. The low-side MOSFET is kept off. In this mode, the lowest input voltage for keeping the output regulated is determined by load current and the resistive drops from the input to the output as given in Equation 1:

$$V_{IN\_MIN} = V_{OUT} + I_{OUT\_MAX} \times (R_{DSON} + R_L) \quad (1)$$

where:

V_{IN_MIN} is minimum input voltage to maintain output voltage in regulation.

I_{OUT_MAX} is maximum output current.

R_{DSON} is high-side MOSFET on-resistance.

R_L is inductor DC resistance (DCR).

Mode Selection

This device can switch between FPWM and PSM work modes. SGM61061S switches to FPWM mode if the MODE pin voltage is more than 1.2V. Although the efficiency is low when load is light in FPWM mode, the VOUT ripple is low and the frequency is relatively fixed. Once the MODE pin voltage falls below 0.4V or floats, SGM61061S switches to PSM mode which has a reduced switching frequency and works with the minimum quiescent current to keep high efficiency at light load. At medium to heavy loads, it operates in pulse width modulation (PWM) state with 1.2MHz (TYP) switching frequency.

Current Limit and Hiccup Mode Short-Circuit Protection

The switch current limit avoids high inductor current and drawing excessive current from a battery or input voltage rail. Excessive current might occur with a heavy load or shorted output circuit condition. The SGM61061S keeps sensing the current of the high-side switch. Once the high-side switch current limit is reached, the high-side switch is turned off and low-side switch is turned on to reduce the inductor current until the current is lower than low-side valley current limit threshold.

If the current limit persists uninterrupted for more than 16 cycles, the device stops switching. A new soft-start is initiated automatically (hiccup) after 1.3ms (TYP). The hiccup repeats until the overload or short-circuit fault is cleared.

Negative Current Limit

In PSM mode, the low-side MOSFET will be turned off once the low-side current fall to I_{ZCD} to maintain high efficiency at light load. However in FPWM mode, the I_{ZCD} changed to negative current, which is defined as negative current limit (I_{LIM_LN}). When the input and output conditions are unchanged, if the low-side current drops to I_{LIM_LN}, the low-side MOSFET will be turned off in advance, then the high-side MOSFET is turned on.

Output Over-Voltage Protection (OVP)

The device contains an over-voltage protection circuit to avoid high overshoots of the output voltage during operation. To minimize the overshoots, the device monitors the FB pin voltage and compares it to the internal OVP threshold. OVP is triggered while the FB voltage rising above 115% (TYP) of reference voltage, and is released while the FB voltage falls below typically 110% (TYP) of reference voltage. When the FB voltage drops below the OVP threshold, the high-side MOSFET can be turned on again in the next cycle.

Output Discharge Function

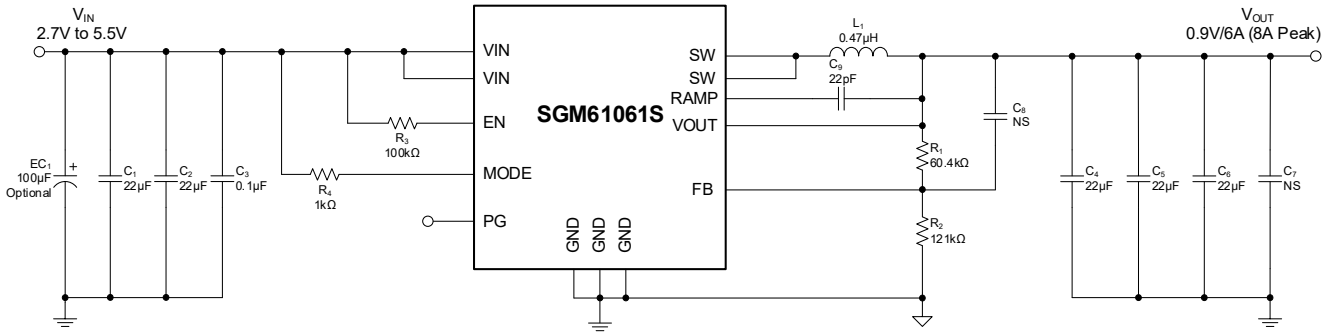
If the device is in any of the following states: UVLO, shutdown by EN, OTP, an internal output discharge FET is turned on and discharges the output through the SW pin smoothly, the resistance of discharge FET is about 140Ω (TYP).

Thermal Shutdown

Thermal protection is designed to protect the die against over-heating damage. If the junction temperature exceeds T_{SD} threshold, the switching stops and the device shuts down. Automatic recovery with a soft-start will begin when the junction temperature drops below the +135℃ (TYP) falling threshold.

APPLICATION INFORMATION

In this section, power supply design with the SGM61061S synchronous Buck converter and selection of the external components will be explained based on the typical application that is applicable for various input and output voltage combinations.



NOTE: If SGM61061S works in PSM mode (MODE pin < 0.4V or floating) and there is no load condition (load current < 13.5μA), the resistance of R_2 must be less than 45kΩ.

Figure 3. SGM61061S Circuit for 0.9V Output

Design Requirements

Table 2 summarizes the requirements for this example as shown in Figure 3. The selected components are given in Table 3.

Table 2. Design Parameters for the Application Example

Design Parameter	Example Value
Input Voltage	2.7V to 5.5V
Output Voltage	0.9V
Output Current	≤ 8A
Mode Selection	FPWM

Table 3. Selected Components for the Design Example

REF	Description	Manufacturer
C_1, C_2	22μF, 10V, 20%, 0603, X5R P/N: GRM188R61A226ME15	muRata
C_3	0.1μF, 16V, 10%, 0603, X7R	Standard
C_4, C_5, C_6	22μF, 6.3V, 20%, 0603, X7T P/N: GRM188D70J226ME01D	muRata
C_9	22pF, ±5%, 50V,C0G,0603	Standard
L_1	0.47μH, Wire Wound, DCRMAX = 4.1mΩ, I_{SAT} (20%) = 13.4A, I_{RMS} (40℃) = 19.7A, SRF = 61MHz, 4mm × 4mm × 2mm P/N: WCX0420CR47MT	Sunlord
R_1	60.4kΩ, 1%, 0603	Standard
R_2	121kΩ, 1%, 0603	Standard
R_3	100kΩ, 1%, 0603	Standard
R_4	1kΩ, 1%, 0603	Standard
U1	SGM61061S, 2.7V to 5.5V Input, 6A (8A Peak) Synchronous Buck Converter, TQFN-2×3-12L	SGM

NOTE: If the long input power cable is used, EC_1 should be installed.

Input Capacitor Selection (C_{IN})

The input capacitor is the low impedance energy source for the converter that helps provide stable operation. A low ESR multilayer ceramic capacitor is recommended for best filtering. In most cases, two 22μF input capacitors are recommended, a larger value reduces input voltage ripple and improves system stability. Usually a 0.1μF low ESR ceramic capacitor needs to be connected between the VIN and GND pins as closely as possible.

Inductor Selection (L)

The important factors for inductor selection are inductance (L), saturation current (I_{SAT}), RMS rating (I_{RMS}), DC resistance (DCR) and dimensions. Use Equation 2 to find the inductor peak current (I_{L_MAX}) and peak-to-peak ripple current (ΔI_L) in static conditions:

$$I_{L\_MAX} = I_{O\_MAX} + \frac{\Delta I_L}{2}$$
$$\Delta I_L = V_{OUT} \times \frac{1-D}{L \times f_{SW}} \quad (2)$$

I_{O_MAX} is the maximum load current, $D = V_{OUT}/V_{IN}$ represents duty cycle and f_{SW} is the switching frequency.

APPLICATION INFORMATION (continued)

Typically, the peak-to-peak inductor current is selected between 10% and 30% of the maximum output current. The inductor of the saturation current is 20% higher than I_{L_MAX} is recommended. The inductor initial tolerance can be as high as -20% to +20% of the nominal value and proper current derating is usually required. Generally, choosing the saturation current above high-side limit is enough. It should be noted that low-side current should avoid falling to negative current limit when no load in FPWM mode. In addition, DC resistance and size should also be taken into account when selecting an appropriate inductor. Larger inductance values reduce the ripple current but lead to sluggish transient response. L_1 = 0.47μH is the recommended values for the typical application.

Output Capacitor Selection (C_{OUT})

The architecture of the SGM61061S allows use of tiny ceramic-type output capacitors with low equivalent series resistance (ESR). These capacitors provide low output voltage ripple and are thus recommended. To keep the resistance up to high frequencies and to achieve narrow capacitance variation with temperature, it is recommended to use X7R or X5R dielectric. Bias voltage can cause significant capacitance drops in the ceramic capacitors. The effective deviation of a ceramic capacitor can be as high as -50% to +20% of the nominal value. C_{OUT} = 3 × 22μF is the recommended values for the typical application.

Output Voltage Setting

Use Equation 3 to select the R_1/R_2 resistor divider to set the V_{OUT}. The parasitic capacitance of the FB pin and R_1 form a low-pass filter, which can effectively filter out high-frequency interference input from the FB pin. However, it also adds a pole to the control loop, and if the frequency of this pole is too low, the stability of the system will be reduced.

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R_1}{R_2}\right) = 0.6V \times \left(1 + \frac{R_1}{R_2}\right) \quad (3)$$

The recommended resistors values for common output voltages are listed in Table 4.

Table 4. Resistor Values for Common Output Voltages

V_{OUT} (V)	R_1 (kΩ)	R_2 (kΩ)
0.9	60.4 (1%)	121 (1%)
1.2	100 (1%)	100 (1%)
1.8	200 (1%)	100 (1%)
3.3	390 (1%)	86.6 (1%)

NOTE: If SGM61061S works in PSM mode (MODE pin < 0.4V or floating) and there is no load condition (load current < 13.5μA), the resistance of R_2 must be less than 45kΩ.

Load Transient Optimization

A feed-forward capacitor reduces the output ripple in PSM and improves the load transient response. Meanwhile, an 8pF feed-forward capacitor is integrated internally. If it is necessary to reduce the drop of output voltage at load transient, the response speed of the system can be improved by increasing the C_{FF} (C_8) capacitance value. Adding a capacitor (C_9) will improve the load transient response between RAMP pin and VOUT pin. The improvement effect is more significant if the capacitor is larger. However, excessive C_{FF} (C_8) capacitance or C_9 capacitance will reduce the stability of the system, which can be compensated by increasing the output capacitance value. The recommended capacitance value for C_9 is less than 60pF in Figure 3.

APPLICATION INFORMATION (continued)

Various Output Voltages

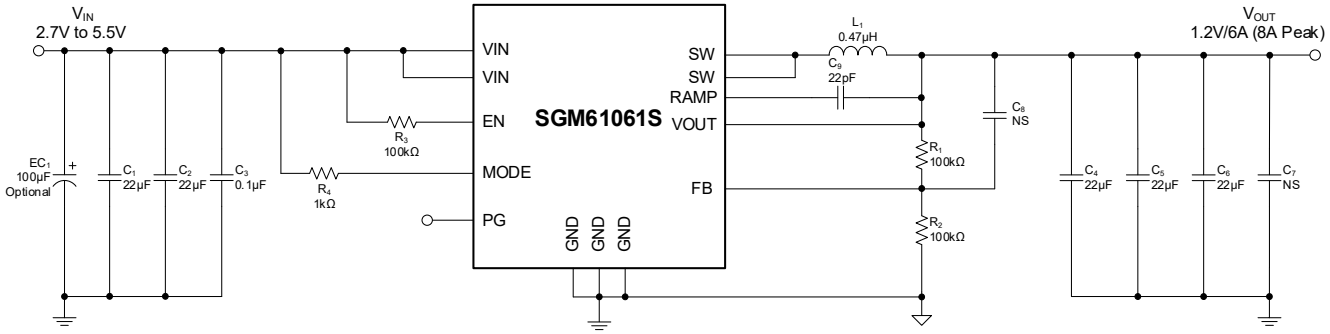


Figure 4. SGM61061S Circuit for 1.2V Output

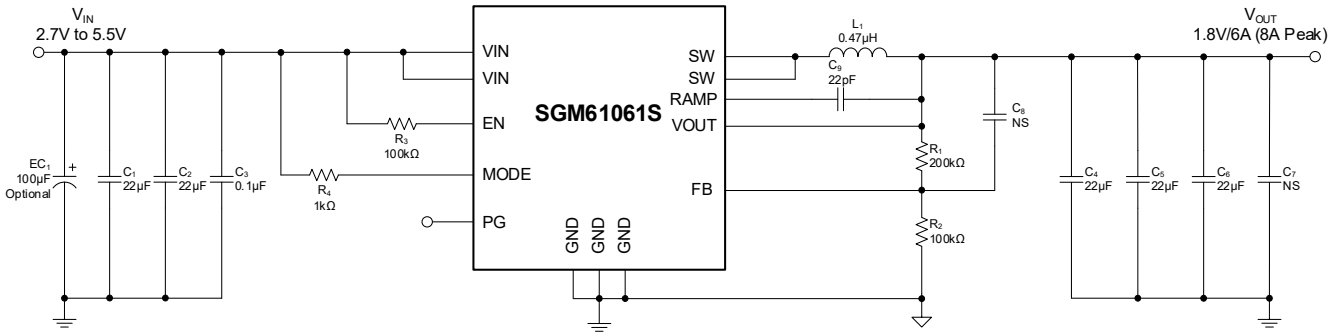


Figure 5. SGM61061S Circuit for 1.8V Output

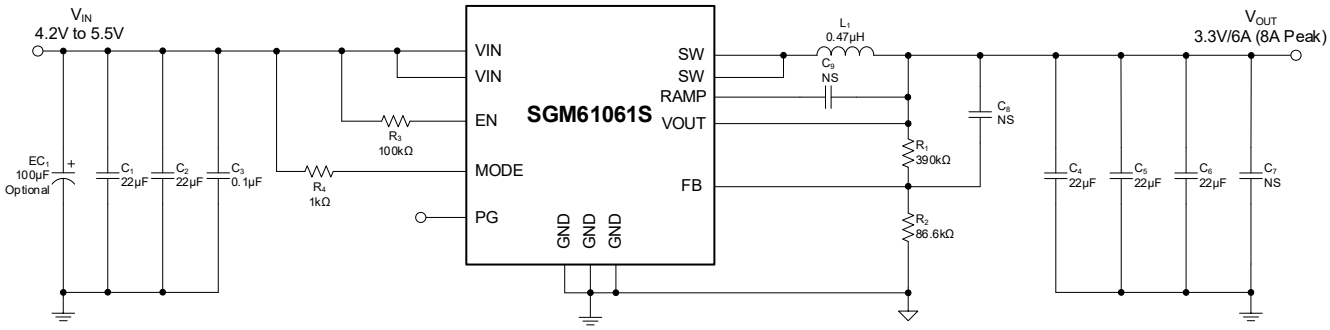
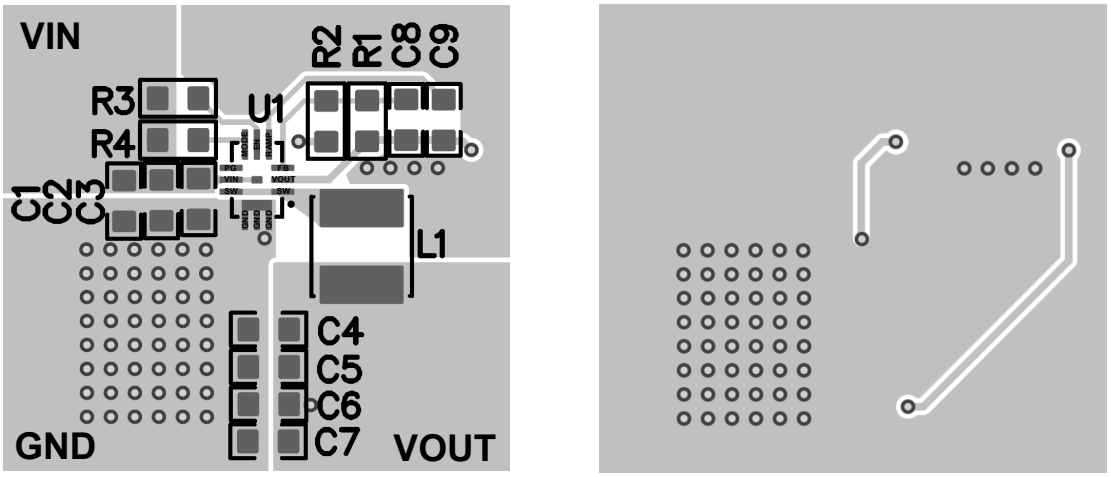


Figure 6. SGM61061S Circuit for 3.3V Output

Layout Guidelines

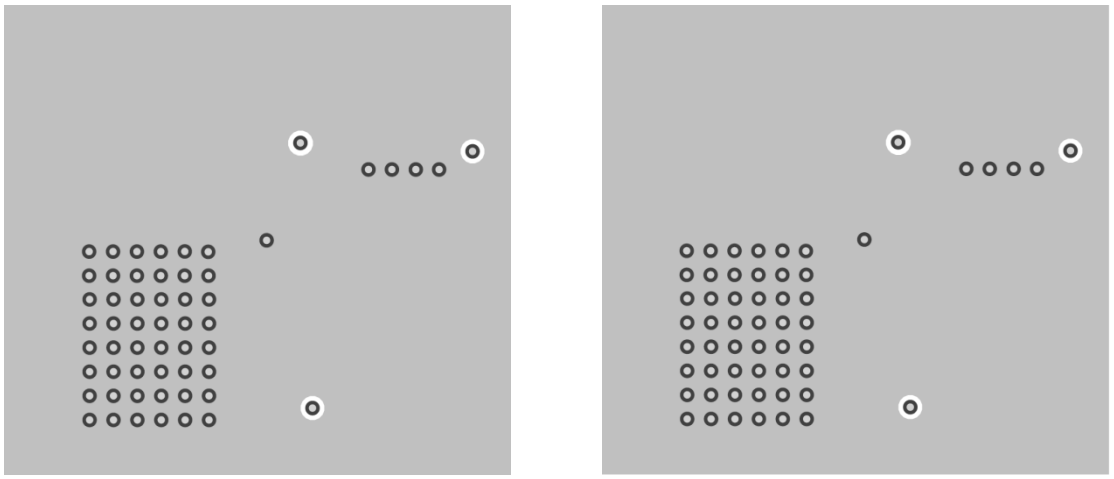
A good printed-circuit-board (PCB) layout is a critical element of any high-performance design. Follow the guidelines below for designing a good layout for the SGM61061S.

- Place the input capacitor close to the device with the shortest possible connection traces.
- Share the same GND return point for the input and output capacitors and locate it as close as possible to the device GND pin to minimize the AC current loops. Place the inductor close to the switching node and connect it with a short trace to minimize the parasitic capacitances coupled to the SW node.
- Keep the signal traces like the FB, VOUT and RAMP sense line away from SW or other noisy sources.
- Use GND planes in middle layers for shielding and minimizing the ground potential drifts.



Top Layer Bottom Layer

Figure 7. Top Layer and Bottom Layer



Middle Layer 1 Middle Layer 2

Figure 8. Middle Layer 1 and Middle Layer 2

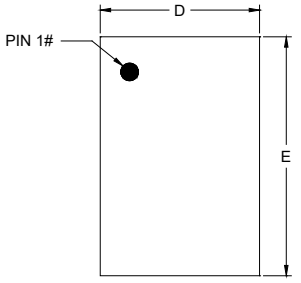
REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

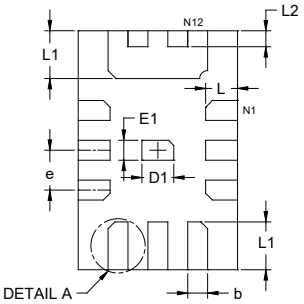
Changes from Original to REV.A (AUGUST 2025)	Page
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

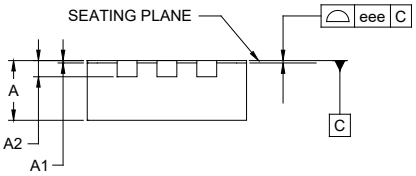
TQFN-2×3-12L



TOP VIEW

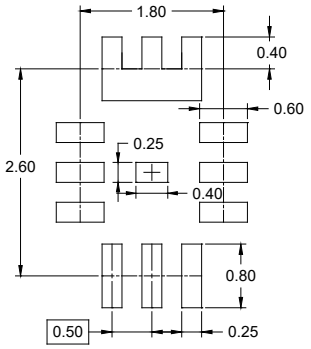


BOTTOM VIEW



SIDE VIEW

DETAIL A
ALTERNATE TERMINAL CONSTRUCTION



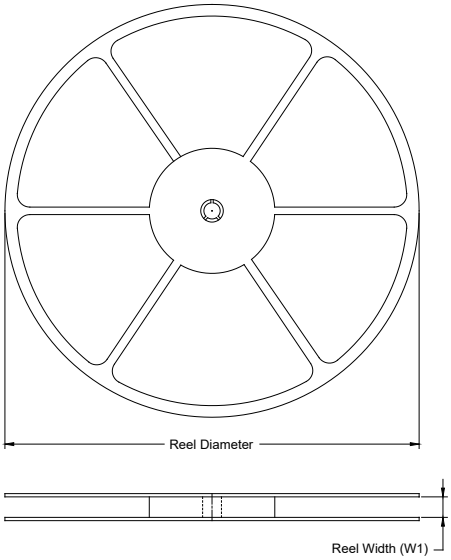
RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	0.700	-	0.800
A1	0.000	-	0.050
A2	0.203 REF		
b	0.200	-	0.300
D	1.900	-	2.100
E	2.900	-	3.100
D1	0.300	-	0.500
E1	0.150	-	0.350
e	0.500 BSC		
L	0.300	-	0.500
L1	0.500	-	0.700
L2	0.200 REF		
eee	0.080		

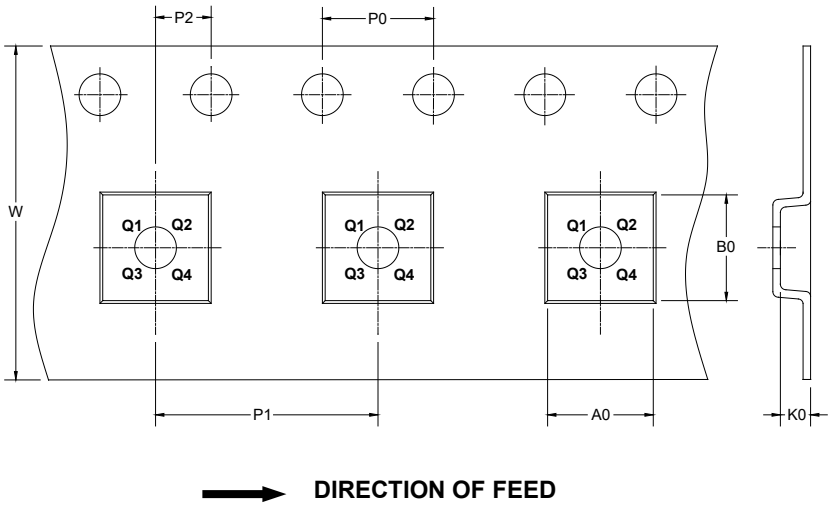
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



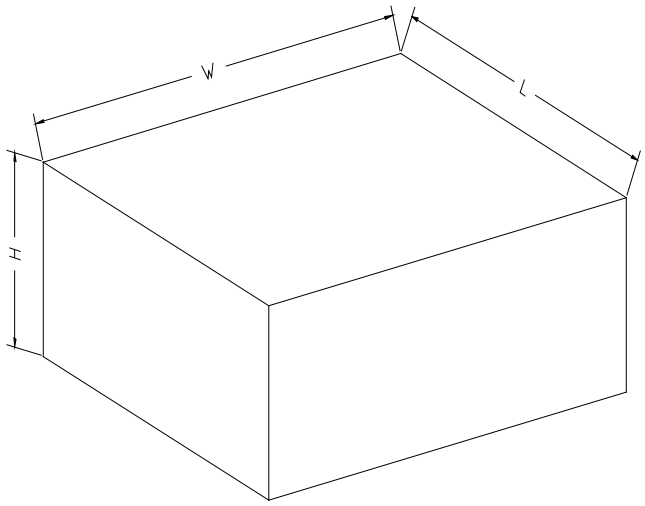
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TQFN-2×3-12L	13"	12.4	2.20	3.25	1.00	4.0	8.0	2.0	12.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002