SGM52421R8/SGM52421R8A
8-Channel, Low Noise, Low Power, 24-Bit, Sigma-Delta ADC with PGA and Reference

GENERAL DESCRIPTION

The SGM52421R8/SGM52421R8A are high-precision, low power, low noise integrated analog front end. They integrate a 24-bit Σ-Δ ADC, supporting 8 differential inputs or 15 single-ended/pseudo-differential inputs, plus an on-chip low-gain amplifier for small-signal acquisition.

The device features three power modes to balance power draw, output data rate, RMS noise, and alongside multiple configurable filters. At 25SPS single-cycle settling, it provides over 80dB rejection for 50Hz and 60Hz interference at low ODRs.

The built-in modules include a precision bandgap reference (compatible with the external differential references), programmable excitation and burnout current sources, and a bias voltage generator. A low-side power switch disables bridge sensors between conversions to reduce power consumption.

The integrated channel sequencer supports up to 16 channels including supply and reference monitoring, enabling interleaved conversion and diagnostics. Each channel can be independently configured for gain, filter, ODR, buffer and reference settings.

The rich diagnostic functions such as CRC and interface verification improve system reliability, while high integration reduces external components, board size, development time and cost. It achieves over 90% SFF (Safe Failure Fraction) complying with IEC 61508 per FMEDA evaluation.

The major difference between SGM52421R8 and SGM52421R8A is that the SGM52421R8A supports an nRST physical reset pin without the external clock input pin, whereas the SGM52421R8 supports the external clock input pin without the physical reset pin.

Power supply: analog 2.7V to 3.6V (or dual 1.8V rails), digital 1.8V to 3.6V. Packaged a Green TQFN-5×5-32IL package, operating temperature range: -40℃ to +125℃. Multi-function pins are marked with full names or primary functions in this datasheet.

FEATURES

- **Power Supply Range: 2.7V to 3.6V and ±1.8V**
- **Up to 22 Noise Free Bits in All Power Modes with Gain = 1**
- **Ultra-Low 1.5μV Offset Error for All Input Ranges in Full Power Mode**
- **0.0015% Gain Error for All Input Ranges**
- **Ultra-Low Differential Input Leakage up to 0.1nA**
- **Matched Excitation Currents with ±0.01% (TYP) Accuracy**
- **3 Power Modes Available**
- **Rail-to-Rail Analog Inputs Applicable for Gain > 1**
- **Provide 8 Differential/15 Pseudo-Differential Inputs**
- **Programmable Gain Allows Settings from 1 to 128**
- **Simultaneous 50Hz/60Hz Rejection at 25SPS (Single Cycle Settling)**
- **Crosspoint Multiplexed Analog Inputs**
- **On-Chip Bias Voltage Generator Available**
- **Low-side Power Switch Incorporated**
- **Multiple Filter Options Offered**
- **Internal Temperature Sensor for Enhanced Functionality**
- **Self and System Calibration Capabilities**
- **Sensor Burnout Detection Enabled**
- **Automatic Channel Sequencer Simplifying Operations**
- **Support Independent Interface Power Supply**
- **3-Wire or 4-Wire Serial Interface**
  - **Compatible with SPI, QSPI, MICROWIRE, and DSP**
  - **Equipped with Schmitt Trigger on SCLK**
- **8kV HBM ESD Support for Harsh Environment**
- **Operating Temperature Range: -40℃ to +125℃**
- **Available in a Green TQFN-5×5-32IL Package**

APPLICATIONS

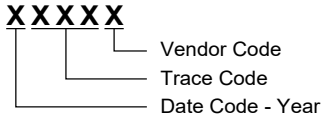
Industrial Process Control
Instrumentation
Temperature Measurement
Smart Transmitters
Pressure Measurement

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM52421R8	TQFN-5×5-32IL	-40℃ to +125℃	SGM52421R8XTVN32G/TR	SGM1XX XTVN32 XXXXX	Tape and Reel, 3000
			SGM52421R8XTVN32SG/TR	SGM1XX XTVN32 XXXXX	Tape and Reel, 500
SGM52421R8A	TQFN-5×5-32IL	-40℃ to +125℃	SGM52421R8AXTVN32G/TR	SGM2FE XTVN32 XXXXX	Tape and Reel, 3000
			SGM52421R8AXTVN32SG/TR	SGM2FE XTVN32 XXXXX	Tape and Reel, 500

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

AV_{DD} to AV_{SS} ..... -0.3V to 3.96V
IOV_{DD} to DGND ..... -0.3V to 3.96V
IOV_{DD} to AV_{SS} ..... -0.3V to 5.94V
AV_{SS} to DGND ..... -1.98V to 0.3V
Analog Input Voltage to AV_{SS} ..... -0.3V to AV_{DD} + 0.3V
Reference Input Voltage to AV_{SS} ..... -0.3V to AV_{DD} + 0.3V
Digital Input Voltage to DGND ..... -0.3V to IOV_{DD} + 0.3V
Digital Output Voltage to AGND ..... -0.3V to IOV_{DD} + 0.3V
AINx/Digital Input Current 10mA
Package Thermal Resistance
TQFN-5×5-32IL, θ_{JA} ..... 27.5℃/W
TQFN-5×5-32IL, θ_{JB} ..... 7.7℃/W
TQFN-5×5-32IL, $\theta_{JC\ (TOP)}$ ..... 22.3℃/W
TQFN-5×5-32IL, $\theta_{JC\ (BOT)}$ ..... 1.2℃/W
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility (1) (2)
HBM ..... ±8000V
CDM ..... ±1500V

NOTES:

1. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.

2. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

RECOMMENDED OPERATING CONDITIONS

Operating Temperature Range ..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

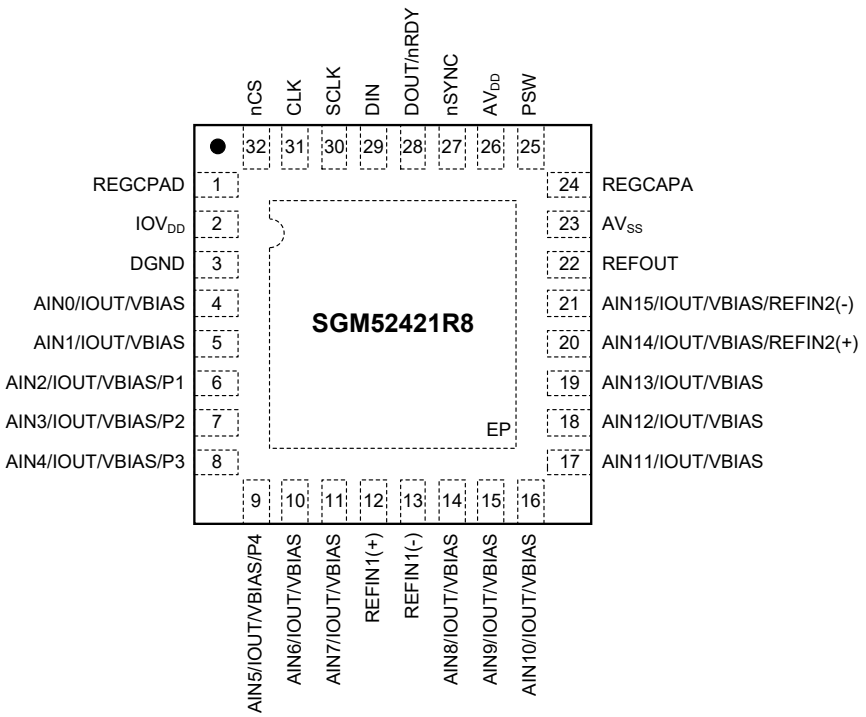
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

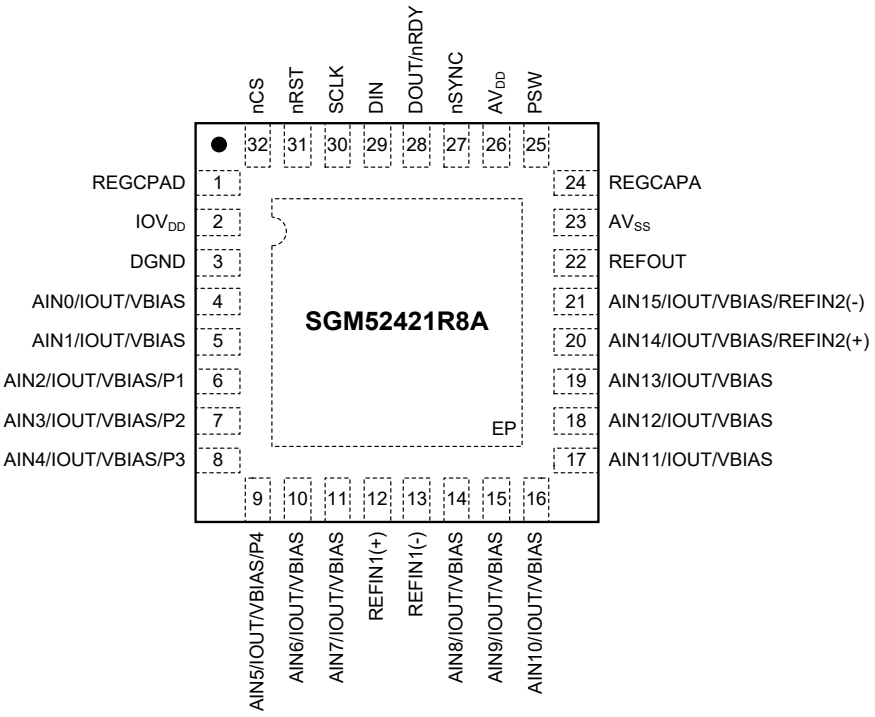
PIN CONFIGURATIONS

SGM52421R8 (TOP VIEW)



TQFN-5×5-32IL

SGM52421R8A (TOP VIEW)



TQFN-5×5-32IL

PIN DESCRIPTION

PIN	NAME	TYPE	FUNCTION
1	REGCAPD	DO	Digital LDO Regulator Output: It is recommended to connect this pin to DGND with a 1μF capacitor for decoupling.
2	IOV_{DD}	Digital	Digital Supply Voltage (IOV_{DD}): 1.8V to 3.6V. IOV_{DD} operates independently of AV_{DD}, so the serial interface can run at 1.8V while AV_{DD} stays at 3.6V.
3	DGND	Digital	Digital Ground.
4	AIN0/IOUT/VBIAS	AIO	Analog Input 0/Internal Excitation Current Source Output/Bias Voltage Pin. The pin is multifunctional. Programmable via registers as positive/negative terminal for differential/pseudo-differential input, access to internal programmable excitation current source, or routed IOUT1/IOUT0. It also generates a bias voltage midway between analog supply rails.
5	AIN1/IOUT/VBIAS	AIO	Analog Input 1/Internal Excitation Current Source Output/Bias Voltage Pin. The pin is multifunctional. Programmable via registers as positive/negative terminal for differential/pseudo-differential input, access to internal programmable excitation current source, or routed IOUT1/IOUT0. It also generates a bias voltage midway between analog supply rails.
6	AIN2/IOUT/VBIAS/P1	AIO	Multifunctional Pin (Analog Input 2/Internal Excitation I/O/Bias Voltage/GPO 1). Configurable via registers, it acts as ± terminal for differential/pseudo-differential input, accesses the programmable internal excitation current source, and routes IOUT0/IOUT1. It also generates mid-rail bias voltage and works as a GPO (referenced to AV_{SS}/AV_{DD}).
7	AIN3/IOUT/VBIAS/P2	AIO	Versatile Pin (Analog Input 3/Internal Excitation I/O/Bias Voltage/GPO 2). Register-configurable as ± terminal for differential/pseudo-differential input. It accesses the programmable internal excitation current source, routes IOUT0/IOUT1, generates mid-rail bias voltage, and acts as a GPO (referenced to AV_{SS}/AV_{DD}).
8	AIN4/IOUT/VBIAS/P3	AIO	Versatile Pin (Analog Input 4/Internal Excitation I/O/Bias Voltage/GPO 3). Register-configurable as ± terminal for differential/pseudo-differential input. It accesses the programmable internal excitation current source, routes IOUT0/IOUT1, generates mid-rail bias voltage, and serves as a GPO (referenced to AV_{SS}/AV_{DD}).
9	AIN5/IOUT/VBIAS/P4	AIO	Versatile Pin (Analog Input 5/Internal Excitation I/O/Bias Voltage/GPO 4). Register-configurable as ± terminal for differential/pseudo-differential input. It accesses the programmable internal excitation current source, routes IOUT0/IOUT1, generates mid-rail bias voltage, and acts as a GPO (referenced to AV_{SS}/AV_{DD}).
10	AIN6/IOUT/VBIAS	AIO	Multifunctional Pin (Analog Input 6/Internal Excitation I/O/Bias Voltage). Register-configurable as ± terminal for differential/pseudo-differential input. It accesses the programmable internal excitation current source, routes IOUT0/IOUT1, and generates mid-rail bias voltage.
11	AIN7/IOUT/VBIAS	AIO	Multifunctional Pin (Analog Input 7/Internal Excitation I/O/Bias Voltage). Register-configurable as ± terminal for differential/pseudo-differential input. It accesses the programmable internal excitation current source, routes IOUT0/IOUT1, and generates mid-rail bias voltage.
12	REFIN1(+)	AI	Positive Reference Input. Connect an external reference between REFIN1(+) and REFIN1(-). REFIN1(+) ranges from AV_{DD} to AV_{SS} + 0.5V. Nominal reference voltage (REFIN1(+) - REFIN1(-)) is 2.5V, but the device supports 0.5V to AV_{DD}.
13	REFIN1(-)	AI	Negative Reference Input Accommodates a Reference Input Ranging from AV_{SS} to AV_{DD} - 0.5V.
14	AIN8/IOUT/VBIAS	AIO	Analog Input 8/Internal Excitation Current Source Output/Bias Voltage: Versatile pin with multiple functions. Configurable via registers as ± terminal for differential/pseudo-differential input. Accesses internal programmable excitation current source (IOUT0/IOUT1 steerable here) and generates bias voltage midway between analog power rails.
15	AIN9/IOUT/VBIAS	AIO	Analog Input 9/Internal Excitation Current Source Output/Bias Voltage: Versatile pin with multiple functions. Configurable via registers as ± terminal for differential/pseudo-differential input. Accesses internal programmable excitation current source (IOUT0/IOUT1 steerable here) and generates bias voltage midway between analog power rails.
16	AIN10/IOUT/VBIAS	AIO	Analog Input 10/Internal Excitation Current Source Output/Bias Voltage: Versatile pin with multiple functions. Configurable via registers as ± terminal for differential/pseudo-differential input. Accesses internal programmable excitation current source (IOUT0/IOUT1 steerable here) and generates bias voltage midway between analog power rails.
17	AIN11/IOUT/VBIAS	AIO	Analog Input 11/Internal Excitation Current Source Output/Bias Voltage: Versatile pin with multiple functions. Configurable via registers as ± terminal for differential/pseudo-differential input. Accesses internal programmable excitation current source (IOUT0/IOUT1 steerable here) and generates bias voltage midway between analog power rails.

PIN DESCRIPTION (continued)

PIN	NAME	TYPE	FUNCTION
18	AIN12/IOUT/VBIAS	AIO	Analog Input 12/Internal Excitation Current Source Output/Bias Voltage: Versatile pin with multiple functions. Configurable via registers as ± terminal for differential/pseudo-differential input. Accesses internal programmable excitation current source (IOUT0/IOUT1 steerable here) and generates bias voltage midway between analog power rails.
19	AIN13/IOUT/VBIAS	AIO	Analog Input 13/Internal Excitation Current Source Output/Bias Voltage: Versatile pin with multiple functions. Configurable via registers as ± terminal for differential/pseudo-differential input. Accesses internal programmable excitation current source (IOUT0/IOUT1 steerable here) and generates bias voltage midway between analog power rails.
20	AIN14/IOUT/VBIAS/ REFIN2(+)	AIO	Analog Input 14/Internal Excitation Current Source Output/Bias Voltage/Positive Reference Input: Multifunctional pin. Register-configurable as ± terminal for differential/pseudo-differential input, accesses internal programmable excitation current source (IOUT0/IOUT1 routable here), and generates bias voltage midway between analog power rails. Also acts as REFIN2(+) input: ranges from AV_{DD} to AV_{SS} + 0.5V. Nominal REFIN2(±) voltage is 2.5V; device supports 0.5V to AV_{DD}.
21	AIN15/IOUT/VBIAS/ REFIN2(-)	AIO	Analog Input 15/Internal Excitation Current Source Output/Bias Voltage/Negative Reference Input: Versatile, multifunctional pin. Register-configurable as ± terminal for differential/pseudo-differential input, accesses internal programmable excitation current source (IOUT0/IOUT1 steerable here), and generates bias voltage midway between analog power rails. Also serves as REFIN2(-) (range: AV_{SS} to AV_{DD} - 0.5V) and internal 2.5V reference buffered output.
22	REFOUT	AO	Internal Reference Output Provides the Buffered Output of the Internal 2.5V Voltage Reference on This Pin.
23	AV_{SS}	Analog	Analog Supply Voltage (AV_{DD}, referenced to AV_{SS}): Regulates AV_{DD} voltage. AV_{DD} - AV_{SS} differential: 2.7V to 3.6V (mid/low power mode). 2.7V to 3.6V (full power mode). AV_{SS} can be < 0V for dual supplies (e.g., AV_{SS} = -1.8V, AV_{DD} = 1.8V provides ±1.8V to ADC).
24	REGCAPA	AO	Analog LDO Regulator Output Requires Decoupling to AV_{SS} Using a 1μF Capacitor.
25	PSW	AI	Low-side Power Switch Connects to AV_{SS}.
26	AV_{DD}	Analog	Analog Supply Voltage.
27	nSYNC	DI	Synchronization Input (nSYNC): Logic input for synchronizing the digital filters and analog modulators in multi-SGM52421R8/SGM52421R8A setups. Low nSYNC resets digital filter nodes, filter/calibration control logic, holds analog modulator in reset, and sets nRDY high (if low). Doesn't affect the digital interface. An external pull-up resistor is required for this nSYNC pin as it is floating internally.
28	DOUT/nRDY	DO	Serial Data Output/Data Ready Output (DOUT/nRDY): Dual-function pin. Acts as serial data output for ADC's output shift register (accesses on-chip data/control registers). Serves as data ready indicator: goes low when conversion completes, returns high if unread before next update. Falling edge can trigger processor interrupt for valid data. With external serial clock, outputs data/control words on the falling SCLK (valid on the rising SCLK) when nCS is low.
29	DIN	DI	Serial Data Input: Feeds ADC's input shift register, transferring data to internal control registers. Register selection bits in the communications register specify the target register.
30	SCLK	DI	Serial Clock Input (SCLK): Interface for ADC data transfers. Schmitt-triggered input enables opto-isolated compatibility. Operates as continuous clock (continuous pulse train) or non-continuous clock (smaller data batches).
31	CLK	DIO	Clock Input/Output Pin. Supports internal or external clock for ADC operation. Enables internal clock output when active; accepts external clock when internal is disabled. Allows multi-ADC synchronization to a common clock for simultaneous conversions. (SGM52421R8 Only)
	nRST	DI	Reset Pin. (SGM52421R8A Only)
32	nCS	DI	Chip Select Input (nCS): Active-low logic input for ADC selection. Used to select the ADC in multi-device serial bus systems or for frame synchronization. If SPI diagnostics are unused, hardwire low to enable 3-wire mode (interfaced via SCLK, DIN, and DOUT).
Exposed Pad	EP	—	Exposed Pad. Connect to AV_{SS}.

NOTE: AI = analog input, AO = analog output, AIO = analog input and output, DI = digital input, DO = digital output, DIO = digital input and output.

ELECTRICAL CHARACTERISTICS

(T_A = -40℃ to +125℃, full power mode AV_{DD} = 2.7V to 3.6V, mid and low power mode AV_{DD} = 2.7V to 3.6V, IOV_{DD} = 1.8V to 3.6V, AV_{SS} = DGND = 0V, REFINx(+) = 2.5V, REFINx(-) = AV_{SS}, master clock = 614.4kHz, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
ADC							
Output Data Rate	f_{ADC}	Low power mode		1.17		2400	SPS
		Mid power mode		2.34		4800	
		Full power mode		9.38		19200	
No Missing Codes (1)		FS (2) > 2, $sinc^4$ filter		24			Bits
		FS (2) > 8, $sinc^3$ filter		24			
Resolution				See the RMS Noise and Resolution section			
RMS Noise and Update Rates				See the RMS Noise and Resolution section			
Integral Nonlinearity	INL	Gain = 1 to 128 (1) (3)		-15	±2 (13)	15	ppm of FSR
Offset Error (4)	E_O	Before calibration	Gain = 1 to 8		±1.5		μV
			Gain = 16 to 128		±1.5		
		After internal calibration/system calibration			In order of noise		
Offset Error Drift vs. Temperature (5)		Full power mode	Gain = 1 or Gain > 32		15		nV/℃
			Gain = 2 to 8		20		
			Gain = 16		42		
			Gain = 32		21		
Gain Error (4) (6)	E_G	Before internal calibration	Gain = 1, T_A = +25℃	-0.0025		0.0025	%
			Gain > 1		±0.0015		
		After system calibration			In order of noise		
Gain Error Drift vs. Temperature					1	2	ppm/℃
Power Supply Rejection (A_{INP} = A_{INN} = 0.9V, External Reference)		Low power mode		86			dB
		Mid power mode (1)		87			
		Full power mode	AV_{DD} at DC	90			
			IOV_{DD} at DC		126		
Common Mode Rejection (7)		At DC (1)	Gain = 1	96	120		dB
		At DC	Gain 2 or 4	100	130		
			Gain ≥ 8	100	140		
		$Sinc^3$, $sinc^4$ filters (1)	10SPS, 50Hz ± 1Hz, 60Hz ± 1Hz		125		
			50SPS, 50Hz ± 1Hz		125		
			60SPS, 60Hz ± 1Hz		125		
		Fast settling filters (1)	First notch at 50Hz, 50Hz ± 1Hz		120		
			First notch at 60Hz, 60Hz ± 1Hz		120		
		Post filters (1)	20SPS, 50Hz ± 1Hz, 60Hz ± 1Hz		135		
			25SPS, 50Hz ± 1Hz, 60Hz ± 1Hz		135		

ELECTRICAL CHARACTERISTICS (continued)

(T_A = -40℃ to +125℃, full power mode AV_{DD} = 2.7V to 3.6V, mid and low power mode AV_{DD} = 2.7V to 3.6V, IOV_{DD} = 1.8V to 3.6V, AV_{SS} = DGND = 0V, REFINx(+) = 2.5V, REFINx(-) = AV_{SS}, master clock = 614.4kHz, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Normal Mode Rejection (1)		Sinc^4 filter, external clock	10SPS, 50Hz ± 1Hz, 60Hz ± 1Hz		125		dB
			50SPS, REJ60 (9) = 1, 50Hz ± 1Hz, 60Hz ± 1Hz		85		
			50SPS, 50Hz ± 1Hz		122		
			60SPS, 60Hz ± 1Hz		123		
		Sinc^4 filter, internal clock	10SPS, 50Hz ± 1Hz, 60Hz ± 1Hz		110		
			50SPS, REJ60 (9) = 1, 50Hz ± 1Hz, 60Hz ± 1Hz		75		
			50SPS, 50Hz ± 1Hz		100		
			60SPS, 60Hz ± 1Hz		100		
		Sinc^3 filter, external clock	10SPS, 50Hz ± 1Hz, 60Hz ± 1Hz		100		
			50SPS, REJ60 (9) = 1, 50Hz ± 1Hz, 60Hz ± 1Hz		69		
			50SPS, 50Hz ± 1Hz		100		
			60SPS, 60Hz ± 1Hz		105		
		Sinc^3 filter, internal clock	10SPS, 50Hz ± 1Hz, 60Hz ± 1Hz		80		
			50SPS, REJ60 (9) = 1, 50Hz ± 1Hz, 60Hz ± 1Hz		60		
			50SPS, 50Hz ± 1Hz		75		
			60SPS, 60Hz ± 1Hz		75		
		Fast settling filters, external clock	First notch at 50Hz, 50Hz ± 0.5Hz		40		
			First notch at 60Hz, 60Hz ± 0.5Hz		40		
		Fast settling filters, internal clock	First notch at 50Hz, 50Hz ± 0.5Hz		30		
			First notch at 60Hz, 60Hz ± 0.5Hz		30		
		Post filters, external clock	20SPS, 50Hz ± 1Hz, 60Hz ± 1Hz		86		
			25SPS, 50Hz ± 1Hz, 60Hz ± 1Hz		62		
		Post filters, internal clock	20SPS, 50Hz ± 1Hz, 60Hz ± 1Hz		75		
			25SPS, 50Hz ± 1Hz, 60Hz ± 1Hz		60		
Analog Inputs (10)							
Differential Input Voltage Ranges (11)		V_{REF} = REFINx(+) - REFINx(-), or internal reference			±V_{REF}/gain		V
Absolute A_{IN} Voltage Limits (1)		Gain = 1 (unbuffered)		AV_{SS} - 0.05		AV_{DD} + 0.05	V
		Gain = 1 (buffered)		AV_{SS} + 0.1		AV_{DD} - 0.1	
		Gain > 1		AV_{SS} - 0.05		AV_{DD} + 0.05	
Absolute Input Current		Buffered	Low power mode		±1		nA
			Mid power mode		±1.2		
			Full power mode		±3.3		
		Gain = 1 (unbuffered), current varies with input voltage			±4		µA/V

ELECTRICAL CHARACTERISTICS (continued)

(T_A = -40℃ to +125℃, full power mode AV_{DD} = 2.7V to 3.6V, mid and low power mode AV_{DD} = 2.7V to 3.6V, IOV_{DD} = 1.8V to 3.6V, AV_{SS} = DGND = 0V, REFINx(+) = 2.5V, REFINx(-) = AV_{SS}, master clock = 614.4kHz, unless otherwise noted.)

PARAMETER		SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Analog Inputs (10)								
Differential Input Current			Buffered	Low power mode		±0.1		nA
				Mid power mode		±0.2		
				Full power mode		±0.6		
Analog Input Current Drift			Buffered	Low power mode		15		pA/℃
				Mid power mode		15		
				Full power mode		20		
			Gain = 1 (unbuffered), current varies with input voltage			±1.1		nA/V/℃
Reference Input								
Internal Reference	Initial Accuracy		T_A = +25℃		2.5 - 0.05%	2.5	2.5 + 0.05%	V
	Drift		T_A = +25℃ to +125℃			6	15	ppm/℃
	Output Current						10	mA
	Load Regulation					185		μV/mA
	Power Supply Rejection					96		dB
External Reference	External REFIN Voltage (1)		REFIN = REFINx(+) - REFINx(-)		0.5	2.5	AV_{DD}	V
	Absolute REFIN Voltage Limits (1)		Unbuffered		AV_{SS} - 0.05		AV_{DD} + 0.05	V
			Buffered		AV_{SS} + 0.1		AV_{DD} - 0.1	
	Absolute Input Current		Buffered	Low power mode		±0.3		nA
				Mid power mode		±0.6		
				Full power mode		±1.8		
			Unbuffered			±10		μA
	Reference Input Current Drift		Buffered (8)	Low power mode		10		pA/℃
				Mid power mode		10		
				Full power mode		10		
			Unbuffered			2		nA/℃
	Normal Mode Rejection					Same as for analog inputs		dB
	Common Mode Rejection					100		
Excitation Current Sources (IOUT0/IOUT1) Available on Any Analog Input Pin								
Output Current						50/100/ 250/500/ 750/1000/ 1500		μA
Initial Tolerance			T_A = +25℃, 50μA to 1.5mA			±0.018		%
Drift						20	50	ppm/℃
Current Matching			Matching between IOUT0 and IOUT1, V_{OUT} = 0V, 50μA to 1.5mA			±0.01		%
Drift Matching (1)			250μA current source			3	10	ppm/℃
			100μA/500μA/750μA/1000μA/1500μA current sources			7	25	
Line Regulation (AV_{DD})						±0.02		%/V
Load Regulation						±0.02		%/V
Output Compliance (1)			100μA/250μA/500μA/750μA/1000μA/ 1500μA current sources, 2% accuracy		AV_{SS} - 0.05		AV_{DD} - 0.8	V

ELECTRICAL CHARACTERISTICS (continued)

(T_A = -40℃ to +125℃, full power mode AV_{DD} = 2.7V to 3.6V, mid and low power mode AV_{DD} = 2.7V to 3.6V, IOV_{DD} = 1.8V to 3.6V, AV_{SS} = DGND = 0V, REFINx(+) = 2.5V, REFINx(-) = AV_{SS}, master clock = 614.4kHz, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Bias Voltage (V_{BIAS}) Generator Available on Any Analog Input Pin						
Bias Voltage	V_{BIAS}			AV_{SS} + (AV_{DD} - AV_{SS})/2		V
V_{BIAS} Generator Start-Up Time		Dependent on the capacitance connected to AINx		1.43		μs/nF
Temperature Sensor						
Accuracy				0.5		℃
Sensitivity				6405		Codes/℃
Low-Side Power Switch						
On-Resistance	R_{ON}			4	10	Ω
Allowable Current (1)		Continuous current			30	mA
Burnout Currents						
A_{IN} Current		Analog inputs must be buffered		0.5/2/4		μA
Digital Outputs (P1 to P4)						
High-Level Output Voltage	V_{OH}	I_{SOURCE} = 100μA	AV_{DD} - 0.35			V
Low-Level Output Voltage	V_{OL}	I_{SINK} = 100μA			0.4	V
Diagnostics						
Power Supply Monitor Detect Level		Analog low dropout regulator (ALDO), AV_{DD} - AV_{SS} ≥ 2.7V		1.6		V
		Digital LDO (DLDO), IOV_{DD} ≥ 1.8V		1.4		
Reference Detect Level		REF_DET_ERR bit active if V_{REF} < 0.45V	0.45		1	V
AINM/AINP Over-Voltage Detect Level			AV_{DD} + 0.1			V
AINM/AINP Under-Voltage Detect Level					AV_{SS} - 0.25	V
Internal/External Clock						
Internal Clock Frequency			614.4 - 1.2%	614.4	614.4 + 1.2%	kHz
Internal Clock Duty Cycle				50:50		%
External Clock Frequency		Internal divide by 4		2.4576		MHz
External Clock Duty Cycle Range				45:55 to 55:45		%
Logic Inputs (1)						
Low-Level Input Voltage	V_{INL}				0.3 × IOV_{DD}	V
High-Level Input Voltage	V_{INH}		0.75 × IOV_{DD}			V
Hysteresis				0.3		V
Input Currents		V_{IN} = IOV_{DD} or GND	-1		1	μA
Input Capacitance		All digital inputs		10		pF
Logic Outputs (Including CLK)						
High-Level Output Voltage (1)	V_{OH}	I_{SOURCE} = 100μA	IOV_{DD} - 0.35			V
Low-Level Output Voltage (1)	V_{OL}	I_{SINK} = 100μA			0.4	V
Floating State Output Capacitance				10		pF
Data Output Coding				Offset Binary		

ELECTRICAL CHARACTERISTICS (continued)

(T_A = -40℃ to +125℃, full power mode AV_{DD} = 2.7V to 3.6V, mid and low power mode AV_{DD} = 2.7V to 3.6V, IOV_{DD} = 1.8V to 3.6V, AV_{SS} = DGND = 0V, REFINx(+) = 2.5V, REFINx(-) = AV_{SS}, master clock = 614.4kHz, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
System Calibration (1)							
Calibration Limit		Full-scale				1.05 × FS	V
		Zero-scale		-1.05 × FS			
Input Span				0.8 × FS		2.1 × FS	V
Power Supply Voltages for All Power Modes							
AV_{DD} to AV_{SS}		Low power mode		2.7		3.6	V
		Mid power mode		2.7		3.6	
		Full power mode		2.7		3.6	
IOV_{DD} to GND				1.8		3.6	V
AV_{SS} to GND				-1.8		0	V
IOV_{DD} to AV_{SS}						5.4	V
Power Supply Currents (10) (12)							
Power Supply Current (External Reference)	I_{AVDD}	Low power mode	Gain = 1 (1), all buffers off		240	300	μA
			Gain = 1, I_{AVDD} increase per AINx buffer (1) (14)		25	50	
			Gain = 2 to 8		350	500	
			Gain = 16 to 128		400	600	
			I_{AVDD} increase per reference buffer (1) (14), all gains		25	50	
		Mid power mode	Gain = 1 (1), all buffers off		280	400	μA
			Gain = 1, I_{AVDD} increase per AINx buffer (1) (14)		50	90	
			Gain = 2 to 8		490	700	
			Gain = 16 to 128		580	900	
			I_{AVDD} increase per reference buffer (1) (14), all gains		60	90	
		Full power mode	Gain = 1 (1), all buffers off		560	700	μA
			Gain = 1, I_{AVDD} increase per AINx buffer (1) (14)		135	300	
			Gain = 2 to 8		1140	1600	
			Gain = 16 to 128		1485	2200	
			I_{AVDD} increase per reference buffer (1) (14), all gains		135	300	
		I_{AVDD} increase	Due to internal reference (1), independent of power mode, the reference buffers are not required when using this reference		60	100	μA
			Due to V_{BIAS} (1), independent of power mode		24		
			Due to diagnostics (1)		8		
	I_{IOVDD}	Low power mode			35		μA
		Mid power mode			50		
		Full power mode			140		

ELECTRICAL CHARACTERISTICS (continued)

(T_A = -40℃ to +125℃, full power mode AV_{DD} = 2.7V to 3.6V, mid and low power mode AV_{DD} = 2.7V to 3.6V, IOV_{DD} = 1.8V to 3.6V, AV_{SS} = DGND = 0V, REFINx(+) = 2.5V, REFINx(-) = AV_{SS}, master clock = 614.4kHz, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Power-Down Currents (12) (Independent of Power Mode)						
Standby Current	I_{AVDD}	LDOs on only		25	50	μA
	I_{IOVDD}			15		
Power-Down Current	I_{AVDD}			0.5	3	μA
	I_{IOVDD}			0.5	3	

NOTES:

1. Although not production tested, these specifications are backed by characterization data during the initial product release.

2. FS represents the decimal equivalent of the FS[10:0] bits in the filter registers.

3. Nonlinearity is production tested solely in full power mode. For other power modes, this specification is supported by characterization data during the initial product release.

4. Post-system or internal zero-scale calibration, offset error aligns with the noise level for the programmed gain and selected output data rate. A system full-scale calibration diminishes gain error to the noise level for the programmed gain and output data rate.

5. Recalibration at any temperature eliminates these errors.

6. Gain error pertains to both positive and negative full-scale. Factory calibration for all gains, T_A = +25℃.

7. For gain > 1, the common mode voltage ranges between AV_{SS} and AV_{DD}.

8. These parameters are calculated at T_A = -40℃ to +85℃.

9. The REJ60 is a bit within the filter registers. Setting REJ60 bit to 1 place a notch at 60Hz when the first notch of the sinc filter is at 50Hz, thereby enabling simultaneous rejection of both 50Hz and 60Hz frequencies.

10. When gain exceeds 1, the analog input buffers activate automatically. Disabling the buffers is only feasible when gain equals 1.

11. With V_{REF} = (AV_{DD} - AV_{SS}), the typical differential input is V_{REF}/gain for low and mid power modes, and V_{REF}/gain for full power mode when gain > 1.

12. Digital inputs equate to either IOV_{DD} or DGND with excitation currents and bias voltage generator disabled.

13. The typical integral nonlinearity (INL) is tested under the condition where absolute AIN voltage is less than (AV_{DD} - 0.7V).

14. This current is tested under the conditions of AINx buffer enabled and REFx buffer enabled.

TIMING SPECIFICATIONS

(Full power mode AV_{DD} = 2.7V to 3.6V, mid and low power mode AV_{DD} = 2.7V to 3.6V, IOV_{DD} = 1.8V to 3.6V, AV_{SS} = DGND = 0V, input logic 0 = 0V, input logic 1 = IOV_{DD}, unless otherwise noted.)

PARAMETER [1] [2]	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCLK High Pulse Width	t_3		100			ns
SCLK Low Pulse Width	t_4		100			ns
Delay between Consecutive Read/Write Operations	t_{12}	Full power mode	3/MCLK [3]			ns
		Mid power mode	12/MCLK			
		Low power mode	24/MCLK			
DOUT/nRDY High Time if DOUT/nRDY is Low and the Next Conversion is Available	t_{13}	Full power mode		6		μs
		Mid power mode		25		
		Low power mode		50		
nSYNC Low Pulse Width	t_{14}	Full power mode	3/MCLK			ns
		Mid power mode	12/MCLK			
		Low power mode	24/MCLK			
Read Operation						
nCS Falling Edge to DOUT/nRDY Active Time	t_1		0		80	ns
SCLK Active Edge to Data Valid Delay [5]	t_2 [4]		0		80	ns
Bus Relinquish Time after nCS Inactive Edge	t_5 [6] [7]		10		80	ns
SCLK Inactive Edge to nCS Inactive Edge	t_6		0			ns
SCLK Inactive Edge to DOUT/nRDY High	t_7 [8]	The DOUT_nRDY_DEL bit is cleared, the nCS_EN bit is cleared	10			ns
		The DOUT_nRDY_DEL bit is set, the nCS_EN bit is cleared	110			
Data Valid after nCS Inactive Edge	t_{7A} [7]	The nCS_EN bit is set	t_5			ns
Write Operation						
nCS Falling Edge to SCLK Active Edge Setup Time [5]	t_8		0			ns
Data Valid to SCLK Edge Setup Time	t_9		30			ns
Data Valid to SCLK Edge Hold Time	t_{10}		25			ns
nCS Rising Edge to SCLK Edge Hold Time	t_{11}		0			ns

NOTES:

1. These specifications underwent sample testing during the initial release to ensure compliance. All input signals are defined with t_R = t_F = 5ns (10% to 90% of IOV_{DD} and timed from a voltage level of IOV_{DD}/2).

2. Refer to timing diagrams.

3. MCLK denotes the master clock frequency.

4. These specifications are determined with the load circuit and defined as the time required for the output to cross the V_{OL} or V_{OH} limits.

5. The SCLK active edge corresponds to the falling edge of SCLK.

6. These specifications are derived from the measured time taken by the data output to change by 0.5V when loaded with the circuit. The measured value is then extrapolated back to remove the effects of charging or discharging the 25pF capacitor. The times provided in the timing characteristics represent the true bus relinquish times of the device and are therefore independent of external bus loading capacitances.

7. nRDY returns high after reading the ADC. In single conversion mode and continuous conversion mode, the same data can be read again, if necessary, while nRDY is high, although subsequent reads must not occur close to the next output update. In continuous read mode, the digital word can be read only once.

8. When the nCS_EN bit is cleared, the DOUT/nRDY pin transitions from its DOUT function to its nRDY function following the last inactive edge of the SCLK. When nCS_EN is set, the DOUT pin continues to output the LSB of the data until the nCS inactive edge.

TIMING DIAGRAMS

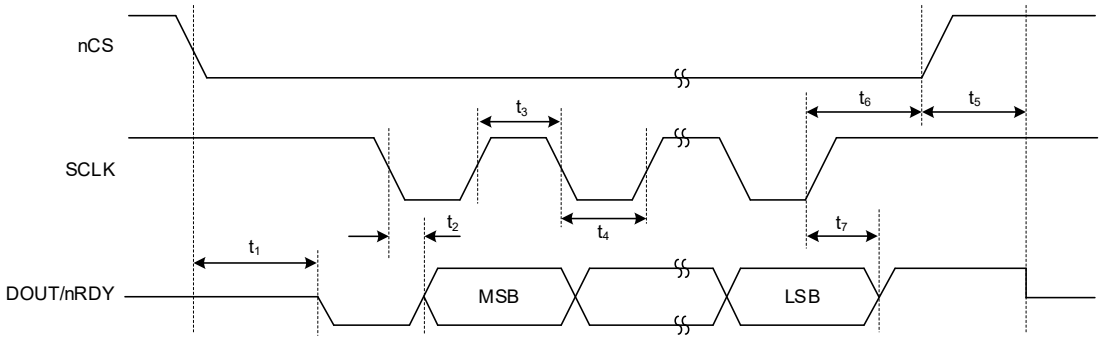


Figure 1. Read Cycle Timing Diagram (nCS_EN Bit Cleared)

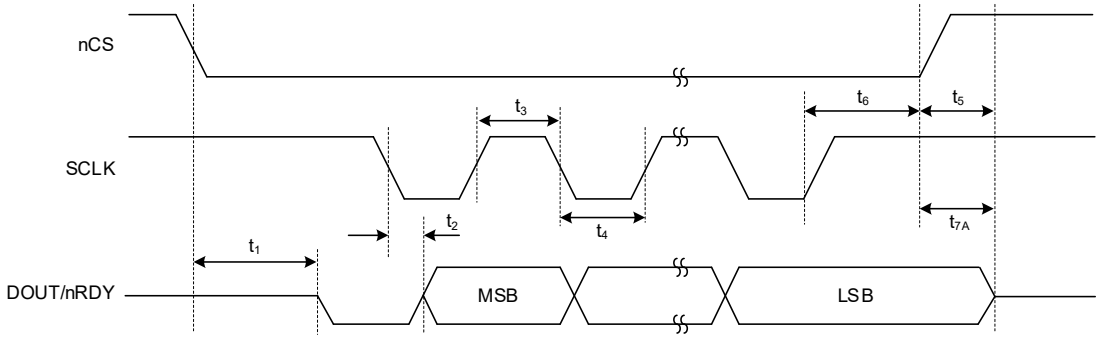


Figure 2. Read Cycle Timing Diagram (nCS_EN Bit Set)

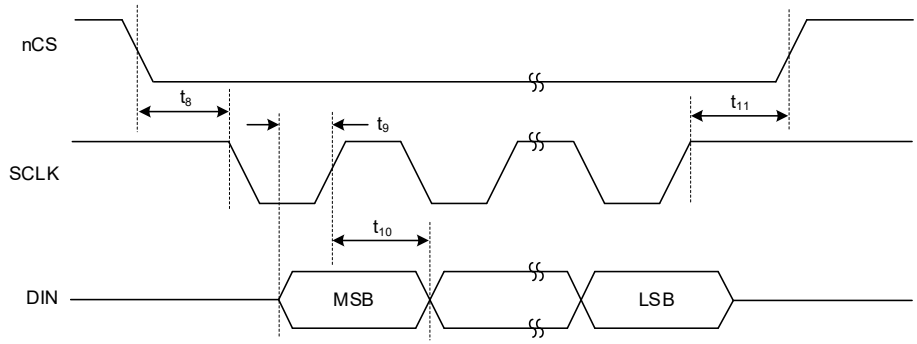


Figure 3. Write Cycle Timing Diagram

TIMING DIAGRAMS (continued)

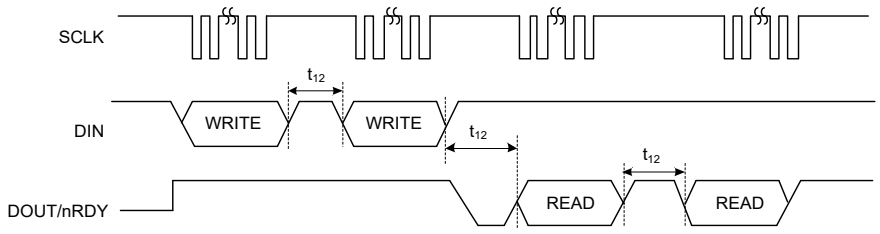


Figure 4. Delay between Consecutive Serial Operations

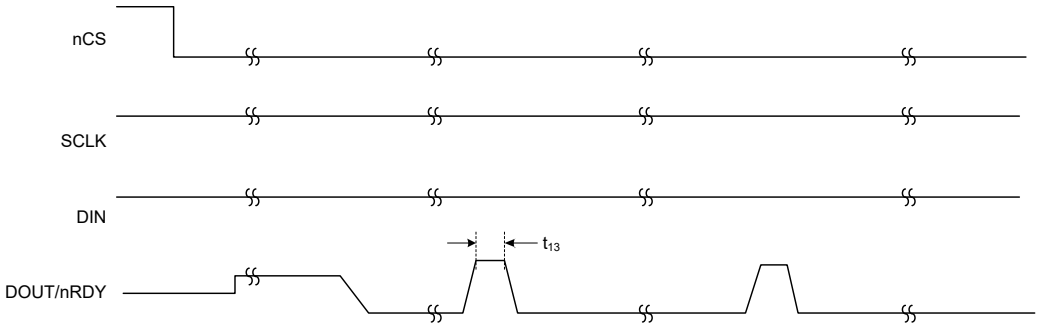


Figure 5. DOUT/nRDY High Time when DOUT/nRDY is Initially Low and the Next Conversion is Available

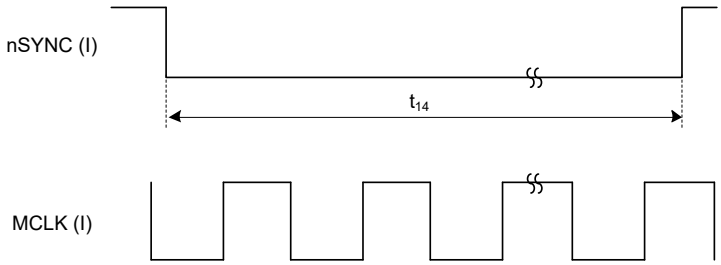
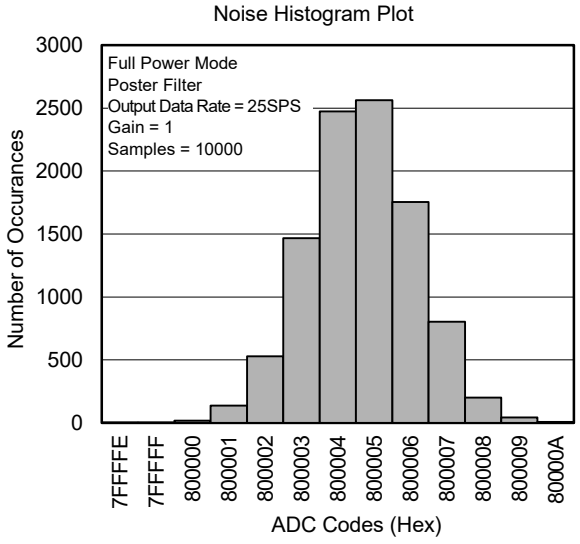
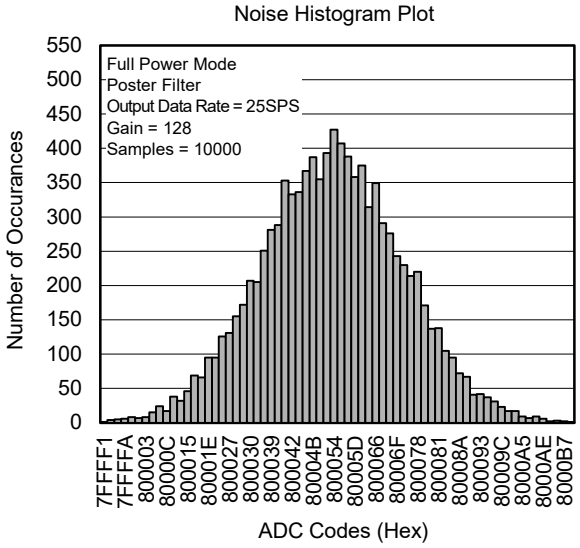
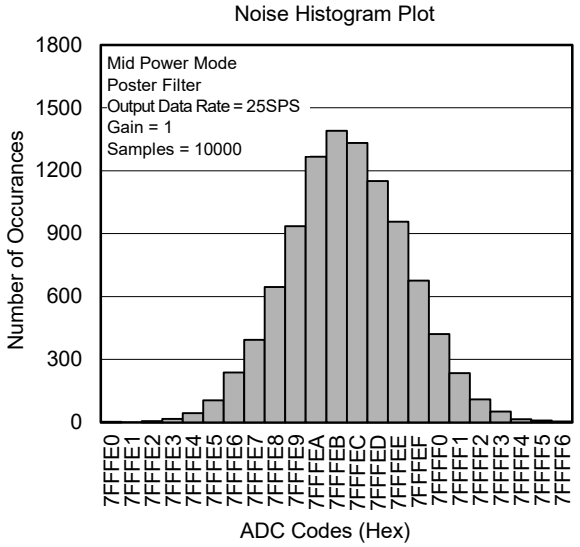


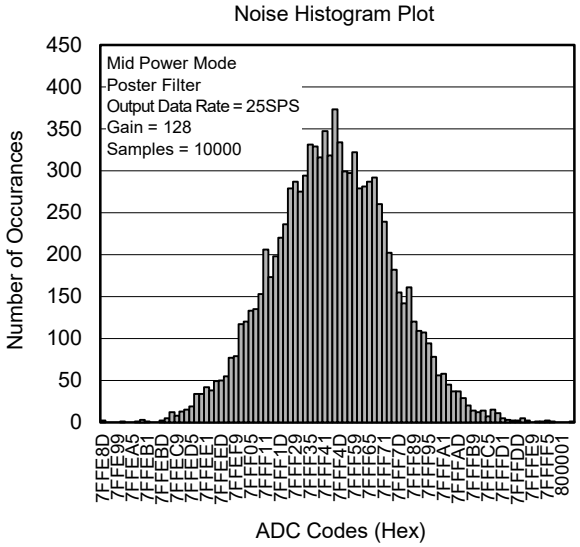
Figure 6. nSYNC Pulse Width

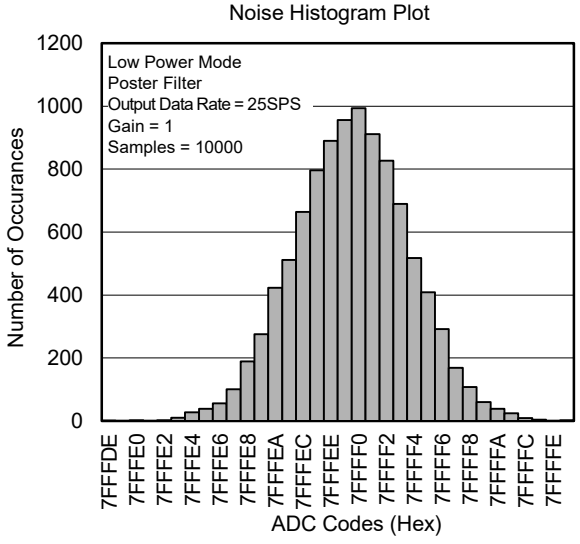
TYPICAL PERFORMANCE CHARACTERISTICS

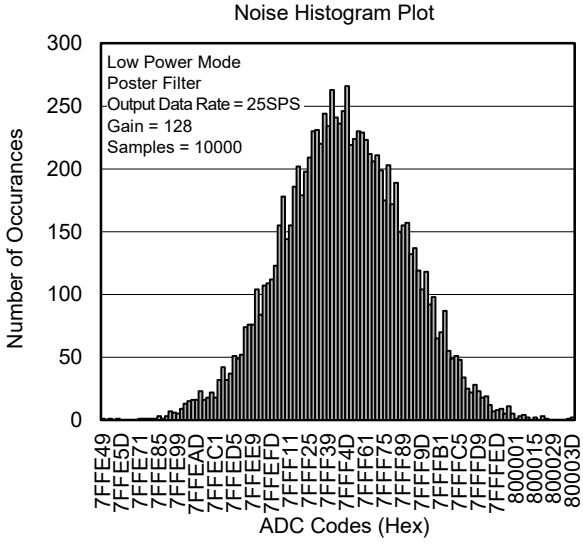






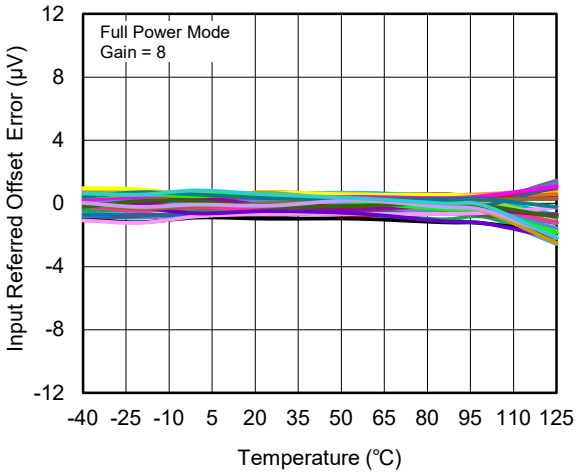




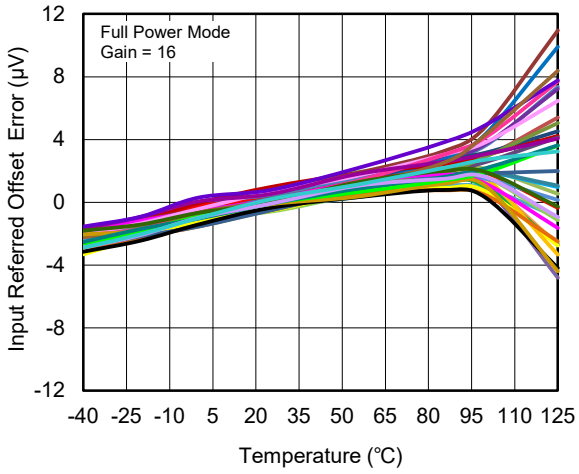


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

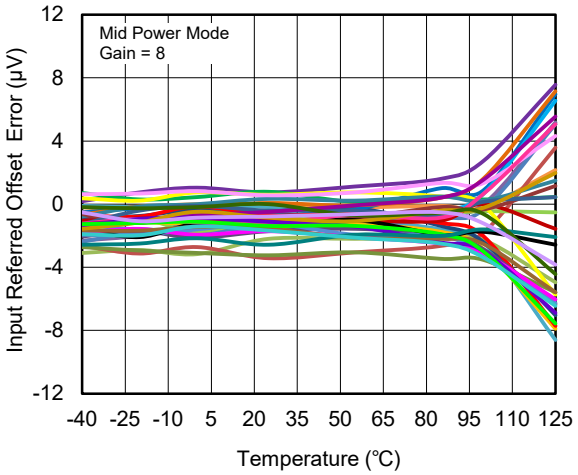
Input Referred Offset Error vs. Temperature



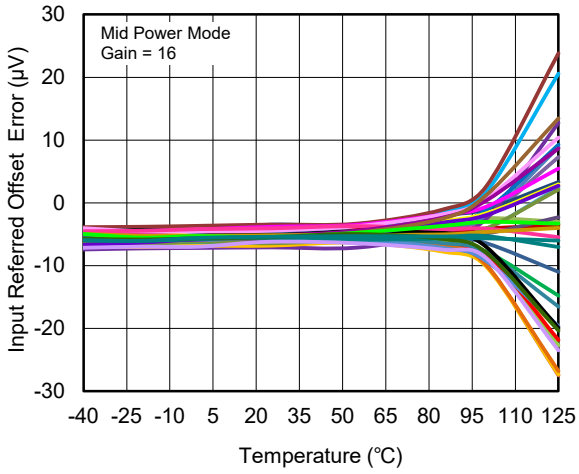
Input Referred Offset Error vs. Temperature



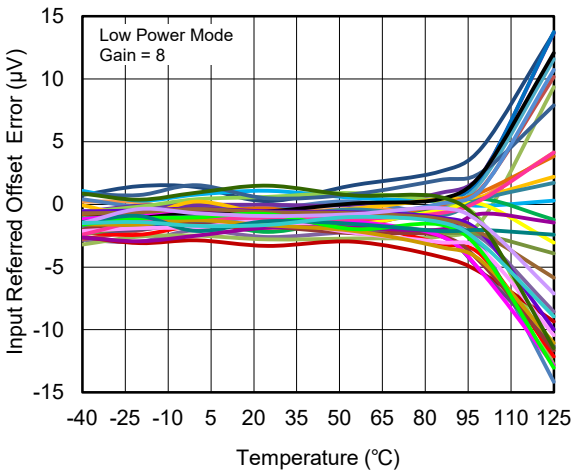
Input Referred Offset Error vs. Temperature



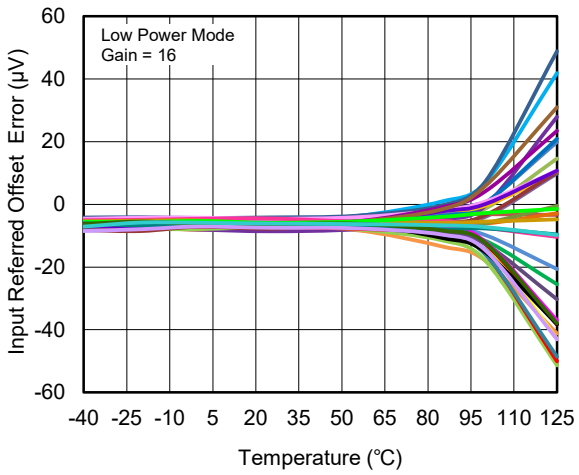
Input Referred Offset Error vs. Temperature



Input Referred Offset Error vs. Temperature

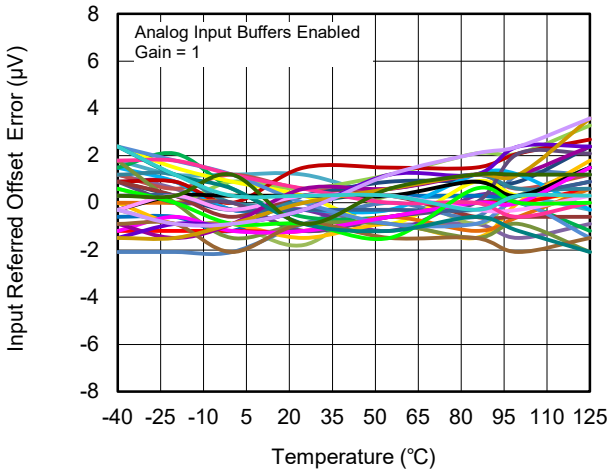


Input Referred Offset Error vs. Temperature

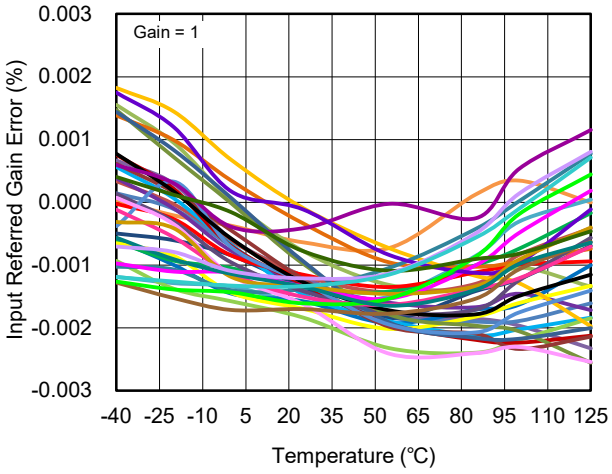


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

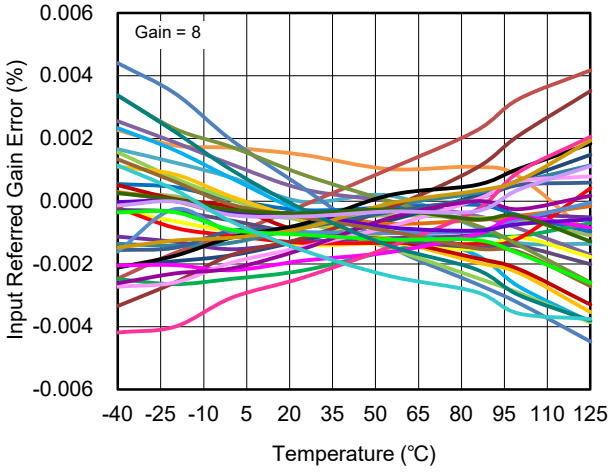
Input Referred Offset Error vs. Temperature



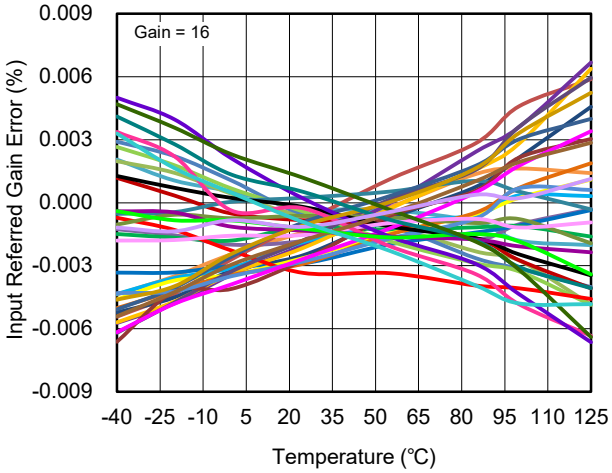
Input Referred Gain Error vs. Temperature



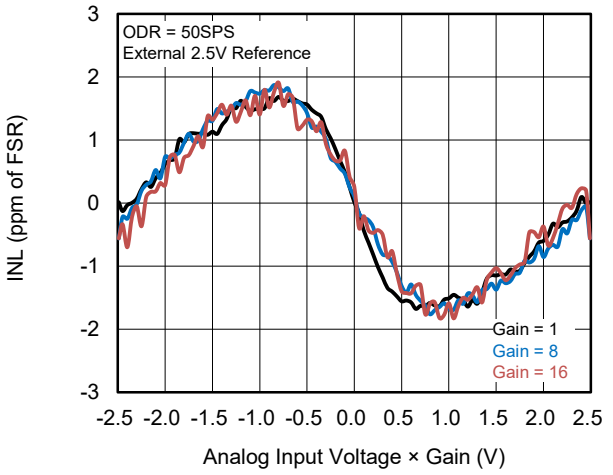
Input Referred Gain Error vs. Temperature



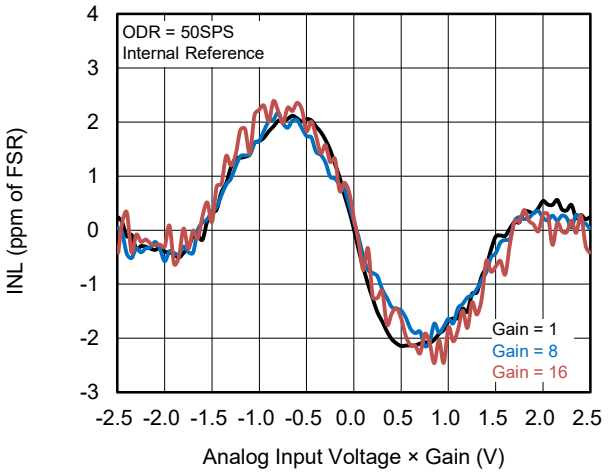
Input Referred Gain Error vs. Temperature



INL vs. Differential Input Signal (Analog Input × Gain)

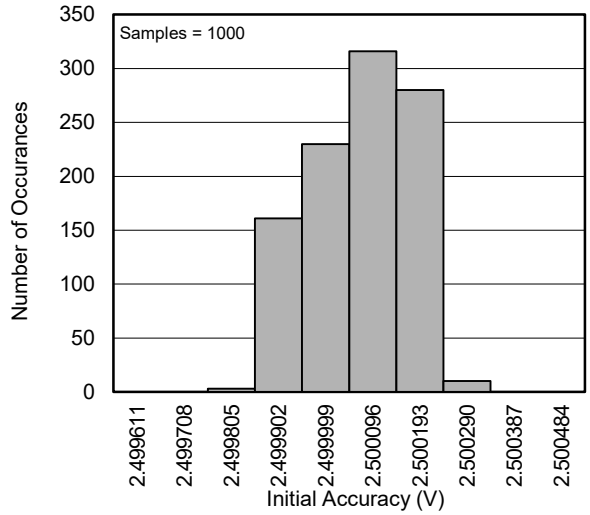


INL vs. Differential Input Signal (Analog Input × Gain)

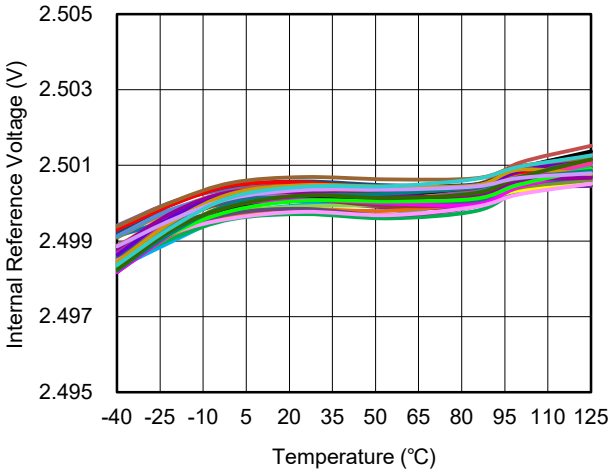


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

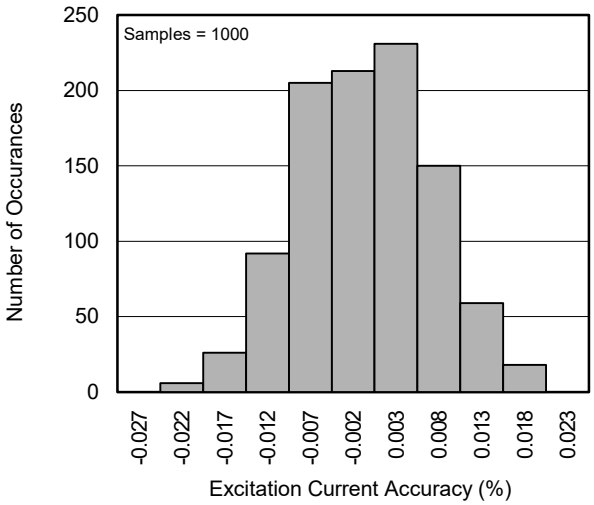
Internal Reference Voltage Histogram



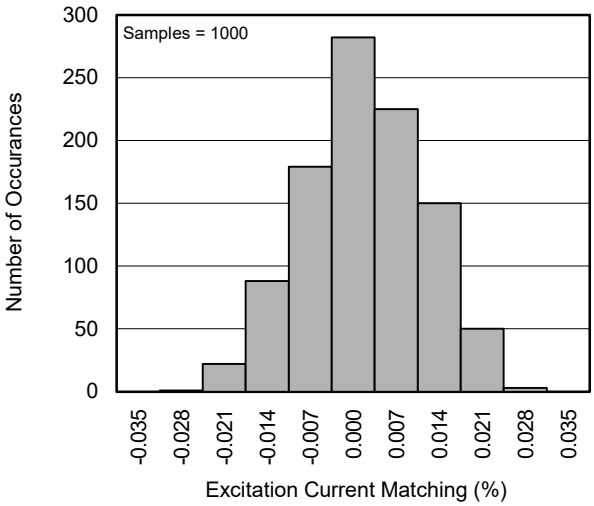
Internal Reference Voltage vs. Temperature



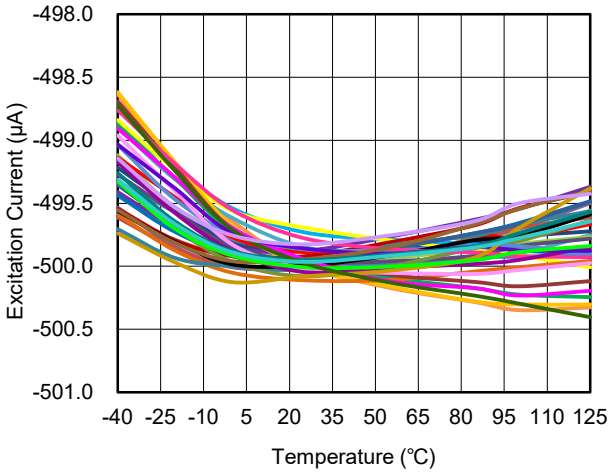
IOUTx Current Initial Accuracy Histogram (500μA)



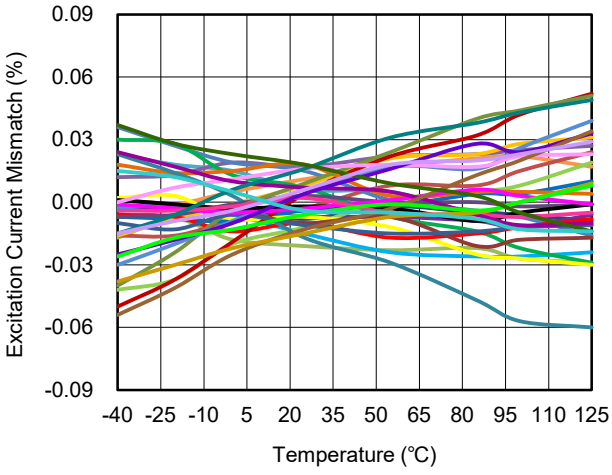
IOUTx Current Initial Matching Histogram (500μA)



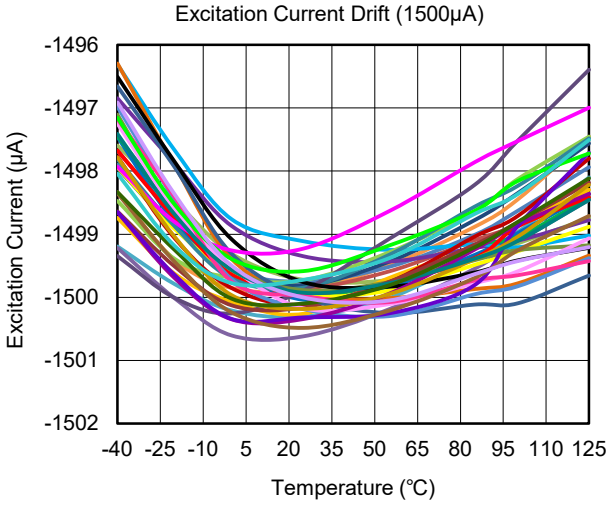
Excitation Current Drift (500μA)

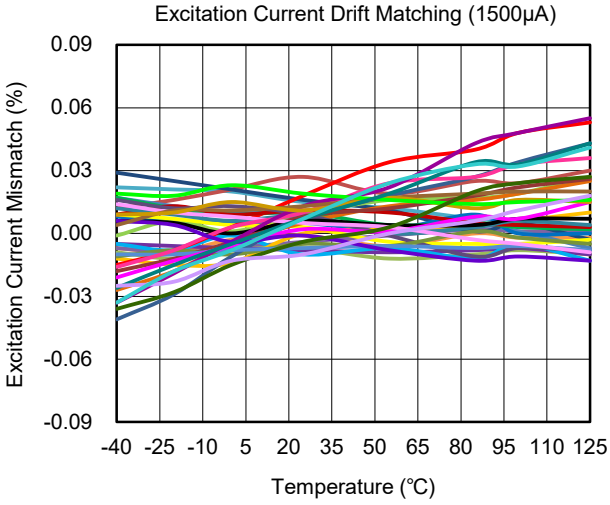


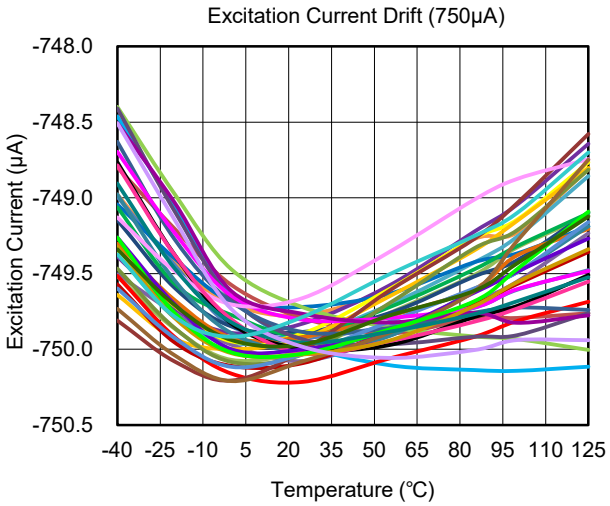
Excitation Current Drift Matching (500μA)

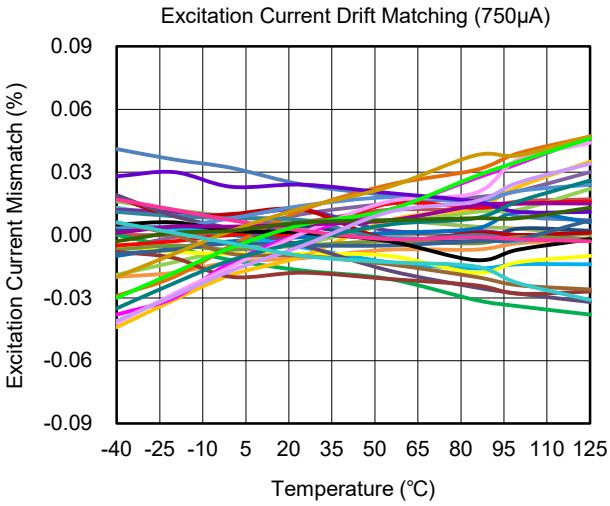


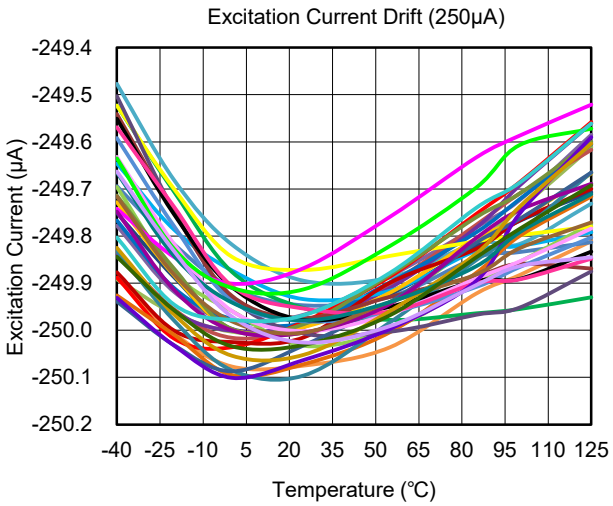
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

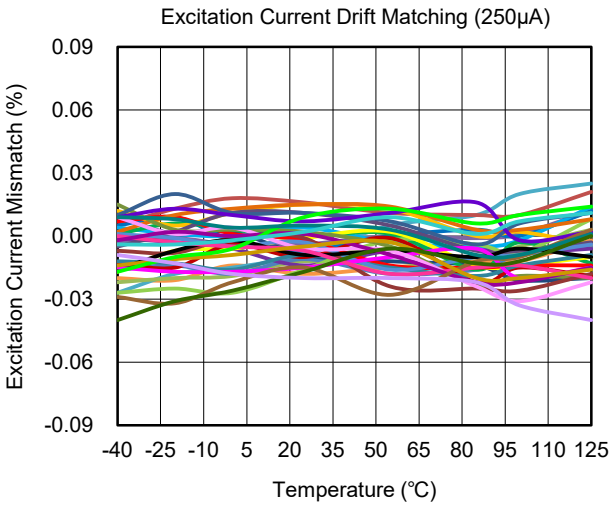




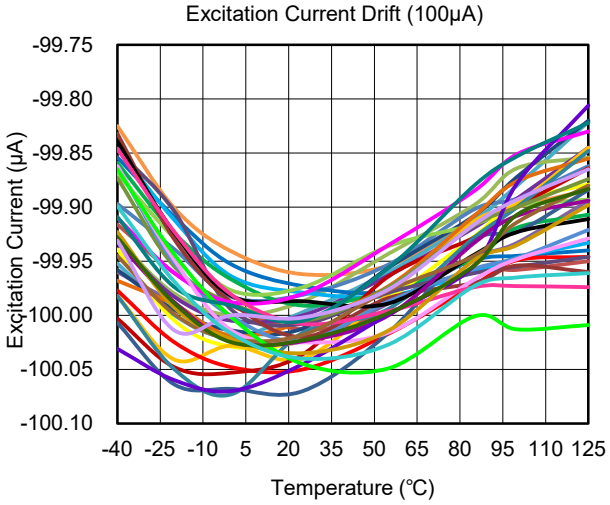


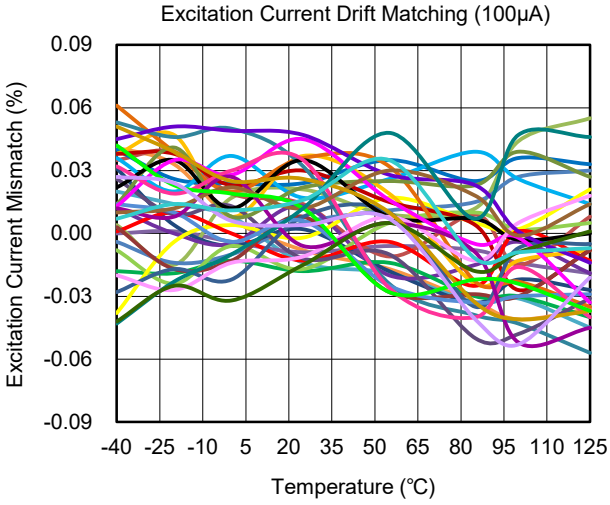


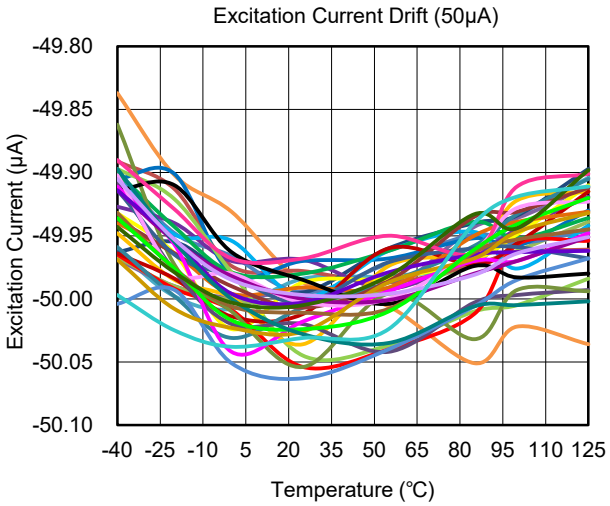


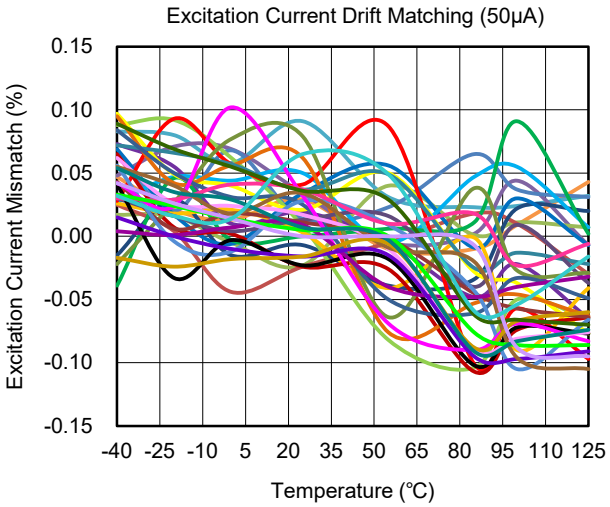


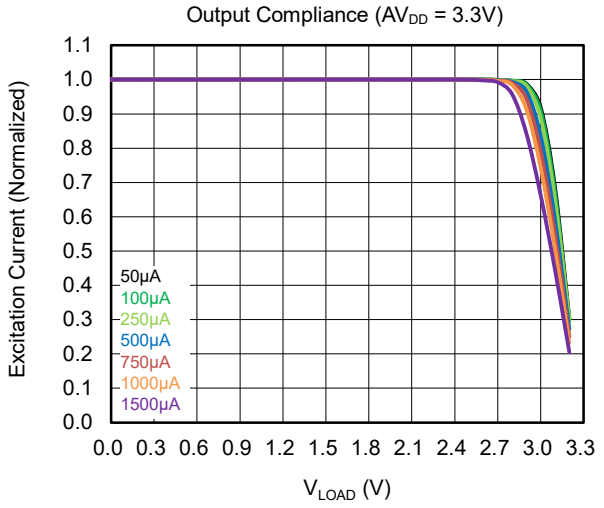
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

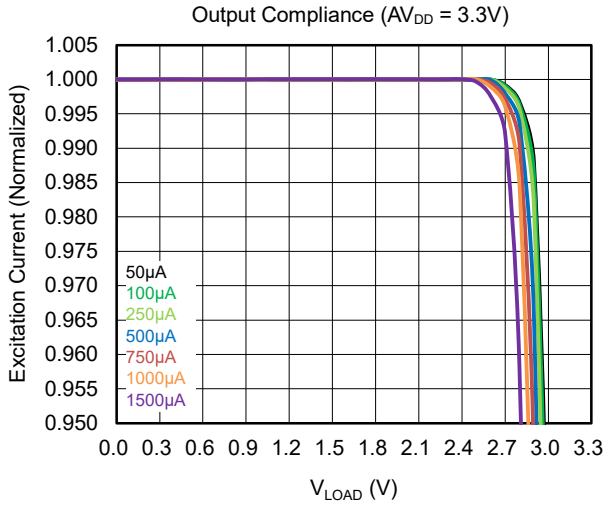






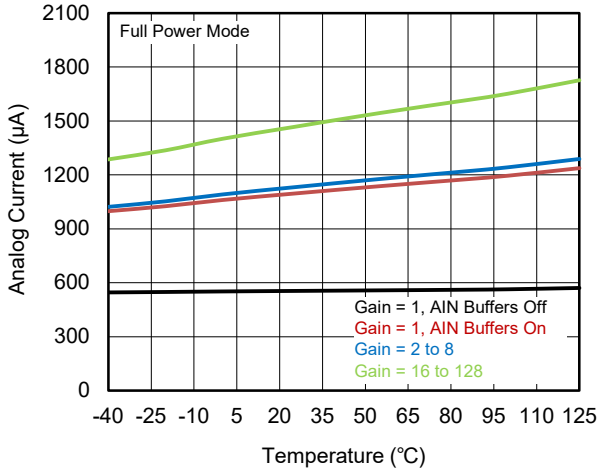




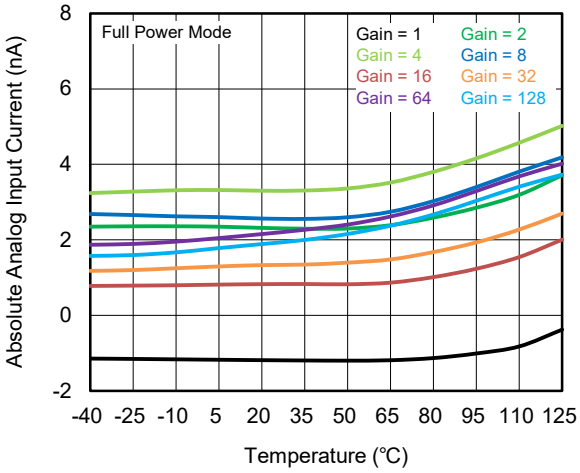


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

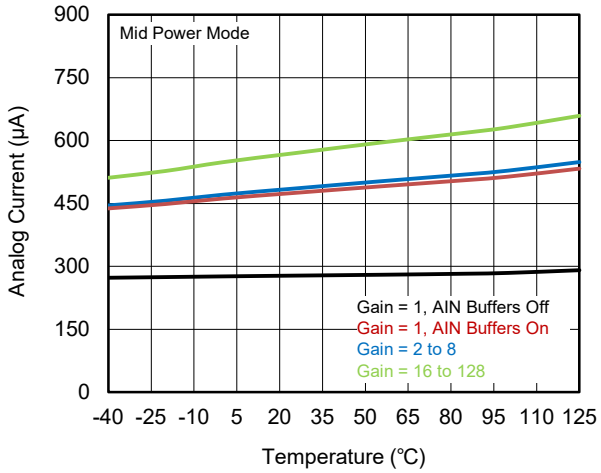
Analog Current vs. Temperature



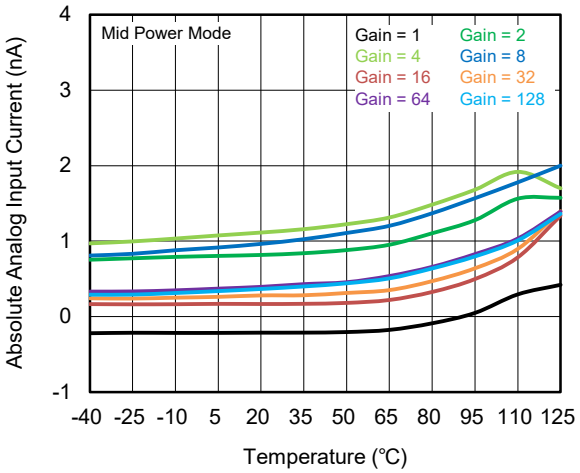
Absolute Analog Input Current vs. Temperature



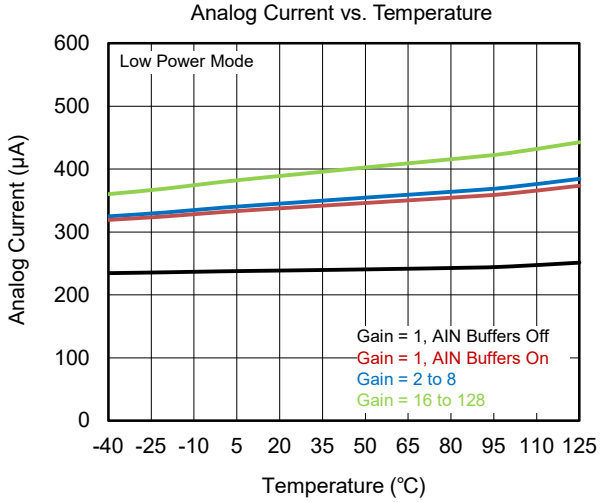
Analog Current vs. Temperature



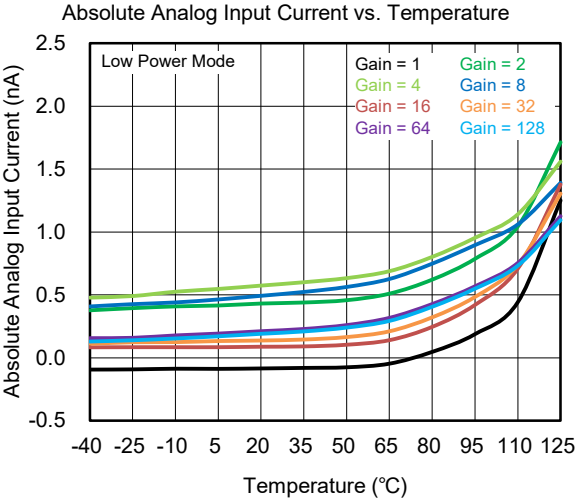
Absolute Analog Input Current vs. Temperature



Analog Current vs. Temperature

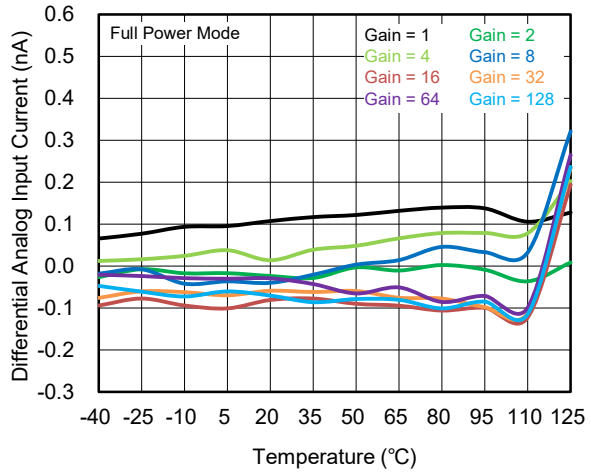


Absolute Analog Input Current vs. Temperature

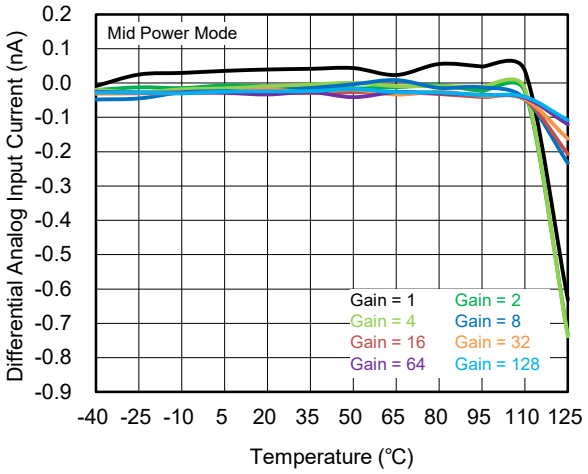


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

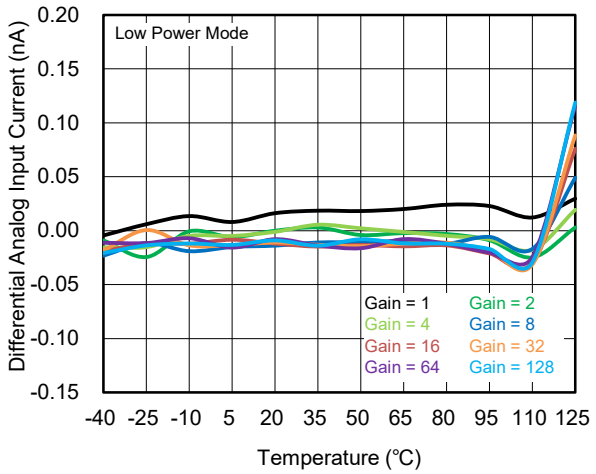
Differential Analog Input Current vs. Temperature



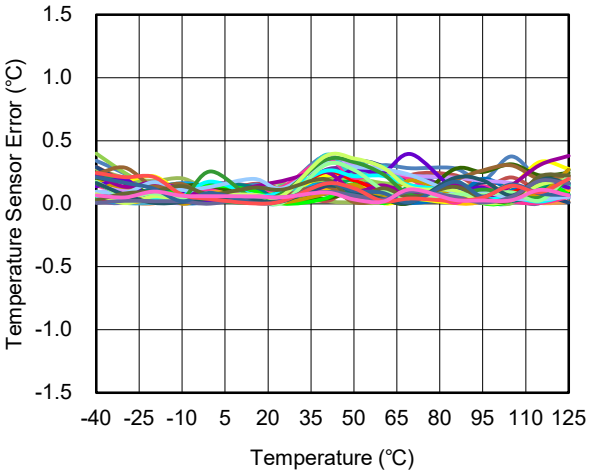
Differential Analog Input Current vs. Temperature



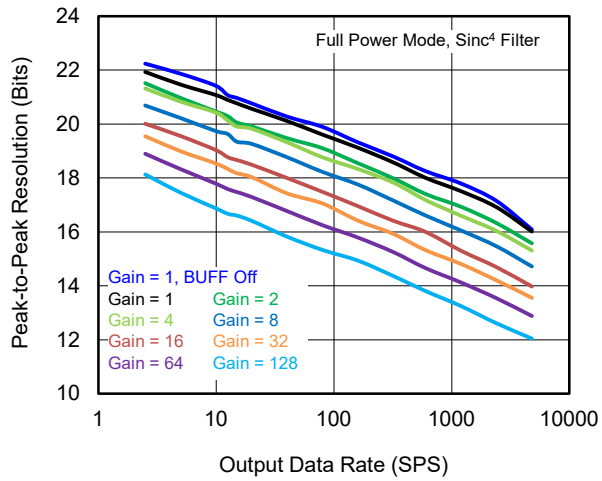
Differential Analog Input Current vs. Temperature



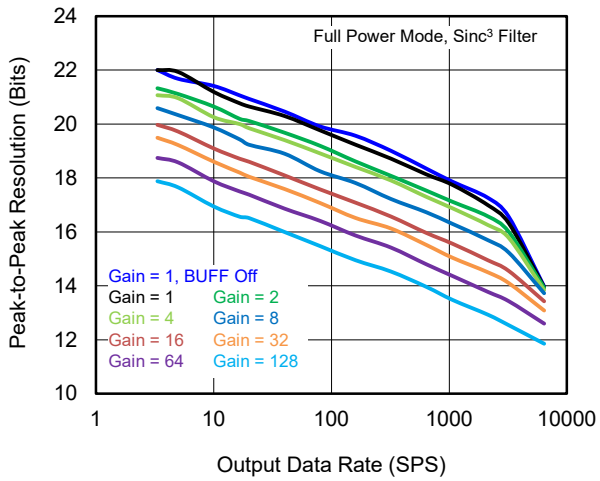
Temperature Sensor Accuracy



Peak-to-Peak Resolution vs. Output Data Rate (Settled)

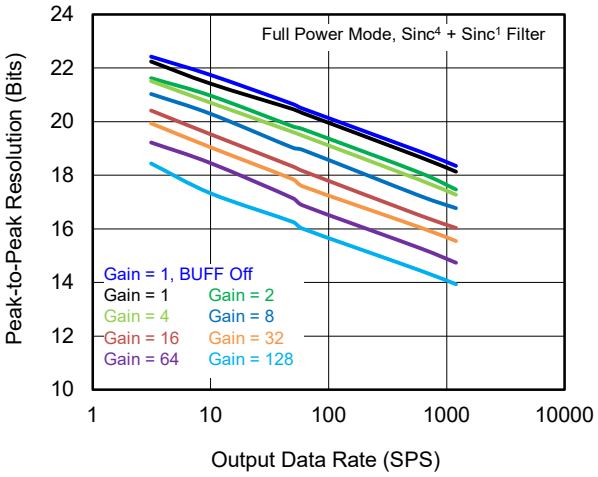


Peak-to-Peak Resolution vs. Output Data Rate (Settled)

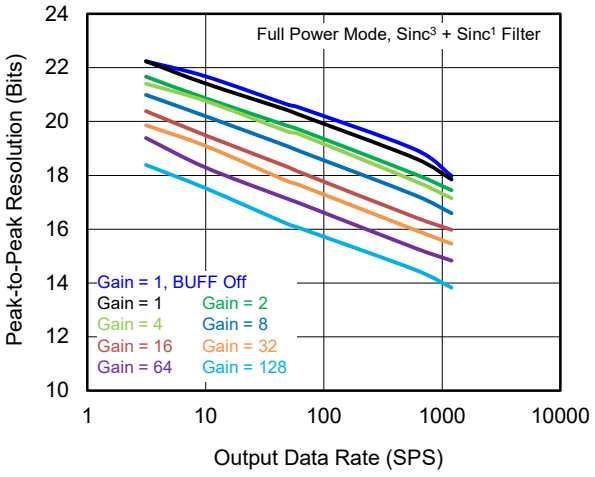


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

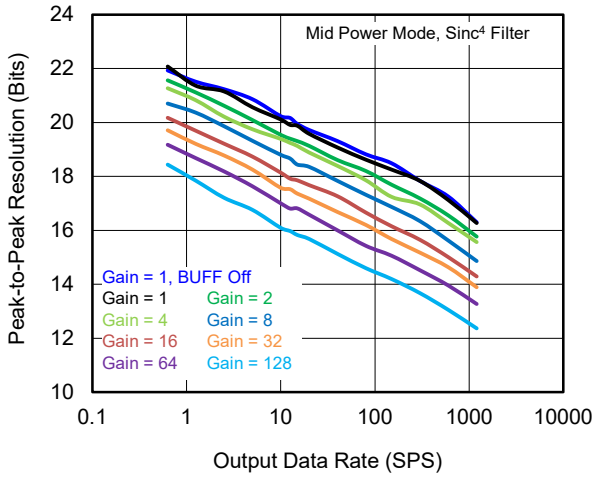
Peak-to-Peak Resolution vs. Output Data Rate



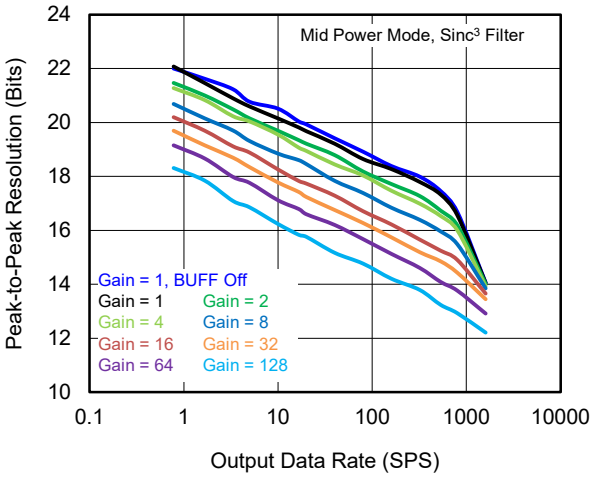
Peak-to-Peak Resolution vs. Output Data Rate



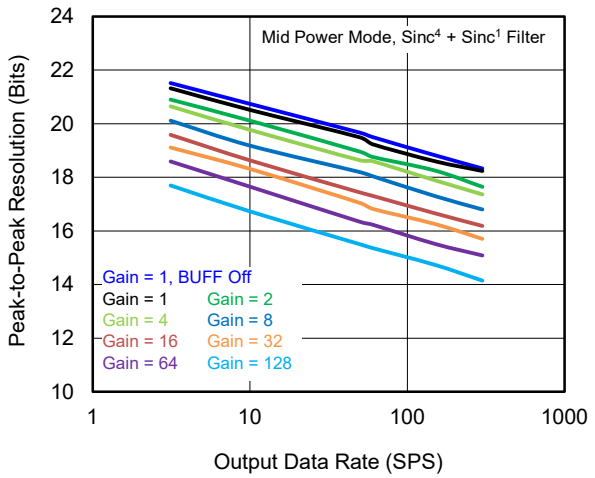
Peak-to-Peak Resolution vs. Output Data Rate (Settled)



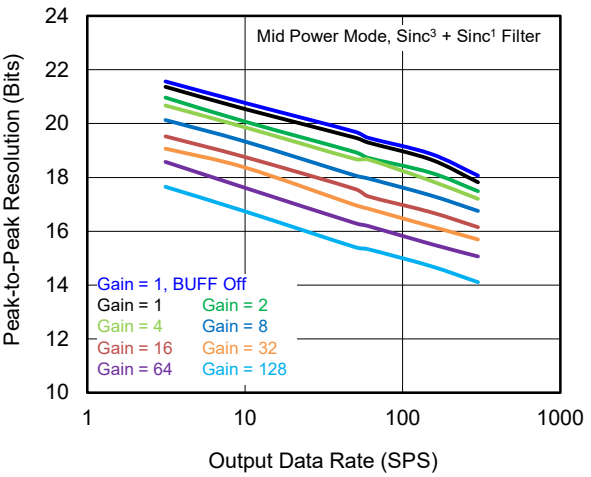
Peak-to-Peak Resolution vs. Output Data Rate (Settled)



Peak-to-Peak Resolution vs. Output Data Rate

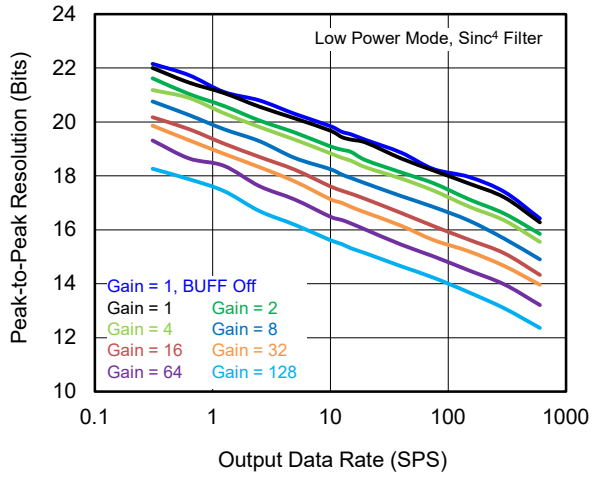


Peak-to-Peak Resolution vs. Output Data Rate

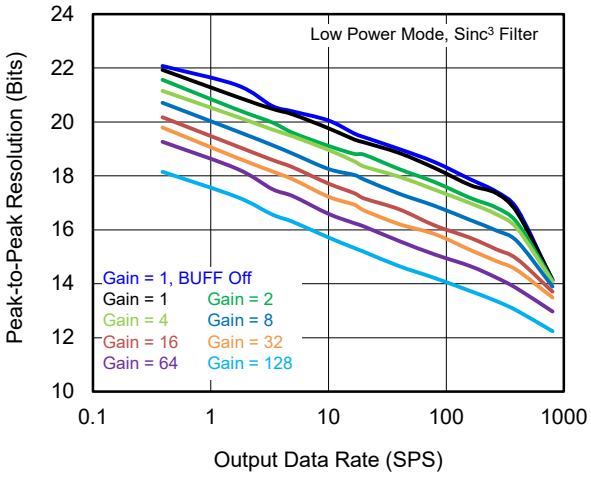


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

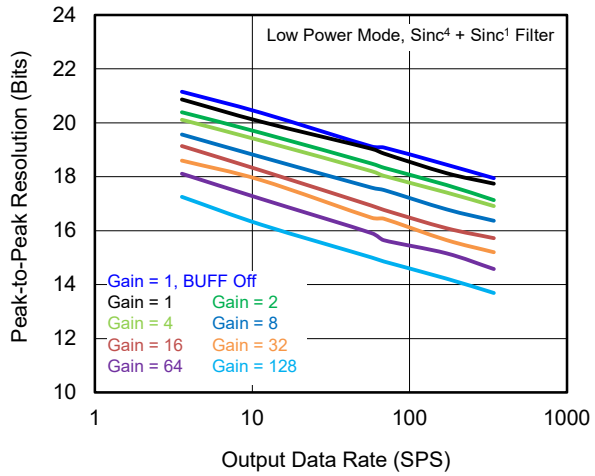
Peak-to-Peak Resolution vs. Output Data Rate (Settled)



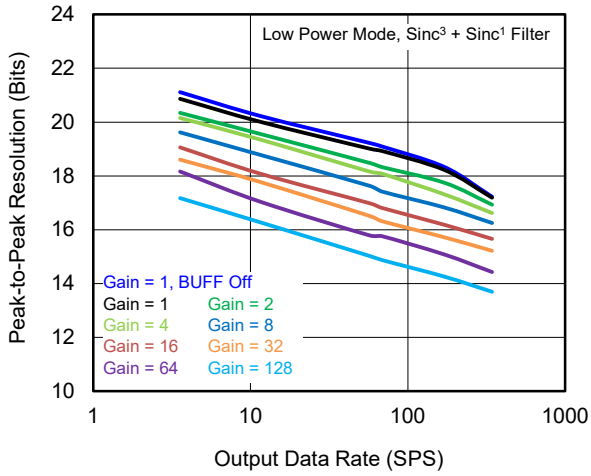
Peak-to-Peak Resolution vs. Output Data Rate (Settled)



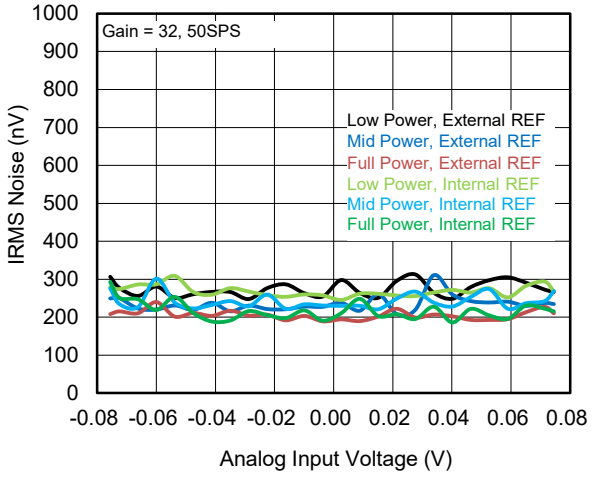
Peak-to-Peak Resolution vs. Output Data Rate



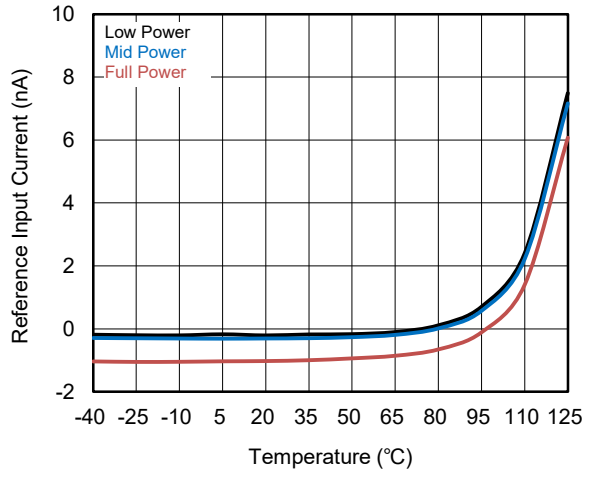
Peak-to-Peak Resolution vs. Output Data Rate



RMS Noise vs. Analog Input Voltage
for Internal Reference and External Reference

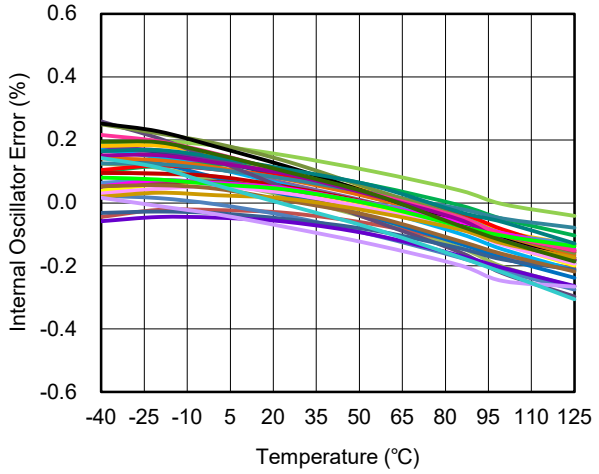


Reference Input Current vs. Temperature
(Reference Buffers Enabled)

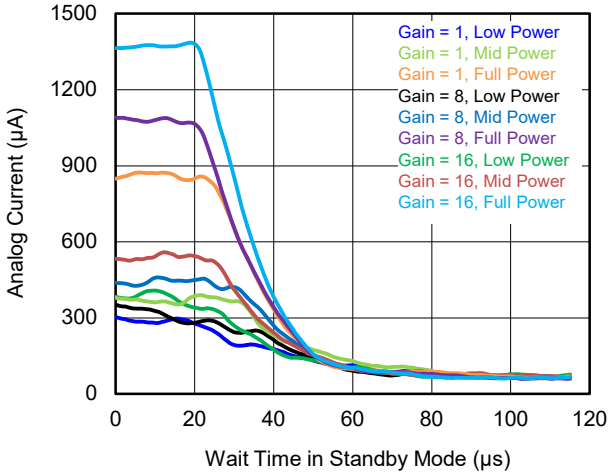


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

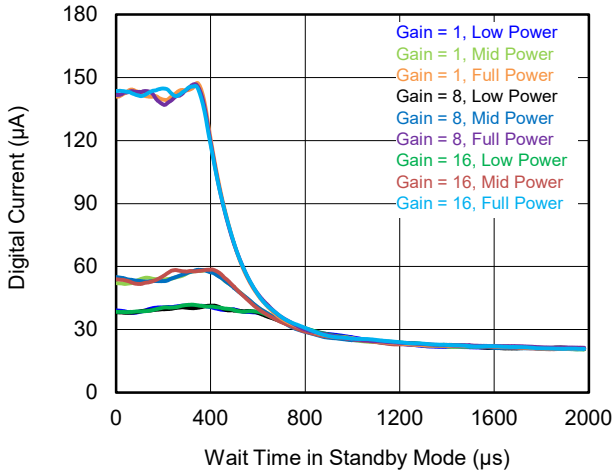
Internal Oscillator Error vs. Temperature



Analog Current vs. Wait Time in Standby Mode, ADC in Single Conversion Mode (50SPS)



Digital Current vs. Wait Time in Standby Mode, ADC in Single Conversion Mode (50SPS)



FUNCTIONAL BLOCK DIAGRAM

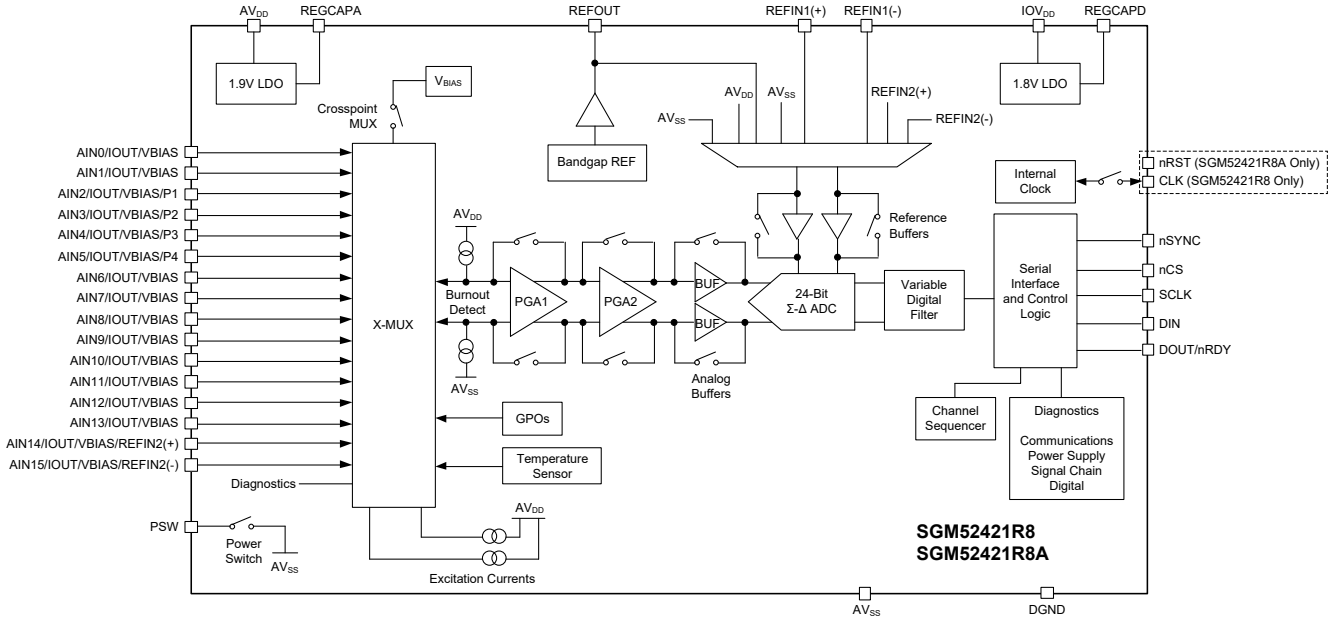


Figure 7. Block Diagram

RMS NOISE AND RESOLUTION

The RMS noise, effective resolution, peak-to-peak noise and noise-free (peak-to-peak) resolution for various output data rates, gain settings, and filters are shown in the below tables. Effective Resolution = Log_2 (Input Range/RMS Noise), and Peak-to-Peak Resolution = Log_2 (Input Range/Peak-to-Peak Noise).

Full Power Mode

Sinc[4]

Table 1. RMS Noise (Peak-to-Peak Noise) vs. Gain and Output Data Rate (μV), Full Power Mode

Filter Word (Dec.)	Output Data Rate (SPS)	Output Data Rate (Zero Latency Mode) (SPS)	f_{3dB} (Hz)	Gain = 1	Gain = 2	Gain = 4	Gain = 8	Gain = 16	Gain = 32	Gain = 64	Gain = 128
2047	9.38	2.34	2.16	0.22 (1.25)	0.14 (0.81)	0.079 (0.46)	0.056 (0.33)	0.049 (0.29)	0.033 (0.19)	0.027 (0.14)	0.024 (0.14)
1920	10	2.5	2.3	0.21 (1.25)	0.15 (0.83)	0.082 (0.48)	0.059 (0.37)	0.047 (0.30)	0.034 (0.20)	0.027 (0.16)	0.024 (0.14)
960	20	5	4.6	0.27 (1.73)	0.21 (1.22)	0.11 (0.67)	0.082 (0.51)	0.067 (0.41)	0.048 (0.30)	0.038 (0.24)	0.035 (0.22)
480	40	10	9.19	0.37 (2.27)	0.27 (1.73)	0.15 (0.89)	0.11 (0.72)	0.095 (0.58)	0.066 (0.41)	0.053 (0.35)	0.050 (0.33)
384	50	12.5	11.49	0.42 (2.56)	0.34 (1.94)	0.18 (1.09)	0.13 (0.77)	0.11 (0.70)	0.074 (0.47)	0.060 (0.40)	0.055 (0.37)
320	60	15	13.79	0.61 (2.80)	0.36 (2.29)	0.22 (1.27)	0.15 (0.94)	0.12 (0.75)	0.081 (0.53)	0.067 (0.43)	0.062 (0.39)
240	80	20	18.38	0.50 (3.22)	0.37 (2.53)	0.22 (1.34)	0.16 (0.99)	0.14 (0.85)	0.093 (0.58)	0.077 (0.49)	0.070 (0.45)
120	160	40	36.77	0.70 (4.41)	0.52 (3.43)	0.31 (1.91)	0.23 (1.40)	0.19 (1.19)	0.14 (0.89)	0.11 (0.70)	0.097 (0.67)
60	320	80	73.53	0.99 (6.26)	0.71 (4.44)	0.44 (2.80)	0.32 (2.04)	0.27 (1.70)	0.19 (1.15)	0.16 (1.00)	0.14 (0.95)
30	640	160	147.06	1.39 (8.76)	1.02 (6.53)	0.60 (3.79)	0.44 (2.82)	0.38 (2.46)	0.26 (1.79)	0.22 (1.38)	0.19 (1.25)
15	1280	320	294.13	1.92 (13)	1.43 (9.63)	0.86 (5.38)	0.63 (4.26)	0.53 (3.59)	0.38 (2.51)	0.30 (2.01)	0.28 (1.85)
8	2400	600	551.49	2.81 (19)	1.99 (14)	1.20 (8.40)	0.89 (6.26)	0.74 (4.77)	0.52 (3.81)	0.43 (3.03)	0.39 (2.73)
4	4800	1200	1103	3.84 (27)	2.82 (20)	1.68 (13)	1.25 (9.20)	1.05 (7.74)	0.73 (5.44)	0.59 (4.38)	0.54 (4.01)
2	9600	2400	2206	5.41 (40)	4.06 (30)	2.43 (19)	1.83 (14)	1.53 (12)	1.07 (8.28)	0.86 (6.56)	0.80 (6.25)
1	19200	4800	4411.9	8.96 (76)	6.42 (51)	3.85 (31)	2.89 (23)	2.42 (19)	1.64 (13)	1.30 (10)	1.19 (9.26)

Table 2. Effective Resolution (Peak-to-Peak Resolution) vs. Gain and Output Data Rate (Bits), Full Power Mode

Filter Word (Dec.)	Output Data Rate (SPS)	Output Data Rate (Zero Latency Mode) (SPS)	Gain = 1	Gain = 2	Gain = 4	Gain = 8	Gain = 16	Gain = 32	Gain = 64	Gain = 128
2047	9.38	2.34	24 (21.9)	24 (21.6)	23.9 (21.4)	23.4 (20.9)	22.6 (20)	22.2 (19.6)	21.5 (19.1)	20.6 (18.1)
1920	10	2.5	24 (21.9)	24 (21.5)	23.9 (21.3)	23.3 (20.7)	22.7 (20)	22.1 (19.5)	21.4 (18.9)	20.6 (18.1)
960	20	5	24 (21.5)	23.5 (21)	23.4 (20.8)	22.9 (20.2)	22.2 (19.6)	21.6 (19)	21 (18.3)	20.1 (17.5)
480	40	10	23.7 (21.1)	23.1 (20.5)	23 (20.4)	22.4 (19.7)	21.6 (19)	21.2 (18.5)	20.5 (17.8)	19.6 (16.9)
384	50	12.5	23.5 (20.9)	22.8 (20.3)	22.7 (20.1)	22.2 (19.6)	21.5 (18.8)	21 (18.3)	20.3 (17.6)	19.4 (16.7)
320	60	15	23 (20.8)	22.7 (20.1)	22.4 (19.9)	22 (19.3)	21.3 (18.7)	20.9 (18.2)	20.2 (17.5)	19.3 (16.6)
240	80	20	23.2 (20.6)	22.7 (19.9)	22.5 (19.8)	21.9 (19.3)	21.1 (18.5)	20.7 (18)	19.9 (17.3)	19.1 (16.4)
120	160	40	22.8 (20.1)	22.2 (19.5)	21.9 (19.3)	21.4 (18.8)	20.7 (18)	20.1 (17.4)	19.5 (16.8)	18.6 (15.8)
60	320	80	22.3 (19.6)	21.7 (19.1)	21.5 (18.8)	20.9 (18.2)	20.1 (17.5)	19.7 (17.1)	18.9 (16.2)	18.1 (15.3)
30	640	160	21.8 (19.1)	21.2 (18.5)	21 (18.3)	20.4 (17.8)	19.7 (17)	19.2 (16.4)	18.5 (15.8)	17.6 (14.9)
15	1280	320	21.3 (18.6)	20.7 (18)	20.5 (17.8)	19.9 (17.2)	19.2 (16.4)	18.7 (15.9)	18 (15.2)	17.1 (14.4)
8	2400	600	20.8 (18)	20.3 (17.4)	20 (17.2)	19.4 (16.6)	18.7 (16)	18.2 (15.3)	17.5 (14.7)	16.6 (13.8)
4	4800	1200	20.3 (17.5)	19.8 (16.9)	19.5 (16.6)	18.9 (16.1)	18.2 (15.3)	17.7 (14.8)	17 (14.1)	16.1 (13.2)
2	9600	2400	19.8 (16.9)	19.2 (16.3)	19 (16)	18.4 (15.5)	17.6 (14.7)	17.2 (14.2)	16.5 (13.5)	15.6 (12.6)
1	19200	4800	19.1 (16)	18.6 (15.6)	18.3 (15.3)	17.7 (14.7)	17 (14)	16.5 (13.6)	15.9 (12.9)	15 (12)

RMS NOISE AND RESOLUTION (continued)

Sinc^3

Table 3. RMS Noise (Peak-to-Peak Noise) vs. Gain and Output Data Rate (μV), Full Power Mode

Filter Word (Dec.)	Output Data Rate (SPS)	Output Data Rate (Zero Latency Mode) (SPS)	f_{3dB} (Hz)	Gain = 1	Gain = 2	Gain = 4	Gain = 8	Gain = 16	Gain = 32	Gain = 64	Gain = 128
2047	9.38	3.13	2.16	0.22 (1.37)	0.14 (0.89)	0.083 (0.46)	0.061 (0.40)	0.051 (0.32)	0.035 (0.20)	0.029 (0.15)	0.026 (0.15)
1920	10	3.33	2.3	0.21 (1.19)	0.16 (0.95)	0.087 (0.57)	0.061 (0.40)	0.053 (0.30)	0.035 (0.21)	0.029 (0.18)	0.026 (0.16)
1280	15	5	3.45	0.32 (1.25)	0.21 (1.10)	0.12 (0.61)	0.081 (0.47)	0.063 (0.36)	0.045 (0.26)	0.035 (0.20)	0.032 (0.19)
640	30	10	6.89	0.39 (2.09)	0.27 (1.52)	0.16 (1.00)	0.11 (0.65)	0.090 (0.56)	0.062 (0.39)	0.051 (0.32)	0.046 (0.31)
384	50	16.67	11.49	0.44 (2.80)	0.33 (2.09)	0.19 (1.19)	0.14 (0.89)	0.12 (0.73)	0.081 (0.52)	0.065 (0.42)	0.061 (0.40)
320	60	20	13.79	0.50 (3.04)	0.36 (2.21)	0.21 (1.33)	0.15 (1.02)	0.13 (0.79)	0.087 (0.58)	0.071 (0.46)	0.066 (0.42)
160	120	40	27.57	0.65 (3.88)	0.49 (2.98)	0.29 (1.80)	0.21 (1.28)	0.18 (1.12)	0.13 (0.79)	0.10 (0.66)	0.093 (0.60)
80	240	80	55.15	0.90 (5.60)	0.67 (4.17)	0.40 (2.53)	0.29 (2.01)	0.25 (1.60)	0.17 (1.13)	0.14 (0.90)	0.13 (0.86)
40	480	160	110.3	1.26 (8.11)	0.95 (6.23)	0.57 (3.59)	0.41 (2.71)	0.34 (2.25)	0.25 (1.67)	0.20 (1.31)	0.18 (1.23)
20	960	320	220.6	1.81 (12)	1.33 (9.03)	0.79 (5.08)	0.60 (4.09)	0.50 (3.21)	0.35 (2.18)	0.28 (1.78)	0.26 (1.65)
10	1920	640	441.19	2.56 (17)	1.89 (13)	1.12 (7.75)	0.83 (5.76)	0.71 (4.90)	0.49 (3.34)	0.40 (2.74)	0.38 (2.45)
6	3200	1066.67	735.32	3.27 (23)	2.46 (18)	1.46 (10)	1.08 (7.76)	0.92 (6.47)	0.65 (4.64)	0.52 (3.70)	0.48 (3.43)
3	6400	2133.33	1470.6	4.88 (38)	3.57 (26)	2.13 (16)	1.55 (12)	1.31 (9.89)	0.92 (6.74)	0.75 (5.58)	0.69 (5.01)
2	9600	3200	2206	7.48 (61)	4.95 (38)	2.88 (22)	2.05 (16)	1.68 (13)	1.16 (8.89)	0.93 (7.08)	0.86 (6.56)
1	19200	6400	4411.9	40 (316)	21 (160)	11 (85)	5.79 (46)	3.60 (28)	2.18 (18)	1.53 (13)	1.34 (11)

Table 4. Effective Resolution (Peak-to-Peak Resolution) vs. Gain and Output Data Rate, Full Power Mode

Filter Word (Dec.)	Output Data Rate (SPS)	Output Data Rate (Zero Latency Mode) (SPS)	Gain = 1	Gain = 2	Gain = 4	Gain = 8	Gain = 16	Gain = 32	Gain = 64	Gain = 128
2047	9.38	3.13	24 (21.8)	24 (21.4)	23.8 (21.4)	23.3 (20.6)	22.5 (19.9)	22.1 (19.5)	21.4 (19)	20.5 (18)
1920	10	3.33	24 (22)	23.9 (21.3)	23.8 (21.1)	23.3 (20.6)	22.5 (20)	22.1 (19.5)	21.4 (18.7)	20.5 (17.9)
1280	15	5	23.9 (21.9)	23.5 (21.1)	23.3 (21)	22.9 (20.3)	22.3 (19.7)	21.7 (19.2)	21.1 (18.6)	20.2 (17.6)
640	30	10	23.6 (21.2)	23.1 (20.6)	22.9 (20.3)	22.5 (19.9)	21.7 (19.1)	21.3 (18.6)	20.6 (17.9)	19.7 (16.9)
384	50	16.67	23.4 (20.8)	22.8 (20.2)	22.7 (20)	22.1 (19.4)	21.4 (18.7)	20.9 (18.2)	20.2 (17.5)	19.3 (16.6)
320	60	20	23.3 (20.6)	22.7 (20.1)	22.5 (19.8)	22 (19.2)	21.2 (18.6)	20.8 (18)	20.1 (17.4)	19.2 (16.5)
160	120	40	22.9 (20.3)	22.3 (19.7)	22 (19.4)	21.5 (18.9)	20.7 (18.1)	20.2 (17.6)	19.6 (16.9)	18.7 (16)
80	240	80	22.4 (19.8)	21.8 (19.2)	21.6 (18.9)	21 (18.2)	20.3 (17.6)	19.8 (17.1)	19.1 (16.4)	18.2 (15.5)
40	480	160	21.9 (19.2)	21.3 (18.6)	21.1 (18.4)	20.5 (17.8)	19.8 (17.1)	19.3 (16.5)	18.6 (15.9)	17.7 (15)
20	960	320	21.4 (18.7)	20.8 (18.1)	20.6 (17.9)	20 (17.2)	19.2 (16.6)	18.8 (16.1)	18.1 (15.4)	17.2 (14.5)
10	1920	640	20.9 (18.1)	20.3 (17.5)	20.1 (17.3)	19.5 (16.7)	18.7 (16)	18.3 (15.5)	17.6 (14.8)	16.7 (14)
6	3200	1066.67	20.5 (17.7)	20 (17.1)	19.7 (16.9)	19.1 (16.3)	18.4 (15.6)	17.9 (15)	17.2 (14.4)	16.3 (13.5)
3	6400	2133.33	20 (17)	19.4 (16.6)	19.2 (16.3)	18.6 (15.7)	17.9 (14.9)	17.4 (14.5)	16.7 (13.8)	15.8 (12.9)
2	9600	3200	19.4 (16.3)	18.9 (16)	18.7 (15.8)	18.2 (15.2)	17.5 (14.6)	17 (14.1)	16.4 (13.4)	15.5 (12.5)
1	19200	6400	16.9 (14)	16.9 (13.9)	16.8 (13.8)	16.7 (13.7)	16.4 (13.4)	16.1 (13.1)	15.6 (12.6)	14.8 (11.9)

RMS NOISE AND RESOLUTION (continued)

Post Filters

Table 5. RMS Noise (Peak-to-Peak Noise) vs. Gain and Output Data Rate (μV), Full Power Mode

Output Date Rate (SPS)	Gain = 1	Gain = 2	Gain = 4	Gain = 8	Gain = 16	Gain = 32	Gain = 64	Gain = 128
16.67	0.42 (2.74)	0.31 (2.00)	0.18 (1.24)	0.13 (0.88)	0.11 (0.68)	0.077 (0.46)	0.065 (0.39)	0.059 (0.34)
20	0.43 (2.62)	0.32 (1.97)	0.19 (1.21)	0.14 (0.90)	0.11 (0.67)	0.081 (0.49)	0.067 (0.39)	0.061 (0.37)
25	0.45 (2.98)	0.33 (2.15)	0.19 (1.15)	0.15 (0.94)	0.12 (0.77)	0.086 (0.55)	0.070 (0.45)	0.064 (0.42)
27.27	0.48 (2.98)	0.36 (2.30)	0.21 (1.40)	0.16 (0.96)	0.13 (0.85)	0.090 (0.57)	0.073 (0.49)	0.069 (0.45)

Table 6. Effective Resolution (Peak-to-Peak Resolution) vs. Gain and Output Data Rate (Bits), Full Power Mode

Output Date Rate (SPS)	Gain = 1	Gain = 2	Gain = 4	Gain = 8	Gain = 16	Gain = 32	Gain = 64	Gain = 128
16.67	23.5 (20.8)	22.9 (20.3)	22.7 (19.9)	22.2 (19.4)	21.4 (18.8)	21 (18.4)	20.2 (17.6)	19.3 (16.8)
20	23.5 (20.9)	22.9 (20.3)	22.7 (20)	22.1 (19.4)	21.4 (18.8)	20.9 (18.3)	20.1 (17.6)	19.3 (16.7)
25	23.4 (20.7)	22.9 (20.1)	22.6 (20.1)	22 (19.3)	21.3 (18.6)	20.8 (18.1)	20.1 (17.4)	19.2 (16.5)
27.27	23.3 (20.7)	22.7 (20.1)	22.5 (19.8)	21.9 (19.3)	21.2 (18.5)	20.7 (18.1)	20 (17.3)	19.1 (16.4)

Fast Settling Filter ($Sinc^4$ + $Sinc^1$)

Table 7. RMS Noise (Peak-to-Peak Noise) vs. Gain and Output Data Rate (μV), Full Power Mode (Average by 16)

Filter Word (Dec.)	Output Data Rate (SPS)	Gain = 1	Gain = 2	Gain = 4	Gain = 8	Gain = 16	Gain = 32	Gain = 64	Gain = 128
384	3.13	0.18 (1.01)	0.12 (0.78)	0.070 (0.42)	0.048 (0.29)	0.039 (0.22)	0.027 (0.16)	0.022 (0.13)	0.021 (0.11)
120	10	0.28 (1.79)	0.19 (1.22)	0.11 (0.73)	0.081 (0.49)	0.066 (0.41)	0.048 (0.29)	0.039 (0.22)	0.036 (0.24)
24	50	0.56 (3.46)	0.41 (2.71)	0.24 (1.57)	0.18 (1.18)	0.15 (0.95)	0.11 (0.66)	0.086 (0.54)	0.079 (0.50)
20	60	0.61 (3.82)	0.45 (2.89)	0.27 (1.71)	0.20 (1.24)	0.16 (1.07)	0.12 (0.79)	0.093 (0.65)	0.086 (0.59)
2	600	1.89 (12)	1.41 (9.00)	0.84 (5.42)	0.63 (4.09)	0.52 (3.39)	0.37 (2.31)	0.30 (1.97)	0.28 (1.75)
1	1200	2.68 (17)	2.01 (14)	1.20 (7.90)	0.88 (5.59)	0.74 (4.66)	0.53 (3.27)	0.43 (2.86)	0.39 (2.50)

Table 8. Effective Resolution (Peak-to-Peak Resolution) vs. Gain and Output Data Rate (Bits), Full Power Mode (Average by 16)

Filter Word (Dec.)	Output Data Rate (SPS)	Gain = 1	Gain = 2	Gain = 4	Gain = 8	Gain = 16	Gain = 32	Gain = 64	Gain = 128
384	3.13	24 (22.2)	24 (21.6)	24 (21.5)	23.6 (21)	22.9 (20.4)	22.4 (19.9)	21.7 (19.2)	20.9 (18.4)
120	10	24 (21.4)	23.6 (21)	23.4 (20.7)	22.9 (20.3)	22.2 (19.5)	21.6 (19)	20.9 (18.5)	20 (17.3)
24	50	23.1 (20.5)	22.5 (19.8)	22.3 (19.6)	21.7 (19)	21 (18.3)	20.5 (17.8)	19.8 (17.1)	18.9 (16.3)
20	60	23 (20.3)	22.4 (19.7)	22.2 (19.5)	21.6 (18.9)	20.9 (18.2)	20.3 (17.6)	19.7 (16.9)	18.8 (16)
2	600	21.3 (18.7)	20.8 (18.1)	20.5 (17.8)	19.9 (17.2)	19.2 (16.5)	18.7 (16)	18 (15.3)	17.1 (14.4)
1	1200	20.8 (18.1)	20.2 (17.5)	20 (17.3)	19.4 (16.8)	18.7 (16)	18.2 (15.5)	17.5 (14.7)	16.6 (13.9)

RMS NOISE AND RESOLUTION (continued)

Fast Settling Filter ($Sinc^3$ + $Sinc^1$)

Table 9. RMS Noise (Peak-to-Peak Noise) vs. Gain and Output Data Rate (μV), Full Power Mode (Average by 16)

Filter Word (Dec.)	Output Data Rate (SPS)	Gain = 1	Gain = 2	Gain = 4	Gain = 8	Gain = 16	Gain = 32	Gain = 64	Gain = 128
384	3.13	0.18 (1.01)	0.13 (0.75)	0.071 (0.45)	0.047 (0.30)	0.039 (0.23)	0.028 (0.16)	0.022 (0.11)	0.021 (0.11)
120	10	0.27 (1.79)	0.19 (1.31)	0.11 (0.70)	0.081 (0.52)	0.068 (0.43)	0.047 (0.28)	0.039 (0.24)	0.036 (0.21)
24	50	0.57 (3.58)	0.41 (2.68)	0.24 (1.55)	0.18 (1.14)	0.15 (0.97)	0.11 (0.70)	0.086 (0.55)	0.080 (0.53)
20	60	0.60 (3.94)	0.44 (2.89)	0.27 (1.63)	0.20 (1.25)	0.17 (1.08)	0.12 (0.75)	0.093 (0.60)	0.087 (0.57)
2	600	1.92 (12)	1.42 (9.33)	0.84 (5.59)	0.62 (4.02)	0.53 (3.54)	0.37 (2.46)	0.30 (1.96)	0.28 (1.71)
1	1200	3.27 (21)	2.21 (14)	1.27 (8.60)	0.92 (6.34)	0.76 (4.85)	0.53 (3.47)	0.42 (2.68)	0.39 (2.69)

Table 10. Effective Resolution (Peak-to-Peak Resolution) vs. Gain and Output Data Rate (Bits), Full Power Mode (Average by 16)

Filter Word (Dec.)	Output Data Rate (SPS)	Gain = 1	Gain = 2	Gain = 4	Gain = 8	Gain = 16	Gain = 32	Gain = 64	Gain = 128
384	3.13	24 (22.2)	24 (21.7)	24 (21.4)	23.7 (21)	22.9 (20.4)	22.4 (19.9)	21.8 (19.4)	20.8 (18.4)
120	10	24 (21.4)	23.6 (20.9)	23.4 (20.8)	22.9 (20.2)	22.1 (19.5)	21.7 (19.1)	20.9 (18.3)	20.1 (17.5)
24	50	23.1 (20.4)	22.5 (19.8)	22.3 (19.6)	21.7 (19.1)	21 (18.3)	20.5 (17.8)	19.8 (17.1)	18.9 (16.2)
20	60	23 (20.3)	22.4 (19.7)	22.2 (19.6)	21.6 (18.9)	20.8 (18.1)	20.4 (17.7)	19.7 (17)	18.8 (16.1)
2	600	21.3 (18.6)	20.7 (18)	20.5 (17.8)	19.9 (17.2)	19.2 (16.4)	18.7 (16)	18 (15.3)	17.1 (14.5)
1	1200	20.5 (17.8)	20.1 (17.4)	19.9 (17.1)	19.4 (16.6)	18.7 (16)	18.2 (15.5)	17.5 (14.8)	16.6 (13.8)

RMS NOISE AND RESOLUTION (continued)

Mid Power Mode

Sinc[4]

Table 11. RMS Noise (Peak-to-Peak Noise) vs. Gain and Output Data Rate (μV), Mid Power Mode

Filter Word (Dec.)	Output Data Rate (SPS)	Output Data Rate (Zero Latency Mode) (SPS)	f_{3dB} (Hz)	Gain = 1	Gain = 2	Gain = 4	Gain = 8	Gain = 16	Gain = 32	Gain = 64	Gain = 128
2047	2.34	0.59	0.54	0.22 (1.19)	0.13 (0.78)	0.075 (0.45)	0.054 (0.34)	0.043 (0.27)	0.028 (0.17)	0.022 (0.12)	0.020 (0.11)
1920	2.5	0.63	0.57	0.21 (1.13)	0.14 (0.81)	0.081 (0.49)	0.056 (0.37)	0.044 (0.26)	0.030 (0.18)	0.024 (0.13)	0.021 (0.11)
960	5	1.25	1.15	0.28 (1.85)	0.18 (1.10)	0.11 (0.67)	0.077 (0.46)	0.061 (0.37)	0.041 (0.26)	0.032 (0.19)	0.030 (0.17)
480	10	2.5	2.3	0.37 (2.15)	0.25 (1.55)	0.16 (1.03)	0.11 (0.66)	0.085 (0.51)	0.057 (0.35)	0.045 (0.26)	0.043 (0.26)
240	20	5	4.6	0.52 (3.22)	0.35 (2.24)	0.20 (1.42)	0.15 (0.95)	0.12 (0.72)	0.082 (0.50)	0.067 (0.38)	0.060 (0.35)
120	40	10	9.19	0.70 (4.41)	0.49 (3.28)	0.29 (1.82)	0.21 (1.37)	0.17 (1.08)	0.12 (0.80)	0.092 (0.60)	0.084 (0.56)
96	50	12.5	11.49	0.78 (5.06)	0.55 (3.61)	0.34 (2.01)	0.24 (1.50)	0.19 (1.26)	0.13 (0.83)	0.10 (0.68)	0.094 (0.61)
80	60	15	13.79	0.97 (5.19)	0.62 (3.85)	0.36 (2.18)	0.27 (1.76)	0.21 (1.32)	0.14 (0.93)	0.11 (0.68)	0.11 (0.67)
60	80	20	18.38	0.99 (6.38)	0.69 (4.35)	0.41 (2.58)	0.30 (1.86)	0.24 (1.49)	0.17 (1.06)	0.13 (0.80)	0.12 (0.74)
30	160	40	36.77	1.35 (9.06)	0.97 (6.26)	0.58 (3.64)	0.42 (2.67)	0.34 (1.98)	0.23 (1.49)	0.19 (1.19)	0.17 (1.09)
15	320	80	73.53	1.90 (12)	1.33 (8.29)	0.83 (5.26)	0.60 (3.82)	0.48 (3.02)	0.33 (2.07)	0.26 (1.77)	0.24 (1.58)
8	600	150	137.87	2.73 (16)	1.90 (12)	1.13 (8.06)	0.85 (5.22)	0.67 (4.29)	0.45 (2.98)	0.36 (2.29)	0.33 (2.08)
4	1200	300	275.74	3.69 (21)	2.67 (17)	1.59 (9.80)	1.17 (7.53)	0.96 (6.08)	0.66 (4.23)	0.51 (3.32)	0.47 (2.99)
2	2400	600	551.49	5.15 (35)	3.78 (26)	2.28 (16)	1.75 (12)	1.37 (9.50)	0.93 (6.16)	0.73 (4.92)	0.67 (4.61)
1	4800	1200	1103	8.66 (63)	6.12 (45)	3.67 (26)	2.76 (21)	2.10 (16)	1.42 (10)	1.13 (7.92)	1.02 (7.41)

Table 12. Effective Resolution (Peak-to-Peak Resolution) vs. Gain and Output Data Rate (Bits), Mid Power Mode

Filter Word (Dec.)	Output Data Rate (SPS)	Output Data Rate (Zero Latency Mode) (SPS)	Gain = 1	Gain = 2	Gain = 4	Gain = 8	Gain = 16	Gain = 32	Gain = 64	Gain = 128
2047	2.34	0.59	24 (22)	24 (21.6)	24 (21.4)	23.5 (20.8)	22.8 (20.1)	22.4 (19.8)	21.8 (19.3)	20.9 (18.5)
1920	2.5	0.63	24 (22.1)	24 (21.6)	23.9 (21.3)	23.4 (20.7)	22.8 (20.2)	22.3 (19.7)	21.6 (19.2)	20.8 (18.4)
960	5	1.25	24 (21.4)	23.7 (21.1)	23.4 (20.8)	23 (20.4)	22.3 (19.7)	21.9 (19.2)	21.2 (18.7)	20.3 (17.8)
480	10	2.5	23.7 (21.2)	23.2 (20.6)	22.9 (20.2)	22.5 (19.9)	21.8 (19.2)	21.4 (18.8)	20.7 (18.2)	19.8 (17.2)
240	20	5	23.2 (20.6)	22.8 (20.1)	22.5 (19.8)	22 (19.3)	21.3 (18.7)	20.9 (18.3)	20.1 (17.6)	19.3 (16.8)
120	40	10	22.8 (20.1)	22.3 (19.5)	22 (19.4)	21.5 (18.8)	20.8 (18.1)	20.4 (17.6)	19.7 (17)	18.8 (16.1)
96	50	12.5	22.6 (19.9)	22.1 (19.4)	21.8 (19.2)	21.3 (18.7)	20.6 (17.9)	20.2 (17.5)	19.5 (16.8)	18.7 (16)
80	60	15	22.3 (19.9)	21.9 (19.3)	21.7 (19.1)	21.2 (18.4)	20.5 (17.9)	20 (17.4)	19.4 (16.8)	18.5 (15.8)
60	80	20	22.3 (19.6)	21.8 (19.1)	21.6 (18.9)	21 (18.4)	20.3 (17.7)	19.8 (17.2)	19.2 (16.6)	18.3 (15.7)
30	160	40	21.8 (19.1)	21.3 (18.6)	21 (18.4)	20.5 (17.8)	19.8 (17.3)	19.4 (16.7)	18.7 (16)	17.8 (15.1)
15	320	80	21.3 (18.6)	20.8 (18.2)	20.5 (17.9)	20 (17.3)	19.3 (16.7)	18.9 (16.2)	18.2 (15.4)	17.3 (14.6)
8	600	150	20.8 (18.3)	20.3 (17.7)	20.1 (17.2)	19.5 (16.9)	18.8 (16.2)	18.4 (15.7)	17.7 (15.1)	16.9 (14.2)
4	1200	300	20.4 (17.8)	19.8 (17.2)	19.6 (17)	19 (16.3)	18.3 (15.6)	17.9 (15.2)	17.2 (14.5)	16.4 (13.7)
2	2400	600	19.9 (17.1)	19.3 (16.6)	19.1 (16.3)	18.4 (15.6)	17.8 (15)	17.4 (14.6)	16.7 (14)	15.8 (13.1)
1	4800	1200	19.1 (16.3)	18.6 (15.8)	18.4 (15.6)	17.8 (14.9)	17.2 (14.3)	16.8 (13.9)	16.1 (13.3)	15.2 (12.4)

RMS NOISE AND RESOLUTION (continued)

Sinc^3

Table 13. RMS Noise (Peak-to-Peak Noise) vs. Gain and Output Data Rate (μV), Mid Power Mode

Filter Word (Dec.)	Output Data Rate (SPS)	Output Data Rate (Zero Latency Mode) (SPS)	f_{3dB} (Hz)	Gain = 1	Gain = 2	Gain = 4	Gain = 8	Gain = 16	Gain = 32	Gain = 64	Gain = 128
2047	2.34	0.78	0.54	0.21 (1.13)	0.14 (0.86)	0.081 (0.49)	0.057 (0.37)	0.045 (0.26)	0.030 (0.18)	0.024 (0.13)	0.022 (0.12)
960	5	1.67	1.15	0.29 (1.73)	0.20 (1.19)	0.11 (0.67)	0.083 (0.54)	0.065 (0.37)	0.044 (0.27)	0.034 (0.19)	0.031 (0.17)
480	10	3.33	2.3	0.39 (2.56)	0.27 (1.70)	0.16 (1.01)	0.12 (0.73)	0.092 (0.55)	0.062 (0.37)	0.049 (0.30)	0.045 (0.28)
320	15	5	3.45	0.54 (3.16)	0.34 (2.15)	0.20 (1.16)	0.14 (0.96)	0.11 (0.65)	0.076 (0.47)	0.060 (0.35)	0.056 (0.33)
160	30	10	6.89	0.70 (4.29)	0.47 (2.95)	0.27 (1.63)	0.20 (1.33)	0.16 (1.00)	0.11 (0.70)	0.085 (0.55)	0.078 (0.51)
96	50	16.67	11.49	0.85 (5.42)	0.58 (3.76)	0.35 (2.28)	0.26 (1.57)	0.21 (1.34)	0.14 (0.89)	0.11 (0.69)	0.099 (0.67)
80	60	20	13.79	0.95 (5.96)	0.65 (4.11)	0.38 (2.48)	0.28 (1.74)	0.22 (1.43)	0.15 (1.01)	0.12 (0.79)	0.11 (0.70)
40	120	40	27.57	1.30 (8.23)	0.89 (5.51)	0.54 (3.50)	0.40 (2.67)	0.32 (1.95)	0.22 (1.41)	0.17 (1.04)	0.16 (1.06)
20	240	80	55.15	1.81 (12)	1.27 (8.41)	0.75 (4.65)	0.57 (3.65)	0.44 (2.92)	0.30 (1.97)	0.24 (1.49)	0.22 (1.40)
10	480	160	110.3	2.52 (16)	1.74 (12)	1.05 (6.89)	0.79 (5.33)	0.64 (4.10)	0.43 (2.86)	0.35 (2.18)	0.31 (2.07)
5	960	320	220.6	3.51 (22)	2.49 (16)	1.53 (9.62)	1.14 (7.28)	0.89 (6.05)	0.63 (4.18)	0.48 (3.13)	0.44 (2.76)
3	1600	533.33	367.66	4.61 (30)	3.39 (23)	2.02 (13)	1.51 (9.82)	1.19 (8.05)	0.80 (5.29)	0.64 (4.49)	0.58 (4.05)
2	2400	800	551.49	7.35 (52)	4.73 (33)	2.75 (19)	1.97 (14)	1.51 (10)	1.01 (7.08)	0.80 (5.61)	0.73 (5.01)
1	4800	1600	1103	40 (295)	21 (151)	11 (80)	5.70 (42)	3.33 (24)	1.95 (14)	1.37 (10)	1.14 (8.26)

Table 14. Effective Resolution (Peak-to-Peak Resolution) vs. Gain and Output Data Rate (Bits), Mid Power Mode

Filter Word (Dec.)	Output Data Rate (SPS)	Output Data Rate (Zero Latency Mode) (SPS)	Gain = 1	Gain = 2	Gain = 4	Gain = 8	Gain = 16	Gain = 32	Gain = 64	Gain = 128
2047	2.34	0.78	24 (22.1)	24 (21.5)	23.9 (21.3)	23.4 (20.7)	22.7 (20.2)	22.3 (19.7)	21.6 (19.2)	20.8 (18.3)
960	5	1.67	24 (21.5)	23.6 (21)	23.4 (20.8)	22.8 (20.2)	22.2 (19.7)	21.8 (19.2)	21.1 (18.7)	20.3 (17.8)
480	10	3.33	23.6 (20.9)	23.1 (20.5)	22.9 (20.2)	22.4 (19.7)	21.7 (19.1)	21.3 (18.7)	20.6 (18)	19.7 (17.1)
320	15	5	23.1 (20.6)	22.8 (20.2)	22.6 (20)	22 (19.3)	21.4 (18.9)	21 (18.3)	20.3 (17.8)	19.4 (16.9)
160	30	10	22.8 (20.2)	22.3 (19.7)	22.1 (19.6)	21.6 (18.8)	20.9 (18.3)	20.5 (17.8)	19.8 (17.1)	18.9 (16.2)
96	50	16.67	22.5 (19.8)	22 (19.3)	21.8 (19.1)	21.2 (18.6)	20.5 (17.8)	20.1 (17.4)	19.4 (16.8)	18.6 (15.8)
80	60	20	22.3 (19.7)	21.9 (19.2)	21.6 (18.9)	21.1 (18.5)	20.4 (17.7)	20 (17.2)	19.3 (16.6)	18.4 (15.8)
40	120	40	21.9 (19.2)	21.4 (18.8)	21.2 (18.4)	20.6 (17.8)	19.9 (17.3)	19.5 (16.8)	18.8 (16.2)	17.9 (15.2)
20	240	80	21.4 (18.6)	20.9 (18.2)	20.7 (18)	20.1 (17.4)	19.4 (16.7)	19 (16.3)	18.3 (15.7)	17.5 (14.8)
10	480	160	20.9 (18.3)	20.5 (17.7)	20.2 (17.5)	19.6 (16.8)	18.9 (16.2)	18.5 (15.7)	17.8 (15.1)	16.9 (14.2)
5	960	320	20.4 (17.8)	19.9 (17.3)	19.6 (17)	19.1 (16.4)	18.4 (15.7)	17.9 (15.2)	17.3 (14.6)	16.4 (13.8)
3	1600	533.33	20 (17.3)	19.5 (16.7)	19.2 (16.5)	18.7 (16)	18 (15.2)	17.6 (14.9)	16.9 (14.1)	16 (13.2)
2	2400	800	19.4 (16.6)	19 (16.2)	18.8 (16)	18.3 (15.5)	17.7 (14.9)	17.2 (14.4)	16.6 (13.8)	15.7 (12.9)
1	4800	1600	16.9 (14)	16.9 (14)	16.8 (13.9)	16.7 (13.8)	16.5 (13.7)	16.3 (13.4)	15.8 (12.9)	15.1 (12.2)

RMS NOISE AND RESOLUTION (continued)

Post Filters

Table 15. RMS Noise (Peak-to-Peak Noise) vs. Gain and Output Data Rate (μV), Mid Power Mode

Output Date Rate (SPS)	Gain = 1	Gain = 2	Gain = 4	Gain = 8	Gain = 16	Gain = 32	Gain = 64	Gain = 128
16.67	0.82 (5.84)	0.58 (3.67)	0.34 (2.27)	0.26 (1.62)	0.20 (1.26)	0.14 (0.84)	0.11 (0.71)	0.099 (0.61)
20	0.85 (5.43)	0.60 (3.94)	0.35 (2.15)	0.26 (1.59)	0.20 (1.24)	0.14 (0.83)	0.11 (0.72)	0.10 (0.65)
25	0.87 (5.66)	0.62 (4.02)	0.37 (2.30)	0.27 (1.75)	0.22 (1.38)	0.15 (0.94)	0.12 (0.77)	0.11 (0.69)
27.27	0.92 (6.20)	0.67 (4.23)	0.40 (2.52)	0.29 (1.97)	0.24 (1.54)	0.16 (1.05)	0.13 (0.84)	0.12 (0.76)

Table 16. Effective Resolution (Peak-to-Peak Resolution) vs. Gain and Output Data Rate (Bits), Mid Power Mode

Output Date Rate (SPS)	Gain = 1	Gain = 2	Gain = 4	Gain = 8	Gain = 16	Gain = 32	Gain = 64	Gain = 128
16.67	22.5 (19.7)	22 (19.4)	21.8 (19.1)	21.2 (18.6)	20.5 (17.9)	20.1 (17.5)	19.4 (16.8)	18.6 (16)
20	22.5 (19.8)	22 (19.3)	21.8 (19.2)	21.2 (18.6)	20.6 (17.9)	20.1 (17.5)	19.4 (16.7)	18.6 (15.9)
25	22.5 (19.8)	21.9 (19.2)	21.7 (19.1)	21.1 (18.4)	20.5 (17.8)	20 (17.3)	19.3 (16.6)	18.4 (15.8)
27.27	22.4 (19.6)	21.8 (19.2)	21.6 (18.9)	21 (18.3)	20.3 (17.6)	19.9 (17.2)	19.2 (16.5)	18.4 (15.7)

Fast Settling Filter ($Sinc^4$ + $Sinc^1$)

Table 17. Effective Resolution (Peak-to-Peak Resolution) vs. Gain and Output Data Rate (Bits), Mid Power Mode

Filter Word (Dec.)	Output Date Rate (SPS)	Gain = 1	Gain = 2	Gain = 4	Gain = 8	Gain = 16	Gain = 32	Gain = 64	Gain = 128
96	3.13	0.31 (1.91)	0.21 (1.28)	0.12 (0.76)	0.086 (0.55)	0.069 (0.40)	0.046 (0.28)	0.036 (0.20)	0.033 (0.18)
30	10	0.51 (3.34)	0.34 (2.21)	0.21 (1.40)	0.16 (1.05)	0.12 (0.77)	0.083 (0.48)	0.065 (0.38)	0.060 (0.36)
6	50	1.06 (6.80)	0.76 (4.92)	0.46 (3.07)	0.34 (2.09)	0.27 (1.76)	0.18 (1.16)	0.15 (0.94)	0.13 (0.84)
5	60	1.19 (8.11)	0.84 (5.63)	0.50 (3.14)	0.37 (2.32)	0.29 (1.92)	0.20 (1.35)	0.16 (1.01)	0.15 (0.93)
2	150	1.89 (13)	1.34 (8.02)	0.80 (5.16)	0.59 (3.88)	0.47 (3.03)	0.31 (2.00)	0.26 (1.67)	0.23 (1.43)
1	300	2.59 (16)	1.89 (12)	1.13 (7.42)	0.84 (5.48)	0.67 (4.19)	0.46 (2.93)	0.36 (2.25)	0.33 (2.16)

Table 18. Effective Resolution (Peak-to-Peak Resolution) vs. Gain and Output Data Rate (Bits), Mid Power Mode (Average by 16)

Filter Word (Dec.)	Output Date Rate (SPS)	Gain = 1	Gain = 2	Gain = 4	Gain = 8	Gain = 16	Gain = 32	Gain = 64	Gain = 128
96	3.13	24 (21.3)	23.5 (20.9)	23.3 (20.6)	22.8 (20.1)	22.1 (19.6)	21.7 (19.1)	21.1 (18.6)	20.2 (17.7)
30	10	23.2 (20.5)	22.8 (20.1)	22.5 (19.8)	21.9 (19.2)	21.3 (18.6)	20.8 (18.3)	20.2 (17.6)	19.3 (16.7)
6	50	22.2 (19.5)	21.6 (19)	21.4 (18.6)	20.8 (18.2)	20.1 (17.4)	19.7 (17)	19 (16.3)	18.2 (15.5)
5	60	22 (19.2)	21.5 (18.8)	21.3 (18.6)	20.7 (18)	20 (17.3)	19.6 (16.8)	18.9 (16.2)	18 (15.4)
2	150	21.3 (18.6)	20.8 (18.3)	20.6 (17.9)	20 (17.3)	19.3 (16.7)	18.9 (16.3)	18.2 (15.5)	17.4 (14.7)
1	300	20.9 (18.2)	20.3 (17.6)	20.1 (17.4)	19.5 (16.8)	18.8 (16.2)	18.4 (15.7)	17.7 (15.1)	16.9 (14.1)

RMS NOISE AND RESOLUTION (continued)

Fast Settling Filter ($Sinc^3$ + $Sinc^1$)

Table 19. RMS Noise (Peak-to-Peak Noise) vs. Gain and Output Data Rate (μV), Mid Power Mode (Average by 16)

Filter Word (Dec.)	Output Date Rate (SPS)	Gain = 1	Gain = 2	Gain = 4	Gain = 8	Gain = 16	Gain = 32	Gain = 64	Gain = 128
96	3.13	0.30 (1.85)	0.20 (1.22)	0.12 (0.75)	0.087 (0.54)	0.068 (0.41)	0.045 (0.28)	0.037 (0.20)	0.034 (0.19)
30	10	0.51 (3.28)	0.34 (2.27)	0.21 (1.31)	0.15 (0.95)	0.12 (0.71)	0.081 (0.46)	0.064 (0.39)	0.060 (0.36)
6	50	1.08 (6.85)	0.78 (4.98)	0.45 (2.97)	0.34 (2.27)	0.27 (1.61)	0.19 (1.22)	0.15 (0.97)	0.14 (0.90)
5	60	1.19 (7.75)	0.85 (5.75)	0.51 (3.00)	0.38 (2.44)	0.29 (1.94)	0.20 (1.33)	0.16 (1.04)	0.15 (0.95)
2	150	1.86 (12)	1.34 (8.44)	0.80 (5.19)	0.60 (3.78)	0.46 (2.91)	0.32 (2.10)	0.25 (1.65)	0.24 (1.46)
1	300	3.17 (22)	2.11 (14)	1.24 (8.29)	0.88 (5.66)	0.67 (4.30)	0.47 (2.95)	0.36 (2.28)	0.32 (2.22)

Table 20. Effective Resolution (Peak-to-Peak Resolution) vs. Gain and Output Data Rate (Bits), Mid Power Mode (Average by 16)

Filter Word (Dec.)	Output Date Rate (SPS)	Gain = 1	Gain = 2	Gain = 4	Gain = 8	Gain = 16	Gain = 32	Gain = 64	Gain = 128
96	3.13	24 (21.4)	23.6 (21)	23.3 (20.7)	22.8 (20.1)	22.1 (19.5)	21.7 (19.1)	21 (18.6)	20.1 (17.6)
30	10	23.2 (20.5)	22.8 (20.1)	22.5 (19.9)	22 (19.3)	21.3 (18.8)	20.9 (18.4)	20.2 (17.6)	19.3 (16.7)
6	50	22.1 (19.5)	21.6 (18.9)	21.4 (18.7)	20.8 (18.1)	20.2 (17.6)	19.7 (17)	19 (16.3)	18.1 (15.4)
5	60	22 (19.3)	21.5 (18.7)	21.2 (18.7)	20.7 (18)	20 (17.3)	19.5 (16.8)	18.9 (16.2)	18 (15.3)
2	150	21.4 (18.7)	20.8 (18.2)	20.6 (17.9)	20 (17.3)	19.4 (16.7)	18.9 (16.2)	18.3 (15.5)	17.3 (14.7)
1	300	20.6 (17.8)	20.2 (17.5)	19.9 (17.2)	19.4 (16.8)	18.8 (16.2)	18.4 (15.7)	17.7 (15.1)	16.9 (14.1)

RMS NOISE AND RESOLUTION (continued)

Low Power Mode

Sinc[4]

Table 21. RMS Noise (Peak-to-Peak Noise) vs. Gain and Output Data Rate (μV), Low Power Mode

Filter Word (Dec.)	Output Data Rate (SPS)	Output Data Rate (Zero Latency Mode) (SPS)	f_{3dB} (Hz)	Gain = 1	Gain = 2	Gain = 4	Gain = 8	Gain = 16	Gain = 32	Gain = 64	Gain = 128
2047	1.17	0.29	0.27	0.21 (1.13)	0.13 (0.78)	0.076 (0.49)	0.055 (0.36)	0.043 (0.25)	0.029 (0.17)	0.023 (0.13)	0.021 (0.11)
1920	1.25	0.31	0.29	0.21 (1.19)	0.15 (0.78)	0.079 (0.52)	0.057 (0.35)	0.043 (0.26)	0.027 (0.16)	0.023 (0.12)	0.022 (0.12)
960	2.5	0.63	0.57	0.27 (1.73)	0.19 (1.16)	0.11 (0.64)	0.079 (0.50)	0.061 (0.36)	0.042 (0.24)	0.032 (0.19)	0.030 (0.16)
480	5	1.25	1.15	0.38 (2.27)	0.25 (1.58)	0.15 (0.95)	0.11 (0.72)	0.087 (0.52)	0.057 (0.34)	0.044 (0.23)	0.042 (0.22)
240	10	2.5	2.3	0.51 (3.22)	0.35 (2.30)	0.22 (1.36)	0.16 (0.98)	0.12 (0.73)	0.080 (0.48)	0.066 (0.39)	0.060 (0.37)
120	20	5	4.6	0.71 (4.35)	0.49 (3.13)	0.30 (1.88)	0.23 (1.51)	0.17 (1.02)	0.12 (0.69)	0.088 (0.55)	0.082 (0.52)
60	40	10	9.19	0.96 (5.96)	0.69 (4.47)	0.42 (2.67)	0.31 (2.01)	0.24 (1.56)	0.16 (1.09)	0.13 (0.85)	0.12 (0.78)
48	50	12.5	11.49	1.11 (7.03)	0.78 (4.86)	0.47 (3.00)	0.35 (2.30)	0.28 (1.74)	0.18 (1.19)	0.14 (0.93)	0.13 (0.86)
40	60	15	13.79	1.24 (7.51)	0.87 (5.16)	0.51 (3.23)	0.39 (2.52)	0.30 (1.89)	0.20 (1.33)	0.16 (1.01)	0.15 (0.96)
30	80	20	18.38	1.35 (8.11)	1.01 (6.38)	0.60 (3.83)	0.44 (2.90)	0.34 (2.17)	0.23 (1.53)	0.18 (1.19)	0.17 (1.09)
15	160	40	36.77	1.88 (12)	1.39 (8.73)	0.83 (5.11)	0.63 (4.01)	0.49 (3.10)	0.33 (2.15)	0.26 (1.75)	0.23 (1.52)
8	300	75	68.94	2.70 (17)	1.92 (12)	1.15 (6.96)	0.84 (5.30)	0.67 (4.33)	0.46 (3.10)	0.36 (2.36)	0.33 (2.04)
4	600	150	137.87	3.74 (23)	2.70 (17)	1.62 (10)	1.22 (7.53)	0.95 (6.15)	0.65 (4.15)	0.50 (3.39)	0.46 (2.98)
2	1200	300	275.74	5.29 (33)	3.91 (25)	2.36 (15)	1.77 (12)	1.39 (8.74)	0.94 (6.05)	0.73 (4.85)	0.67 (4.49)
1	2400	600	551.49	8.74 (63)	6.15 (42)	3.73 (26)	2.80 (20)	2.13 (15)	1.44 (9.79)	1.15 (8.25)	1.05 (7.43)

Table 22. Effective Resolution (Peak-to-Peak Resolution) vs. Gain and Output Data Rate (Bits), Low Power Mode

Filter Word (Dec.)	Output Data Rate (SPS)	Output Data Rate (Zero Latency Mode) (SPS)	Gain = 1	Gain = 2	Gain = 4	Gain = 8	Gain = 16	Gain = 32	Gain = 64	Gain = 128
2047	1.17	0.29	24 (22.1)	24 (21.6)	24 (21.3)	23.4 (20.7)	22.8 (20.3)	22.4 (19.8)	21.7 (19.2)	20.8 (18.4)
1920	1.25	0.31	24 (22)	24 (21.6)	23.9 (21.2)	23.4 (20.8)	22.8 (20.2)	22.4 (19.9)	21.7 (19.3)	20.7 (18.3)
960	2.5	0.63	24 (21.5)	23.6 (21)	23.5 (20.9)	22.9 (20.3)	22.3 (19.7)	21.8 (19.3)	21.2 (18.6)	20.3 (17.9)
480	5	1.25	23.6 (21.1)	23.2 (20.6)	23 (20.3)	22.4 (19.7)	21.8 (19.2)	21.4 (18.8)	20.7 (18.4)	19.8 (17.4)
240	10	2.5	23.2 (20.6)	22.8 (20.1)	22.5 (19.8)	21.9 (19.3)	21.3 (18.7)	20.9 (18.3)	20.2 (17.6)	19.3 (16.7)
120	20	5	22.7 (20.1)	22.3 (19.6)	22 (19.3)	21.4 (18.7)	20.8 (18.2)	20.4 (17.8)	19.8 (17.1)	18.9 (16.2)
60	40	10	22.3 (19.7)	21.8 (19.1)	21.5 (18.8)	20.9 (18.2)	20.3 (17.6)	19.9 (17.1)	19.2 (16.5)	18.3 (15.6)
48	50	12.5	22.1 (19.4)	21.6 (19)	21.3 (18.7)	20.8 (18.1)	20.1 (17.5)	19.7 (17)	19.1 (16.4)	18.2 (15.5)
40	60	15	21.9 (19.3)	21.5 (18.9)	21.2 (18.6)	20.6 (17.9)	20 (17.3)	19.6 (16.8)	18.9 (16.2)	18 (15.3)
30	80	20	21.8 (19.2)	21.2 (18.6)	21 (18.3)	20.4 (17.7)	19.8 (17.1)	19.3 (16.6)	18.7 (16)	17.8 (15.1)
15	160	40	21.3 (18.6)	20.8 (18.1)	20.5 (17.9)	19.9 (17.3)	19.3 (16.6)	18.8 (16.1)	18.2 (15.4)	17.3 (14.6)
8	300	75	20.8 (18.2)	20.3 (17.7)	20.1 (17.5)	19.5 (16.8)	18.8 (16.1)	18.4 (15.6)	17.7 (15)	16.8 (14.2)
4	600	150	20.3 (17.7)	19.8 (17.1)	19.6 (16.9)	19 (16.3)	18.3 (15.6)	17.9 (15.2)	17.2 (14.5)	16.4 (13.7)
2	1200	300	19.9 (17.2)	19.3 (16.6)	19 (16.3)	18.4 (15.7)	17.8 (15.1)	17.3 (14.7)	16.7 (14)	15.8 (13.1)
1	2400	600	19.1 (16.3)	18.6 (15.8)	18.4 (15.6)	17.8 (14.9)	17.2 (14.3)	16.7 (14)	16.1 (13.2)	15.2 (12.4)

RMS NOISE AND RESOLUTION (continued)

Sinc^3

Table 23. RMS Noise (Peak-to-Peak Noise) vs. Gain and Output Data Rate (μV), Low Power Mode

Filter Word (Dec.)	Output Data Rate (SPS)	Output Data Rate (Zero Latency Mode) (SPS)	f_{3dB} (Hz)	Gain = 1	Gain = 2	Gain = 4	Gain = 8	Gain = 16	Gain = 32	Gain = 64	Gain = 128
2047	1.17	0.39	0.27	0.21 (1.25)	0.14 (0.81)	0.083 (0.54)	0.058 (0.36)	0.046 (0.26)	0.030 (0.17)	0.024 (0.12)	0.023 (0.13)
480	5	1.67	1.15	0.40 (2.50)	0.27 (1.73)	0.16 (1.04)	0.12 (0.76)	0.093 (0.56)	0.063 (0.37)	0.048 (0.25)	0.045 (0.26)
240	10	3.33	2.3	0.54 (3.40)	0.37 (2.41)	0.23 (1.45)	0.17 (1.08)	0.13 (0.79)	0.087 (0.53)	0.069 (0.42)	0.064 (0.40)
160	15	5	3.45	0.70 (3.93)	0.48 (3.16)	0.29 (1.73)	0.21 (1.35)	0.16 (0.96)	0.11 (0.65)	0.084 (0.50)	0.077 (0.49)
80	30	10	6.89	0.94 (5.60)	0.67 (4.41)	0.40 (2.44)	0.29 (2.00)	0.22 (1.45)	0.15 (1.02)	0.12 (0.79)	0.11 (0.73)
48	50	16.67	11.49	1.15 (7.51)	0.83 (5.43)	0.50 (3.29)	0.38 (2.33)	0.30 (1.87)	0.20 (1.25)	0.15 (1.01)	0.15 (0.95)
40	60	20	13.79	1.28 (8.05)	0.91 (5.52)	0.56 (3.74)	0.41 (2.61)	0.32 (2.12)	0.21 (1.45)	0.17 (1.09)	0.15 (1.05)
20	120	40	27.57	1.81 (11)	1.27 (8.02)	0.77 (4.87)	0.57 (3.78)	0.45 (2.82)	0.30 (2.06)	0.24 (1.59)	0.23 (1.52)
10	240	80	55.15	2.48 (16)	1.79 (11)	1.10 (6.81)	0.82 (5.16)	0.65 (4.27)	0.43 (2.66)	0.34 (2.25)	0.31 (2.06)
5	480	160	110.3	3.53 (24)	2.53 (17)	1.53 (9.63)	1.16 (7.42)	0.92 (5.86)	0.61 (4.00)	0.49 (3.03)	0.45 (2.87)
3	800	266.67	183.83	4.67 (30)	3.39 (22)	2.04 (13)	1.50 (9.71)	1.19 (7.88)	0.80 (5.33)	0.64 (4.08)	0.58 (3.73)
2	1200	400	275.74	7.34 (49)	4.77 (32)	2.78 (18)	2.01 (13)	1.51 (10)	1.02 (6.74)	0.80 (5.40)	0.73 (4.77)
1	2400	800	551.49	40 (275)	20 (141)	10 (72)	5.75 (41)	3.35 (23)	1.99 (14)	1.40 (9.74)	1.18 (8.08)

Table 24. Effective Resolution (Peak-to-Peak Resolution) vs. Gain and Output Data Rate, Low Power Mode

Filter Word (Dec.)	Output Data Rate (SPS)	Output Data Rate (Zero Latency Mode) (SPS)	Gain = 1	Gain = 2	Gain = 4	Gain = 8	Gain = 16	Gain = 32	Gain = 64	Gain = 128
2047	1.17	0.39	24 (21.9)	24 (21.6)	23.9 (21.2)	23.4 (20.7)	22.7 (20.2)	22.3 (19.8)	21.7 (19.3)	20.7 (18.2)
480	5	1.67	23.6 (20.9)	23.1 (20.5)	22.9 (20.2)	22.3 (19.7)	21.7 (19.1)	21.2 (18.7)	20.6 (18.3)	19.7 (17.2)
240	10	3.33	23.1 (20.5)	22.7 (20)	22.4 (19.7)	21.8 (19.1)	21.2 (18.6)	20.8 (18.2)	20.1 (17.5)	19.2 (16.6)
160	15	5	22.8 (20.3)	22.3 (19.6)	22 (19.5)	21.5 (18.8)	20.9 (18.3)	20.5 (17.9)	19.8 (17.2)	18.9 (16.3)
80	30	10	22.3 (19.8)	21.8 (19.1)	21.6 (19)	21 (18.3)	20.4 (17.7)	20 (17.2)	19.3 (16.6)	18.5 (15.7)
48	50	16.67	22.1 (19.3)	21.5 (18.8)	21.3 (18.5)	20.7 (18)	20 (17.4)	19.6 (16.9)	19 (16.2)	18 (15.3)
40	60	20	21.9 (19.2)	21.4 (18.8)	21.1 (18.4)	20.5 (17.9)	19.9 (17.2)	19.5 (16.7)	18.8 (16.1)	18 (15.2)
20	120	40	21.4 (18.8)	20.9 (18.3)	20.6 (18)	20.1 (17.3)	19.4 (16.8)	19 (16.2)	18.3 (15.6)	17.4 (14.6)
10	240	80	20.9 (18.3)	20.4 (17.8)	20.1 (17.5)	19.5 (16.9)	18.9 (16.2)	18.5 (15.8)	17.8 (15.1)	16.9 (14.2)
5	480	160	20.4 (17.7)	19.9 (17.2)	19.6 (17)	19 (16.4)	18.4 (15.7)	18 (15.3)	17.3 (14.7)	16.4 (13.7)
3	800	266.67	20 (17.4)	19.5 (16.8)	19.2 (16.6)	18.7 (16)	18 (15.3)	17.6 (14.8)	16.9 (14.2)	16 (13.4)
2	1200	400	19.4 (16.6)	19 (16.3)	18.8 (16.1)	18.2 (15.6)	17.7 (14.9)	17.2 (14.5)	16.6 (13.8)	15.7 (13)
1	2400	800	16.9 (14.2)	16.9 (14.1)	16.9 (14.1)	16.7 (13.9)	16.5 (13.7)	16.3 (13.5)	15.8 (13)	15 (12.2)

RMS NOISE AND RESOLUTION (continued)

Post Filters

Table 25. RMS Noise (Peak-to-Peak Noise) vs. Gain and Output Data Rate (μV), Low Power Mode

Output Date Rate (SPS)	Gain = 1	Gain = 2	Gain = 4	Gain = 8	Gain = 16	Gain = 32	Gain = 64	Gain = 128
16.67	1.13 (7.15)	0.83 (5.46)	0.49 (3.18)	0.37 (2.40)	0.28 (1.63)	0.19 (1.20)	0.15 (0.91)	0.13 (0.85)
20	1.16 (7.57)	0.83 (5.55)	0.50 (3.38)	0.38 (2.57)	0.29 (1.77)	0.20 (1.12)	0.15 (0.92)	0.14 (0.85)
25	1.23 (8.11)	0.88 (5.51)	0.53 (3.59)	0.40 (2.43)	0.31 (2.02)	0.21 (1.36)	0.17 (1.07)	0.15 (0.99)
27.27	1.30 (7.87)	0.93 (5.99)	0.56 (3.49)	0.43 (2.87)	0.33 (2.18)	0.23 (1.48)	0.17 (1.06)	0.16 (1.07)

Table 26. Effective Resolution (Peak-to-Peak Resolution) vs. Gain and Output Data Rate (Bits), Low Power Mode

Output Date Rate (SPS)	Gain = 1	Gain = 2	Gain = 4	Gain = 8	Gain = 16	Gain = 32	Gain = 64	Gain = 128
16.67	22.1 (19.4)	21.5 (18.8)	21.3 (18.6)	20.7 (18)	20.1 (17.5)	19.6 (17)	19 (16.4)	18.2 (15.5)
20	22 (19.3)	21.5 (18.8)	21.3 (18.5)	20.6 (17.9)	20 (17.4)	19.6 (17.1)	19 (16.4)	18 (15.5)
25	22 (19.2)	21.4 (18.8)	21.2 (18.4)	20.6 (18)	19.9 (17.2)	19.5 (16.8)	18.8 (16.2)	18 (15.3)
27.27	21.9 (19.3)	21.4 (18.7)	21.1 (18.5)	20.5 (17.7)	19.8 (17.1)	19.4 (16.7)	18.8 (16.2)	17.9 (15.2)

Fast Settling Filter ($Sinc^4$ + $Sinc^1$)

Table 27. RMS Noise (Peak-to-Peak Noise) vs. Gain and Output Data Rate (μV), Low Power Mode (Average by 16)

Filter Word (Dec.)	Output Date Rate (SPS)	Gain = 1	Gain = 2	Gain = 4	Gain = 8	Gain = 16	Gain = 32	Gain = 64	Gain = 128
96	3.57	0.41 (2.62)	0.27 (1.82)	0.17 (1.10)	0.12 (0.81)	0.094 (0.54)	0.066 (0.39)	0.050 (0.28)	0.044 (0.25)
30	11.43	0.69 (4.65)	0.49 (3.10)	0.29 (1.89)	0.21 (1.44)	0.17 (1.02)	0.11 (0.65)	0.090 (0.53)	0.082 (0.51)
6	57.14	1.49 (9.30)	1.07 (6.80)	0.65 (4.13)	0.49 (3.15)	0.38 (2.50)	0.26 (1.71)	0.20 (1.27)	0.18 (1.19)
5	68.57	1.62 (11)	1.16 (7.57)	0.71 (4.66)	0.53 (3.35)	0.41 (2.80)	0.28 (1.75)	0.22 (1.52)	0.20 (1.32)
2	171.43	2.57 (17)	1.86 (12)	1.11 (7.15)	0.85 (5.51)	0.67 (4.48)	0.44 (3.04)	0.35 (2.13)	0.33 (2.04)
1	342.86	3.59 (23)	2.64 (17)	1.60 (10)	1.20 (7.39)	0.94 (5.78)	0.64 (4.15)	0.50 (3.19)	0.45 (2.96)

Table 28. Effective Resolution (Peak-to-Peak Resolution) vs. Gain and Output Data Rate (Bits), Low Power Mode (Average by 16)

Filter Word (Dec.)	Output Date Rate (SPS)	Gain = 1	Gain = 2	Gain = 4	Gain = 8	Gain = 16	Gain = 32	Gain = 64	Gain = 128
96	3.57	23.5 (20.9)	23.1 (20.4)	22.8 (20.1)	22.3 (19.6)	21.7 (19.1)	21.2 (18.6)	20.6 (18.1)	19.7 (17.3)
30	11.43	22.8 (20)	22.3 (19.6)	22 (19.3)	21.5 (18.7)	20.8 (18.2)	20.4 (17.9)	19.7 (17.2)	18.9 (16.2)
6	57.14	21.7 (19)	21.2 (18.5)	20.9 (18.2)	20.3 (17.6)	19.7 (16.9)	19.2 (16.5)	18.6 (15.9)	17.7 (15)
5	68.57	21.6 (18.9)	21 (18.3)	20.7 (18)	20.2 (17.5)	19.5 (16.8)	19.1 (16.4)	18.4 (15.6)	17.6 (14.9)
2	171.43	20.9 (18.1)	20.4 (17.7)	20.1 (17.4)	19.5 (16.8)	18.8 (16.1)	18.4 (15.7)	17.8 (15.2)	16.9 (14.2)
1	342.86	20.4 (17.7)	19.9 (17.1)	19.6 (16.9)	19 (16.4)	18.3 (15.7)	17.9 (15.2)	17.3 (14.6)	16.4 (13.7)

RMS NOISE AND RESOLUTION (continued)

Fast Settling Filter ($Sinc^3$ + $Sinc^1$)

Table 29. RMS Noise (Peak-to-Peak Noise) vs. Gain and Output Data Rate (μV), Low Power Mode (Average by 16)

Filter Word (Dec.)	Output Date Rate (SPS)	Gain = 1	Gain = 2	Gain = 4	Gain = 8	Gain = 16	Gain = 32	Gain = 64	Gain = 128
96	3.57	0.40 (2.62)	0.28 (1.88)	0.17 (1.07)	0.12 (0.78)	0.096 (0.57)	0.065 (0.39)	0.050 (0.27)	0.046 (0.26)
30	11.43	0.69 (4.71)	0.49 (3.22)	0.29 (1.86)	0.22 (1.38)	0.17 (1.12)	0.12 (0.69)	0.092 (0.58)	0.082 (0.49)
6	57.14	1.51 (9.45)	1.08 (6.83)	0.65 (4.26)	0.49 (3.08)	0.38 (2.41)	0.26 (1.67)	0.20 (1.38)	0.19 (1.17)
5	68.57	1.64 (10)	1.16 (7.60)	0.71 (4.50)	0.52 (3.57)	0.41 (2.72)	0.28 (1.91)	0.22 (1.41)	0.21 (1.30)
2	171.43	2.62 (16)	1.88 (11)	1.15 (7.69)	0.85 (5.39)	0.64 (4.21)	0.45 (2.90)	0.35 (2.26)	0.32 (2.00)
1	342.86	5.10 (33)	3.21 (20)	1.88 (12)	1.32 (8.01)	0.97 (6.04)	0.65 (4.10)	0.51 (3.54)	0.46 (2.95)

Table 30. Effective Resolution (Peak-to-Peak Resolution) vs. Gain and Output Data Rate (Bits), Low Power Mode (Average by 16)

Filter Word (Dec.)	Output Date Rate (SPS)	Gain = 1	Gain = 2	Gain = 4	Gain = 8	Gain = 16	Gain = 32	Gain = 64	Gain = 128
96	3.57	23.6 (20.9)	23.1 (20.3)	22.8 (20.2)	22.3 (19.6)	21.6 (19.1)	21.2 (18.6)	20.6 (18.2)	19.7 (17.2)
30	11.43	22.8 (20)	22.3 (19.6)	22 (19.4)	21.4 (18.8)	20.8 (18.1)	20.4 (17.8)	19.7 (17)	18.9 (16.3)
6	57.14	21.7 (19)	21.1 (18.5)	20.9 (18.2)	20.3 (17.6)	19.6 (17)	19.2 (16.5)	18.6 (15.8)	17.7 (15)
5	68.57	21.5 (18.9)	21 (18.3)	20.7 (18.1)	20.2 (17.4)	19.5 (16.8)	19.1 (16.3)	18.4 (15.8)	17.5 (14.9)
2	171.43	20.9 (18.2)	20.3 (17.7)	20 (17.3)	19.5 (16.8)	18.9 (16.2)	18.4 (15.7)	17.8 (15.1)	16.9 (14.3)
1	342.86	19.9 (17.2)	19.6 (16.9)	19.3 (16.6)	18.8 (16.3)	18.3 (15.7)	17.9 (15.2)	17.2 (14.4)	16.4 (13.7)

TERMINOLOGY

AINP/AINM

AINP denotes the positive analog input, while AINM stands for the negative analog input.

Integral Nonlinearity (INL)

INL is the maximum code deviation from the transfer function's end-point straight line. Zero-scale lays 0.5LSB below the first code transition, full-scale 0.5LSB above the last transition. Error is given in full-scale range ppm.

Gain Error

Gain error is the offset of the final code transition from its ideal input voltage, valid for both unipolar and bipolar ranges.

It represents the ADC span error, covering full-scale deviations but excluding zero errors. For unipolar signals, it equals full-scale error minus offset error. For bipolar signals, it equals full-scale error minus bipolar zero error.

Offset Error

In unipolar mode, the offset error is the shift of the first code transition from the ideal AINP voltage (AINM + 0.5LSB).

In bipolar mode, it describes how the midscale transition (0111…111 to 1000…000) deviates from the ideal AINP voltage (AINM - 0.5LSB).

Offset Calibration Range

In system calibration modes, the SGM52421R8 series calibrates analog input offset. Its offset calibration range specifies the valid input voltage range for the accurate offset calibration.

Full-Scale Calibration Range

The full-scale calibration range defines the valid input voltage range for the accurate full-scale calibration of the SGM52421R8 series in system calibration mode.

Input Span

In system calibration, two sequential voltages applied to the analog input set the input range for the SGM52421R8 series. The input span defines the min/max zero-to-full-scale voltages for the accurate gain calibration.

DETAILED DESCRIPTION

Overview

The SGM52421R8/SGM52421R8A are low power Σ-Δ ADCs integrating a modulator, buffer, reference, gain stage and on-chip digital filter, designed for wide dynamic range low-frequency signal sensing in pressure transducers, weigh scales and temperature measurement.

Power Modes

The SGM52421R8/SGM52421R8A feature three power modes (high, mid, low) for flexible balancing of speed, RMS noise and supply current.

Analog Inputs

The SGM52421R8/SGM52421R8A support 8 differential or 15 pseudo-differential analog inputs, which can be buffered or unbuffered. Its flexible multiplexer allows any pin to serve as AINP or AINM.

Multiplexer

The integrated multiplexer expands channel count and synchronizes channel switching with conversions.

Reference

The SGM52421R8/SGM52421R8A integrate a 2.5V reference (maximum 15ppm/℃ drift) and on-chip reference buffers for internal or external use.

Programmable Gain Array (PGA)

The SGM52421R8/SGM52421R8A's PGA amplifies analog input signals with the selectable gains (1, 2, 4, 8, 16, 32, 64, 128).

Burnout Currents

The chip integrates two programmable burnout currents (programmed to 500nA, 2μA, or 4μA) for external sensor presence detection.

Σ-Δ ADC and Filter

The SGM52421R8/SGM52421R8A integrate a 4th-order Σ-Δ modulator with a digital filter, offering filter options: $sinc^4$, $sinc^3$, fast filter, post filter and zero latency.

Channel Sequencer

The SGM52421R8/SGM52421R8A support up to 16 configurable channels for analog, reference or supply inputs, enabling diagnostics like supply monitoring to interleave with conversions. Its sequencer auto-scans enabled channels, with the conversion time matching channel settling time.

Per Channel Configuration

The SGM52421R8/SGM52421R8A support up to 8 setups, each defining gain, ODR, filter type and reference source, with channels assignable to individual setups.

Serial Interface

The SGM52421R8/SGM52421R8A support 3-wire or 4-wire SPI for accessing its on-chip registers.

Clock

The SGM52421R8/SGM52421R8A include a 614.4kHz internal clock, selectable over an external clock, and can output this clock externally for other circuits.

Temperature Sensor

The on-chip temperature sensor monitors the die temperature.

Digital Outputs

The SGM52421R8/SGM52421R8A feature four general-purpose digital outputs to drive external circuits, such as external multiplexers.

Calibration

The SGM52421R8/SGM52421R8A integrate the internal and system calibration, enabling offset and gain error correction for the device or full system.

Excitation Currents

The SGM52421R8/SGM52421R8A have two independently adjustable excitation currents with levels from 50μA to 1.5mA.

Bias Voltage

The SGM52421R8/SGM52421R8A integrate a bias generator set to $(AV_{DD} - AV_{SS})/2$ for thermocouple biasing, routable to any input and supporting multiple channels.

Bridge Power Switch (PSW)

A low-side power switch allows the user to power down bridges that are interfaced to the ADC.

Diagnostics

The SGM52421R8/SGM52421R8A provide rich diagnostics including reference, over-/under-voltage detection, SPI CRC, memory CRC and read/write checks, ensuring high fault coverage.

DETAILED DESCRIPTION (continued)

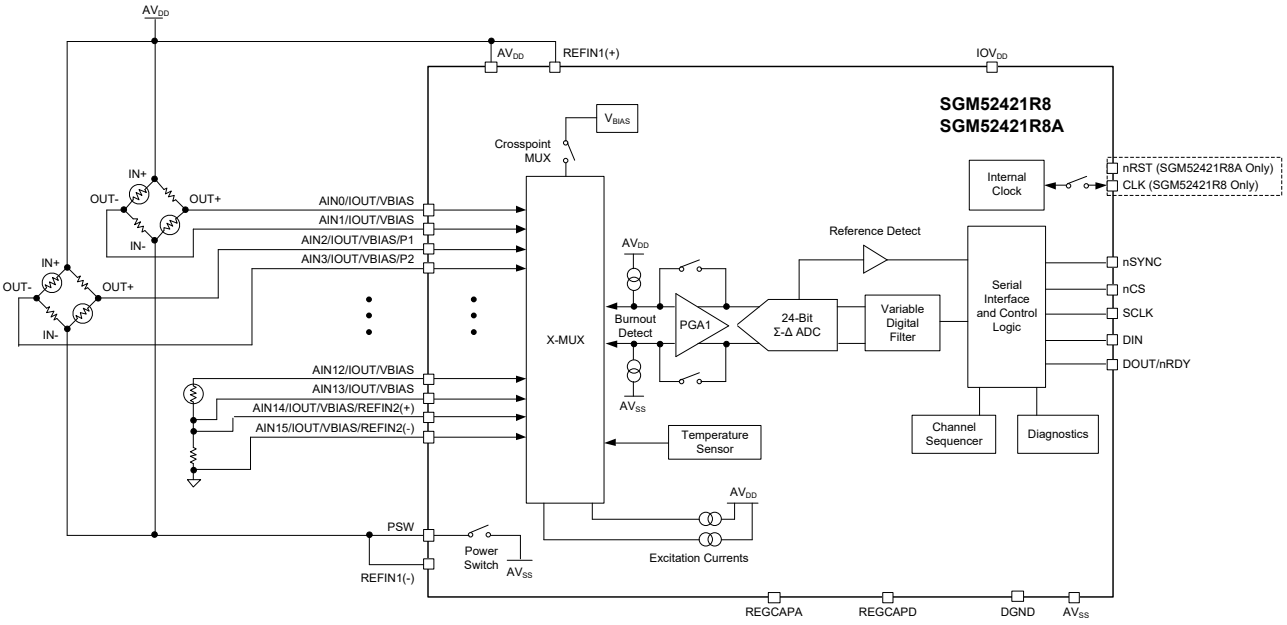


Figure 8. Basic Connection Diagram

Power Supplies

The SGM52421R8/SGM52421R8A support analog supply of 2.7V to 3.6V across all power modes, and the digital supply range is 1.8V to 3.6V. It features two separate power pins: AV_{DD} and IOV_{DD}. Referenced to AV_{SS}, AV_{DD} feeds the analog regulator for the ADC. Referenced to DGND, IOV_{DD} defines SPI logic levels and supplies power for the digital circuits.

Single Supply Operation (AV_{SS} = DGND)

For single supply operation on AV_{DD}, AV_{SS} and DGND may share a common ground plane. The external level shifting is needed for true bipolar inputs to adjust common mode voltage.

Split Supply Operation (AV_{SS} ≠ DGND)

The SGM52421R8/SGM52421R8A support negative AV_{SS} for true bipolar inputs. Fully differential 0V-centered signals work without external level shifting. For a 3.6V split supply, AV_{DD} = +1.8V and AV_{SS} = -1.8V. The internal shifting keeps digital outputs between DGND and IOV_{DD}.

Follow absolute maximum ratings for split AV_{DD}/AV_{SS} operation, and keep IOV_{DD} below 3.6V.

Digital Communication

The SGM52421R8/SGM52421R8A feature 3/4-wire SPI interfaces, compatible with QSPI, MICROWIRE and DSPs. It runs in SPI Mode 3 with nCS held low. The SCLK stays high at idle: data outputs on its falling edge, and inputs on the rising edge.

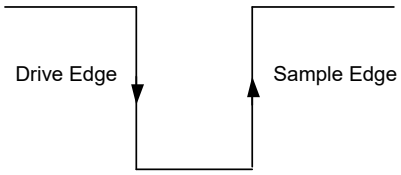


Figure 9. SPI Mode 3, SCLK Edges

Accessing the ADC Register Map

This 8-bit write-only communications register governs access to all ADC registers. The interface defaults to waiting for its write upon power-up or reset, so all communications start here.

Its bits 0-5 define the target register and the bit 6 selects the read/write action. After each register access, the interface reverts to the initial state.

To restore synchronization: apply 64+ high DIN clock cycles for full device reset, or pull nCS high to reset the interface and halt ongoing operations.

Figure 10 and Figure 11 show the register read/write sequences: send an 8-bit command to the communications register first, and then transmit register data.

Reading the read-only ID register (value 0x18) is recommended to verify communication. Refer to Table 31 and Table 32 for more details on two registers.

DETAILED DESCRIPTION (continued)

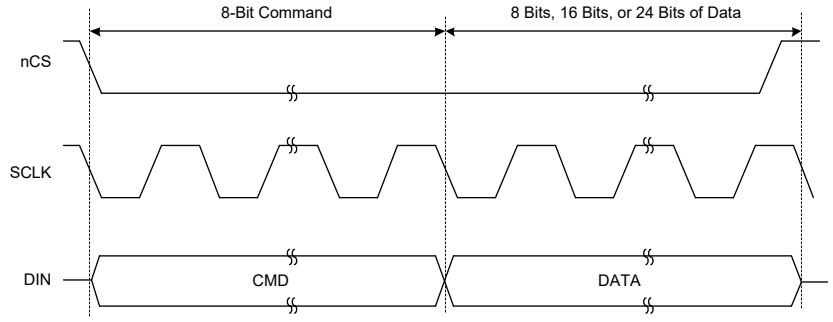


Figure 10. Register Write Sequence (Send 8-Bit Command with Address, then 8/16/24-Bit Data Varying by Register)

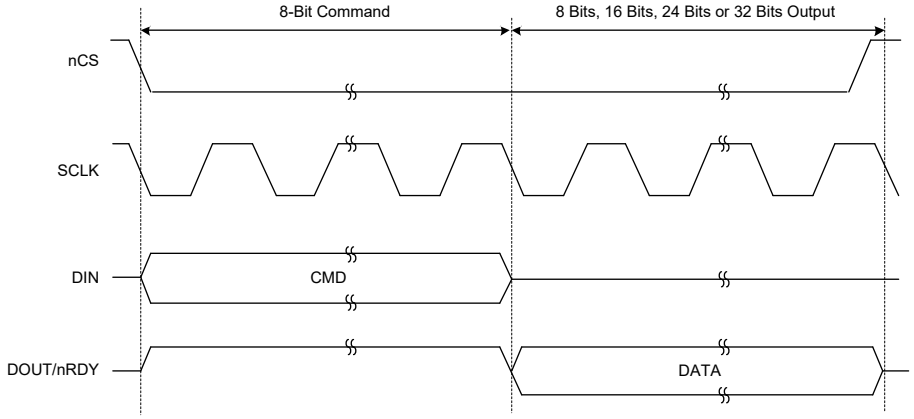


Figure 11. Register Read Sequence (Transmit 8-Bit Address Command, then Receive 8/16/24/32-Bit DOUT Data Based on Register, CRC is Enabled)

Table 31. Communications Register

Addr.	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	R/W
0x00	Communications	[7:0]	nWEN	R/$\overline{W}$	RS[5:0]						0x00	W

Table 32. ID Register

Addr.	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	R/W
0x05	ID	[7:0]	DEVICE_ID[3:0]				SILICON_REVISION[3:0]				0x18	R

DETAILED DESCRIPTION (continued)

Configuration Overview

After power-up or reset, the device uses default settings: Channel 0 is active with AIN0/AIN1 as differential inputs and Setup 0 applied. Input/reference buffers are off, gain is 1, and external reference is used. It runs in low power continuous conversion mode with internal oscillator as main clock, and only SPI_IGNORE_ERR diagnostic function is enabled.

This is a partial setting list, refer to Registers Maps section for more details. Figure 12 presents a four-step ADC configuration flow: channel setup (Box A), parameter setup (Box B), diagnostics (Box C) and ADC control (Box D).

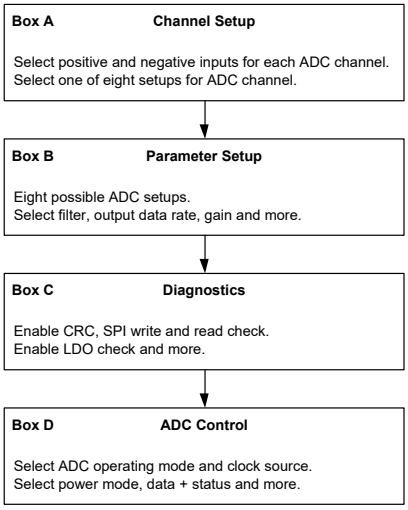


Figure 12. Recommended ADC Configuration Flow

Channel Configuration

The device provides 16 analog input channels and 8 independent setups. Users may assign any input pair and setup to each channel for flexible, per-channel differential configuration. Power and reference signals can also be selected as inputs via internal multiplexer. Up to 16 ADC configurations are supported, enabling interleaved conversion and diagnostics.

Channel Registers

The channel registers set each channel's positive/negative analog inputs, enable status and assigned setup. With the multiple channels active, the sequencer scans enabled channels from 0 to 15 and skips disabled ones. See Table 33 for channel 0 register details.

ADC Setups

Eight independent setups are available, each containing configuration, filter, gain and offset registers. As shown in Figure 13, each setup group corresponds to the numbered registers. Setups are selected via channel registers, enabling independent configuration per channel. Table 34 to Table 37 list Setup 0 registers, and the same structure applies to Setup 1 through 7.

Table 33. Channel 0 Register

Addr.	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	R/W
0x09	CHANNEL_0	[15:8]	Enable	Setup[2:0]			0		AINP[4:3]		0x8001	R/W
		[7:0]	AINP[2:0]			AINM[4:0]						

Table 34. Configuration 0 Register

Addr.	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	R/W
0x19	CONFIG_0	[15:8]	0				Bipolar	Burnout[1:0]		REF_BUFP	0x0860	R/W
		[7:0]	REF_BUFM	AIN_BUFP	AIN_BUFM	REF_SEL[1:0]		PGA[2:0]				

Table 35. Filter 0 Register

Addr.	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	R/W
0x21	FILTER_0	[23:9]	Filter[2:0]			REJ60	POST_FILTER[2:0]			SINGLE_CYCLE	0x060180	R/W
		[15:8]	0					FS[10:8]				
		[7:0]	FS[7:0]									

Table 36. Offset 0 Register

Addr.	Name	Bits	Bits[23:0]	Reset	R/W
0x29	OFFSET_0	[23:0]	Offset[23:0]	0x800000	R/W

Table 37. Gain 0 Register

Addr.	Name	Bits	Bits[23:0]	Reset	R/W
0x31	GAIN_0	[23:0]	Gain[23:0]	0x555555	R/W

DETAILED DESCRIPTION (continued)

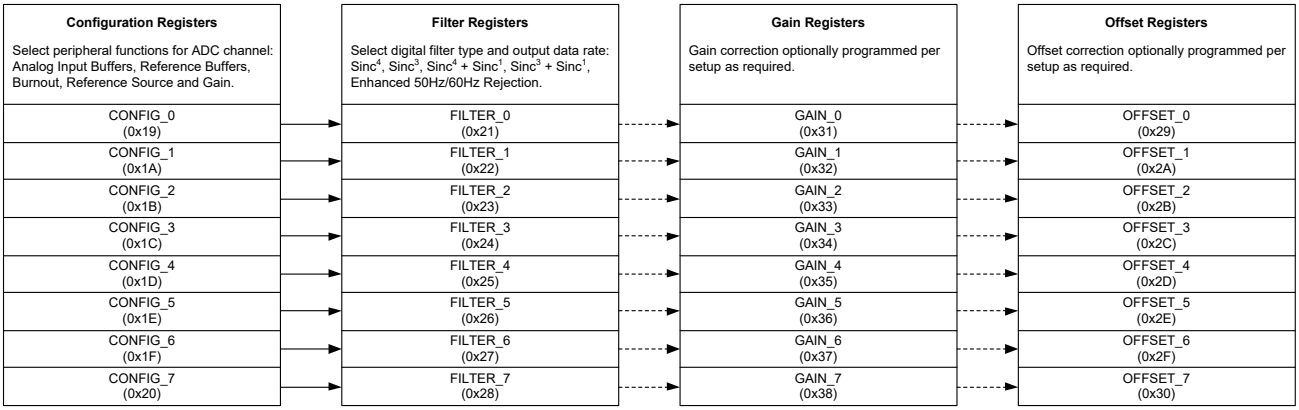


Figure 13. ADC Setup Register Grouping

Configuration Registers

Configuration registers set ADC output coding (bipolar offset binary for negative inputs, unipolar straight binary for positive inputs only). The inputs must stay within AV_{DD} - AV_{SS} range.

They also select reference sources (internal 2.5V, two external reference ports or AV_{DD} - AV_{SS}), set PGA gain (1/2/4/8/16/32/64/128) and enable analog & reference buffers.

Filter Registers

Filter registers configure the ADC modulator's digital filter type and output data rate. Refer to the Digital Filter section for more details.

Gain Registers

These 24-bit read/write gain registers store ADC gain calibration coefficients. Factory-calibrated for gain = 1 with device-specific default values, which get overwritten after full-scale calibration. See the Calibration section for more details.

Offset Registers

These 24-bit read/write offset registers store ADC offset calibration data, with a default reset value of 0x800000. This value will be overwritten by user writes or zero-scale calibration.

Diagnostics

The ERROR_EN register toggles device diagnostics. The SPI_IGNORE function is enabled by default to flag improper write timing. Other functions cover SPI access, SCLK count, CRC and LDO monitoring.

Enabled diagnostics set corresponding error flags, which collectively trigger the status *_ERR bits. Check the error register for fault details. The MCLK_COUNT register tracks the internal oscillator frequency. Refer to Table 38 to Table 40 and Diagnostics section for full register information.

ADC Control Register

The ADC control register sets power modes, conversion modes, standby, power-down and calibration functions. It also selects clock source and enables the internal reference. Reference options are defined in setup registers.

It configures digital interface features including status-attached data read and continuous read. See Table 41 and the Digital Interface section for more details.

Table 38. Error Register

Addr.	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	R/W
0x06	Error	[23:16]	0					ADC_CAL_ERR	ADC_CONV_ERR	ADC_SAT_ERR	0x000000	R
		[15:8]	AINP_OV_ERR	AINP_UV_ERR	AINM_OV_ERR	AINM_UV_ERR	REF_DET_ERR	0	DLDO_PSM_ERR	0		
		[7:0]	ALDO_PSM_ERR	SPI_IGNORE_ERR	SPI_SCLK_CNT_ERR	SPI_READ_ERR	SPI_WRITE_ERR	SPI_CRC_ERR	MM_CRC_ERR	ROM_CRC_ERR		

DETAILED DESCRIPTION (continued)

Table 39. Error Enable Register

Addr.	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	R/W
0x07	ERROR_EN	[23:16]	0	MCLK_CNT_EN	0			ADC_CAL_ERR_EN	ADC_CONV_ERR_EN	ADC_SAT_ERR_EN	0x000040	R/W
		[15:8]	AINP_OV_ERR_EN	AINP_UV_ERR_EN	AINM_OV_ERR_EN	AINM_UV_ERR_EN	REF_DET_ERR_EN	DLDO_PSM_TRIP_TEST_EN	DLDO_PSM_ERR_EN	ALDO_PSM_TRIP_TEST_EN		
		[7:0]	ALDO_PSM_ERR_EN	SPI_IGNORE_ERR_EN	SPI_SCLK_CNT_ERR_EN	SPI_READ_ERR_EN	SPI_WRITE_ERR_EN	SPI_CRC_ERR_EN	MM_CRC_ERR_EN	ROM_CRC_ERR_EN		

Table 40. MCLK Count Register

Addr.	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	R/W
0x08	MCLK_COUNT	[7:0]	MCLK_COUNT[7:0]								0x00	R

Table 41. ADC Control Register

Addr.	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	R/W
0x01	ADC_CONTROL	[15:8]	0			DOUT_nRDY_DEL	CONT_READ	DATA_STATUS	nCS_EN	REF_EN	0x0000	R/W
		[7:0]	POWER_MODE[1:0]		Mode[3:0]				CLK_SEL[1:0]			

Understanding Configuration Flexibility

Figure 14 to Figure 16 mark the configured registers in black and the redundant registers in gray.

A common application uses the adjacent differential analog inputs sharing identical setup, gain and offset settings. For four differential channels, use AIN0/AIN1, AIN2/AIN3, AIN4/AIN5 and AIN6/AIN7.

Gain and offset registers programming is optional, as marked by dashed lines. Offset and full-scale calibrations will automatically update these registers for selected channels.

The eight setups support separate configurations for the four differential inputs, to meet different speed, noise, gain and offset demands. Figure 15 illustrates this flexible per-channel setup.

Figure 16 illustrates the channel routing from analog inputs to setup configurations. This example uses two differential and two single-ended inputs (AIN0/AIN7, AIN6/AIN7 for single-ended).

AIN0/AIN1 uses Setup 0, the two single-ended diagnostic inputs use Setup 1, and AIN2/AIN3 uses Setup 2. Corresponding CONFIG_x and FILTER_x registers for the three setups are configured, with per-setup gain and offset adjustment available optionally.

CHANNEL_0 to CHANNEL_3 are enabled via their MSB bits. The device sequencer scans these channels in ascending order and cycles repeatedly during conversion.

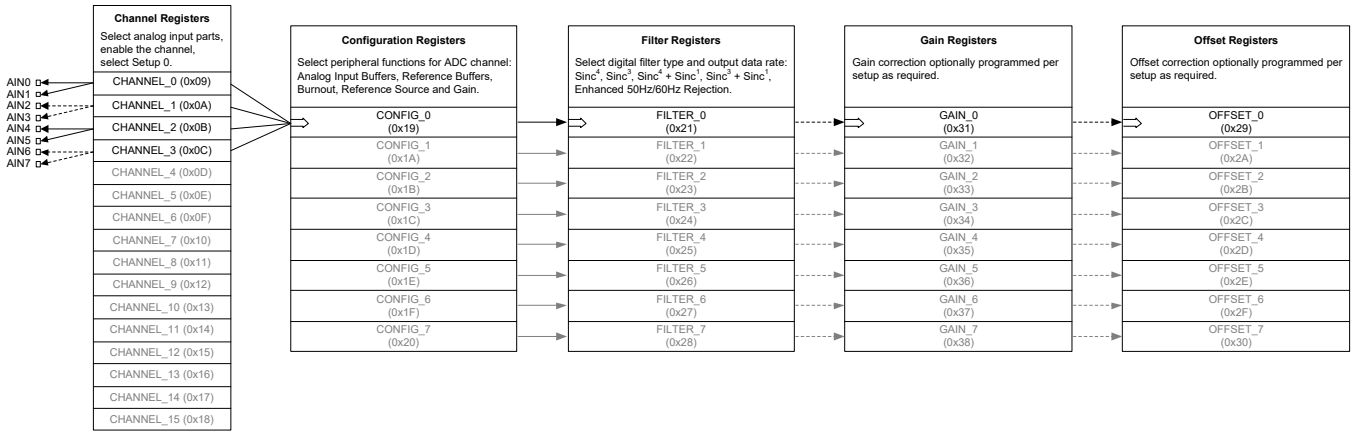


Figure 14. Four Fully Differential Inputs Sharing One Setup (CONFIG_0, FILTER_0, GAIN_0, OFFSET_0)

DETAILED DESCRIPTION (continued)

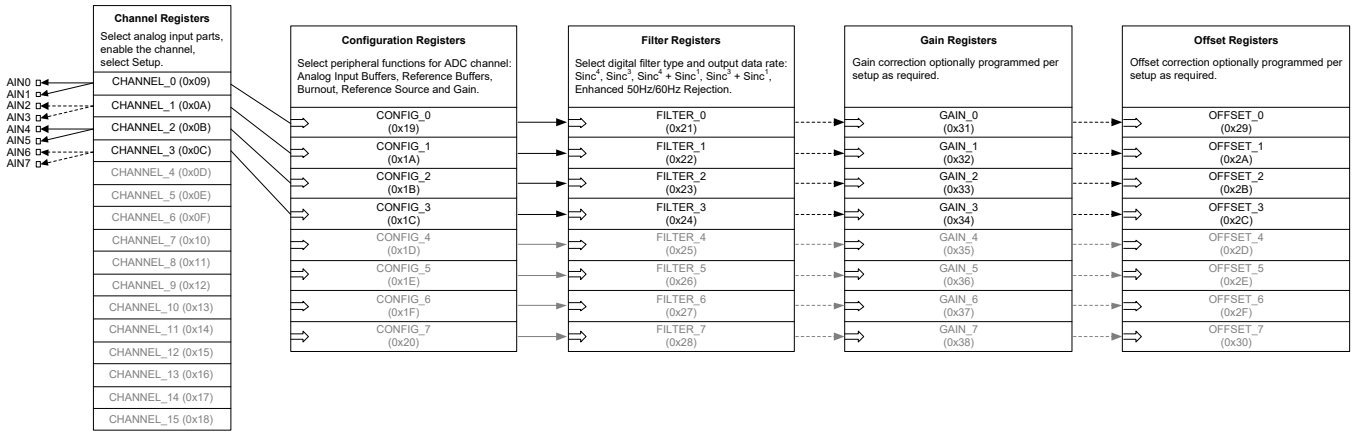


Figure 15. Four Fully Differential Inputs, Each Assigned an Independent Setup

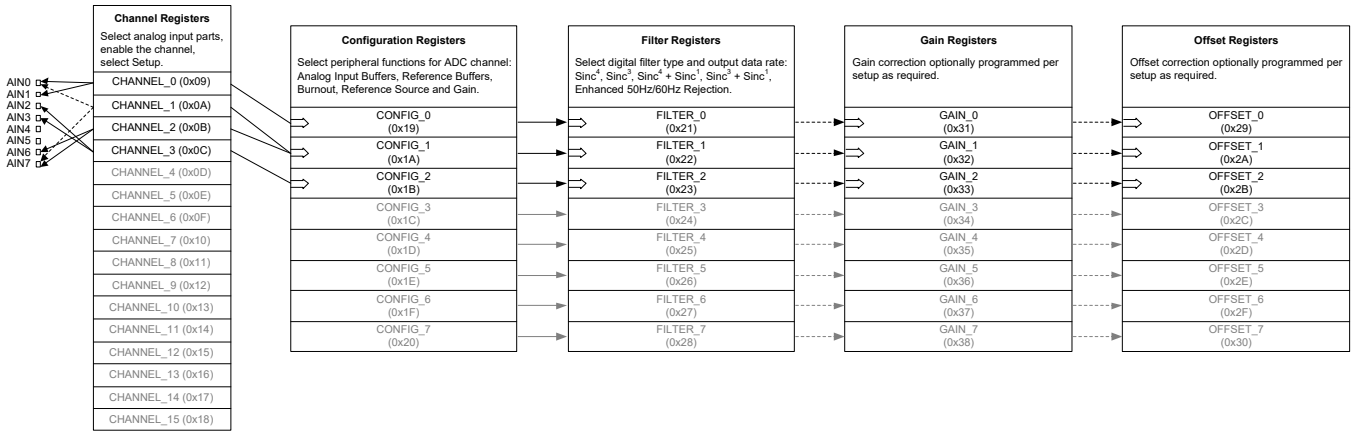


Figure 16. Mixed Differential and Single-Ended Inputs Configured with Multiple Shared Setups

DETAILED DESCRIPTION (continued)

Analog Input Channel

The device features flexible multiplexing, letting AIN0 - AIN15 serve as positive or negative inputs. This supports pin connection diagnostics and simplifies PCB design, compatible with 2/3/4-wire RTD (resistance temperature detector) circuits.

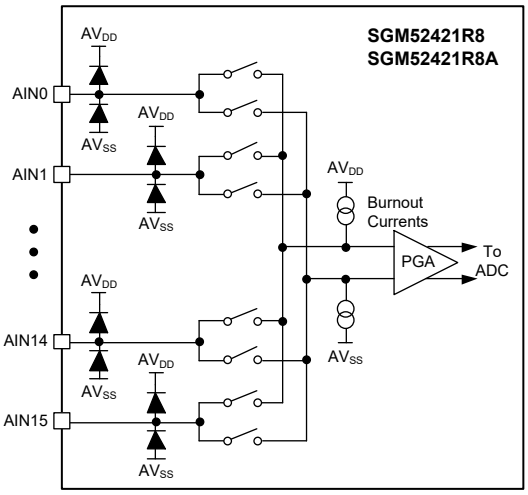


Figure 17. Analog Input Multiplexer Circuit

The channel registers use AINP[4:0] and AINM[4:0] bits (Table 42) for channel setup, supporting 8 differential, 15 pseudo-differential or mixed inputs. The adjacent pins are recommended for differential pairs to reduce mismatch.

At gain = 1, input buffers are configurable via AIN_BUFP and AIN_BUFM bits (Table 43). Buffers activate automatically when gain > 1.

• Buffered mode: High input impedance, suitable for strain gauges, RTDs. Input range: AV_{SS} + 100mV to AV_{DD} - 100mV.

• Unbuffered mode: Higher input current, prone to gain errors with RC networks. Input range: AV_{SS} - 50mV to AV_{DD} + 50mV.

With gain > 1, the rail-to-rail PGA works with auto-enabled buffers, and input range extends to AV_{SS} - 50mV to AV_{DD} + 50mV. Exceeding voltage limits impairs linearity and noise performance.

Programmable Gain Array (PGA)

The multiplexer output feeds the PGA when the gain stage is enabled. The on-chip PGA amplifies low-amplitude signals while preserving good noise performance.

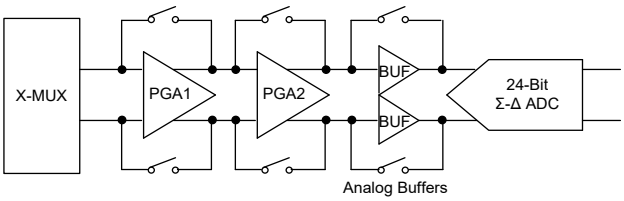


Figure 18. PGA

The PGA gain (1/2/4/8/16/32/64/128) is set via the configuration register bits (Table 43). It has two stages: gain = 1 bypasses both; gains = 2 to 8 use one stage; gain above 8 uses two stages.

Input range = $\pm V_{REF}$/gain. With 2.5V external reference, the unipolar range is 0V to 2.5V, the bipolar is ±2.5V (minimum span ±19.53mV at maximum gain). When V_{REF} equals AV_{DD}, the input range needs restriction. Refer to Electrical Characteristics for more details.

Reference

The device integrates a low noise 2.5V internal reference with maximum drift of 15ppm/°C. It cuts external components and PCB area, ideal for thermocouple and similar applications.

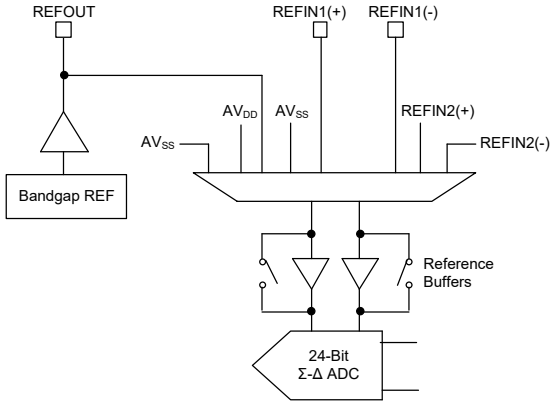


Figure 19. Reference Connections

Table 42. Channel Registers

Addr.	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	R/W
0x09 to 0x18	CHANNEL_0 to CHANNEL_15	[15:8]	Enable	Setup[2:0]			0		AINP[4:3]		0x8001 (1)	R/W
		[7:0]	AINP[2:0]			AINM[4:0]						

NOTE: 1. The CHANNEL_0 register is reset to 0x8001. All the other channels are reset to 0x0001.

Table 43. Configuration Registers

Addr.	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	R/W
0x19 to 0x20	CONFIG_0 to CONFIG_7	[15:8]	0				Bipolar	Burnout[1:0]		REF_BUFP	0x0860	R/W
		[7:0]	REF_BUFM	AIN_BUFP	AIN_BUFM	REF_SEL[1:0]		PGA[2:0]				

DETAILED DESCRIPTION (continued)

Enable the internal 2.5V reference via the REF_EN bit of the ADC_CONTROL register, or select the external reference REFIN1/REFIN2 through the REF_SEL[1:0] bits in the configuration register (Table 43). The internal reference can output via REFOUT pin, requiring a 1μF decoupling capacitor.

• Unbuffered reference inputs: the common mode range is AV_{SS} - 50mV ~ AV_{DD} + 50mV.
• Buffered reference inputs: 100mV headroom required.
• Supported reference voltage: 0.5V to AV_{DD} (nominal 2.5V).

Ratiometric designs suppress low-frequency excitation noise. Non-ratiometric circuits need a low noise reference. The unbuffered reference pins have the dynamic high impedance, and RC networks may cause DC gain errors. Use on-chip reference buffers when the reference source has high output impedance.

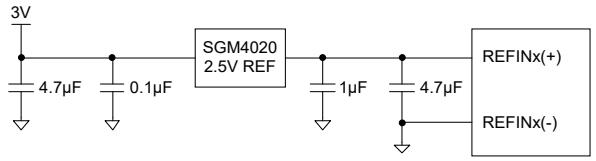


Figure 20. Reference Voltage Wiring for SGM52421R8/SGM52421R8A

Bipolar/Unipolar Configuration

The ADC supports unipolar and bipolar input ranges to match sensor outputs.

With split supplies, the true bipolar inputs are available. For single supplies, the bipolar mode does not allow voltages below AV_{SS}. Inputs are referenced to AINM.

Example (V_{REF} = AV_{DD} = 3V, gain = 1):
• Unipolar (AINM = 1.5V): AINP ranges: 1.5V to 3V.
• Bipolar: AINP ranges: 0V to AV_{DD}.

Set the Bipolar bit in the configuration register to select the mode.

Data Output Coding

In unipolar ADC mode, the outputs use straight binary. Zero differential input gives all 0s, midscale yields 100 ... 000, and full-scale produces all 1s. Analog inputs correspond to such binary codes.

$$Code = (2^N \times A_{IN} \times Gain)/V_{REF} \quad (1)$$

In bipolar ADC mode, the outputs adopt offset binary. Negative full-scale outputs all 0s, zero differential input gives 100 ... 000, and the positive full-scale generates all 1s for analog inputs.

$$Code = 2^{N-1} \times [(A_{IN} \times Gain/V_{REF}) + 1] \quad (2)$$

where:
N = 24.
A_{IN} = Analog input voltage.
Gain = Gain setting (1 to 128).

Excitation Currents

The SGM52421R8/SGM52421R8A integrate two matched software-configurable constant current sources, selectable at 50μA, 100μA, 250μA, 500μA, 750μA, 1mA or 1.5mA. They excite the external resistive bridges and RTD sensors, sourcing current from AV_{DD} to any analog input pin.

The IOUT1_CH[3:0] and IOUT0_CH[3:0] bits in the IO_CONTROL_1 register set the target pins, while the IOUT1/IOUT0 adjust the current levels independently. Both outputs can feed one shared pin. The internal reference is not required for these excitation currents.

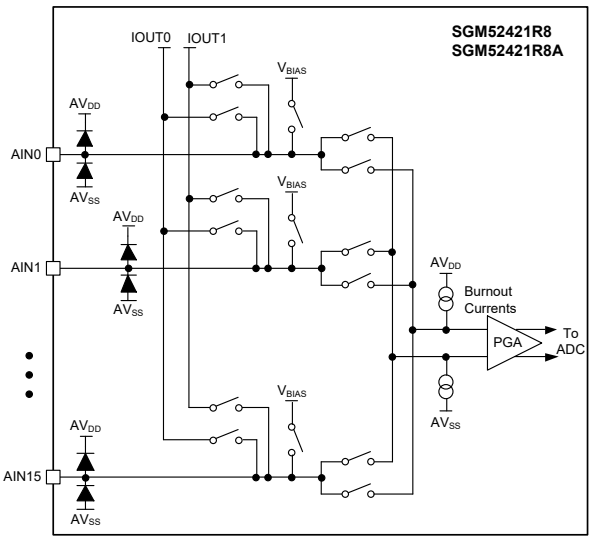


Figure 21. Excitation Current and Bias Voltage Connections

Bridge Power-Down Switch

The bridge circuits like strain gages and load cells draw most system current. A 350Ω load cell needs 8.6mA under 3V supply. The bridge power-down switch cuts the power to save the current during idle time. This switch supports up to 30mA continuous current with maximum 10Ω on-resistance, controlled by the PDSW bit in the IO_CONTROL_1 register.

Logic Outputs

The SGM52421R8/SGM52421R8A feature four general-purpose digital outputs P1-P4. The GPIO_CTRLx bits in the IO_CONTROL_1 register enable them, while the GPIO_DATx bits set the pin high/low states. Their logic levels follow AV_{DD} instead of IOV_{DD}. Refer to Table 44 for more details.

DETAILED DESCRIPTION (continued)

These pins can drive external circuits like multiplexers to expand channels. They select active multiplexer pins. Since the multiplexer works independently, reset the modulator and filter via nSYNC or register writes after each channel switch.

Bias Voltage Generator

The SGM52421R8/SGM52421R8A integrate an on-chip bias voltage generator. It sets the selected input pins to half the voltage between AV_{DD} and AV_{SS}. This function suits the single supply ADC thermocouple operations by providing required DC biasing. Enabled via the VBIASx bits in the IO_CONTROL_2 register, its startup time varies with load capacitance. The detailed parameters are listed in the Electrical Characteristics section.

Clock

The SGM52421R8/SGM52421R8A integrate a 614.4kHz on-chip clock with ±1.2% tolerance. Clock source is chosen via the CLK_SEL[1:0] bits in the ADC_CONTROL register.

The internal clock can output through the CLK pin for multi-ADC synchronization. One chip's clock can drive all devices, which may be synchronized via the shared reset or nSYNC pulses.

Power Modes

The SGM52421R8/SGM52421R8A offer three power modes selected via the POWER_MODE[1:0] bits in ADC_CONTROL register. They adjust the power consumption and the clock frequency by dividing the 614.4kHz internal clock with different ratios, further changing data rate and device performance. Refer to Table 45 for more details.

Standby and Power-Down Modes

Standby mode powers down most modules, while LDOs stay on to retain register data. Enabled reference, oscillator, P1-P4 outputs, bias generator, power switch and excitation currents keep working and can be turned off via the relevant bits. Reference detection is disabled here, while the other diagnostics stay active if previously enabled.

Clock-dependent diagnostics only work in conversion or idle mode, not standby. Typical standby current is 25μA with only LDOs active; it rises by 49μA with the bias generator.

Exiting standby takes 130 MCLK cycles. If the internal oscillator is enabled, it will be disabled upon entering standby and re-enabled after exiting standby, with an additional 40μs stabilization time required. For the external clock, ensure it runs before waking the device, and avoid writing to ADC_CONTROL register until full settlement. Refer to Table 46 and Table 47 for more details.

Power-down mode shuts down all circuits including LDOs. Registers lose data and P1-P4 enter tri-state. The device must enter standby first to avoid unintended power-down. Keep external clock active during this transition.

Wake-up needs 64 SCLK cycles with nCS low and DIN high for serial reset. Typical startup settling time is 2ms before register access, and the typical power-down current is 0.5μA.

Table 44. Input/Output Control 1 Register

Addr.	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	R/W
0x03	IO_CONTROL_1	[23:16]	GPIO_DAT4	GPIO_DAT3	GPIO_DAT2	GPIO_DAT1	GPIO_CTRL4	GPIO_CTRL3	GPIO_CTRL2	GPIO_CTRL1	0x000000	R/W
		[15:8]	PDSW	0	IOUT1[2:0]			IOUT0[2:0]				
		[7:0]	IOUT1_CH[3:0]				IOUT0_CH[3:0]					

Table 45. Power Modes

Power Mode	Master Clock (kHz)	Output Data Rate (1) (SPS)	Current
Full Power	614.4	9.37 to 19200	See the Electrical Characteristics section
Mid Power	153.6	2.34 to 4800	
Low Power	76.8	1.17 to 2400	

NOTE: 1. Unsettled, using a $sinc^3$/$sinc^4$ filter.

Table 46. Input/Output Control 2 Register

Addr.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	R/W
0x04	IO_CONTROL_2	VBIAS15	VBIAS14	VBIAS13	VBIAS12	VBIAS11	VBIAS10	VBIAS9	VBIAS8	0x0000	R/W
		VBIAS7	VBIAS6	VBIAS5	VBIAS4	VBIAS3	VBIAS2	VBIAS1	VBIAS0		

Table 47. ADC Control Register

Addr.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	R/W
0x01	ADC_CONTROL	0			DOUT_nRDY_DEL	CONT_READ	DATA_STATUS	nCS_EN	REF_EN	0x0000	R/W
		POWER_MODE[1:0]		Mode[3:0]				CLK_SEL[1:0]			

DETAILED DESCRIPTION (continued)

Digital Interface

The chip's programmable features are managed via on-chip registers accessed through its serial interface. All transactions start with writing the communications register, which defines subsequent read/write targets. Write operations follow with register data; standard reads also begin with this setup (excluding continuous read mode).

The interface uses four pins: nCS, DIN, SCLK and DOUT/nRDY. The DIN inputs data while DOUT/nRDY outputs data and acts as a ready flag. The SCLK synchronizes all transfers, and the nCS selects the device. Relevant read/write timings and inter-operation delays are shown in related figures. The same data can be read multiple times in normal mode, while the continuous read allows only one access per update.

Tying nCS low enables 3-wire operation, which is suitable for MCU connection with SCLK recommended to idle high. nCS can also serve as frame synchronization for DSP interfaces. When certain SPI error diagnostics are enabled, nCS framing and the nCS_EN bit are mandatory.

A stream of logic 1s on DIN resets the serial interface to its initial state. The ADC supports single and continuous conversion modes.

Single Conversion Mode

In single conversion mode, the device enters standby after one conversion. With an active clock, DOUT/nRDY drops low to signal completion and rises after data read; the repeated reads are allowed even when it is high. Avoid accessing ADC_CONTROL register near the end of conversion, as the Mode[3:0] bits update for the standby state.

For multiple enabled channels, the ADC scans them sequentially. The DOUT/nRDY stays high during conversion and goes low when the data is ready, then the next channel starts sampling. Read current data promptly before the register updates. The chip enters standby after all channels finish conversion.

Setting the DATA_STATUS bit outputs status register alongside conversion data, with its four LSBs marking the corresponding channel.

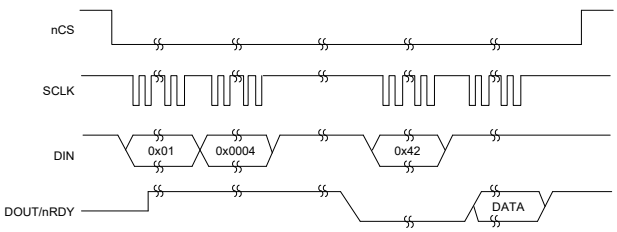


Figure 22. Single Conversion Configuration

Continuous Conversion Mode

The continuous conversion is the default startup mode. The ADC runs conversions nonstop, with nRDY and DOUT/nRDY (when nCS is low) pulling low upon completion. Read data via the communications register; the repeated reads are allowed, but avoid access right before new data updates to prevent data loss.

With multiple enabled channels, the ADC scans them from low to high repeatedly. DOUT/nRDY pulses low for each finished conversion, and the data can be read during the next conversion. Setting the DATA_STATUS bit outputs status register with conversion data to identify the active channel.

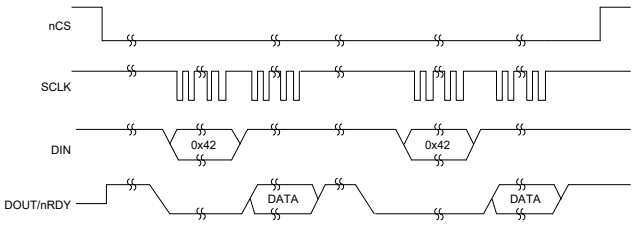


Figure 23. Continuous Conversion Configuration

Continuous Read Mode

The continuous read mode skips prior communications register writes. After DOUT/nRDY goes low, send SCLKs to read data; the pin rises afterward. Each dataset can only be read once, so the complete reading finishes before the next conversion. Unread data will be overwritten. This mode can only be enabled in continuous mode.

Set the CONT_READ bit to activate it, where only data register reads are allowed. Exit via command 0x42 (when DOUT/nRDY is low) or software reset. Keep DIN low normally in this mode.

For multiple channels, data outputs sequentially. The DATA_STATUS bit enabled appends the status bits to mark the corresponding channel.

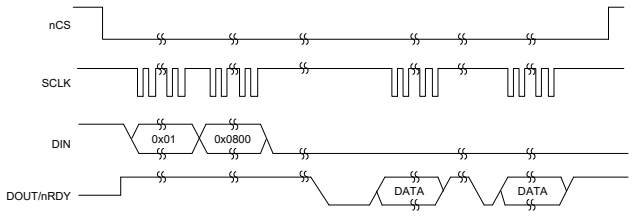


Figure 24. Continuous Read Configuration

DETAILED DESCRIPTION (continued)

Data_Status

The device can append the status register data to the conversion results, making it ideal for multi-channel applications. Its four LSBs identify the active channel, and the ERROR_FLAG bit reports faults. Enable this function by setting the DATA_STATUS bit in the ADC_CONTROL register.

Serial Interface Reset (DOUT_nRDY_DEL and nCS_EN Bits)

The DOUT/nRDY pin switching timing is configurable. By default, it changes role at least 10ns after the final SCLK rising edge. Setting the DOUT_nRDY_DEL bit extends this delay to minimum 110ns.

Setting nCS_EN bit to high keeps the DOUT/nRDY outputting data until the nCS goes high, which is suitable for nCS-framed reads. Otherwise, set it low to switch pin function after the last SCLK edge. This bit must be high with nCS framing all transactions when the SPI error diagnostics are enabled.

The serial interface resets on nCS rising edge, waiting for communications register writes. Keep nCS low throughout multi-byte transfers.

Reset

Write 64 consecutive logic 1s to reset the chip circuits and serial interface. It restores logic, filters, modulator and all registers to defaults. Power-up triggers automatic reset, which takes 90 MCLK cycles. This operation fixes interface faults caused by SCLK noise. In addition, the SGM52421R8A has a dedicated physical nRST pin to fully reset the chip, which is the key difference from the SGM52421R8.

Calibration

The device offers four calibration modes to correct offset and gain errors: internal zero-scale, internal full-scale, system zero-scale and system full-scale. Only one channel works during calibration. Conversion results are adjusted via the calibration registers before storage.

The offset register defaults to 0x800000, and the gain register uses a nominal value of 0x555555. Gain calibration ranges from 0.4 × V_{REF}/gain to 1.05 × V_{REF}/gain. Relevant formulas apply to the ideal unipolar operation.

$$Data = \left(\frac{0.75 \times V_{IN}}{V_{REF}} \times 2^{23} - (Offset - 0x800000) \right) \times \frac{Gain}{0x400000} \times 2 \quad (3)$$

This formula represents the ideal conversion relationship for bipolar mode, excluding ADC gain and offset errors.

$$Data = \left(\frac{0.75 \times V_{IN}}{V_{REF}} \times 2^{23} - (Offset - 0x800000) \right) \times \frac{Gain}{0x400000} + 0x800000 \quad (4)$$

Start calibration by configuring Mode[3:0] bits in the ADC_CONTROL register. The DOUT/nRDY and nRDY go high during calibration, then restore and the chip enters idle mode upon completion, with the related calibration registers updated.

For the internal offset calibration, the positive and negative input pins are internally short-circuited. It is necessary to ensure the negative pin voltage stays within low noise limits. Internal full-scale calibration connects full-scale voltage to the input automatically. It is recommended after channel gain changes and must be run before internal zero-scale calibration. Reset the offset register to 0x800000 beforehand. All gain settings are fully calibrated during factory production, eliminating the need for users to perform internal full-scale calibration. Executing internal full-scale calibration might degrade the device's gain error performance.

System calibrations need external zero-scale and full-scale voltages applied in advance to eliminate system errors, with zero-scale calibration done first. Monitor nRDY or DOUT/nRDY via polling or interrupt to check the calibration status.

Offset and system full-scale calibration take one filter settling time, while internal full-scale calibration (gain > 1) takes four. Lower data rates deliver higher calibration accuracy. Recalibrate the channel if reference or gain changes.

Offset and system full-scale calibration work across all power modes. Internal full-scale calibration only supports low and mid power modes, and its result remains valid in full power mode with unchanged gain.

The typical uncalibrated offset error is ±1.5μV (gain 1 ~ 128), and the calibration cuts it down to noise level. The factory gain error across all gain ranges is within ±0.0015%. System full-scale calibration reduces gain error to noise level.

The 24-bit calibration registers are accessible for read/write except during calibration. Users can read coefficients or load preset values from EEPROM to adjust span and offset.

All register write operations shall be ignored and shall have no effect while calibration is underway. When detecting calibration completion via the falling edge of the DOUT/nRDY pin, wait at least 3 MCLK cycles after sending the calibration command before checking the DOUT/nRDY pin.

DETAILED DESCRIPTION (continued)

Span and Offset Limits

System calibration has fixed offset and span limits. The upper full-scale limit is capped at 1.05 × V_{REF}/gain, with the analog modulator supporting the 5% over-range.

Input span ranges from 0.8 × V_{REF}/gain to 2.1 × V_{REF}/gain for both unipolar and bipolar modes. The allowable offset varies by operating mode and the configured span, and the sum of offset and span must not exceed 1.05 × V_{REF}/gain.

Unipolar mode limits:
- Span = 0.8 × V_{REF}/gain: offset range -1.05 to +0.25 × V_{REF}/gain
- Span = V_{REF}/gain: offset range -1.05 to +0.05 × V_{REF}/gain
- Offset = 0.2 × V_{REF}/gain: max span = 0.85 × V_{REF}/gain

Bipolar mode limits:
- Span = ±0.4 × V_{REF}/gain: offset range -0.65 to +0.65 × V_{REF}/gain
- Span = ±V_{REF}/gain: offset range -0.05 to +0.05 × V_{REF}/gain
- Offset = ±0.2 × V_{REF}/gain: max span = ±0.85 × V_{REF}/gain

System Synchronization

The nSYNC pin resets modulator and digital filter without altering configurations, letting sampling start at its rising edge. Pull nSYNC low for at least four MCLK cycles for valid synchronization.

For multiple devices sharing a clock, a shared nSYNC signal unifies operation. Its falling edge resets modules and holds the steady state while low. Devices resume sampling on the MCLK falling edge after nSYNC rises. Drive nSYNC high at MCLK rising edge to keep all devices aligned. The delayed rising edge may cause up to one MCLK cycle offset between units.

nSYNC also acts as a conversion trigger: the rising edge starts conversion, and nRDY falling edge marks completion. Reserve full filter settling time for data updates. For instance, a sinc^4 filter with zero latency disabled has the settling time of 4/f_{ADC}.

Digital Filter

This chip supports multiple configurable digital filters, which affect data rate, settling time and 50Hz/60Hz noise rejection. Filter types are selected via corresponding register bits for sinc filters.

Sinc^4 Filter

The device defaults to sinc^4 filter on power-up. It delivers superior noise performance and optimal 50Hz/60Hz rejection, yet features longer settling time. Gray modules in Figure 25 remain unused.

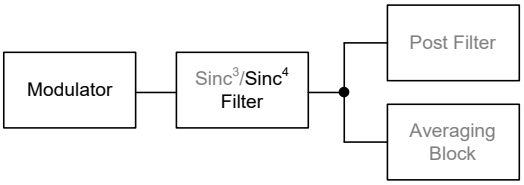


Figure 25. Sinc^4 Filter

Sinc^4 Output Data Rate and Settling Time

The single-channel continuous conversion output data rate is defined as below.

$$f_{ADC} = f_{CLK}/(32 \times FS[10:0]) \quad (5)$$

where:
Define parameters:
f_{ADC} = Output data rate.
f_{CLK} = Master clock (Full: 614.4kHz, Mid: 153.6kHz, Low: 76.8kHz).
FS[10:0] = Filter register value, range 1 ~ 2047.

Data rate ranges:
Full power: 9.38SPS to 19200SPS.
Mid power: 2.35SPS to 4800SPS.
Low power: 1.17SPS to 2400SPS.

The settling time for the sinc^4 filter is equal to

$$t_{SETTLE} = (4 \times 32 \times FS[10:0] + \text{Dead Time})/f_{CLK} \quad (6)$$

where Dead Time = 83.

When a channel change occurs, the modulator and filter are reset. The settling time is allowed to generate the first conversion after the channel change. Subsequent conversions on this channel occur at 1/f_{ADC}. Refer to Figure 26.

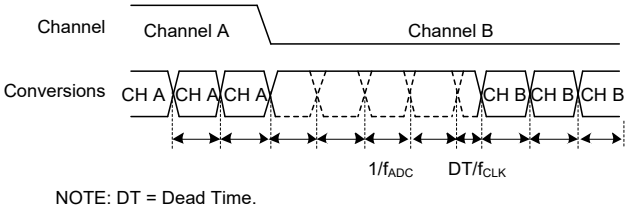


Figure 26. Sinc^4 Channel Change

Table 48. Filter Registers

Addr.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	R/W
0x21 to 0x28	FILTER_0 to FILTER_7	Filter[2:0]			REJ60	POST_FILTER[2:0]			SINGLE_CYCLE	0x060180	R/W
		0					FS[10:8]				
		FS[7:0]									

DETAILED DESCRIPTION (continued)

Upon the analog input step changes, the ADC keeps outputting data at the set rate. It takes four conversion cycles for readings to stabilize normally. If the change occurs during mid-conversion, the stabilization requires five conversion cycles. Refer to Figure 27.

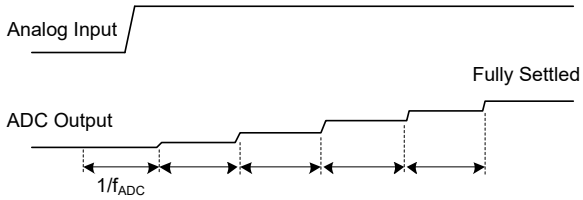


Figure 27. Asynchronous Step Change in the Analog Input

Table 49 lists typical FS[10:0] settings and their corresponding output data rates as well as the settling times.

Table 49. Examples of Output Data Rates and the Corresponding Settling Times for Sinc^4 Filter

Power Mode	FS[10:0] Settings	Output Data Rate (SPS)	Settling Time (ms)
Full Power (f_{CLK} = 614.4kHz)	1920	10	400.14
	384	50	80.14
	320	60	66.80
Mid Power (f_{CLK} = 153.6kHz)	480	10	400.54
	96	50	80.54
	80	60	67.21
Low Power (f_{CLK} = 76.8kHz)	240	10	401.08
	48	50	81.08
	40	60	67.75

Sinc^4 Zero Latency

Enable zero latency by setting the SINGLE_CYCLE bit to 1. In this mode, the single-channel continuous conversion time roughly equals settling time, and the conversion intervals stay consistent for single or multi-channel operation. The single-channel output data rate is defined as follows.

$$f_{ADC} = f_{CLK}/(4 \times 32 \times FS[10:0]) \quad (7)$$

where:

f_{ADC} = Output data rate.

f_{CLK} = Master clock frequency.

FS[10:0] = The decimal equivalent of the FS[10:0] bits in the setup filter register.

Channel switching adds initial conversion delay:

Dead Time/f_{CLK}.

where Dead Time = 83.

This delay is negligible at low data rates but critical at high rates. Table 50 lists related data rates and settling times for typical FS[10:0] settings.

Multi-channel operation inherently uses zero latency mode, so enabling the SINGLE_CYCLE bit brings no extra advantage.

Table 50. Examples of Output Data Rates and the Corresponding Settling Times for Sinc^4 Filter (Zero Latency)

Power Mode	FS[10:0] Settings	Output Data Rate (SPS)	Settling Time (ms)
Full Power (f_{CLK} = 614.4kHz)	1920	2.5	400.14
	384	12.5	80.14
	320	15	66.80
Mid Power (f_{CLK} = 153.6kHz)	480	2.5	400.54
	96	12.5	80.54
	80	15	67.21
Low Power (f_{CLK} = 76.8kHz)	240	2.5	401.08
	48	12.5	81.08
	40	15	67.75

With the steady input or channel switching, conversions maintain a nearly constant data rate. For single-channel operation, a step change aligned with conversion cycles yields fully settled results. An asynchronous step change will produce one unsettled conversion, as shown in Figure 28.

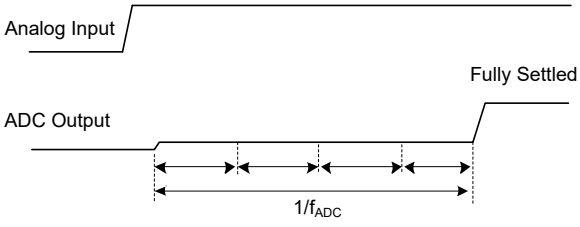


Figure 28. Sinc^4 Zero Latency Operation

Sequencer

Manual channel switching follows the sinc^4 filter rules above. Auto-sequencing for multiple enabled channels has different timing. Refer to Table 49 for the settling time under this condition.

DETAILED DESCRIPTION (continued)

Sinc^4 50Hz and 60Hz Rejection

Figure 29 presents the sinc^4 filter frequency response at 50SPS with zero latency disabled. With zero latency enabled under the same settings, the filter response stays unchanged while the data rate drops to 12.5SPS. With a stable master clock, this filter delivers minimum 120dB rejection for 50Hz (±1Hz) interference.

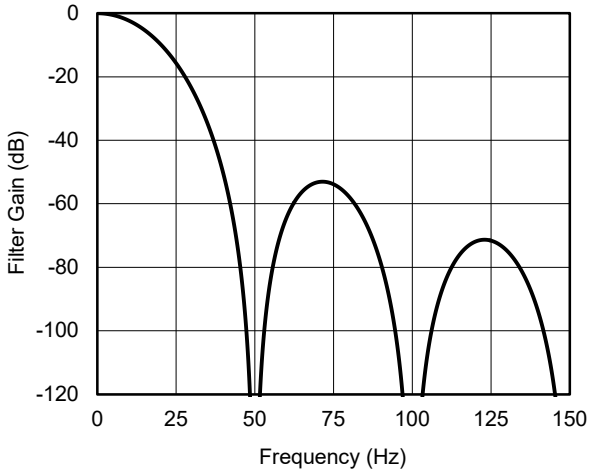


Figure 29. Sinc^4 Filter Response (50SPS with Zero Latency Disabled or 12.5SPS with Zero Latency Enabled)

Figure 30 shows the sinc^4 filter response at 60SPS with zero latency off. Enabling zero latency keeps the response unchanged, while the data rate falls to 15SPS. With a stable master clock, it achieves at least 120dB rejection for 60Hz (±1Hz) interference.

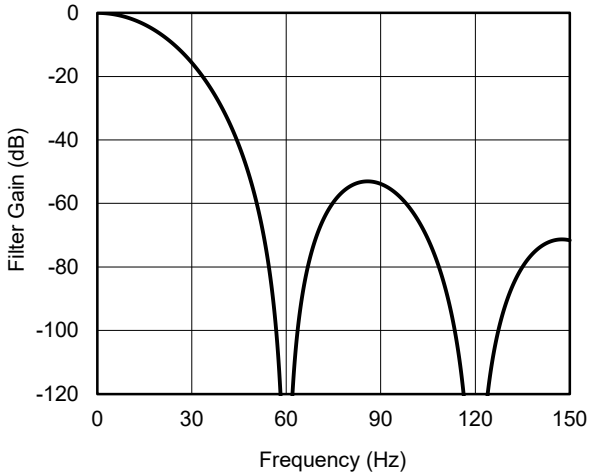


Figure 30. Sinc^4 Filter Response (60SPS with Zero Latency Disabled or 15SPS with Zero Latency Enabled)

At 10SPS (zero latency off) or 2.5SPS (zero latency on), the device rejects both 50Hz and 60Hz interference. With a steady main clock, the sinc^4 filter delivers minimum 120dB rejection for 50Hz (±1Hz) and 60Hz (±1Hz) signals. Refer to Figure 31.

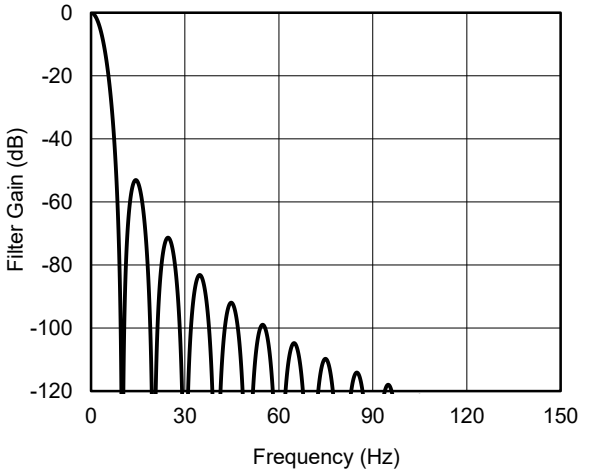


Figure 31. Sinc^4 Filter Response (10SPS with Zero Latency Disabled or 2.5SPS with Zero Latency Enabled)

The REJ60 register bit also enables concurrent 50Hz/60Hz rejection. The sinc filter creates a 50Hz notch, while this bit adds a 60Hz first-order notch. Output rates are 50SPS (zero latency off) and 12.5SPS (zero latency on). Figure 32 plots the sinc^4 filter response. It achieves at least 82dB rejection for 50Hz ± 1Hz and 60Hz ± 1Hz with a stable main clock.

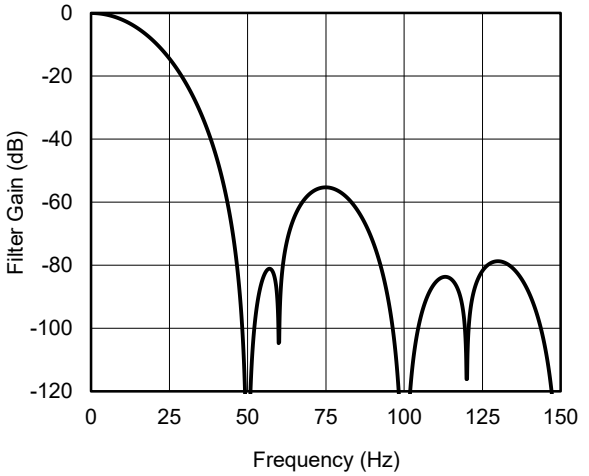


Figure 32. Sinc^4 Filter Response (50SPS with Zero Latency Disabled or 12.5SPS with Zero Latency Enabled, REJ60 = 1)

DETAILED DESCRIPTION (continued)

Sinc^3 Filter

The filter register bits switch between sinc^3 and sinc^4 filters. The sinc^3 version features low noise, medium settling time and moderate 50Hz/60Hz (±1Hz) rejection. Gray blocks in Figure 33 are not functional.

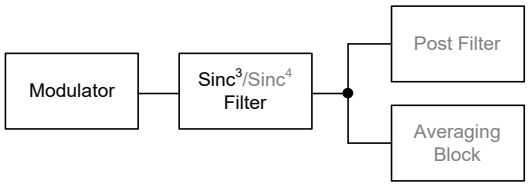


Figure 33. Sinc^3 Filter

Sinc^3 Output Data Rate and Settling Time

The output data rate refers to single-channel conversion speed during continuous ADC operation.

$$f_{ADC} = f_{CLK}/(32 \times FS[10:0]) \quad (8)$$

where:

f_{ADC} = Output data rate.

f_{CLK} = Master clock frequency (614.4kHz in full power mode, 153.6kHz in mid power mode and 76.8kHz in low power mode).

FS[10:0] = The decimal equivalent of the FS[10:0] bits in the filter register. FS[10:0] can have a value from 1 to 2047.

Output data rate ranges: 9.38SPS to 19200SPS (full power), 2.35SPS to 4800SPS (mid power), 1.17SPS to 2400SPS (low power).

The settling time for the sinc^3 filter is equal to

$$t_{SETTLE} = (3 \times 32 \times FS[10:0] + \text{Dead Time})/f_{CLK} \quad (9)$$

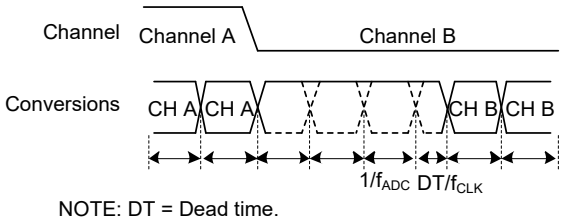
where Dead Time = 82.

Table 51 gives some examples of FS[10:0] settings and the corresponding output data rates and settling times.

Table 51. Examples of Output Data Rates and the Corresponding Settling Times for Sinc^3 Filter

Power Mode	FS[10:0] Settings	Output Data Rate (SPS)	Settling Time (ms)
Full Power (f_{CLK} = 614.4kHz)	1920	10	300.13
	384	50	60.13
	320	60	50.13
Mid Power (f_{CLK} = 153.6kHz)	480	10	300.53
	96	50	60.53
	80	60	50.53
Low Power (f_{CLK} = 76.8kHz)	240	10	301.07
	48	50	61.07
	40	60	51.07

Channel switching resets the modulator and filter. The first conversion needs full settling time (Figure 34); follow-up outputs run at 1/f_{ADC}.



NOTE: DT = Dead time.

Figure 34. Sinc^3 Channel Change

Single-channel step input changes won't be detected instantly. The ADC keeps outputting data at set speed, and needs three conversions for accurate results normally. If the change happens mid-conversion, full settling takes four conversions. Refer to Figure 35.

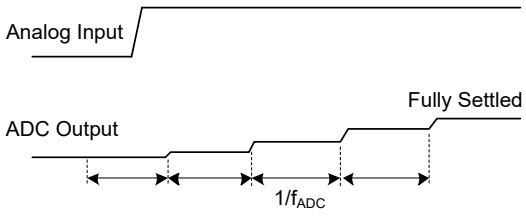


Figure 35. Asynchronous Step Change in the Analog Input

Sinc^3 Zero Latency

Set the filter register's SINGLE_CYCLE bit to 1 to enable zero latency. In continuous single-channel conversion, the conversion time nearly matches settling time. This mode delivers consistent intervals between conversions across single or multiple channels. The output data rate for continuous single-channel sampling equals:

$$f_{ADC} = f_{CLK}/(3 \times 32 \times FS[10:0]) \quad (10)$$

where:

f_{ADC} = Output data rate.

f_{CLK} = Master clock frequency.

FS[10:0] = The decimal equivalent of the FS[10:0] bits in the filter register.

Channel switching adds a first-conversion delay of Dead Time/f_{CLK}: 82 cycles. The delay barely affects settling time at low data rates but matters at high rates. Table 52 lists single-channel output rates and multi-channel settling time for typical FS[10:0] settings. For multi-channel operation, the devices apply full settling time after channel changes, so zero latency via SINGLE_CYCLE bit provides no advantage.

DETAILED DESCRIPTION (continued)

For steady inputs or channel switches, conversions maintain nearly fixed output rates. On a single-channel, synchronized input steps yield fully settled results. Asynchronous steps produce one unsettled conversion (Figure 36).

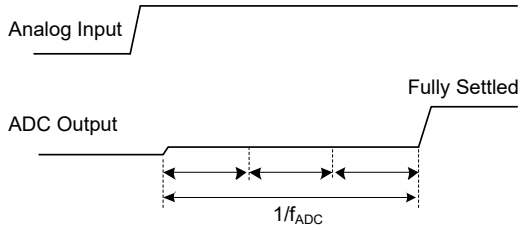


Figure 36. Sinc^3 Zero Latency Operation

Table 52. Examples of Output Data Rates and the Corresponding Settling Times for Sinc^3 Filter (Zero Latency)

Power Mode	FS[10:0] Settings	Output Data Rate (SPS)	Settling Time (ms)
Full Power (f_{CLK} = 614.4kHz)	1920	3.33	300.13
	384	16.67	60.13
	320	20	50.13
Mid Power (f_{CLK} = 153.6kHz)	480	3.33	300.53
	96	16.67	60.53
	80	20	50.53
Low Power (f_{CLK} = 76.8kHz)	240	3.33	301.07
	48	16.67	61.07
	40	20	51.07

Sequencer

Manual channel switching follows the Sinc^3 Filter section. With multiple channels enabled, the internal sequencer cycles through them automatically. Refer to Table 51 for the settling time under this condition.

Sinc^3 50Hz and 60Hz Rejection

Figure 37 presents the sinc^3 filter response at 50SPS with zero latency off. Enabling zero latency keeps the response unchanged while lowering the rate to 16.67SPS. This filter offers minimum 95dB rejection for 50Hz ± 1Hz with a stable main clock.

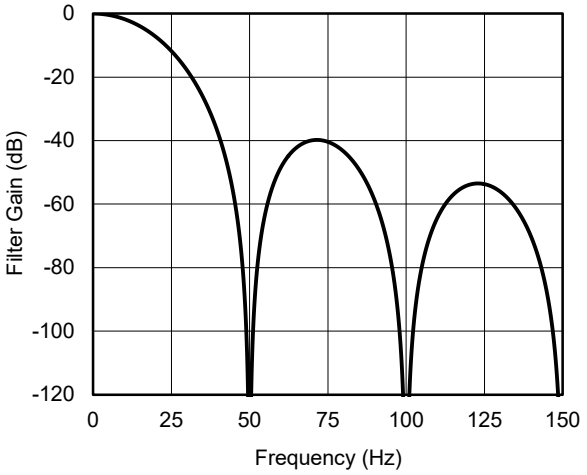


Figure 37. Sinc^3 Filter Response (50SPS with Zero Latency Disabled or 16.67SPS with Zero Latency Enabled)

Figure 38 illustrates the sinc^3 filter response at 60SPS with zero latency disabled. Enabling zero latency retains the response and sets the rate to 20SPS. It provides at least 95dB rejection for 60Hz ± 1Hz with a stable master clock.

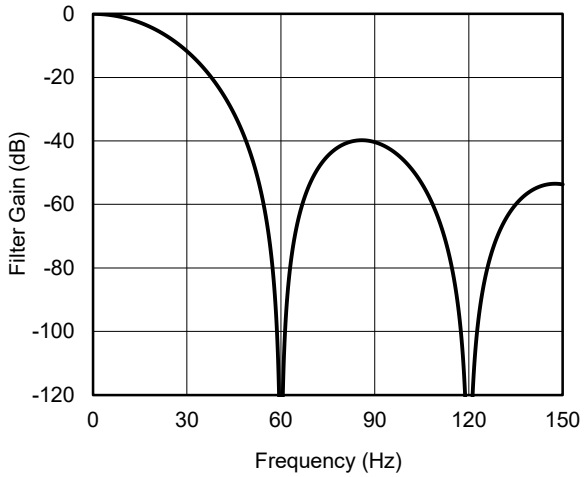


Figure 38. Sinc^3 Filter Response (60SPS with Zero Latency Disabled or 20SPS with Zero Latency Enabled)

DETAILED DESCRIPTION (continued)

The 50Hz and 60Hz interference is rejected at 10SPS (zero latency off) or 3.33SPS (zero latency on). The sinc^3 filter delivers minimum 100dB rejection for 50Hz ± 1Hz and 60Hz ± 1Hz, as shown in Figure 39.

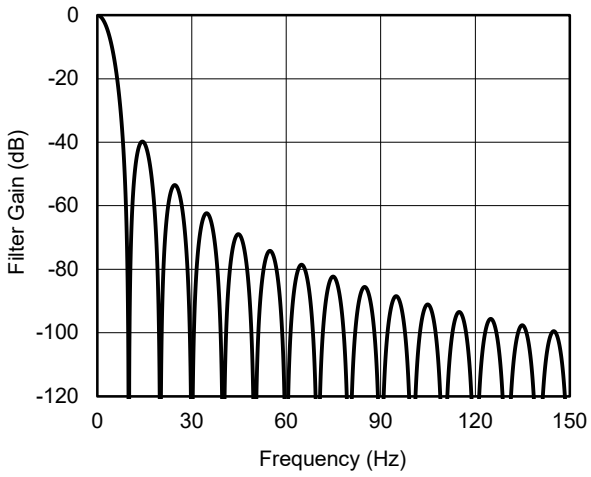


Figure 39. Sinc^3 Filter Response (10SPS with Zero Latency Disabled or 3.33SPS with Zero Latency Enabled)

The filter register's REJ60 bit also enables combined 50Hz/60Hz rejection. The sinc filter creates a 50Hz notch, while this bit adds a 60Hz first-order notch. Output rates are 50SPS (zero latency off) and 16.67SPS (on). Figure 40 shows the corresponding sinc^3 filter response. It delivers over 67dB rejection for 50Hz/60Hz (±1Hz) with a stable clock.

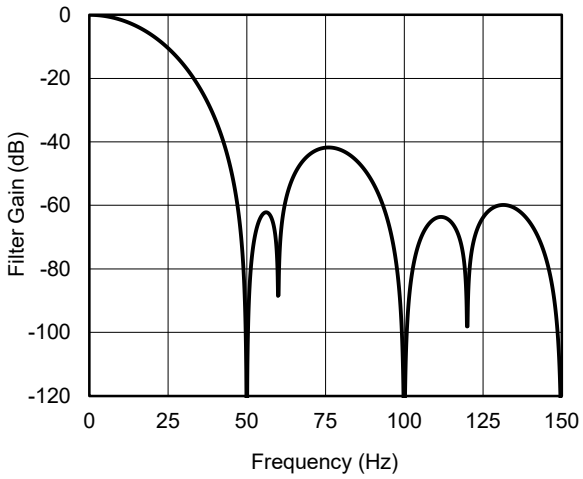


Figure 40. Sinc^3 Filter Response (50SPS with Zero Latency Disabled or 16.67SPS with Zero Latency Enabled, REJ60 = 1)

Fast Settling Mode (Sinc^4 + Sinc^1 Filter)

Fast settling mode features settling time near the first filter notch reciprocal, enabling 50Hz/60Hz rejection at rates close to 1/50Hz or 1/60Hz. Its settling time roughly equals the inverse of output data rate, keeping conversion time steady across single and multi-channel operation. Activate this mode via filter register bits. It adds a sinc^1 stage after sinc^4: 16-point averaging for full/mid power, 8-point for low power. Gray blocks in Figure 41 are unused.

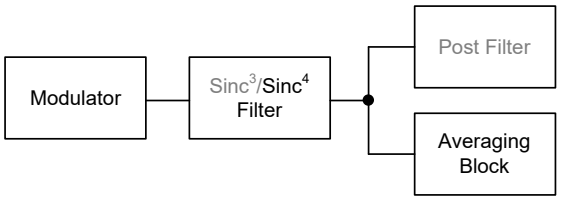


Figure 41. Fast Settling Mode, Sinc^4 + Sinc^1 Filter

Output Data Rate and Settling Time, Sinc^4 + Sinc^1 Filter

When the analog input is continuously sampled on a single-channel, the output data rate equals

$$f_{ADC} = f_{CLK}/(Avg \times 32 \times FS[10:0]) \quad (11)$$

where:

f_{ADC} = Output data rate.

f_{CLK} = Master clock frequency (614.4kHz in full power mode, 153.6kHz in mid power mode, and 76.8kHz in low power mode).

Avg = 16 for the full or mid power mode and 8 for low power mode.

FS[10:0] = The decimal equivalent of the FS[10:0] bits in the filter register. FS[10:0] can have a value from 1 to 2047.

When another channel is selected by the user, there is an extra delay in the first conversion. The settling time is equal to:

$$t_{SETTLE} = ((4 + Avg - 1) \times 32 \times FS[10:0] + Dead\ Time)/f_{CLK} \quad (12)$$

where Dead Time = 83.

DETAILED DESCRIPTION (continued)

Table 53 lists sample FS[10:0] settings and the corresponding output data rates and settling times.

Table 53. Examples of Output Data Rates and the Corresponding Settling Times (Fast Settling Mode, Sinc^4 + Sinc^1)

Power Mode	FS[10:0] Settings	First Notch (Hz)	Output Data Rate (SPS)	Settling Time (ms)
Full Power (f_{CLK} = 614.4kHz, Average by16)	120	10	10	118.89
	24	50	50	23.89
	20	60	60	19.93
Mid Power (f_{CLK} = 153.6kHz, Average by16)	30	10	10	119.29
	6	50	50	24.29
	5	60	60	20.33
Low Power (f_{CLK} = 76.8kHz, Average 8)	30	10	10	138.58
	6	50	50	28.58
	5	60	60	24.00

Steady analog inputs or channel switches maintain nearly fixed conversion output rates.

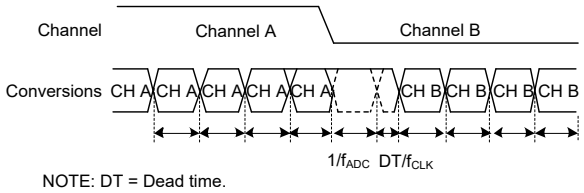


Figure 42. Fast Settling, Sinc^4 + Sinc^1 Filter

During single-channel conversion, the ADC keeps outputting data after an analog step change. A synchronized change produces one unsettled result (Figure 43), while an asynchronous one yields one or two unsettled outputs.

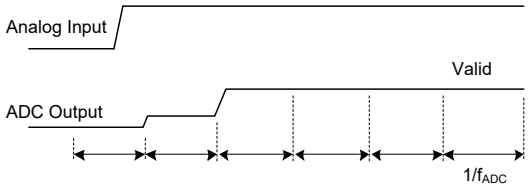


Figure 43. Step Change on the Analog Input, Sinc^4 + Sinc^1 Filter

Sequencer

The fast settling mode rules apply to manual channel switching. With multiple channels enabled, the internal sequencer runs automatically. Refer to Table 53 for the settling time under this condition.

50Hz and 60Hz Rejection, Sinc^4 + Sinc^1 Filter

Figure 44 shows the frequency response for FS[10:0] value = 24 (full power) or 6 (mid/low power). Corresponding output rates are listed in Table 53. The sinc filter sets its first notch at

$$f_{NOTCH} = f_{CLK}/(32 \times FS[10:0]) \quad (13)$$

The sinc^1 filter creates notches at f_{NOTCH}/Avg, with Avg = 16 for full/mid power and 8 for low power, plus harmonics of this frequency. With FS[10:0] value = 6, the sinc filter produces an 800Hz notch in full/mid power, while averaging adds 50Hz and its harmonics. In low power mode, the sinc filter notch is 400Hz, alongside 50Hz harmonic notches from averaging.

The 50Hz first-order notch has narrow bandwidth. It offers strong rejection at exactly 50Hz with a stable clock, but performance drops notably at 50Hz ± 1Hz. Rejection is at least 40dB at 50Hz ± 0.5Hz, so a high-quality clock is advised for the fast settling mode.

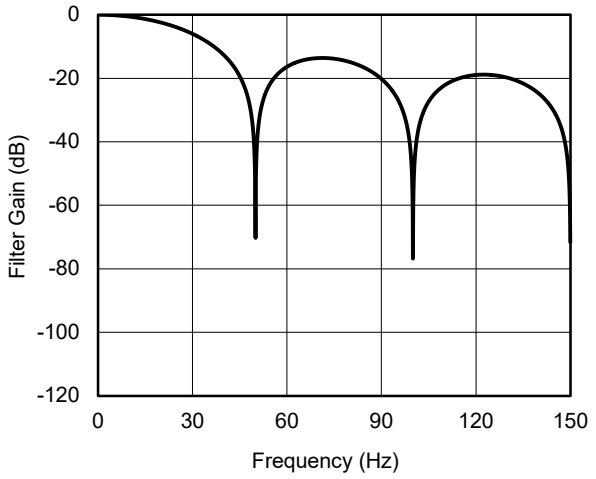


Figure 44. 50Hz Rejection

Figure 45 displays the filter response for FS[10:0] value = 20 (full power) or 5 (mid/low power). It creates notches at 60Hz and its harmonics, with minimum 40dB rejection at 60Hz ± 0.5Hz.

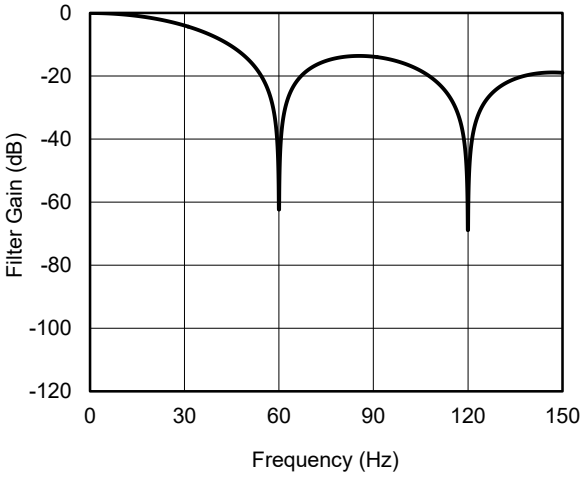


Figure 45. 60Hz Rejection

DETAILED DESCRIPTION (continued)

FS[10:0] value = 384 (full power) or 30 (mid/low power) enables concurrent 50Hz/60Hz rejection. Notches lie at 10Hz and its harmonics. Typical rejection reaches 44dB at 50Hz ± 0.5Hz and 60Hz ± 0.5Hz.

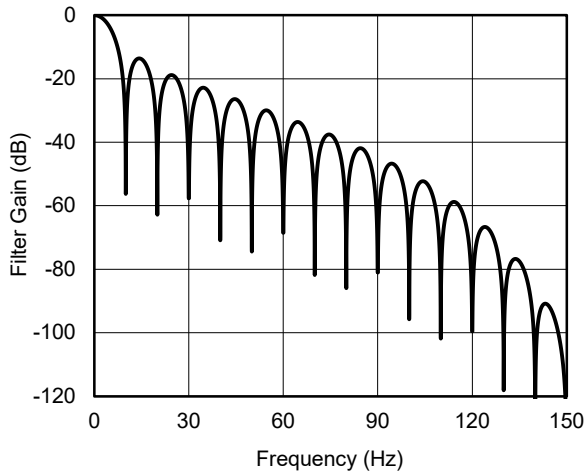


Figure 46. Simultaneous 50Hz and 60Hz Rejection

Fast Settling Mode (Sinc^3 + Sinc^1 Filter)

In fast settling mode, settling time approximates the reciprocal of the first filter notch, enabling 50Hz/60Hz rejection at rates near 1/50Hz or 1/60Hz. Settling time roughly equals the inverse of output data rate, keeping conversion time consistent for single and multi-channel use. Activate this mode via filter register bits. It adds a sinc^1 stage after sinc^3: 16-point averaging for full/mid power, 8-point for low power. Gray blocks in Figure 47 are unused.

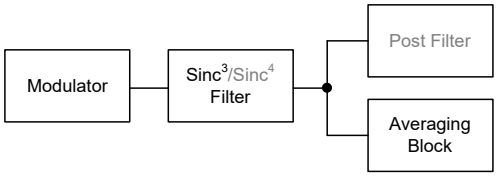


Figure 47. Fast Settling Mode, Sinc^3 + Sinc^1 Filter

Output Data Rate and Settling Time, Sinc^3 + Sinc^1 Filter

When continuously converting on a single-channel, the output data rate is

$$f_{ADC} = f_{CLK}/(Avg \times 32 \times FS[10:0]) \quad (14)$$

where:

f_{ADC} = Output data rate.

f_{CLK} = Master clock frequency (614.4kHz in full power mode, 153.6kHz in mid power mode, and 76.8kHz in low power mode).

Avg = 16 in full or mid power mode and 8 in low power mode.

FS[10:0] is the decimal equivalent of the FS[10:0] bits in the filter register. FS[10:0] can have a value from 1 to 2047.

When another channel is selected by the user, there is an extra delay in the first conversion. The settling time is equal to

$$t_{SETTLE} = ((3 + Avg - 1) \times 32 \times FS[10:0] + Dead\ Time)/f_{CLK} \quad (15)$$

where Dead Time = 82.

Table 54 lists some sample FS[10:0] settings and the corresponding output data rates and settling times.

Table 54. Examples of Output Data Rates and the Corresponding Settling Times (Fast Settling Mode, Sinc^3 + Sinc^1)

Power Mode	FS[10:0] Settings	First Notch (Hz)	Output Data Rate (SPS)	Settling Time (ms)
Full Power (f_{CLK} = 614.4kHz, Average by16)	120	10	10	112.63
	24	50	50	22.63
	20	60	60	18.88
Mid Power (f_{CLK} = 153.6kHz, Average by16)	30	10	10	113.03
	6	50	50	23.03
	5	60	60	19.28
Low Power (f_{CLK} = 76.8kHz, Average 8)	30	10	10	126.07
	6	50	50	26.07
	5	60	60	21.90

Stable analog inputs or channel changes deliver conversions at nearly steady output rates. Refer to Figure 48.

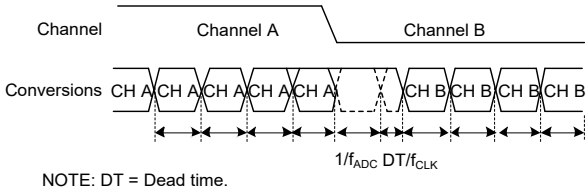


Figure 48. Fast Settling, Sinc^3 + Sinc^1 Filter

During single-channel conversion, the ADC keeps outputting data after an analog step change. A synchronized change produces one unsettled result (Figure 49), while an asynchronous one yields one or two unsettled outputs.

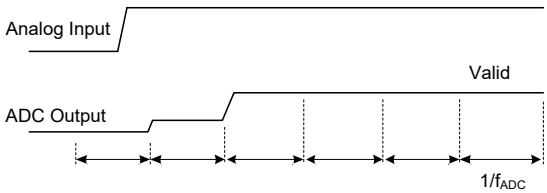


Figure 49. Step Change on the Analog Input, Sinc^3 + Sinc^1 Filter

DETAILED DESCRIPTION (continued)

Sequencer

The rules for fast settling mode ($sinc^3$ + $sinc^1$) apply to manual channel switching. With multiple channels enabled, the built-in sequencer operates automatically. Refer to Table 54 for the settling time under this condition.

50Hz and 60Hz Rejection, $Sinc^3$ + $Sinc^1$ Filter

Figure 50 shows the frequency response for FS[10:0] value = 24 (full power) or 6 (mid/low power). Corresponding output data rates are specified in Table 54. The sinc filter sets its first notch at

$$f_{NOTCH} = f_{CLK}/(32 \times FS[10:0]) \quad (16)$$

The averaging stage generates notches at f_{NOTCH}/Avg and its harmonics. Avg is 16 for full/mid power modes and 8 for low power mode. With FS[10:0] value = 6, the sinc filter creates an 800Hz notch in full/mid power, while averaging produces notches at 50Hz and its multiples. In low power mode, the sinc filter notch shifts to 400Hz, with 50Hz harmonic notches remaining.

The 50Hz first-order notch has a narrow bandwidth. It delivers effective rejection at exactly 50Hz with a stable clock, but performance drops sharply within 50Hz ± 1Hz. Rejection is no less than 40dB at 50Hz ± 0.5Hz. A high-quality clock is thus recommended for fast settling mode.

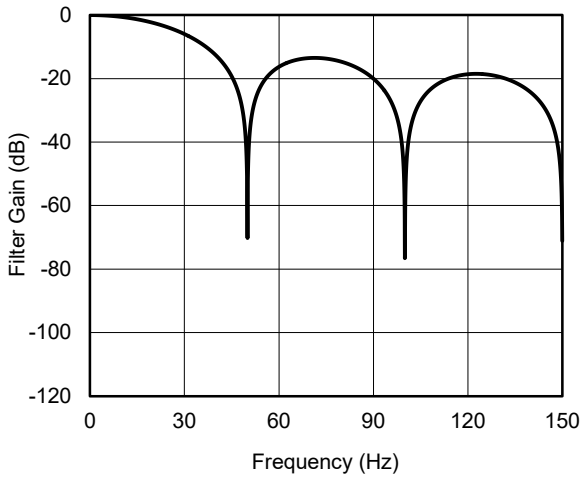


Figure 50. 50Hz Rejection

Figure 51 presents the filter response for FS[10:0] value = 20 (full power) or 5 (mid/low power). Notches are formed at 60Hz and its harmonics, with a minimum rejection of 40dB at 60Hz ± 0.5Hz.

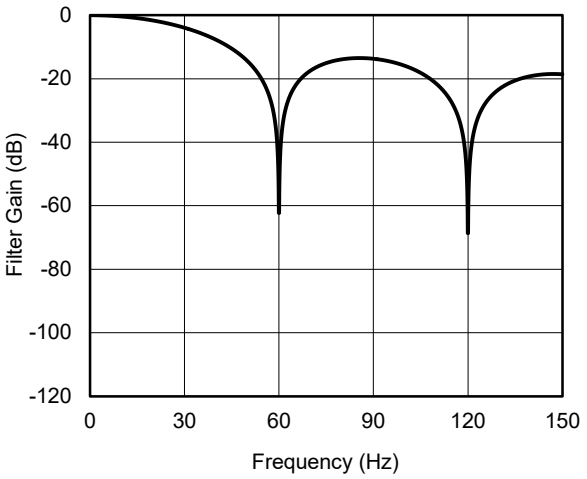


Figure 51. 60Hz Rejection

Setting FS[10:0] value to 384 (full power) or 30 (mid/low power) enables concurrent 50Hz and 60Hz rejection. Notches occur at 10Hz and its harmonics. The typical rejection reaches 42dB at 50Hz ± 0.5Hz and 60Hz ± 0.5Hz.

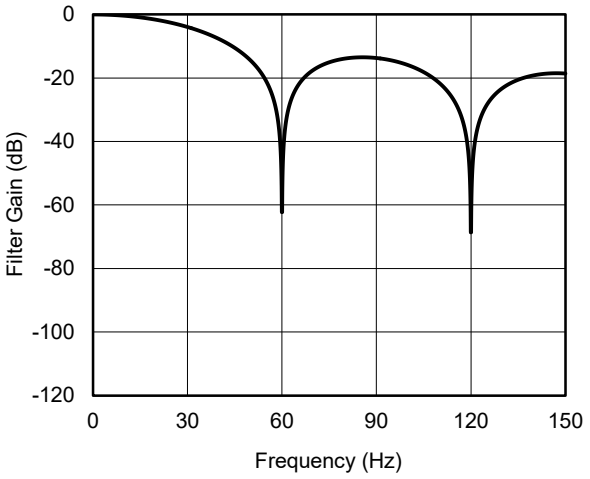


Figure 52. Simultaneous 50Hz and 60Hz Rejection

DETAILED DESCRIPTION (continued)

Post Filters

The post filters deliver simultaneous 50Hz and 60Hz rejection, with adjustable trade-off between settling time and attenuation. They support a maximum output data rate of 27.27SPS and can suppress 50Hz ± 1Hz and 60Hz ± 1Hz interference by up to 90dB. These filters process the output of the $sinc^3$ filter. To enable post filters, set all filter bits to logic 1, and select the specific post filter configuration via the POST_FILTER[2:0] bits in the filter register. Gray blocks in Figure 53 are unused.

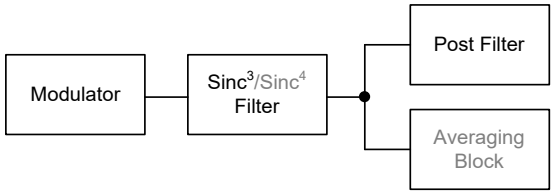


Figure 53. Post Filters

Table 55 shows the output data rates with the accompanying settling times and the rejection. When continuously converting on a single-channel, the first conversion requires a time of t_{SETTLE}. Subsequent conversions occur at $1/f_{ADC}$. When multiple channels are enabled (either manually or using the sequencer), the settling time is required to generate a valid conversion on each enabled channel.

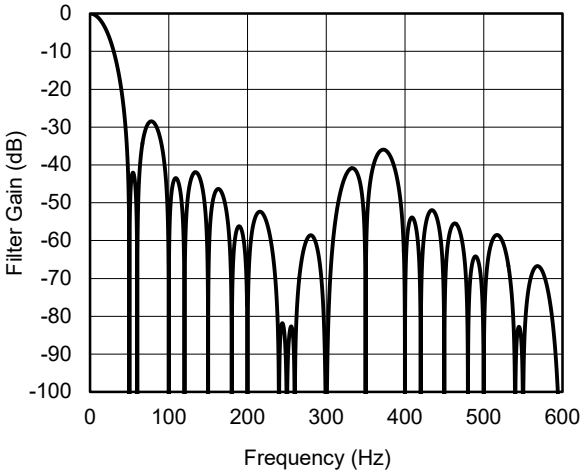


Figure 54. DC to 600Hz, 27.27SPS Output Data Rate, 36.67ms Settling Time

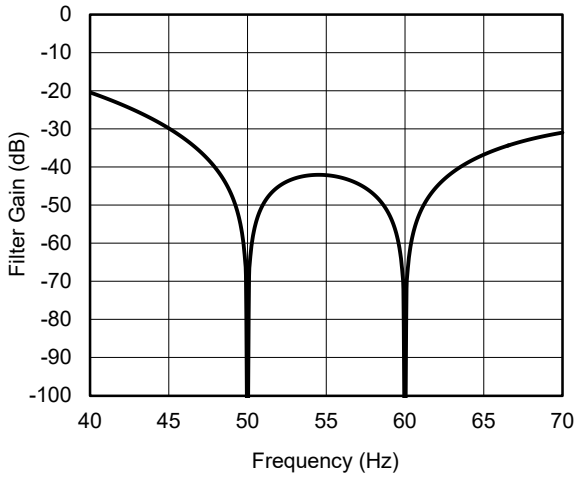


Figure 55. Zoom in 40Hz to 70Hz, 27.27SPS Output Data Rate, 36.67ms Settling Time

Table 55. Post Filters: Output Data Rate, Settling Time (t_{SETTLE}), and Rejection

Output Data Rate (SPS)	f_{3dB} (Hz)	Settling Time (t_{SETTLE}) (ms)			Simultaneous Rejection of 50Hz ± 1Hz and 60Hz ± 1Hz (dB) (1)
		Full Power Mode	Mid Power Mode	Low Power Mode	
27.27	17.28	38.463	38.854	39.375	47
25	15.12	41.796	42.1875	42.708	62
20	13.38	51.797	52.187	52.708	86
16.67	12.66	61.797	62.187	62.708	92

NOTE:

1. Stable master clock used.

DETAILED DESCRIPTION (continued)

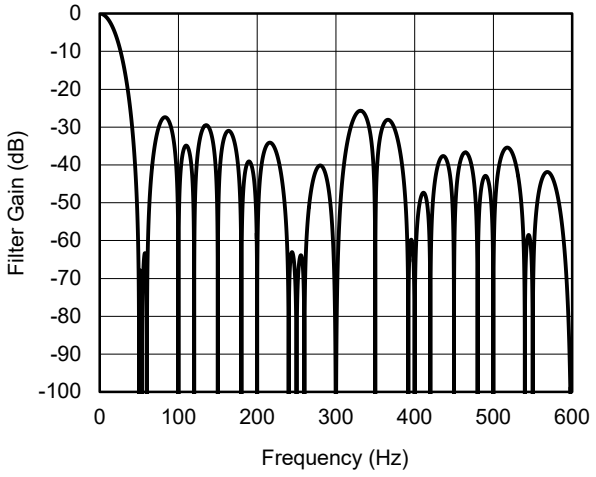


Figure 56. DC to 600Hz, 25SPS Output Data Rate, 40ms Settling Time

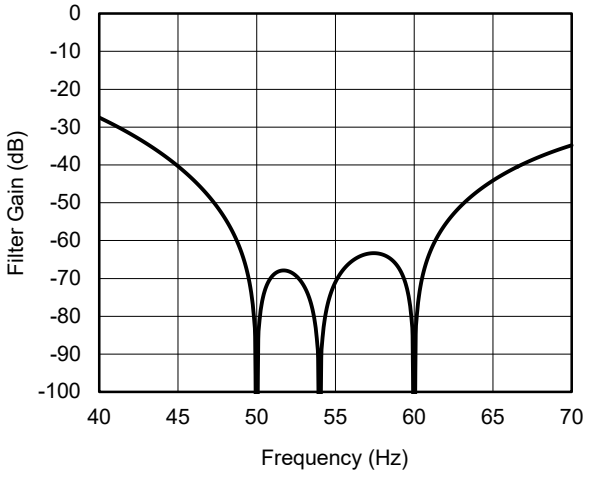


Figure 57. Zoom in 40Hz to 70Hz, 25SPS Output Data Rate, 40ms Settling Time

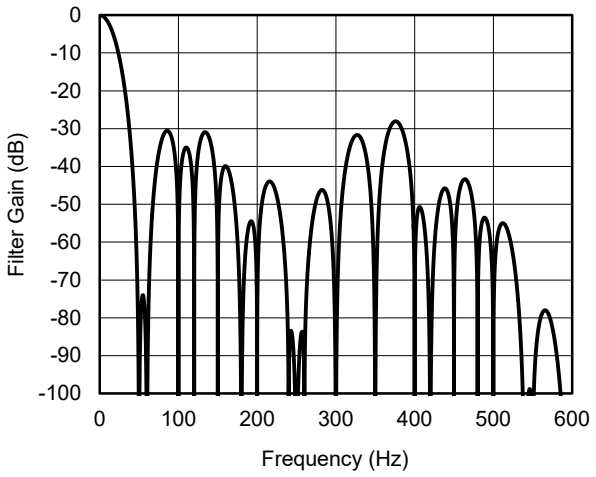


Figure 58. DC to 600Hz, 20SPS Output Data Rate, 50ms Settling Time

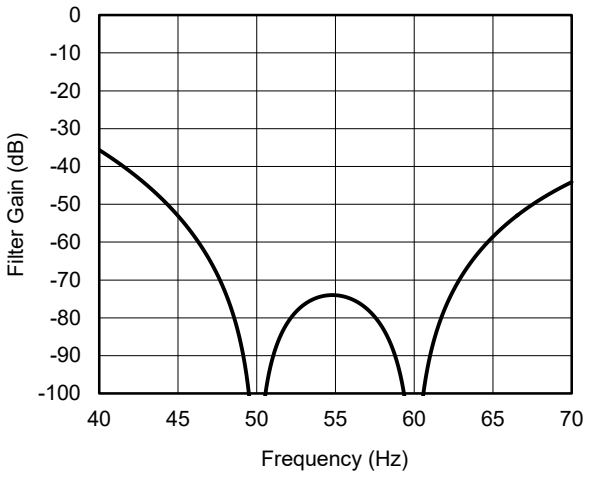


Figure 59. Zoom in 40Hz to 70Hz, 20SPS Output Data Rate, 50ms Settling Time

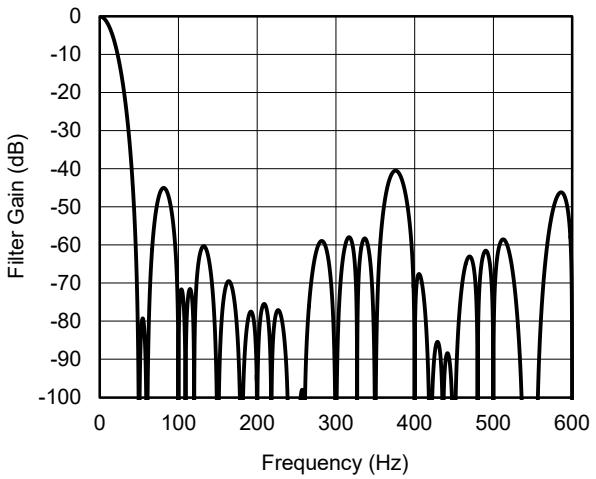


Figure 60. DC to 600Hz, 16.667SPS Output Data Rate, 60ms Settling Time

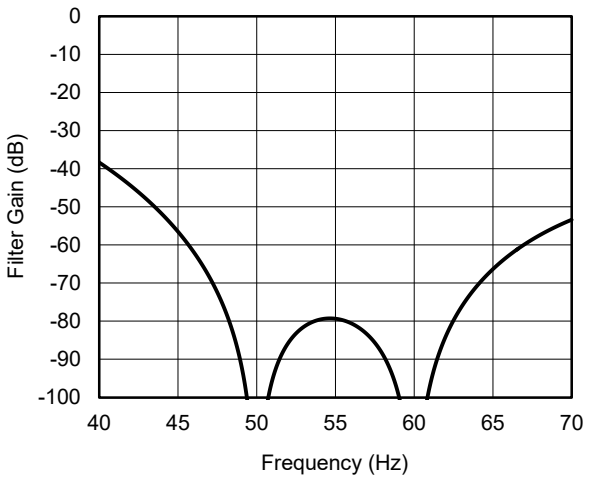


Figure 61. Zoom in 40Hz to 70Hz, 16.667SPS Output Data Rate, 60ms Settling Time

DETAILED DESCRIPTION (continued)

Summary of Filter Options

The SGM52421R8/SGM52421R8A support multiple filter modes. Filter selection impacts output data rate, settling time, RMS noise, stop-band attenuation and 50Hz/60Hz rejection. Table 56 lists the typical configurations with their throughput and line frequency rejection performance.

Table 56. Filter Summary

Filter	Power Mode	Output Data Rate (SPS)	REJ60 Bit	50Hz Rejection (dB) (1) (2)
$Sinc^4$	All	10	0	120dB (50Hz and 60Hz)
	All	50	0	120dB (50Hz only)
	All	50	1	82dB (50Hz and 60Hz)
	All	60	0	120dB (60Hz only)
$Sinc^4$, Zero Latency	All	12.5	0	120dB (50Hz only)
	All	12.5	1	82dB (50Hz and 60Hz)
	All	15	0	120 dB (60Hz only)
$Sinc^3$	All	10	0	100dB (50Hz and 60Hz)
	All	50	0	95dB (50Hz only)
	All	50	1	67dB (50Hz and 60Hz)
	All	60	0	95dB (60Hz only)
Fast Settling ($Sinc^4$ + $Sinc^1$)	Full/Mid	60	0	40dB (60Hz only)
	Low	60	0	40dB (60Hz only)
	Full/Mid	50	0	40dB (50Hz only)
	Low	50	0	40dB (50Hz only)
	Full/Mid	10	0	40dB (50Hz and 60Hz)
	Low	10	0	40dB (50Hz and 60Hz)
Fast Settling ($Sinc^3$ + $Sinc^1$)	Full/Mid	60	0	40dB (60Hz only)
	Low	60	0	40dB (60Hz only)
	Full/Mid	50	0	40dB (50Hz only)
	Low	50	0	40dB (50Hz only)
	Full/Mid	10	0	40dB (50Hz and 60Hz)
	Low	10	0	40dB (50Hz and 60Hz)
Post Filter	All	27.27	0	47dB (50Hz and 60Hz)
	All	25	0	62dB (50Hz and 60Hz)
	All	20	0	85dB (50Hz and 60Hz)
	All	16.67	0	90dB (50Hz and 60Hz)

NOTES:

1. Calculations are based on a steady master clock.

2. Fast settling mode measures 50Hz/60Hz rejection within ±0.5Hz bandwidth. Other modes use ±1Hz range.

DETAILED DESCRIPTION (continued)

Diagnostics

The SGM52421R8/SGM52421R8A integrate rich on-chip diagnostics. These functions verify valid register access and data writing, proper LDO decoupling, availability of external reference (if applied), and normal operation of ADC modulator and filter.

Signal Chain Check

The reference and supply voltages can serve as ADC inputs for device voltage monitoring. The chip also provides an internal 20mV signal with 10mV common mode level, selectable via the channel registers. Its negative terminal connects to AV_{SS}.

When measuring this 20mV signal, disregard the AINM_UV_ERR flag even if triggered. This signal verifies PGA performance; higher PGA gain doubles the relative input amplitude.

Note that 20mV reference cannot test the signal chain at gain 1 with AIN_BUFM buffer enabled due to 100mV headroom requirement. Use supply or LDO voltage for such tests instead.

Reference Detect

The SGM52421R8/SGM52421R8A integrate circuits to detect valid external reference for conversion and calibration. This function benefits RTD, strain gage and the other systems using external reference sources.

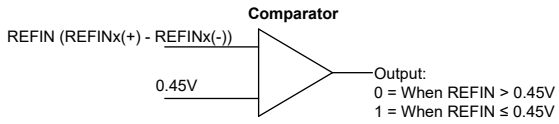


Figure 62. Reference Detect Circuitry

Enable this function by setting REF_DET_ERR_EN bit in ERROR_EN register to high. The chip flags the invalid external reference when REFINx(+/-) pins differential voltage drops below 0.45V or either pin is open, asserting REF_DET_ERR bit and status *_ERR bits.

During the normal conversion, invalid reference outputs all 1s data, so check this result instead of continuous flag monitoring. During offset/full-scale calibration, the chip blocks calibration register updates to prevent wrong coefficients. Verify REF_DET_ERR bit after each calibration if required.

The flag may trigger on standby exit; read the error register to clear it afterwards.

Calibration, Conversion and Saturation Errors

The SGM52421R8/SGM52421R8A monitor conversion and calibration via built-in diagnostics. Enable them with ADC_CAL_ERR_EN, ADC_CONV_ERR_EN and ADC_SAT_ERR_EN bits. The related error flags will assert upon faults.

The ADC_CONV_ERR bit triggers on digital filter overflow/underflow, with output clamped to all 0s or 1s. This flag updates the data register and be cleared only after the error register is read.

The ADC_SAT_ERR bit indicates modulator saturation when 20 consecutive 1s or 0s are detected.

For the offset calibration, if the coefficients exceed the range from 0x7FFFF to 0xF80000, the offset register will be updated and the ADC_CAL_ERR bit will not be set. The full-scale calibration checks filter overflow; faults disable gain register update and raise the error flag.

Over-Voltage/Under-Voltage Detection

On-chip over-/under-voltage monitors track absolute voltage of AINx pins. Operating beyond the rated range impairs the linearity of the ADC.

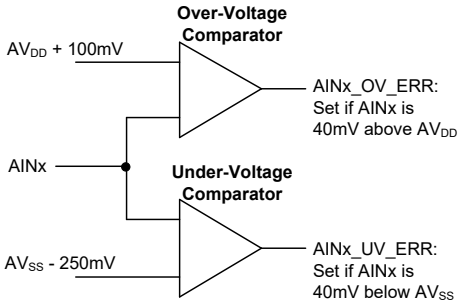


Figure 63. Analog Input Over-Voltage/Under-Voltage Monitors

Separate OV/UV monitoring is available for AINP and AINM. Enable respective checks via the AINP_OV_ERR_EN, AINP_UV_ERR_EN, AINM_OV_ERR_EN and AINM_UV_ERR_EN bits. The AINP triggers OV above AV_{DD} and UV below AV_{SS}; same rules apply to AINM. Corresponding error flags will assert. Read the error register to clear flags after monitoring.

Power Supply Monitors

Besides external signals, the ADC monitors AV_{DD} and IOV_{DD}. These supply voltages are divided by 6 internally before feeding into the Σ-Δ modulator, enabling supply fluctuation detection.

DETAILED DESCRIPTION (continued)

LDO Monitoring

The device features multiple LDO monitoring functions. Analog and digital LDO outputs can be selected as ADC inputs and are tracked continuously.

Power Supply Monitor

Enable ALDO and DLDO monitoring via the ALDO_PSM_ERR_EN and DLDO_PSM_ERR_EN bits. ALDO below 1.6V sets the ALDO_PSM_ERR bit. DLDO below 1.4V sets the DLDO_PSM_ERR bit. Flags stay active until error register is read, even after voltage recovers.

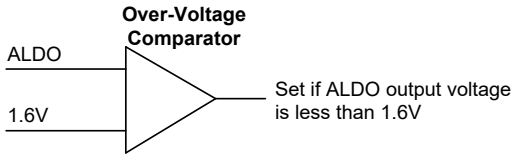


Figure 64. Analog LDO Monitor

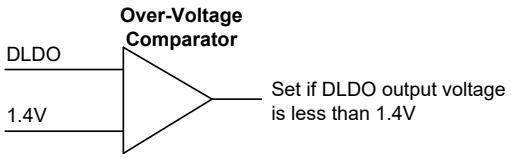


Figure 65. Digital LDO Monitor

The chip supports power monitor circuit testing. Setting the ALDO_PSM_TRIP_TEST_EN or DLDO_PSM_TRIP_TEST_EN bit connects test inputs to GND, which asserts the related LDO error flags.

MCLK Counter

A stable master clock is critical, as it determines data rate, settling time and filter notch frequencies. The device supports MCLK monitoring. Setting the MCLK_CNT_EN bit makes the MCLK_COUNT register increment every 131 clock cycles, for frequency calculation over a fixed interval. This register rolls over at full-scale.

The update of the register is asynchronous to read, which may cause invalid readings. Read the register four times in two separate intervals to get valid values.

SPI SCLK Counter

The SPI SCLK counter tracks pulses per read/write operation, requiring nCS framing. Valid operations use 8/16/32/40/48 SCLK pulses. Non-multiples of eight trigger the SPI_SCLK_CNT_ERR bit and abort invalid writes. Enable via the SPI_SCLK_CNT_ERR_EN bit.

SPI Read/Write Errors

The chip validates SPI read/write register addresses alongside SCLK monitoring. Enable the address check via the SPI_READ_ERR_EN and SPI_WRITE_ERR_EN bits. Accessing undefined registers triggers corresponding error flags and aborts operations.

Combined with SCLK counter and CRC, these diagnostics strengthen SPI reliability and prevent abnormal interface states.

SPI_IGNORE Error

Registers are inaccessible during power-up initialization and offset/gain calibration. Writes in these busy states trigger the SPI_IGNORE_ERR bit and get discarded. This diagnostic is enabled by default and can be disabled via the SPI_IGNORE_ERR_EN bit. The flag clears upon register read.

Checksum Protection

A CRC checksum enhances SPI reliability for register access. Write errors assert CRC_ERR; verify writes via readback and checksum validation.

The fixed CRC polynomial is $x^8 + x^2 + x + 1$. Toggle this function via the CRC_ERR_EN bit. Checksum is added to all SPI transactions: computed from command plus data for writes and reads. See Figure 66 and Figure 67 for transaction details.

With checksum enabled in continuous read mode, an implicit 0x99 command precedes each data transmission for checksum calculation. This guarantees a nonzero checksum even when ADC data is 0x000000.

DETAILED DESCRIPTION (continued)

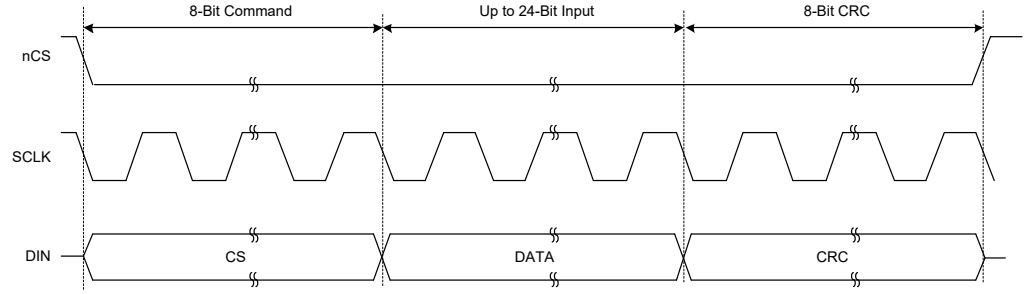


Figure 66. SPI Write Transaction with CRC

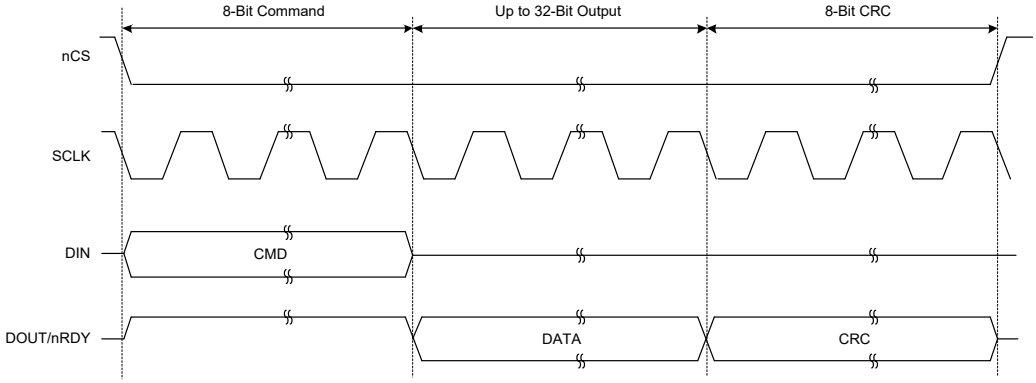


Figure 67. SPI Read Transaction with CRC

Memory Map Checksum Protection

The on-chip registers also support CRC verification, excluding continuously updated status, data, error and MCLK counter registers. The CRC runs every 1/2400 second and recalculates on the register writes, calibrations, single-conversion standby entry and continuous read mode exit. Enable this function via the MM_CRC_ERR_EN bit; the faults will assert the MM_CRC_ERR bit.

ROM Checksum Protection

All registers load ROM-stored defaults at power-up. On power-up, the ROM content undergoes CRC check. Enable this feature via the ROM_CRC_ERR_EN bit; the errors trigger the ROM_CRC_ERR bit. When active, the internal master clock stays on in standby mode.

CRC Calculation

This 8-bit checksum uses polynomial $x^8 + x^2 + x + 1$. Shift data left 8 bits, and then repeatedly XOR with the polynomial aligned to the leading 1 of the current value. The final remainder less than the polynomial is the checksum.

Example of a Polynomial CRC Calculation 24-Bit Word: 0x654321 (8-Bit Command and 16-Bit Data)

Here is an example of generating the 8-bit checksum with the given polynomial.

```
Initial Value          011001010100001100100001
                       011001010100001100100001100000000   left shifted eight bits
x^8 + x^2 + x + 1 =        100000111   polynomial
  100100100000110010000100000000     XOR result
  100000111                          polynomial
    10001100011001000010000000      XOR result
    100000111                       polynomial
      11111110010000100000000       XOR result
      100000111                     Polynomial value
      11111011100001000000000       XOR result
       100000111                    Polynomial value
       11110000000100000000         XOR result
        100000111                   Polynomial value
        11100111000100000000        XOR result
        100000111                   Polynomial value
         11001001001000000000       XOR result
         100000111                  Polynomial value
          10010101010000000000      XOR result
          100000111                 Polynomial value
           10110110000000000        XOR result
           100000111                Polynomial value
            1101011000000           XOR result
            100000111               Polynomial value
             101010110000           XOR result
             100000111              Polynomial value
              1010001000            XOR result
              100000111             Polynomial value
               10000110             checksum = 0x86
```

DETAILED DESCRIPTION (continued)

Burnout Currents

The device integrates two programmable constant current sources with selectable levels: 0.5μA, 2μA and 4μA. One sources current from AV_{DD} to AINP, the other sinks current from AINM to AV_{SS} for open-circuit detection.

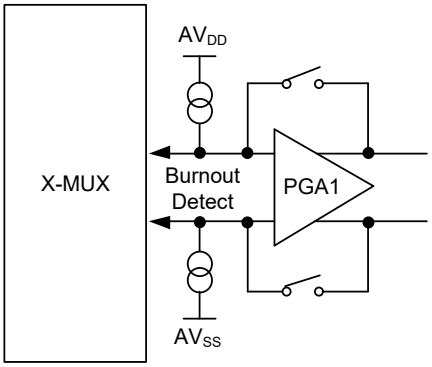


Figure 68. Burnout Currents

The two current sources activate or deactivate synchronously and are configured via the Burnout[1:0] bits. They check transducer status prior to sampling. When enabled, currents flow through the external circuit. A near full-scale reading indicates an open sensor, sensor overload or missing reference with the REF_DET_ERR bit asserted.

Nearly full-scale readings require checking open sensor, overload or missing reference. A 0V reading points to transducer short-circuit. Set the Burnout[1:0] bits to 00 to disable currents for normal operation. The current sources operate within rated input voltage range with buffers enabled.

Temperature Sensor

The built-in die temperature sensor is selected via AINP[4:0] and AINM[4:0] bits in the channel register, measuring the temperature sensor voltage against AV_{SS}. AINM tied to AV_{SS} may trigger the AINM_UV_ERR bit when monitoring temperature; disregard this flag.

Its typical sensitivity is 6405 codes/℃.

Temperature (℃) = ((Conversion - 0x800000)/6405) - 276 (17)

The on-chip temperature sensor features a typical accuracy of ±0.5℃.

Grounding and Layout

The device uses differential analog and reference inputs, offering strong common mode noise rejection. The analog and digital power supplies have independent pins to reduce crosstalk.

The digital filter suppresses broadband supply noise (except harmonics of master clock) and input noise, provided the modulator stays unsaturated. This makes the converter more noise-resistant than traditional high-resolution ADCs.

Given its high-resolution and low inherent noise, strict PCB layout and grounding rules are required: partition analog and digital areas, use solid ground planes for shielding, and route return currents close to signal paths.

Do not route digital traces beneath the chip to avoid die noise coupling; reserve the area under the device for analog ground planes. Use wide power traces for low impedance and fewer glitches. Shield high-speed clock signals with digital ground, keep clocks away from analog inputs, and prevent analog-to-digital trace crossovers. Route traces on opposite PCB layers perpendicularly to minimize crosstalk; micro-strip layout is preferred.

Proper decoupling is critical. Decouple AV_{DD} to AV_{SS} and IOV_{DD} to DGND each with a 1μF tantalum capacitor parallel to a 0.1μF ceramic capacitor. Place the 0.1μF capacitor right next to the chip. Decouple all analog inputs and external reference pins REFINx(+)/REFINx(-) to AV_{SS}.

The integrated LDOs require a 1μF capacitor: connect REGCAPA to AV_{SS} and REGCAPD to DGND. For split-supply operation, implement a dedicated AV_{SS} plane.

REGISTERS MAPS

Table 57. Register Maps

Addr.	Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	R/W
0x00	Communications	nWEN	R/$\overline{W}$	RS[5:0]						0x00	W
0x00	Status	nRDY	ERROR_FLAG	0	POR_FLAG	CH_ACTIVE[3:0]				0x00	R
0x01	ADC_CONTROL	0			DOUT_nRDY_DEL	CONT_READ	DATA_STATUS	nCS_EN	REF_EN	0x0000	R/W
		POWER_MODE[1:0]		Mode[3:0]				CLK_SEL[1:0]			
0x02	Data	Data[23:16]								0x000000	R
		Data[15:8]									
		Data[7:0]									
0x03	IO_CONTROL_1	GPIO_DAT4	GPIO_DAT3	GPIO_DAT2	GPIO_DAT1	GPIO_CTRL4	GPIO_CTRL3	GPIO_CTRL2	GPIO_CTRL1	0x000000	R/W
		PDSW	0	IOUT1[2:0]			IOUT0[2:0]				
		IOUT1_CH[3:0]				IOUT0_CH[3:0]					
0x04	IO_CONTROL_2	VBIAS15	VBIAS14	VBIAS13	VBIAS12	VBIAS11	VBIAS10	VBIAS9	VBIAS8	0x0000	R/W
		VBIAS7	VBIAS6	VBIAS5	VBIAS4	VBIAS3	VBIAS2	VBIAS1	VBIAS0		
0x05	ID	DEVICE_ID[3:0]				SILICON_REVISION[3:0]				0x18	R
0x06	Error	0					ADC_CAL_ERR	ADC_CONV_ERR	ADC_SAT_ERR	0x000000	R
		AINP_OV_ERR	AINP_UV_ERR	AINM_OV_ERR	AINM_UV_ERR	REF_DET_ERR	0	DLDO_PSM_ERR	0		
		ALDO_PSM_ERR	SPI_IGNORE_ERR	SPI_SCLK_CNT_ERR	SPI_READ_ERR	SPI_WRITE_ERR	SPI_CRC_ERR	MM_CRC_ERR	ROM_CRC_ERR		
0x07	ERROR_EN	0	MCLK_CNT_EN	0			ADC_CAL_ERR_EN	ADC_CONV_ERR_EN	ADC_SAT_ERR_EN	0x000040	R/W
		AINP_OV_ERR_EN	AINP_UV_ERR_EN	AINM_OV_ERR_EN	AINM_UV_ERR_EN	REF_DET_ERR_EN	DLDO_PSM_TRIP_TEST_EN	DLDO_PSM_ERR_EN	ALDO_PSM_TRIP_TEST_EN		
		ALDO_PSM_ERR_EN	SPI_IGNORE_ERR_EN	SPI_SCLK_CNT_ERR_EN	SPI_READ_ERR_EN	SPI_WRITE_ERR_EN	SPI_CRC_ERR_EN	MM_CRC_ERR_EN	ROM_CRC_ERR_EN		
0x08	MCLK_COUNT	MCLK_COUNT[7:0]								0x00	R
0x09 to 0x18	CHANNEL_0 to CHANNEL_15	Enable	Setup[2:0]			0		AINP[4:3]		0x8001 (1)	R/W
		AINP[2:0]			AINM[4:0]						
0x19 to 0x20	CONFIG_0 to CONFIG_7	0				Bipolar	Burnout[1:0]		REF_BUFP	0x0860	R/W
		REF_BUFM	AIN_BUFP	AIN_BUFM	REF_SEL[1:0]		PGA[2:0]				
0x21 to 0x28	FILTER_0 to FILTER_7	Filter[2:0]			REJ60	POST_FILTER[2:0]			SINGLE_CYCLE	0x060180	R/W
		0					FS[10:8]				
		FS[7:0]									
0x29 to 0x30	OFFSET_0 to OFFSET_7	Offset[23:16]								0x800000	R/W
		Offset[15:8]									
		Offset[7:0]									
0x31 to 0x38	GAIN_0 to GAIN_7	Gain[23:16]								0x555555	R/W
		Gain[15:8]									
		Gain[7:0]									

NOTE:

1. The CHANNEL_0 register is reset to 0x8001. All the other channels are reset to 0x0001.

REGISTER MAPS (continued)

REG0x00: Communications Register [Reset = 0x00]

BITS	BIT NAME	TYPE	DESCRIPTION
D[7]	nWEN	W	Write Enable Bit The bit must be set to 0, so that a write operation to the communication registers to actually take place. If a value of 1 is initially written, the device will not clock in any subsequent bits into the register; it will remain latched at this bit until a value of 0 is written. Once a value of 0 is written to the nWEN bit, the subsequent 7 bits are then loaded into the communication register.
D[6]	R/$\overline{W}$	W	0 = The next operation is a write to a specified register 1 = The next operation is a read from the designated register
D[5:0]	RS[5:0]	W	Register Address Bits These bits select which ADC registers are being selected during the serial interface communication. Refer to Table 57.

REG0x00: Status Register [Power-On/Reset = 0x00]

BITS	BIT NAME	TYPE	DESCRIPTION
D[7]	nRDY	R	Ready Bit for the ADC The bit clears when the data is written to the ADC data register. The nRDY bit sets automatically in three cases: 1) after the ADC data register is read. 2) a while before the register gets the new conversion data (to warn against reading). 3) when the device enters power-down/standby mode. The DOUT/nRDY pin also signals the conversion end, serving as an alternative to the status register for monitoring ADC conversion data.
D[6]	ERROR_FLAG	R	ADC Error Bit The bit shows if any error bit in the error register is asserted. It is high when one or more error bits are set, and clears upon reading the error register.
D[5]	0	R	The bit is set to 0.
D[4]	POR_FLAG	R	Power-On Reset Flag The bit indicates a power-on reset, which happens on power-up, when the supply voltage drops below the threshold, during reset execution, or when exiting the power-down mode. The bit clears only after reading the status register.
D[3:0]	CH_ACTIVE[3:0]	R	These bits identify the channel that the ADC is converting. 0000 = Channel 0 0001 = Channel 1 0010 = Channel 2 0011 = Channel 3 0100 = Channel 4 0101 = Channel 5 0110 = Channel 6 0111 = Channel 7 1000 = Channel 8 1001 = Channel 9 1010 = Channel 10 1011 = Channel 11 1100 = Channel 12 1101 = Channel 13 1110 = Channel 14 1111 = Channel 15

REGISTER MAPS (continued)

REG0x01: ADC Control (ADC_CONTROL) Register [Power-On/Reset = 0x0000]

BITS	BIT NAME	TYPE	DESCRIPTION
D[15:13]	000	R/W	These bits must be set to 0.
D[12]	DOUT_nRDY_DEL	R/W	The bit controls the SCLK inactive edge to DOUT_nRDY high time. 0 = The delay is 10ns minimum 1 = The delay is increased to 100ns minimum This function is useful when nCS is tied low (the nCS_EN bit is set to 0).
D[11]	CONT_READ	R/W	Data Register Continuous Read When the bit is set to 1 (with the data register selected), the serial interface enables continuous reading of the data register. Specifically, after nRDY goes low (indicating the conversion completion), the SCLK pulses will automatically put the data register contents on the DOUT pin. No rewrite to the communications register is needed for subsequent data reads. - Enable continuous read: Set the CONT_READ bit. - Disable continuous read: Write a read data command while DOUT/nRDY is low. With the continuous read enabled, the ADC monitors DIN for the disable instruction. Also, 64 consecutive 1s on DIN trigger a reset—keep DIN low until an instruction is written.
D[10]	DATA_STATUS	R/W	The bit enables status register transmission post each data register read. When the DATA_STATUS bit is set, status register contents are sent with every data register read. This function benefits multi-channel selection, as the status register identifies which channel the data register value corresponds to.
D[9]	nCS_EN	R/W	The bit controls the operation of the DOUT/nRDY pin during data read operations. 0 = The DOUT pin returns to being an nRDY pin within nanoseconds of the SCLK inactive edge (the delay is determined by the DOUT_nRDY_DEL bit) 1 = Continue to output the LSB of the register being read until nCS is taken high When the nCS_EN bit is set, all read operations must be framed by nCS. The nCS_EN bit must be set to use diagnostic functions: SPI_WRITE_ERR, SPI_READ_ERR, and SPI_SCLK_CNT_ERR.
D[8]	REF_EN	R/W	Internal Reference Voltage Enable 0 = The internal reference is disabled 1 = The internal reference is enabled and available at the REFOUT pin
D[7:6]	POWER_MODE[1:0]	R/W	Power Mode Select 00 = Low power 01 = Mid power 10 = Full power 11 = Full power The current consumption and output data rate ranges depend on power mode.
D[5:2]	Mode[3:0]	R/W	ADC Operation Mode Control Bit See Table 58.
D[1:0]	CLK_SEL[1:0]	R/W	ADC Clock Source Select (SGM52421R8 Only) 00 = Internal 614.4kHz clock. The internal clock is not available at the CLK pin 01 = Internal 614.4kHz clock. This clock is available at the CLK pin 10 = External 614.4kHz clock 11 = External clock. The external clock is divided by 4 within the SGM52421R8 The SGM52421R8 supports either its on-chip 614.4kHz clock or an external clock. An external clock enables synchronization of multiple such devices and improves 50Hz/60Hz rejection when driving the ADC accurately.

REGISTER MAPS (continued)

Table 58. Operating Modes

Mode[3:0] Bits	Description
0000	Continuous Conversion Mode (default). In continuous conversion mode, the ADC runs conversions nonstop and stores results in the data register; nRDY goes low upon conversion completion. Users can read results in two ways: - Enter continuous read mode, where SCLK pulses auto-place conversions on DOUT. - Write to the communications register to trigger ADC output. After power-on reset, or ADC reconfiguration, the filter needs full settling time for the first valid conversion. Subsequent conversions follow the selected output data rate (dependent on filter choice).
0001	Single Conversion Mode. In single conversion mode, the ADC powers up, runs one conversion on the selected channel (needing full filter settling time), then stores the result in the data register. nRDY goes low, the ADC returns to standby mode. The result stays in the data register, and nRDY remains low until the data is read or a new conversion starts.
0010	Standby Mode. In standby mode, all SGM52421R8/SGM52421R8A sections power down except LDOs. The internal reference, on-chip oscillator, low-side power switch, and bias voltage generator can be enabled/disabled here. The on-chip registers retain contents. Enabled diagnostics stay active (and can be toggled) in standby mode. However, diagnostics needing the master clock (reference detect, UV/OV detection, LDO trip tests, memory map CRC, MCLK counter) must be enabled in continuous conversion or idle mode—they won't work if enabled in standby.
0011	Power-Down Mode. In power-down mode, all SGM52421R8/SGM52421R8A circuits power down, including the current sources, power switch, burnout currents, bias generator, clock circuitry, and LDOs. The on-chip registers lose their contents, requiring full reprogramming when exiting this mode.
0100	Idle Mode. In idle mode, the ADC filter and modulator are held in a reset state even though the modulator clocks continue to be provided. In idle mode, the ADC filter and modulator stay reset, though modulator clocks persist.
0101	Internal Zero-Scale (Offset) Calibration. An internal short auto-connects to the input. nRDY goes high on calibration start and low when done. Post-calibration, the ADC enters idle mode. The measured offset coefficient is stored in the selected channel's offset register. Select only one channel for zero-scale calibration, which takes one settling period.
0110	Internal Full-Scale (Gain) Calibration. A full-scale input voltage auto-connects to the selected analog input for calibration. nRDY goes high on calibration start and low when complete. Post-calibration, the ADC enters idle mode, and the measured full-scale coefficient is stored in the selected channel's gain register. Full-scale calibration is required after a channel's gain change to minimize full-scale error; select only one channel. The SGM52421R8/SGM52421R8A are factory-calibrated at gain 1, with no support for further calibrations at this gain. Internal full-scale calibration (gain > 1) takes four settling periods and is unavailable in full power mode—switch to mid/low power mode for it (calibration remains valid in full power mode due to shared reference/gain). Internal full-scale calibration must precede zero-scale calibration. Thus, write 0x800000 to the offset register to reset it before any full-scale calibration.
0111	System Zero-Scale (Offset) Calibration. Connect the system zero-scale input to the selected channel's input pins. nRDY goes high on calibration start and low when complete. Post-calibration, the ADC enters idle mode, and the measured offset coefficient is stored in the channel's offset register. System zero-scale calibration is required after a channel's gain change. Select only one channel. It takes one settling period.
1000	System Full-Scale (Gain) Calibration. Connect the system full-scale input to the selected channel's input pins. nRDY goes high on calibration start and low when complete. Post-calibration, the ADC enters idle mode, and the measured full-scale coefficient is stored in the channel's gain register. System full-scale calibration is required after a channel's gain change. Select only one channel. It takes one settling period.
1001 to1111	Reserved.

REGISTER MAPS (continued)

REG0x02: Data Register [Power-On/Reset = 0x000000]

BITS	BIT NAME	TYPE	DESCRIPTION
D[23:0]	Data[23:0]	R	The data register is used to store the conversion results of the ADC. It is a read-only register. When the read operation from this register is completed, the nRDY bit/pin is set.

REG0x03: IO_CONTROL_1 Register [Power-On/Reset = 0x000000]

BITS	BIT NAME	TYPE	DESCRIPTION
D[23]	GPIO_DAT4	R/W	Digital Output P4 When the GPIO_CTRL4 bit is set, the GPIO_DAT4 bit determines P4's output: high for high P4, low for low P4. Reading IO_CONTROL_1 register then shows P4's status via the GPIO_DAT4 bit.
D[22]	GPIO_DAT3	R/W	Digital Output P3 When the GPIO_CTRL3 bit is set, the GPIO_DAT3 bit determines P3's output: high for high P3, low for low P3. Reading IO_CONTROL_1 register then shows P3's status via the GPIO_DAT3 bit.
D[21]	GPIO_DAT2	R/W	Digital Output P2 When the GPIO_CTRL2 bit is set, the GPIO_DAT2 bit determines P2's output: high for high P2, low for low P2. Reading IO_CONTROL_1 register then shows P2's status via the GPIO_DAT2 bit.
D[20]	GPIO_DAT1	R/W	Digital Output P1 When the GPIO_CTRL1 bit is set, the GPIO_DAT1 bit determines P1's output: high for high P1, low for low P1. Reading IO_CONTROL_1 register then shows P1's status via the GPIO_DAT1 bit.
D[19]	GPIO_CTRL4	R/W	Digital Output P4 Enable 0 = Pin acts as analog input AIN5 1 = Digital output P4 is active
D[18]	GPIO_CTRL3	R/W	Digital Output P3 Enable 0 = Pin acts as analog input AIN4 1 = Digital output P3 is active
D[17]	GPIO_CTRL2	R/W	Digital Output P2 Enable 0 = Pin acts as analog input AIN3 1 = Digital output P2 is active
D[16]	GPIO_CTRL1	R/W	Digital Output P1 Enable 0 = Pin acts as analog input AIN2 1 = Digital output P1 is active
D[15]	PDSW	R/W	Bridge Power-Down Switch Control Bit Set the bit to close bridge power-down switch (PDSW) to AGND (sinks up to 30mA). Clear the bit to open it. The PDSW stays active when ADC is in standby.
D[14]	0	R/W	The bit must be set to 0.
D[13:11]	IOUT1[2:0]	R/W	Set the value of the excitation current for IOUT1. 000 = Off 001 = 50μA 010 = 100μA 011 = 250μA 100 = 500μA 101 = 750μA 110 = 1000μA 111 = 1500μA
D[10:8]	IOUT0[2:0]	R/W	Set the value of the excitation current for IOUT0. 000 = Off 001 = 50μA 010 = 100μA 011 = 250μA 100 = 500μA 101 = 750μA 110 = 1000μA 111 = 1500μA

REGISTER MAPS (continued)

REG0x03: IO_CONTROL_1 Register [Power-On/Reset = 0x000000] (continued)

BITS	BIT NAME	TYPE	DESCRIPTION
D[7:4]	IOUT1_CH[3:0]	R/W	Channel Select Bits for the Excitation Current for IOUT1 0000 = IOUT1 is available on the AIN0 pin 0001 = IOUT1 is available on the AIN1 pin 0010 = IOUT1 is available on the AIN2 pin 0011 = IOUT1 is available on the AIN3 pin 0100 = IOUT1 is available on the AIN4 pin 0101 = IOUT1 is available on the AIN5 pin 0110 = IOUT1 is available on the AIN6 pin 0111 = IOUT1 is available on the AIN7 pin 1000 = IOUT1 is available on the AIN8 pin 1001 = IOUT1 is available on the AIN9 pin 1010 = IOUT1 is available on the AIN10 pin 1011 = IOUT1 is available on the AIN11 pin 1100 = IOUT1 is available on the AIN12 pin 1101 = IOUT1 is available on the AIN13 pin 1110 = IOUT1 is available on the AIN14 pin 0111 = IOUT1 is available on the AIN15 pin
D[3:0]	IOUT0_CH[3:0]	R/W	Channel Select Bits for the Excitation Current for IOUT0 0000 = IOUT0 is available on the AIN0 pin 0001 = IOUT0 is available on the AIN1 pin 0010 = IOUT0 is available on the AIN2 pin 0011 = IOUT0 is available on the AIN3 pin 0100 = IOUT0 is available on the AIN4 pin 0101 = IOUT0 is available on the AIN5 pin 0110 = IOUT0 is available on the AIN6 pin 0111 = IOUT0 is available on the AIN7 pin 1000 = IOUT0 is available on the AIN8 pin 1001 = IOUT0 is available on the AIN9 pin 1010 = IOUT0 is available on the AIN10 pin 1011 = IOUT0 is available on the AIN11 pin 1100 = IOUT0 is available on the AIN12 pin 1101 = IOUT0 is available on the AIN13 pin 1110 = IOUT0 is available on the AIN14 pin 1111 = IOUT0 is available on the AIN15 pin

REGISTER MAPS (continued)

REG0x04: IO_CONTROL_2 Register [Power-On/Reset = 0x0000]

BITS	BIT NAME	TYPE	DESCRIPTION
D[15]	VBIAS15	R/W	Enable the bias voltage on the AIN15 channel. The internal bias voltage is available on AIN15 when the bit is set.
D[14]	VBIAS14	R/W	Enable the bias voltage on the AIN14 channel. The internal bias voltage is available on AIN14 when the bit is set.
D[13]	VBIAS13	R/W	Enable the bias voltage on the AIN13 channel. The internal bias voltage is available on AIN13 when the bit is set.
D[12]	VBIAS12	R/W	Enable the bias voltage on the AIN12 channel. The internal bias voltage is available on AIN12 when the bit is set.
D[11]	VBIAS11	R/W	Enable the bias voltage on the AIN11 channel. The internal bias voltage is available on AIN11 when the bit is set.
D[10]	VBIAS10	R/W	Enable the bias voltage on the AIN10 channel. The internal bias voltage is available on AIN10 when the bit is set.
D[9]	VBIAS9	R/W	Enable the bias voltage on the AIN9 channel. The internal bias voltage is available on AIN9 when the bit is set.
D[8]	VBIAS8	R/W	Enable the bias voltage on the AIN8 channel. The internal bias voltage is available on AIN8 when the bit is set.
D[7]	VBIAS7	R/W	Enable the bias voltage on the AIN7 channel. The internal bias voltage is available on AIN7 when the bit is set.
D[6]	VBIAS6	R/W	Enable the bias voltage on the AIN6 channel. The internal bias voltage is available on AIN6 when the bit is set.
D[5]	VBIAS5	R/W	Enable the bias voltage on the AIN5 channel. The internal bias voltage is available on AIN5 when the bit is set.
D[4]	VBIAS4	R/W	Enable the bias voltage on the AIN4 channel. The internal bias voltage is available on AIN4 when the bit is set.
D[3]	VBIAS3	R/W	Enable the bias voltage on the AIN3 channel. The internal bias voltage is available on AIN3 when the bit is set.
D[2]	VBIAS2	R/W	Enable the bias voltage on the AIN2 channel. The internal bias voltage is available on AIN2 when the bit is set.
D[1]	VBIAS1	R/W	Enable the bias voltage on the AIN1 channel. The internal bias voltage is available on AIN1 when the bit is set.
D[0]	VBIAS0	R/W	Enable the bias voltage on the AIN0 channel. The internal bias voltage is available on AIN0 when the bit is set.

REG0x05: ID Register [Power-On/Reset = 0x18]

BITS	BIT NAME	TYPE	DESCRIPTION
D[7:4]	DEVICE_ID[3:0]	R	The ID register is used to store the identification number of the device. It is a read-only register.
D[3:0]	SILICON_ REVISION[3:0]	R	

REGISTER MAPS (continued)

REG0x06: Error Register [Power-On/Reset = 0x000000]

BITS	BIT NAME	TYPE	DESCRIPTION
D[23:19]	00000	R	These bits must be set to 0.
D[18]	ADC_CAL_ERR	R	Calibration Check This flag is set if the calibration starts but doesn't complete, indicating an error. The related calibration register remains updated.
D[17]	ADC_CONV_ERR	R	The bit indicates conversion validity. It is set if a conversion error occurs.
D[16]	ADC_SAT_ERR	R	ADC Saturation Flag This flag is set if the modulator saturates during conversion.
D[15]	AINP_OV_ERR	R	Over-Voltage Detection on AINP.
D[14]	AINP_UV_ERR	R	Under-Voltage Detection on AINP.
D[13]	AINM_OV_ERR	R	Over-Voltage Detection on AINM.
D[12]	AINM_UV_ERR	R	Under-Voltage Detection on AINM.
D[11]	REF_DET_ERR	R	Reference Detection This flag indicates if the ADC's external reference is open-circuited or below 0.45V.
D[10]	0	R	The bit must be set to 0.
D[9]	DLDO_PSM_ERR	R	Digital LDO error. This flag sets if a digital LDO error is detected.
D[8]	0	R	The bit must be set to 0.
D[7]	ALDO_PSM_ERR	R	Analog LDO Error This flag is set if an error is detected with the analog LDO voltage.
D[6]	SPI_IGNORE_ERR	R	During power-on reset and calibrations, on-chip registers are unwritable—user write instructions are ignored by the ADC. This bit is set to indicate the ADC is busy and the write instruction was ignored. The SPI_IGNORE_ERR bit clears when read.
D[5]	SPI_SCLK_CNT_ERR	R	All serial communications use multiples of eight bits. The bit is set when the number of SCLK cycles is not a multiple of eight.
D[4]	SPI_READ_ERR	R	The bit is set when an error occurs during an SPI read operation.
D[3]	SPI_WRITE_ERR	R	The bit is set when an error occurs during an SPI write operation.
D[2]	SPI_CRC_ERR	R	The bit is set if an error occurs in the CRC check of the serial communications.
D[1]	MM_CRC_ERR	R	Memory Map Error A CRC calculation runs on the memory map whenever the registers are written to. Periodic CRC checks then occur on on-chip registers. If the register contents change, the MM_CRC_ERR bit is set.
D[0]	ROM_CRC_ERR	R	ROM Error A CRC calculation is performed on the ROM contents (which store the default register values) during power-up. If the ROM contents have changed, the ROM_CRC_ERR bit is set.

REGISTER MAPS (continued)

REG0x07: ERROR_EN Register [Power-On/Reset = 0x000040]

BITS	BIT NAME	TYPE	DESCRIPTION
D[23]	0	R/W	The bit must be set to 0.
D[22]	MCLK_CNT_EN	R/W	Master Clock Counter When set, this bit enables the master clock counter, whose result is reported in the MCLK_COUNT register. The counter monitors the ADC's master clock—external if used, or the on-chip oscillator if selected as the source.
D[21:19]	000	R/W	These bits must be set to 0.
D[18]	ADC_CAL_ERR_EN	R/W	When set, this bit enables the calibration fail check.
D[17]	ADC_CONV_ERR_EN	R/W	When set, this bit monitors conversions and sets the ADC_CONV_ERR bit on failure.
D[16]	ADC_SAT_ERR_EN	R/W	When set, this bit enables the ADC modulator saturation check.
D[15]	AINP_OV_ERR_EN	R/W	When set, this bit enables the over-voltage monitor on all active AINP channels.
D[14]	AINP_UV_ERR_EN	R/W	When set, this bit enables the under-voltage monitor on all active AINP channels.
D[13]	AINM_OV_ERR_EN	R/W	When set, this bit enables the over-voltage monitor on all active AINM channels.
D[12]	AINM_UV_ERR_EN	R/W	When set, this bit enables the under-voltage monitor on all active AINM channels.
D[11]	REF_DET_ERR_EN	R/W	When set, this bit continuously monitors the ADC's external reference, flagging errors for open circuits or values < 0.45V.
D[10]	DLDO_PSM_TRIP_TEST_EN	R/W	Check the digital LDO monitoring test mechanism. When set, this bit ties the test circuit input to DGND (instead of LDO output) and sets the DLDO_PSM_ERR bit in the error register.
D[9]	DLDO_PSM_ERR_EN	R/W	When set, this bit continuously monitors the digital LDO voltage, setting the DLDO_PSM_ERR bit in the error register if the output is out of specification.
D[8]	ALDO_PSM_TRIP_TEST_EN	R/W	Check the analog LDO monitoring test mechanism. When set, this bit ties the test circuit input to AV_{SS} (instead of LDO output) and sets the ALDO_PSM_ERR bit in the error register.
D[7]	ALDO_PSM_ERR_EN	R/W	When set, this bit continuously monitors the analog LDO voltage, setting the ALDO_PSM_ERR bit in the error register if the output is out of specification.
D[6]	SPI_IGNORE_ERR_EN	R/W	During power-on reset and calibrations, on-chip registers are unwritable (ADC ignores user writes). Set this bit to have the SPI_IGNORE_ERR bit in the error register notify users of ignored writes.
D[5]	SPI_SCLK_CNT_ERR_EN	R/W	When set, this bit enables the SCLK counter. All ADC read/write operations use 8-bit multiples. The counter tracks SCLK pulses per serial communication, framed by nCS. If pulses aren't 8-bit multiples, the SPI_SCLK_CNT_ERR bit sets (e.g., for SCLK glitches causing excess pulses). The nCS_EN bit in ADC_CONTROL register must be 1 when using this function.
D[4]	SPI_READ_ERR_EN	R/W	When set, this bit triggers the SPI_READ_ERR bit in the error register on read errors (e.g., reading invalid addresses). The nCS_EN bit in ADC_CONTROL register must be 1 when using this function.
D[3]	SPI_WRITE_ERR_EN	R/W	When set, this bit triggers the SPI_WRITE_ERR bit in the error register on write errors (e.g., writing to invalid addresses or read-only registers). The nCS_EN bit in ADC_CONTROL register must be 1 when using this function.
D[2]	SPI_CRC_ERR_EN	R/W	When set, this bit enables CRC checking for all read and write operations. The SPI_CRC_ERR bit in the error register is set upon CRC check failure. Additionally, an 8-bit CRC word is appended to all data read from the SGM52421R8/SGM52421R8A.
D[1]	MM_CRC_ERR_EN	R/W	When set, this bit triggers a CRC calculation on the memory map each time that the registers are written to, followed by periodic CRC checks on on-chip registers. The MM_CRC_ERR bit is set if register contents change.
D[0]	ROM_CRC_ERR_EN	R/W	When set, this bit initiates a CRC calculation on ROM contents during power-on. The ROM_CRC_ERR bit is set if ROM contents have changed.

REGISTER MAPS (continued)

REG0x08: MCLK_COUNT Register [Power-On/Reset = 0x00]

BITS	BIT NAME	TYPE	DESCRIPTION
D[7:0]	MCLK_COUNT[7:0]	R	This register enables users to determine the frequency of the internal/external oscillator. Internally, a clock counter increments every 131 pulses of the sampling clock (614.4kHz in full power mode, 153.6kHz in mid power mode, and 768kHz in low power mode). The 8-bit counter overflows when reaching its maximum value and its output is readable via this register. Note that the register incrementation is asynchronous to read operations. If a read coincides with an increment, an invalid value may be returned. To prevent this: 1. Read the register four times consecutively. 2. Repeat the four-read sequence at a later point. 3. Compare the two sets of readings to identify valid values at both timing instants.

REG0x09 to REG0x18: Channel Registers (CHANNEL_0 to CHANNEL_15) [Power-On/Reset = 0x8001 for CHANNEL_0, All Other Channel Registers are Set to 0x0001]

BITS	BIT NAME	TYPE	DESCRIPTION
D[15]	Enable	R/W	Channel Enable Bit Setting this bit enables the channel for conversion. By default, only Channel 0 is enabled. Conversions start at the lowest enabled channel, cycle upward, then wrap to the lowest. When the ADC outputs a channel's result, the status register's 4 LSBs show its number (0-15) for identification. With the ADC_CONTROL register's DATA_STATUS bit set, the status register's contents are appended to each read result—use this to match values to channels when multiple are enabled.
D[14:12]	Setup[2:0]	R/W	Setup Select These bits select one of eight setups to configure the ADC for the channel. A setup includes four registers: analog config, output data rate/filter, offset, and gain. All active channels can share a setup (same 3-bit value) or up to eight channels can have unique configurations.
D[11:10]	00	R/W	These bits must be set to 0.
D[9:5]	AINP[4:0]	R/W	Positive Analog Input AINP Input Select These bits select the analog input connected to the channel's positive input. 00000 = AIN0 (default) 00001 = AIN1 00010 = AIN2 00011 = AIN3 00100 = AIN4 00101 = AIN5 00110 = AIN6 00111 = AIN7 01000 = AIN8 01001 = AIN9 01010 = AIN10 01011 = AIN11 01100 = AIN12 01101 = AIN13 01110 = AIN14 01111 = AIN15 10000 = Temperature sensor 10001 = AV_{SS} 10010 = Internal reference 10011 = DGND 10100 = (AV_{DD} - AV_{SS})/6+. Use in conjunction with (AV_{DD} - AV_{SS})/6- to monitor supply AV_{DD} - AV_{SS} 10101 = (AV_{DD} - AV_{SS})/6-. Use in conjunction with (AV_{DD} - AV_{SS})/6+ to monitor supply AV_{DD} - AV_{SS} 10110 = (IOV_{DD} - DGND)/6+. Use in conjunction with (IOV_{DD} - DGND)/6- to monitor IOV_{DD} - DGND 10111 = (IOV_{DD} - DGND)/6-. Use in conjunction with (IOV_{DD} - DGND)/6+ to monitor IOV_{DD} - DGND 11000 = (ALDO - AV_{SS})/6+. Use in conjunction with (ALDO - AV_{SS})/6- to monitor the analog LDO 11001 = (ALDO - AV_{SS})/6-. Use in conjunction with (ALDO - AV_{SS})/6+ to monitor the analog LDO 11010 = (DLDO - DGND)/6+. Use in conjunction with (DLDO - DGND)/6- to monitor the digital LDO 11011 = (DLDO - DGND)/6-. Use in conjunction with (DLDO - DGND)/6+ to monitor the digital LDO 11100 = V_20MV_P. Use in conjunction with V_20MV_M to apply a 20mV_{P-P} signal to the ADC 11101 = V_20MV_M. Use in conjunction with V_20MV_P to apply a 20mV_{P-P} signal to the ADC 11110 = Reserved 11111 = Reserved

REGISTER MAPS (continued)

REG0x09 to REG0x18: Channel Registers (CHANNEL_0 to CHANNEL_15) [Power-On/Reset = 0x8001 for CHANNEL_0, All Other Channel Registers are Set to 0x0001] (continued)

BITS	BIT NAME	TYPE	DESCRIPTION
D[4:0]	AINM[4:0]	R/W	Negative Analog Input AINM Input Select These bits select the analog input connected to the channel's negative input. 00000 = AIN0 00001 = AIN1 (default) 00010 = AIN2 00011 = AIN3 00100 = AIN4 00101 = AIN5 00110 = AIN6 00111 = AIN7 01000 = AIN8 01001 = AIN9 01010 = AIN10 01011 = AIN11 01100 = AIN12 01101 = AIN13 01110 = AIN14 01111 = AIN15 10000 = Temperature sensor 10001 = AV_{SS} 10010 = Internal reference 10011 = DGND 10100 = (AV_{DD} - AV_{SS})/6+. Use in conjunction with (AV_{DD} - AV_{SS})/6- to monitor supply AV_{DD} - AV_{SS} 10101 = (AV_{DD} - AV_{SS})/6-. Use in conjunction with (AV_{DD} - AV_{SS})/6+ to monitor supply AV_{DD} - AV_{SS} 10110 = (IOV_{DD} - DGND)/6+. Use in conjunction with (IOV_{DD} - DGND)/6- to monitor IOV_{DD} - DGND 10111 = (IOV_{DD} - DGND)/6-. Use in conjunction with (IOV_{DD} - DGND)/6+ to monitor IOV_{DD} - DGND 11000 = (ALDO - AV_{SS})/6+. Use in conjunction with (ALDO - AV_{SS})/6- to monitor the analog LDO 11001 = (ALDO - AV_{SS})/6-. Use in conjunction with (ALDO - AV_{SS})/6+ to monitor the analog LDO 11010 = (DLDO - DGND)/6+. Use in conjunction with (DLDO - DGND)/6- to monitor the digital LDO 11011 = (DLDO - DGND)/6-. Use in conjunction with (DLDO - DGND)/6+ to monitor the digital LDO 11100 = V_20MV_P. Use in conjunction with V_20MV_M to apply a 20mV_{P-P} signal to the ADC 11101 = V_20MV_M. Use in conjunction with V_20MV_P to apply a 20mV_{P-P} signal to the ADC 11110 = Reserved 11111 = Reserved

REGISTER MAPS (continued)

REG0x19 to REG0x20: Configuration Registers (CONFIG_0 to CONFIG_7) [Power-On/Reset = 0x0860]

BITS	BIT NAME	TYPE	DESCRIPTION
D[15:12]	0000	R/W	These bits must be set to 0.
D[11]	Bipolar	R/W	Polarity Select Bit Setting this bit selects bipolar operation. Clearing it selects unipolar operation.
D[10:9]	Burnout[1:0]	R/W	These bits select the magnitude of the sensor burnout detect current source. 00 = Burnout current source off (default) 01 = Burnout current source on, 0.5μA 10 = Burnout current source on, 2μA 11 = Burnout current source on, 4μA
D[8]	REF_BUFP	R/W	Buffer Enable on REFINx(+) Setting this bit buffers the positive reference input (internal/external). Clearing it leaves it unbuffered.
D[7]	REF_BUFM	R/W	Buffer Enable on REFINx(-) Setting this bit buffers the negative reference input (internal/external). Clearing it leaves it unbuffered.
D[6]	AIN_BUFP	R/W	Buffer Enable on AINP Setting this bit buffers the selected positive analog input pin. Clearing it leaves it unbuffered.
D[5]	AIN_BUFM	R/W	Buffer Enable on AINM Setting this bit buffers the selected negative analog input pin. Clearing it leaves it unbuffered.
D[4:3]	REF_SEL[1:0]	R/W	Reference Source Select Bits These bits determine the reference source utilized for conversions on all channels that rely on this configuration register. 00 = REFIN1(+)/REFIN1(-) 01 = REFIN2(+)/REFIN2(-) 10 = Internal reference 11 = AV_{DD}
D[2:0]	PGA[2:0]	R/W	Gain Select Bits These bits select the gain for conversions on all channels using this configuration register. See Table 59.

Table 59. PGA[2:0] Bits Details

PGA[2:0]	Gain	Input Range When V_{REF} = 2.5V (Bipolar Mode)
000	1	±2.5V
001	2	±1.25V
010	4	± 625mV
011	8	±312.5mV
100	16	±156.25mV
101	32	±78.125mV
110	64	±39.06mV
111	128	±19.53mV

REGISTER MAPS (continued)

REG0x21 to REG0x28: Filter Registers (FILTER_0 to FILTER_7) [Power-On/Reset = 0x060180]

BITS	BIT NAME	TYPE	DESCRIPTION
D[23:21]	Filter[2:0]	R/W	Filter Type Select Bits These bits select the filter type. 000 = $Sinc^4$ filter (default) 001 = Reserved 010 = $Sinc^3$ filter 011 = Reserved 100 = Fast settling with $sinc^4$ filter, followed by an averaging block (settling time = conversion time). Averages by 16 in full/mid power modes, 8 in low power mode 101 = Fast settling with $sinc^3$ filter, followed by an averaging block (settling time = conversion time). Averages by 16 in full/mid power modes, 8 in low power mode 110 = Reserved 111 = Post filter enabled The SGM52421R8/SGM52421R8A have selectable post filters (via the POST_FILTER[2:0] bits). They feature single-cycle settling (far better than basic $sinc^3$/$sinc^4$ filters) and excellent 50Hz/60Hz rejection.
D[20]	REJ60	R/W	Setting this bit adds a 60Hz first-order notch when the sinc filter's first notch is at 50Hz, enabling simultaneous 50Hz/60Hz rejection.
D[19:17]	POST_FILTER[2:0]	R/W	Post Filter Type Select Bits When filter bits = 1, the $sinc^3$ filter is followed by a post filter with good 50Hz/60Hz rejection and near-zero latency at output data rates. See Table 60.
D[16]	SINGLE_CYCLE	R/W	Single Cycle Conversion Enable Bit Setting this bit makes the SGM52421R8/SGM52421R8A settle in one conversion cycle, acting as a zero latency ADC. It has no effect with multiple enabled channels, single conversion mode, or fast filters.
D[15:11]	00000	R/W	These bits must be set to 0.
D[10:0]	FS[10:0]	R/W	Filter Output Data Rate Select Bits These bits set the output data rate for $sinc^3$, $sinc^4$, and fast settling filters. They also affect the sinc filter's first notch position, cutoff frequency, and (with gain selection) output noise—thus determining effective resolution (see noise tables). The FS range is from 1 to 2047.

Table 60. POST_FILTER[2:0] Bits Details

POST_FILTER[2:0]	Output Data Rate (SPS)	Rejection at 50Hz and 60Hz ± 1Hz (dB)
000	Reserved	Not applicable
010	Reserved	Not applicable
010	27.27	47
011	25	62
100	Reserved	Not applicable
101	20	86
110	16.7	92
111	Reserved	Not applicable

REGISTER MAPS (continued)

REG0x29 to REG0x30: Offset Registers (OFFSET_0 to OFFSET_7) [Power-On/Reset = 0x800000]

The SGM52421R8/SGM52421R8A feature eight offset registers, labeled OFFSET_0 through OFFSET_7. Each offset register corresponds to a specific setting, where OFFSET_x is associated with setting x. These offset registers are 24-bit read/write registers that store the offset calibration factor for the ADC, with a default power-on reset value of 0x800000. The offset registers function in conjunction with their corresponding gain registers to form register pairs. If the user initiates either an internal or system zero-scale calibration, the power-on reset value will be automatically overwritten. When writing to the offset register, it is necessary to place the ADC in standby or idle mode.

REG0x31 to REG0x38: Gain Registers (GAIN_0 to GAIN_7) [Power-On/Reset = 0x555555]

The SGM52421R8/SGM52421R8A feature eight gain registers, labeled GAIN_0 through GAIN_7. Each gain register corresponds to a specific setting, where GAIN_x is associated with setting x. These gain registers are 24-bit and store the full-scale calibration coefficient for the analog-to-digital converter (ADC). The SGM52421R8/ SGM52421R8A undergo factory calibration to a gain of 1. Upon power-on or after a reset, the gain registers contain the factory-calibrated value. These registers are both readable and writable. However, when writing to these registers, the ADC must be placed in either standby mode or idle mode. Additionally, the default value will be automatically overwritten if an internal or system full-scale calibration is initiated by the user or if the full-scale registers are modified.

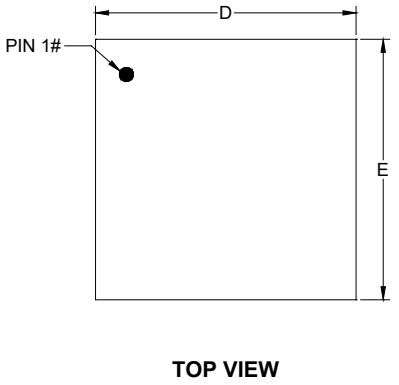
REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

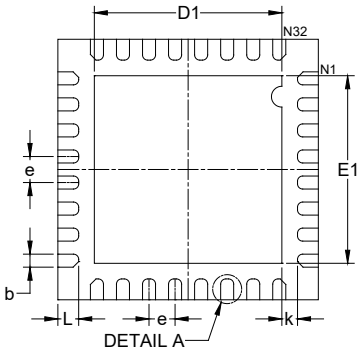
Changes from Original to REV.A (JUNE 2026)	Page
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

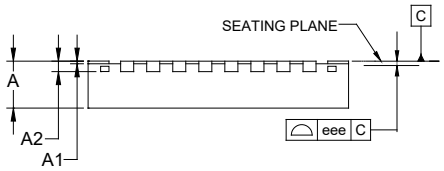
TQFN-5×5-32IL



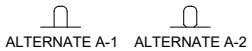
TOP VIEW



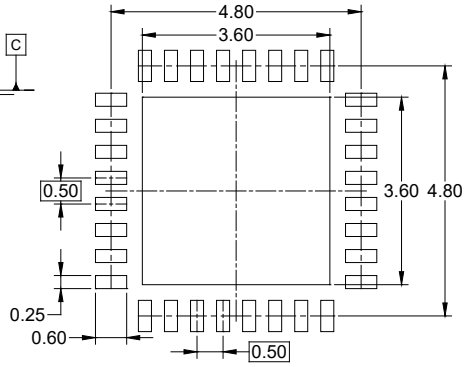
BOTTOM VIEW



SIDE VIEW



DETAIL A
ALTERNATE TERMINAL CONSTRUCTION



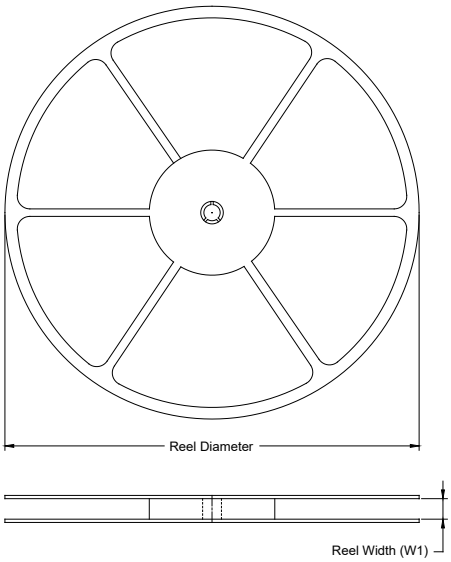
RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	0.850	-	0.950
A1	0.000	-	0.050
A2	0.200 REF		
b	0.200	-	0.300
D	4.900	-	5.100
E	4.900	-	5.100
D1	3.500	-	3.700
E1	3.500	-	3.700
e	0.500 BSC		
L	0.300	-	0.500
k	0.200 MIN		
eee	0.080		

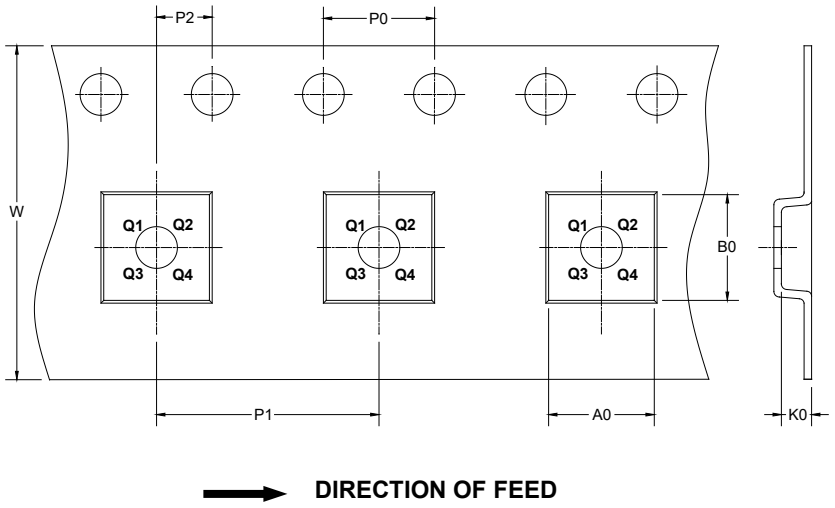
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



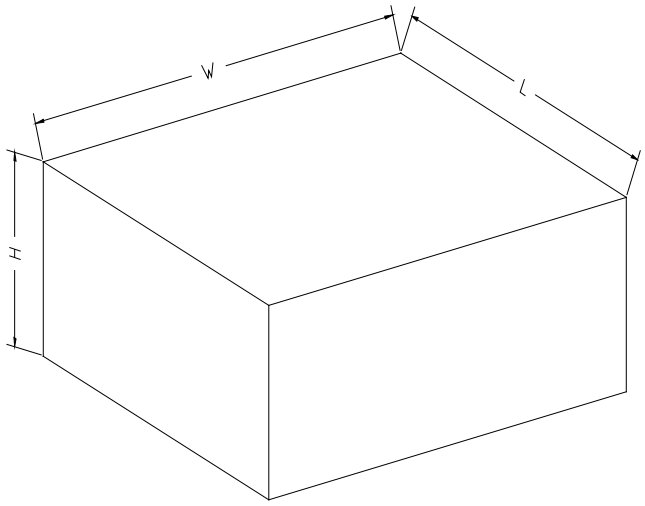
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TQFN-5×5-32IL	13″	12.4	5.30	5.30	1.10	4.0	8.0	2.0	12.0	Q2

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002