SGM61122
4.5V to 17V Input, 2A Output, Synchronous Buck Converter

GENERAL DESCRIPTION

The SGM61122 is an adaptive constant on-time control (ACOT) synchronous Buck converter with a wide input voltage range of 4.5V to 17V. This device has 2A output current capability and operates at pseudo-fixed frequency. It is an easy-to-use device with power switches and internal compensation circuit, which are all integrated in a small 6-pin package, and supports low equivalent series resistance (ESR) output capacitors. A typical 0.7ms soft-start ramp is also included to minimize the inrush current.

Protection features include cycle-by-cycle current limit, hiccup mode short-circuit protection and thermal shutdown in case of excessive power dissipation.

The SGM61122A enters in pulse-skip mode to improve efficiency during light load operation, while the SGM61122B works in Forced PWM Mode over all load conditions to achieve low output ripple and good regulation.

The SGM61122 is available in a Green SOT-563-6 package.

FEATURES

- **Wide 4.5V to 17V Input Voltage Range**
- **2A Continuous Output Current**
- **Integrated 90mΩ/50mΩ Power MOSFETs**
- **0.604V Reference Voltage**
- **Shutdown Current: 4μA (TYP)**
- **0.7ms Internal Soft-Start Time**
- **Pseudo-Fixed 650kHz Switching Frequency**
- **Adaptive Constant On-Time Mode Control**
- **Pulse-Skip Mode (SGM61122A)**
- **Forced PWM Mode (SGM61122B)**
- **Adjustable Input Under-Voltage Lockout**
- **Cycle-by-Cycle Over-Current Limit**
- **Thermal Shutdown with Auto Recovery**
- **Available in a Green SOT-563-6 Package**

APPLICATIONS

12V Distributed Power Supply Buses
Industrial and Consumer Applications
General Purpose Point of Load
TV
Surveillance
Set-Top Boxes

SIMPLIFIED SCHEMATIC

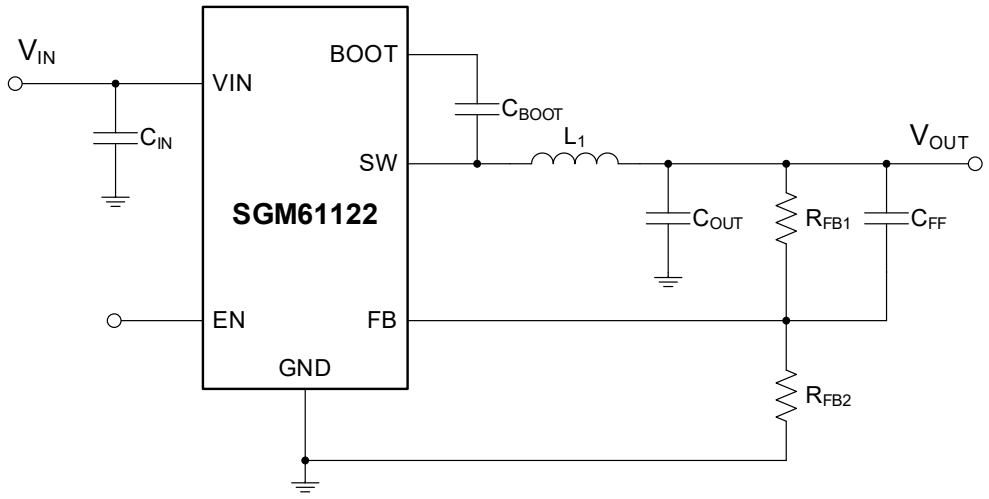


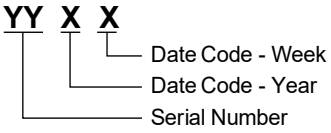
Figure 1. Simplified Schematic

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM61122A	SOT-563-6	-40℃ to +125℃	SGM61122AXKB6G/TR	0SXX	Tape and Reel, 5000
SGM61122B	SOT-563-6	-40℃ to +125℃	SGM61122BXKB6G/TR	0UXX	Tape and Reel, 5000

MARKING INFORMATION

NOTE: XX = Date Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

VIN Voltage ..... -0.3V to 18V
BOOT-SW Voltages ..... -0.3V to 6V
SW Voltage ..... -2V to V_{IN} + 0.3V
SW Voltage (20ns Transient) ..... -3.5V to 20V
EN, FB Voltage ..... -0.3V to 6V
Package Thermal Resistance
SOT-563-6, θ_{JA} ..... 119.9℃/W
SOT-563-6, θ_{JB} ..... 21.9℃/W
SOT-563-6, θ_{JC} ..... 71.3℃/W
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility (1) (2)
HBM ..... ±4000V
CDM ..... ±2000V

NOTES:

1. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.

2. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

RECOMMENDED OPERATING CONDITIONS

Input Voltage Range, V_{IN} ..... 4.5V to 17V
Output Voltage Range ..... 0.604V to 7V
EN, FB Voltage ..... -0.3V to 5.5V
Operating Junction Temperature Range ..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

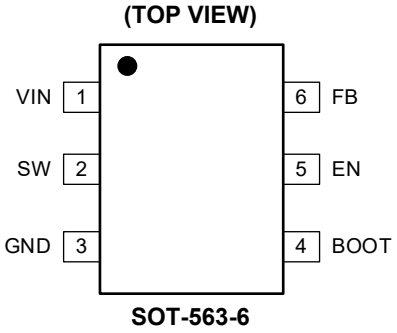
ESD SENSITIVITY CAUTION

This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION



PIN DESCRIPTION

PIN	NAME	TYPE	FUNCTION
1	VIN	P	Supply Input. Connect VIN to a power source with 4.5V to 17V voltage range. Decouple VIN to GND as close as possible with a high frequency, low ESR ceramic capacitor (X5R or higher grade is recommended).
2	SW	P	Switching Node. Connection point of the internal converter lower and upper power MOSFETs. Connect this pin to the output inductor and the bootstrap capacitor.
3	GND	G	Device Ground Reference Pin.
4	BOOT	P	Bootstrap Pin. Bootstrap supply for high-side driver. Connect a 0.1μF ceramic capacitor between BOOT and SW pins.
5	EN	I	Active-High Enable Input. Pull up to a logic-high voltage (TYP 1.2V, and lower than 5.5V) to enable the device, and pull down to disable it. Input UVLO level can be programmed using a resistor divider from VIN. Do not leave this pin floating.
6	FB	I	Feedback Pin for Setting the Output Voltage. Tap an output feedback resistor divider to this pin.

NOTE: I = input, P = power, G = ground.

ELECTRICAL CHARACTERISTICS

(T_J = -40℃ to +125℃, V_{IN} = 12V, typical values are measured at T_J = +25℃, unless otherwise noted.)

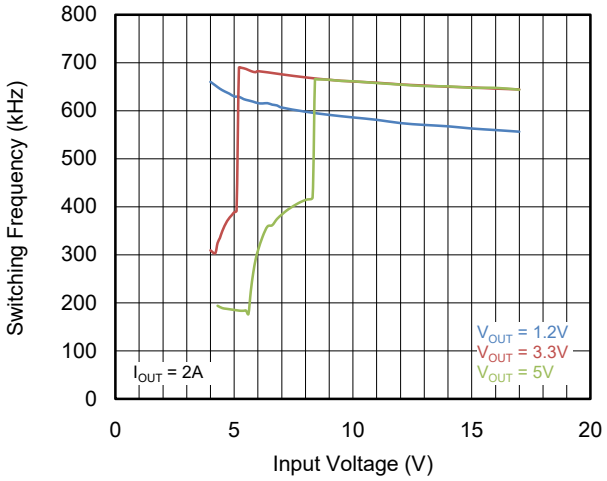
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Current							
Operating Non-Switching Supply Current	I_{IN}	V_{IN} current, V_{EN} = 5V, V_{FB} = 1V	SGM61122A		120		μA
			SGM61122B		310		
Shutdown Supply Current	I_{INSDN}	V_{IN} current, V_{EN} = 0V			4		μA
Logic Threshold							
EN High-Level Input Voltage	V_{ENH}	EN rising			1.2	1.3	V
EN Low-Level Input Voltage	V_{ENL}	EN falling		0.9	1.05		V
EN Hysteresis	V_{EN_HYS}				150		mV
Feedback Voltage							
Feedback Reference Voltage	V_{REF}	T_J = +25℃		584	604	624	mV
Feedback Reference Voltage		T_J = -40℃ to +125℃		581	604	627	mV
FB Input Current	I_{FB}	V_{FB} = 0.65V			0.01	0.1	μA
MOSFET							
High-side Switch On-Resistance	R_{DSON_HS}	V_{BOOT} - V_{SW} = 5.5V			90		mΩ
Low-side Switch On-Resistance	R_{DSON_LS}				50		mΩ
Current Limit							
Low-side Current Limit	I_{OCL}	Valley current, T_J = +25℃		2.5	4.6	6.4	A
Negative Current Limit	I_{NOCL}	SGM61122B only			-1.1		A
Thermal Shutdown							
Thermal Shutdown Threshold (1)	T_{SDN}	Shutdown temperature			160		℃
		Hysteresis			30		
Frequency							
Switching Frequency	f_{SW}	V_{IN} = 12V, V_{OUT} = 3.3V, CCM			650		kHz
On-Time & Off-Time Control							
Minimum Off-Time (1)	$t_{OFF(MIN)}$	V_{FB} = 0.5V			100		ns
Minimum On-Time (1)	$t_{ON(MIN)}$				68		ns
Soft-Start							
Soft-Start Time	t_{SS}	Internal soft-start time			0.7		ms
Output Under-Voltage							
Output UVP Threshold	V_{UVP}	Hiccup detect threshold, percentage of V_{REF}			60		%
UVP Deglitch Time	t_{UVP}				24		μs
Hiccup Time before Restart	$t_{HICCUP-RE}$				15		ms
UVLO							
UVLO Threshold	V_{UVLO}	V_{IN} rising			4	4.4	V
		V_{IN} falling		3.2	3.6		
UVLO Threshold Hysteresis	V_{UVLO_HYS}	Hysteresis			0.4		

NOTE:
1. Specified by design. Not production tested.

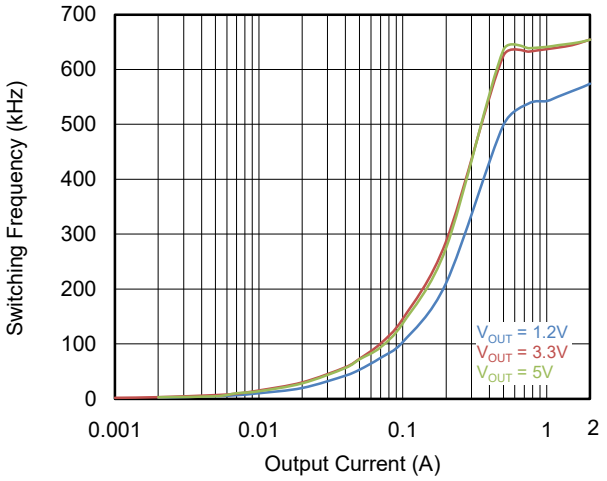
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = +25℃, V_{IN} = 12V, V_{OUT} = 3.3V, L_1 = 4.7μH, DCR = 30.8mΩ, and C_{OUT} = 22μF × 2, unless otherwise noted.

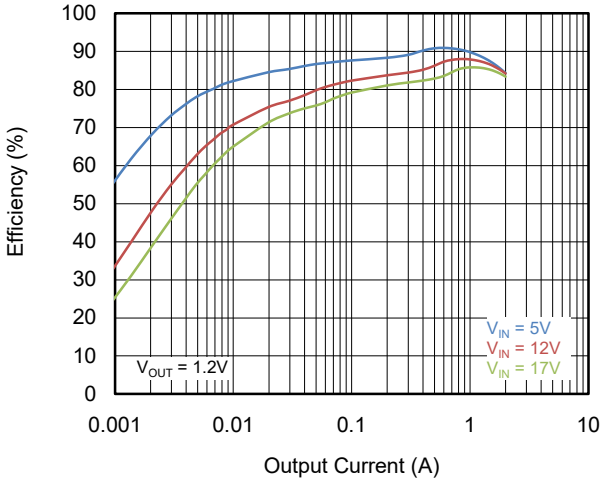
Switching Frequency vs. Input Voltage (SGM61122A)



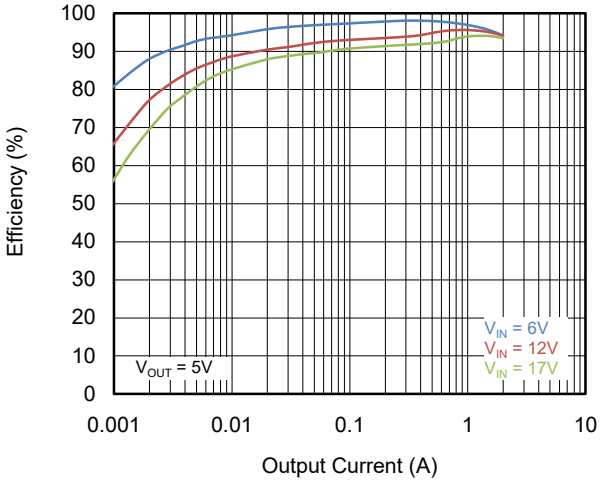
Switching Frequency vs. Output Current (SGM61122A)



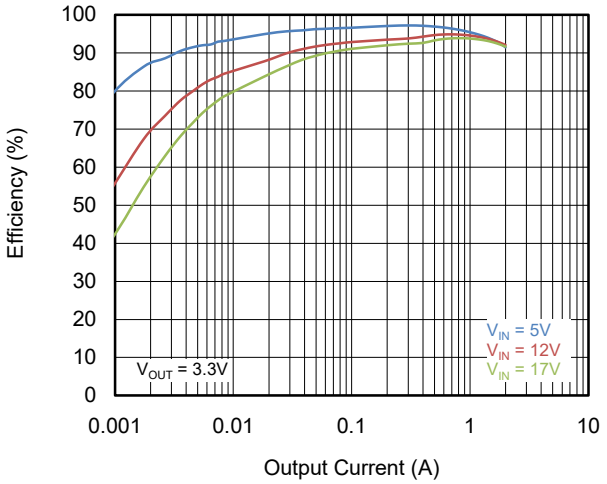
Efficiency vs. Output Current (SGM61122A)



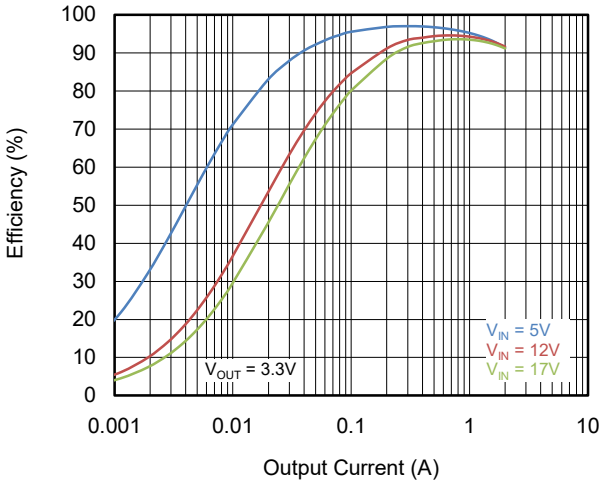
Efficiency vs. Output Current (SGM61122A)



Efficiency vs. Output Current (SGM61122A)



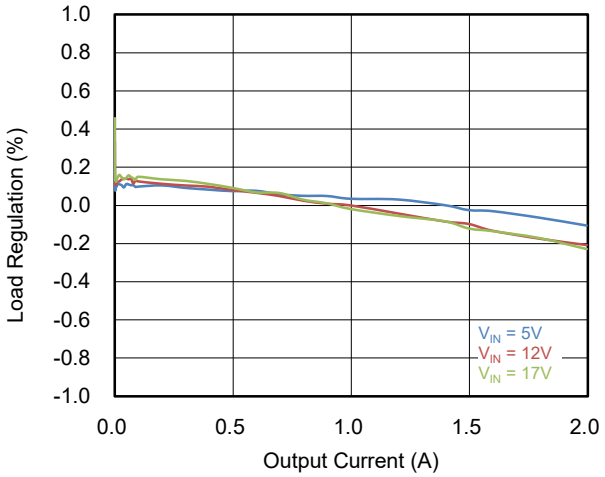
Efficiency vs. Output Current (SGM61122B)



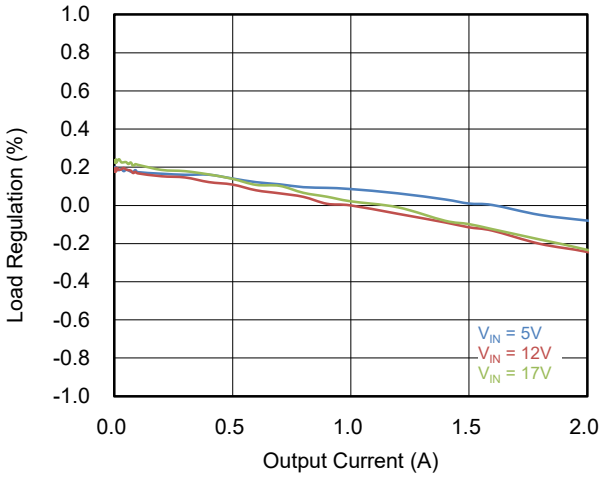
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, V_{IN} = 12V, V_{OUT} = 3.3V, L_1 = 4.7μH, DCR = 30.8mΩ, and C_{OUT} = 22μF × 2, unless otherwise noted.

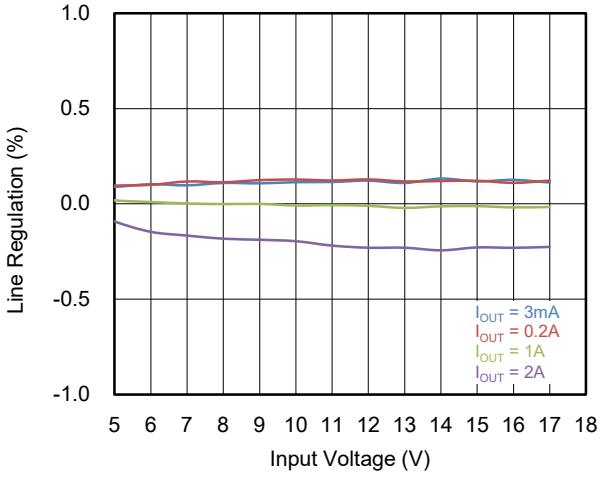
Load Regulation (SGM61122A)



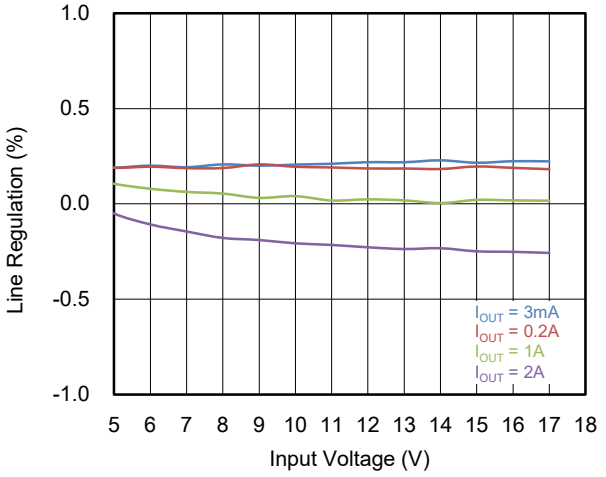
Load Regulation (SGM61122B)



Line Regulation (SGM61122A)



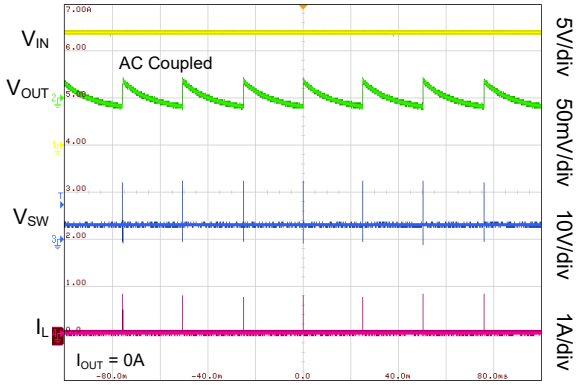
Line Regulation (SGM61122B)



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

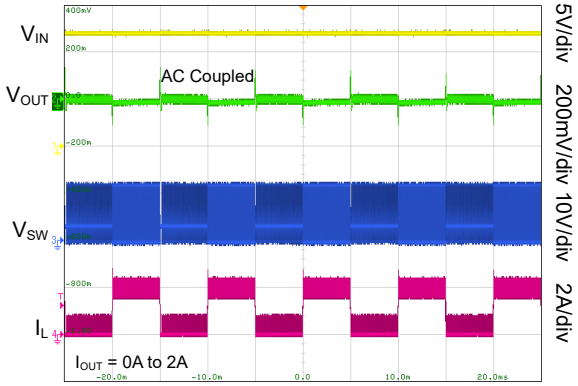
T_A = +25℃, V_{IN} = 12V, V_{OUT} = 3.3V, L_1 = 4.7μH, DCR = 30.8mΩ, and C_{OUT} = 22μF × 2, unless otherwise noted.

Output Voltage Ripple (SGM61122A)



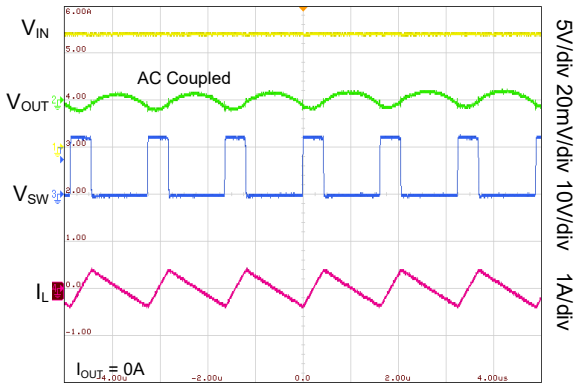
Time (20ms/div)

Load Transient (SGM61122A)



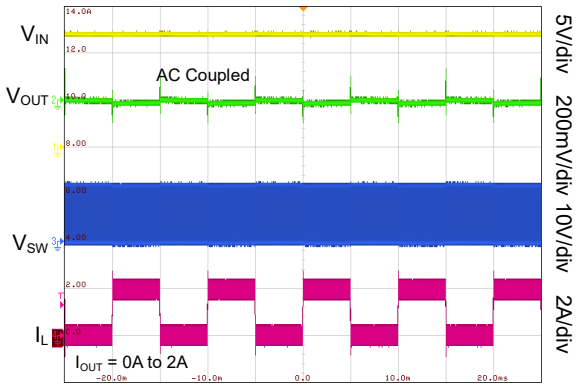
Time (5ms/div)

Output Voltage Ripple (SGM61122B)



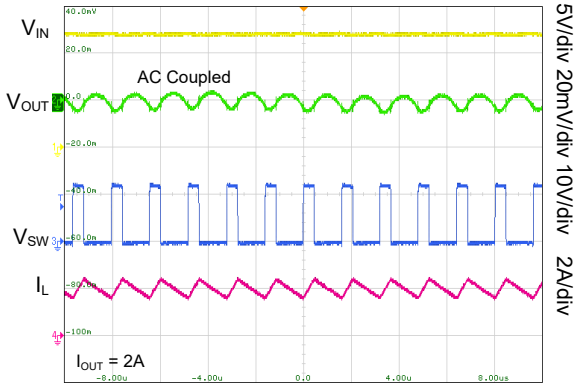
Time (1μs/div)

Load Transient (SGM61122B)



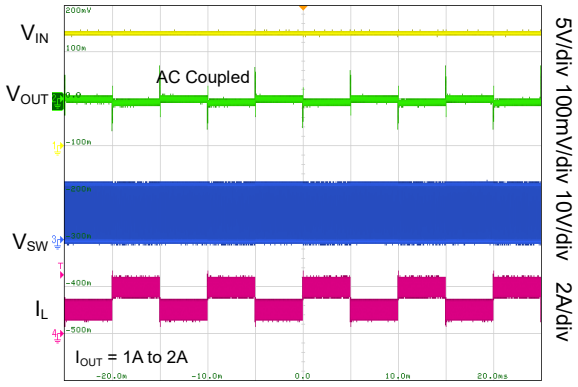
Time (5ms/div)

Output Voltage Ripple



Time (2μs/div)

Load Transient

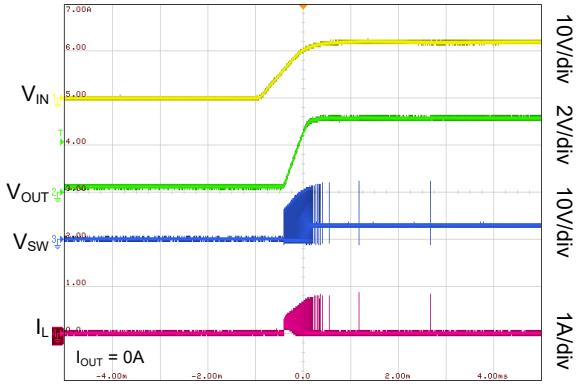


Time (5ms/div)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

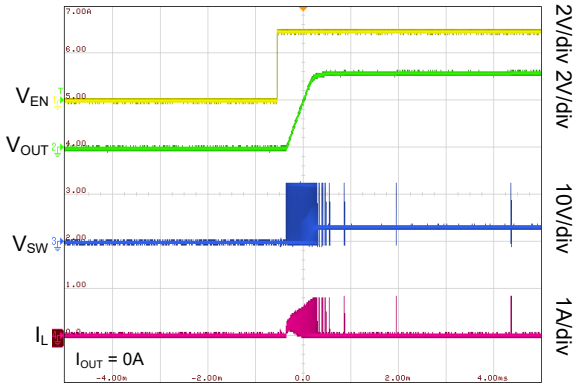
T_A = +25℃, V_{IN} = 12V, V_{OUT} = 3.3V, L_1 = 4.7μH, DCR = 30.8mΩ, and C_{OUT} = 22μF × 2, unless otherwise noted.

VIN Startup (SGM61122A)



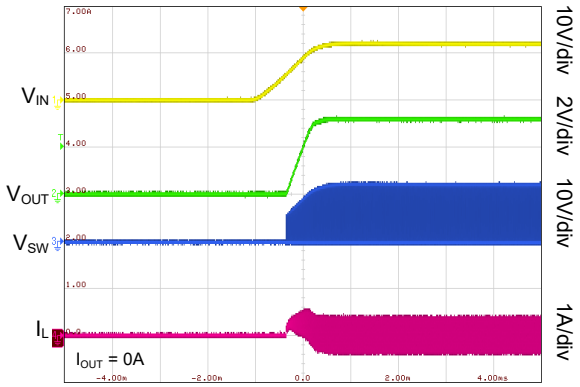
Time (1ms/div)

EN Startup (SGM61122A)



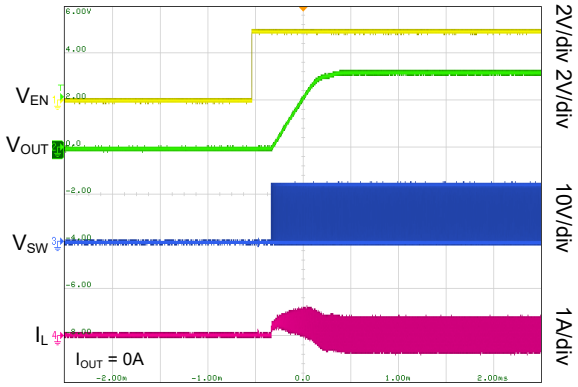
Time (1ms/div)

VIN Startup (SGM61122B)



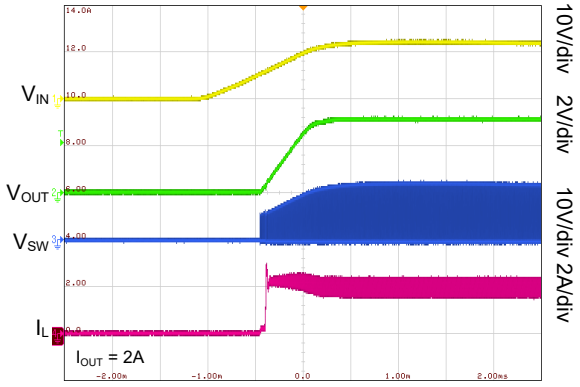
Time (1ms/div)

EN Startup (SGM61122B)



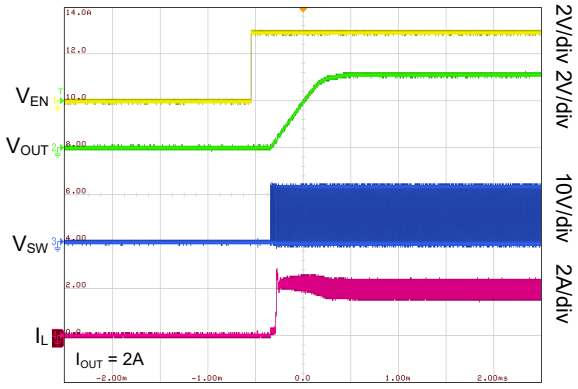
Time (500μs/div)

VIN Startup



Time (500μs/div)

EN Startup

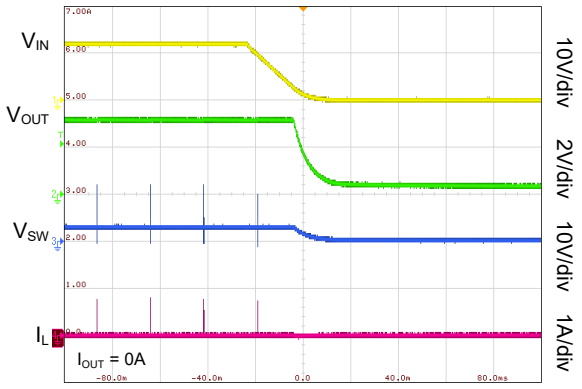


Time (500μs/div)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

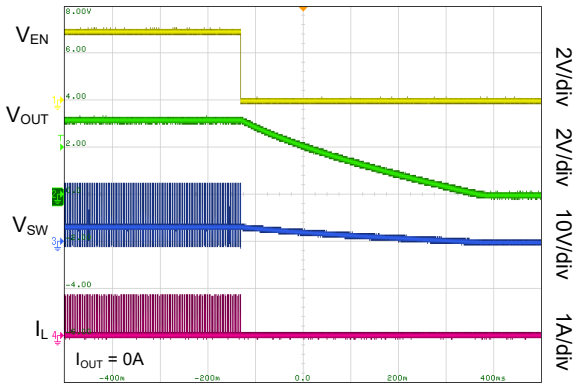
T_A = +25℃, V_{IN} = 12V, V_{OUT} = 3.3V, L_1 = 4.7μH, DCR = 30.8mΩ, and C_{OUT} = 22μF × 2, unless otherwise noted.

VIN Shutdown (SGM61122A)



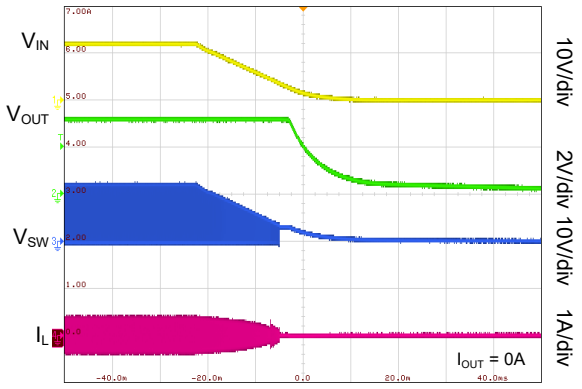
Time (20ms/div)

EN Shutdown (SGM61122A)



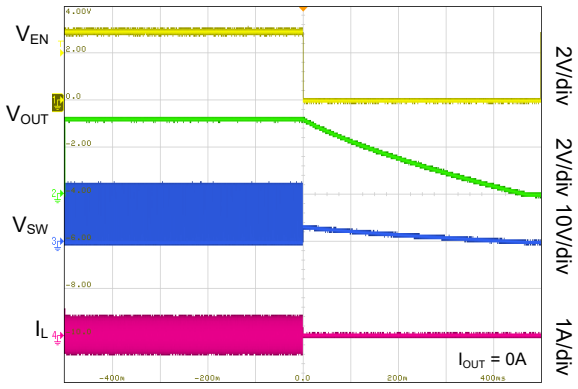
Time (100ms/div)

VIN Shutdown (SGM61122B)



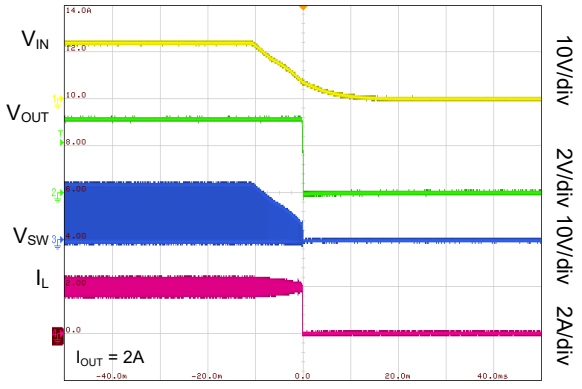
Time (10ms/div)

EN Shutdown (SGM61122B)



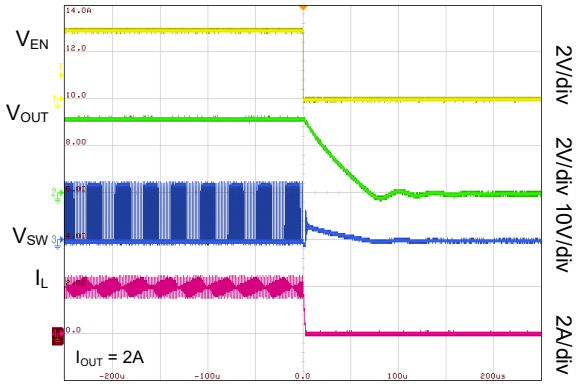
Time (100ms/div)

VIN Shutdown



Time (10ms/div)

EN Shutdown

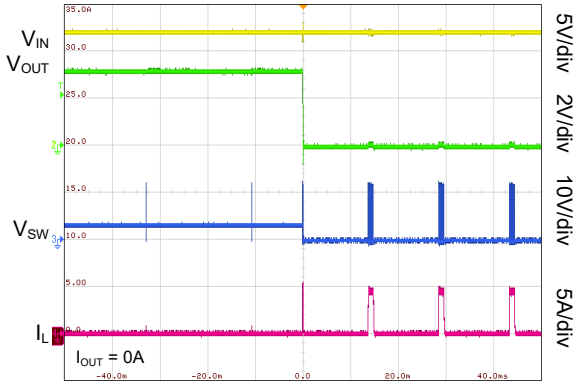


Time (50μs/div)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

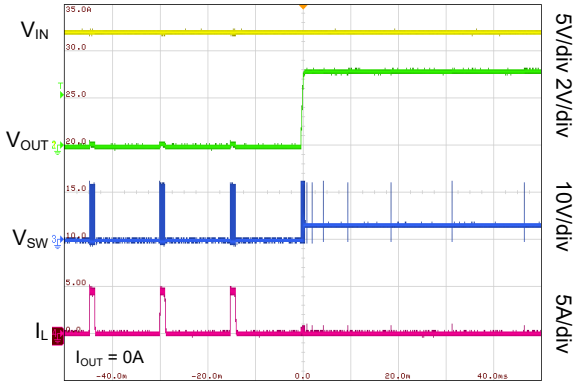
T_A = +25℃, V_{IN} = 12V, V_{OUT} = 3.3V, L_1 = 4.7μH, DCR = 30.8mΩ, and C_{OUT} = 22μF × 2, unless otherwise noted.

Short-Circuit Entry (SGM61122A)



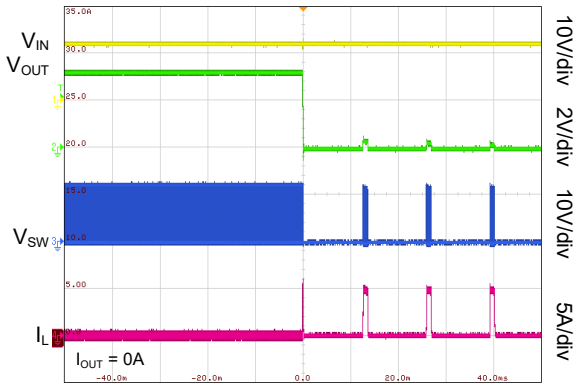
Time (10ms/div)

Short-Circuit Recovery (SGM61122A)



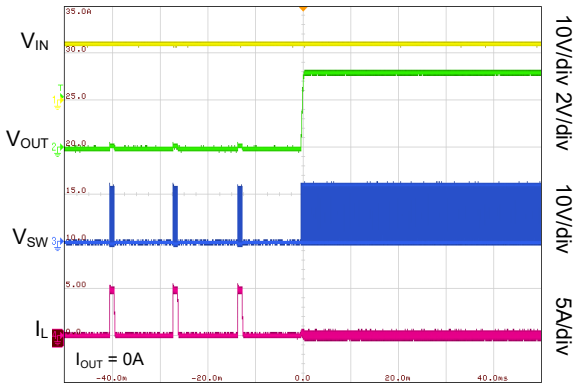
Time (10ms/div)

Short-Circuit Entry (SGM61122B)



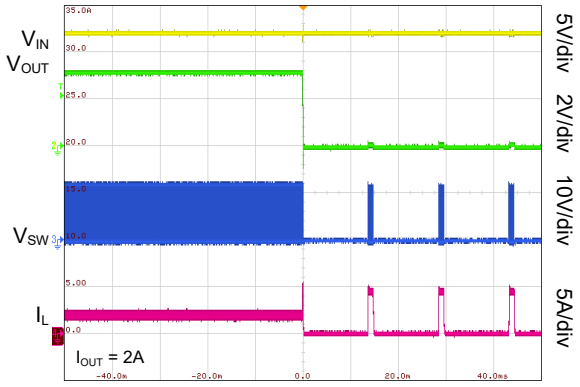
Time (10ms/div)

Short-Circuit Recovery (SGM61122B)



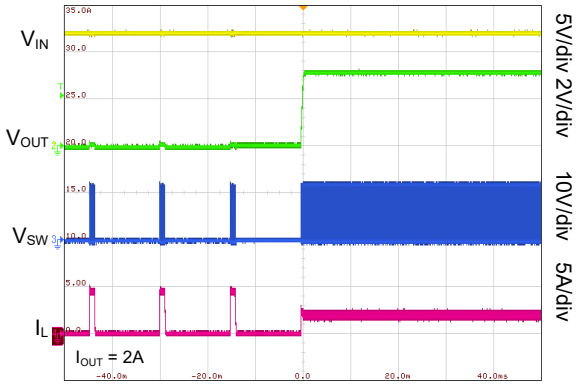
Time (10ms/div)

Short-Circuit Entry



Time (10ms/div)

Short-Circuit Recovery



Time (10ms/div)

FUNCTIONAL BLOCK DIAGRAM

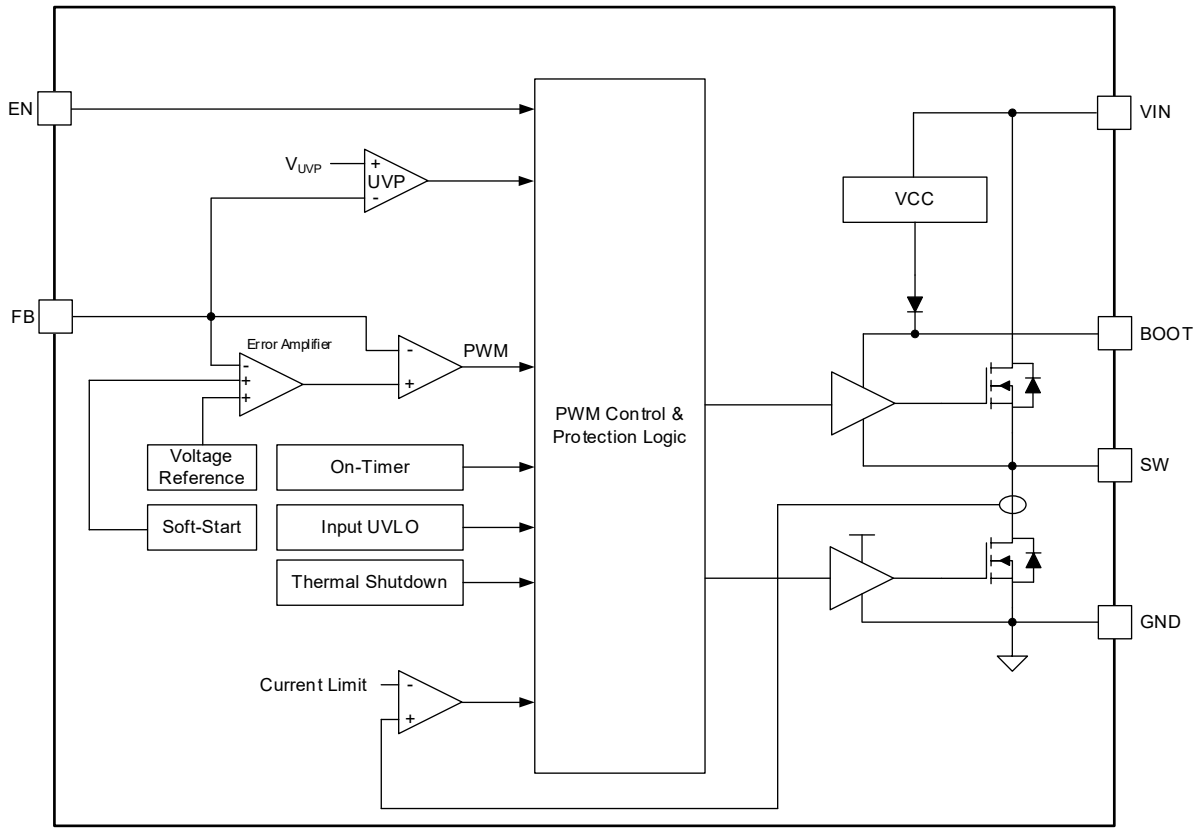


Figure 2. Block Diagram

DETAILED DESCRIPTION

Overview

The SGM61122 is a 17V/2A synchronous Buck converter with over-current, short-circuit protections and thermal shutdown with auto recovery.

Adaptive Constant On-Time Control

In conventional voltage mode control (VMC) or current mode control (CMC) converters, a fixed frequency clock timing signal generates a saw-tooth ramp that is compared with the compensation network output to adjust the PWM duty cycle (on-time) as control variable and regulate the output voltage and/or current feedback(s) to govern the control variable and keep the output regulated with fast reaction to load or V_{IN} variations. The existence of the compensator in VMC or CMC converter inherently introduces some delay in the loop response.

Unlike VMC or CMC, the adaptive constant on-time (ACOT) control is a hysteretic mode control without clock signal. Each switching cycle starts with a relatively constant on-time pulse when an internal comparator senses that the output voltage drops below the desired output voltage. Output voltage is sensed by the feedback (FB) pin through an output resistor divider and is compared to the internal reference voltage (V_{REF}) with an error amplifier. The amplifier output is sent to a comparator and when the feedback voltage (V_{FB}) falls below amplifier output, the comparator triggers the on-time control logic that turns on the high-side switch. ACOT control is able to dynamically adjust the on-time duration based on the input voltage and output voltage so that it can achieve relative constant frequency during steady state operation, which minimizes the EMI interference at some sensitive bands of certain frequencies in the system. An internal ramp is added to the feedback (V_{FB}) to simulate output ripple, so it supports low ESR output capacitors applications.

Enable Pin and UVLO Adjustment

A Zener diode is designed to clamp the EN input voltage, which is not allowed to go through large current. The voltage on the EN pin provides precise enable and disable control of SGM61122. The device will enable if the EN pin voltage exceeds the enable threshold of 1.2V and VIN exceeds its UVLO threshold. The device will disable if the EN voltage is externally pulled low or the VIN pin voltage falls below its UVLO threshold. The EN pin cannot be left floating and can be connected to VIN with a resistor of no less than 100kΩ to enable the device.

An external input UVLO adjustment circuit is recommended in Figure 3, and the R_{ENT} is recommended to be no less than 100kΩ. The EN input can be driven by an external logic signal to facilitate system sequencing and protection. If V_{EN} < 1.05V (TYP), the device will shut down. Only if 5.5V > V_{EN} > 1.2V (TYP), the device will start operation.

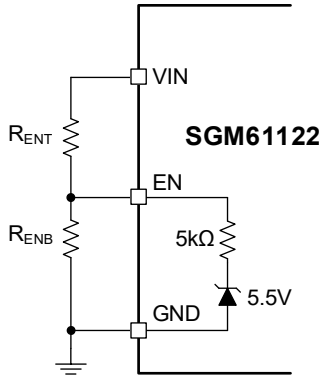


Figure 3. System UVLO by Enable Divider

DETAILED DESCRIPTION (continued)

Bootstrap Voltage (BOOT)

To power the upper switch gate driver, a voltage higher than VIN is needed. Bootstrap technique is used to provide this voltage from the switching node by using a 0.1μF bootstrap capacitor between SW and BOOT pins along with an internal bootstrap diode. The voltage is internally regulated for driving the high-side switch. An X5R or X7R ceramic capacitor is recommended for C_{BOOT} to have stable capacitance against temperature and voltage variations.

Output Voltage Programming

The output voltage is set by a resistor divider between V_{OUT} and GND that is tapped to the FB pin. It is recommended to use 1% or higher quality resistors with low thermal tolerance for an accurate and thermally stable output voltage.

Use Equation 1 and Figure 1 to calculate the output voltage. Lower divider resistor values increase loss and reduce light load efficiency. Consider larger resistors to improve efficiency at light load, and start with 100kΩ for the upper resistor (R_{FB1}). Note that if R_{FB1} is too high (> 1MΩ), the FB pin leakage current and other noises can easily affect the accuracy and performance of the regulator.

$$V_{OUT} = V_{REF} \times \left[\frac{R_{FB1}}{R_{FB2}} + 1 \right] \quad (1)$$

Internal Voltage Reference and Soft-Start

The SGM61122 device has an internal 0.604V reference (V_{REF}) to program the output at the desired level. When the converter starts (or is enabled), an internal ramp voltage begins to rise from near 0V to slightly above 0.604V with a ramp time of 0.7ms. The lower of V_{REF} and this ramp is used as reference for the error amplifier. Therefore, during startup, the ramp provides a soft-start for the output. The soft-start is needed to avoid high inrush currents caused by rapid increase of output voltage across output capacitors and the load.

Operation with Pulse-Skip Mode (SGM61122A)

When SGM61122A operates in discontinuous conduction mode (DCM) with light load, it goes into the pulse-skip mode in which internal power dissipation is significantly reduced. Moreover, the operating frequency starts to drop depending on the load.

The details are explained in Figure 4 that shows the timings of the ACOT control in DCM. Inductor current (I_L) is monitored with a zero-crossing detector and when I_L crosses the zero, both high-side and low-side MOSFETs are turned off (if $V_{FB} > V_{REF\_EA}$). They will not be turned on again until the V_{FB} falls below V_{REF_EA} and triggers a new on-time pulse. During this off-time period, all non-essential circuits are shut down to minimize losses and the load is supplied by the output capacitor stored energy. The control circuitry wakes up when the new on-pulse is triggered.

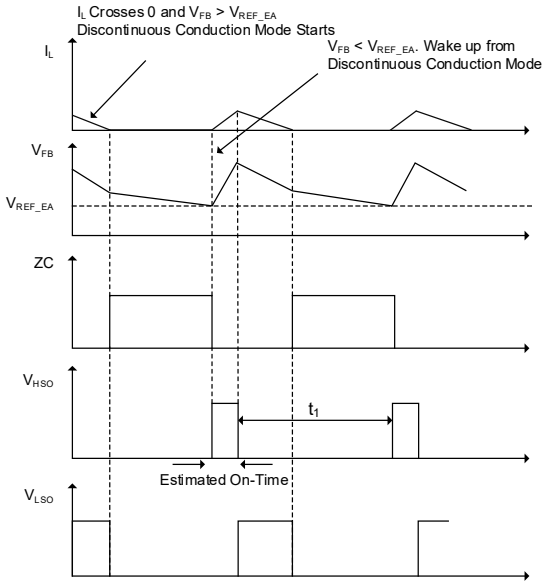


Figure 4. Pulse-Skip Mode (DCM)

Forced Pulse Width Modulation Mode (SGM61122B)

SGM61122B is locked in forced pulse width modulation mode from full load to no load. Negative inductor currents are allowed at light load to keep continuous inductor current operation. It is a tradeoff that sacrifices light load efficiency for keeping switching frequency relatively fixed, lower output ripple, and better output regulation. Negative current limit is designed to avoid fatal negative current for SGM61122B. The valley current of inductor is detected during low-side MOSFET conduction. When the inductor current exceeds the I_{NOCL} threshold, the low-side MOSFET is turned off.

High Duty Cycle Operation

The SGM61122 supports high duty cycle operation up to 95% by smoothly reducing the switching frequency. When the duty cycle exceeds 75%, the t_{ON} starts to extend automatically and the switching frequency decreases to keep output voltage in regulation and improve the load transient performance. The minimum switching frequency is limited to about 250kHz.

DETAILED DESCRIPTION (continued)

Low-Side Current Limit and Short-Circuit Protection (Hiccup)

A cycle-by-cycle valley current detection is implemented to limit the output current. During t_{OFF} portion of each cycle (in which low-side MOSFET is conducting), the current of the low-side MOSFET is monitored by measuring its drain-to-source voltage which is proportional to the current. This measurement is temperature compensated for better accuracy. If the low-side MOSFET current exceeds I_{OCL} threshold, the converter maintains low-side MOSFET on and delays the creation of a new pulse, even the voltage feedback loop requires one, until the inductor current, which is going through low-side MOSFET during t_{OFF}, drops below the I_{OCL} threshold. During current limiting, the output voltage will drop because the power supplied by the system is less than that demanded by the load. If the output voltage drops below the output UVP threshold (see Output Under-Voltage Protection section), the device will enter hiccup mode.

Output Under-Voltage Protection

SGM61122 features output under-voltage protection. If soft-stat is ready and the feedback (V_{FB}) decreases to 60% of the reference voltage, the device enters hiccup mode. In hiccup mode, the regulator is shut down and kept off for 15ms typically before the SGM61122 tries to start again. If over-current or a short-circuit fault condition still exists, the hiccup mode will repeat until the fault condition is removed. Hiccup mode can help to reduce power dissipation and prevent overheating and potential damage to the device.

Thermal Shutdown

If the junction temperature exceeds +160℃ (TYP), the device is forced to stop switching. It will recover automatically when T_J falls below the recovery threshold.

APPLICATION INFORMATION

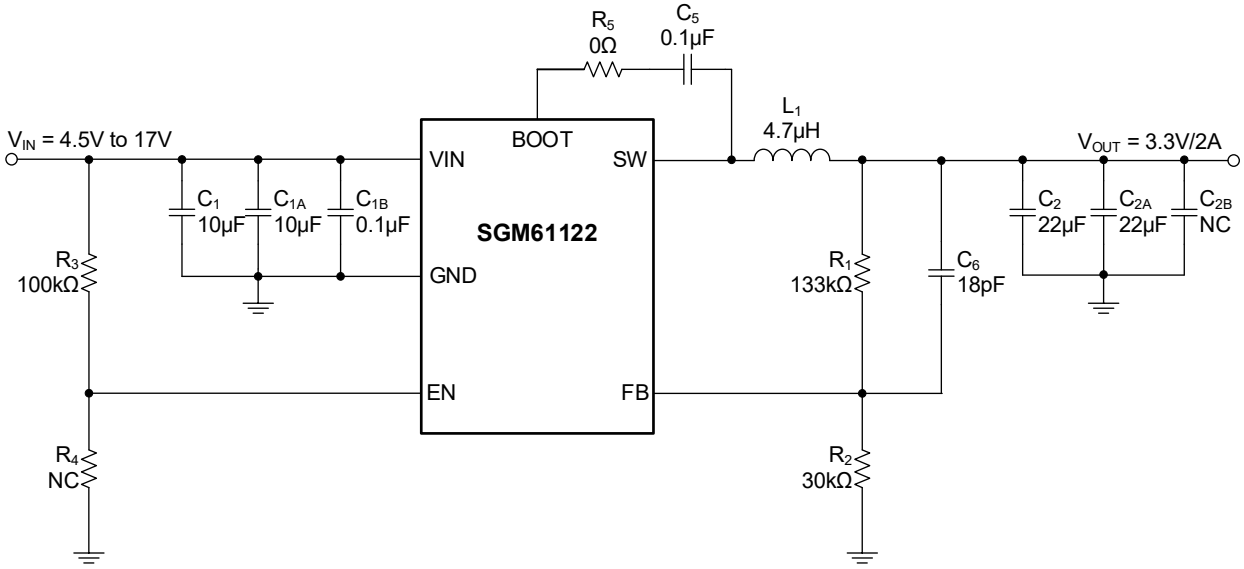


Figure 5. A Reference Design for 3.3V/2A Application

The design method and component selection for the SGM61122 Buck converter is explained in this section. Schematic of a basic design is shown in Figure 5. Only a few external components are needed to provide a constant output voltage from a wide input voltage range.

The external components are designed based on the application requirements and device stability. Some suitable output filters (L and C_{OUT}) along with C_6 and divider resistor values are provided in Table 1 to simplify component selection.

Table 1. Recommended Component Values

V_{OUT} (V)	L_1 (μH)	C_2 + C_{2A} (μF)	R_1 (kΩ)	R_2 (kΩ)	C_6 (pF)
1.2	2.2	44	30	30	18
3.3	4.7	44	133	30	18
5	4.7	44	220	30	18

Design Requirements

A typical application circuit for the SGM61122 as a Buck converter is shown in Figure 5. It is used for converting a 4.5V to 17V supply voltage to a lower voltage level supply voltage (3.3V) suitable for the system. The design parameters given in Table 2 are used for this design example.

Table 2. Design Parameters

Design Parameters	Example Values
Input Voltage	12V (TYP), 4.5V to 17V
Input Ripple Voltage	240mV, 2% of V_{IN_TYP}
Output Voltage	3.3V
Output Voltage Ripple	66mV, 2% of V_{OUT}
Output Current Rating	2A
Transient Response, 1A to 2A Load Step	165mV, 5% of V_{OUT}
Operation Frequency	650kHz

Input Capacitor Selection

A high-quality ceramic capacitor (X5R or X7R or better dielectric grade) must be used for input decoupling of the SGM61122. At least 3μF of effective capacitance (after de-ratings) is needed on the VIN input. In some applications, additional bulk capacitance may also be required for the VIN input, for example, when the SGM61122 is more than 5cm away from the input source. The VIN capacitor RMS current rating must be greater than the RMS current of input current ripple. The RMS current of input current ripple is given by Equation 2, and its maximum occurs at D = 50%. Using the design example I_{OUT} = 2A, yields the maximum I_{CIN_RMS} of 1A.

$$I_{CIN\_RMS} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \frac{(V_{IN} - V_{OUT})}{V_{IN}}} = I_{OUT} \times \sqrt{D \times (1-D)} \quad (2)$$

APPLICATION INFORMATION (continued)

For this design, a ceramic capacitor with at least 25V voltage rating is required to support the maximum input voltage. So, two 10μF/25V capacitors are selected for VIN to cover all DC bias, thermal and aging de-ratings. The input capacitance determines the regulator input voltage ripple. This ripple can be calculated from Equation 3. In this example, the total effective capacitance of the 2 × 10μF/25V capacitor is around 8μF at 12V input, and the input voltage ripple is 77mV.

$$\Delta V_{IN} = \frac{I_{OUT} \times D \times (1-D)}{C_{IN} \times f_{SW}} \quad (3)$$

It is recommended placing an additional small size 0.1μF ceramic capacitor right beside VIN and GND pins for high frequency filtering.

Inductor Selection

Equation 4 is conventionally used to calculate the output inductance of a Buck converter. The ratio of inductor current ripple (ΔI_L) to the maximum output current (I_{OUT}) is represented as K_{IND} factor ($\Delta I_L/I_{OUT}$). The inductor ripple current is bypassed and filtered by the output capacitor and the inductor DC current is passed to the output. Inductor ripple is selected based on a few considerations. The peak inductor current (I_{OUT} + $\Delta I_L/2$) must have a safe margin from the saturation current of the inductor in the worst-case conditions especially if a hard-saturation core type inductor (such as ferrite) is chosen. The ripple current also affects the selection of the output capacitor. C_{OUT} RMS current rating must be higher than the inductor RMS ripple. Typically, a 40% ripple is selected (K_{IND} = 0.4).

$$L = \frac{V_{IN\_MAX} - V_{OUT}}{I_{OUT} \times K_{IND}} \times \frac{V_{OUT}}{V_{IN\_MAX} \times f_{SW}} \quad (4)$$

In this example, the calculated inductance is 5.11μH with K_{IND} = 0.4, for compact applications, a 4.7μH inductor is selected. The ripple, RMS and peak inductor current calculations are summarized in Equations 5, 6 and 7 respectively.

$$\Delta I_L = \frac{V_{IN\_MAX} - V_{OUT}}{L} \times \frac{V_{OUT}}{V_{IN\_MAX} \times f_{SW}} \quad (5)$$

$$I_{L\_RMS} = \sqrt{I_{OUT}^2 + \frac{\Delta I_L^2}{12}} \quad (6)$$

$$I_{L\_PEAK} = I_{OUT} + \frac{\Delta I_L}{2} \quad (7)$$

Note that during startup, load transients or fault conditions, the peak inductor current may exceed the calculated I_{L_PEAK}. Therefore, it is always safer to choose the inductor saturation current higher than the switch current limit.

Output Capacitor Selection

The output capacitors and inductor filter the AC part of the PWM switching voltage and provide an acceptable level of output voltage ripple superimposed on the desired output DC voltage. Additionally, the capacitors store energy to assist in maintaining output voltage regulation during load transient. The output voltage ripple (ΔV_{OUT}) depends on the output capacitor value at the operating voltage, temperature (℃) and its parasitic parameters (ESR and ESL):

$$\Delta V_{OUT} = \Delta I_L \times ESR + \frac{V_{IN} - V_{OUT}}{L} \times ESL + \frac{\Delta I_L}{8 \times f_{SW} \times C_{OUT}} \quad (8)$$

The voltage rating of the output capacitors should be selected with enough margins to ensure that capacitance drop (voltage and temperature de-rating) is not significant.

The type of output capacitors will determine which terms of Equation 8 are dominant. For ceramic output capacitors, the ESR and ESL are virtually zero, so the output voltage ripple will be dominated by the capacitive term. For electrolytic output capacitors, the value of capacitance is relatively high, and compared with ESR and ESL terms, the third term in Equation 8 can be ignored.

To reduce the voltage ripple, either inductance or the total capacitance is increased. Higher quality capacitors, larger inductance or using parallel capacitors can help reduce the output ripple in a design using electrolytic output capacitors.

APPLICATION INFORMATION (continued)

The ESR of some commercial electrolytic capacitors can be quite high, and it is recommended using quality capacitors with the ESR or the total impedance clearly documented in the datasheet. ESR of an electrolytic capacitor may increase significantly at cold ambient temperatures with a factor of 10 or so, which increases the ripple and can deteriorate the regulator stability.

The transient response of the regulator also depends on the quantity and type of output capacitors. In general, reducing the ESR of the output capacitance will lead to a better transient response. The ESR can be minimized by simply adding more capacitors in parallel or by using higher quality capacitors. When a fast load transient of magnitude ΔI_L and rate of di/dt occurs, the output voltage will jump or dip by a transient magnitude of ΔV_{OUT}:

$$\Delta V_{OUT} = \Delta I_L \times ESR + \frac{di}{dt} \times ESL \quad (9)$$

Right after the transient, the inductor current remains almost constant especially for larger inductors and the transient current is carried by the capacitor. The output voltage will deviate from its nominal value for a short time depending on the system bandwidth, the inductor and the output capacitance. In this example, according to Table 1, 2 × 22μF/16V X5R ceramic capacitors with 2mΩ of ESR can meet the above conditions.

Bootstrap Capacitor Selection

Use a 0.1μF high-quality ceramic capacitor (X5R or X7R) with 10V or higher voltage rating for the bootstrap capacitor (C_5).

Output Voltage Setting

Use an external resistor divider (R_1 and R_2) to set the output voltage using Equation 10:

$$R_1 = R_2 \times \left(\frac{V_{OUT}}{V_{REF}} - 1 \right) \quad (10)$$

where V_{REF} = 604mV is the internal reference. For example, by choosing R_2 = 30kΩ, the R_1 value for 3.3V output will be calculated as 133.9kΩ, so the nearest resistance of 133kΩ is selected.

Feed-Forward Capacitor Selection

The SGM61122 contains an internal compensation circuit, an internal ramp is added to the feedback (V_{FB}) to simulate output ripple. For ultra-low output capacitance ESR (ceramic capacitor) applications, it is recommended adding a 18pF feed-forward capacitor (C_6) to provide a low-impedance path for output voltage ripple and ensure minimal phase shift of the voltage ripple at the feedback node while maintaining acceptable transient response.

APPLICATION INFORMATION (continued)

Layout Guide

PCB is an essential element of any switching power supply. The converter operation can be significantly disturbed due to the existence of the large and fast rising/falling voltages that can couple through stray capacitances to other signal paths, and also due to the large and fast changing currents that can interact through parasitic magnetic couplings, unless those interferences are minimized and properly managed in the layout design. Insufficient conductance in copper traces for the high current paths results in high resistive losses in the power paths and voltage errors. The following guidelines provided here are necessary to design a good layout:

- Bypass VIN pin to GND pin with low-ESR ceramic capacitors (X5R or X7R better dielectric) placed as close as possible to VIN pin.
- Use short, wide and direct traces for high-current connections (VIN, SW and GND).
- Keep the BOOT - SW voltage path as short as possible.
- Place the feedback resistors as close as possible to the FB pin that is sensitive to noise.
- Minimize the area and path length of the loop formed by VIN pin, bypass capacitors connections and SW pin.

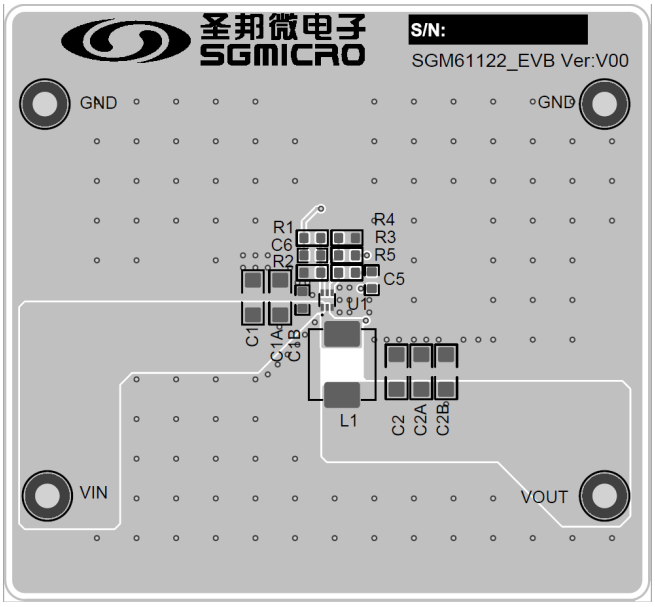


Figure 6. PCB Top Layer

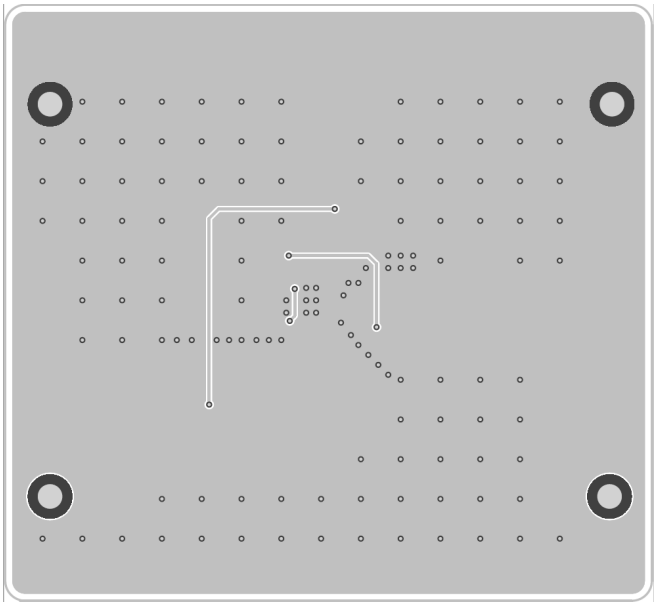


Figure 7. PCB Bottom Layer

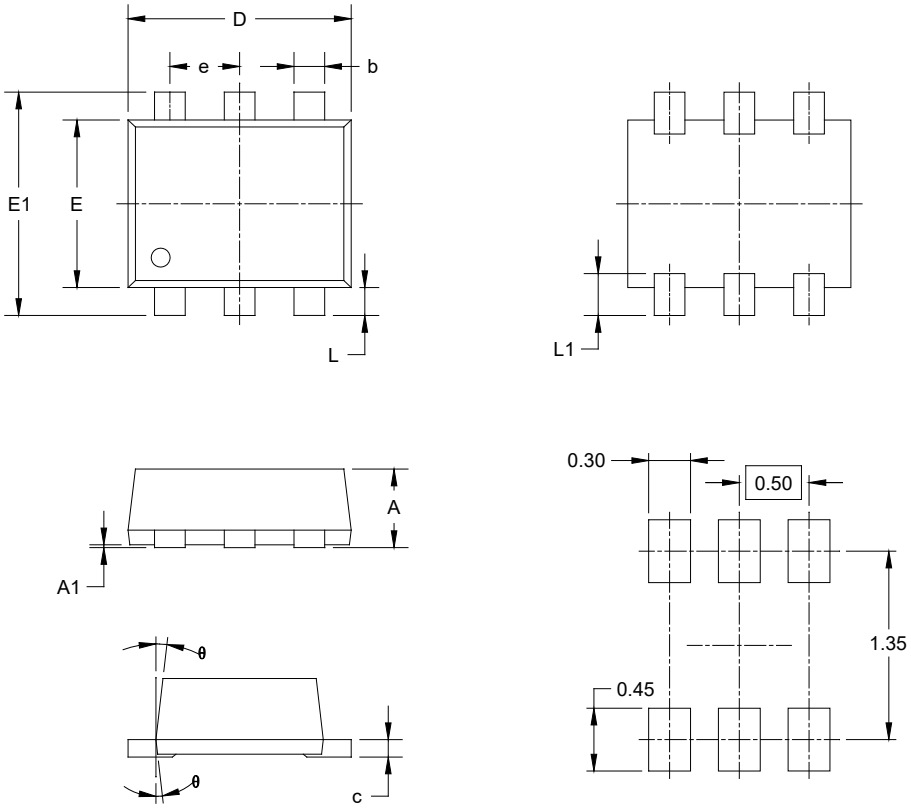
REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original to REV.A (AUGUST 2026)	Page
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

SOT-563-6



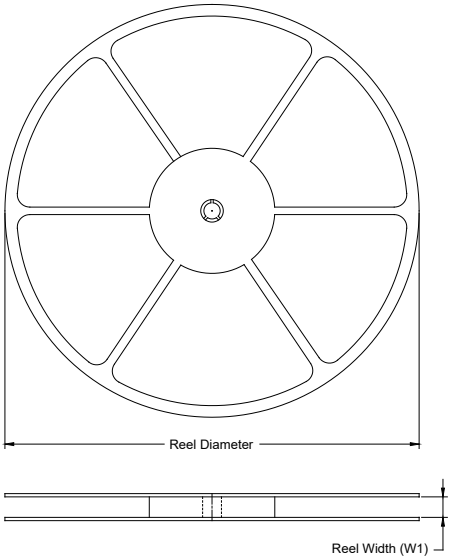
RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.525	0.600	0.021	0.024
A1	0.000	0.050	0.000	0.002
b	0.170	0.270	0.007	0.011
c	0.090	0.180	0.004	0.007
D	1.500	1.700	0.059	0.067
E	1.100	1.300	0.043	0.051
E1	1.500	1.700	0.059	0.067
e	0.450	0.550	0.018	0.022
L	0.100	0.300	0.004	0.012
L1	0.200	0.400	0.008	0.016
θ	9° REF		9° REF	

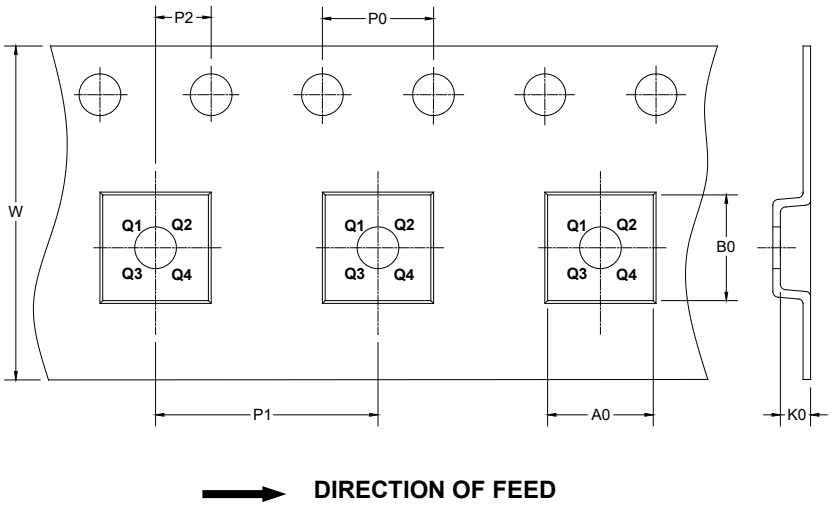
NOTES:
1. Body dimensions do not include mode flash or protrusion.
2. This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



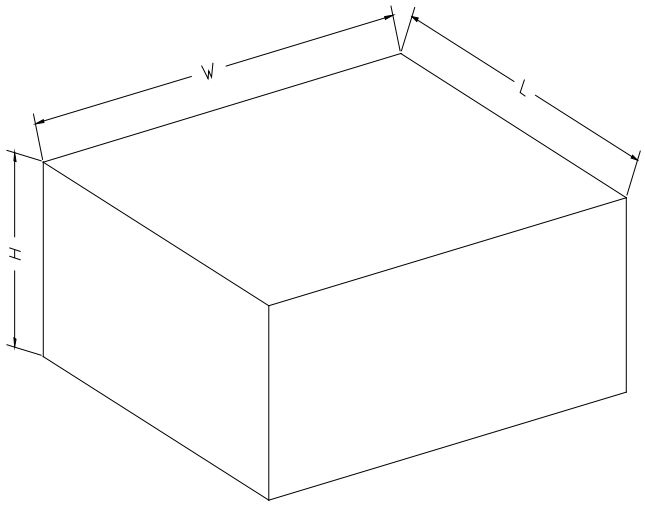
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
SOT-563-6	7"	9.5	1.78	1.78	0.69	4.0	4.0	2.0	8.0	Q3

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18

DD0002