SGMGH10865
650V 27mΩ GaNFET with Integrated Gate Clamp

GENERAL DESCRIPTION

The SGMGH10865 GaNFET IC seamlessly integrates a 650V E-Mode GaN FET with advanced features, setting a new standard for performance, ease of use, and reliability in power electronics. The integrated gate clamp, driven by accurate LDO-based circuitry, maintains a tightly regulated driving voltage for the GaN FET within a flexible gate-input voltage range of 10V to 24V, ensuring full protection of the GaN power transistor against excessive voltage stress while maximizing GaN performance.

The SGMGH10865 offers users the ability to adjust the turn-on and turn-off slew rate of the GaN FET with external gate resistors, optimizing both EMI and power efficiency. The integrated Miller clamp prevents false turn-on caused by the high dv/dt slope of the drain voltage.

The SGMGH10865 features a high level of integration with a GaN FET and robust protection, making it suitable for a range of applications, from simple setups with low component count to high-frequency and high-power applications.

FEATURES

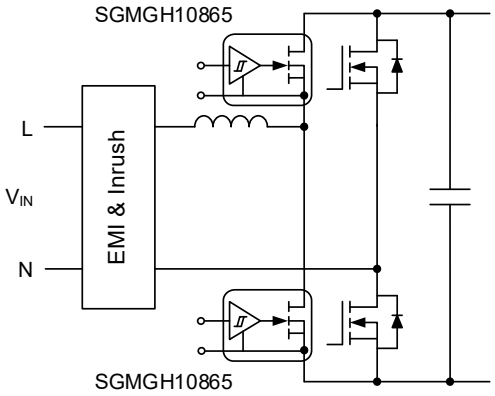
- **27mΩ E-Mode GaN with Integrated Gate Clamp**
- **650V Continuous, 800V Transient Voltage Rating**
- **Wide 10V to 24V Gate Input Voltage Range**
- **Adjustable Turn-On and Turn-Off Slew Rate**
- **Integrated Miller Clamp**
- **dv/dt Immunity up to 100V/ns**
- **Paralleling Capability**
- **Zero Reverse Recovery Charge**
- **High Frequency Operation up to 2MHz**
- **Available in a Green TO-247-4 Package**

APPLICATIONS

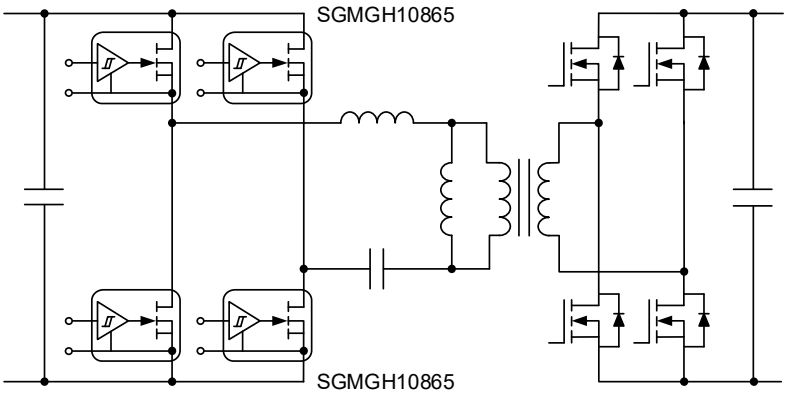
High-Power Switch-Mode Power Supplies
AC/DC, DC/DC, DC/AC Converters
Half-Bridge and Full-Bridge Converters
Data Center/AI Server PSU
Air Conditioner, Solar Inverter, Motor Drive
Automotive OBC & DC/DC Converter

SIMPLIFIED SCHEMATIC

Totem Pole PFC



LLC Resonant Converter

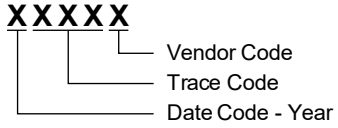


PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGMGH10865	TO-247-4	-55℃ to +150℃	SGMGH10865TON4G	2TOON4 XXXXX	Tube, 30

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Drain Voltage 650V
Drain Voltage, Transient (1) 800V
Drain Voltage, Pulsed (2) 750V
Drain Current (T_C = +25℃) 63A
Drain Current (T_C = +100℃) 40A
Drain Current, Pulsed (T_J = +25℃) 127A
Drain Current, Pulsed (T_J = +150℃) 64A
Gate Input Voltage ..... -0.6V to 26V
Gate Input Voltage, Pulsed (2) ..... -10V to 26V
Drain-to-Source Slew Rate, dv/dt 100V/ns
Total Dissipation 305W
Package Thermal Resistance
TO-247-4, $R_{\theta JA}$ (3) ..... 36.78℃/W
TO-247-4, $R_{\theta JC\_TOP}$ ..... 11.22℃/W
TO-247-4, $R_{\theta JC\_BOTTOM}$ ..... 0.41℃/W
Junction Temperature ..... -55℃ to +150℃
Storage Temperature Range ..... -55℃ to +150℃
ESD Susceptibility (4) (5)
HBM ..... ±2000V
CDM ..... ±1000V

NOTES:

1. t_{PULSE} < 200μs.

2. t_{PULSE} < 100ns.

3. According to standards defined in JESD51 and JESD51-1, thermal characteristic of the package is simulated. $R_{\theta JA}$ is determined with the device mounted on one square inch of copper pad, single layer 2oz copper on FR4 board.

4. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.

5. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

RECOMMENDED OPERATING CONDITIONS

Gate Input High Voltage ..... 10V to 24V
Gate Input Low Voltage ..... -0.3V to 0.3V

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

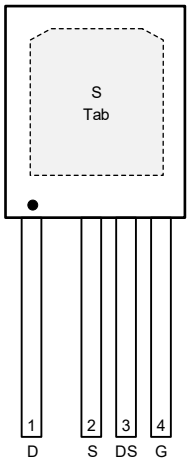
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

(TOP VIEW)



TO-247-4

PIN DESCRIPTION

PIN	NAME	FUNCTION
1	D	Drain of Power GaN FET.
2, Tab	S	Source of Power GaN FET.
3	DS	Driver Source.
4	G	Gate Input. Connect to the drive output of controller or gate driver.

ELECTRICAL CHARACTERISTICS

(T_J = +25℃, V_{GS} = 15V, V_{DS} = 400V, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Gate Characteristics							
Gate Input Threshold Voltage (1)	V_{G_HI}	Gate Rising			4		V
Gate Input Low Threshold (1)	V_{G_LO}	Gate Falling			3.3		
Gate Quiescent Current	I_{G_Q}	V_{GS} = 15V, V_{DS} = 0V			1.9	5.2	mA
Power GaN FET							
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0V, V_{DS} = 650V			2	20	μA
Drain-to-Source On-State Resistance (1)	R_{DSON}	V_{GS} = 15V, I_{DS} = 8A	T_J = +25℃		27	37	mΩ
			T_J = +150℃		55		
Source-to-Drain Reverse Voltage	V_{SD}	V_{GS} = 0V, I_{SD} = 4A			2.3		V
Total Gate Charge (1)	Q_G				12.9		nC
Output Charge (1)	Q_{OSS}	V_{GS} = 0V, V_{DS} = 400V			132		
Reverse Recovery Charge (1)	Q_{RR}				0		
Input Capacitance (1)	C_{ISS}				509		pF
Output Capacitance (1)	C_{OSS}	V_{GS} = 0V, V_{DS} = 400V			179		pF
Effective Output Capacitance, Energy Related (1)	C_{O_ER}				253		
Effective Output Capacitance, Time Related (1)	C_{O_TR}				331		
Switch Characteristics							
Minimum Input Pulse Width that Changes the Output (1)	t_{GH_PW}				20		ns
Minimum On Time (1)					100		
Turn-On Delay Time(1)	t_{D_ON}				30		
Rise Time (1)	t_R				10		
Turn-Off Delay Time(1)	t_{D_OFF}				25		
Fall Time (1)	t_F				10		

NOTE: 1. Not 100% tested and guaranteed by design.

TYPICAL PERFORMANCE CHARACTERISTICS

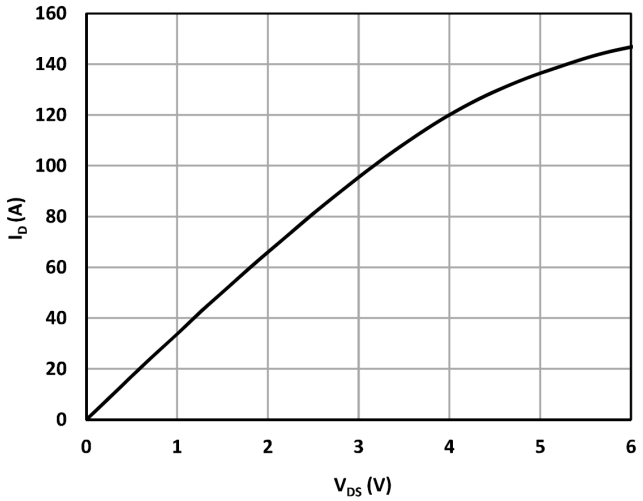


Figure 1. Drain Current vs. Drain-to-Source Voltage, T_J=25°C

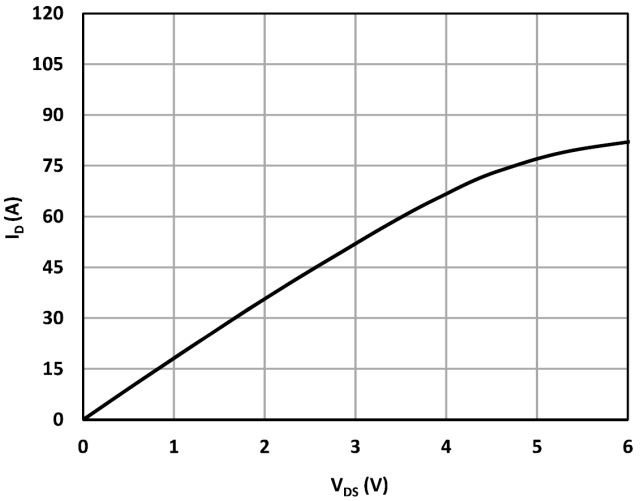


Figure 2. Drain Current vs. Drain-to-Source Voltage, T_J=150°C

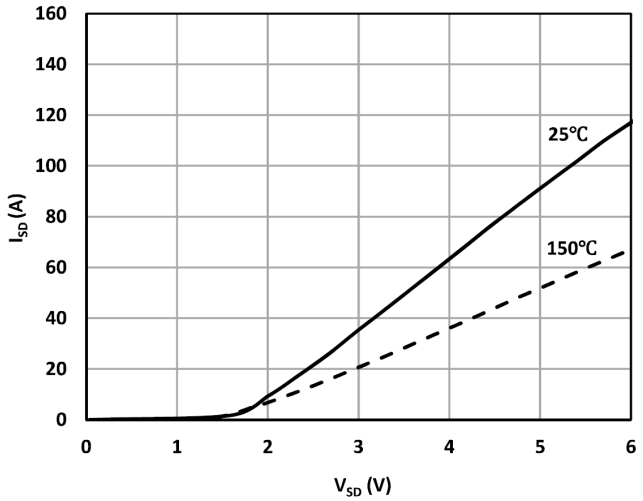


Figure 3. Source-Drain Reverse Conduction Voltage, T_J=25°C

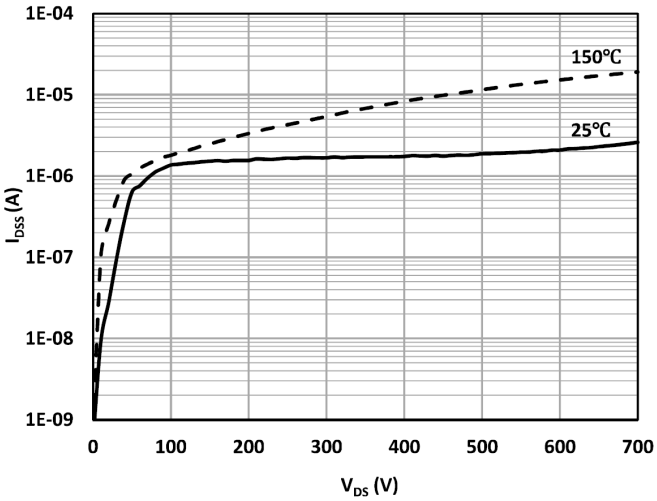


Figure 4. Drain Leakage Current vs Drain Voltage

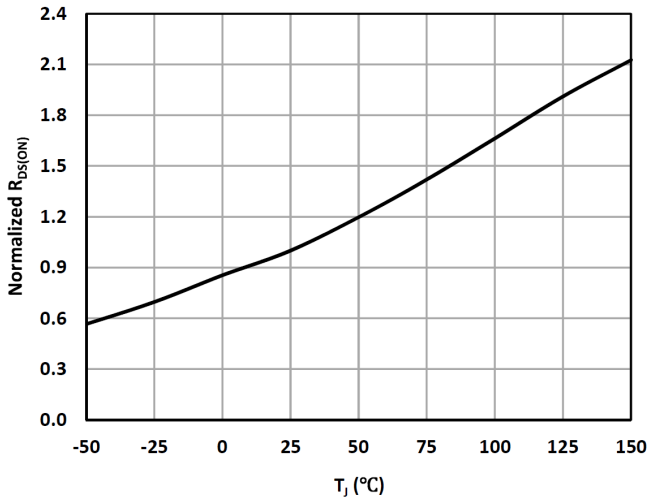


Figure 5. Normalized $R_{DS(ON)}$ vs Temperature

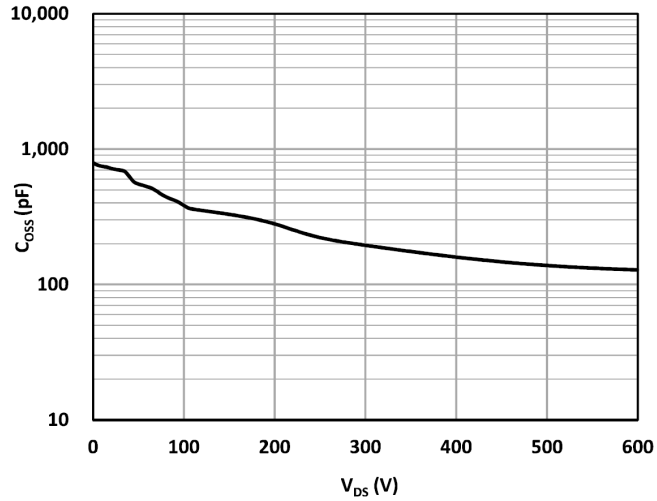


Figure 6. Output Capacitance vs Drain Voltage

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

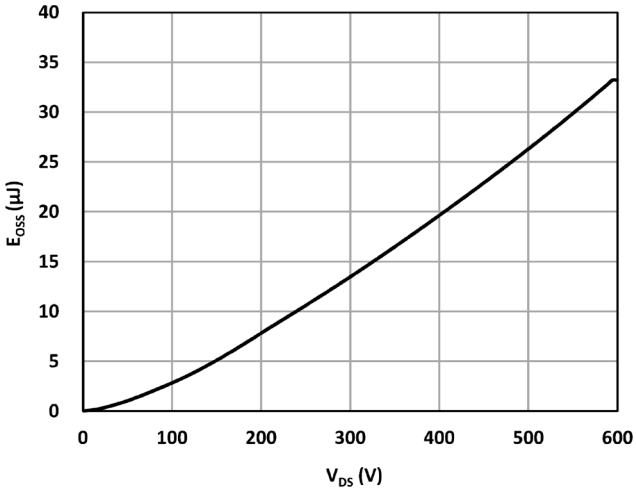


Figure 7. Output Capacitance Stored Energy vs Drain Voltage

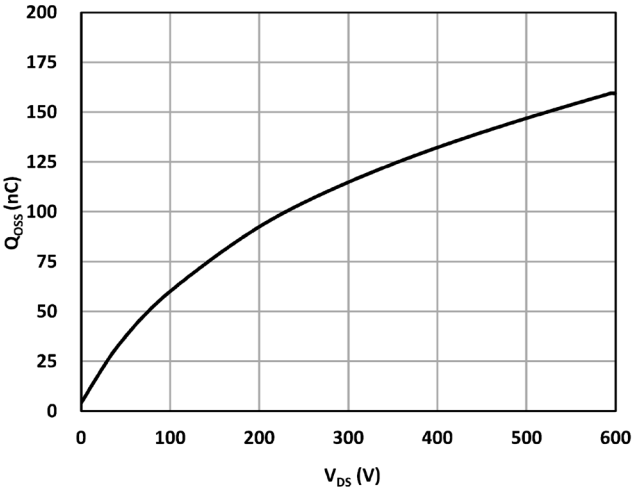


Figure 8. Output Charges vs Drain Voltage

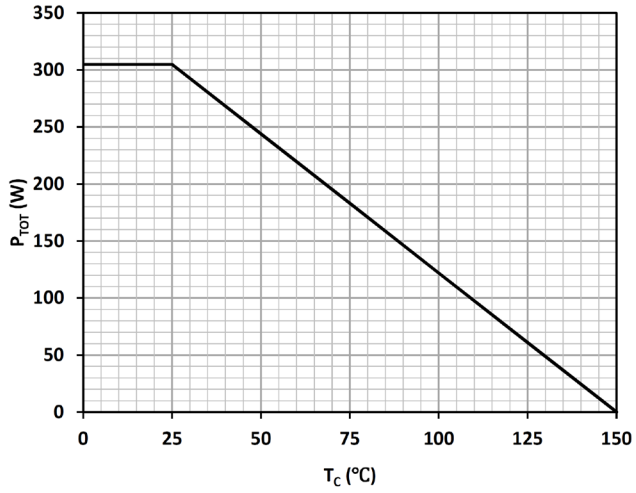


Figure 9. Power Dissipation

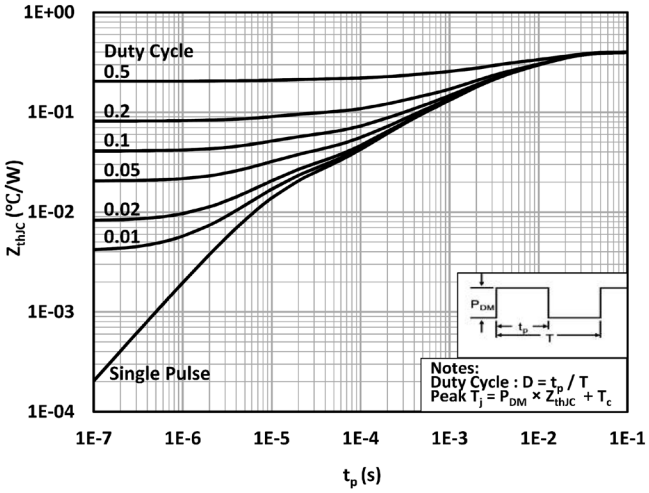


Figure 10. Max. Transient Thermal Impedance

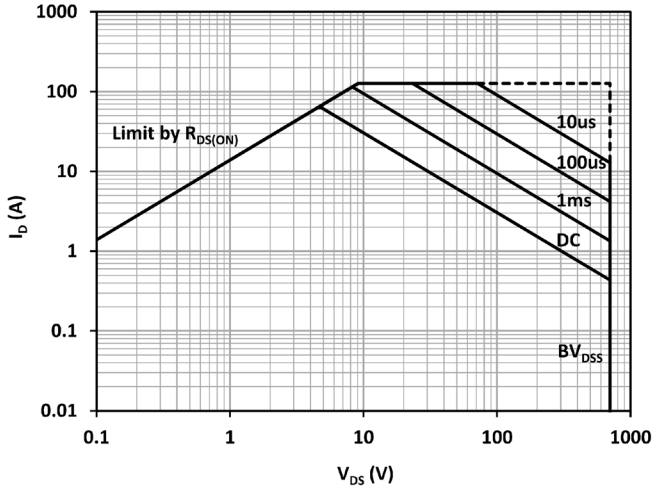


Figure 11. Safe Operating Area, T_J=25°C

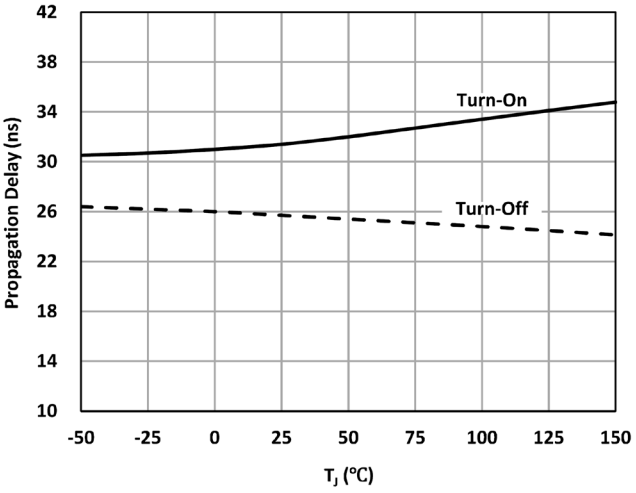


Figure 12. Turn-On/Off Propagation Delay vs Temperature

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

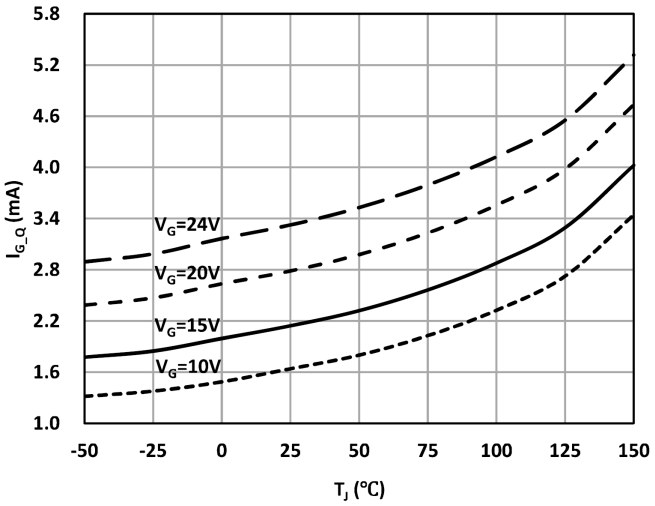


Figure 13. Gate Quiescent Current vs Temperature

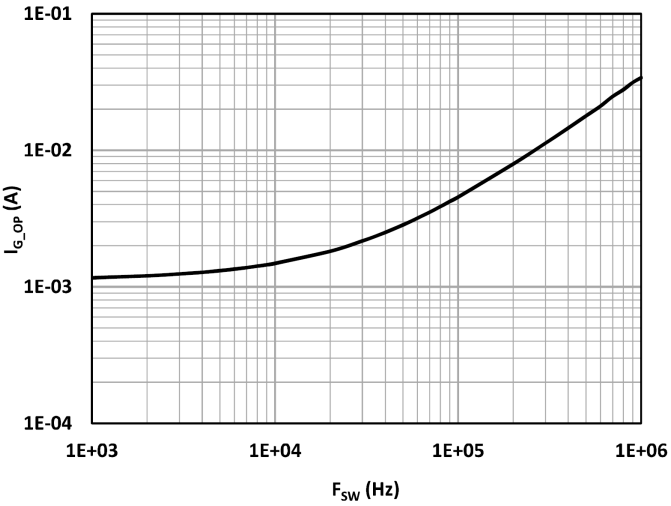


Figure 14. Gate Operating Current vs Switching Frequency

FUNCTIONAL BLOCK DIAGRAM

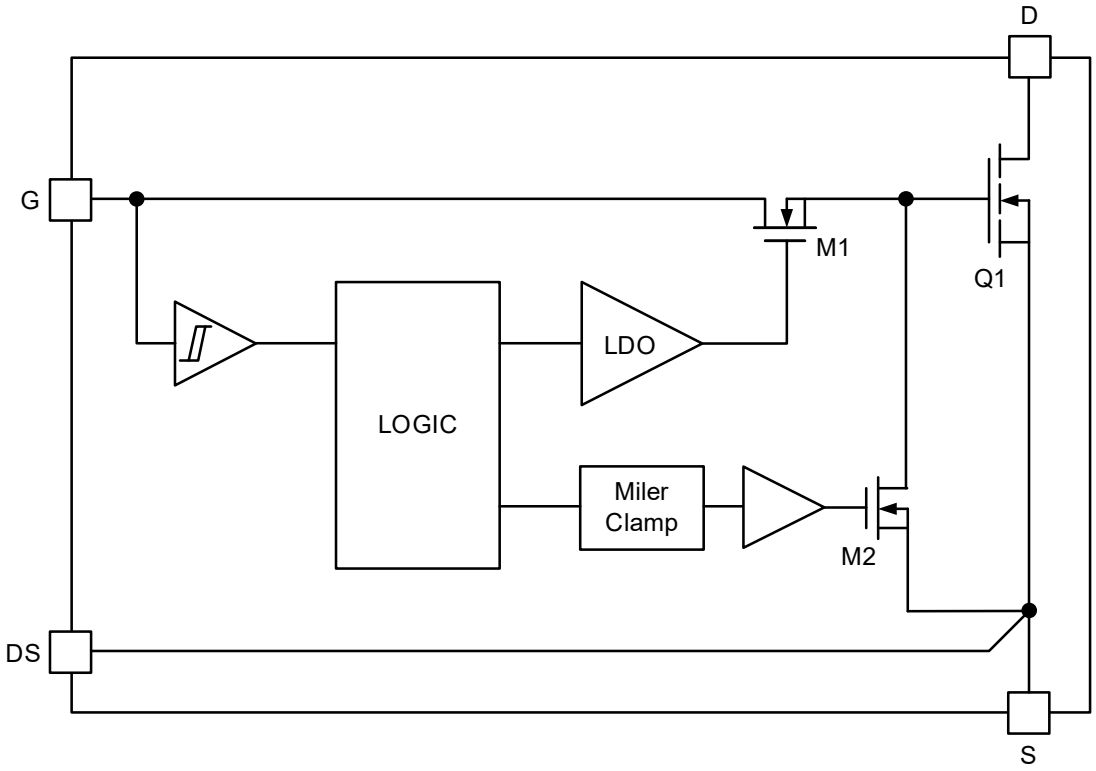


Figure 15. Block Diagram

DETAILED DESCRIPTION

The SGMGH10865 is a 650V GaNFET IC integrating a high-performance enhancement-mode GaN FET with advanced features, offering the most reliable, efficient, and easy-to-use GaN power device.

The SGMGH10865 features a gate clamp to provide a wide G input voltage range of 10V to 24V. With accurate LDO-based circuitry, the gate voltage is tightly regulated to protect the GaN FET from excessive voltage stress while maximizing performance. The SGMGH10865 allows adjusting both the turn-on and turn-off slew rates of the GaN FET by adding external gate resistors, optimizing both EMI and efficiency.

Highly integrated with a GaN FET and robust protection circuitry in a TO-247-4 package, the SGMGH10865 offers simple setup with low component count and drives next-generation high-frequency and high-power applications.

Input and Output

The SGMGH10865 has an input pin, G, to control the integrated GaN FET. When the input G voltage exceeds the input high threshold (4V TYP), the SGMGH10865 propagates the input signal to the gate of GaN FET, turning the GaN FET on and shorting the drain, D, to the source, S, with an on-resistance of 27mΩ (TYP). When the input G voltage falls below the input low threshold (3.3V TYP), the SGMGH10865 blocks the input-signal propagation and pulls down the gate of GaN FET to S, turning the GaN FET off and opening the output of D. Figure16 illustrates the timing diagram of the input and output with the gate-to-source voltage of the GaN FET, V_{GS}. The SGMGH10865 features a 20ns (TYP) input deglitch filter for turn-on to remove unwanted pulses from the G input. A narrow input pulse exceeding this deglitch delay time will be extended to a minimum output pulse of 100ns (TYP).

The SGMGH10865 provides a wide G input voltage range of 10V to 24V for the maximum flexibility. This is achieved by integrating internal gate clamp driven by an accurate LDO-based circuitry, ensuring a tightly regulated gate voltage to protect the GaN FET from excessive voltage stress while maximizing the performance.

The internal circuitry of the SGMGH10865 is powered from the G input, eliminating the need for a sustainable supply voltage from an external power source.

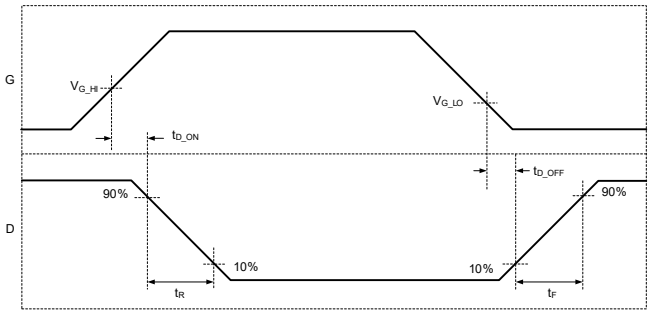


Figure 16. Timing Diagram of Input and Output

Adjustable Turn-On and Turn-Off Slew Rate

The SGMGH10865 supports users the ability to adjust both the turn-on and turn-off slew rates of the GaN FET independently. This is achieved by adding external gate resistors and a diode between the driver output and the G pin of SGMGH10865 as shown in Figure 17, targeting optimization of efficiency, reliability, and EMI performance.

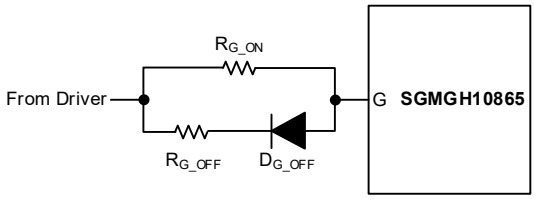


Figure 17. Configuration of Adjustable Turn-On and Turn-Off Slew Rate

Integrated Miller Clamp

GaN FETs can switch much faster than traditional silicon-based MOSFETs, resulting in a higher dv/dt slope of the drain voltage. The SGMGH10865 integrates a Miller clamp with a strong pull-down strength of 0.5Ω (TYP) at the gate to provide a robust low impedance path necessary for eliminating high dv/dt induced gate turn-on. This feature allows removing the negative power supply for gate drivers in conventional designs.

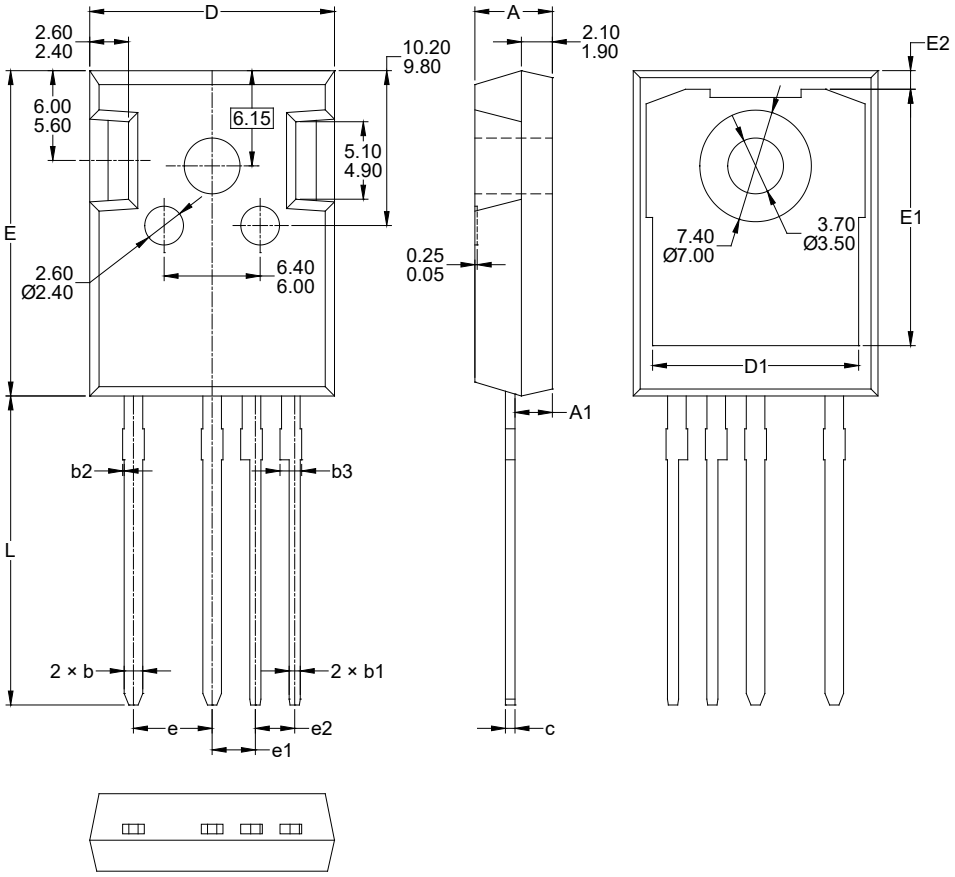
REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original to REV.A (JUNE 2026)	Page
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

TO-247-4



Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	4.900	-	5.100
A1	2.310	-	2.510
b	1.100	-	1.300
b1	0.650	-	0.790
b2	-	-	0.200
b3	1.100	-	1.440
c	0.580	-	0.660
D	15.700	-	15.900
D1	13.100	-	13.500
E	20.900	-	21.100
E1	16.250	-	16.850
E2	1.050	-	1.350
e	5.080 BSC		
e1	2.790 BSC		
e2	2.540 BSC		
L	19.800	-	20.100

NOTES:
1. This drawing is subject to change without notice.
2. The dimensions do not include mold flashes, protrusions or gate burrs.