SGM41548
High Input Voltage, 3.78A Single-Cell Battery Charger with NVDC Power Path Management and PD PHY

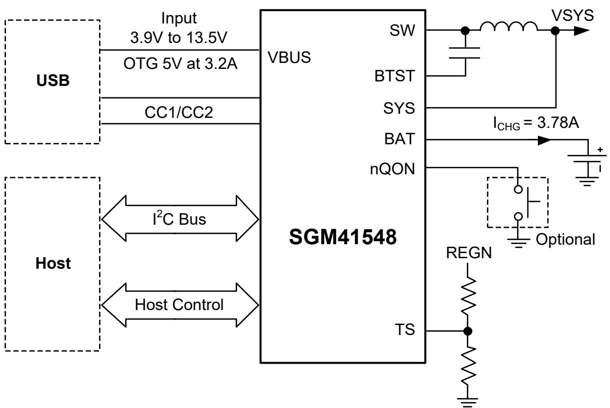
FEATURES

- High Efficiency, 1.5MHz, Synchronous Buck Charger
  - 94.7% Charge Efficiency at 1A from 5V Input
  - 91.6% Charge Efficiency at 2A from 9V Input
  - Selectable Pulse Skip Mode (PSM) for Light Load Efficiency
- USB On-The-Go (OTG) Support (Boost Mode)
  - Boost Converter with up to 3.2A Output
  - Boost Efficiency of 95.5% at 0.5A and 94.1% at 1A
  - Accurate Hiccup Mode Over-Current Protection
  - Soft-Start Capable with up to 500μF Capacitive Load
  - Output Short-Circuit Protection
- Single Input for USB or High Voltage Adapters
  - 3.9V to 13.5V Operating Input Voltage Range
  - 22V Absolute Maximum Input Voltage Rating
  - Programmable Input Current Limit and Dynamic Power Management (IINDPM, 100mA to 3.3A with 100mA Resolution) to Support USB 2.0 and USB 3.0 Standards and High Voltage Adapters
  - Maximum Power Tracking by Programmable Input Voltage Limit (VINDPM) with Selectable Offset
  - VINDPM Tracking of Battery Voltage
  - Auto Detect USB BC1.2, SDP, CDP, DCP and Non-Standard Adapters
  - Support PD 3.2 except Fast Role Swap Function
  - Dual-Role PD Compatible
  - Cable Plug and Orientation Detection
- High Battery Discharge Efficiency with 26mΩ Switch
- Battery Discharge MOSFET up to 12A
- Integrated ADC for System Monitor
- Narrow Voltage DC (NVDC) Power Path Management
  - Instant-On with No or Highly Depleted Battery
  - Ideal Diode Operation in Battery Supplement Mode
- Ship Mode, Wake-Up and Full System Reset Capability by Battery FET Control
- Flexible Autonomous and I^{2}C Operation Modes for Optimal System Performance
- Fully Integrated Switches, Current Sense and Compensation
- External Direct Charging Path Enable Output
- 1.5μA Ship Mode Low Battery Leakage Current
- High Accuracy
  - ±0.5% Charge Voltage Regulation (10mV/Step)
  - ±5% Charge Current Regulation at 1.38A
  - ±6% Input Current Regulation at 0.9A
- Safety
  - Battery Temperature Sensing (Charge/Boost Modes)
  - Thermal Regulation and Thermal Shutdown
  - Input Under-Voltage Lockout (UVLO)
  - Input Over-Voltage (ACOV) Protection

APPLICATIONS

Smart Phones, EPOS
Portable Internet Devices and Accessory

SIMPLIFIED SCHEMATIC



GENERAL DESCRIPTION

The SGM41548 is a battery charger and system power path management device with PD PHY for using with single-cell Li-Ion or Li-polymer batteries. This highly integrated 3.78A device is capable of fast charging and supports a wide input voltage range suitable for smart phones, tablets and portable systems. I^2C programming makes it a very flexible powering and charger design solution.

The device includes four main power switches: input reverse blocking FET (RBFET, Q1), high-side switching FET for Buck or Boost mode (HSFET, Q2), low-side switching FET for Buck or Boost mode (LSFET, Q3) and battery FET that controls the interconnection of the system and battery (BATFET, Q4). The bootstrap diode for the high-side gate driving is also integrated. The internal power path has a very low impedance that reduces the charging time and maximizes the battery discharge efficiency. Moreover, the input voltage and current regulations provide maximum charging power delivery to the battery with various types of input sources.

A wide range of input sources are supported, including standard USB hosts, charging ports and USB compliant high voltage adapters. The default input current limit is automatically selected based on the built-in USB interface. This limit is determined by the detection circuit in the system (e.g. USB PHY). The SGM41548 is USB 2.0 and USB 3.0 power specifications compliant with input current and voltage regulation. It also meets USB On-The-Go (OTG) power rating specification and is capable of boosting the battery voltage to supply up to 9V (MAX) on VBUS with 3.2A (MAX) current limit.

The system voltage is regulated slightly above the battery voltage by the power path management circuit and is kept above the programmable minimum system voltage (3.5V by default). Therefore, system power is maintained even if the battery is completely depleted or removed. Dynamic power management (DPM) feature is also included that automatically reduces the charge current if the input current or voltage limit is reached. If the system load continues to increase after reduction of charge current down to zero, the power path management provides the deficit from battery by discharging battery to the system until the system power demand is fulfilled. This is called supplement mode, which prevents the input source from overloading.

Starting and termination of a charging cycle can be accomplished without software control. The sensed battery voltage is used to decide for starting phase of charging in one of the five phases of charging cycle: trickle charge, pre-charge, fast charge (constant current and constant voltage) and optional top-off charge. When the charge current falls below a preset limit and the battery voltage is above recharge threshold, the charger function will automatically terminate and end the charging cycle. If the voltage of a charged battery falls below the recharge threshold, the charger begins another charging cycle.

Several safety features are provided in the SGM41548 such as over-voltage and over-current protections, battery temperature monitoring, charging safety timing, thermal shutdown and input UVLO. TS pin is connected to an NTC thermistor for battery temperature monitoring and protection in both charge and Boost modes according to JEITA profile. This device also features thermal regulation in which the charge current is reduced, if the junction temperature exceeds 80℃ or 120℃ (selectable).

Charging status is reported by the PD_nINT output when CH_INT_STAT bit is 0b1 and fault/status bits. A negative pulse is sent to the nINT output pin as soon as a fault occurs to notify the host. BATFET reset control is provided by nQON pin to exit ship mode or for a full system reset.

The device also provides an 8-bit analog-to-digital converter (ADC) for monitoring input and charge current and input/battery/system/TS voltages.

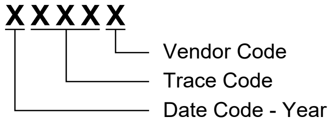
The SGM41548 is available in a Green TQFN-4×4-24L package.

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM41548	TQFN-4×4-24L	-40℃ to +85℃	SGM41548YTQF24G/TR	SGM41548 YTQF24 XXXXX	Tape and Reel, 3000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Voltage Range (with Respect to GND)
- VBUS (Converter Not Switching) .... -2V to 22V
- BTST, PMID (Converter Not Switching) .... -0.3V to 22V
- SW .... -2V to 16V
- SW (Peak for 10ns Duration) .... -3V to 16V
- CC1, CC2 .... -0.3V to 22V
- BTST to SW .... -0.3V to 6V
- D+, D- .... -0.3V to 6V
- REGN, TS, nCE, BAT, SYS (Converter Not Switching) .... -0.3V to 6V
- SDA, SCL, nINT, nQON, PD_nINT .... -0.3V to 6V

Output Sink Current
- nINT 6mA

Package Thermal Resistance
- TQFN-4×4-24L, θ_{JA} .... 26.1℃/W
- TQFN-4×4-24L, θ_{JB} .... 7.4℃/W
- TQFN-4×4-24L, $\theta_{JC\ (TOP)}$ .... 23.9℃/W
- TQFN-4×4-24L, $\theta_{JC\ (BOT)}$ .... 1.8℃/W

Junction Temperature .... +150℃

Storage Temperature Range .... -65℃ to +150℃

Lead Temperature (Soldering, 10s) .... +260℃

ESD Susceptibility (1) (2)

HBM .... ±4000V

CDM .... ±1000V

NOTES:

1. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.
2. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

RECOMMENDED OPERATING CONDITIONS

Input Voltage Range, V_{VBUS} .... 3.9V to 13.5V

Input Current (VBUS), I_{IN} .... 3.3A (MAX)

Output DC Current (SW), I_{SWOP} .... 3.78A (MAX)

Battery Voltage, V_{BATOP} .... 4.77V (MAX)

Fast Charging Current, I_{CHGOP} .... 3.78A (MAX)

Discharging Current (Continuous), I_{BATOP} .... 9A (MAX)

Discharging Current (2ms), I_{BATOP} .... 12A (MAX)

Operating Junction Temperature Range ...... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

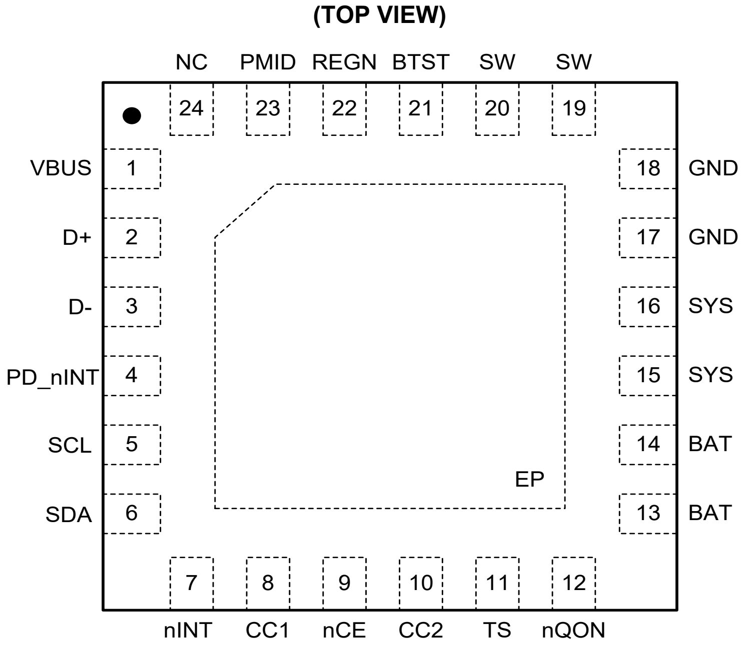
ESD SENSITIVITY CAUTION

This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION



TQFN-4×4-24L

PIN DESCRIPTION

PIN	NAME	TYPE	FUNCTION
1	VBUS	P	Charger Input (V_{IN}). The internal N-channel reverse blocking MOSFET (RBFET) is connected between VBUS and PMID pins. Connect a 1μF ceramic capacitor from VBUS pin to GND close to the device.
2	D+	AIO	Positive USB Data Line. D+/D- based USB device protocol detection and voltage of this pin can be set by DP_VSET[1:0].
3	D-	AIO	Negative USB Data Line. D+/D- based USB device protocol detection and voltage of this pin can be set by DM_VSET[1:0].
4	PD_nINT	DO	PD PHY Open-Drain Interrupt Output. Connect the PD_nINT pin to a logic rail through 10kΩ resistor. The PD_nINT pin pulls low to request the host to read PD fault. Other Function - Open-Drain Charge Status Output (STAT Pin). Use a 10kΩ pull-up to the logic high rail (or an LED + a resistor). The STAT pin acts as follows: During charge: low (LED ON). Charge completed or charger in sleep mode: high (LED OFF). Charge suspended (in response to a fault): 1Hz, 50% duty cycle pulses (LED BLINKS). The function can be disabled via CH_INT_STAT and EN_ICHG_MON[1:0] register.
5	SCL	DI	I^2C Clock Signal. Use a 10kΩ pull-up to the logic high rail.
6	SDA	DIO	I^2C Data Signal. Use a 10kΩ pull-up to the logic high rail. The SDA line is forced to release and the I^2C interface block is reset when the SCL or SDA held low 25ms I^2C timeout fault occurs.
7	nINT	DO	Open-Drain Interrupt Output Pin. Use a 10kΩ pull-up to the logic high rail. The nINT pin is active low and sends a negative 256μs pulse to inform the host about a new charger status update or a fault.
8	CC1	AIO	Type-C Connector Configuration Channel 1. It is used to detect a device plug event, determine the cable orientation, transmit or receive PD protocols.
9	nCE	DI	Charge Enable Input Pin (Active Low). Battery charging is enabled when CHG_CONFIG bit is 0b1 and nCE pin is pulled low. Do not leave nCE pin floating.
10	CC2	AIO	Type-C Connector Configuration Channel 2. It is used to detect a device plug event, determine the cable orientation, transmit or receive PD protocols.

PIN DESCRIPTION (continued)

PIN	NAME	TYPE	FUNCTION
11	TS	AI	Temperature Sense Input Pin. Connect to the battery NTC thermistor that is grounded on the other side. To program operating temperature window, it can be biased by a resistor divider between REGN pin and GND. Charge suspends if TS voltage goes out of the programmed range. It is recommended to use a 103AT-2 type thermistor. If NTC or TS pin function is not needed, use a 10kΩ/10kΩ pair for the resistor divider.
12	nQON	DI	BATFET On/Off Control Pin. Use an internal pull-up to a small voltage for maintaining the default high logic (whenever a source or battery is available). In the ship mode, the BATFET is off. To exit the ship mode and turn BATFET on, a logic low pulse with a duration of $t_{SHIPMODE}$ (1s TYP) can be applied to nQON. When the VBUS source is not connected, a logic low pulse with a duration of t_{QON_RST} (10s TYP) resets the system power (SYS) by turning BATFET off for t_{BATFET_RST} (320ms TYP) and then goes back to provide a full power reset for system. The nQON pin can be left floating if its function is not used.
13, 14	BAT	P	Battery Positive Terminal Pin. Use a 10μF capacitor between BAT pin and GND close to the device. The SYS and BAT pins are internally connected by BATFET with current sensing capability.
15, 16	SYS	P	Connection Point to Converter Output. The SYS is connected to the converter LC filter output that powers the system. The BAT to SYS internal current (power from battery to system) is sensed. Connect 2 × 10μF capacitors between SYS pin and GND close to the device.
17, 18	GND	—	Ground Pin of the Device.
19, 20	SW	P	Switching Node Output. Connect SW pin to the output inductor. Connect a 47nF bootstrap capacitor from SW pin to BTST pin.
21	BTST	P	High-side Driver Positive Supply. It is internally connected to the bootstrap diode cathode. Use a 47nF ceramic capacitor from SW pin to BTST pin.
22	REGN	P	LDO Output that Powers LSFET Driver and Internal Circuits. Internally, the REGN pin is connected to the anode of the bootstrap diode. Place a 2.2μF (10V rating) ceramic capacitor between REGN pin and GND. It is recommended to place the capacitor close to the REGN pin.
23	PMID	P	PMID Pin. The PMID is the actual higher voltage port of converter (Buck or Boost) and is connected to the drain of the reverse blocking MOSFET (RBFET) and the drain of HSFET. Connect 2 × 10μF ceramic capacitors from PMID pin to GND. It is the proper point for decoupling of high frequency switching currents.
24	NC	—	No Connection.
EP	Exposed Pad	P	Thermal Pad and Ground Reference. It is the ground reference for the device and also the thermal pad to conduct heat from the device (not suitable for high current return). Tie externally to the PCB ground plane (GND). Thermal vias under the pad are needed to conduct the heat to the PCB ground planes.

NOTE: AI = analog input, AO = analog output, AIO = analog input and output, DI = digital input, DO = digital output, DIO = digital input and output, P = power.

ELECTRICAL CHARACTERISTICS

(V_{VBUS_UVLOZ} < V_{VBUS} < V_{VBUS_OV} and V_{VBUS} > V_{BAT} + V_{SLEEP}, T_J = -40℃ to +125℃, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER		SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Quiescent Currents							
Battery Discharge Current (BAT, SW, SYS) in Buck Mode		I_{BQ_VBUS}	V_{BAT} = 4.5V, V_{VBUS} < V_{VBUS_UVLOZ}, leakage between BAT and VBUS, BATFET off, ADC disabled, PD PHY in shutdown mode		0.1	1.5	μA
Battery Discharge Current (BAT) in Buck Mode		$I_{BQ\_HIZ\_BOFF}$	V_{BAT} = 4.5V, HIZ mode and BATFET_DIS = 1 or no VBUS, I²C disabled, BATFET disabled, ADC disabled, PD PHY in shutdown mode		1.5	3.4	μA
			V_{BAT} = 4.5V, HIZ mode and BATFET_DIS = 1 or no VBUS, I²C disabled, BATFET disabled, ADC disabled, PD PHY CC in UFP mode		114	170	
			V_{BAT} = 4.5V, HIZ mode and BATFET_DIS = 1 or no VBUS, I²C disabled, BATFET disabled, ADC disabled, PD PHY CC in DRP mode, DCSRCDRP[6:0] = 010 1000		130	190	
Battery Discharge Current (BAT, SW, SYS)		$I_{BQ\_HIZ\_BON}$	V_{BAT} = 4.5V, HIZ mode and BATFET_DIS = 0 or no VBUS, I²C disabled, BATFET enabled, ADC disabled, PD PHY in shutdown mode		3.5	8	μA
			V_{BAT} = 4.5V, HIZ mode and BATFET_DIS = 0 or no VBUS, I²C disabled, BATFET enabled, ADC disabled, PD PHY CC in UFP mode		115	180	
Input Supply Current (VBUS) in Buck Mode		I_{VBUS_HIZ}	V_{VBUS} = 5V, HIZ mode and BATFET_DIS = 1, no battery		12	18	μA
			V_{VBUS} = 12V, HIZ mode and BATFET_DIS = 1, no battery		25	35	
		I_{VBUS}	V_{VBUS} = 12V, V_{VBUS} > V_{BAT}, converter not switching		2.5	3.5	mA
			V_{BAT} = 3.8V, I_{SYS} = 0A, V_{VBUS} > V_{BAT}, V_{VBUS} > V_{VBUS_UVLOZ}, converter switching, BATFET off		2.3		
Battery Discharge Current in Boost Mode		I_{BOOST}	V_{BAT} = 4.2V, I_{VBUS} = 0A, converter switching		3.2		mA
BAT Pin and VBUS Pin Power-Up							
VBUS Operating Range		V_{VBUS_OP}	V_{VBUS} rising	3.9		13.5	V
VBUS UVLO to Have Active I²C (with No Battery)		V_{VBUS_UVLOZ}	V_{VBUS} rising, T_J = +25℃	3	3.25	3.5	V
I²C Active Hysteresis		$V_{VBUS\_UVLOZ\_HYS}$	V_{VBUS} falling from above V_{VBUS_UVLOZ}		250		mV
V_{VBUS} Minimum (as One of the Conditions) to Turn on REGN		$V_{VBUS\_PRESENT}$	V_{VBUS} rising, T_J = +25℃	3.3	3.55	3.82	V
V_{VBUS} Hysteresis (as One of the Conditions) to Turn on REGN		$V_{VBUS\_PRESENT\_HYS}$	V_{VBUS} falling from above $V_{VBUS\_PRESENT}$		400		mV
Sleep Mode Falling Threshold		V_{SLEEP}	V_{VBUS} - V_{BAT}, $V_{VBUSMIN\_FALL}$ ≤ V_{BAT} ≤ V_{BAT_REG}, V_{VBUS} falling, T_J = +25℃, initial accuracy	35	80	135	mV
Sleep Mode Rising Threshold		V_{SLEEPZ}	V_{VBUS} - V_{BAT}, $V_{VBUSMIN\_FALL}$ ≤ V_{BAT} ≤ V_{BAT_REG}, V_{VBUS} rising, T_J = +25℃, initial accuracy	180	240	300	mV
VBUS Over-Voltage Rising Threshold	6.5V Setting	$V_{VBUS\_OV\_RISE}$	OVP[1:0] = 01, V_{VBUS} rising	6.32	6.5	6.68	V
	10.5V Setting		OVP[1:0] = 10, V_{VBUS} rising	10.3	10.5	10.7	
	14V Setting		OVP[1:0] = 11, V_{VBUS} rising	13.8	14	14.2	
VBUS Over-Voltage Hysteresis	6.5V Setting	$V_{VBUS\_OV\_HYS}$	OVP[1:0] = 01		100		mV
	10.5V Setting		OVP[1:0] = 10		250		
	14V Setting		OVP[1:0] = 11		300		
BAT Voltage to Have Active I²C (No Source on VBUS)		V_{BAT_UVLOZ}	V_{BAT} rising	2.23	2.45	2.67	V
BAT Depletion Threshold		$V_{BAT\_DPL\_FALL}$	V_{BAT} falling	2.14	2.2	2.26	V
		$V_{BAT\_DPL\_RISE}$	V_{BAT} rising	2.34	2.4	2.46	
BAT Depletion Rising Hysteresis		$V_{BAT\_DPL\_HYS}$			200		mV

ELECTRICAL CHARACTERISTICS (continued)

($V_{VBUS\_UVLOZ} < V_{VBUS} < V_{VBUS\_OV}$ and $V_{VBUS} > V_{BAT} + V_{SLEEP}$, T_J = -40℃ to +125℃, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Bad Adapter Detection Current (Internal Current Sink)	I_{BAD_SRC}	Sink current from VBUS to GND			25		mA
Bad Adapter Detection (VBUS Voltage Drop) Falling Threshold	$V_{VBUSMIN\_FALL}$	V_{VBUS} falling		3.7	3.8	3.9	V
Bad Adapter Detection (VBUS Voltage Drop) Hysteresis	$V_{VBUSMIN\_HYS}$				170		mV
Power Path Management							
System Regulation Voltage	V_{SYS}	I_{SYS} = 0A, V_{BAT} = 4.4V, $V_{BAT} > V_{SYS\_MIN}$, BATFET_DIS = 1			V_{BAT} + 50mV		V
Minimum DC System Voltage Output	V_{SYS_MIN}	I_{SYS} = 0A, V_{BAT} < SYS_MIN[2:0] = 101 (3.5V), BATFET_DIS = 1		3.64	3.7		V
Maximum DC System Voltage Output	V_{SYS_MAX}	I_{SYS} = 0A, V_{BAT} = 4.4V, $V_{BAT} > V_{SYS\_MIN}$ = 3.5V, BATFET_DIS = 1		4.4	4.45	4.5	V
Top Reverse Blocking MOSFET On-Resistance between VBUS and PMID - Q1	R_{ON_RBFET}				33		mΩ
Top Switching MOSFET On-Resistance between PMID and SW - Q2	R_{ON_HSFET}	V_{REGN} = 5V			35		mΩ
Bottom Switching MOSFET On-Resistance between SW and GND - Q3	R_{ON_LSFET}	V_{REGN} = 5V			35		mΩ
BATFET Forward Voltage in Supplement Mode	V_{FWD}				30		mV
Battery Charger							
Charge Voltage Program Range	$V_{BAT\_REG\_RANGE}$			3.5		4.77	V
Charge Voltage Step	$V_{BAT\_REG\_STEP}$				10		mV
Charge Voltage Setting	V_{BAT_REG}	VREG[6:0] = 100 0110 (4.200V)	T_J = +25℃	4.19	4.2	4.21	V
			T_J = -40℃ to +85℃	4.182		4.218	
		VREG[6:0] = 101 0000 (4.300V)	T_J = +25℃	4.29	4.3	4.31	
			T_J = -40℃ to +85℃	4.282		4.32	
		VREG[6:0] = 101 1010 (4.400V)	T_J = +25℃	4.39	4.4	4.41	
			T_J = -40℃ to +85℃	4.381		4.42	
		VREG[6:0] = 110 0100 (4.500V)	T_J = +25℃	4.49	4.5	4.51	
			T_J = -40℃ to +85℃	4.482		4.521	
Charge Voltage Setting Accuracy	$V_{BAT\_REG\_ACC}$	V_{BAT_REG} = 4.200V or V_{BAT_REG} = 4.300V or V_{BAT_REG} = 4.400V or V_{BAT_REG} = 4.500V	T_J = +25℃	-0.3		0.3	%
			T_J = -40℃ to +85℃	0.5		0.5	
Charge Current Regulation Range	$I_{CHG\_REG\_RANGE}$			0		3780	mA
Charge Current Regulation Step	$I_{CHG\_REG\_STEP}$				60		mA
Charge Current Regulation Setting	I_{CHG_REG}	V_{BAT} = 3.2V, T_J = +25℃	ICHG[5:0] = 00 0001 (60mA)	0.045	0.06	0.08	A
			ICHG[5:0] = 00 0100 (240mA)	0.205	0.24	0.285	
			ICHG[5:0] = 00 1100 (720mA)	0.66	0.72	0.78	
			ICHG[5:0] = 01 0111 (1.38A)	1.315	1.38	1.445	
			ICHG[5:0] = 10 0010 (2.04A)	1.98	2.04	2.1	
		V_{BAT} = 3.8V, T_J = +25℃	ICHG[5:0] = 00 0001 (60mA)	0.055	0.065	0.075	
			ICHG[5:0] = 00 0100 (240mA)	0.23	0.245	0.255	
			ICHG[5:0] = 00 1100 (720mA)	0.69	0.72	0.75	
			ICHG[5:0] = 01 0111 (1.38A)	1.325	1.38	1.435	
			ICHG[5:0] = 10 0010 (2.04A)	1.98	2.04	2.1	

ELECTRICAL CHARACTERISTICS (continued)

(V_{VBUS_UVLOZ} < V_{VBUS} < V_{VBUS_OV} and V_{VBUS} > V_{BAT} + V_{SLEEP}, T_J = -40℃ to +125℃, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Pre-Charge Current Regulation Setting	I_{PRECHG}	IPRECHG[3:0] = 0101 (180mA), T_J = +25℃		150	180	210	mA
Battery LOW Falling Threshold	V_{BATLOW_FALL}	I_{CHG} = 480mA		2.85	2.97	3.09	V
Battery LOW Rising Threshold	V_{BATLOW_RISE}	Change from pre-charge to fast charging		3.1	3.17	3.24	V
Termination Current Regulation Setting	I_{TERM}	ITERM[3:0] = 0101 (180mA), V_{BAT_REG} = 4.200V, T_J = +25℃	I_{CHG} > 0.72A	160	175	190	mA
			I_{CHG} ≤ 0.72A	160	175	190	
Battery Short Voltage	V_{SHORT}	V_{BAT} falling		1.94	2	2.06	V
	V_{SHORTZ}	V_{BAT} rising		2.14	2.2	2.26	
Battery Short Current	I_{SHORT}	V_{BAT} < V_{SHORTZ}			60		mA
Recharge Threshold below V_{BAT_REG}	V_{RECHG}	V_{BAT} falling, VRECHG[1:0] = 00 (100mV)		85	105	130	mV
		V_{BAT} falling, VRECHG[1:0] = 01 (200mV)		185	205	230	
System Discharge Load Current	I_{SYS_LOAD}	V_{SYS} = 4.2V			30		mA
BATFET MOSFET On-Resistance	R_{ON_BATFET}	V_{BAT} = 4.2V, measured from BAT pin to SYS pin			26	40	mΩ
Input Voltage and Current Regulation (DPM: Dynamic Power Management)							
Input Voltage Regulation Limit	V_{INDPM}	VINDPM[3:0] = 0101	VINDPM_OS[1:0] = 00	4.35	4.4	4.45	V
			VINDPM_OS[1:0] = 01	6.34	6.4	6.46	
			VINDPM_OS[1:0] = 10	7.92	8	8.08	
			VINDPM_OS[1:0] = 11	10.9	11	11.1	
Input Voltage Regulation Accuracy	V_{INDPM_ACC}			-1.2		1.2	%
Input Voltage Regulation Limit Tracking VBAT	V_{DPM_VBAT}	V_{BAT} = 4V, V_{INDPM} = 3.9V, T_J = +25℃, VDPM_BAT_TRACK[1:0] = 11 (300mV)		4.22	4.3	4.38	V
Input Voltage Regulation Accuracy Tracking VBAT	$V_{DPM\_VBAT\_ACC}$			-2		2	%
USB Input Current Regulation Limit	I_{INDPM}	V_{VBUS} = 5V, current pulled from SW, T_J = +25℃	IINDPM[5:0] = 00 0000 (100mA)		95	120	mA
			IINDPM[5:0] = 00 1000 (500mA)	440		520	
			IINDPM[5:0] = 01 0000 (900mA)	810		900	
			IINDPM[5:0] = 01 1100 (1.5A)	1360		1500	
			IINDPM[5:0] = 10 0110 (2A)	1830		2000	
Input Current Limit during System Start-Up Sequence	I_{IN_START}				200		mA
BAT Pin Over-Voltage Protection							
Battery Over-Voltage Threshold	V_{BATOVP_RISE}	As percentage of V_{BAT_REG}, T_J = +25℃	V_{BAT} rising	102.9	103.9	104.9	%
	V_{BATOVP_FALL}		V_{BAT} falling	100.9	101.9	103	
Thermal Regulation and Thermal Shutdown							
Junction Temperature Regulation Threshold	$T_{JUNCTION\_REG}$	Temperature increasing	TREG = 1 (120℃)		120		℃
			TREG = 0 (80℃)		80		
Thermal Shutdown Rising Temperature	T_{SHUT}	Temperature increasing			150		℃
Thermal Shutdown Hysteresis	T_{SHUT_HYS}				30		℃
JEITA Thermistor Comparator (Buck Mode)							
T1 (0℃) Threshold Voltage on TS Pin	V_{T1}	Charge suspends if temperature T is below T1 (T < T1), as percentage of V_{REGN}		72.75	73.25	73.75	%
V_{T1} Falling		As percentage of V_{REGN}		71.1	71.6	72.1	

ELECTRICAL CHARACTERISTICS (continued)

(V_{VBUS_UVLOZ} < V_{VBUS} < V_{VBUS_OV} and V_{VBUS} > V_{BAT} + V_{SLEEP}, T_J = -40℃ to +125℃, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
JEITA Thermistor Comparator (Buck Mode)						
T2 (10℃) Threshold Voltage on TS Pin	V_{T2}	Charge sets to I_{CHG}/2 and the lower of 4.1V and V_{BAT_REG} if T1 < T < T2, as percentage of V_{REGN}	67.6	68.1	68.6	%
V_{T2} Falling		As percentage of V_{REGN}	66.2	66.7	67.2	
V_{T3} Rising	V_{T3}	As percentage of V_{REGN}	45.5	46	46.5	%
T3 (45℃) Threshold Voltage on TS Pin		Charge sets to the lower of 4.1V and V_{BAT_REG} if T3 < T < T4, as percentage of V_{REGN}	44	44.5	45	
V_{T4} Rising	V_{T4}	As percentage of V_{REGN}	35	35.5	36	%
T4 (60℃) Threshold Voltage on TS Pin		Charge suspends if T > T4, as percentage of V_{REGN}	33.6	34.1	34.6	
Cold or Hot Thermistor Comparator (Boost Mode)						
Cold Temperature Threshold (TS Pin Voltage Rising Threshold)	V_{BCOLD}	As percentage of V_{REGN} (approx. -20℃ w/ 103AT)	79.3	80	80.7	%
TS Voltage Falling (Exit from Cold Range to Cool)		As percentage of V_{REGN}	78.3	79	79.7	
Hot Temperature Threshold (TS Pin Voltage Falling Threshold)	V_{BHOT}	As percentage of V_{REGN} (approx. 60℃ w/ 103AT)	30.4	31.1	31.8	%
TS Voltage Rising (Exit from Hot Range to Warm)		As percentage of V_{REGN}	33.7	34.4	35.1	
Charge Over-Current Comparator (Cycle-by-Cycle)						
HSFET Cycle-by-Cycle Over-Current Threshold	I_{HSFET_OCP}	T_J = +25℃	6.65		9.51	A
System Overload Threshold	I_{BATFET_OCP}	T_J = +25℃ (2ms)	12			A
Charge Under-Current Comparator (Cycle-by-Cycle)						
LSFET Under-Current Falling Threshold	I_{LSFET_UCP}	Change rectifier from synchronous mode to non-synchronous mode		500		mA
PWM						
PWM Switching Frequency	f_{SW}	Oscillator frequency, T_J = +25℃; Buck mode	1400	1500	1600	kHz
		Oscillator frequency, T_J = +25℃; Boost mode	400	500	600	
			1400	1500	1600	
Maximum PWM Duty Cycle [(1)]	D_{MAX}			99		%
Boost Mode Operation						
Boost Mode Regulation Voltage	V_{OTG_REG}	V_{BAT} = 3.8V, I_{PMID} = 0A, BOOSTV[2:0] = 010 (5.175V)	5.085	5.175	5.265	V
Boost Mode Regulation Voltage Accuracy	$V_{OTG\_REG\_ACC}$	V_{BAT} = 3.8V, I_{PMID} = 0A, BOOSTV[2:0] = 010 (5.175V)	-1.8		1.8	%
Exit Boost Mode due to Low Battery Voltage	V_{BATLOW_OTG}	V_{BAT} falling, MIN_BAT_SEL = 0	2.95	3	3.05	V
		V_{BAT} rising, MIN_BAT_SEL = 0	3.1	3.2	3.3	
		V_{BAT} falling, MIN_BAT_SEL = 1	2.65	2.7	2.75	
		V_{BAT} rising, MIN_BAT_SEL = 1	2.8	2.9	3	
OTG Mode Maximum Output Current	I_{OTG}	T_J = +25℃, initial accuracy; BOOST_LIM[2:0] = 010 (1.2A)	1.2	1.3	1.4	A
		T_J = +25℃, initial accuracy; BOOST_LIM[2:0] = 100 (2A)	2	2.15	2.3	
		T_J = +25℃, initial accuracy; BOOST_LIM[2:0] = 111 (3.2A)	3.2	3.45	3.7	
OTG Over-Voltage Threshold	V_{OTG_OVP}	Rising threshold	9.78	10	10.22	V
HSFET Under-Current Falling Threshold	I_{OTG_HSZCP}	Change rectifier from synchronous mode to non-synchronous mode		200		mA
REGN LDO						
REGN LDO Output Voltage	V_{REGN}	V_{VBUS} = 9V, I_{REGN} = 40mA	4.75	5.05	5.35	V
		V_{VBUS} = 5V, I_{REGN} = 20mA	4.53	4.65	4.81	

ELECTRICAL CHARACTERISTICS (continued)

(V_{VBUS_UVLOZ} < V_{VBUS} < V_{VBUS_OV} and V_{VBUS} > V_{BAT} + V_{SLEEP}, T_J = -40℃ to +125℃, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER		SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Analog-to-Digital Converter (ADC)							
Resolution		RES	Rising threshold		8		bits
Typical Battery Voltage Range		V_{BAT_RANGE}		2.304		4.851	V
Typical Battery Voltage Resolution		V_{BAT_RES}			10.98		mV
Typical System Voltage Range		V_{SYS_RANGE}		2.304		4.851	V
Typical System Voltage Resolution		V_{SYS_RES}			10.98		mV
Typical V_{VBUS} Voltage Range		V_{VBUS_RANGE}		2.6		15.35	V
Typical V_{VBUS} Voltage Resolution		V_{VBUS_RES}			50		mV
Typical Battery Charge Current Range		I_{BAT_RANGE}		0		6.4	A
Typical Battery Charge Current Resolution		I_{BATRES}			25.1		mA
Typical I_{VBUS} Current Range		I_{VBUS_RANGE}		0		3.313	A
Typical I_{VBUS} Current Resolution		I_{VBUS_RES}			25.1		mA
Typical TS Voltage Range		V_{TS_RANGE}		21		81.273	%
Typical TS Voltage Resolution		V_{TS_RES}			0.543		%
Logic I/O Pin Characteristics (nCE, nQON, SCL and SDA)							
Input Low Threshold	nCE, nQON, SCL, SDA	V_{IL}				0.4	V
Input High Threshold		V_{IH}		0.85			V
Output Low Threshold		V_{OL_SDA}	Sink 2mA			0.4	V
High-Level Leakage Current		I_{BIAS}	Pull up rail 1.8V		0.1	1	μA
Internal nQON Pull-Up		V_{QON}	Battery only mode		V_{BAT} - 0.7		V
			V_{VBUS} ≥ 5V		4.2		
Logic I/O Pin Characteristics (nINT and PD_nINT) - Open-Drain							
Low-Level Output Voltage		V_{OL}	Sink 5mA			0.2	V
Common Normative Signaling Requirements for Transmitter							
Maximum Difference between the Bit-Rate during the Part of the Packet Following the Preamble and the Reference Bit-Rate		$p_{BitRate}$	V_{DD} = 3V to 5.5V			0.25	%
Time from the End of Last Bit of A Frame until the Start of the First Bit of the Next Preamble		$t_{InterFrameGap}$	V_{DD} = 3V to 5.5V	25			μs
Time before the Start of the First Bit of the Preamble When the Transmitter Shall Start Driving the Line		$t_{StartDrive}$	V_{DD} = 3V to 5.5V	-1		1	μs
BMC Common Normative Requirements							
Time to Cease Driving the Line after the End of the Last Bit of the Frame		$t_{EndDriveBMC}$	V_{DD} = 3V to 5.5V			23	μs
Fall Time		t_{Fall}	V_{DD} = 3V to 5.5V	300			ns
Time to Cease Driving the Line after the Final High-to-Low Transition		$t_{HoldLowBMC}$	V_{DD} = 3V to 5.5V	1			μs
Rise Time		t_{Rise}	V_{DD} = 3V to 5.5V	300			ns
Voltage Swing		V_{Swing}	V_{DD} = 3V to 5.5V	1.05	1.125	1.2	V
Transmitter Output Impedance		Z_{Driver}	V_{DD} = 3V to 5.5V, RTX_SEL[1:0] = 10	33		75	Ω

ELECTRICAL CHARACTERISTICS (continued)

(V_{VBUS_UVLOZ} < V_{VBUS} < V_{VBUS_OV} and V_{VBUS} > V_{BAT} + V_{SLEEP}, T_J = -40℃ to +125℃, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
BMC Receiver Normative Requirements						
Time Window for Detecting Non-Idle	$t_{TransitionWindow}$	V_{DD} = 3V to 5.5V	12		20	μs
Receiver Input Impedance	Z_{BmcRx}	V_{DD} = 3V to 5.5V	0.8			MΩ
Type-C Port Control						
DFP 80μA CC Current	DFP80μ	V_{DD} = 3V to 5.5V, T_J = -40℃ to +85℃	70	80	90	μA
DFP 180μA CC Current	DFP180μ	V_{DD} = 3V to 5.5V, T_J = -40℃ to +85℃	160	180	200	μA
DFP 330μA CC Current	DFP330μ	V_{DD} = 3V to 5.5V, T_J = -40℃ to +85℃	290	330	370	μA
UFP Rd	Rd	V_{DD} = 3V to 5.5V	4.7	5.1	5.5	kΩ
UFP Pull-Down Voltage in Dead Battery under DFP80μ and DFP 180μA	V_{DBL}	V_{DD} = 0V			1.7	V
UFP Pull-Down Voltage in Dead Battery under DFP 330μA	V_{DBH}	V_{DD} = 0V			2.75	V

NOTE:

1. Guaranteed by design. Not production tested.

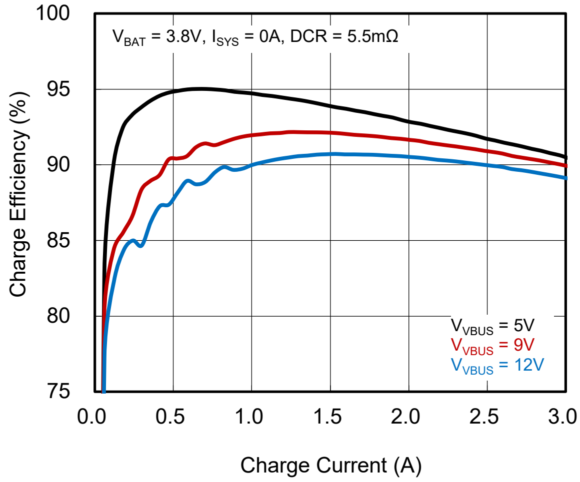
TIMING REQUIREMENTS

(V_{VBUS_UVLOZ} < V_{VBUS} < V_{VBUS_OV} and V_{VBUS} > V_{BAT} + V_{SLEEP}, T_J = +25℃, unless otherwise noted.)

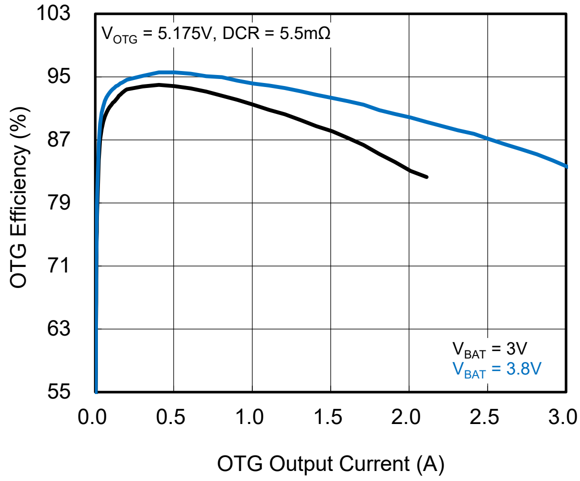
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{VBUS}/V_{BAT} Power-Up						
VBUS OVP Reaction Time	t_{ACOV}	V_{VBUS} rising above ACOV threshold to turn off Q2		0.1		μs
Wait Window for Bad Adapter Detection	t_{BAD_SRC}			30		ms
Battery Charger						
Deglitch Time for Charge Termination	t_{TERM_DGL}	ITERM_TIMER = 0		230		ms
Deglitch Time for Recharge	t_{RECHG_DGL}			230		ms
System Over-Current Deglitch Time to Turn off Q4	$t_{SYSOVLD\_DGL}$			120		μs
Battery Over-Voltage Deglitch Time to Disable Charge	t_{BATOVP}			1		μs
Charge Safety Timer Accuracy in Trickle Charge	t_{SAFETY_TRKCHG}		2.1	2.3	2.5	h
Charge Safety Timer Accuracy in Pre-Charge	t_{SAFETY_PRECHG}		2.1	2.3	2.5	h
Typical Charge Safety Timer Range	t_{SAFETY}	CHG_TIMER = 1	14.9	16.2	17.5	h
Typical Top-Off Timer Range	t_{TOP_OFF}	TOPOFF_TIMER[1:0] = 10	31.5	35	37.5	min
Battery Monitor						
Conversion Time	t_{CONV}	CONV_RATE = 0		8		ms
nQON Timing and Ship Mode Timing						
nQON Negative Pulse Low Pulse Width to Turn on BATFET and Exit Ship Mode	$t_{SHIPMODE}$	tSHIPMODE = 1	0.9	1	1.1	s
nQON Low Time to Reset BATFET	t_{QON_RST}		9	10	11	s
BATFET off Time during Full System Reset	t_{BATFET_RST}		295	320	345	ms
Wait Delay for Entering Ship Mode	t_{SM_DLY}	BATFET_DLY = 1	11.4	12.3	13.2	s
Digital Clock and Watchdog Timer						
Watchdog Reset Time	t_{WDT}	WATCHDOG[1:0] = 01, REGN LDO disabled	37.9	40.9	44	s
Digital Clock Frequency in Low Power	f_{LPDIG}	REGN LDO disabled		31.25		kHz
Digital Clock Frequency	f_{DIG}	REGN LDO enabled		500		kHz
I^2C Interface						
SCL Clock Frequency	f_{SCL}				1000	kHz

TYPICAL PERFORMANCE CHARACTERISTICS

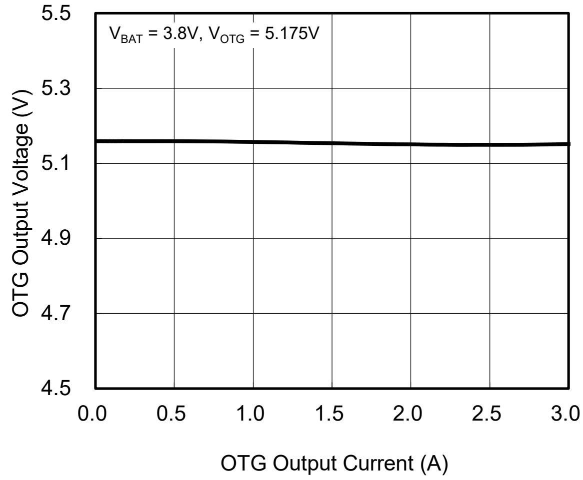
Charge Efficiency vs. Charge Current



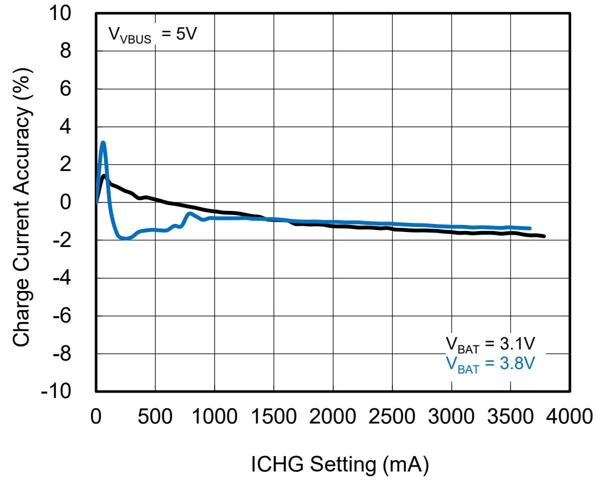
OTG Efficiency vs. OTG Output Current



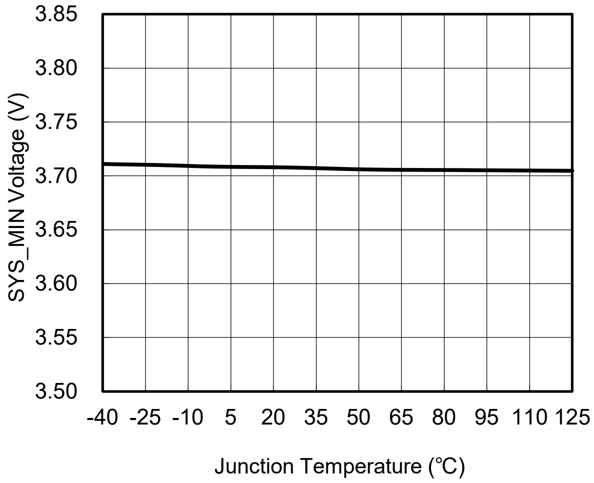
OTG Output Voltage vs. OTG Output Current



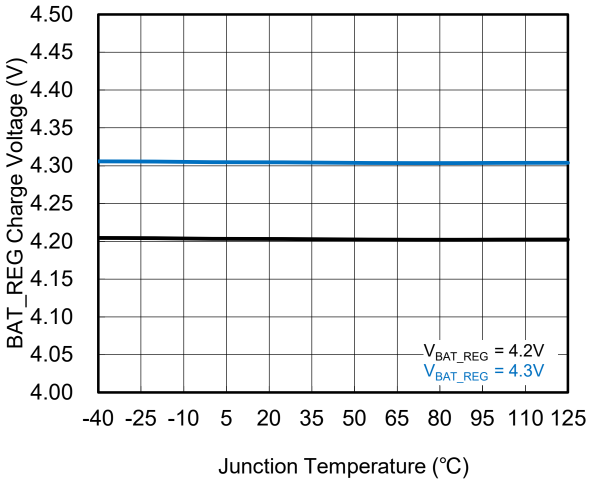
Charge Current Accuracy vs. ICHG Setting



SYS_MIN Voltage vs. Junction Temperature

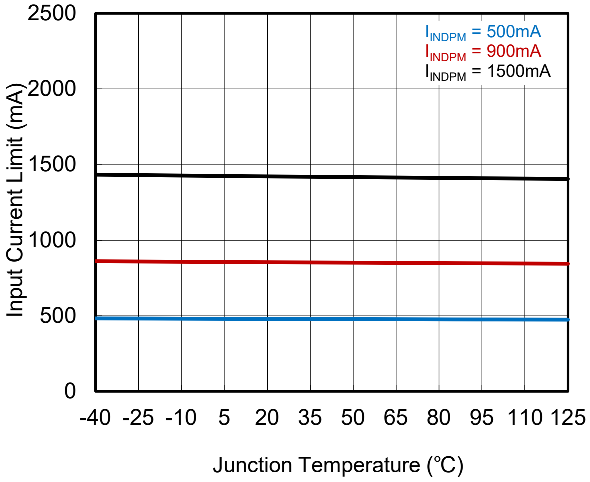


BAT_REG Charge Voltage vs. Junction Temperature

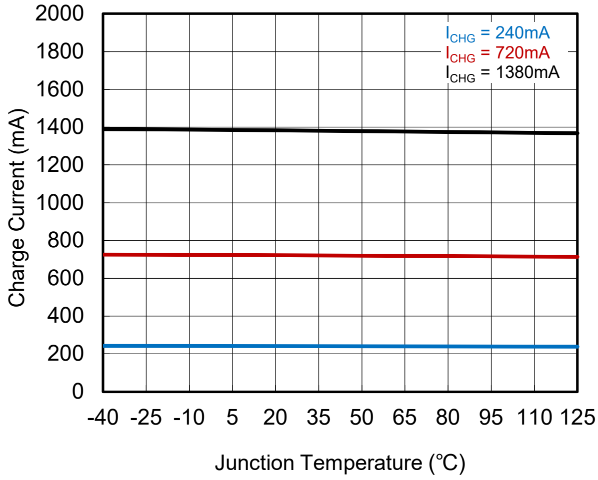


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

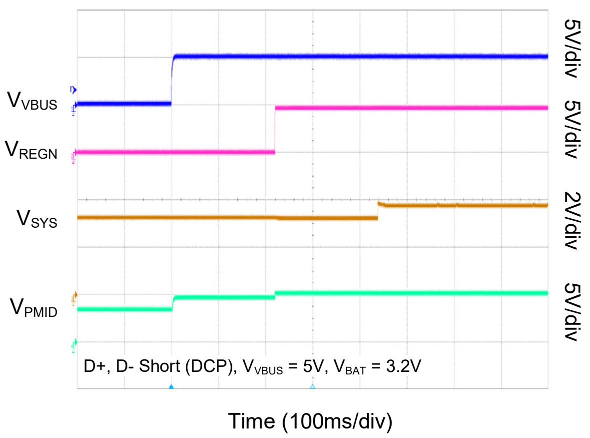
Input Current Limit vs. Junction Temperature



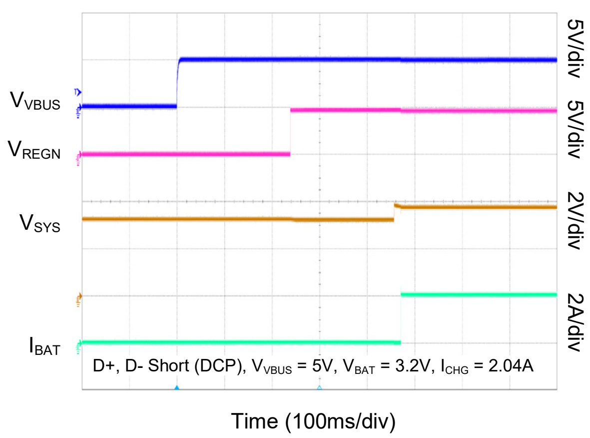
Charge Current vs. Junction Temperature



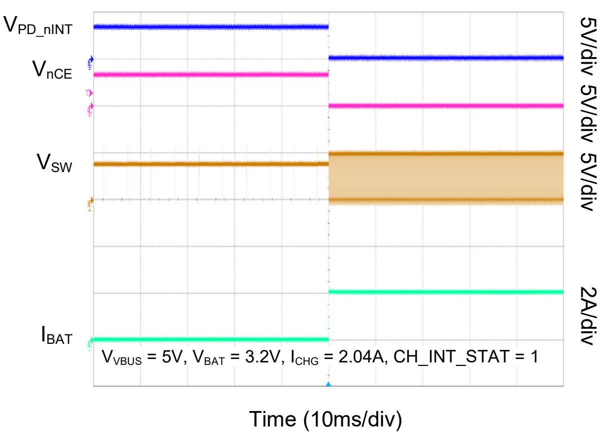
VBUS Power-Up with Charge Disabled



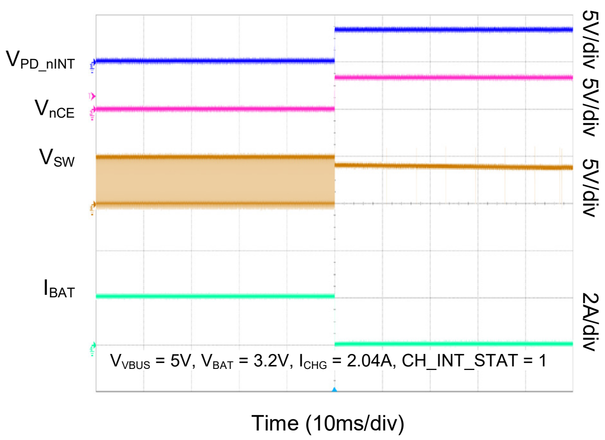
VBUS Power-Up with Charge Enabled



Charge Enabled by nCE Pin

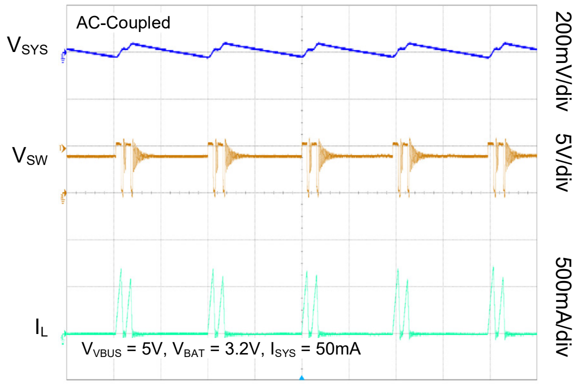


Charge Disabled by nCE Pin



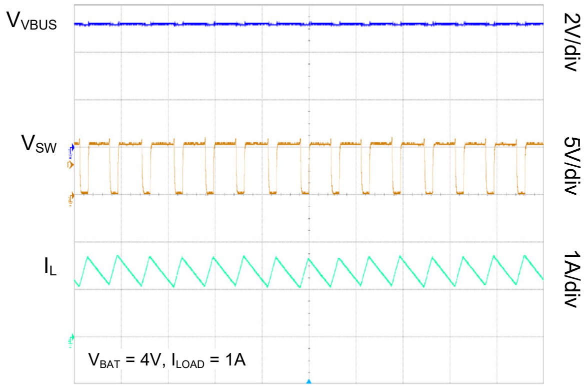
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

PSM Switching in Buck Mode, Charge Disabled



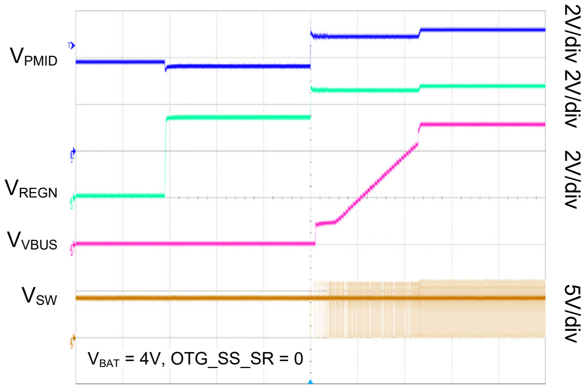
Time (5μs/div)

OTG Switching (Boost Mode)



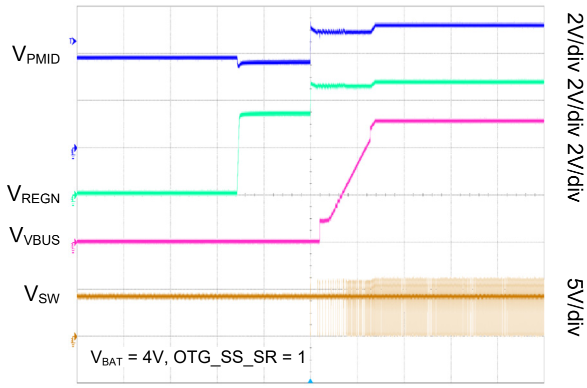
Time (1μs/div)

OTG Start-Up



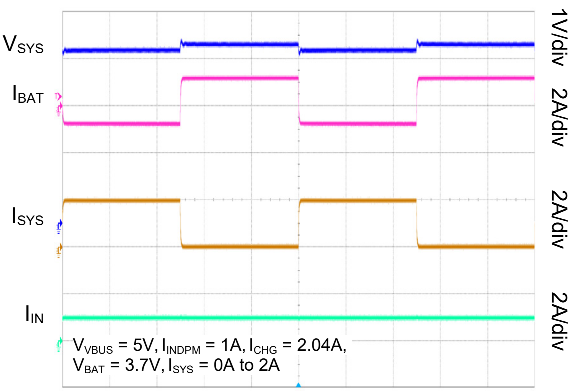
Time (10ms/div)

OTG Start-Up



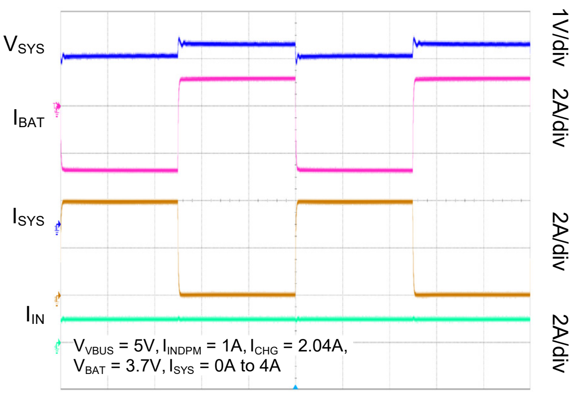
Time (5ms/div)

System Load Transient



Time (2ms/div)

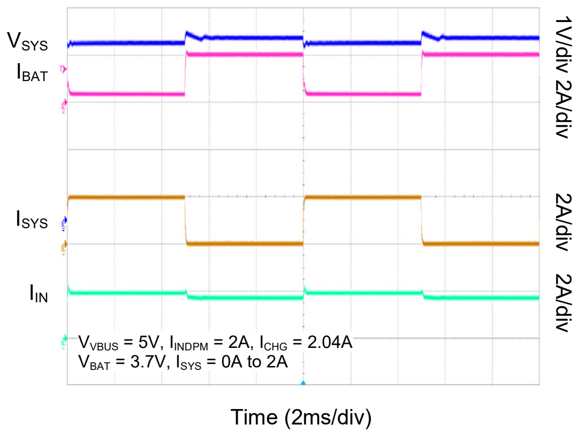
System Load Transient



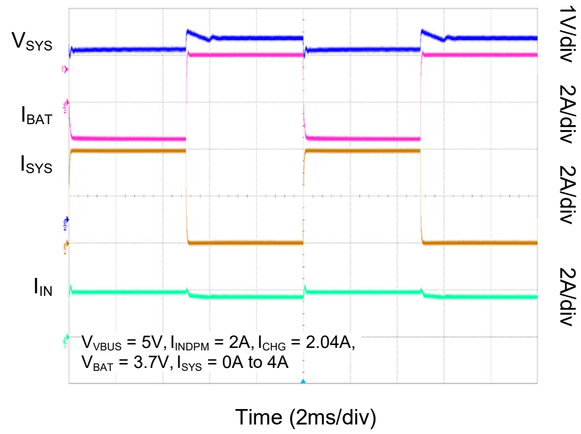
Time (2ms/div)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

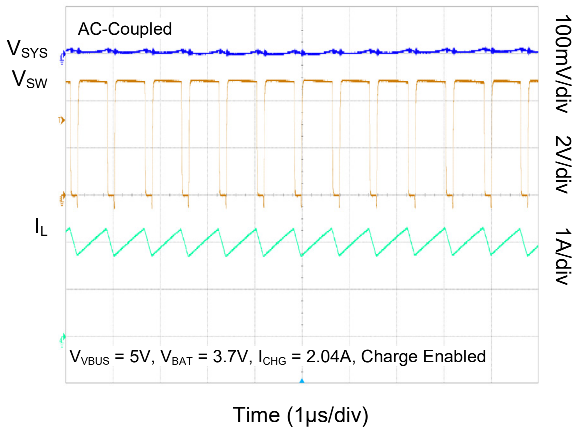
System Load Transient



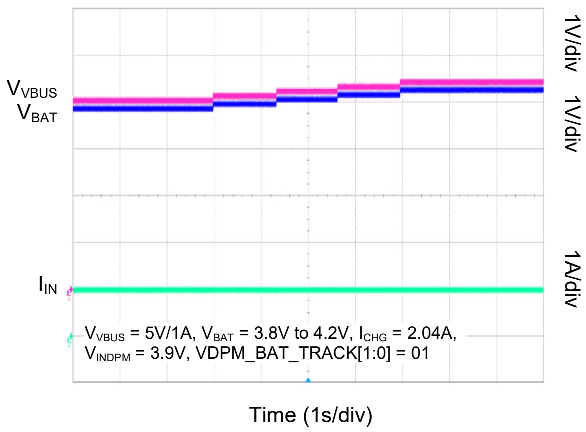
System Load Transient



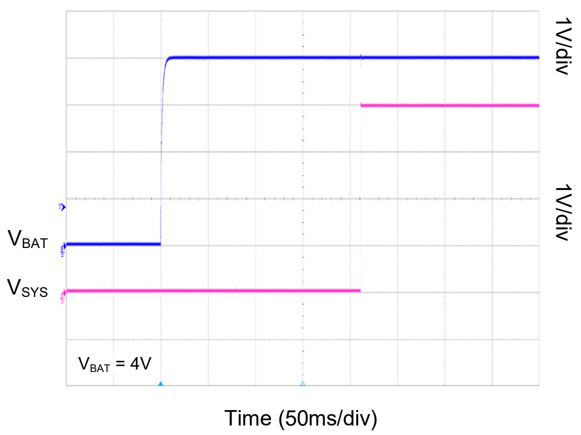
PWM Switching in Buck Mode



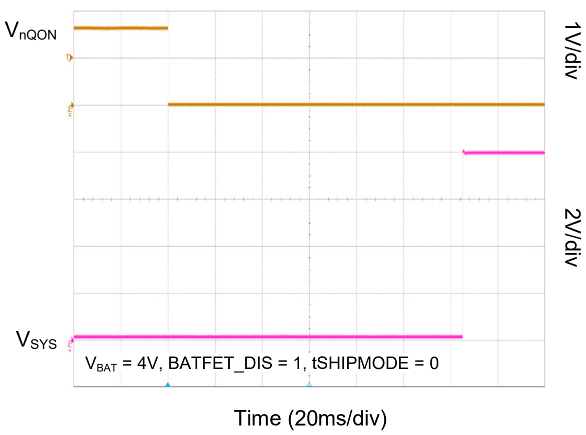
V_{INDPM} Tracking Battery Voltage



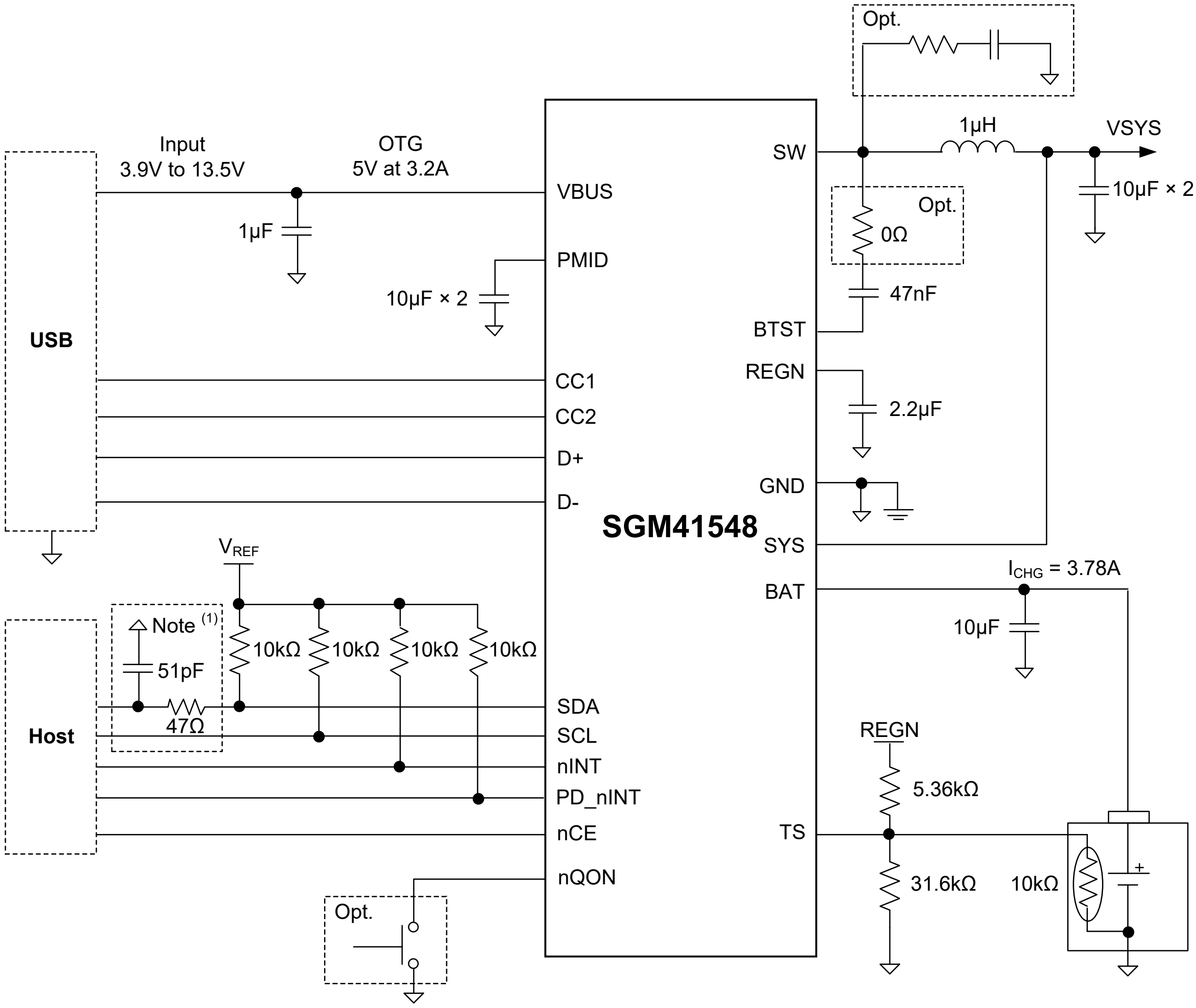
BAT Power-Up with VBUS Absent



Exit Ship Mode by nQON Pin



TYPICAL APPLICATION CIRCUIT



NOTE:

1. It is recommended to make provision in this section.

Figure 1. Typical Application Circuit

FUNCTIONAL BLOCK DIAGRAM

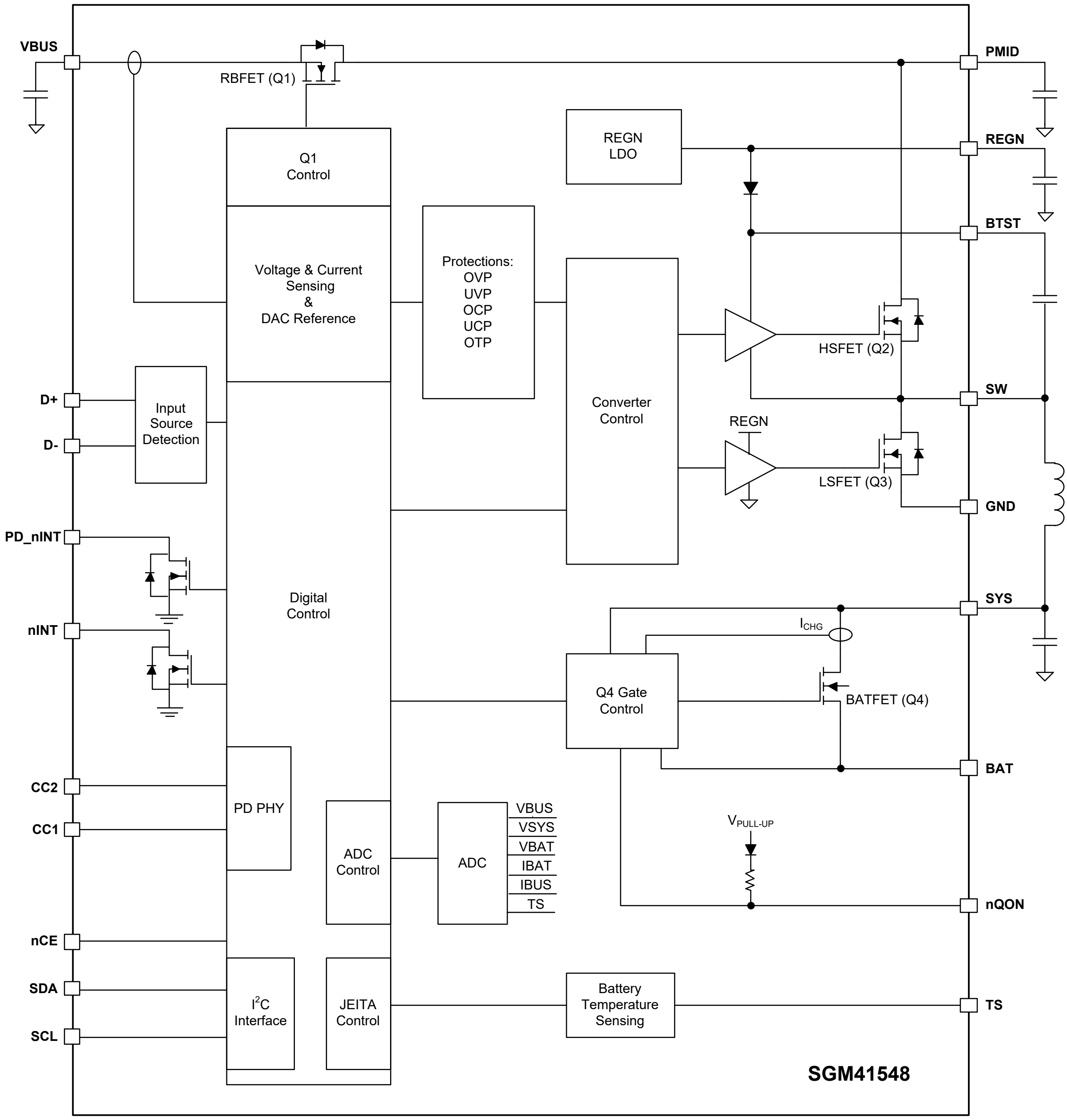


Figure 2. Block Diagram

DETAILED DESCRIPTION

The SGM41548 is a power management and charger device for applications such as cell phones and tablets that use high capacity single-cell Li-Ion or Li-polymer batteries. The SGM41548 can accommodate a wide range of input sources including USB, wall adapter and car chargers. It is optimized for 5V input (USB voltage) but is capable of operating with input voltages from 3.9V to 13.5V. It also supports JEITA profile for battery charging safety at high or low temperatures. Automatic power path selection to power the system (SYS) from the input source (VBUS), battery (BAT) or both is another feature of the device. Battery charge current is programmable and can reach a maximum of 3.78A (charge). In the Boost mode, the battery voltage is boosted to power the VBUS pin (3.2A MAX) when it is a power receiving node (USB OTG) that is typically regulated to 5.175V.

The device may operate in several different modes:

In HIZ mode, the reverse blocking FET (Q1), internal REGN LDO, converter switches and some other parts of the internal circuit remain off to save the battery while it supplies DC power to the system through BATFET.

In the sleep mode, the switching is stopped. The charger goes to the sleep mode when the input source voltage (V_{VBUS}) is not high enough for charging the battery. In other words, V_{VBUS} is smaller than V_{BAT} + V_{SLEEP} (where V_{SLEEP} is a small threshold) and Buck converter is not able to charge, even at its maximum duty cycle. The Boost may also go to the sleep mode if similar issue happens in the reverse direction (when V_{VBUS} is almost equal to or smaller than V_{BAT}).

In supplement mode, the input source power is not enough to supply system demanded power and the battery assists by discharging to the system in parallel and providing the deficit.

Power-On Reset (POR)

The internal circuit of the device is powered from the greater voltage between V_{VBUS} and V_{BAT}. When the voltage of the selected source goes above its UVLO level (V_{VBUS} > V_{VBUS_UVLOZ} or V_{BAT} > V_{BAT_UVLOZ}), a POR happens and activates the sleep comparator, battery depletion comparator and BATFET driver. Upon activation, the I^2C interface will also be ready for communication and all registers reset to their default values.

Power-Up from Battery Only (No Input Source)

When only the battery is presented as a source and its voltage is above depletion threshold ($V_{BAT\_DPL\_RISE}$), the BATFET turns on and connects the battery to the system. The quiescent current is minimum because the REGN LDO remains off. Conduction losses are also low due to small R_{DSON} of BATFET. Low losses help to extend the battery run time.

The discharge current through BATFET is continuously monitored. In the supplement mode, if a system overload (or short) occurs (I_{BAT} > I_{BATFET_OCP}), the BATFET is turned off immediately and BATFET_DIS bit is set to 0b1. The BATFET will not enable until the input source is applied or one of the BATFET Enable Mode (Exit Ship Mode) methods (explained later) is used to activate the BATFET.

Power-Up Process from the Input Power Source

Upon connection of an input source (VBUS), its voltage is checked to turn on the internal REGN LDO regulator and the bias circuits (whether the battery is present or not). The input current limit is determined and set before the Buck converter is started. The sequences of actions when VBUS as input source is powered up are:

1. REGN LDO power-up.
2. Poor power source detection (qualification).
3. Input power source type detection. (Based on D+/D- input. It is used to set the default input current limit (IINDPM[5:0]).)
4. Setting of the input voltage limit threshold (VINDPM threshold).
5. DC/DC converter power-up.

Details of the power-up steps are explained in the following sections.

DETAILED DESCRIPTION (continued)

REGN LDO Power-Up

The REGN low dropout regulator powers the internal bias circuits, HSFET and LSFET gate drivers and TS rail (thermistor pin). The REGN enables when the following two conditions are satisfied and remain valid for a 220ms delay time, otherwise the device stays in high impedance mode (HIZ) with REGN LDO off.

1. $V_{VBUS} > V_{VBUS\_PRESENT}$.
2. $V_{VBUS} > V_{BAT} + V_{SLEEPZ}$ (in Buck mode) or $V_{VBUS} < V_{BAT} + V_{SLEEP}$ (in Boost mode).

In HIZ state, the quiescent current drawn from VBUS is very small (less than I_{VBUS_HIZ}). System is powered only by the battery in HIZ mode.

Poor Power Source Detection (Qualification)

When REGN LDO is powered, the input source (adapter) is checked for its type and current capacity. To start the Buck converter, the input (VBUS) must meet the following conditions:

1. $V_{VBUS} < V_{VBUS\_OV}$.
2. $V_{VBUS} > V_{VBUSMIN\_RISE}$ during t_{BAD_SRC} test period (30ms TYP) in which the I_{BAD_SRC} (25mA TYP, can be disabled by VBUS_SINK_DIS bit) current is pulled from VBUS.

If the test is failed, the conditions are repeatedly checked every two seconds. As soon as the input source passes qualification, the VBUS_GD bit in status register is set to 0b1 and a pulse is sent to the nINT pin to inform the host. Type detection will start as next step.

Input Power Source Type Detection

The input source detection will run through the D+/D- lines while REGN LDO is powered and after the VBUS_GD bit is set. The SGM41548 can detect the input source types, which include CDP/SDP/DCP and non-standard adapter through the D+/D- pins following USB BC1.2 specification. A pulse is sent to nINT pin to inform the host when the input source type detection is completed. Some registers and pins are also updated as detailed below:

1. Input current limit register (the value in the IINDPM[5:0]) is changed to set current limit.
2. PG_STAT (power good) bit is set.
3. VBUS_STAT[2:0] register is updated to indicate USB or adapter input source types.

The input current is always limited by the IINDPM[5:0] register and the limit can be updated by the host if needed.

Input Current Limit by D+/D- Detection

The SGM41548 integrates a D+/D- based input source detection to set the input current limit when VBUS is plugged in. When the input source is plugged in, the starts USB BC1.2 detection and sets the CDP/SDP/DCP related input current limit. And if the data contact detection timer expires, the non-standard adapter detection starts and then sets the input current limit. Please refer to Table 1 and Table 2.

Table 1. Non-Standard Adapter Detection

Non-Standard Adapter	D+ Threshold	D- Threshold	Input Current Limit (A)
Divider 1	V_{D+} within V_{2P7}	V_{D-} within V_{2P0}	2.1
Divider 2	V_{D+} within V_{1P2}	V_{D-} within V_{1P2}	2
Divider 3	V_{D+} within V_{2P0}	V_{D-} within V_{2P7}	1
Divider 4	V_{D+} within V_{2P7}	V_{D-} within V_{2P7}	2.4

Table 2. Input Current Limit Setting from D+/D- Detection

D+/D- Detection	Input Current Limit (I_{INDPM})	VBUS_STAT[2:0]
USB SDP (USB500)	500mA	001
USB CDP	1.5A	010
USB DCP	2.4A	011
Divider 1	2.1A	110
Divider 2	2A	110
Divider 3	1A	110
Divider 4	2.4A	110
Unknown 5V Adapter	500mA	101

DETAILED DESCRIPTION (continued)

Force Detection of Input Current Limit

The host can set EN_IINDET bit to 0b1 in host mode to force the device to run. And the EN_IINDET bit returns to 0b0 by itself and input result is updated after the detection is completed.

D+/D- Output Voltage Setting

The host can be set D+/D- output voltages by DP_VSET[1:0] and DM_VSET[1:0] to HIZ, 0V, 0.6V or 3.3V. When BC1.2 detection runs, these bits are ignored.

Setting of the Input Voltage Limit Threshold (VINDPM Threshold)

A wide voltage range (3.9V to 5.4V, 5.9V to 9V, 10.5V to 12V) is supported for the input voltage limit setting in VINDPM[3:0] and VINDPM_OS[1:0]. 4.5V is the default for USB.

The device supports dynamic tracking of the battery voltage (VINDPM). VDPM_BAT_TRACK[1:0] bits can be used to enable tracking (0b00 to disable tracking) and set the tracking offset value. When the tracking is enabled, the input voltage limit will be set to the larger value between the VINDPM[3:0] and V_{BAT} + VDPM_BAT_TRACK[1:0]. The VDPM_BAT_TRACK[1:0] tracking offset can be set to 200mV, 250mV or 300mV. And this function only takes effect when VINDPM_OS[1:0] = 00.

DC/DC Converter Power-Up

The 1.5MHz switching converter composed of LSFET and HSFET is enabled, which can start switching when the input current limit is set. Converter is initiated with a soft-start when the system voltage is ramped up. If SYS voltage is less than 2.2V, the input current is limited to 200mA or IINDPM[5:0] or the peak of inductor current, depending on whichever is smaller, otherwise the limit is set to IINDPM[5:0].

The BATFET remains on to charge the battery if the battery charging function is enabled, otherwise BATFET turns off.

When the converter operates for battery charging, it acts as an efficient, fixed frequency synchronous Buck converter regardless of the input/output voltages and currents. However, it is capable of switching to pulse skip mode (PSM) at light load when charging is disabled or when the detected battery voltage is less than minimum system voltage setting. PSM operation can be enabled or prevented in Buck mode through using the PSM_FWD_DIS bit.

Boost Mode

The SGM41548 supports USB On-The-Go. When a load device is connected to the USB port, the converter can operate as a step-up synchronous converter (Boost mode) with 1.5MHz switching frequency to supply power from the battery to that load. The USB OTG output current limit requirement is achieved by programming. However, the Boost converter can deliver 3.2A to the output (maximum limit). Converter will be set to Boost mode if at least 30ms or 8ms (setting by OTG_SS_SR bit) is passed from enabling this mode (OTG_CONFIG = 1) and the following conditions are satisfied:

1. $V_{BAT} > V_{BATLOW\_OTG}$.
2. $V_{VBUS} < V_{BAT} + V_{SLEEP}$ (in sleep mode) and $V_{VBUS} < V_{VBUS\_PRESENT}$.
3. Acceptable voltage range at TS pin ($V_{BHOT} < V_{TS} < V_{BCOLD}$).

The output voltage is set to V_{VBUS} = 5.175V and is maintained as long as V_{BAT} is above V_{BATLOW_OTG}. The output current can reach up to the programmed value by BOOST_LIM[2:0] register bits (0.5A - 3.2A). The VBUS_STAT[2:0] status register bits are set to 0b111 in Boost mode (OTG).

Host Mode and Default Mode Operation with Watchdog Timer

After a power-on reset, the device starts in default mode (standalone) with all registers reset as default. If the watchdog timer expires, the device will also enter the default mode with WATCHDOG_FAULT bit set to 0b1. When the host is in sleep mode or there is no host, the device stays in the default mode in which the SGM41548 operates like an autonomous charger. The battery is charged for 16.2 hours (default value for the fast charging safety timer). Then the charge stops while Buck converter continues to operate to power the system load.

Most of the flexibility features of the SGM41548 become available in the host mode when the device is controlled by a host with I^2C. By setting the WD_RST bit to 0b1, the charger mode changes from default mode to host mode. In this mode, the WATCHDOG_FAULT bit is 0b0 and all device parameters can be programmed by the host. To prevent the device watchdog from reset that results in going back to default mode, the host must disable the watchdog timer by setting WATCHDOG[1:0] = 00, or it must consistently reset the watchdog timer before expiry by writing 0b1 to WD_RST bit to prevent WATCHDOG_FAULT bit from being set. Every time 0b1 is written to the WD_RST bit, the watchdog timer will restart counting. Therefore, it should be reset again before overflow (expiry) to keep the device in the host mode. If the watchdog timer expires (WATCHDOG_FAULT = 1), the device returns to default mode and some registers are reset to their default values as shown in the RESET BY column of the register tables in Register Maps for Charger section.

DETAILED DESCRIPTION (continued)

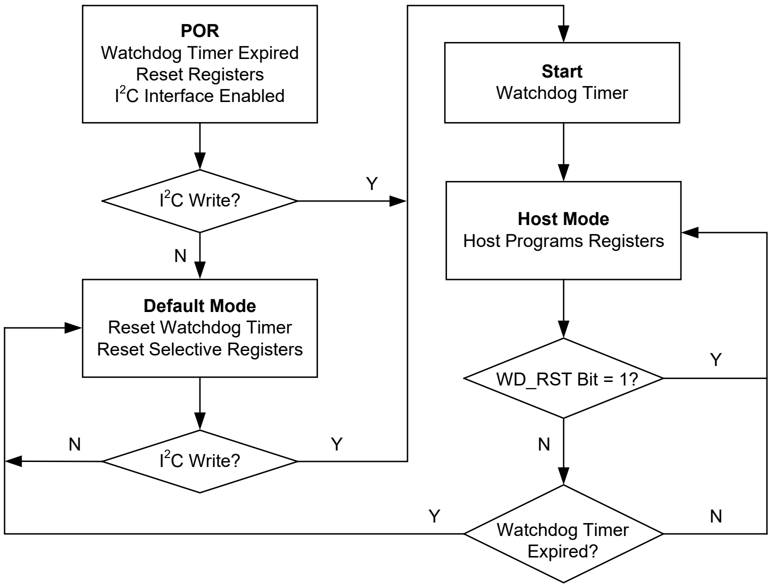


Figure 3. Watchdog Timer Flow Chart

Battery Charging Management

The SGM41548 is designed for charging single-cell Li-Ion or Li-poly batteries with a charge current up to 3.78A (MAX). The battery connection switch (BATFET) is in the charge or discharge current path and features low on-resistance (26mΩ TYP) to allow high efficiency and low voltage drop.

Charging Cycle in Autonomous Mode

Charging is enabled if CHG_CONFIG = 1 and nCE pin is pulled low. In default mode, the SGM41548 runs a charge cycle with the default parameters itemized in Table 3. At any moment, the device can be controlled for charging through the host mode.

Table 3. Charging Parameter Default Setting

Default Mode	SGM41548
Charging Voltage (V_{BAT_REG})	4.200V
Charging Current (I_{CHG})	2.04A
Pre-Charge Current (I_{PRECHG})	180mA
Termination Current (I_{TERM})	180mA
Temperature Profile	JEITA
Safety Timer	16.2h

Start a New Charging Cycle

If the converter can start switching and all the following conditions are satisfied, a new charge cycle starts:

- NTC temperature fault is not asserted (TS pin).
- Safety timer fault is not asserted.
- BATFET is not forced off. (BATFET_DIS = 0).
- Charging is enabled (3 conditions: CHG_CONFIG = 1, ICHG[5:0] register is not 0mA and nCE pin is low).
- Battery voltage is below the programmed full charge level (V_{BAT_REG}).

A new charge cycle starts automatically if battery voltage falls below the recharge threshold level (V_{BAT_REG} - 100mV, V_{BAT_REG} - 200mV, V_{BAT_REG} - 300mV or V_{BAT_REG} - 400mV configured by VRECHG[1:0] bits). Also, if the charge cycle is completed, a new charging cycle can be initiated by toggling the nCE pin or CHG_CONFIG bit.

Normally, a charge cycle terminates when the charge voltage is above the recharge threshold level and the charging current falls below the termination threshold if the device is not in thermal regulation or dynamic power management (DPM) mode.

DETAILED DESCRIPTION (continued)

Battery Charging Profile

The SGM41548 features a full battery charging profile with five phases. In the beginning of the cycle, the battery voltage (V_{BAT}) is tested, and appropriate current and voltage regulation levels are selected as shown in Table 4. Depending on the detected status of the battery, the proper phase is selected to start or continue the charging cycle. The phases are trickle charge (V_{BAT} < 2.2V), pre-charge, fast charge (constant current and constant voltage) and optional top-off charge.

Table 4. Charging Current Setting Based on V_{BAT}

V_{BAT} Voltage	Selected Charging Current	Default Value in the Register	CHRG_STAT[1:0]
< 2.2V	I_{SHORT}	60mA	01
2.2V to 3.17V	I_{PRECHG}	180mA	01
> 3.17V	I_{CHG}	2.04A	10

Note that in the DPM or thermal regulation mode, normal charging functions are temporarily modified: the charge current will be less than the value in the register. The termination is disabled, and the charging safety timer is slowed down by counting at half clock rate.

Charge Termination

A charge cycle is terminated when the battery voltage is higher than the recharge threshold and the charge current falls below the programmed termination current. Unless there is a high power demand for system and it needs to operate in supplement mode, the BATFET turns off at the end of the charge cycle. Even after termination, the Buck converter operates continuously to supply the system.

The CHRG_STAT[1:0] bits are set to 0b11 and a negative pulse is sent to nINT pin after termination.

If the charger is regulating input current, input voltage or junction temperature instead of charge current, termination will be temporarily prevented. The EN_TERM bit is termination control bit and can be set to 0b0 to disable termination before it happens.

At low termination currents (60mA TYP), the offset in the internal comparator may give rise to a higher (+10mA to +20mA) actual termination current. A delay in termination can be added (optional) as a compensation for comparator offset using a programmable top-off timer. During the delay, constant voltage charge phase continues and gives the falling charge current a chance to drop closer to the programmed value. The top-off delay timer has the same restrictions as the safety timer. As an example, under some conditions, if the safety timer is suspended, the top-off timer will also be suspended or if the safety timer is slowed down, the termination timer will also be slowed down. The TOPOFF_ACTIVE bit reports the active/inactive status of the top-off timer. The CHRG_STAT[1:0] and TOPOFF_ACTIVE bits can be read to find status of the termination.

Any of the following events resets the top-off timer:

1. Disable to enable transition of nCE (charge enable).
2. A low to high change in the status of termination.
3. Set REG_RST bit to 0b1.

The setting of the top-off timer is applied at the time of termination detection and unless a new charge cycle is started, modifying the top-off timer parameters after termination has no effect. A negative pulse is sent to nINT when top-off timer is started or ended.

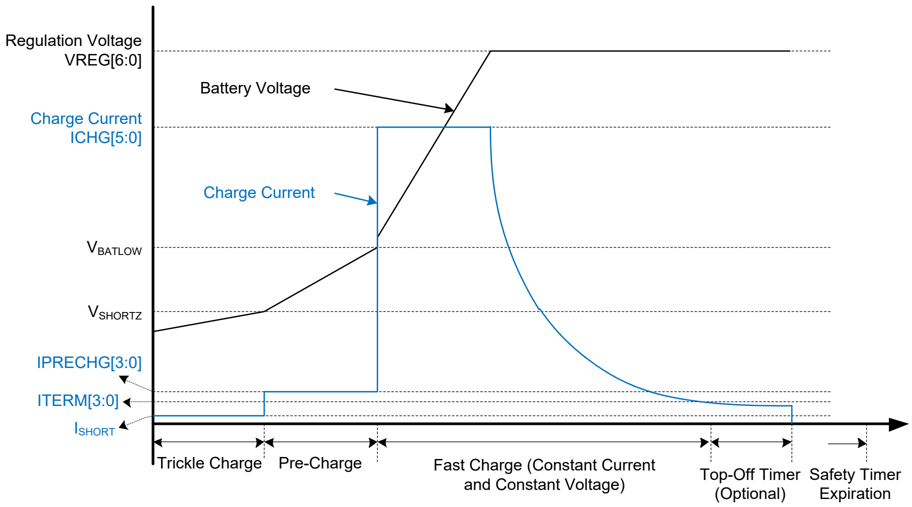


Figure 4. Battery Charging Profile

DETAILED DESCRIPTION (continued)

Temperature Qualification

The charging current and voltage of the battery must be limited when battery is cold or hot. A thermistor input for battery temperature monitoring is included in the device that can protect the battery based on JEITA guidelines.

Compliance with JEITA Guideline

JEITA guideline (April 20, 2007 release) is implemented in the device for safe charging of the Li-Ion battery. JEITA highlights the considerations and limits that should be considered for charging at cold or hot battery temperatures. High charge current and voltage must be avoided outside the normal operating temperatures (typically 0℃ and 60℃). This functionality can be disabled if not needed. Four temperature levels are defined by JEITA from T1 (minimum) to T4 (maximum). Outside this range, charging should be stopped. The corresponding voltages sensed by NTC are named V_{T1} to V_{T4}. Due to the sensor negative resistance, a higher temperature results in a lower voltage on TS pin. The battery cool range is between T1 and T2, and the warm range is between T3 and T4. Charge must be limited in the cool and warm ranges.

One of the conditions for starting a charge cycle is having the TS voltage within V_{T1} to V_{T4} window limits. If during the charge, battery gets too cold or too hot and TS voltage exceeds the T1 - T4 limits, charging is suspended (zero charge current) and the controller waits for the battery temperature to come back within the T1 to T4 window.

JEITA recommends reducing charge current to 1/2 of fast charging current or lower at cool temperatures (T1 - T2). For warmer temperature (within T3 - T4 range), charge voltage is recommended to be kept below 4.1V.

The SGM41548 exceeds the JEITA requirement by their flexible charge parameter settings. At warm temperature range (T3 - T4), the charge voltage is set to the lower of V_{BAT_REG} and 4.1V when JEITA_VSET_H = 0, the charge voltage is set to V_{BAT_REG} when JEITA_VSET_H = 1, and the charge current can be reduced down to 0%, 20% or 50% of fast charging current by the JEITA_ISET_H[1:0] bits. At cool temperatures (T1 - T2), the current setting can be reduced down to 50% or 20% of fast charging current selected by the JEITA_ISET_L bit when EN_JEITA_ISET_L = 1, and the charge voltage is set to V_{BAT_REG} when JEITA_VSET_L = 0, the charge voltage is set to the lower of V_{BAT_REG} and 4.1V when JEITA_VSET_L = 1. Additional, the cool threshold T2 and warm threshold T3 can be changed through JEITA_VT2[1:0] and JEITA_VT3[1:0], and the charge current can be disabled by setting EN_JEITA_ISET_L = 0.

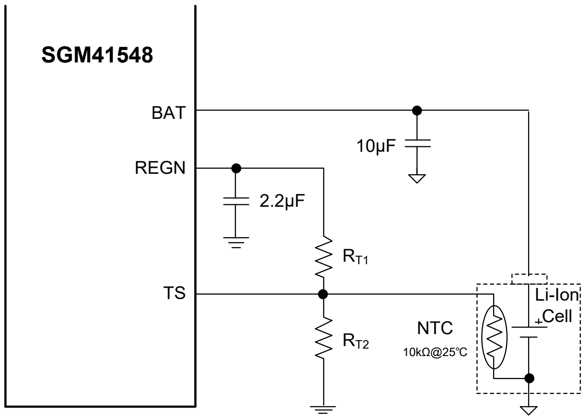


Figure 5. Battery Thermistor Connection and Bias Network

A 103AT-2 type thermistor is recommended to use for the SGM41548. Other thermistors may be used and bias network (see Figure 5) can be calculated based on the following equations:

$$R_{T2} = \frac{R_{THCOLD} \times R_{THHOT} \times \left(\frac{1}{V_{T1}} - \frac{1}{V_{T4}}\right)}{R_{THHOT} \times \left(\frac{1}{V_{T4}} - 1\right) - R_{THCOLD} \times \left(\frac{1}{V_{T1}} - 1\right)} \quad (1)$$

$$R_{T1} = \frac{\left(\frac{1}{V_{T1}} - 1\right)}{\left(\frac{1}{R_{T2}}\right) + \left(\frac{1}{R_{THCOLD}}\right)} \quad (2)$$

Where, V_{T1} and V_{T4} are T_{COLD} and T_{HOT} threshold voltages on TS pin as percentage to V_{REGN}, R_{THCOLD} and R_{THHOT} are thermistor resistances (R_{TH}) at desired T1 (Cold) and T4 (Hot) temperatures. Select T_{COLD} = 0℃ and T_{HOT} = 60℃ for Li-Ion or Li-polymer batteries. For a 103AT-2 type thermistor R_{THCOLD} = 27.28kΩ and R_{THHOT} = 3.02kΩ, the calculation results are: R_{T1} = 5.32kΩ and R_{T2} = 31.3kΩ. The standard value of R_{T1} is 5.36kΩ and that of R_{T2} is 31.6kΩ.

DETAILED DESCRIPTION (continued)

Boost Mode Temperature Monitoring (Battery Discharge)

The device is capable of monitoring the battery temperature for safety during the Boost mode. The temperature must remain within the V_{BCOLD} to V_{BHOT} thresholds, otherwise the Boost mode will be suspended and VBUS_STAT[2:0] bits are set to 0b000. Moreover, NTC_FAULT[2:0] register is updated to report Boost mode cold or hot condition. Once the temperature returns within the window, the Boost mode is resumed and NTC_FAULT[2:0] register is cleared to 0b000 (normal).

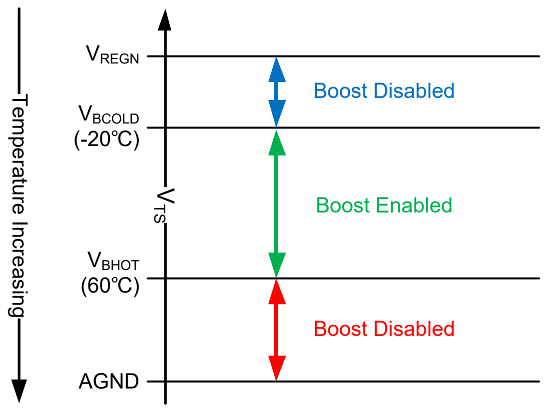


Figure 6. TS Pin Thermistor Temperature Window Settings in Boost Mode

Safety Timer

Abnormal battery conditions may result in prolonged charge cycles. An internal safety timer is considered to stop charging in such conditions. If the safety time is expired, CHRG_FAULT[1:0] bits are set to 0b11 and a negative pulse is sent to nINT pin. By default, the charge time limit. And it is 2 hours if the battery voltage does not rise above V_{BATLOW} threshold. And it is 16.2 hours if it goes above V_{BATLOW}. This feature is optional and can be disabled by clearing EN_TIMER bit. The 16.2 hours limit can also be reduced to 7 hours by clearing CHG_TIMER bit.

The safety timer counts at half clock rate when charger is running under input voltage regulation, input current regulation, JEITA cool or thermal regulation. Because in these conditions, the actual charge current is likely to be less than the register setting. As an example, if the safety timer is set to 7 hours and the charger is regulating the input current (IINDPM_STAT = 1) in the whole charging cycle, the actual safety time will be 14 hours. Clearing the EN_TMR2X bit will disable the half clock rate feature.

The safety timer is paused if a fault occurs or charger is in supplement mode, charging is suspended. It will resume once the fault condition is removed. If charging cycle is stopped by a restart or by toggling nCE pin or CHG_CONFIG bit, the timer resets and restarts a new timing.

Narrow Voltage DC (NVDC) Design in SGM41548

The SGM41548 features an NVDC design using the BATFET that connects the system to the battery. By using the linear region of the BATFET, the charger regulates the system bus voltage (SYS pin) above the minimum setting using Buck converter even if the battery voltage is very low. MOSFET linear mode allows for the large voltage difference between SYS and BAT pins to appear as V_{DS} across the switch while conducting and charging battery. The SYS_MIN[2:0] register sets the minimum system voltage (default 3.5V). If the system is in minimum system voltage regulation, the VSYS_STAT bit is set.

The BATFET operates in linear region when the battery voltage is lower than the minimum system voltage. The system voltage is regulated to 200mV (TYP) above the minimum system voltage setting. The battery gradually gets charged and its voltage rises above the minimum system voltage and lets BATFET change from linear mode to fully turned-on switch such that the voltage difference between the system and battery is the small V_{DS} of fully on BATFET.

The system voltage is always regulated to 50mV (TYP) above the battery voltage if:

1. The charging is terminated.
2. Charging is disabled and the battery voltage is above the minimum system voltage setting.

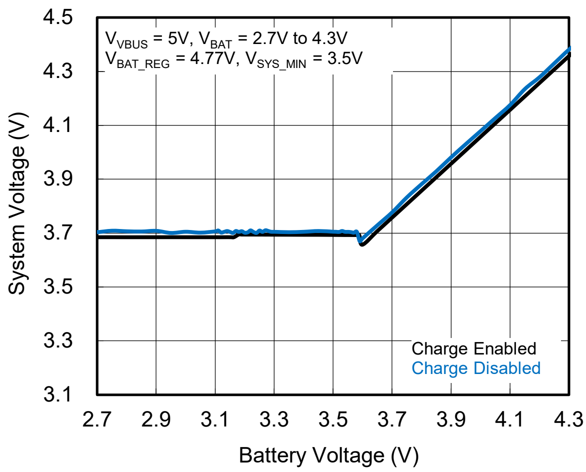


Figure 7. System Voltage vs. Battery Voltage

DETAILED DESCRIPTION (continued)

SGM41548 Dynamic Power Management (DPM)

The SGM41548 features a dynamic power management (DPM). To implement DPM, the device always monitors the input current and voltage to regulate power demand from the source and avoid input adapter overloading or to meet the maximum current limits specified in the USB specs. Overloading an input source may result in either current trying to exceed the input current limit (I_{INDPM}) or the voltage tending to fall below the input voltage limit (V_{INDPM}). With DPM, the device keeps the VSYS regulating to its minimum setting by reducing the battery charge current adequately such that the input parameter (voltage or current) does not exceed the limit. In other words, charge current is reduced to satisfy $I_{IN} \leq I_{INDPM}$ or $V_{IN} \geq V_{INDPM}$ whichever occurs first. DPM can be either an I_{IN} type (IINDPM) or V_{IN} type (VINDPM) depending on which limit is reached.

Changing to the supplement mode may be required if the charge current is decreased and reached to zero, but the input is still overloaded. In this case, the charger reduces the system voltage below the battery voltage to allow operation in the supplement mode and provide a portion of system power demand from the battery through the BATFET.

The IINDPM_STAT or VINDPM_STAT status bits are set during an IINDPM or VINDPM respectively. Figure 8 summarizes the DPM behavior (IINDPM type) for a design example with a 9V/1.2A adapter, 3.2V battery, 2.8A charge current setting and 3.4V minimum system voltage setting.

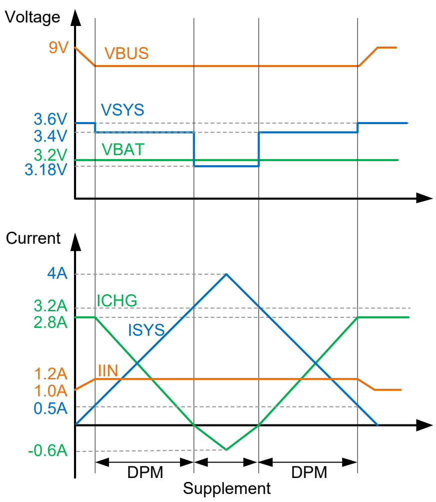


Figure 8. DPM Behavior Plot

Battery Supplement Mode

If the system voltage drops 45mV below the battery voltage, the BATFET gradually starts to turn on. The threshold margin is 180mV only if not in charge mode, not in DPM and V_{SYS_MIN} setting is less than V_{BAT}. At low discharge currents, the BATFET gate voltage is regulated (R_{DS} modulation) such that the BATFET V_{DS} stays at 30mV. At higher currents, the BATFET will turn fully on (reaching its lowest R_{DSON}). From this point, increasing the discharge current will linearly increase the BATFET V_{DS} (determined by $R_{DSON} \times I_D$). Using the MOSFET linear mode at lower currents prevents swinging oscillation from entering and exiting the supplement mode.

BATFET gate regulation V-I characteristics is shown in Figure 9. If the battery voltage falls below its minimum depletion, the BATFET turns off and exits supplement mode.

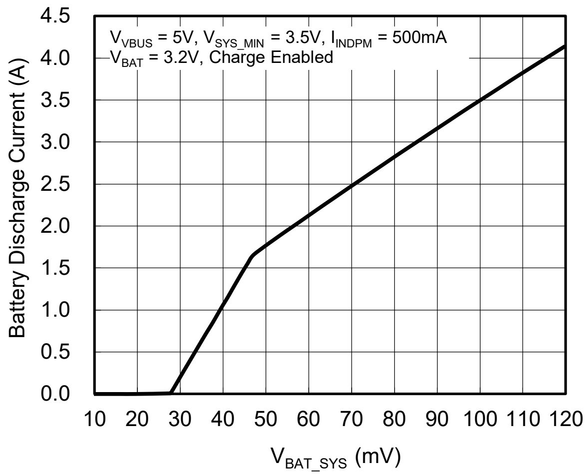


Figure 9. BATFET Gate Regulation V-I Curve

Battery Monitor

The SGM41548 has a battery monitor that can provide measurements of input voltage, battery voltage, system voltage, thermistor ratio, charging current and input current, based on the device modes of operation and REG0x19 register. The measurements are presented in Battery Monitor Registers (REG0x13 - REG0x18). The battery monitor has two conversion modes, which are determined by using CONV_RATE bit: one-shot conversion (default) and 1 second continuous conversion.

For the one-shot conversion (CONV_RATE = 0), the conversion will start when the CONV_START bit is set and which conversion is active depends on REG0x19. During the conversion process, the CONV_START bit is set and it is cleared by the device after the conversion is completed. The conversion result is provided after t_{CONV} (8ms TYP).

For the continuous conversion (CONV_RATE = 1), the conversion will start when the CONV_RATE bit is set and all conversions are active. During active conversion process, setting the CONV_START bit indicates that the conversion is in progress. The conversion result is provided every 1 second automatically. The battery monitor ends continuous conversion mode when the CONV_RATE bit is cleared.

When the battery monitor is active, the REGN power is enabled and it can increase the quiescent current.

DETAILED DESCRIPTION (continued)

Table 5. Battery Monitor Modes of Operation

Parameter	Enable Bit	ADC Register	Modes of Operation			
			Charge Mode	Boost Mode	Disable Charge Mode	Battery Only Mode
Battery Voltage (V_{BAT})	REG0x19[4]	REG0x13	Yes	Yes	Yes	Yes
System Voltage (V_{SYS})	REG0x19[3]	REG0x14	Yes	Yes	Yes	Yes
TS Voltage Percentage (TS)	REG0x19[2]	REG0x15	Yes	Yes	Yes	Yes
VBUS Voltage (V_{VBUS})	REG0x19[5]	REG0x16	Yes	Yes	Yes	N/A
Charge Current (I_{BAT})	REG0x19[6]	REG0x17	Yes	N/A	N/A	N/A
Input Current (I_{VBUS})	REG0x19[7]	REG0x18	Yes	N/A	Yes	N/A

BATFET Control for System Power Reset and Ship Mode

Ship Mode (BATFET Disable)

Ship mode is usually used when the system is stored or in idle state for a long time or is in shipping. In such conditions, it is better to completely disconnect battery and make system voltage zero to minimize the leakage and extend the battery life. To enter ship mode, the BATFET has to be forced off by setting BATFET_DIS bit. The BATFET turns off immediately if the BATFET_DLY bit is 0b0, or turns off after a t_{SM_DLY} delay (12.3s TYP) if the BATFET_DLY bit is set.

Exit Ship Mode (BATFET Enable)

To exit the ship mode and enable the BATFET, one of the following can be applied:

With the chip no powered by VBUS:
1. Connect the adapter to the input with a valid voltage to the VBUS input.
2. Pull nQON pin from logic high to low to enable BATFET, for example, by shorting nQON to GND. The negative pulse width should be at least a $t_{SHIPMODE}$ (1s TYP) for deglitching.

With the chip already powered by VBUS:
3. Clear BATFET_DIS bit by using host and I^2C.
4. Set REG_RST bit to 0b1 to reset all registers.
5. Apply a negative pulse to nQON pin (same as 2).

Full System Reset with BATFET Using nQON

When the input source is not present, the BATFET can act as a load on/off switch between the system and battery. This feature can be used to apply a power-on reset to the system. Host can toggle BATFET_DIS bit to cycle power off/on and reset the system. A push-button connected to nQON pin or a negative pulse can also be used to manually force a system power cycle when BATFET is ON (BATFET_DIS = 0). For this function, a negative logic pulse with a minimum width of t_{QON_RST} (10s TYP) must be applied to the nQON pin that results in a temporary BATFET turn-off for t_{BATFET_RST} (320ms TYP) that automatically turns on afterward. Setting EN_BATFET_RST bit to 0b0 can disable the function.

Full system reset function, either with or without adapter present. If BATFET_RST_WVBUS = 1, the system reset function starts after t_{QON_RST} when the nQON pin is pulled low. Once the reset process starts, the device first turns off the converter and then turns off the BATFET for t_{BATFET_RST}. If BATFET_RST_WVBUS = 0, the system reset function does not start until t_{QON_RST} after the nQON pin is pulled low and the adapter is removed.

In summary, the nQON pin controls BATFET and system reset in two different ways:

1. Enable BATFET: Applying an nQON logic high to low transition with longer than $t_{SHIPMODE}$ deglitch time (negative pulse) turns on BATFET to exit ship mode (Figure 10 left). HIZ is also enabled (EN_HIZ = 1) when exiting ship mode. After exiting ship mode, the host can disable HIZ (EN_HIZ = 0). OTG cannot be enabled (OTG_CONFIG = 1) until HIZ is disabled.

2. Reset BATFET: By applying a logic low for a duration of at least t_{QON_RST} to nQON pin and BATFET is allowed to turn on (BATFET_DIS = 0), the BATFET turns off for t_{BATFET_RST} and then it is re-enabled resulting in a system power-on reset (Figure 10 right). This function can be disabled by clearing EN_BATFET_RST bit.

A typical push button circuit for nQON is given in Figure 11.

DETAILED DESCRIPTION (continued)

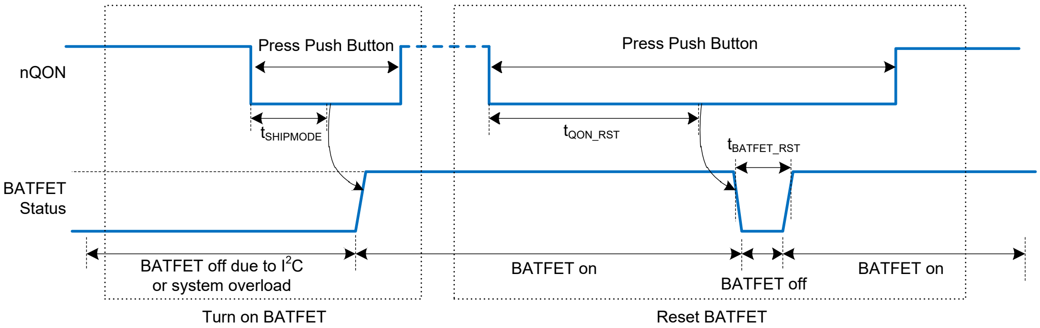


Figure 10. nQON Enable and Reset BATFET Timing

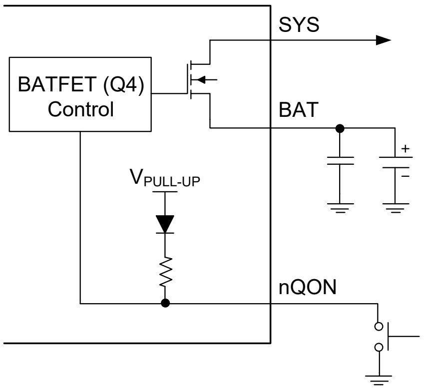


Figure 11. nQON Manual Operation Circuit

Status Outputs Pins (nINT)

Power Good Indication (PG_STAT Bit)

When a good input source is connected to VBUS and input type is detected, the PG_STAT status bit goes high. A good input source is detected if all following conditions on V_{VBUS} are satisfied and input type detection is completed:

- V_{VBUS} is in the operating range: $V_{VBUS\_UVLOZ} < V_{VBUS} < V_{VBUS\_OV}$.
- Device is not in sleep mode: $V_{VBUS} > V_{BAT} + V_{SLEEP}$.
- Input source is not poor: $V_{VBUS} > V_{VBUSMIN\_RISE}$ when I_{BAD_SRC} (25mA TYP) loading is applied. (Poor source detection.)
- Completed input source type detection.

PD PHY Interrupt to Host (PD_nINT)

Function 1: The TCPC has an open-drain output, active low PD_nINT pin. The pin is used to indicate change of state and will be asserted when any alert bits are set.

Function 2: When CH_INT_STAT = 1, charging state is indicated as explained in Table 6 and the functionality of the STAT pin is disabled if the EN_ICHG_MON[1:0] bits are set to 0b10 or 0b11. This pin is able to drive an LED.

Table 6. STAT Pin Function

Charging State	STAT Indicator
Charging battery (or recharge)	Low (LED ON)
Charging completed	High (LED OFF)
Charging is disabled or in sleep mode	High (LED OFF)
Charge is suspended due to input over-voltage, TS fault, timer faults or system over-voltage or Boost mode is suspended (TS fault)	1Hz Blinking
EN_ICHG_MON[1:0] = 01, controlled by register only, no matter with charging state	STAT_SET[1:0]

nINT Interrupt Output Pin

When a new update occurs in the charger states, a 256μs negative pulse is sent through the nINT pin to interrupt the host. The host may not continuously monitor the charger device and by receiving the interrupt, it can react and check the charger situation on time.

The following events can generate an interrupt pulse:

1. Faults reflect in REG0x09 register (watchdog, Boost overload, charge faults and battery over-voltage).
2. Charging is completed.
3. D+/D- detection identifies a connected source (USB or adapter).

DETAILED DESCRIPTION (continued)

4. Input source voltage enters the "input good" range:
   a) V_{VBUS} exceeds V_{BAT} (not in sleep mode).
   b) V_{VBUS} comes below V_{VBUS_OV}.
   c) V_{VBUS} remains above $V_{VBUSMIN\_RISE}$ when I_{BAD_SRC} (25mA TYP) load current is applied.
5. Input removes or out of the "input good" range.
6. A DPM event (VINDPM or IINDPM) occurs (a maskable interrupt).

Once a fault/flag happens, the INT pulse is asserted immediately and the fault/flag bits are updated in REG0x09 and REG0x0E. Fault/flag status is not reset in the register until the host reads it. A new fault/flag will not assert a new INT pulse until the host reads REG0x09 and REG0x0E and all the previous faults/flags are cleared. Therefore, in order to read the current time faults, the host must read REG0x09 two times consecutively. The first read returns the history of the fault register status (from the time of the last read or reset) and the second one checks the current active faults. As an exception, the NTC_FAULT[2:0] bits report the actual real-time status of TS pin.

Current Pulse Control Protocol

The device provides the control to generate the VBUS current pulse protocol to communicate with adjustable high voltage adapter, in order to signal adapter to increase/decrease output voltage. To enable the interface, the EN_PUMPX bit must be set. Then the host can select the increase/decrease voltage pulse by setting either the PUMPX_UP or PUMPX_DN bit to start the VBUS current pulse sequence. During the current pulse sequence, the PUMPX_UP and PUMPX_DN bits are set to indicate pulse sequence in progress and the device pulses the input current limit between current limit set forth by IINDPM[5:0] register and the 100mA current limit. When the pulse sequence is completed, the input current limit is returned to value set by IINDPM[5:0] register and the PUMPX_UP or PUMPX_DN bit is cleared. In addition, the EN_PUMPX bit can be cleared during the current pulse sequence to terminate the sequence and force charger to return to input current limit as set forth by the IINDPM[5:0] register immediately. When the EN_PUMPX bit is low, writing to PUMPX_UP and PUMPX_DN bits would be ignored, which has no effect on VBUS current limit.

SGM41548 Protection Features

Monitoring of Voltage and Current

During the converter operation, the input and system voltages (VBUS and VSYS) and switch currents are constantly monitored to assure safe operation of the device in both Buck and Boost modes, as described below.

Buck Mode Voltage and Current Monitoring

1. Input Over-Voltage (ACOV)

Converter switching will stop as soon as VBUS voltage exceeds V_{VBUS_OV} over-voltage limit that is programmable by OVP[1:0] in REG0x10. It is selectable among 5.5V, 6.5V, 10.5V and 14V (default) for USB or 5V, 9V or 12V adapters respectively.

Each time VBUS exceeds the OVP limit, an INT pulse is asserted. As long as the over-voltage persists, the CHRG_FAULT[1:0] bits are set to 0b01 in REG0x09. Fault will be cleared to 0b00 if the voltage comes back below limit (and a hysteresis threshold) and host reads the fault register. Charger resumes its normal operation when the voltage comes back below OVP limit.

2. System Over-Voltage (SYSOVP)

During a system load transient, the device clamps the system voltage to protect the system components from over-voltage. The SYSOVP over-voltage limit threshold is 350mV + V_{SYS_REG} (system regulation voltage + 350mV). Once a SYSOVP occurs, switching stops to clamp any overshoot and a 30mA sink current is applied to SYS to pull the voltage down.

Boost Mode Voltage and Current Monitoring

In Boost mode, the RBFET (reverse blocking) and LSFET (low-side switch) FET currents and VBUS voltage are monitored for protection.

1. Soft-Start on VBUS

Boost mode begins with a soft-start to prevent large inrush currents when it is enabled.

2. Output Short Protection for VBUS

Short-circuit protection is provided for VBUS output in Boost mode. To accept different types of load connected to VBUS and OTG adaptation, an accurate constant current regulation control is implemented for Boost mode. In case of a short-circuit on VBUS pin, the Q1 turns off and retries 7 times (Hiccup). If short is not removed after retries, the OTG will be disabled by clearing OTG_CONFIG bit. Also, an INT pulse is sent and the BOOST_FAULT bit is set to 0b1 in REG0x09. When the host activates the Boost mode again, the BOOST_FAULT bit will be cleared.

3. Output Over-Voltage Protection for VBUS

In Boost mode, converter stops switching and exits Boost mode (by clearing OTG_CONFIG bit) if VBUS voltage rises above regulation and exceeds the V_{OTG_OVP} over-voltage limit (10V TYP). An INT pulse is sent and the BOOST_FAULT bit is set to 0b1.

DETAILED DESCRIPTION (continued)

SGM41548 Thermal Regulation and Shutdown

Buck Mode Thermal Protections

Internal junction temperature (T_J) is always monitored to avoid overheating. A limit of +120℃ is considered for maximum IC surface temperature in Buck mode and if T_J intends to exceed this level, the device reduces the charge current to keep maximum temperature limited to +120℃ (thermal regulation mode) and sets the THERM_STAT bit to 0b1. As expected, the actual charging current is usually lower than programmed value during thermal regulation. Therefore, the safety timer runs at half clock rate and charge termination is disabled during thermal regulation.

If the junction temperature exceeds T_{SHUT} (+150℃), thermal shutdown protection arises in which the converter is turned off, CHRG_FAULT[1:0] bits are set to 0b10 in the fault register and an INT pulse is sent.

When the device recovers and T_J falls below the hysteresis band of T_{SHUT_HYS} (30℃ under T_{SHUT}), the converter resumes automatically.

Boost Mode Thermal Protections

Similar to Buck mode, T_J is monitored in Boost mode for thermal shutdown protection. If junction temperature exceeds T_{SHUT} (+150 ℃), the Boost mode will be disabled (OTG_CONFIG bit clears). If T_J falls below the hysteresis band of T_{SHUT_HYS} (30℃ under T_{SHUT}), the Boost can recover again by re-enabling OTG_CONFIG bit by host.

Battery Protections

Battery Over-Voltage Protection (BATOVP)

The over-voltage limit for the battery is 3.9% above the battery regulation voltage setting. In case of a BATOVP, charging or external direct charging stops right away, the BAT_FAULT bit is set to 0b1 and an INT pulse is sent.

Battery Over-Discharge Protection

If the battery discharges too much and V_{BAT} falls below the depletion level ($V_{BAT\_DPL\_FALL}$), the device turns off BATFET to protect battery. This protection is latched and is not recovered until an input source is connected to the VBUS pin. In such condition, the battery will start charging with the small I_{SHORT} current (60mA TYP) first as long as $V_{BAT} < V_{SHORTZ}$. When battery voltage is increased and $V_{SHORTZ} < V_{BAT} < V_{BATLOW}$, the charge current will increase to the pre-charge current level programmed in the IPRECHG[3:0] register.

Battery Over-Current Protection for System

The BATFET will latch off, if its current limit is exceeded due to a short or large overload on the system ($I_{BAT} > I_{BATFET\_OCP}$). To reset this latch off and enable BATFET, the "Exit Ship Mode" procedure must be followed.

USB_PD

The PD function of the PD PHY complies with USB Power Delivery spec 3.2. Some "Not support" functions are listed in the Register Maps section.

Type-C Detection

The USB_PD implements multiple comparators which can be used by software to determine the state of the CC1, CC2 pins. This status information provides the host processor all of the information required to determine attach and detach status of the cable. The USB_PD has three threshold comparators matching the USB Type-C specification for the three charge current levels, which can be detected by a Type-C device. These comparators can automatically trigger interrupts to occur when there is a state change.

Detection through Autonomous DRP Toggles

The SGM41548 offers the capability to perform autonomous DRP toggles. In DRP toggles, the SGM41548 seamlessly executes DRP toggling between SRC (source) and SNK (sink) roles. The PD PHY can also present as a SRC or SNK only and monitor CC1, CC2 status.

Dead Battery Mode

The SGM41548 provides support for dead battery mode, activated when conditions such as low battery power or the absence of VDD occurs, resulting in the inability to sustain communication over USB Type-C. In dead battery mode, the SGM41548 applies Rd to both CC1 and CC2 pins and adheres to all sink rules.

When the SGM41548 is connected to a source, it operates as a sink, facilitating the provision of VBUS power from the source. This enables the recharging of the battery to restore it to an operational level, ensuring continuous functionality and operational continuity even in challenging power conditions.

I^2C Serial Interface and Data Communication

Standard I^2C interface is used to program SGM41548 parameters and get status reports. I^2C is the well-known 2-wire serial communication interface that can connect one (or more) master device(s) to some slave devices for two-way communication. The bus lines are named serial data (SDA) and serial clock (SCL). The device that initiates a data transfer is a master. A master generates the SCL signal. Slave devices have unique addresses to identify. A master is typically a micro controller or a digital signal processor.

The SGM41548 operates as a slave device that address is 0x7C (7CH). It has 27 8-bit registers, numbered from REG0x00 to REG0x1A. A register read beyond REG0x0F returns 0xFF.

DETAILED DESCRIPTION (continued)

Physical Layer

The standard I^2C interface of SGM41548 supports standard mode and fast mode communication speeds. The frequency of standard mode is up to 100kbits/s, while the fast mode is up to 1Mbits/s. Bus lines are pulled high by weak current source or pull-up resistors and in logic high state with no clocking when the bus is free. The SDA pin is open-drain.

I^2C Data Communication

START and STOP Conditions

A transaction is started through taking control of the bus by master if the bus is free. The transaction is terminated by releasing the bus when the data transfer job is done as shown in Figure 12. All transactions are started by master which applies a START condition on the bus lines to take over the bus and exchange data. At the end, the master terminates the transaction by applying one (or more) STOP condition. START condition is generated by master when SCL is high and a high to low transition on the SDA. Similarly, a STOP is defined when SCL is high and SDA goes from low to high. START and STOP are always generated by a master. After a START and before a STOP the bus is considered busy.

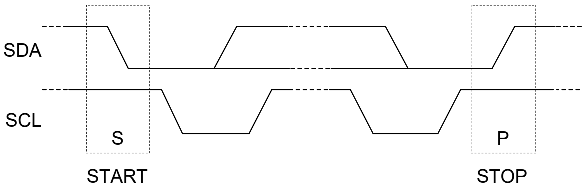


Figure 12. I^2C Bus in START and STOP Conditions

Data Bit Transmission and Validity

The data bit (high or low) must remain stable on the SDA line during the high period of the clock. The state of the SDA can only change when the clock (SCL) is low. For each data bit transmission, one clock pulse is generated by master. Bit transfer in I^2C is shown in Figure 13.

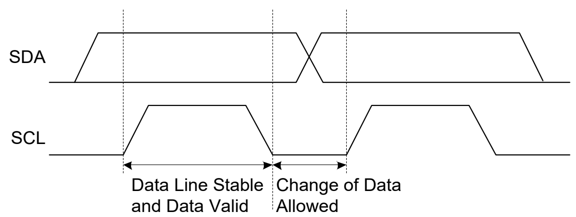


Figure 13. I^2C Bus Bit Transfer

Byte Format

Data is transmitted in 8-bit packets (one byte at a time). The number of bytes in one transaction is not limited. In each packet, the 8 bits are sent successively with the Most Significant Bit (MSB) first. An acknowledge (or not-acknowledge) bit must come after the 8 data bits. This bit informs the transmitter whether the receiver is ready to proceed for the next byte or not. Figure 14 shows the byte transfer process with I^2C interface.

Acknowledge (ACK) and Not Acknowledge (NCK)

After transmission of each byte by transmitter, an acknowledge bit is replied by the receiver as the ninth bit. With the acknowledge bit, the receiver informs the transmitter that the byte is received, and another byte is expected or can be sent (ACK) or it is not expected (NCK = not ACK). Clock (SCL) is always generated by master, including the acknowledge clock pulse, no matter who is acting as transmitter or receiver. SDA line is released for receiver control during the acknowledge clock pulse. And the receiver can pull the SDA line low as ACK (reply a 0 bit) or let it be high as NCK during the SCL high pulse. After that, the master can either apply a STOP (P) condition to end the transaction or send a new START (S) condition to start a new transfer (called repeated start). For example, when master wants to read a register in slave, one start is needed to send the slave address and register address, and then, without a STOP condition, another start is sent by master to initiate the receiving transaction from slave. Master then sends the STOP condition and releases the bus.

Data Direction Bit and Addressing Slaves

The first byte sent by master after the START is always the target slave address (7 bits) and the eighth data-direction bit ($R/\overline{W}$). $R/\overline{W}$ bit is 0b0 for a WRITE transaction and 1 for READ (when master is asking for data). Data direction is the same for all next bytes of the transaction. To reverse it, a new START or repeated START condition must be sent by master (STOP will end the transaction). Usually the second byte is a WRITE sending the register address that is supposed to be accessed in the next byte(s). The data transfer transaction is shown in Figure 15.

WRITE: If the master wants to write in the register, the third byte can be written directly as shown in Figure 16 for a single write data transfer. After receiving the ACK, master may issue a STOP condition to end the transaction or send the next register data, which will be written to the next address in a slave as multi-write. A STOP is needed after sending the last data.

READ: If the master wants to read a single register (Figure 17), it sends a new START condition along with device address with $R/\overline{W}$ bit = 1. After ACK is received, master reads the SDA line to receive the content of the register. Master replies with NCK to inform slave that no more data is needed (single read) or it can send an ACK to request for sending the next register content (multi-read). This can continue until an NCK is sent by master. A STOP must be sent by master in any case to end the transaction.

DETAILED DESCRIPTION (continued)

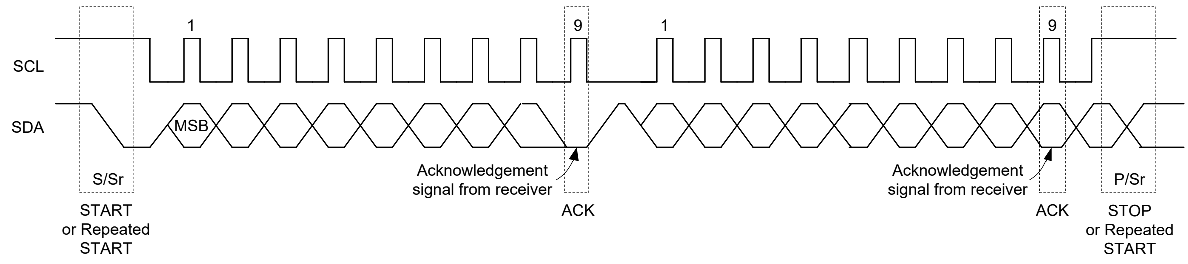


Figure 14. Byte Transfer Process

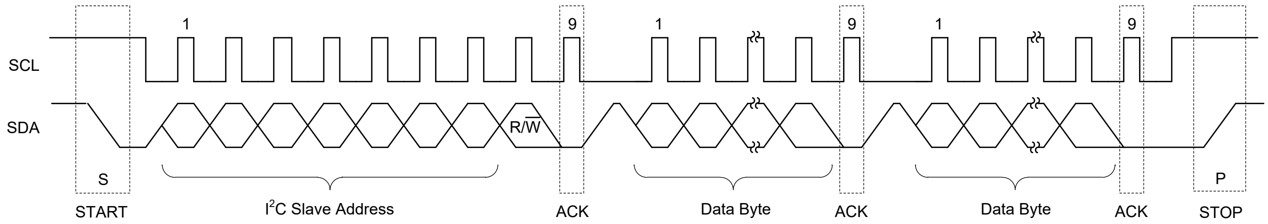


Figure 15. Data Transfer Transaction

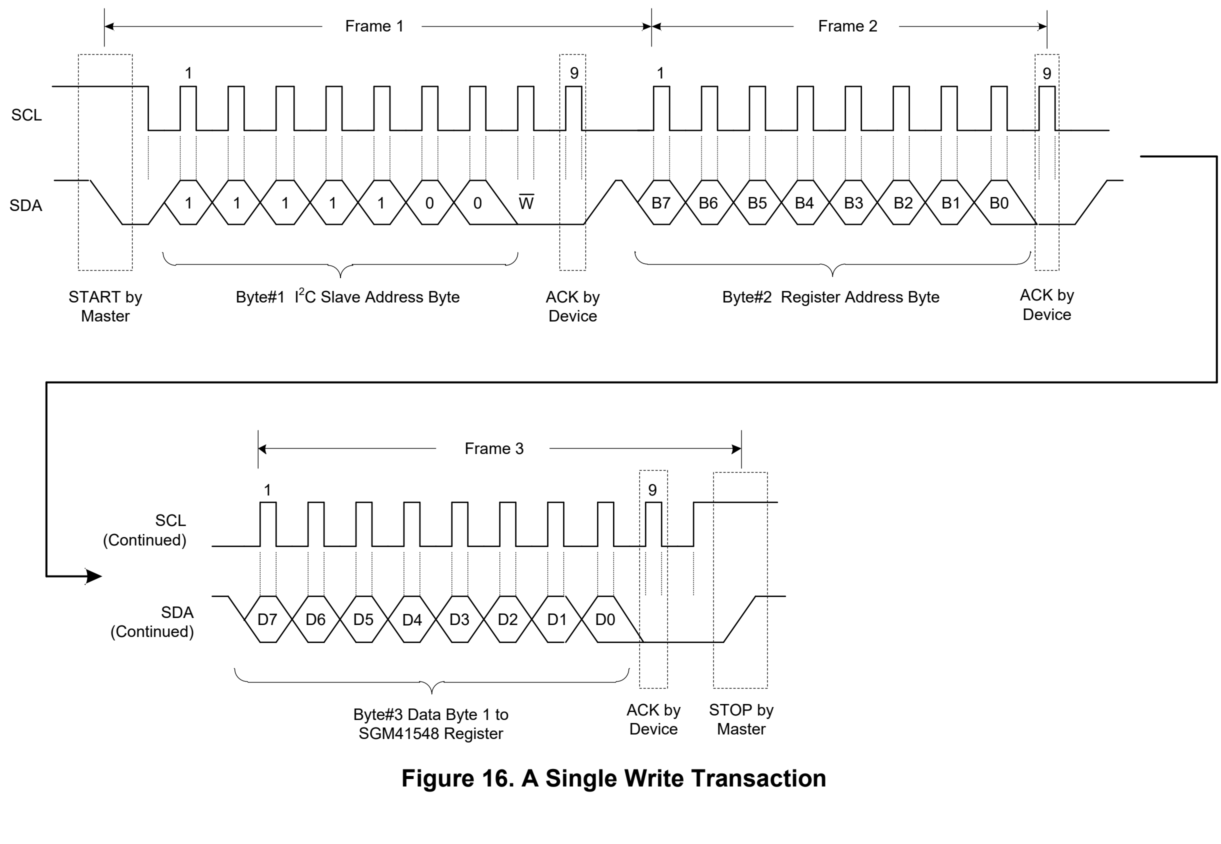


Figure 16. A Single Write Transaction

DETAILED DESCRIPTION (continued)

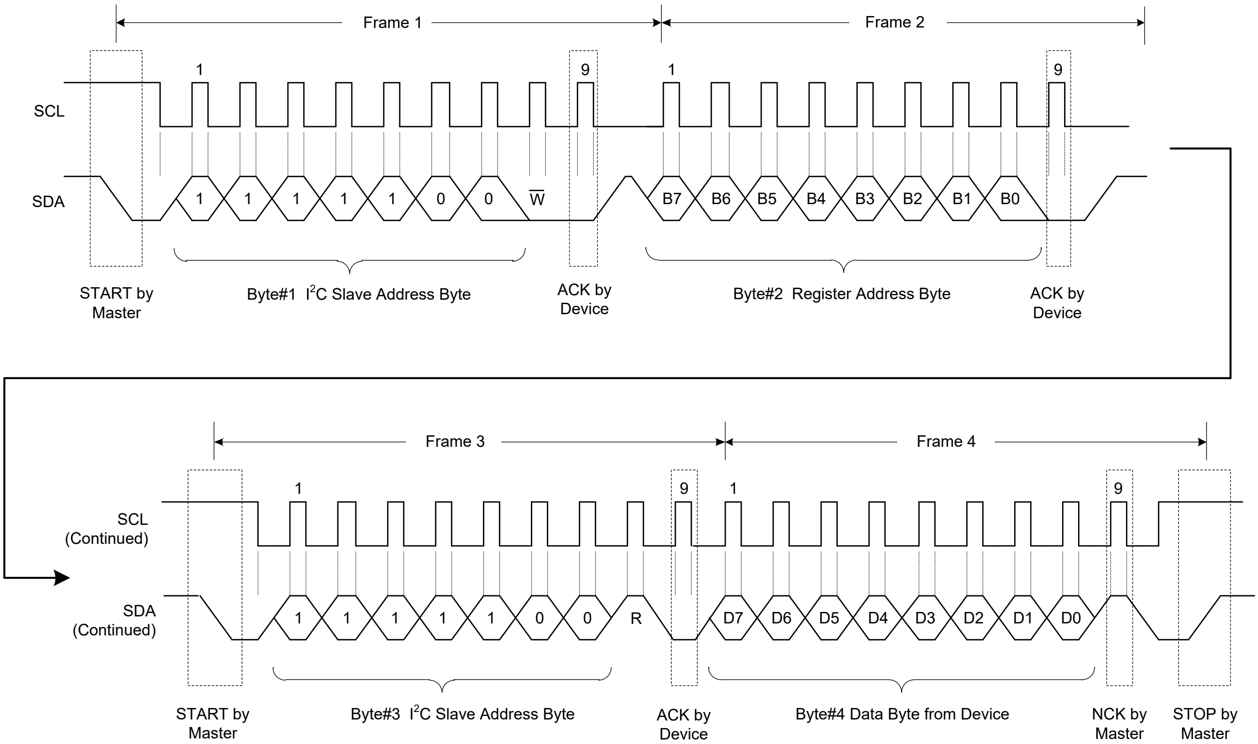


Figure 17. A Single Read Transaction

DETAILED DESCRIPTION (continued)

Data Transactions with Multi-Read or Multi-Write

Multi-read and multi-write are supported by SGM41548, as explained in Figure 18 and Figure 19. In the multi-write, every new data byte sent by master is written to the next register of the device. A STOP is sent whenever master is done with writing into device registers.

In a multi-read transaction, after receiving the first register data (its address is already written to the slave), the master replies with an ACK to ask the slave to send the next register data. This can continue as much as it is needed by master. Master sends back an NCK after the last received byte and issues a STOP condition.

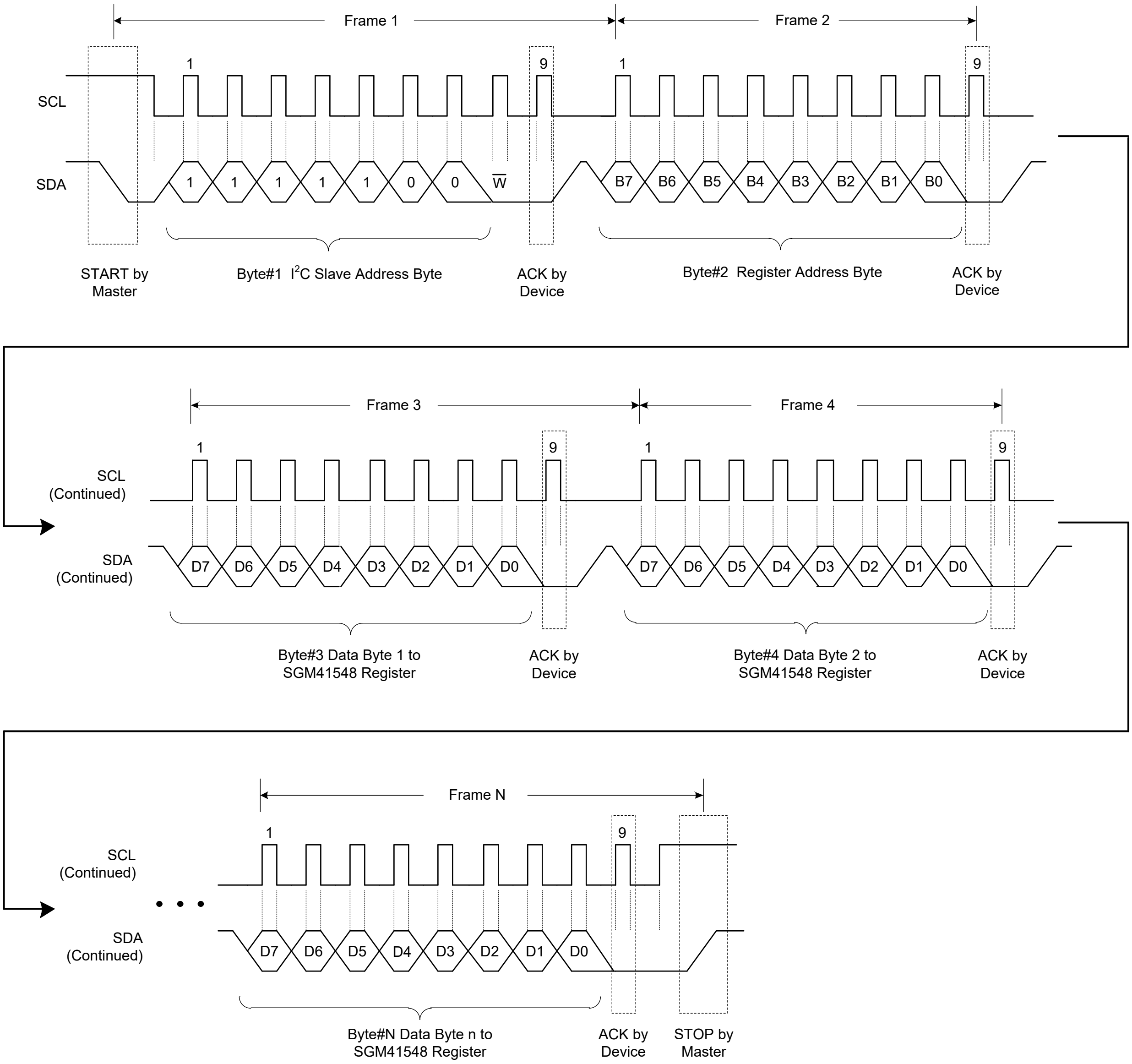


Figure 18. A Multi-Write Transaction

DETAILED DESCRIPTION (continued)

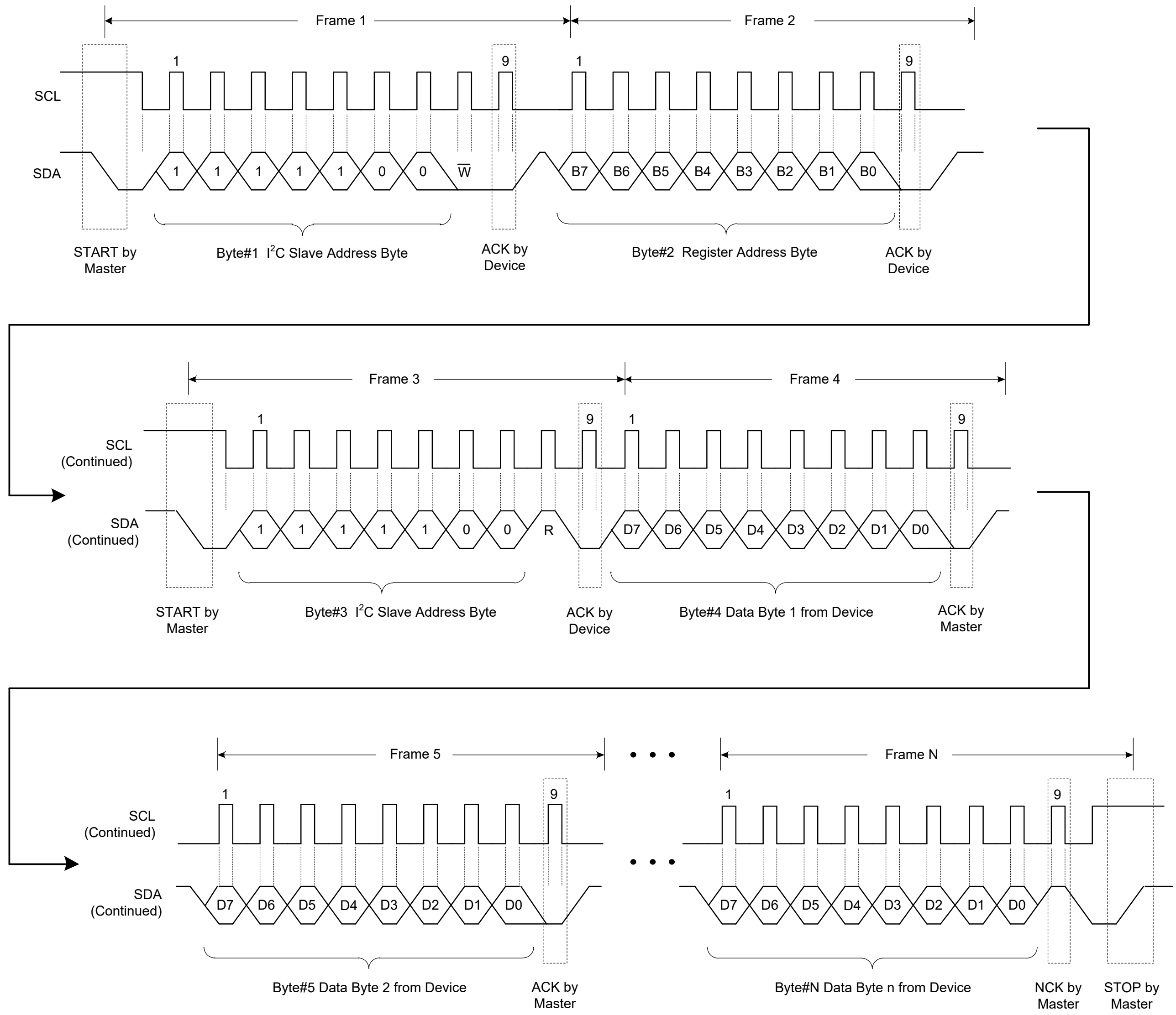


Figure 19. A Multi-Read Transaction

REGISTER MAPS FOR CHARGER

All registers are 8-bit and individual bits are named from D[0] (LSB) to D[7] (MSB).

I²C Register Address Map

FUNCTION	STAT	FLAG	MASK	THRESHOLD SETTING	ENABLE	DEGLITCH
D+/D- Detection	0x08[7:5]	0x0E[7]	—	—	0x12[2] & 0x07[7]	—
IINDPM Update	—	—	—	—	0x02[6]	—
D+/D- Output Voltage Setting	—	—	—	0x0D[4:3] / 0x0D[2:1]	—	—
Current Pulse Control (PE Protocol)	—	—	—	0x0D[6:5]	0x0D[7]	—
EN_CHG	0x08[4:3]	—	—	—	0x01[4]	—
Trickle Charge Current	0x08[4:3]	—	—	0x0F[6]	—	—
Pre-Charge Current	0x08[4:3]	—	—	0x03[7:4] & 0x10[3]	—	—
Fast Charge (Constant Current)	0x08[4:3]	—	—	0x02[5:0]	—	—
Fast Charge (Constant Voltage)	0x08[4:3] & 0x0A[4]	—	—	0x04[7:1]	—	—
Termination Setting	0x08[4:3]	—	—	0x03[3:0] & 0x10[4]	0x05[7]	0x10[5]
Termination Delay	0x0A[3]	—	—	0x11[3:2]	0x11[3:2]	—
Input Current Limit	0x0A[5]	—	0x0A[0]	0x00[5:0] & 0x0F[4]	—	—
Input Voltage Limit	0x0A[6]	—	0x0A[1]	0x06[3:0] & 0x0F[1:0] & 0x07[1:0]	—	—
Minimal System Voltage	0x08[0]	—	—	0x01[3:1]	—	—
Pre-Charge to Fast Charge Threshold	—	—	—	0x11[7:6]	—	—
Battery Recharge Threshold	—	—	—	0x11[1:0]	—	—
EN_OTG	0x08[7:5]	—	—	0x01[0]	0x01[5]	—
OTG Mode Current Limit	0x0A[5]	—	0x0A[0]	0x10[2:0]	—	—
OTG Mode Voltage	—	—	—	0x06[6:4]	—	—
Boost Mode Startup Delay	—	—	—	0x1A[3]	—	—
Switch Frequency/Capability	—	—	—	0x12[1] / 0x1A[2]	—	—
EN_HIZ		—	—	—	0x12[3]	—
PSM_FWD_DIS	—	—	—	—	0x01[7]	—
Enable Half Clock Rate Safety Timer	—	—	—	—	0x07[6]	—
Fast Charge Safety Timer	0x09[5:4]	—	—	0x05[2]	0x05[3]	—
Trickle/Pre-Charge Safety Timer	0x09[5:4]	—	—	—	0x19[1:0] & 0x05[3]	—
WATCHDOG	0x09[7]	—	—	0x05[5:4]	0x05[5:4]	—
Watchdog Timer Reset	—	—	—	—	0x01[6]	—
Registers Reset	—	—	—	—	0x0B[7]	—
System Reset	—	—	—	—	0x07[2] (& 0x1A[1] if VBUS present)	—
Exit Ship Mode Timing	—	—	—	0x0F[7]	—	—
Enter Ship Mode	—	—	—	—	0x07[5]	0x07[3]
Enable STAT pin Function	—	—	—	0x0F[3:2]	0x0F[5] & 0x00[7:6]	—
VBUS_SINK_DIS	—	—	—	—	0x1A[4]	—
Enable VBUS Pull-Down	—	—	—	—	0x1A[5]	—
JEITA Cool	0x09[2:0]	—	—	0x0C[7] & 0x05[0] & 0x0C[3:2]	0x0D[0] & 0x0C[6]	—
JEITA Warm	0x09[2:0]	—	—	0x07[4] & 0x0C[5:4] & 0x0C[1:0]	0x0D[0]	—
ADC	—	—	—	—	0x11[5:4] & 0x19[7:2]	—
Thermal Regulation	0x08[1]	—	—	0x05[1]	0x1A[0]	—
Thermal Shutdown	0x09[5:4]	—	—	—	—	—
Enable BATFET Hiccup at Thermal Shutdown	—	—	—	—	0x05[6]	—
VBUS_FAULT	0x08[2] & 0x09[5:4] & 0x0A[7] 0x0A[2]	—	—	0x10[7:6]	—	—
BAT_FAULT	0x09[3]	—	—	—	—	—
OTG_FAULT	0x09[6]	—	—	0x06[7]	—	—
BATFET OCP	—	—	—	0x12[7:6]	—	0x12[5:4]
Part Information	0x0B[6:0]	—	—	—	—	—

REGISTER MAPS FOR CHARGER (continued)

7-Bit I²C Slave Device Address: 0b1111 100 + W/R

Bit Types:

R/W: Read/Write bit(s)

R: Read only bit(s)

RC: Bit(s) cleared to 0b0 by being read

R/WC: Read/Write. Writing a 0b1 clears the bit. Writing a 0b0 has no effect.

n: Parameter code formed by the bits as an unsigned binary number.

REG0x00: Input Current Limit Register [Reset = 0x17]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:6]	EN_ICHG_MON[1:0]	00	R/W	Enable STAT Pin Function only CH_INT_STAT bit is 0b1 00 = Enable following charging state (default) 01 = Enable following STAT_SET[1:0] bits 10 = Disable (float pin) 11 = Disable (float pin) These bits turn on or off the function of the STAT open-drain output pin (charge status or customer customized indicator).	REG_RST
D[5:0]	IINDPM[5:0]	01 0111	R/W	Input Current Limit Value (n: 6 bits): = 100 + 100n (mA) Offset: 100mA Bit Step: 100mA Range: 100mA (00 0000) - 3300mA (10 0000) Default: 2400mA (01 0111) Note: Values above 0b10 0000 (3300mA) are clamped to 0b10 0000 (3300mA).	REG_RST

REG0x01: Charger Control 1 Register [Reset = 0x1A]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	PSM_FWD_DIS	0	R/W	Disable PSM Mode in Forward Buck Mode 0 = Enable (default) 1 = Disable	REG_RST
D[6]	WD_RST	0	R/WC	I²C Watchdog Timer Reset 0 = Normal (default) 1 = Reset Watchdog timer reset control bit. Write 0b1 to this bit to avoid watchdog expiry. The WD_RST bit resets to 0b0 after watchdog timer reset (expiry).	REG_RST or Watchdog
D[5]	OTG_CONFIG	0	R/W	Enable OTG 0 = OTG disable (default) 1 = OTG enable This bit has priority over charge enable in the CHG_CONFIG.	REG_RST or Watchdog
D[4]	CHG_CONFIG	1	R/W	Enable Battery Charging 0 = Charge disable 1 = Charge enable (default) Charge is enabled when CHG_CONFIG bit is 0b1 and nCE pin is pulled low.	REG_RST or Watchdog
D[3:1]	SYS_MIN[2:0]	101	R/W	Minimum System Voltage 000 = 2.6V 001 = 2.8V 010 = 3V 011 = 3.2V 100 = 3.4V 101 = 3.5V (default) 110 = 3.6V 111 = 3.7V	REG_RST
D[0]	MIN_BAT_SEL	0	R/W	Minimum Battery Voltage for OTG Mode 0 = 3V V_{BAT} falling (default) 1 = 2.7V V_{BAT} falling Default: V_{BAT} falling, V_{BATLOW_OTG} = 3V. V_{BAT} rising, V_{BATLOW_OTG} = 3.2V.	REG_RST

REGISTER MAPS FOR CHARGER (continued)

REG0x02: Charge Current Limit Register [Reset = 0x22]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	Reserved	0	R/W	Reserved	REG_RST
D[6]	IINDPM_UPDATE_DIS	0	R/W	Disable Bit for IINDPM Updating after DPDM Detection 0 = Enable (default) 1 = Disable	REG_RST or Watchdog
D[5:0]	ICHG[5:0]	10 0010	R/W	Fast Charge Current Value (n: 6 bits): = 60n (mA) Offset: 0mA Bit Step: 60mA Range: 0mA (00 0000) - 3780mA (11 1111) Default: 2040mA (10 0010) Note: Setting ICHG[5:0] = 0mA disables charge	REG_RST or Watchdog

REG0x03: Pre-Charge and Termination Current Limit Register [Reset = 0x55]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:4]	IPRECHG[3:0]	0101	R/W	Pre-Charge Current Limit (n: 4 bits): = 30 + 30n (mA) Offset: 30mA Bit Step: 30mA Range: 30mA (0000) - 480mA (1111) Default: 180mA (0101)	REG_RST or Watchdog
D[3:0]	ITERM[3:0]	0101	R/W	Termination Current Limit (n: 4 bits): = 30 + 30n (mA) Offset: 30mA Bit Step: 30mA Range: 30mA (0000) - 480mA (1111) Default: 180mA (0101)	REG_RST or Watchdog

REG0x04: Battery Voltage Limit Register [Reset = 0x8C]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:1]	VREG[6:0]	100 0110	R/W	Charge Voltage Limit (n: 7 bits): = 3500 + 10n (mV) Offset: 3.5V Bit Step: 10mV Range: 3500mV (000 0000) - 4770mV (111 1111) Default: 4.200V (100 0110)	REG_RST or Watchdog
D[0]	Reserved	0	R/W	Reserved	REG_RST or Watchdog

REGISTER MAPS FOR CHARGER (continued)

REG0x05: Charger Control 2 Register [Reset = 0x9F]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	EN_TERM	1	R/W	Charging Termination Enable 0 = Disable 1 = Enable (default)	REG_RST or Watchdog
D[6]	EN_TSD_DISFET	0	R/W	At thermal shutdown mode, turn off BATFET, and then hiccup to measure T_J to resume BATFET. 0 = Disable (default) 1 = Enable	REG_RST
D[5:4]	WATCHDOG[1:0]	01	R/W	Watchdog Timer Setting 00 = Disable watchdog timer 01 = 40s (default) 10 = 80s 11 = 160s Expiry time of the watchdog timer if it is not reset.	REG_RST or Watchdog
D[3]	EN_TIMER	1	R/W	Charge Safety Timer Enable 0 = Disable 1 = Enable (default) When it is enabled, the trickle charge, pre-charge and fast charge periods are included in the timing. When it is disabled, charge safety timer is disabled regardless of REG0x19 D[1:0].	REG_RST or Watchdog
D[2]	CHG_TIMER	1	R/W	Charge Safety Timer in Fast Charge Setting 0 = 7h 1 = 16.2h (default)	REG_RST or Watchdog
D[1]	TREG	1	R/W	Thermal Regulation Threshold 0 = 80℃ 1 = 120℃ (default) For Buck mode.	REG_RST or Watchdog
D[0]	JEITA_ISET_L (0℃ - 10℃)	1	R/W	JEITA Cool Charging Current Setting 0 = 50% of ICHG[5:0] 1 = 20% of ICHG[5:0] (default) When EN_JEITA_ISET_L bit is 0b1.	REG_RST or Watchdog

REGISTER MAPS FOR CHARGER (continued)

REG0x06: Charger Control 3 Register [Reset = 0x26]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	OTG_OVP	0	R/W	Boost Over-Voltage Threshold on VBUS Voltage Sense 0 = 10V (default) 1 = 6.25V	REG_RST or Watchdog
D[6:4]	BOOSTV[2:0]	010	R/W	Boost Mode Voltage Regulation 000 = 4.85V 001 = 5.00V 010 = 5.175V (default) 011 = 5.30V 100 = 7V 101 = 7.5V 110 = 9V 111 = 9V	REG_RST
D[3:0]	VINDPM[3:0]	0110	R/W	VINDPM Threshold (n: 4 bits): = Offset + 0.1n (V) Offset: 3.9V (VINDPM_OS[1:0] = 00, default) Bit Step: 100mV Range: 3.9V (0000) - 5.4V (1111) Default: 4.5V (0110) Offset: 5.9V (VINDPM_OS[1:0] = 01) Bit Step: 100mV Range: 5.9V (0000) - 7.4V (1111) Offset: 7.5V (VINDPM_OS[1:0] = 10) Bit Step: 100mV Range: 7.5V (0000) - 9V (1111) Offset: 10.5V (VINDPM_OS[1:0] = 11) Bit Step: 100mV Range: 10.5V (0000) - 12V (1111)	REG_RST

REGISTER MAPS FOR CHARGER (continued)

REG0x07: Charger Control 4 Register [Reset = 0x4C]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	EN_IINDET	0	R/WC	Input Current Limit Detection 0 = Not in input current limit detection (default) 1 = Force input current limit detection when VBUS is present Reload with 0 when input detection is completed.	REG_RST or Watchdog
D[6]	EN_TMR2X	1	R/W	Enable Half Clock Rate Safety Timer 0 = Disable 1 = Safety timer slows down during DPM, JEITA cool, or thermal regulation (default) Slow down by a factor of 2.	REG_RST or Watchdog
D[5]	BATFET_DIS	0	R/W	Disable BATFET 0 = Allow BATFET (Q4) to turn on (default) 1 = Turn off BATFET (Q4) after a t_{SM_DLY} delay time (REG0x07 D[3]) t_{SM_DLY} is typically 12.3 seconds.	REG_RST
D[4]	JEITA_VSET_H (45℃ - 60℃)	0	R/W	JEITA Warm Charging Voltage Setting 0 = The lower of 4.1V and VREG[6:0] (default) 1 = VREG[6:0]	REG_RST or Watchdog
D[3]	BATFET_DLY	1	R/W	BATFET Turn Off Delay Control 0 = Turn off BATFET immediately 1 = Turn off BATFET after t_{SM_DLY} (default) BATFET_DIS bit is set.	REG_RST
D[2]	EN_BATFET_RST	1	R/W	nQON Pulled Down for t_{QON_RST} Allows BATFET Reset for System Power Reset 0 = Disable BATFET reset 1 = Enable BATFET reset (default)	REG_RST or Watchdog
D[1:0]	VDPM_BAT_ TRACK[1:0]	00	R/W	Dynamic VINDPM Tracking 00 = Disable (V_{INDPM} set by register) (default) 01 = V_{BAT} + 200mV 10 = V_{BAT} + 250mV 11 = V_{BAT} + 300mV Set V_{INDPM} to track V_{BAT} voltage. Actual V_{INDPM} is the larger of VINDPM[3:0] value and this register value.	REG_RST

REG0x08: Charger Status 1 Register [Reset = 0xXX]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:5]	VBUS_STAT[2:0]	xxx	R	VBUS Status Register 000 = No input 001 = USB SDP (500mA) 010 = USB CDP (1.5A) 011 = USB DCP (2.4A) 101 = Unknown adapter (500mA) 110 = Non-standard adapter (1A/2A/2.1A/2.4A) 111 = OTG Current limit value is reported in IINDPM[5:0] register.	N/A
D[4:3]	CHRG_STAT[1:0]	xx	R	Charging Status 00 = Charge disable 01 = Pre-charge (V_{BAT} < V_{BATLOW}) 10 = Fast charging (constant current or voltage) 11 = Charging terminated	N/A
D[2]	PG_STAT	x	R	Input Power Status (VBUS in good voltage range and not poor) 0 = Input power source is not good 1 = Input power source is good	N/A
D[1]	THERM_STAT	x	R	Thermal Regulation Status 0 = Not in thermal regulation 1 = In thermal regulation	N/A
D[0]	VSYS_STAT	x	R	System Voltage Regulation Status 0 = Not in VSYSMIN regulation (V_{BAT} > V_{SYS_MIN}) 1 = In VSYSMIN regulation (V_{BAT} < V_{SYS_MIN})	N/A

REGISTER MAPS FOR CHARGER (continued)

REG0x09: Fault Status Register [Reset = 0xXX]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	WATCHDOG_FAULT	x	R	Watchdog Fault Status 0 = Normal (no fault) 1 = Watchdog timer expired	N/A
D[6]	BOOST_FAULT	x	R	Boost Mode Fault Status 0 = Normal 1 = VBUS is overloaded in OTG, or VBUS OVP, or battery voltage is too low (any condition that prevents Boost starting)	N/A
D[5:4]	CHRG_FAULT[1:0]	xx	R	Charging Fault Status 00 = Normal 01 = Input fault (VBUS OVP or V_{BAT} < V_{VBUS} < 3.8V) 10 = Thermal shutdown 11 = Charge safety timer expired	N/A
D[3]	BAT_FAULT	x	R	Battery Fault Status 0 = Normal 1 = Battery over-voltage (BATOVP)	N/A
D[2:0]	NTC_FAULT[2:0]	xxx	R	JEITA Condition Based on Battery NTC Temperature Measurement 000 = Normal 010 = Warm (Buck mode only) 011 = Cool (Buck mode only) 101 = Cold 110 = Hot NTC fault bits are updated in real-time and do not need a read to reset.	N/A

REG0x0A: Charger Status 2 Register [Reset = 0xXX]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	VBUS_GD	x	R	Good Input Source Detected 0 = A good VBUS is not attached 1 = A good VBUS is attached	N/A
D[6]	VINDPM_STAT	x	R	Input Voltage Regulation (Dynamic Power Management) 0 = Not in VINDPM 1 = In VINDPM	N/A
D[5]	IINDPM_STAT	x	R	Input Current Regulation (Dynamic Power Management) 0 = Not in IINDPM 1 = In IINDPM	N/A
D[4]	CV_STAT	x	R	CV Mode Status Indicator 0 = V_{BAT} is lower than VREG[6:0] 1 = V_{BAT} approaches to VREG[6:0]	N/A
D[3]	TOPOFF_ACTIVE	x	R	Active Top-Off Timer Counting Status 0 = Top-off timer is not counting 1 = Top-off timer is counting	N/A
D[2]	ACOV_STAT	x	R	Input Over-Voltage Status (AC adapter is the input source) 0 = No over-voltage (no ACOV) 1 = Over-voltage is detected (ACOV)	N/A
D[1]	VINDPM_INT_MASK	0	R/W	VINDPM Event Detection Interrupt Mask 0 = Allow VINDPM to send INT pulse (default) 1 = Mask VINDPM INT pulse	REG_RST
D[0]	IINDPM_INT_MASK	0	R/W	IINDPM Event Detection Mask 0 = Allow IINDPM to send INT pulse (default) 1 = Mask IINDPM INT pulse	REG_RST

REGISTER MAPS FOR CHARGER (continued)

REG0x0B: Part Information Register [Reset = 0x6X]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	REG_RST	0	R/WC	Register Reset 0 = No effect (keep current register settings) (default) 1 = Reset R/W bits of all registers to the default and reset safety timer (it also resets itself to 0b0 after register reset is completed.)	REG_RST
D[6:3]	PN[3:0]	1101	R	Part ID 1101 = SGM41548	N/A
D[2]	SGMPART	1	R		N/A
D[1:0]	DEV_REV[1:0]	00	R	Revision	N/A

REG0x0C: Charger Control 5 Register [Reset = 0x75]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	JEITA_VSET_L (0℃ - 10℃)	0	R/W	JEITA Cool Charge Voltage Setting 0 = VREG[6:0] (default) 1 = The lower of 4.1V and VREG[6:0]	REG_RST or Watchdog
D[6]	EN_JEITA_ISET_L (0℃ - 10℃)	1	R/W	Charge Enable during Cool Temperature 0 = Disable 1 = Enable (default)	REG_RST or Watchdog
D[5:4]	JEITA_ISET_H[1:0] (45℃ - 60℃)	11	R/W	JEITA Warm Charge Current Setting 00 = 0% of ICHG[5:0] 01 = 20% of ICHG[5:0] 10 = 50% of ICHG[5:0] 11 = 100% of ICHG[5:0] (default) In warm condition, the safety timer does not become 2X.	REG_RST or Watchdog
D[3:2]	JEITA_VT2[1:0]	01	R/W	JEITA Cool Threshold Setting 00 = V_{T2} = 70.75% (5.5℃) 01 = V_{T2} = 68.1% (10℃) (default) 10 = V_{T2} = 65.25% (15℃) 11 = V_{T2} = 62.25% (20℃)	REG_RST or Watchdog
D[1:0]	JEITA_VT3[1:0]	01	R/W	JEITA Warm Threshold Setting 00 = V_{T3} = 48.25% (40℃) 01 = V_{T3} = 44.5% (45℃) (default) 10 = V_{T3} = 40.75% (50.5℃) 11 = V_{T3} = 37.75% (54.5℃)	REG_RST or Watchdog

REGISTER MAPS FOR CHARGER (continued)

REG0x0D: Charger Control 6 Register [Reset = 0x01]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	EN_PUMPX	0	R/W	Current Pulse Control Enable 0 = Disable (default) 1 = Enable (PUMPX_UP and PUMPX_DN)	REG_RST or Watchdog
D[6]	PUMPX_UP	0	R/WC	Current Pulse Control Voltage Up Enable 0 = Disable (default) 1 = Enable This bit is can only be set when EN_PUMPX bit is set and returns to 0 after current pulse control sequence is completed.	REG_RST or Watchdog
D[5]	PUMPX_DN	0	R/WC	Current Pulse Control Voltage Down Enable 0 = Disable (default) 1 = Enable This bit is can only be set when EN_PUMPX bit is set and returns to 0 after current pulse control sequence is completed.	REG_RST or Watchdog
D[4:3]	DP_VSET[1:0]	00	R/W	D+ Output Voltage Setting 00 = HIZ (default) 01 = 0V 10 = 0.6V 11 = 3.3V Register bits are reset to default value when input source is plugged in and can be changed after D+/D- detection is completed.	REG_RST or Watchdog or Adapter Plug-In
D[2:1]	DM_VSET[1:0]	00	R/W	D- Output Voltage Setting 00 = HIZ (default) 01 = 0V 10 = 0.6V 11 = 3.3V Register bits are reset to default value when input source is plugged in and can be changed after D+/D- detection is completed.	REG_RST or Watchdog or Adapter Plug-In
D[0]	EN_JEITA	1	R/W	JEITA Enable 0 = Disable 1 = Enable (default)	REG_RST or Watchdog

REGISTER MAPS FOR CHARGER (continued)

REG0x0E: Charger Flag Register [Reset = 0xXX]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	INPUT_DET_DONE_FLAG	x	RC	VBUS Input Detection Done Flag 0 = Normal 1 = Detection done DPDM detection done flag after VBUS plug-in or set EN_IINDET = 1. Reading this bit will reset it to 0b0.	N/A
D[6:0]	Reserved	xxx xxxx	R	Reserved	N/A

REG0x0F: Charger Control 7 Register [Reset = 0x80]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	tSHIPMODE	1	R/W	nQON Negative Pulse Low Pulse Width to Turn on BATFET and Exit Ship Mode 0 = 100ms 1 = 1s (default)	REG_RST
D[6]	ISHORT_SET	0	R/W	Trickle Charge Current Setting 0 = 60mA (default) 1 = 120mA	REG_RST or Watchdog
D[5]	CH_INT_STAT	0	R/W	PD_nINT Pin or Charge Status (STAT Pin) Function 0 = PD_nINT Pin function (default) 1 = Charge Status (STAT Pin) function	REG_RST
D[4]	IINDPM_SET	0	R/W	Setting Bit for Actual Input Current Limit 0 = Actual Input current limit is equal to 95% of the setting value by IINDPM[5:0] bits (default) 1 = Actual Input current limit is equal to 80% of the setting value by IINDPM[5:0] bits	REG_RST or Watchdog
D[3:2]	STAT_SET[1:0]	00	R/W	STAT Pin Output Setting 00 = LED off (HIZ) (default) 01 = LED on (low) 10 = LED Blinking 1s on 1s off 11 = LED Blinking 1s on 3s off This bits only takes effect when EN_ICHG_MON[1:0] bits are 0b01 and CH_INT_STAT bit is 0b1.	REG_RST or Watchdog
D[1:0]	VINDPM_OS[1:0]	00	R/W	VINDPM Offset 00 = 3.9V (default) 01 = 5.9V 10 = 7.5V 11 = 10.5V	REG_RST

REGISTER MAPS FOR CHARGER (continued)

REG0x10: Charger Control 8 Register [Reset = 0xDA]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:6]	OVP[1:0]	11	R/W	VBUS Pin OVP Threshold 00 = 5.5V 01 = 6.5V (5V input) 10 = 10.5V (9V input) 11 = 14V (12V input) (default) OVP threshold for input supply.	REG_RST
D[5]	ITERM_TIMER	0	R/W	ITERM Deglitch Timer Setting 0 = 230ms (default) 1 = 16ms	REG_RST or Watchdog
D[4]	ITERM_SEL	1	R/W	I_{TERM} Range Select in Charge Mode 0 = ITERM[3:0] × 2 1 = ITERM[3:0] (default)	REG_RST or Watchdog
D[3]	IPRECHG_SEL	1	R/W	I_{PRECHG} Range Select in Charge Mode 0 = IPRECHG[3:0] × 2 1 = IPRECHG[3:0] (default)	REG_RST or Watchdog
D[2:0]	BOOST_LIM[2:0]	010	R/W	Boost Mode Current Limit 000 = 0.5A 001 = 1A 010 = 1.2A (default) 011 = 1.5A 100 = 2A 101 = 2.5A 110 = 3A 111 = 3.2A	REG_RST or Watchdog

REG0x11: Charger Control 9 Register [Reset = 0x80]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:6]	BATLOWV[1:0]	10	R/W	Battery Pre-Charge to Fast Charge Threshold 00 = 2.8V 01 = 3.0V 10 = 3.15V (default) 11 = 3.15V	REG_RST or Watchdog
D[5]	CONV_START	0	R/W	ADC Conversion Start Control 0 = ADC conversion not active (default) 1 = Start ADC conversion This bit is read-only when CONV_RATE bit is 0b1. The bit stays high during ADC conversion.	REG_RST or Watchdog
D[4]	CONV_RATE	0	R/W	ADC Conversion Rate Selection 0 = One shot ADC conversion (default) 1 = Start 1s continuous conversion When set 0b0, which ADC conversion is active depends on REG0x19. When set 0b1, all ADC conversions are active.	REG_RST or Watchdog
D[3:2]	TOPOFF_TIMER[1:0]	00	R/W	Top-Off Timer 00 = Disabled (default) 01 = 15 minutes 10 = 35 minutes 11 = 45 minutes The charge extension time is added after the termination condition is detected. If disabled, charging terminates as soon as termination conditions are met.	REG_RST or Watchdog
D[1:0]	VRECHG[1:0]	00	R/W	Battery Recharge Threshold 00 = 100mV below VREG[6:0] (default) 01 = 200mV below VREG[6:0] 10 = 300mV below VREG[6:0] 11 = 400mV below VREG[6:0] A recharge cycle will start if a fully charged battery voltage drops below VREG[6:0] - VRECHG[1:0] settings.	REG_RST or Watchdog

REGISTER MAPS FOR CHARGER (continued)

REG0x12: Charger Control 10 Register [Reset = 0xC4]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:6]	IBATOCP[1:0]	11	R/W	BATFET OCP 00 = 6A 01 = 8A 10 = 10A 11 = 12A (default)	REG_RST or Watchdog
D[5:4]	IBATOCP_DEG[1:0]	00	R/W	BATFET OCP Deglitch Time 00 = 128μs (default) 01 = 256μs 10 = 1ms 11 = 2ms	REG_RST or Watchdog
D[3]	EN_HIZ	0	R/W	Enable HIZ Mode 0 = Disable (default) 1 = Enable In HIZ mode, the VBUS pin is effectively disconnected from internal circuit. Some leakage current may exist.	REG_RST or Watchdog or Adapter Plug-In
D[2]	BC1.2	1	R/W	BC1.2 Auto Detection 0 = Disable 1 = Enable (default)	REG_RST or Watchdog
D[1]	OTGF	0	R/W	Frequency Select in Boost Mode 0 = 1.5MHz (default) 1 = 500kHz	REG_RST or Watchdog
D[0]	Reserved	0	R	Reserved	N/A

REG0x13: VBAT_ADC Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	BATV[7:0]	0000 0000	R	ADC Conversion of Battery Voltage (V_{BAT}): = 2304 + 10.98n (mV) Offset: 2.304V Bit Step: 10.98mV Range: 2.304V (0000 0000) - 4.851V (1110 1000) Default: 2.304V (0000 0000) 1110 1001 - 1111 1111 = Reserved	N/A

REG0x14 VSYS_ADC Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	SYSV[7:0]	0000 0000	R	ADC conversion of System Voltage (V_{SYS}): = 2304 + 10.98n (mV) Offset: 2.304V Bit Step: 10.98mV Range: 2.304V (0000 0000) - 4.851V (1110 1000) Default: 2.304V (0000 0000) 1110 1001 - 1111 1111 = Reserved	N/A

REGISTER MAPS FOR CHARGER (continued)

REG0x15: TS_ADC Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	TSPCT[7:0]	0000 0000	R	ADC Conversion of TS Voltage (TS) as Percentage of REGN: = 21 + 0.543n (%) Offset: 21% Bit Step: 0.543% Range: 21% (0000 0000) - 81.273% (0110 1111) Default: 21% (0000 0000) 0111 0000 - 1111 1111 = Reserved	N/A

REG0x16: VBUS_ADC Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	VBUSV[7:0]	0000 0000	R	ADC Conversion of VBUS Voltage (V_{VBUS}): = 2600 + 50n (mV) Offset: 2.6V Bit Step: 50mV Range: 2.6V (0000 0000) - 15.35V (1111 1111) Default: 2.6V (0000 0000)	N/A

REG0x17: IBAT_ADC Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	ICHGR[7:0]	0000 0000	R	ADC Conversion of Charge Current (I_{BAT}): = 25.1n (mA) Offset: 0mA Bit Step: 25.1mA Range: 0mA (0000 0000) - 6400mA (1111 1111) Default: 0mA (0000 0000)	N/A

REG0x18: IBUS_ADC Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	IBUSR[7:0]	0000 0000	R	ADC Conversion of Input Current (I_{VBUS}): = 25.1n (mA) Offset: 0mA Bit Step: 25.1mA Range: 0mA (0000 0000) - 3313mA (1000 0100) Default: 0mA (0000 0000) 1000 0101 - 1111 1111 = Reserved	N/A

REGISTER MAPS FOR CHARGER (continued)

REG0x19: ADC_Function_Disable Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	IBUS_ADC_DIS	0	R/W	IBUS ADC Control 0 = Enable (default) 1 = Disable	REG_RST
D[6]	IBAT_ADC_DIS	0	R/W	IBAT ADC Control 0 = Enable (default) 1 = Disable	REG_RST
D[5]	VBUS_ADC_DIS	0	R/W	VBUS ADC Control 0 = Enable (default) 1 = Disable	REG_RST
D[4]	VBAT_ADC_DIS	0	R/W	VBAT ADC Control 0 = Enable (default) 1 = Disable	REG_RST
D[3]	VSYS_ADC_DIS	0	R/W	VSYS ADC Control 0 = Enable (default) 1 = Disable	REG_RST
D[2]	TS_ADC_DIS	0	R/W	TS ADC Control 0 = Enable (default) 1 = Disable	REG_RST
D[1]	SAFETY_TRKCHG_DIS	0	R/W	Charge Safety Timer In Trickle Charge Disable 0 = Enable (default) 1 = Disable	REG_RST
D[0]	SAFETY_PRECHG_DIS	0	R/W	Charge Safety Timer In Pre-Charge Disable 0 = Enable (default) 1 = Disable	REG_RST

REG0x1A: MISC_CTRL Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:6]	Reserved	00	R/W	Reserved	REG_RST
D[5]	EN_VBUS_PD	0	R/W	Enable the VBUS 2kΩ Pull-Down Resistor 0 = Disable the VBUS pull-down resistor (default) 1 = Enable the VBUS pull-down resistor	REG_RST
D[4]	VBUS_SINK_DIS	0	R/W	Disable the VBUS Sink during Poor Source Detection 0 = Enable the 25mA VBUS sink with 30ms (default) 1 = Disable the VBUS sink	REG_RST
D[3]	OTG_SS_SR	0	R/W	Boost Mode Startup Delay and Soft-start Slew Rate Control 0 = 30ms delay and 100mV/500μs soft-start slew rate (default) 1 = 8ms delay and 100mV/128μs soft-start slew rate	REG_RST
D[2]	DRV_CAPACITY	0	R/W	Driver Capacity for the Power MOSFET 0 = Normal capacity (default) 1 = Increased capacity	REG_RST
D[1]	BATFET_RST_WVBUS	0	R/W	Allow BATFET Reset for System Power Reset with/without VBUS Present 0 = Only reset BATFET without VBUS present (default) 1 = Can reset BATFET with VBUS present	REG_RST
D[0]	TJ_REG _CTRL	0	R/W	T_J Regulation Loop Control 0 = Only enable the T_J regulation loop in charge mode (default) 1 = Enable the T_J regulation loop in Buck mode	REG_RST

REGISTER MAPS FOR PD PHY

I²C Register Address Map

ADDRESS	REGISTER NAME	DEFAULT	TYPE
Identification Registers			
0x00	VENDOR_ID Register	0x7E	R
0x01	VENDOR_ID Register	0x37	R
0x02	PRODUCT_ID Register	0x48	R
0x03	PRODUCT_ID Register	0x05	R
0x04	DEVICE_ID Register	0x00	R
0x05	DEVICE_ID Register	0x01	R
0x06	USBTYPEC_REV Register	0x23	R
0x07	USBTYPEC_REV Register	0x00	R
0x08	USBPD_VER Register	0x10	R
0x09	USBPD_REV Register	0x32	R
0x0A	PDIF_VER Register	0x13	R
0x0B	PDIF_REV Register	0x20	R
Alert Registers			
0x10	ALERT_L Register	0x00	R/WC
0x11	ALERT_H Register	0x00	R/WC
Mask Registers			
0x12	ALERT_L_MASK Register	0x7F	R/W
0x13	ALERT_H_MASK Register	0x26	R/W
0x14	POWER_STATUS_MASK Register	0x4C	R/W
0x15	FAULT_STATUS_MASK Register	0x01	R/W
0x16	EXTENDED_STATUS_MASK Register	0x01	R/W
Control Registers			
0x19	TCPC_CONTROL Register	0x00	R/W
0x1A	ROLE_CONTROL Register	0x0A	R/W
Status Registers			
0x1D	CC_STATUS Register	0x00	R
0x1E	POWER_STATUS Register	0x00	R
0x1F	FAULT_STATUS Register	0x00	R/WC
0x20	EXTENDED_STATUS Register	0x00	R
Command Register			
0x23	COMMAND Register	0x00	R/WC
Capabilities Registers			
0x24	DEVICE_CAPABILITIES_1L Register	0xD0	R
0x25	DEVICE_CAPABILITIES_1H Register	0x02	R
0x26	DEVICE_CAPABILITIES_2L Register	0x3E	R
0x27	DEVICE_CAPABILITIES_2H Register	0x00	R
0x28	STANDARD_INPUT_CAPABILITIES Register	0x00	R
0x29	STANDARD_OUTPUT_CAPABILITIES Register	0x00	R
MESSAGE_HEADER_INFO Register			
0x2E	MESSAGE_HEADER_INFO Register	0x02	R/W

REGISTER MAPS FOR PD PHY (continued)

ADDRESS	REGISTER NAME	DEFAULT	TYPE
Receive Detect Register			
0x2F	RECETVE_DETECT Register	0x00	R/W
Receive Buffer Registers			
0x30	RX_BYTE_COUNT Register	0x00	R
0x31	RX_BUF_FRAME_TYPE Register	0x00	R
0x32	RX_BUF_HEADER_BYTE_0 Register	0x00	R
0x33	RX_BUF_HEADER_BYTE_1 Register	0x00	R
0x34 ~ 0x4F	RX_BUF_OBJx(1 ~ 7)_BYTE_x(0 ~ 3) Register	0x00	R
Transmit Register			
0x50	TX_BUF_FRAME_TYPE Register	0x00	R/W
Transmit Buffer Registers			
0x51	TX_BYTE_COUNT Register	0x00	R/W
0x52	TX_BUF_HEADER_BYTE_0 Register	0x00	R/W
0x53	TX_BUF_HEADER_BYTE_1 Register	0x00	R/W
0x54 ~ 0x6F	TX_BUF_OBJx(1 ~ 7)_BYTE_x(0 ~ 3) Register	0x00	R/W
Vendor Defined Registers			
0x97	VENDOR_DEFINED_STATUS Register	0x00	R
0x98	SG_INT Register	0x00	R/WC
0x99	VENDOR_DEFINED_ALERT_MASK Register	0x00	R/WC
0x9B	SG_SHUTDOWN Register	0x00	R/WC
0xA0	RESET_CTRL Register	0x30	R/W, R/WC
0xA2	TDRP Register	0x03	R/W
0xA3	DCSRCDRP Register	0x28	R/W
0xA5	PD_WDT Register	0x00	R/W
0xA6	PD_DEBUG_KEY Register	0x00	R/W
0xA7	PD_DEBUG_CTRL1 Register	0x10	R/W
0xA8	PD_DEBUG_CTRL2 Register	0x00	R/W

REGISTER MAPS FOR PD PHY (continued)

7-Bit I^2C Slave Device Address: 0b1100 000 + W/R

Bit Types:
R/W: Read/Write bit(s)
R: Read only bit(s)
RC: Bit(s) cleared to 0b0 by being read
R/WC: Read/Write. Writing a 0b1 clears the bit. Writing a 0b0 has no effect.

REG0x00: VENDOR_ID Register [Reset = 0x7E]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	VID[7:0]	0111 1110	R	A unique 16-bit unsigned integer, representing the vender ID. Low byte.	N/A

REG0x01: VENDOR_ID Register [Reset = 0x37]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	VID[15:8]	0011 0111	R	A unique 16-bit unsigned integer, representing the vender ID. High byte.	N/A

REG0x02: PRODUCT_ID Register [Reset = 0x48]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	PID[7:0]	0x48	R	A unique 16-bit unsigned integer. Assigned uniquely by the vendor to identify the TCPC. Low byte.	N/A

REG0x03: PRODUCT_ID Register [Reset = 0x05]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	PID[15:8]	0x05	R	A unique 16-bit unsigned integer. Assigned uniquely by the vendor to identify the TCPC. High byte.	N/A

REG0x04: DEVICE_ID Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	DID[7:0]	0000 0000	R	A unique 16-bit unsigned integer. Assigned by the vendor to identify the version of the SGM41548. Low byte.	N/A

REG0x05: DEVICE_ID Register [Reset = 0x01]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	DID[15:8]	0000 0001	R	A unique 16-bit unsigned integer. Assigned by the vendor to identify the version of the SGM41548. High byte.	N/A

REG0x06: USBTYPEC_REV Register [Reset = 0x23]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	USBTYPEC_REV[7:0]	0010 0011	R	Byte 0 of a 16-bit USB Type-C revision. Revision 2.3.	N/A

REG0x07: USBTYPEC_REV Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	Reserved	0000 0000	R	Reserved Set to 0.	N/A

REGISTER MAPS FOR PD PHY (continued)

REG0x08: USBPD_VER Register [Reset = 0x10]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	USBPD_VER[7:0]	0001 0000	R	Byte 0 of a 16-bit USB PD version. Version 1.0.	N/A

REG0x09: USBPD_REV Register [Reset = 0x32]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	USBPD_REV[7:0]	0011 0010	R	Byte 1 of a 16-bit USB PD revision. Revision 3.2.	N/A

REG0x0A: PDIF_VER Register [Reset = 0x13]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	PDIF_VER[7:0]	0001 0011	R	Byte 0 of a 16-bit PD interface (TCPC) version. Version 1.3.	N/A

REG0x0B: PDIF_REV Register [Reset = 0x20]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	PDIF_REV[7:0]	0010 0000	R	Byte 1 of a 16-bit PD interface (TCPC) revision. Revision 2.0.	N/A

REG0x10: ALERT_L Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	Reserved	0	R	Reserved	N/A
D[6]	TX_SUCCESS	0	R/WC	0 = Cleared (default) 1 = Reset or the SOP* message is successfully transmitted	SOFT_RESET or PD_WDT
D[5]	TX_DISCARD	0	R/WC	0 = Cleared (default) 1 = Reset or SOP* message transmission is not sent due to an incoming receive message	
D[4]	TX_FAIL	0	R/WC	0 = Cleared (default) 1 = The SOP* message is successfully transmitted. No GoodCRC response is received on SOP* message transmission	
D[3]	RX_HARD_RESET	0	R/WC	0 = Cleared (default) 1 = Received Hard Reset message	
D[2]	RX_SOP_MSG_STATUS	0	R/WC	0 = Cleared (default) 1 = Receive buffer registers changed	
D[1]	POWER_STATUS	0	R/WC	0 = Cleared (default) 1 = Power status changed	
D[0]	CC_STATUS	0	R/WC	0 = Cleared (default) 1 = CC status changed The SGM41548 shall not assert this bit when the LOOKING4CONNECTION bit of CC_STATUS register changes state if EN_LOOKING4CON_ALERT bit of TCPC_CONTROL register is set to 0b0.	

REGISTER MAPS FOR PD PHY (continued)

REG0x11: ALERT_H Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	VENDOR_DEFINED_ALERT	0	R/WC	0 = Cleared (default) 1 = Vendor defined event has occurred. Read the SG_INT register (REG0x98) for details interrupts.	SOFT_RESET or PD_WDT
D[6]	Reserved	0	R	Reserved	N/A
D[5]	EXTENDED_STATUS	0	R/WC	0 = Cleared (default) 1 = Extended status changed	SOFT_RESET or PD_WDT
D[4:3]	Reserved	00	R	Reserved	N/A
D[2]	RXBUF_OVFLOW	0	R/WC	0 = SGM41548 Rx buffer is functioning properly (default) 1 = SGM41548 Rx buffer has overflowed	SOFT_RESET or PD_WDT
D[1]	FAULT	0	R/WC	0 = No fault (default) 1 = A fault has occurred. Read the FAULT_STATUS register (REG0x1F)	SOFT_RESET
D[0]	Reserved	0	R	Reserved	N/A

REG0x12: ALERT_L_MASK Register [Reset = 0x7F]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	Reserved	0	R	Reserved	N/A
D[6]	M_TX_SUCCESS	1	R/W	0 = Interrupt masked 1 = Interrupt unmasked (default)	SOFT_RESET or PD_WDT
D[5]	M_TX_DISCARD	1	R/W	0 = Interrupt masked 1 = Interrupt unmasked (default)	SOFT_RESET or PD_WDT
D[4]	M_TX_FAIL	1	R/W	0 = Interrupt masked 1 = Interrupt unmasked (default)	SOFT_RESET or PD_WDT
D[3]	M_RX_HARD_RESET	1	R/W	0 = Interrupt masked 1 = Interrupt unmasked (default)	SOFT_RESET or PD_WDT
D[2]	M_RX_SOP_MSG_STATUS	1	R/W	0 = Interrupt masked 1 = Interrupt unmasked (default)	SOFT_RESET or PD_WDT
D[1]	M_POWER_STATUS	1	R/W	0 = Interrupt masked 1 = Interrupt unmasked (default)	SOFT_RESET or PD_WDT
D[0]	M_CC_STATUS	1	R/W	0 = Interrupt masked 1 = Interrupt unmasked (default)	SOFT_RESET or PD_WDT

REG0x13: ALERT_H_MASK Register [Reset = 0x26]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	M_VENDOR_INT_STATUS	0	R/W	0 = Interrupt masked (default) 1 = Interrupt unmasked	SOFT_RESET or PD_WDT
D[6]	Reserved	0	R	Reserved	N/A
D[5]	M_EXTENDED_STATUS	1	R/W	0 = Interrupt masked 1 = Interrupt unmasked (default)	SOFT_RESET or PD_WDT
D[4:3]	Reserved	00	R	Reserved	N/A
D[2]	M_RXBUF_OVFLOW	1	R/W	0 = Interrupt masked 1 = Interrupt unmasked (default)	SOFT_RESET or PD_WDT
D[1]	M_FAULT	1	R/W	0 = Interrupt masked 1 = Interrupt unmasked (default)	SOFT_RESET or PD_WDT
D[0]	Reserved	0	R	Reserved	N/A

REGISTER MAPS FOR PD PHY (continued)

REG0x14: POWER_STATUS_MASK Register [Reset = 0x4C]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	DBG_ACC_CONNECT_MASK	0	R/W	0 = Interrupt masked (default) 1 = Interrupt unmasked	SOFT_RESET or PD_WDT
D[6]	M_TCPC_INITIAL	1	R/W	0 = Interrupt masked 1 = Interrupt unmasked (default)	SOFT_RESET or PD_WDT
D[5:4]	Reserved	00	R	Reserved	N/A
D[3]	M_VBUS_PRESENT_DETC	1	R/W	0 = Interrupt masked 1 = Interrupt unmasked (default)	SOFT_RESET or PD_WDT
D[2]	M_VBUS_PRESENT	1	R/W	0 = Interrupt masked 1 = Interrupt unmasked (default)	SOFT_RESET or PD_WDT
D[1:0]	Reserved	00	R	Reserved	N/A

REG0x15: FAULT_STATUS_MASK Register [Reset = 0x01]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	M_ALL_REGISTERS_RESET	0	R/W	0 = Interrupt masked (default) 1 = Interrupt unmasked	SOFT_RESET or PD_WDT
D[6:1]	Reserved	00 0000	R	Reserved	N/A
D[0]	M_I2C_ERROR	1	R/W	0 = Interrupt masked 1 = Interrupt unmasked (default)	SOFT_RESET or PD_WDT

REG0x16: EXTENDED_STATUS_MASK Register [Reset = 0x01]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:1]	Reserved	000 0000	R	Reserved	N/A
D[0]	M_VSAFE_0V	1	R/W	0 = Interrupt masked 1 = Interrupt unmasked (default)	SOFT_RESET or PD_WDT

REGISTER MAPS FOR PD PHY (continued)

REG0x19: TCPC_CONTROL Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	Reserved	0	R	Reserved	N/A
D[6]	EN_LOOKING4CON_ALERT	0	R/W	0 = Disable the CC_STATUS bit assertion of ALERT_L register when the LOOKING4CONNECTION bit of CC_STATUS register changes (default) 1 = Enable the CC_STATUS bit assertion of ALERT_L register when the LOOKING4CONNECTION bit of CC_STATUS register changes	SOFT_RESET or PD_WDT
D[5:2]	Reserved	0000	R	Reserved	N/A
D[1]	BIST_TEST_MODE	0	R/W	0 = Normal operation. RECEIVE_DETECT-enabled messages passed to TCPM via alert (default) 1 = BIST test mode. RECEIVE_DETECT-triggered messages generate GoodCRC response but may not reach TCPM via alert	SOFT_RESET or PD_WDT
D[0]	PLUG_ORIENT	0	R/W	0 = If PD messaging is enabled, monitor the CC1 pin for BMC communications (default) 1 = If PD messaging is enabled, monitor the CC2 pin for BMC communications	SOFT_RESET or PD_WDT

REG0x1A: ROLE_CONTROL Register [Reset = 0x0A]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	Reserved	0	R	Reserved	N/A
D[6]	EN_DRP	0	R/W	0 = No DRP. Bits[3:0] determine the settings of Rp, Rd and Ra (default) 1 = DRP	SOFT_RESET or PD_WDT
D[5:4]	RP_VALUE[1:0]	00	R/W	00 = Rp (default) 01 = Rp 1.5A 10 = Rp 3.0A 11 = Reserved	SOFT_RESET or PD_WDT
D[3:2]	CC2[1:0]	10	R/W	00 = Ra 01 = Rp (use Rp definition in RP_VALUE[1:0] register) 10 = Rd (default) 11 = Open (disconnect or don not care)	SOFT_RESET or PD_WDT
D[1:0]	CC1[1:0]	10	R/W	00 = Ra 01 = Rp (use Rp definition in RP_VALUE[1:0] register) 10 = Rd (default) 11 = Open (disconnect or don not care)	SOFT_RESET or PD_WDT

REGISTER MAPS FOR PD PHY (continued)

REG0x1D: CC_STATUS Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:6]	Reserved	00	R	Reserved	N/A
D[5]	LOOKING4CONNECTION	0	R	0 = TCPC is not actively looking for a connection. A transition from '1' to '0' indicates a potential connection has been found (default) 1 = TCPC is looking for a connection (toggling as a DRP or looking for a connection as sink/source only condition)	N/A
D[4]	CONNECT_RESULT	0	R	0 = SGM41548 is presenting Rp (default) 1 = SGM41548 is presenting Rd	N/A
D[3:2]	CC2_STATUS[1:0]	00	R	If the CC2[1:0] bits of the ROLE_CONTROL register are Rp or the CONNECT_RESULT bit is 0b0: 00 = SRC.Open (open, Rp) (default) 01 = SRC.Ra (below maximum vRa) 10 = SRC.Rd (within the vRd range) 11 = Reserved If the CC2[1:0] bits of the ROLE_CONTROL register are Rd or the CONNECT_RESULT bit is 0b1: 00 = SNK.Open (below maximum vRa) (default) 01 = SNK.Default (above minimum vRd-Connect) 10 = SNK.Power1.5 (above minimum vRd-Connect) detects Rp 1.5A 11 = SNK.Power3.0 (above minimum vRd-Connect) detects Rp 3.0A If the CC2[1:0] bits of the ROLE_CONTROL register are Ra, this field is set to 0b00. If the CC2[1:0] bits of the ROLE_CONTROL register are Open, this field is set to 0b00. This field always returns 0b00 if LOOKING4CONNECTION = 1. Otherwise, the returned value depends on CC2[1:0] bits of the ROLE_CONTROL register.	N/A
D[1:0]	CC1_STATUS[1:0]	00	R	If the CC1[1:0] bits of the ROLE_CONTROL register are Rp or CONNECT_RESULT bit is 0b0: 00 = SRC.Open (open, Rp) (default) 01 = SRC.Ra (below maximum vRa) 10 = SRC.Rd (within the vRd range) 11 = Reserved If the CC1[1:0] bits of the ROLE_CONTROL register are Rd or the CONNECT_RESULT bit is 0b1: 00 = SNK.Open (below maximum vRa) (default) 01 = SNK.Default (above minimum vRd-Connect) 10 = SNK.Power1.5 (above minimum vRd-Connect) detects Rp 1.5A 11 = SNK.Power3.0 (above minimum vRd-Connect) detects Rp 3.0A If the CC1[1:0] bits of the ROLE_CONTROL register are Ra, this field is set to 0b00. If the CC1[1:0] bits of the ROLE_CONTROL register are Open, this field is set to 0b00. This field always returns 0b00 if LOOKING4CONNECTION = 1. Otherwise, the returned value depends on CC1[1:0] bits of the ROLE_CONTROL register.	N/A

REGISTER MAPS FOR PD PHY (continued)

REG0x1E: POWER_STATUS Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	DBG_ACC_CONNECT	0	R	0 = No debug accessory connected (default) 1 = Debug accessory connected	N/A
D[6]	TCPC_INITIAL	0	R	0 = SGM41548 initialization complete. All registers are valid (default) 1 = SGM41548 is still undergoing internal initialization. Note: this interrupt take effect only when exit the shutdown mode.	N/A
D[5:4]	Reserved	00	R	Reserved	N/A
D[3]	EN_VBUS_DET	0	R	0 = VBUS vSafe0V detection disabled (default) 1 = VBUS vSafe0V detection enabled Note: this bit is initialized to 0b1 when exit the shutdown mode.	N/A
D[2]	VBUS_PRESENT	0	R	0 = VBUS disconnected (default) 1 = VBUS connected The SGM41548 will report VBUS present if it detects VBUS is higher than $V_{VBUS\_PRESENT}$ (3.55V TYP). The SGM41548 will report VBUS is not present if it detects VBUS is lower than $V_{VBUS\_PRESENT\_FALL}$ (3.15V TYP). The SGM41548 may report VBUS is not present if VBUS is between 3.15V and 3.55V.	N/A
D[1:0]	Reserved	00	R	Reserved	N/A

REG0x1F: FAULT_STATUS Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	ALL_REGISTERS_RESET	0	R/WC	This bit is asserted when the SGM41548 resets all registers to their default values. This happens at initial power-up or if an unexpected power reset occurs.	SOFT_RESET
D[6:1]	Reserved	00 0000	R	Reserved	N/A
D[0]	I2C_ERROR	0	R/WC	0 = No error (default) 1 = I^2C error has occurred	SOFT_RESET

REG0x20: EXTENDED_STATUS Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:1]	Reserved	000 0000	R	Reserved	N/A
D[0]	VSAFE_0V	0	R	0 = VBUS is not at vSafe0V (default) 1 = VBUS is at vSafe0V The SGM41548 reports that VBUS is at vSafe0V when SGM41548 detects that VBUS is below 0.8V.	N/A

REG0x23: COMMAND Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	COMMAND[7:0]	0000 0000	R/WC	00100010 = DisableVbusDetect Disable VBUS present and vSafe0V detection. 00110011 = EnableVbusDetect Enable VBUS present and vSafe0V detection. 10011001 = Look4Connection Start DRP toggling if the EN_DRP bit of the ROLE_CONTROL register is 0b1. If the CC1[1:0]/ CC2[1:0] bits of the ROLE_CONTROL register are 0b01, start with Rp, if the CC1[1:0]/CC2[1:0] bits of the ROLE_CONTROL register are 0b10, start with Rd.	SOFT_RESET or PD_WDT

REGISTER MAPS FOR PD PHY (continued)

REG0x24: DEVICE_CAPABILITIES_1L Register [Reset = 0xD0]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:5]	ROLES_SUPPORT[2:0]	110	R	000 = Type-C port manager can configure the port as source only or sink only (not DRP) 001 = Source only 010 = Sink only 011 = Sink with accessory support (optional) 100 = DRP only 101 = Source, sink, DRP, adapter/cable all supported 110 = Source, sink, DRP (default) 111 = Not valid	N/A
D[4]	ALL_SOP_SUPPORT	1	R	0 = All SOP* messages except SOP'_DBG/ SOP"_DBG 1 = All SOP* messages are supported (default) Configured in the RECEIVE_DETECT and TX_BUF_FRAME_TYPE registers.	N/A
D[3]	Reserved	0	R	Reserved	N/A
D[2]	CPB_SINK_VBUS	0	R	0 = SGM41548 cannot control the sink path to the system load (default) 1 = SGM41548 can control the sink path to the system load	N/A
D[1]	SOURCE_HV_VBUS	0	R	0 = SGM41548 cannot control the source high voltage path to VBUS (default) 1 = SGM41548 can control the source high voltage path to VBUS	N/A
D[0]	SOURCE_VBUS	0	R	0 = SGM41548 cannot control the source path to VBUS (default) 1 = SGM41548 can control the source path to VBUS	N/A

REG0x25: DEVICE_CAPABILITIES_1H Register [Reset = 0x02]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	VBUS_NONDEFAULT_TARGET	0	R	0 = VBUS_NONDEFAULT_TARGET register not implemented (default) 1 = VBUS_NONDEFAULT_TARGET register implemented	N/A
D[6]	CPB_VBUS_OC	0	R	0 = VBUS OCP is not reported by the SGM41548 (default) 1 = VBUS OCP is reported by the SGM41548	N/A
D[5]	CPB_VBUS_OV	0	R	0 = VBUS OVP is not reported by the SGM41548 (default) 1 = VBUS OVP is reported by the SGM41548	N/A
D[4]	CPB_BLEED_DISC	0	R	0 = No bleed discharge implemented in SGM41548 (default) 1 = Bleed discharge is implemented in the SGM41548	N/A
D[3]	CPB_FORCE_DISC	0	R	0 = No force discharge implemented in SGM41548 (default) 1 = Force discharge is implemented in the SGM41548	N/A
D[2]	VBUS_MEASURE_ALARM	0	R	0 = No VBUS voltage measurement nor VBUS alarms (default) 1 = VBUS voltage measurement and VBUS alarms	N/A
D[1:0]	SOURCE_RP_SUPPORT[1:0]	10	R	00 = Rp default only 01 = Rp 1.5A and default 10 = Rp 3.0A, 1.5A, and default (default) 11 = Reserved Rp values which can be programmed by the TCPM through the ROLE_CONTROL register.	N/A

REGISTER MAPS FOR PD PHY (continued)

REG0x26: DEVICE_CAPABILITIES_2L Register [Reset = 0x3E]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	SINK_DISCONNECT_DET	0	R	0 = VBUS_SINK_DISCONNECT_THRESHOLD not implemented (default = use VBUS_PRESENT bit of POWER_STATUS register is 0b0 to indicate a sink disconnect) (default) 1 = VBUS_SINK_DISCONNECT_THRESHOLD is implemented	N/A
D[6]	STOP_DISC_THD	0	R	0 = VBUS_STOP_DISCHARGE_THRESHOLD is not implemented (default) 1 = VBUS_STOP_DISCHARGE_THRESHOLD is implemented	N/A
D[5:4]	VBUS_VOL_ALARM_LSB[1:0]	11	R	11 = Not support this function	N/A
D[3:1]	VCONN_POWER[2:0]	111	R	000 = 1.0W 001 = 1.5W 010 = 2.0W 011 = 3W 100 = 4W 101 = 5W 110 = 6W 111 = External (default)	N/A
D[0]	VCONN_OCF	0	R	0 = SGM41548 is not capable of detecting a VCONN fault (default) 1 = SGM41548 is capable of detecting a VCONN fault	N/A

REG0x27: DEVICE_CAPABILITIES_2H Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	DEVICE_CAPABILITIES_3_SUPPORT	0	R	0 = TCPC does not support the DEVICE_CAPABILITIES_3_SUPPORT register (default) 1 = TCPC supports the DEVICE_CAPABILITIES_3_SUPPORT register	N/A
D[6]	Reserved	0	R	Reserved	N/A
D[5]	GENERIC_TIMER	0	R	0 = GENERIC_TIMER register is not supported (default) 1 = GENERIC_TIMER register is supported	N/A
D[4]	LONG_MSG	0	R	0 = TCPC only supports 30 bytes content of the SOP* message. The value in RX_BYTE_COUNT shall be less than or equal to 31. The value in TX_BYTE_COUNT shall be less than or equal to 30 (default) 1 = TCPC is capable of supporting 264 bytes content of the SOP* message. The TX_BUF holds up to 264 bytes content of the SOP* message. The value supported in TX_BYTE_COUNT shall be up to 132. RX_BUF holds up to 264 bytes content SOP* message plus a 30 bytes content SOP* message	N/A
D[3]	Reserved	0	R	Reserved	N/A
D[2]	SOURCE_FR_SWAP	0	R	0 = Not capable of sending fast role swap signal as source when receiving SendFRSwapSignal command or receiving standard input source fast role swap low (default) 1 = Capable of sending fast role swap signal as source TCPC when receiving SendFRSwapSignal command. If SOURCE_FR_SWAP[1:0] = 10 in the STANDARD_INPUT_CAPABILITIES register, capable of sending fast role swap signal as source when standard input source fast role swap is set low	N/A
D[1:0]	Reserved	00	R	Reserved	N/A

REGISTER MAPS FOR PD PHY (continued)

REG0x28: STANDARD_INPUT_CAPABILITIES Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:5]	Reserved	000	R	Reserved	N/A
D[4:3]	SOURCE_FR_SWAP[1:0]	00	R	00 = Not present in TCPC (default) 01 = Present in TCPC as an input only pin 10 = Present in TCPC as a bidirectional pin, sharing with the STANDARD OUTPUT SIGNAL VBUS Sink Disconnect Detect Indicator. The VBUS_SINK_DISCONNECT_DET_IND bit in the STANDARD_ OUTPUT_CAPABILITIES register shall also be set to 0b1 11 = Reserved	N/A
D[2]	VBUS_EXT_OVP	0	R	VBUS External Over-Voltage Fault 0 = Not present in TCPC (default) 1 = Present in TCPC	N/A
D[1]	VBUS_EXT_OCP	0	R	VBUS External Over-Current Fault 0 = Not present in TCPC (default) 1 = Present in TCPC	N/A
D[0]	FORCE_OFF_VBUS	0	R	Force Off VBUS (Source or Sink) 0 = Not present in TCPC (default) 1 = Present in TCPC	N/A

REG0x29: STANDARD_OUTPUT_CAPABILITIES Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	VBUS_SINK_DISCONNECT_DET_IND	0	R	Sink Disconnect Detection Indicator 0 = Not present in TCPC (default) 1 = Present in TCPC Shall present in TCPC if the SOURCE_FR_SWAP[1:0] bits in the STANDARD_INPUT_CAPABILITIES register are set to 0b10 (present as a bidirectional pin).	N/A
D[6]	CPB_DBG_ACC_IND	0	R	Debug Accessory Indicator 0 = Not present in TCPC (default) 1 = Present in TCPC	N/A
D[5]	CPB_VBUS_PRESENT_MNT	0	R	VBUS Present Monitor 0 = Not present in TCPC (default) 1 = Present in TCPC	N/A
D[4]	CPB_AUDIO_ADT_ACC_IND	0	R	Audio Adapter Accessory Indicator 0 = Not present in TCPC (default) 1 = Present in TCPC	N/A
D[3]	CPB_ACTIVE_CABLE_IND	0	R	Active Cable Indicator 0 = Not present in TCPC (default) 1 = Present in TCPC	N/A
D[2]	CPB_MUX_CFG_CTRL	0	R	MUX Configuration Control 0 = Not present in TCPC (default) 1 = Present in TCPC	N/A
D[1]	CPB_CONNECT_PRESENT	0	R	Connection Present 0 = No Connection (default) 1 = Connection Controlled by the TCPM.	N/A
D[0]	CPB_CONNECT_ORIENT	0	R	Connector Orientation 0 = Not present in TCPC (default) 1 = Present in TCPC	N/A

REGISTER MAPS FOR PD PHY (continued)

REG0x2E: MESSAGE_HEADER_INFO Register [Reset = 0x02]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:5]	Reserved	000	R	Reserved	N/A
D[4]	CABLE_PLUG	0	R/W	0 = Message originated from source, sink, or DRP (default) 1 = Message originated from a cable plug	SOFT_RESET or PD_WDT
D[3]	DATA_ROLE	0	R/W	0 = UFP (default) 1 = DFP	SOFT_RESET or PD_WDT
D[2:1]	USBPD_SPECREV[1:0]	01	R/W	00 = Revision 1.0 01 = Revision 2.0 (default) 10 = Revision 3.0 11 = Reserved	SOFT_RESET or PD_WDT
D[0]	POWER_ROLE	0	R/W	0 = Sink (default) 1 = Source	SOFT_RESET or PD_WDT

REG0x2F: RECEIVE_DETECT Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	Reserved	0	R	Reserved	N/A
D[6]	EN_CABLE_RST	0	R/W	0 = SGM41548 does not detect cable reset signaling (default) 1 = SGM41548 detects cable reset signaling	SOFT_RESET or PD_WDT
D[5]	EN_HARD_RST	0	R/W	0 = SGM41548 does not detect hard reset signaling (default) 1 = SGM41548 detects hard reset signaling	SOFT_RESET or PD_WDT
D[4]	EN_SOP2DB	0	R/W	0 = SGM41548 does not detect SOP_DBG" message (default) 1 = SGM41548 detects SOP_DBG" message	SOFT_RESET or PD_WDT
D[3]	EN_SOP1DB	0	R/W	0 = SGM41548 does not detect SOP_DBG' message (default) 1 = SGM41548 detects SOP_DBG' message	SOFT_RESET or PD_WDT
D[2]	EN_SOP2	0	R/W	0 = SGM41548 does not detect SOP" message (default) 1 = SGM41548 detects SOP" message	SOFT_RESET or PD_WDT
D[1]	EN_SOP1	0	R/W	0 = SGM41548 does not detect SOP' message (default) 1 = SGM41548 detects SOP' message	SOFT_RESET or PD_WDT
D[0]	EN_SOP	0	R/W	0 = SGM41548 does not detect SOP message (default) 1 = SGM41548 detects SOP message	SOFT_RESET or PD_WDT

REGISTER MAPS FOR PD PHY (continued)

REG0x30: RX_BYTE_COUNT Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	RX_BYTE_COUNT	0000 0000	R	Indicate number of bytes in this register that are not stale. The TCPM should read the first RECEIVE_BYTE_COUNT bytes in this register. This is the number counts form the RX_BUF_FRAME_TYPE register to the RX_BUF register stored the last data byte.	SOFT_RESET or PD_WDT

REG0x31: RX_BUF_FRAME_TYPE Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:3]	Reserved	0000	R	Reserved	N/A
D[2:0]	RX_FRAME_TYPE[2:0]	000	R	Type of Received Frame 000 = Received SOP (default) 001 = Received SOP' 010 = Received SOP'' 011 = Received SOP_DBG' 100 = Received SOP_DBG'' 110 = Received cable reset all others are reserved	SOFT_RESET or PD_WDT

REG0x32: RX_BUF_HEADER_BYTE_0 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	RX_HEAD_0[7:0]	0000 0000	R	Byte 0 (Bits[7:0]) of Message Header	SOFT_RESET or PD_WDT

REG0x33: RX_BUF_HEADER_BYTE_1 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	RX_HEAD_1[7:0]	0000 0000	R	Byte 1 (Bits[15:8]) of Message Header	SOFT_RESET or PD_WDT

REG0x34 ~ REG0x4F: RX_BUF_OBJx(1 ~ 7)_BYTE_x(0 ~ 3) Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	RX_OBJx_BYTE_x[7:0]	0000 0000	R	Byte x(0 ~ 3) of Data Object x(1 ~ 7) of Receive Buffer	SOFT_RESET or PD_WDT

REG0x50: TX_BUF_FRAME_TYPE Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:6]	Reserved	00	R	Reserved	N/A
D[5:4]	TX_RETRY_CNT[1:0]	00	R/W	00 = No message retry is required (default) 01 = Automatically retry message transmission once 10 = Automatically retry message transmission twice 11 = Automatically retry message transmission three times	SOFT_RESET or PD_WDT
D[3]	Reserved	0	R	Reserved	N/A
D[2:0]	TX_FRAME_TYPE[2:0]	000	R/W	000 = Transmit SOP (default) 001 = Transmit SOP' 010 = Transmit SOP'' 011 = Transmit SOP_DBG' 100 = Transmit SOP_DBG'' 101 = Transmit hard reset 110 = Transmit cable reset 111 = Transmit BIST carrier mode 2 (SGM41548 shall exit the BIST mode no later than $t_{BISTContMode}$ max)	SOFT_RESET or PD_WDT

REGISTER MAPS FOR PD PHY (continued)

REG0x51: TX_BYTE_COUNT Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	TX_BYTE_COUNT[7:0]	0000 0000	R/W	The number of bytes the TCPM will write.	SOFT_RESET or PD_WDT

REG0x52: TX_BUF_HEADER_BYTE_0 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	TX_HEAD_0[7:0]	0000 0000	R/W	Byte 0 (Bits[7:0]) of Message Header	SOFT_RESET or PD_WDT

REG0x53: TX_BUF_HEADER_BYTE_1 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	TX_HEAD_1[7:0]	0000 0000	R/W	Byte 1 (Bits[15:8]) of Message Header	SOFT_RESET or PD_WDT

REG0x54 ~ REG0x6F: TX_BUF_OBJx(1 ~ 7)_BYTE_x(0 ~ 3) Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	TX_OBJx_BYTE_x[7:0]	0000 0000	R/W	Byte x(0 ~ 3) of Data Object x(1 ~ 7) of Transmit Buffer	SOFT_RESET or PD_WDT

REG0x97: VENDOR_DEFINED_STATUS Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:5]	Reserved	000	R	Reserved	N/A
D[4]	TDIE_OTP_STATUS	0	R	0 = Not in TDIE OTP status (default) 1 = In TDIE OTP status	N/A
D[3]	Reserved	0	R	Reserved	N/A
D[2]	CC_OVP_STATUS	0	R	0 = CC is not in OVP status (default) 1 = CC is in OVP status	N/A
D[1]	VSAFE0V_STATUS	0	R	0 = VBUS is not at vSafe0V (default) 1 = VBUS is at vSafe0V	N/A
D[0]	Reserved	0	R	Reserved	N/A

REG0x98: SG_INT Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:6]	Reserved	00	R	Reserved	N/A
D[5]	INT_RA_DETACH	0	R/WC	0 = No Ra detach event (default) 1 = Ra detach event occurs	SOFT_RESET or PD_WDT
D[4]	INT_TDIE_OTP	0	R/WC	0 = No TDIE OTP event (default) 1 = TDIE OTP event occurs	SOFT_RESET or PD_WDT
D[3]	Reserved	0	R	Reserved	N/A
D[2]	CC_OVP	0	R/WC	0 = No CC OVP event (default) 1 = CC OVP event occurs	SOFT_RESET or PD_WDT
D[1]	INT_VSAFE0V_STATUS	0	R/WC	0 = No VBUS vSafe0V event (default) 1 = VBUS vSafe0V event occurs	SOFT_RESET or PD_WDT
D[0]	Reserved	0	R	Reserved	N/A

REGISTER MAPS FOR PD PHY (continued)

REG0x99: VENDOR_DEFINED_ALERT_MASK Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:6]	Reserved	00	R	Reserved	N/A
D[5]	M_RA_DETACH	0	R/W	0 = Interrupt masked (default) 1 = Interrupt unmasked	SOFT_RESET or PD_WDT
D[4]	M_TDIE_OTP	0	R/W	0 = Interrupt masked (default) 1 = Interrupt unmasked	SOFT_RESET or PD_WDT
D[3]	Reserved	0	R	Reserved	N/A
D[2]	M_CC_OVP	0	R/W	0 = Interrupt masked (default) 1 = Interrupt unmasked	SOFT_RESET or PD_WDT
D[1]	M_VSAFE0V	0	R/W	0 = Interrupt masked (default) 1 = Interrupt unmasked	SOFT_RESET or PD_WDT
D[0]	Reserved	0	R	Reserved	N/A

REG0x9B: SG_SHUTDOWN Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:6]	Reserved	00	R	Reserved	N/A
D[5]	SHUTDOWN_OFF	0	R/W	0 = Shutdown mode (default) 1 = Non-shutdown mode	SOFT_RESET or PD_WDT
D[4:0]	Reserved	0 0000	R	Reserved	N/A

REG0xA0: RESET_CTRL Register [Reset = 0x30]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:6]	Reserved	00	R	Reserved	N/A
D[5]	CABLE_RESET_CTRL	1	R/W	0 = Not clear RECEIVE_DETECT register when cable reset received 1 = Clear RECEIVE_DETECT register when cable reset received (default)	SOFT_RESET or PD_WDT
D[4]	HARD_RESET_CTRL	1	R/W	0 = Not clear ALERT_MASK registers when hard reset happens 1 = Clear ALERT_MASK when hard reset happens (default)	SOFT_RESET or PD_WDT
D[3:1]	Reserved	000	R	Reserved	N/A
D[0]	SOFT_RESET	0	R/WC	Write 0b1 to trigger soft-reset. All registers will be reset to the default value. Clear after soft reset completed.	SOFT_RESET or PD_WDT

REG0xA2: TDRP Register [Reset = 0x03]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:4]	Reserved	0000	R	Reserved	N/A
D[3:0]	TDRP[3:0]	0011	R/W	The period of DRP advertisement. (Period = TDRP × 6.4 + 51.2ms) 0000 = 51.2ms 0001 = 57.6ms 0010 = 64ms 0011 = 70.4ms (default) … 1110 = 140.8ms 1111 = 147.2ms	SOFT_RESET or PD_WDT

REGISTER MAPS FOR PD PHY (continued)

REG0xA3: DCSRCDRP Register [Reset = 0x28]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	Reserved	0	R	Reserved	N/A
D[6:0]	DCSRCDRP[6:0]	010 1000	R/W	The duty of time when DRP advertises source. DUTY = (DCSRCDRP[6:0] + 1)/128 Default: 41/128	SOFT_RESET or PD_WDT

REG0xA5: PD_WDT Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:3]	Reserved	0 0000	R	Reserved	N/A
D[2:0]	PD_WDT[2:0]	000	R/W	PD Watchdog Timer Setting Bits 000 = Disable watchdog (default) 001 = 0.625s 010 = 1.25s 011 = 2.5s 100 ~ 111 = 5s Any I^2C operation will reset the PD watchdog.	SOFT_RESET or PD_WDT

REG0xA6: PD_DEBUG_KEY Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	PD_DEBUG_KEY[7:0]	0000 0000	R/W	Key to Enable/Disable the Write Right for REG0xA7 and REG0xA8 0x00 = Disable (default) 0x5A = Enable Others = Disable	SOFT_RESET

REG0xA7: PD_DEBUG_CTRL1 Register [Reset = 0x10]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:6]	RTX_SEL[1:0]	00	R/W	CC Transmitter Output Resistor 00 = 20Ω (default) 01 = 28Ω 10 = 40.7Ω 11 = 58Ω	SOFT_RESET
D[5:4]	VSLEW[1:0]	01	R/W	CC Transmitter Output Rising/Falling Time 00 = 350ns 01 = 440ns (default) 10 = 440ns 11 = 550ns	SOFT_RESET
D[3:0]	VPD_RDAC[3:0]	0000	R/W	CC Transmitter Output High Voltage Offset Setting 0000 = 0mV (default) 0001 = +12.5mV 0010 = +25mV 0011 = +37.5mV 0100 = +50mV 0101 = +62.5mV 0110 = +75mV 0111 = +87.5mV 1000 = +12.5mV 1001 = 0mV 1010 = -12.5mV 1011 = -25mV 1100 = -37.5mV 1101 = -50mV 1110 = -62.5mV 1111 = -75mV	SOFT_RESET

REGISTER MAPS FOR PD PHY (continued)

REG0xA8: PD_DEBUG_CTRL2 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:3]	Reserved	0 0000	R/W	Reserved	SOFT_RESET
D[2]	CC_FILTER_SEL	0	R/W	CC Receiver RC Filter Selection 0 = 30kΩ & 10pF (default) 1 = 15kΩ & 10pF	SOFT_RESET
D[1]	VREF_COUPLE_SEL	0	R/W	CC Receiver V_{IH} and V_{IL} Threshold Setting, only Take Effect When the NO_COUPLE Bit = 0 0 = 1.125V and 0.875V (default) 1 = 1.0625V and 0.9375V	SOFT_RESET
D[0]	NO_COUPLE	0	R/W	The Method of CC Voltage Sense for the Receiver 0 = Capacitance coupling (default) 1 = Comparator direct comparisons	SOFT_RESET

APPLICATION INFORMATION

The SGM41548 is typically used as a charger with power path management in smart phones, tablets and other portable devices. In the design, it comes along with a host controller (a processor with I^2C interface) and a single-cell Li-Ion or Li-polymer battery.

Detailed Design Procedure

Inductor Design

Small energy storage elements (inductor and capacitor) can be used since the high frequency (1.5MHz) switching converter is used in the SGM41548. Inductor should tolerate current which is higher than the maximum charge current (I_{CHG}) plus half the inductor peak to peak ripple current (ΔI) without saturation:

$$I_{SAT} > I_{CHG} + \frac{\Delta I}{2} \quad (3)$$

The inductor ripple current is determined by the input voltage (V_{VBUS}), duty cycle ($D = V_{BAT}/V_{VBUS}$), switching frequency (f_S = 1.5MHz) and the inductance (L). In CCM:

$$\Delta I = \frac{V_{VBUS} \times D \times (1-D)}{f_S \times L} \quad (4)$$

Inductor ripple current is maximum when D ≈ 0.5. If the input voltage range (V_{VBUS}) is limited higher, D values can be considered.

In the practical designs, inductor peak to peak current ripple is selected in a range from 20% to 40% of the maximum DC current $\Delta I = (0.2 \sim 0.4) \times I_{CHG}$ for a good trade-off between inductor size and efficiency. Selecting the higher ripple allows choosing of smaller inductance.

For each application, V_{VBUS} and I_{CHG} are known, so L can be calculated from (4) and current rating of the inductor can be selected from (3). Choose an inductor that has small DCR and core losses at 1.5MHz to have high efficiency and cool operation at full load.

Input Capacitor Design

Select low ESR ceramic input capacitor (X7R or X5R) with sufficient voltage and RMS ripple current rating for decoupling of the input switching ripple current (I_{CIN}). The RMS ripple current in the worst case is around the $I_{CHG}/2$ when D ≈ 0.5. If the converter does not operate at D ≈ 50%, in the worst case, the capacitor RMS current can be estimated from (5) in which D is the closest operating duty cycle to 0.5.

$$I_{CIN} = I_{CHG} \times \sqrt{D \times (1-D)} \quad (5)$$

For SGM41548, place C_{IN} across PMID and GND pins close to the chip. Voltage rating of the capacitor must be at least 25% higher than the normal input voltage to minimize voltage derating. A rating of 25V or higher is preferred for a 15V input voltage. For a 13.5V input voltage, the preferred rating is 25V or higher.

A C_{IN} = 22μF is suggested.

Output Capacitor Design

The output capacitance (on the system) must have enough RMS (ripple) current rating to carry the inductor switching ripple and provide enough energy for system transient current demands. I_{COUT} (C_{OUT} RMS current) can be calculated by:

$$I_{COUT} = \frac{I_{RIPPLE}}{2 \times \sqrt{3}} \approx 0.29 \times I_{RIPPLE} \quad (6)$$

And the output voltage ripple can be calculated by:

$$\Delta V_O = \frac{V_{OUT}}{8LC_{OUT}f_S^2}\left(1 - \frac{V_{OUT}}{V_{VBUS}}\right) \quad (7)$$

Increasing L or C_{OUT} (the LC filter) can reduce the ripple.

The internal loop compensation of the device is optimized for > 22μF ceramic output capacitor. 10V, X7R (or X5R) ceramic capacitors are recommended for the output.

Input Power Supply Considerations

To power the system from the SGM41548, either an input power source with a voltage range from 3.9V to 13.5V and at least 100mA current rating should power VBUS, or a single-cell Li-Ion battery with voltage higher than V_{BAT_UVLOZ} should be connected to BAT pin of the device. The input source must have enough current rating to allow maximum power delivery through charger (Buck converter) to the system.

APPLICATION INFORMATION (continued)

Layout Guidelines

The switching node (SW) creates very high frequency noises, which are several times higher than f_{SW} (1.5MHz) due to sharp rise and fall of the voltage and current in the switches. To reduce the ringing issues and noise generation, it is important to design a proper layout for minimizing the current path impedance and loop area. The reference layout is shown in Figure 20. The following considerations can help to make a better layout.

1. Place the input capacitor between PMID and GND pins as close as possible to the chip with the shortest copper connections (avoid vias). Choose the smallest capacitor size.

2. Connect one pin of the inductor as close as possible to the SW pin of the device and minimize the copper area connected to the SW node to reduce capacitive coupling from SW area to nearby signal traces. This decreases the noise induced through parasitic stray capacitances and displacement currents to other conductors. SW connection should be wide enough to carry the charging current. Keep other signals and traces away from SW if possible.

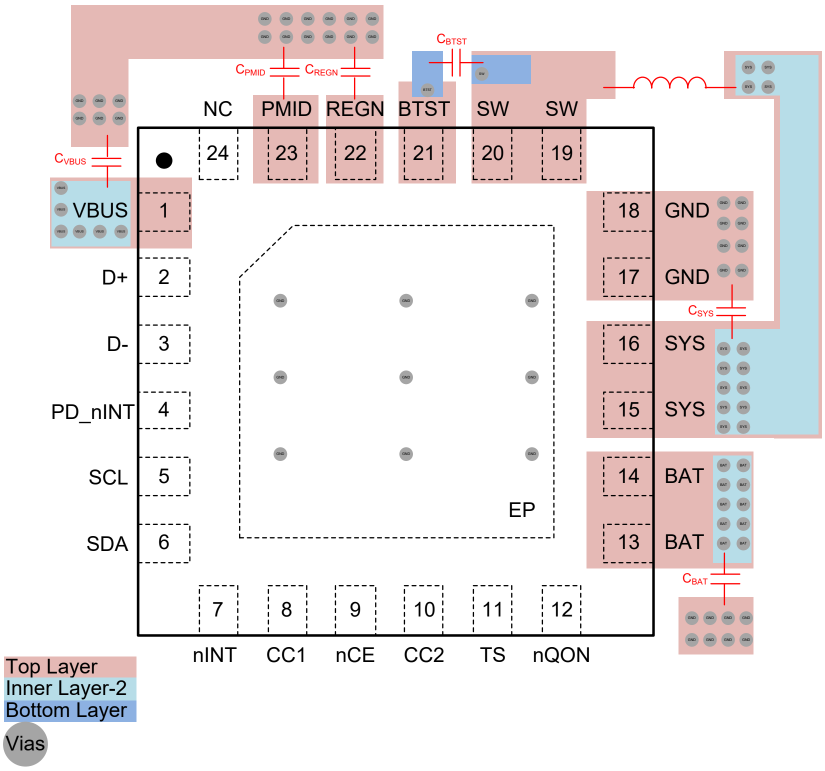
3. Place output capacitor GND pin as close as possible to the GND pin of the device and the GND pin of input capacitor C_{IN}. It is better to avoid using vias for these connections and keep the high frequency current paths short enough and on the same layer. A GND copper layer under the component layer helps to reduce noise emissions. Note that the DC current and AC current paths are in the layout and keep them short and decoupled as much as possible.

4. For analog signals, it is better to use a separate analog ground (AGND) branched only at one point from GND pin. To avoid high current flow through the AGND path, it should be connected to GND only at one point (preferably the GND pin).

5. Place decoupling capacitors close to the IC pins with the shortest copper connections.

6. Solder the exposed thermal pad of the package to the PCB ground planes. Ensure that there are enough thermal vias directly under the IC, connecting to the ground plane on the other layers for better heat dissipation and cooling of the device.

7. Select proper sizes for the vias and ensure that enough copper is available to carry the current for the given current path. Vias usually have some considerable parasitic inductance and resistance.



NOTES:
1. The layout example is actually a board with 4 layers. The inner layer-1 is a GND copper layer and not shown in the figure.
2. Only the critical circuit path layout is shown for reference, and other heat dissipation planes and vias are not shown in the figure. For more detailed information, please refer to the SGM41548 evaluation kit on www.sg-micro.com.

Figure 20. Reference Layout

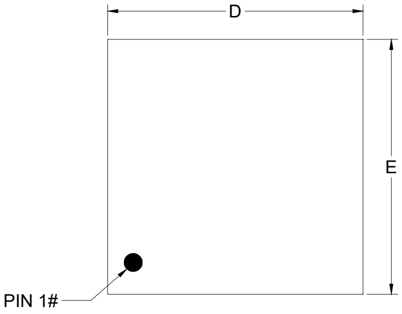
REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

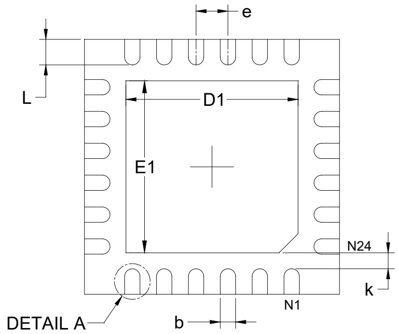
Changes from Original to REV.A (MAY 2026)	**Page**
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

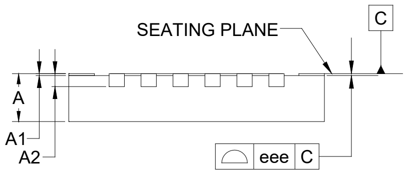
TQFN-4×4-24L



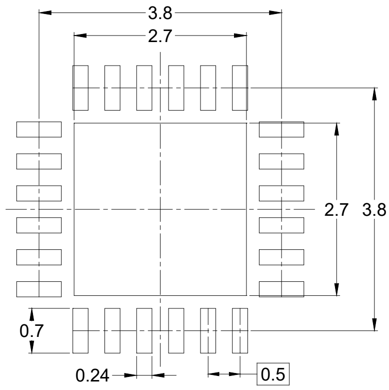
TOP VIEW



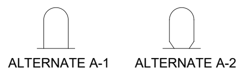
BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN (Unit: mm)



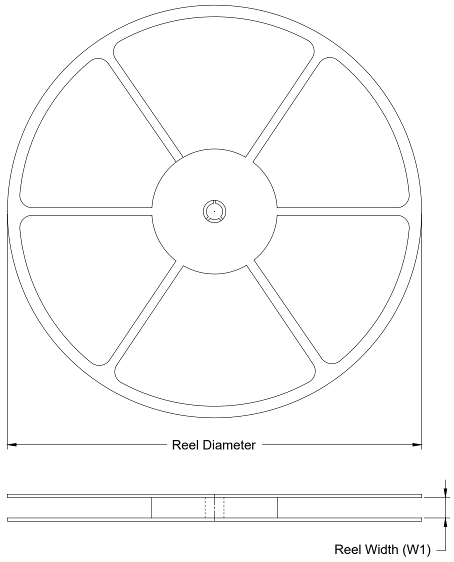
DETAIL A
ALTERNATE TERMINAL
CONSTRUCTION

Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	0.700	-	0.800
A1	0.000	-	0.050
A2	0.203 REF		
b	0.180	-	0.300
D	3.900	-	4.100
E	3.900	-	4.100
D1	2.600	-	2.800
E1	2.600	-	2.800
e	0.500 BSC		
k	0.200 MIN		
L	0.300	-	0.500
eee	0.080		

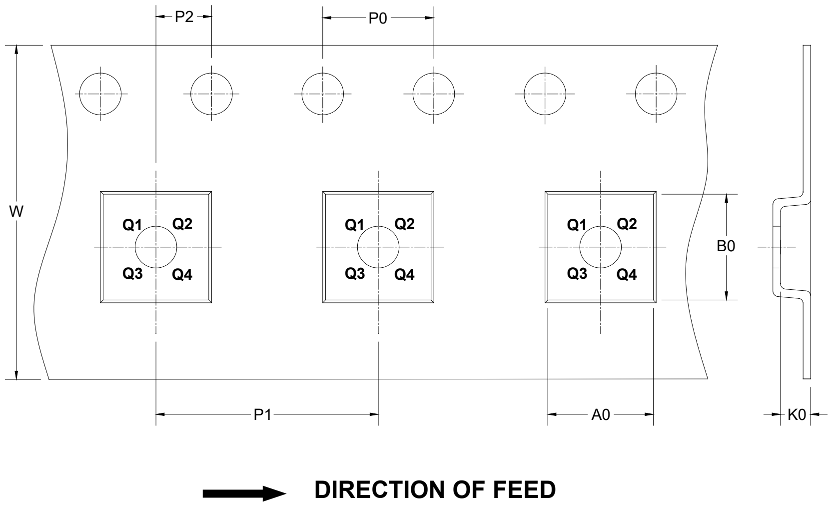
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



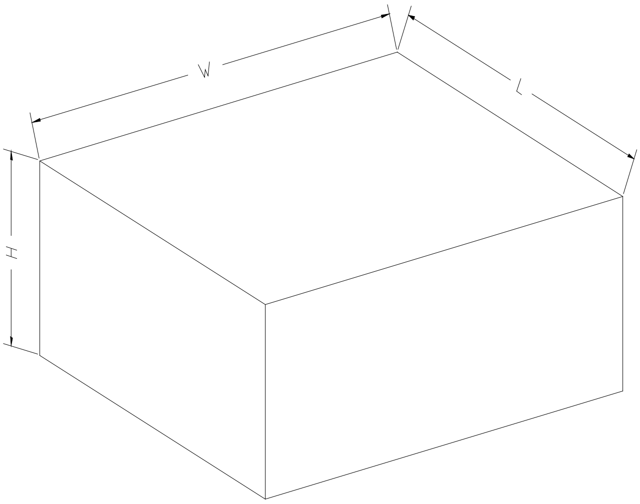
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TQFN-4×4-24L	13″	12.4	4.30	4.30	1.10	4.0	8.0	2.0	12.0	Q2

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002