

GENERAL DESCRIPTION

The 74AHC595Q is an 8-bit serial-in/serial-out or parallel-out shift register with 3-state controlled outputs designed for 2.0V to 5.5V V_{CC} operation.

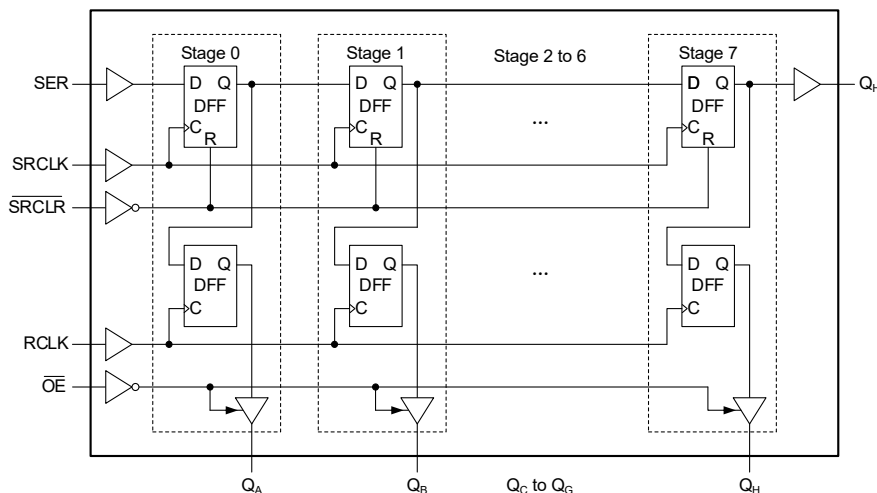
The device integrates an 8-bit shift register and an 8-bit D-type storage register. The storage register features parallel 3-state outputs. The shift register provides a clear input ($\overline{SRCLR}$) with direct overriding function, a serial input (SER) and a serial output (Q_H) to implement cascading. When output enable input ($\overline{OE}$) is held low, the data in storage register will appear at the outputs. When $\overline{OE}$ is held high, all outputs except Q_H are in high-impedance state.

Both the shift register and storage register have separate clocks. The shift register clock (SRCLK) and storage register clock (RCLK) are positive-edge triggered. If the SRCLK and RCLK are connected together, the shift register always leads one clock pulse than the storage register all the time.

The device is AEC-Q100 qualified (Automotive Electronics Council (AEC) standard Q100 Grade 1) and it is suitable for automotive applications.

The 74AHC595Q is available in Green TSSOP-16 and TQFN-2.5×3.5-16L packages. It operates over a temperature range of -40°C to +125°C.

LOGIC DIAGRAM



FEATURES

- AEC-Q100 Qualified for Automotive Applications
Device Temperature Grade 1
 $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$
- Wide Supply Voltage Range: 2.0V to 5.5V
- 8-Bit Serial-In/Serial-Out or Parallel-Out Shift Register
- Direct Clear Input of Shift Register
- -40°C to +125°C Operating Temperature Range
- Available in Green TSSOP-16 and TQFN-2.5×3.5-16L Packages

APPLICATIONS

Automotive Applications
Medical Equipment

Automotive, 8-Bit Serial-In/Serial-Out or Parallel-Out 74AHC595Q Shift Register with 3-State Controlled Outputs

PACKAGE/ORDERING INFORMATION

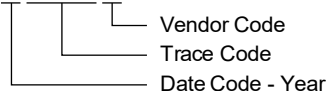
MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE TOP MARKING	PACKING OPTION
74AHC595Q	TSSOP-16	-40°C to +125°C	74AHC595QTS16G/TR	1DXTS16 XXXXX	Tape and Reel, 4000
	TQFN-2.5×3.5-16L	-40°C to +125°C	74AHC595QTRG16G/TR	1DYTRG XXXXYY	Tape and Reel, 8000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code. XXXX = Date Code, Trace Code and Vendor Code.

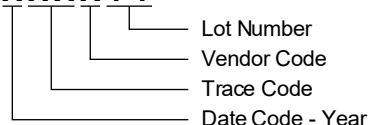
TSSOP-16

XXXXX



TQFN-2.5×3.5-16L

XXXXYY



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage Range, V_{CC} -0.5V to 7.0V
 Input Voltage Range, V_I ⁽¹⁾ -0.5V to 7.0V
 Output Voltage Range, V_O ⁽¹⁾ -0.5V to MIN(7.0V, $V_{CC} + 0.5V$)
 Input Clamp Current, I_{IK} ($V_I < 0V$) -20mA
 Output Clamp Current, I_{OK} ($V_O < 0V$ or $V_O > V_{CC}$) $\pm 20mA$
 Continuous Output Current, I_O ($V_O = 0V$ to V_{CC}) $\pm 25mA$
 Continuous Current through V_{CC} or GND $\pm 75mA$
 Junction Temperature ⁽²⁾ +150°C
 Storage Temperature Range -65°C to +150°C
 Lead Temperature (Soldering, 10s) +260°C
 ESD Susceptibility ^{(3) (4)}
 HBM $\pm 5000V$
 CDM $\pm 1000V$

NOTES:

1. The input and output voltage ratings may be exceeded if the input and output clamp current ratings are observed.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability.
3. For human body model (HBM), all pins comply with AEC-Q100-002 specification.
4. For charged device model (CDM), all pins comply with AEC-Q100-011 specification.
5. Unused input pins must be held at V_{CC} or GND to guarantee the device in normal operation.

RECOMMENDED OPERATING CONDITIONS

Supply Voltage Range, V_{CC} 2.0V to 5.5V
 Input Voltage Range, V_I ⁽⁵⁾ 0V to 5.5V
 Output Voltage Range, V_O 0V to V_{CC}
 Input Transition Rise or Fall Rate, $\Delta t/\Delta V$
 $V_{CC} = 3.3V \pm 0.3V$ 100ns/V (MAX)
 $V_{CC} = 5.0V \pm 0.5V$ 20ns/V (MAX)
 Operating Temperature Range -40°C to +125°C

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

74AHC595Q Automotive, 8-Bit Serial-In/Serial-Out or Parallel-Out Shift Register with 3-State Controlled Outputs

FUNCTION TABLE

CONTROL INPUTS				INPUT	OUTPUTS		FUNCTION
SRCLK	RCLK	OE	SRCLR	SER	Q _{H'}	Q _A ~ Q _H	
X	X	L	L	X	L	NC	When $\overline{\text{SRCLR}}$ is low, it only affects the shift register.
X	↑	L	L	X	L	L	Load the empty shift register into the storage register.
X	X	H	L	X	L	Z	Shift register is reset and all parallel outputs are in high-impedance state.
↑	X	L	H	H	Q _{G'}	NC	When shift register stage 0 goes high, data of all shift register stages shifted through, e.g. the serial output (Q _{H'}) presents the previous state of stage 6 (internal Q _{G'}).
X	↑	L	H	X	NC	Q _{X'}	Data of shift register (internal Q _{X'}) is transferred to the storage register and parallel output stages.
↑	↑	L	H	X	Q _{G'}	Q _{X'}	Data of shift register shifted through, previous data of the shift register is transferred to the storage register and parallel output stages.

H = High Voltage Level

L = Low Voltage Level

↑ = Low-to-High Clock Transition

Z = High-Impedance State

NC = No Change

X = Don't Care

TIMING DIAGRAM

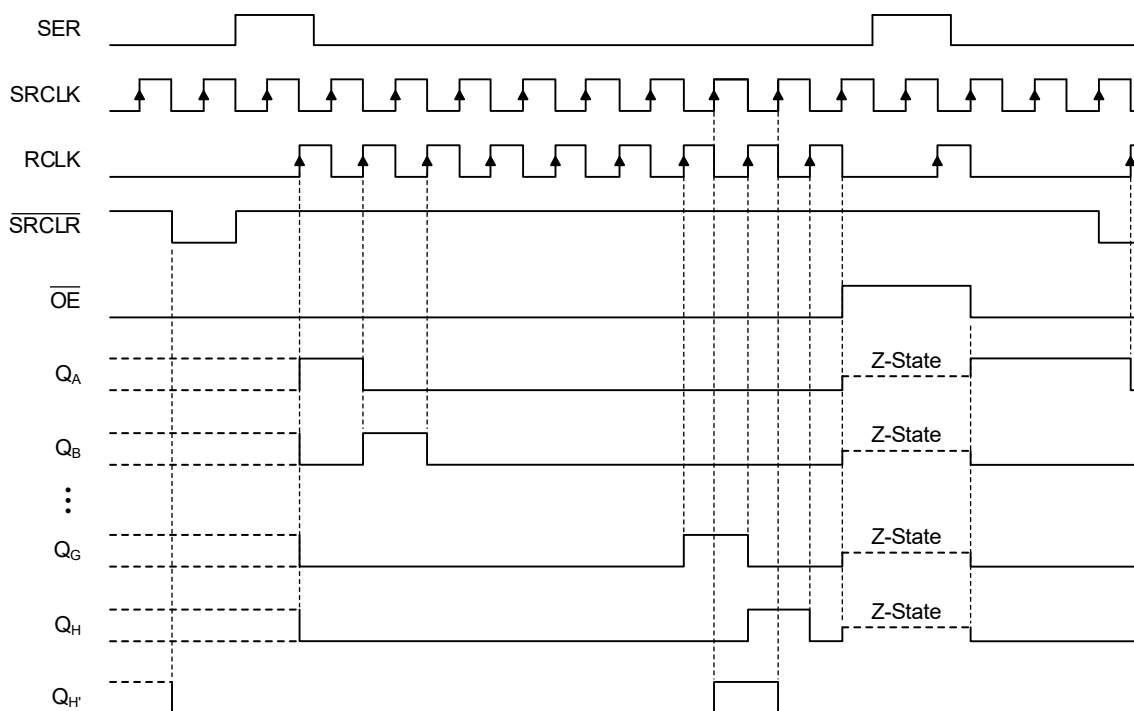
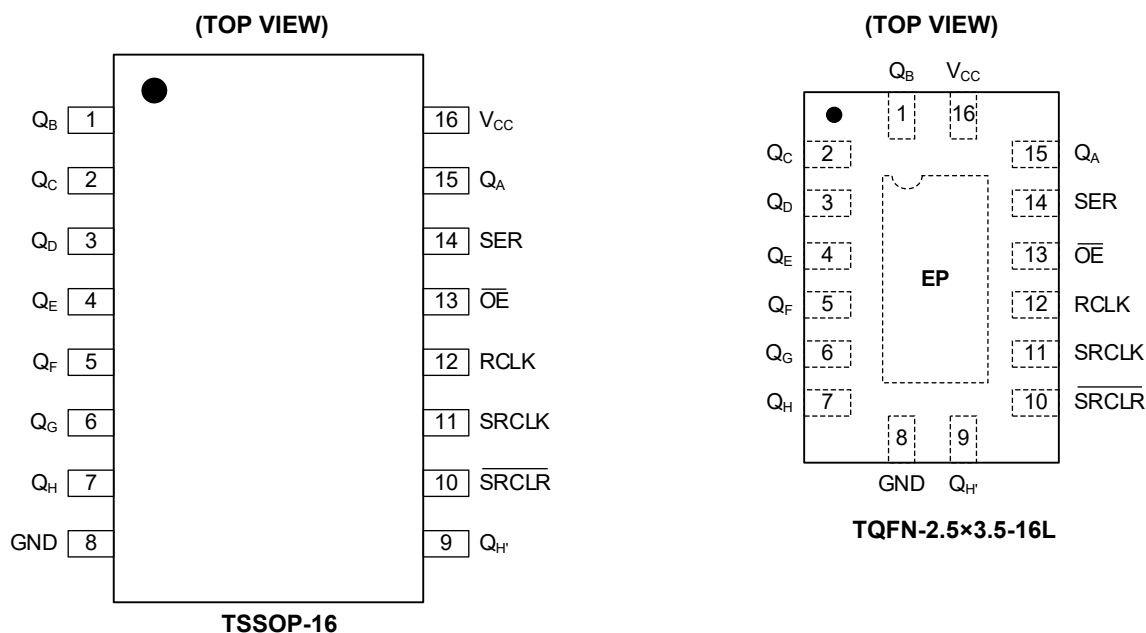


Figure 1. Timing Diagram

74AHC595Q Automotive, 8-Bit Serial-In/Serial-Out or Parallel-Out Shift Register with 3-State Controlled Outputs

PIN CONFIGURATIONS



PIN DESCRIPTION

PIN	NAME	FUNCTION
15, 1, 2, 3, 4, 5, 6, 7	Q_A , Q_B , Q_C , Q_D , Q_E , Q_F , Q_G , Q_H	Parallel Data Outputs.
8	GND	Ground.
9	$Q_{H'}$	Serial Data Output.
10	$\overline{SRCLR}$	Shift Register Clear Input (Active-Low).
11	SRCLK	Shift Register Clock Input (Rising Edge Triggered).
12	RCLK	Storage Register Clock Input (Rising Edge Triggered).
13	$\overline{OE}$	Output Enable Input (Active-Low).
14	SER	Serial Data Input.
16	V_{CC}	Power Supply.
Exposed Pad	EP	Connect it to GND internally. This pad is not an electrical connection point. TQFN-2.5x3.5-16L package only.

Automotive, 8-Bit Serial-In/Serial-Out or Parallel-Out 74AHC595Q Shift Register with 3-State Controlled Outputs

ELECTRICAL CHARACTERISTICS

(Full = -40°C to +125°C, all typical values are measured at T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	TEMP	MIN	TYP	MAX	UNITS
High-Level Input Voltage	V _{IH}	V _{CC} = 2.0V	Full	1.5			V
		V _{CC} = 3.0V	Full	2.1			
		V _{CC} = 5.5V	Full	3.85			
Low-Level Input Voltage	V _{IL}	V _{CC} = 2.0V	Full			0.5	V
		V _{CC} = 3.0V	Full			0.9	
		V _{CC} = 5.5V	Full			1.65	
High-Level Output Voltage	V _{OH}	V _{CC} = 2.0V, I _{OH} = -50μA	Full	1.9	1.995		V
		V _{CC} = 3.0V, I _{OH} = -50μA	Full	2.9	2.995		
		V _{CC} = 4.5V, I _{OH} = -50μA	Full	4.4	4.495		
		V _{CC} = 3.0V, I _{OH} = -4mA	Full	2.5	2.85		
		V _{CC} = 4.5V, I _{OH} = -8mA	Full	3.8	4.3		
Low-Level Output Voltage	V _{OL}	V _{CC} = 2.0V, I _{OL} = 50μA	Full		0.005	0.1	V
		V _{CC} = 3.0V, I _{OL} = 50μA	Full		0.005	0.1	
		V _{CC} = 4.5V, I _{OL} = 50μA	Full		0.005	0.1	
		V _{CC} = 3.0V, I _{OL} = 4mA	Full		0.15	0.5	
		V _{CC} = 4.5V, I _{OL} = 8mA	Full		0.20	0.5	
Input Leakage Current	I _I	V _{CC} = 0V to 5.5V, V _I = 5.5V or GND	Full		±0.01	±1	μA
Off-State Output Current	I _{OZ}	Q _A ~ Q _H , V _{CC} = 5.5V, V _I = V _{CC} or GND, V _O = V _{CC} or GND, $\overline{OE}$ = V _{IH} or V _{IL}	Full		±0.01	±5	μA
Supply Current	I _{CC}	V _{CC} = 5.5V, V _I = V _{CC} or GND, I _O = 0A	Full		0.02	5	μA
Input Capacitance	C _I	V _{CC} = 5.0V, V _I = V _{CC} or GND	+25°C		4		pF
Output Capacitance	C _O	V _{CC} = 5.0V, V _O = V _{CC} or GND	+25°C		5.5		pF

74AHC595Q Automotive, 8-Bit Serial-In/Serial-Out or Parallel-Out Shift Register with 3-State Controlled Outputs

DYNAMIC CHARACTERISTICS

(See Figure 2 for test circuit. Full = -40°C to +125°C, $C_L = 50\text{pF}$, all typical values are measured at $T_A = +25^\circ\text{C}$, $V_{CC} = 3.3\text{V}$ and 5.0V respectively, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		TEMP	MIN ⁽¹⁾	TYP	MAX ⁽¹⁾	UNITS
Low-to-High Propagation Delay	t _{PLH}	RCLK to Q _A ~ Q _H , see Figure 4	V _{CC} = 3.3V ± 0.3V	Full	1	8.5	14.2	ns
			V _{CC} = 5.0V ± 0.5V	Full	0.5	6.5	10.2	
		SRCLK to Q _H , see Figure 3	V _{CC} = 3.3V ± 0.3V	Full	1	9.0	14.4	
			V _{CC} = 5.0V ± 0.5V	Full	1	6.5	10.3	
High-to-Low Propagation Delay	t _{PHL}	RCLK to Q _A ~ Q _H , see Figure 4	V _{CC} = 3.3V ± 0.3V	Full	1	8.5	13.6	ns
			V _{CC} = 5.0V ± 0.5V	Full	1	6.5	10.2	
		SRCLK to Q _H , see Figure 3	V _{CC} = 3.3V ± 0.3V	Full	1	8.5	13.9	
			V _{CC} = 5.0V ± 0.5V	Full	0.5	8.5	13.7	
		SRCLR to Q _H , see Figure 6	V _{CC} = 3.3V ± 0.3V	Full	1	7.5	14.9	
			V _{CC} = 5.0V ± 0.5V	Full	0.5	6.5	11.7	
Off-to-High Propagation Delay	t _{PZH}	$\overline{OE}$ to Q _A ~ Q _H , see Figure 7	V _{CC} = 3.3V ± 0.3V	Full	1	7.5	13.0	ns
Off-to-Low Propagation Delay	t _{PZL}		V _{CC} = 5.0V ± 0.5V	Full	0.5	6.0	9.6	
			V _{CC} = 3.3V ± 0.3V	Full	1	7.5	12.0	
			V _{CC} = 5.0V ± 0.5V	Full	0.5	6.0	9.4	
High-to-Off Propagation Delay	t _{PHZ}	$\overline{OE}$ to Q _A ~ Q _H , see Figure 7	V _{CC} = 3.3V ± 0.3V	Full	1	11.0	15.8	ns
Low-to-Off Propagation Delay	t _{PLZ}		V _{CC} = 5.0V ± 0.5V	Full	1	8.0	11.4	
			V _{CC} = 3.3V ± 0.3V	Full	1	11.0	16.8	
			V _{CC} = 5.0V ± 0.5V	Full	1	6.5	12.2	
Maximum Frequency	f _{MAX}	See Figure 3 and Figure 4	V _{CC} = 3.3V ± 0.3V	Full	90	130		MHz
			V _{CC} = 5.0V ± 0.5V	Full	100	155		

NOTE:

1. Specified by design and characterization, not production tested.

Automotive, 8-Bit Serial-In/Serial-Out or Parallel-Out 74AHC595Q Shift Register with 3-State Controlled Outputs

DYNAMIC CHARACTERISTICS (continued)

(See Figure 2 for test circuit. Full = -40°C to +125°C, $C_L = 50\text{pF}$, all typical values are measured at $T_A = +25^\circ\text{C}$, $V_{CC} = 3.3\text{V}$ and 5.0V respectively, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	TEMP	MIN ⁽¹⁾	TYP	MAX ⁽¹⁾	UNITS
Pulse Width	t_W	SRCLK high or low, see Figure 3	$V_{CC} = 3.3\text{V} \pm 0.3\text{V}$	Full	6		ns
			$V_{CC} = 5.0\text{V} \pm 0.5\text{V}$	Full	6		
		RCLK high or low, see Figure 4	$V_{CC} = 3.3\text{V} \pm 0.3\text{V}$	Full	6		
			$V_{CC} = 5.0\text{V} \pm 0.5\text{V}$	Full	6		
		$\overline{\text{SRCLR}}$ low, see Figure 6	$V_{CC} = 3.3\text{V} \pm 0.3\text{V}$	Full	9		
			$V_{CC} = 5.0\text{V} \pm 0.5\text{V}$	Full	9		
Setup Time	t_{SU}	SER before SRCLK $\uparrow$, see Figure 5	$V_{CC} = 3.3\text{V} \pm 0.3\text{V}$	Full	4		ns
			$V_{CC} = 5.0\text{V} \pm 0.5\text{V}$	Full	3		
		SRCLK $\uparrow$ before RCLK $\uparrow$ ⁽²⁾ , see Figure 4	$V_{CC} = 3.3\text{V} \pm 0.3\text{V}$	Full	7		
			$V_{CC} = 5.0\text{V} \pm 0.5\text{V}$	Full	4		
		$\overline{\text{SRCLR}}$ low before RCLK $\uparrow$, see Figure 6	$V_{CC} = 3.3\text{V} \pm 0.3\text{V}$	Full	7		
			$V_{CC} = 5.0\text{V} \pm 0.5\text{V}$	Full	5		
		$\overline{\text{SRCLR}}$ high (inactive) before SRCLK $\uparrow$, see Figure 6	$V_{CC} = 3.3\text{V} \pm 0.3\text{V}$	Full	2		
			$V_{CC} = 5.0\text{V} \pm 0.5\text{V}$	Full	2		
Hold Time	t_H	SER after SRCLK $\uparrow$, see Figure 5	$V_{CC} = 3.3\text{V} \pm 0.3\text{V}$	Full	2.5		ns
			$V_{CC} = 5.0\text{V} \pm 0.5\text{V}$	Full	2		
Power Dissipation Capacitance ^{(3) (4)}	C_{PD}	No load, $V_{CC} = 5.0\text{V} \pm 0.5\text{V}$, $f = 10\text{MHz}$	+25°C		85		pF

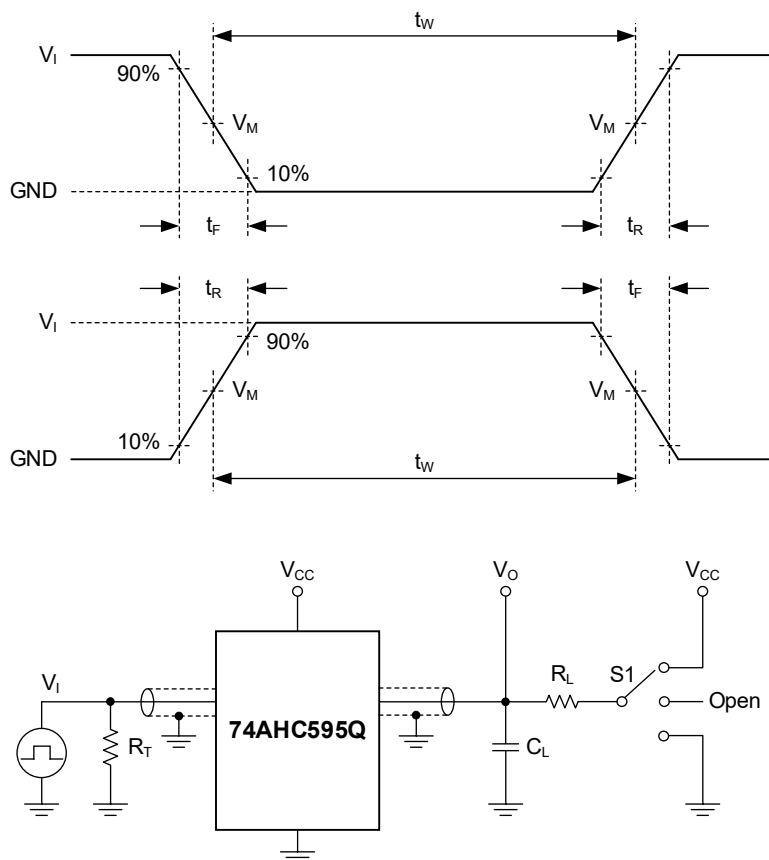
NOTES:

- Specified by design and characterization, not production tested.
- The setup time enables the storage register to get stable data from the shift register. In this case where clocks can be tied together, the shift register is a clock pulse in front of the storage register.
- C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$$
 where:
 f_i = Input frequency in MHz.
 f_o = Output frequency in MHz.
 C_L = Output load capacitance in pF.
 V_{CC} = Supply voltage in Volts.
 N = Number of inputs switching.
 $\Sigma(C_L \times V_{CC}^2 \times f_o)$ = Sum of outputs.
- All 9 outputs switching.

74AHC595Q Automotive, 8-Bit Serial-In/Serial-Out or Parallel-Out Shift Register with 3-State Controlled Outputs

TEST CIRCUIT



Test conditions are given in Table 1.

Definitions test circuit:

R_L : Load resistance.

C_L : Load capacitance (includes jig and probe).

R_T : Termination resistance (equals to output impedance Z_O of the pulse generator).

$S1$: Test selection switch.

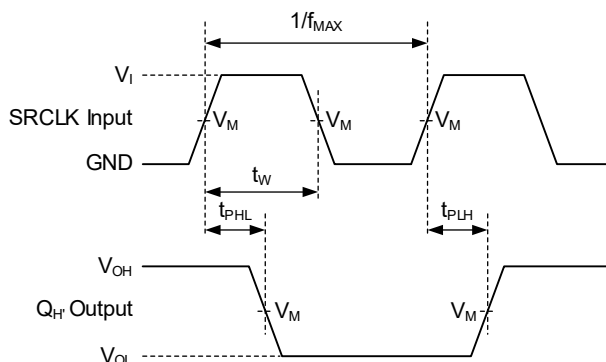
Figure 2. Test Circuit for Measuring Switching Times

Table 1. Test Conditions

SUPPLY VOLTAGE	INPUT		LOAD		S1 POSITION		
V_{CC}	V_I	t_R, t_F	C_L	R_L	t_{PHL}, t_{PLH}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
2.0V to 5.5V	V_{CC}	$\leq 3.0\text{ns}$	50pF	1k Ω	Open	GND	V_{CC}

74AHC595Q Automotive, 8-Bit Serial-In/Serial-Out or Parallel-Out Shift Register with 3-State Controlled Outputs

WAVEFORMS

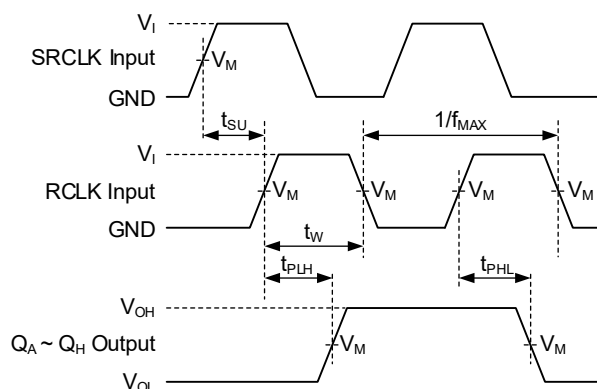


Test conditions are given in Table 1.

Measurement points are given in Table 2.

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Figure 3. Shift Register Clock Input to Output Propagation Delay Times, Pulse Width and Maximum Frequency

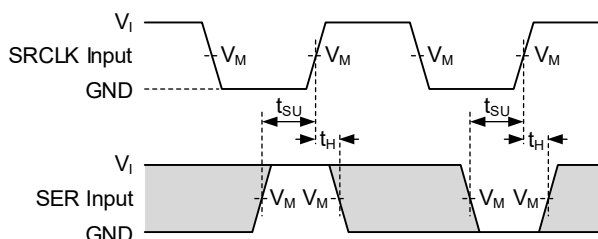


Test conditions are given in Table 1.

Measurement points are given in Table 2.

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Figure 4. Storage Register Clock Input to Output Propagation Delay Times, Shift Register Clock to Storage Register Clock Setup Time, Pulse Width and Maximum Frequency



Test conditions are given in Table 1.

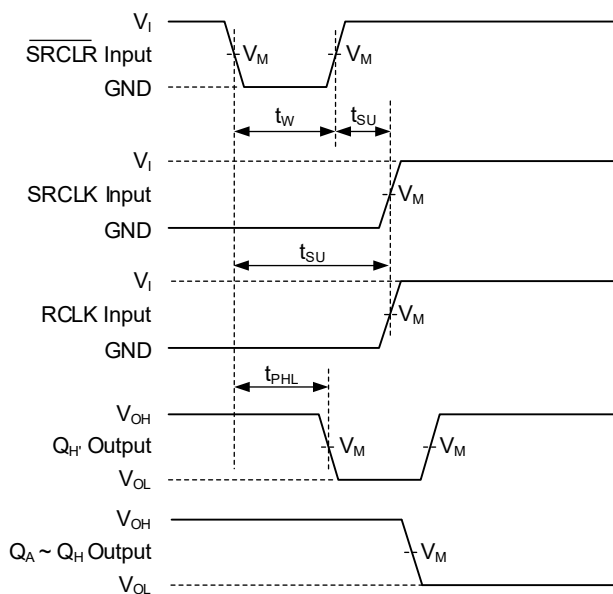
Measurement points are given in Table 2.

The shaded areas refer to when the input is allowed to change for predictable output performance.

Figure 5. Data Setup and Hold Times

74AHC595Q Automotive, 8-Bit Serial-In/Serial-Out or Parallel-Out Shift Register with 3-State Controlled Outputs

WAVEFORMS (continued)

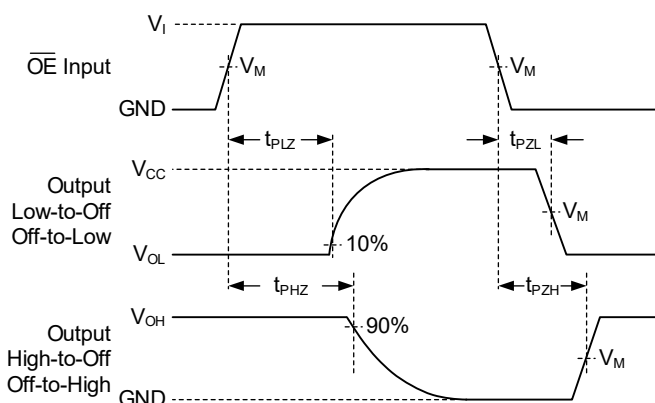


Test conditions are given in Table 1.

Measurement points are given in Table 2.

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Figure 6. Clear Input to Output Propagation Delay Times, Pulse Width and Setup Time



Test conditions are given in Table 1.

Measurement points are given in Table 2.

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Figure 7. Enable and Disable Times

Table 2. Measurement Points

SUPPLY VOLTAGE	INPUT		OUTPUT
V_{CC}	V_I	$V_M^{(1)}$	V_M
2.0V to 5.5V	V_{CC}	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$

NOTE:

1. The measurement points should be V_{IH} or V_{IL} when the input rising or falling time exceeds 3.0ns.

74AHC595Q Automotive, 8-Bit Serial-In/Serial-Out or Parallel-Out Shift Register with 3-State Controlled Outputs

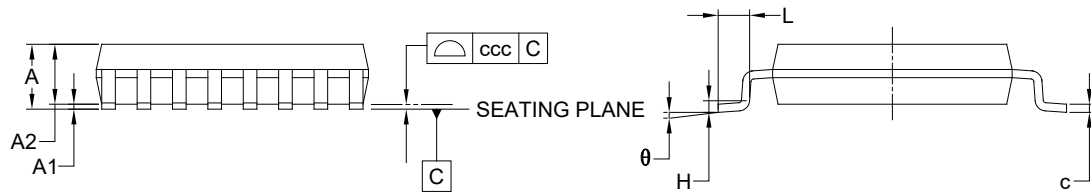
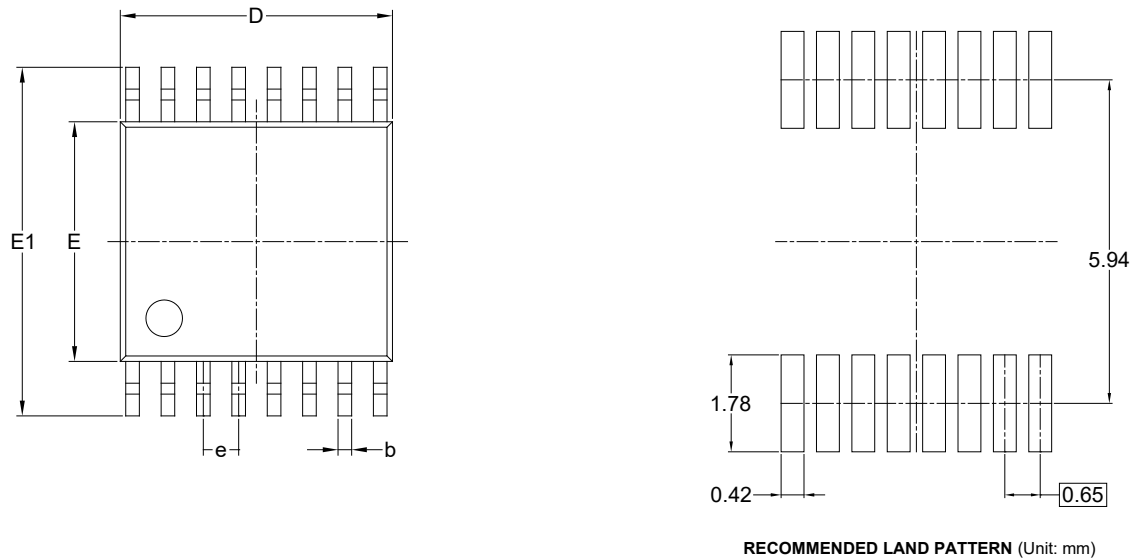
REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

OCTOBER 2025 – REV.A.1 to REV.A.2		Page
Updated Timing Diagram section.....		3
JUNE 2025 – REV.A to REV.A.1		Page
Updated Electrical Characteristics section		5
Added TQFN-2.5×3.5-16L package		All
Changes from Original (FEBRUARY 2025) to REV.A		Page
Changed from product preview to production data.....		All

PACKAGE OUTLINE DIMENSIONS

TSSOP-16



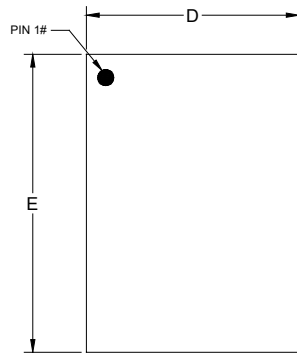
Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	-	-	1.200
A1	0.050	-	0.150
A2	0.800	-	1.050
b	0.190	-	0.300
c	0.090	-	0.200
D	4.860	-	5.100
E	4.300	-	4.500
E1	6.200	-	6.600
e	0.650 BSC		
L	0.450	-	0.750
H	0.250 TYP		
θ	0°	-	8°
ccc	0.100		

NOTES:

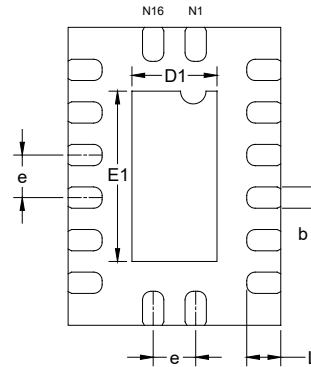
1. This drawing is subject to change without notice.
2. The dimensions do not include mold flashes, protrusions or gate burrs.
3. Reference JEDEC MO-153.

PACKAGE OUTLINE DIMENSIONS

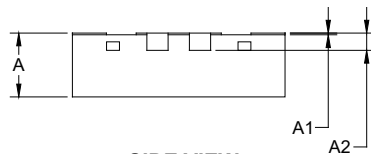
TQFN-2.5×3.5-16L



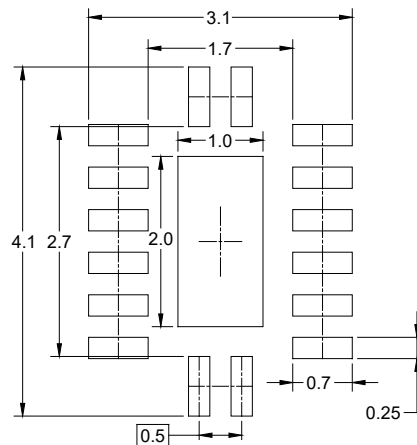
TOP VIEW



BOTTOM VIEW



SIDE VIEW



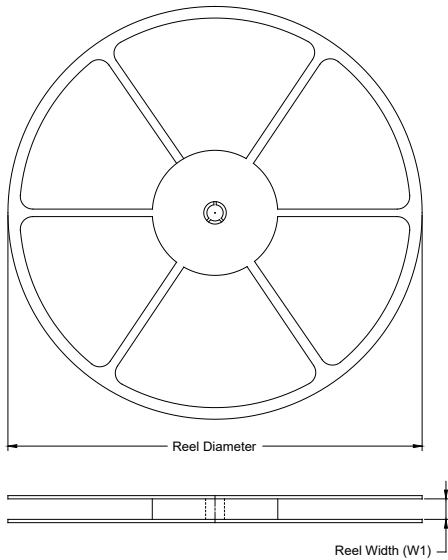
RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A2	0.203 REF		
b	0.20	0.25	0.30
D	2.40	2.50	2.60
D1	0.85	1.00	1.15
E	3.40	3.50	3.60
E1	1.85	2.00	2.15
e	0.45	0.50	0.55
L	0.30	0.40	0.50

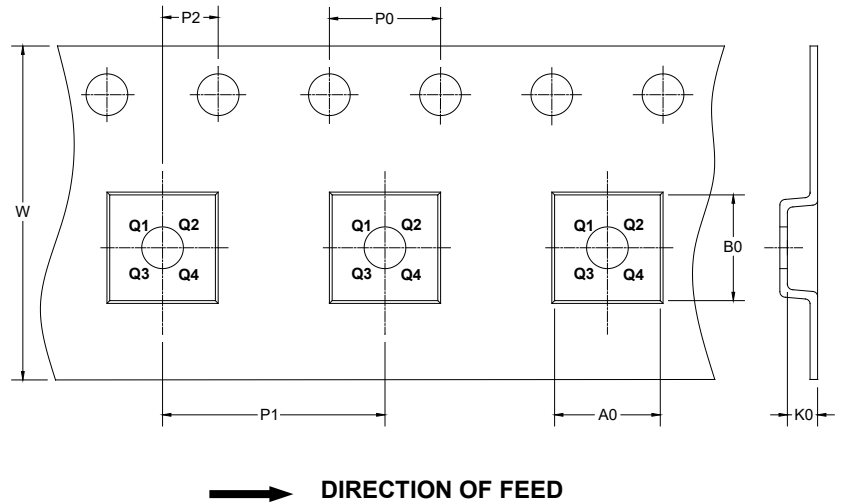
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

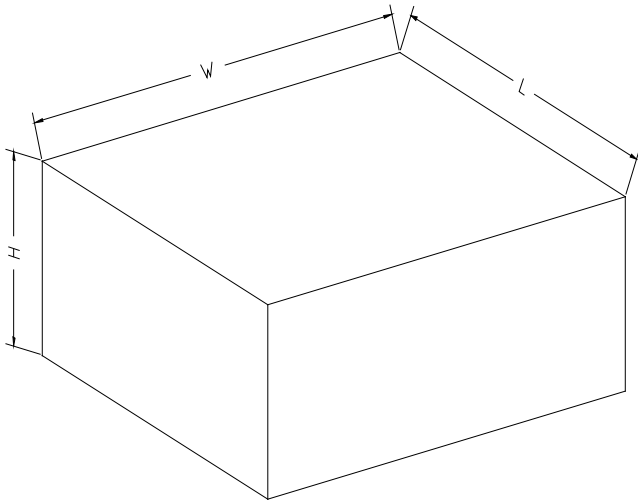
KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TSSOP-16	13"	12.4	6.80	5.40	1.50	4.0	8.0	2.0	12.0	Q1
TQFN-2.5×3.5-16L	13"	12.4	2.80	3.80	1.13	4.0	4.0	2.0	12.0	Q1

DD00001

PACKAGE INFORMATION

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13"	386	280	370	5

DD0002