

GENERAL DESCRIPTION

The 74HC4067 and 74HCT4067 devices are digitally controlled analog switches that include four address inputs (S0 to S3), sixteen individual I/O channels (Y0 to Y15), a common I/O pin (Z) and an active-low enable control input (\overline{EN}).

The 74HC4067 and 74HCT4067 are single-pole/16-throw (SP16T) analog switches, where one terminal is linked to an individual input/output (Y0 to Y15), and the other pins are connected to the common input/output (Z).

When pin \overline{EN} is active low, one of the sixteen switches is chosen through the configuration of pins S0 to S3, setting it in a low-impedance on-state. All other unselected switches are in a high-impedance off-state. Conversely, when pin \overline{EN} is active high, all switches are in the high-impedance off-state, regardless of the state of pins S0 to S3.

The analog inputs/outputs (Y0 to Y15 and Z) can vary between V_{CC} as the upper limit and GND as the lower limit.

The 74HC4067 and 74HCT4067 are available in Green SOIC-24, TSSOP-24 and TQFN-3.5x5.5-24BL packages. They operate over an ambient temperature range of -40°C to +125°C.

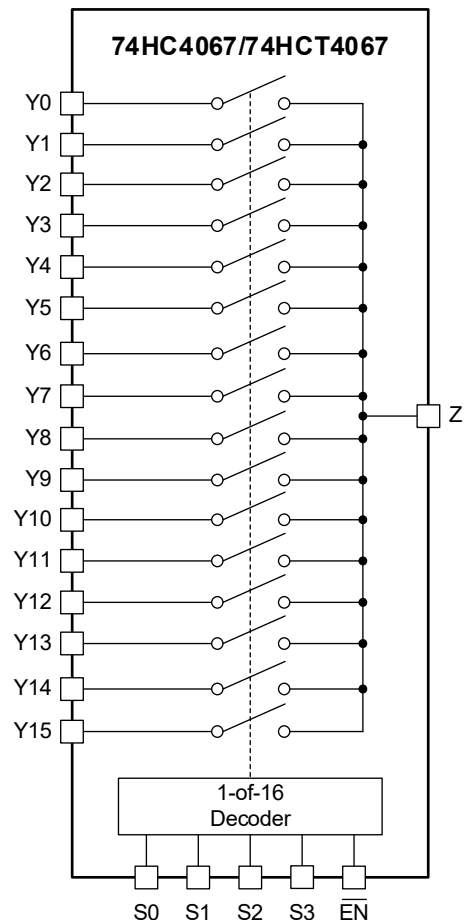
APPLICATIONS

Industrial, Telecom, Medical Equipment
Computing Equipment

FEATURES

- **Wide Supply Voltage Range:**
 - ♦ 74HC4067: 2V to 12V
 - ♦ 74HCT4067: 4.5V to 5.5V
- **Low On-Resistance:**
 - ♦ 220Ω (TYP) at $V_{CC} = 2V$
 - ♦ 86Ω (TYP) at $V_{CC} = 5V$
 - ♦ 60Ω (TYP) at $V_{CC} = 10V$
- **Integrated Break-Before-Make Function**
- **-40°C to +125°C Operating Temperature Range**
- **Available in Green SOIC-24, TSSOP-24 and TQFN-3.5x5.5-24BL Packages**

LOGIC DIAGRAM



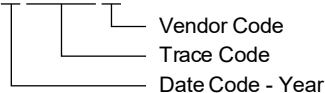
PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
74HC4067	SOIC-24	-40°C to +125°C	74HC4067XS24G/TR	74HC4067XS24 XXXXX	Tape and Reel, 1500
	TSSOP-24	-40°C to +125°C	74HC4067XTS24G/TR	74HC4067 XTS24 XXXXX	Tape and Reel, 4000
	TQFN-3.5×5.5-24BL	-40°C to +125°C	74HC4067XTWJ24G/TR	74HC4067 XTWJ24 XXXXX	Tape and Reel, 3000
74HCT4067	SOIC-24	-40°C to +125°C	74HCT4067XS24G/TR	74HCT4067XS24 XXXXX	Tape and Reel, 1500
	TSSOP-24	-40°C to +125°C	74HCT4067XTS24G/TR	74HCT4067 XTS24 XXXXX	Tape and Reel, 4000
	TQFN-3.5×5.5-24BL	-40°C to +125°C	74HCT4067XTWJ24G/TR	74HCT4067 XTWJ24 XXXXX	Tape and Reel, 3000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.

XXXXX



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions.

Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage Range, V_{CC}	-0.5V to 13.2V
Input Voltage Range, V_I	-0.5V to MIN(13.2V, $V_{CC} + 0.5V$)
Switch Voltage Range, V_{SW}	-0.5V to MIN(13.2V, $V_{CC} + 0.5V$)
Input Clamp Current, $I_{IK}^{(1)}$ ($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) $\pm 20mA$
Switch Clamp Current, $I_{SK}^{(1)}$ ($V_{SW} < -0.5V$ or $V_{SW} > V_{CC} + 0.5V$) $\pm 20mA$
Switch Current, I_{SW} ($V_{SW} = -0.5V$ to $V_{CC} + 0.5V$)	$\pm 25mA$
Supply Current, I_{CC}	50mA
Ground Current, I_{GND}	-50mA
Junction Temperature ⁽²⁾	+150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 10s)	+260°C
ESD Susceptibility ^{(3) (4)}	
HBM	$\pm 6000V$
CDM	$\pm 1000V$

NOTES:

1. The input and output voltage ratings may be exceeded if the input and output clamp current ratings are observed.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability.
3. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.
4. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

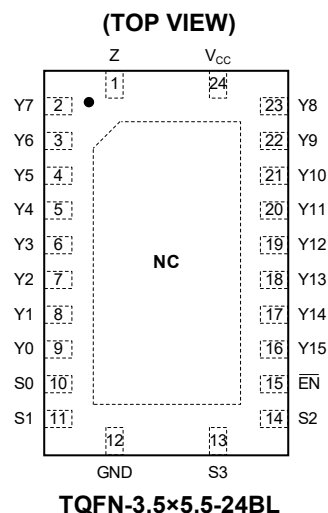
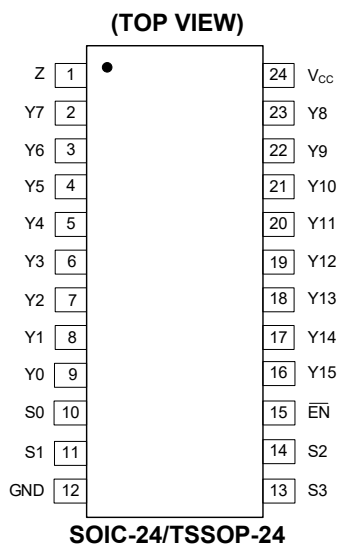
RECOMMENDED OPERATING CONDITIONS**For 74HC4067**

Supply Voltage Range, V_{CC}	2V to 12V, 5V (TYP)
Input Voltage Range, V_I	0V to V_{CC}
Switch Voltage Range, V_{SW}	0V to V_{CC}
Rise Time, t_R	
$V_{CC} = 2V$	1000ns (MAX)
$V_{CC} = 5V$	500ns (MAX), 6.0ns (TYP)
$V_{CC} = 10V$	250ns (MAX)
Fall Time, t_F	
$V_{CC} = 2V$	1000ns (MAX)
$V_{CC} = 5V$	500ns (MAX), 6.0ns (TYP)
$V_{CC} = 10V$	250ns (MAX)
Operating Ambient Temperature Range	-40°C to +125°C

For 74HCT4067

Supply Voltage Range, V_{CC}	4.5V to 5.5V, 5V (TYP)
Input Voltage Range, V_I	0V to V_{CC}
Switch Voltage Range, V_{SW}	0V to V_{CC}
Rise Time, t_R	
$V_{CC} = 5V$	500ns (MAX), 6.0ns (TYP)
Fall Time, t_F	
$V_{CC} = 5V$	500ns (MAX), 6.0ns (TYP)
Operating Ambient Temperature Range	-40°C to +125°C

PIN CONFIGURATIONS



PIN DESCRIPTION

PIN	NAME	FUNCTION
1	Z	Common Input/Output.
2 – 9	Y7 – Y0	Individual Input/Output 7 – 0.
10	S0	Address Input 0.
11	S1	Address Input 1.
12	GND	Ground.
13	S3	Address Input 3.
14	S2	Address Input 2.
15	$\overline{\text{EN}}$	Enable Control Input (Active-Low).
16 – 23	Y15 – Y8	Individual Input/Output 15 – 8.
24	V _{cc}	Power Supply Voltage.
Exposed Pad	NC	No Connection. TQFN-3.5x5.5-24BL package only.

FUNCTION TABLE

$\overline{\text{EN}}$	INPUTS				CHANNEL ON
	S3	S2	S1	S0	
L	L	L	L	L	Y0 to Z
L	L	L	L	H	Y1 to Z
L	L	L	H	L	Y2 to Z
L	L	L	H	H	Y3 to Z
L	L	H	L	L	Y4 to Z
L	L	H	L	H	Y5 to Z
L	L	H	H	L	Y6 to Z
L	L	H	H	H	Y7 to Z
L	H	L	L	L	Y8 to Z
L	H	L	L	H	Y9 to Z
L	H	L	H	L	Y10 to Z
L	H	L	H	H	Y11 to Z
L	H	H	L	L	Y12 to Z
L	H	H	L	H	Y13 to Z
L	H	H	H	L	Y14 to Z
L	H	H	H	H	Y15 to Z
H	X	X	X	X	—

NOTE: H = High Voltage Level, L = Low Voltage Level, X = Don't Care.

ELECTRICAL CHARACTERISTICS

(Full = -40°C to +125°C, all typical values are measured at $T_A = +25^\circ\text{C}$. V_I equals either V_{IH} or V_{IL} . V_{IS} represents the input voltage at either the Yn or Z terminal, depending on which is designated as an input. V_{OS} represents the output voltage at either the Yn or Z terminal, depending on which is designated as an output.)

PARAMETER	SYMBOL	CONDITIONS	TEMP	MIN	TYP	MAX	UNITS	
On-Resistance Per Switch for 74HC4067								
On-Resistance (Peak)	R_{ON_PEAK}	$V_{IS} = \text{GND to } V_{CC}$, see Figure 1	$V_{CC} = 2\text{V}, I_{SW} = 100\mu\text{A}^{(1)}$	+25°C		1600	Ω	
			$V_{CC} = 5\text{V}, I_{SW} = 1\text{mA}$	+25°C		105		135
				Full				170
			$V_{CC} = 10\text{V}, I_{SW} = 1\text{mA}$	+25°C		65		85
Full				105				
On-Resistance (Rail)	R_{ON_RAIL}	$V_{IS} = \text{GND or } V_{CC}$, see Figure 1	$V_{CC} = 2\text{V}, I_{SW} = 100\mu\text{A}^{(1)}$	+25°C		220	Ω	
				Full				500
			$V_{CC} = 5\text{V}, I_{SW} = 1\text{mA}$	+25°C		86		120
				Full				160
			$V_{CC} = 10\text{V}, I_{SW} = 1\text{mA}$	+25°C		60		80
				Full				100
On-Resistance Mismatch between Channels	ΔR_{ON}	$V_{IS} = \text{GND to } V_{CC}$, see Figure 1	$V_{CC} = 2\text{V}$	+25°C		40	Ω	
				Full				12
			$V_{CC} = 5\text{V}$	+25°C		3		12
				Full				15
			$V_{CC} = 10\text{V}$	+25°C		3		12
				Full				15
On-Resistance Per Switch for 74HCT4067								
On-Resistance (Peak)	R_{ON_PEAK}	$V_{IS} = \text{GND to } V_{CC}$, see Figure 1	$V_{CC} = 5\text{V}, I_{SW} = 1\text{mA}$	+25°C		105	Ω	
				Full				170
On-Resistance (Rail)	R_{ON_RAIL}	$V_{IS} = \text{GND or } V_{CC}$, see Figure 1	$V_{CC} = 5\text{V}, I_{SW} = 1\text{mA}$	+25°C		86	Ω	
				Full				160
On-Resistance Mismatch between Channels	ΔR_{ON}	$V_{IS} = \text{GND to } V_{CC}$, see Figure 1	$V_{CC} = 5\text{V}$	+25°C		3	Ω	
				Full				15

NOTE:

1. When the supply voltage ($V_{CC} - \text{GND}$) nears 2V, the on-resistance of analog switch becomes highly non-linear. Consequently, it is advisable to utilize these devices for transmitting digital signals at such supply voltages.

ELECTRICAL CHARACTERISTICS (continued)

(Full = -40°C to +125°C, all typical values are measured at $T_A = +25^\circ\text{C}$. V_{IS} represents the input voltage at either the Y_n or Z terminal, depending on which is designated as an input. V_{OS} represents the output voltage at either the Y_n or Z terminal, depending on which is designated as an output.)

PARAMETER	SYMBOL	CONDITIONS	TEMP	MIN	TYP	MAX	UNITS	
For 74HC4067								
High-Level Input Voltage	V_{IH}	$V_{CC} = 2V$	Full	1.5			V	
		$V_{CC} = 5V$	Full	3.15				
		$V_{CC} = 10V$	Full	6.3				
Low-Level Input Voltage	V_{IL}	$V_{CC} = 2V$	Full			0.5	V	
		$V_{CC} = 5V$	Full			1.5		
		$V_{CC} = 10V$	Full			3.0		
Input Leakage Current	I_i	$V_i = V_{CC}$ or GND	$V_{CC} = 5V$	+25°C		±0.01	±0.5	µA
				Full			±1	
			$V_{CC} = 10V$	+25°C		±0.01	±0.5	
				Full			±1	
Off-State Leakage Current	I_{S_OFF}	$V_{CC} = 10V$, $V_i = V_{IH}$ or V_{IL} , $V_{IS} = V_{CC}$ or GND, $V_{OS} = GND$ or V_{CC} , see Figure 2	Per channel	+25°C		±0.01	±0.5	µA
				Full			±1	
			All channels	+25°C		±0.01	±0.5	
				Full			±1	
On-State Leakage Current	I_{S_ON}	$V_{CC} = 10V$, $V_i = V_{IH}$ or V_{IL} , $V_{IS} = V_{CC}$ or GND, $V_{OS} = \text{floating}$ or $V_{IS} = \text{floating}$, $V_{OS} = V_{CC}$ or GND, see Figure 3	+25°C		±0.01	±0.5	µA	
			Full			±1		
Supply Current	I_{CC}	$V_i = V_{CC}$ or GND, $V_{IS} = GND$ or V_{CC} , $V_{OS} = V_{CC}$ or GND	$V_{CC} = 5V$	+25°C		0.01	0.5	µA
				Full			5	
			$V_{CC} = 10V$	+25°C		0.01	15	
				Full			100	
For 74HCT4067								
High-Level Input voltage	V_{IH}	$V_{CC} = 4.5V$ to $5.5V$	Full	2			V	
Low-Level Input Voltage	V_{IL}	$V_{CC} = 4.5V$ to $5.5V$	Full			0.8	V	
Input Leakage Current	I_i	$V_{CC} = 5.5V$, $V_i = V_{CC}$ or GND	+25°C		±0.01	±0.5	µA	
			Full			±1		
Off-State Leakage Current	I_{S_OFF}	$V_{CC} = 5.5V$, $V_i = V_{IH}$ or V_{IL} , $V_{IS} = V_{CC}$ or GND, $V_{OS} = GND$ or V_{CC} , see Figure 2	Per channel	+25°C		±0.01	±0.5	µA
				Full			±1	
			All channels	+25°C		±0.01	±0.5	
				Full			±1	
On-State Leakage Current	I_{S_ON}	$V_{CC} = 5.5V$, $V_i = V_{IH}$ or V_{IL} , $V_{IS} = V_{CC}$ or GND, $V_{OS} = \text{floating}$ or $V_{IS} = \text{floating}$, $V_{OS} = V_{CC}$ or GND, see Figure 3	+25°C		±0.01	±0.5	µA	
			Full			±1		
Supply Current	I_{CC}	$V_{CC} = 4.5V$ to $5.5V$, $V_i = V_{CC}$ or GND, $V_{IS} = GND$ or V_{CC} , $V_{OS} = V_{CC}$ or GND	+25°C		0.01	0.5	µA	
			Full			5		
Additional Supply Current	ΔI_{CC}	$V_{CC} = 4.5V$ to $5.5V$, per input pin, $V_i = V_{CC} - 2.1V$, other inputs at V_{CC} or GND	Pin \overline{EN}	+25°C		22	30	µA
				Full			35	
			Pins Sn	+25°C		22	30	
				Full			35	

DYNAMIC CHARACTERISTICS

(See Figure 7 for test circuit. Full = -40°C to +125°C, all typical values are measured at $T_A = +25^\circ\text{C}$. $GND = 0V$, $t_R = t_F = 6\text{ns}$, $C_L = 50\text{pF}$. V_{IS} represents the input voltage at either the Y_n or Z terminal, depending on which is designated as an input. V_{OS} represents the output voltage at either the Y_n or Z terminal, depending on which is designated as an output.)

PARAMETER	SYMBOL	CONDITIONS	TEMP	MIN ⁽¹⁾	TYP	MAX ⁽¹⁾	UNITS	
For 74HC4067								
Propagation Delay ⁽²⁾⁽³⁾	t_{PD}	Yn to Z, see Figure 8	$V_{CC} = 2V$	Full	1.0	24	41.2	ns
			$V_{CC} = 5V$	Full	0.5	5.0	8.4	
			$V_{CC} = 10V$	Full	0.5	3.0	5.0	
		Z to Yn, see Figure 8	$V_{CC} = 2V$	Full	1.0	20	32.3	
			$V_{CC} = 5V$	Full	0.5	4.5	7.3	
			$V_{CC} = 10V$	Full	0.5	3.0	4.8	
Turn-Off Time ⁽⁴⁾	t_{OFF}	\overline{EN} to Yn, see Figure 9	$V_{CC} = 2V$	Full	1.0	69	113	ns
			$V_{CC} = 5V$	Full	1.0	23	36.6	
			$V_{CC} = 10V$	Full	1.0	18	27.3	
		Sn to Yn, see Figure 9	$V_{CC} = 2V$	Full	1.0	73	122	
			$V_{CC} = 5V$	Full	1.0	24	38.8	
			$V_{CC} = 10V$	Full	1.0	19	28.5	
		\overline{EN} to Z, see Figure 9	$V_{CC} = 2V$	Full	1.0	69	114	
			$V_{CC} = 5V$	Full	1.0	25	38.9	
			$V_{CC} = 10V$	Full	1.0	20	29.5	
		Sn to Z, see Figure 9	$V_{CC} = 2V$	Full	1.0	74	124	
			$V_{CC} = 5V$	Full	1.0	26	41.1	
			$V_{CC} = 10V$	Full	1.0	20	30.6	
Turn-On Time ⁽⁵⁾	t_{ON}	\overline{EN} to Yn, see Figure 9	$V_{CC} = 2V$	Full	1.0	145	238	ns
			$V_{CC} = 5V$	Full	1.0	34	59.7	
			$V_{CC} = 10V$	Full	1.0	23	40.1	
		Sn to Yn, see Figure 9	$V_{CC} = 2V$	Full	1.0	152	256	
			$V_{CC} = 5V$	Full	1.0	36	64.3	
			$V_{CC} = 10V$	Full	1.0	24	42.5	
		\overline{EN} to Z, see Figure 9	$V_{CC} = 2V$	Full	1.0	144	243	
			$V_{CC} = 5V$	Full	1.0	34	61.2	
			$V_{CC} = 10V$	Full	1.0	23	40.9	
		Sn to Z, see Figure 9	$V_{CC} = 2V$	Full	1.0	156	262	
			$V_{CC} = 5V$	Full	1.0	37	65.8	
			$V_{CC} = 10V$	Full	1.0	24	43.2	

NOTES:

- Specified by design and characterization, not production tested.
- t_{PD} is the same as t_{PHL} and t_{PLH} .
- Because of the higher capacitance at the Z terminal (16 switches to 1), the delay figures are higher at the Z terminal than at the Y terminal.
- t_{OFF} is the same as t_{PHZ} and t_{PLZ} .
- t_{ON} is the same as t_{PZH} and t_{PZL} .

DYNAMIC CHARACTERISTICS (continued)

(See Figure 7 for test circuit. Full = -40°C to +125°C, all typical values are measured at T_A = +25°C. GND = 0V, t_R = t_F = 6ns, C_L = 50pF. V_{IS} represents the input voltage at either the Y_n or Z terminal, depending on which is designated as an input. V_{OS} represents the output voltage at either the Y_n or Z terminal, depending on which is designated as an output.)

PARAMETER	SYMBOL	CONDITIONS	TEMP	MIN ⁽¹⁾	TYP	MAX ⁽¹⁾	UNITS	
Power Dissipation Capacitance ⁽⁶⁾	C _{PD}	Per switch, V _I = GND to V _{CC}	+25°C		18		pF	
For 74HCT4067								
Propagation Delay ^{(2) (3)}	t _{PD}	Y _n to Z, see Figure 8	V _{CC} = 5V	Full	0.5	5.0	ns	
		Z to Y _n , see Figure 8	V _{CC} = 5V	Full	0.5	4.5		7.3
Turn-Off Time ⁽⁴⁾	t _{OFF}	$\overline{E}N$ to Y _n , see Figure 9	V _{CC} = 5V	Full	1.0	23	ns	
		Sn to Y _n , see Figure 9	V _{CC} = 5V	Full	1.0	24		38.8
		$\overline{E}N$ to Z, see Figure 9	V _{CC} = 5V	Full	1.0	25		38.9
		Sn to Z, see Figure 9	V _{CC} = 5V	Full	1.0	26		41.1
Turn-On Time ⁽⁵⁾	t _{ON}	$\overline{E}N$ to Y _n , see Figure 9	V _{CC} = 5V	Full	1.0	34	ns	
		Sn to Y _n , see Figure 9	V _{CC} = 5V	Full	1.0	36		64.3
		$\overline{E}N$ to Z, see Figure 9	V _{CC} = 5V	Full	1.0	34		61.2
		Sn to Z, see Figure 9	V _{CC} = 5V	Full	1.0	37		65.8
Power Dissipation Capacitance ⁽⁶⁾	C _{PD}	Per switch, V _I = GND to V _{CC}	+25°C		18		pF	

NOTES:

- Specified by design and characterization, not production tested.
- t_{PD} is the same as t_{PHL} and t_{PLH}.
- Because of the higher capacitance at the Z terminal (16 switches to 1), the delay figures are higher at the Z terminal than at the Y terminal.
- t_{OFF} is the same as t_{PHZ} and t_{PLZ}.
- t_{ON} is the same as t_{PZH} and t_{PZL}.
- C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma\{(C_L + C_{SW}) \times V_{CC}^2 \times f_o\}$$

where:

f_i = Input frequency in MHz.

f_o = Output frequency in MHz.

C_L = Output load capacitance in pF.

C_{SW} = Switch capacitance in pF.

V_{CC} = Supply voltage in Volts.

Σ{(C_L + C_{SW}) × V_{CC}² × f_o} = Sum of outputs.

DYNAMIC CHARACTERISTICS (continued)

($T_A = +25^\circ\text{C}$, $\text{GND} = 0\text{V}$. V_I equals either V_{IH} or V_{IL} . V_{IS} represents the input voltage at either the Y_n or Z terminal, depending on which is designated as an input. V_{OS} represents the output voltage at either the Y_n or Z terminal, depending on which is designated as an output.)

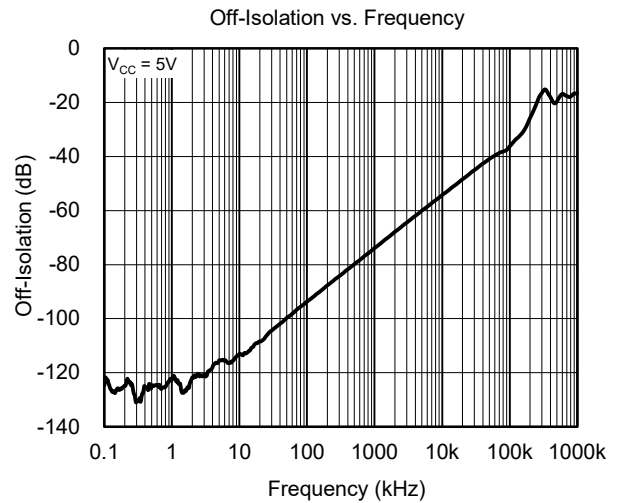
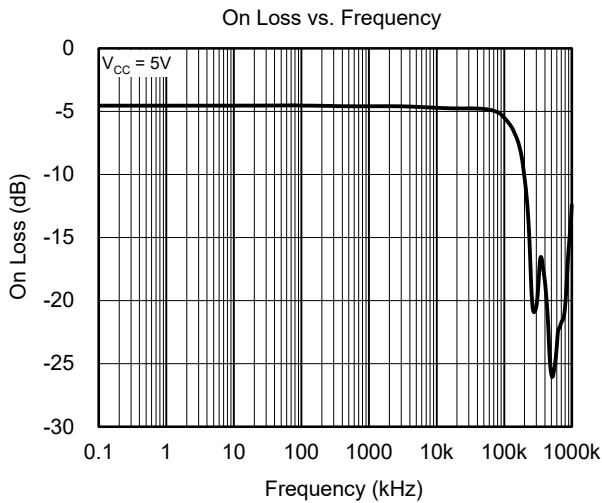
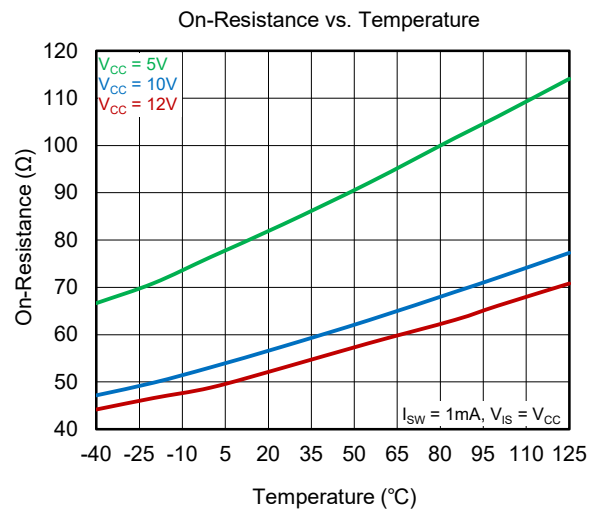
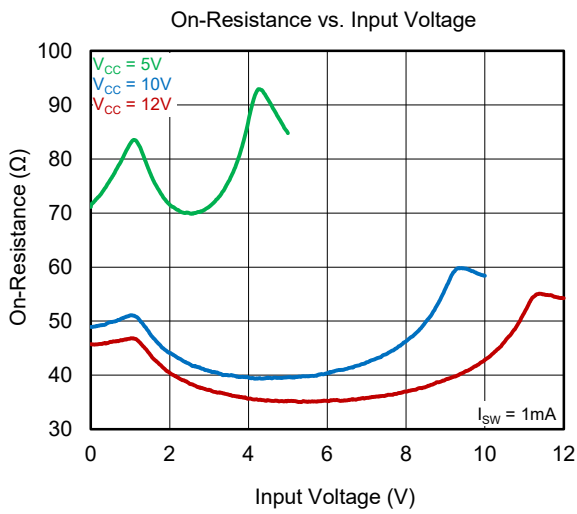
PARAMETER	SYMBOL	CONDITIONS	TEMP	MIN	TYP	MAX	UNITS
For 74HC4067							
Total Harmonic Distortion	THD	$R_L = 10\text{k}\Omega$, $f_i = 1\text{kHz}$, see Figure 4	$V_{CC} = 5\text{V}$, $V_{IS_P-P} = 4.5\text{V}$	$+25^\circ\text{C}$	0.16		%
			$V_{CC} = 10\text{V}$, $V_{IS_P-P} = 9.0\text{V}$	$+25^\circ\text{C}$	0.12		
		$R_L = 10\text{k}\Omega$, $f_i = 10\text{kHz}$, see Figure 4	$V_{CC} = 5\text{V}$, $V_{IS_P-P} = 4.5\text{V}$	$+25^\circ\text{C}$	0.16		%
			$V_{CC} = 10\text{V}$, $V_{IS_P-P} = 9.0\text{V}$	$+25^\circ\text{C}$	0.12		
Isolation (Off-State) ⁽¹⁾	α_{ISO}	$R_L = 50\Omega$, $C_L = 50\text{pF}$, $f = 10\text{MHz}$, see Figure 5	$V_{CC} = 5\text{V}$	$+25^\circ\text{C}$	-55		dB
			$V_{CC} = 10\text{V}$	$+25^\circ\text{C}$	-55		
-3dB Bandwidth ⁽¹⁾	f_{-3dB}	$R_L = 50\Omega$, $C_L = 10\text{pF}$, see Figure 6	$V_{CC} = 5\text{V}$	$+25^\circ\text{C}$	150		MHz
			$V_{CC} = 10\text{V}$	$+25^\circ\text{C}$	200		
Switch Capacitance	C_{SW}	Individual pins Y_n	$+25^\circ\text{C}$	5		pF	
		Common pin Z	$+25^\circ\text{C}$	25			
Input Capacitance	C_I		$+25^\circ\text{C}$	4		pF	
For 74HCT4067							
Total Harmonic Distortion	THD	$R_L = 10\text{k}\Omega$, $f_i = 1\text{kHz}$, see Figure 4	$V_{CC} = 5\text{V}$, $V_{IS_P-P} = 4.5\text{V}$	$+25^\circ\text{C}$	0.16		%
			$V_{CC} = 5\text{V}$, $V_{IS_P-P} = 4.5\text{V}$	$+25^\circ\text{C}$	0.16		
Isolation (Off-State) ⁽¹⁾	α_{ISO}	$R_L = 50\Omega$, $C_L = 50\text{pF}$, $f = 10\text{MHz}$, see Figure 5	$V_{CC} = 5\text{V}$	$+25^\circ\text{C}$	-55		dB
-3dB Bandwidth ⁽¹⁾	f_{-3dB}	$R_L = 50\Omega$, $C_L = 10\text{pF}$, see Figure 6	$V_{CC} = 5\text{V}$	$+25^\circ\text{C}$	150		MHz
Switch Capacitance	C_{SW}	Individual pins Y_n	$+25^\circ\text{C}$	5		pF	
		Common pin Z	$+25^\circ\text{C}$	25			
Input Capacitance	C_I		$+25^\circ\text{C}$	4		pF	

NOTE:

- Set input voltage $V_{IS} = 0\text{dBm}$ ($0\text{dBm} = 1\text{mW}$ for 50Ω).

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = +25°C, unless otherwise noted.



TEST CIRCUITS

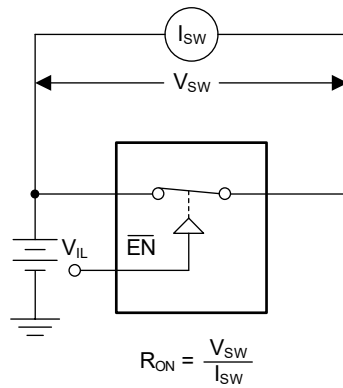


Figure 1. Test Circuit for Measuring On-Resistance

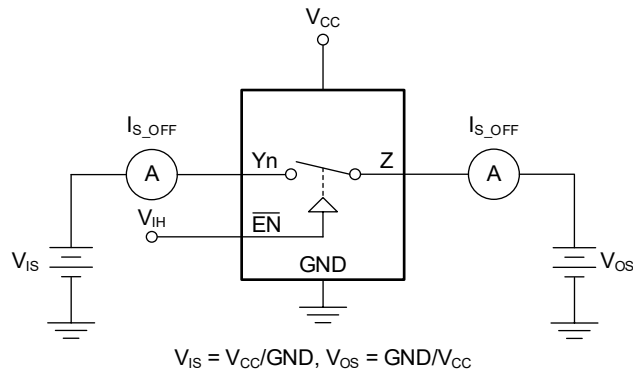


Figure 2. Test Circuit for Measuring Off-State Leakage Current

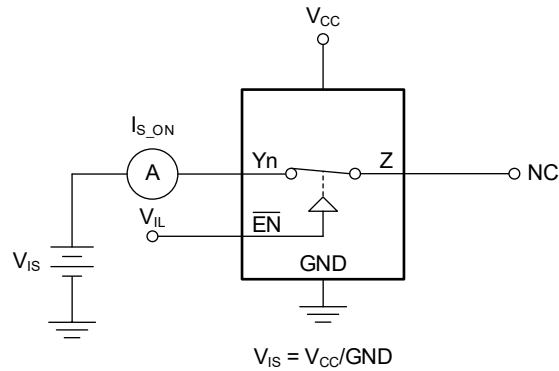


Figure 3. Test Circuit for Measuring On-State Leakage Current

TEST CIRCUITS (continued)

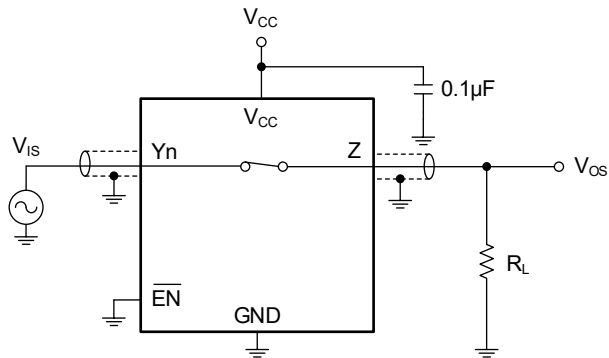
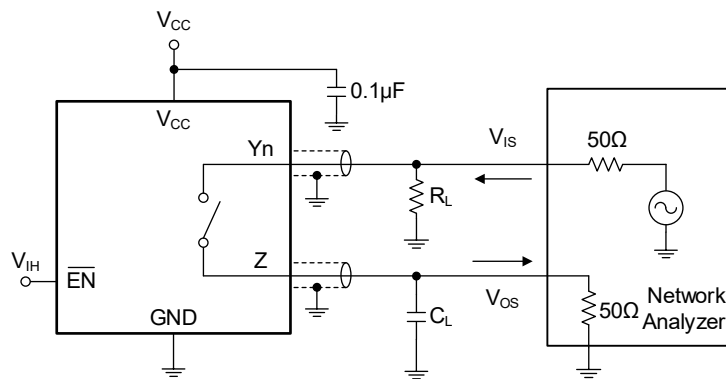


Figure 4. Test Circuit for Measuring Total Harmonic Distortion



$$\text{Off-Isolation} = 20\log(V_{OS}/V_{IS})$$

Figure 5. Test Circuit for Measuring Isolation (Off-State)

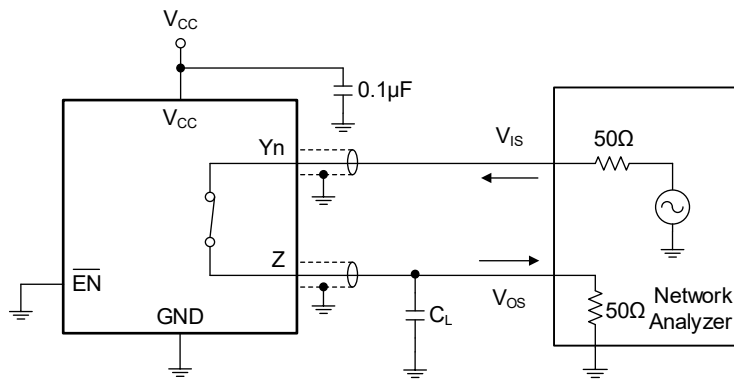
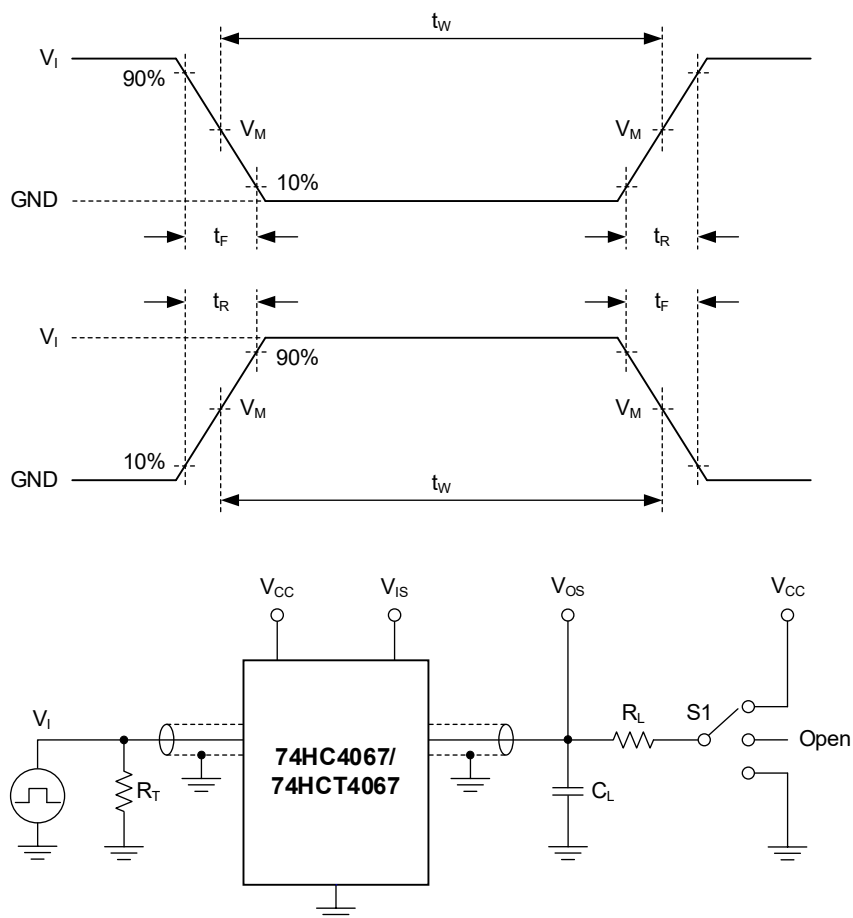


Figure 6. Test Circuit for Measuring -3dB Bandwidth

TEST CIRCUITS (continued)



Test conditions are given in Table 1.

Definitions test circuit:

R_L : Load resistance.

C_L : Load capacitance (includes jig and probe).

R_T : Termination resistance (equals to output impedance Z_O of the pulse generator).

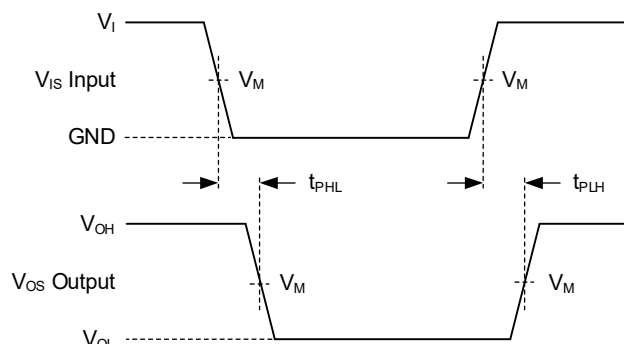
S1: Test selection switch.

Figure 7. Test Circuit for Measuring Switching Times

Table 1. Test Conditions

TEST	INPUT				OUTPUT		S1 POSITION
	CONTROL $\bar{E}N$	ADDRESS S_n	SWITCH $Y_n (Z)$	t_R, t_F	SWITCH $Z (Y_n)$		
	V_I	V_I	V_{IS}		C_L	R_L	
t_{PHL}, t_{PLH}	GND	GND or V_{CC}	GND to V_{CC}	$\leq 6ns$	50pF	—	Open
t_{PHZ}, t_{PZH}	GND to V_{CC}	GND to V_{CC}	V_{CC}	$\leq 6ns$	50pF	1k Ω	GND
t_{PLZ}, t_{PZL}	GND to V_{CC}	GND to V_{CC}	GND	$\leq 6ns$	50pF	1k Ω	V_{CC}

WAVEFORMS

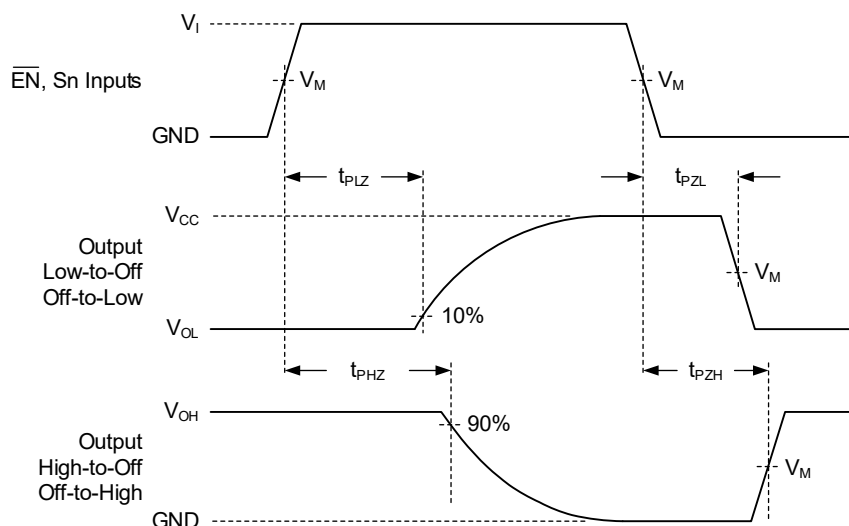


Test conditions are given in Table 1.

Measurement points are given in Table 2.

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Figure 8. Input (V_I) to Output (V_{Os}) Propagation Delay Times



Test conditions are given in Table 1.

Measurement points are given in Table 2.

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Figure 9. Turn-On and Turn-Off Times

Table 2. Measurement Points

TYPE	INPUT		OUTPUT
	V_I	$V_M^{(1)}$	V_M
74HC4067	V_{CC}	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$
74HCT4067	3.0 V	1.3V	1.3V

NOTE:

1. The measurement points should be V_{IH} or V_{IL} when the input rising or falling time exceeds 6ns.

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

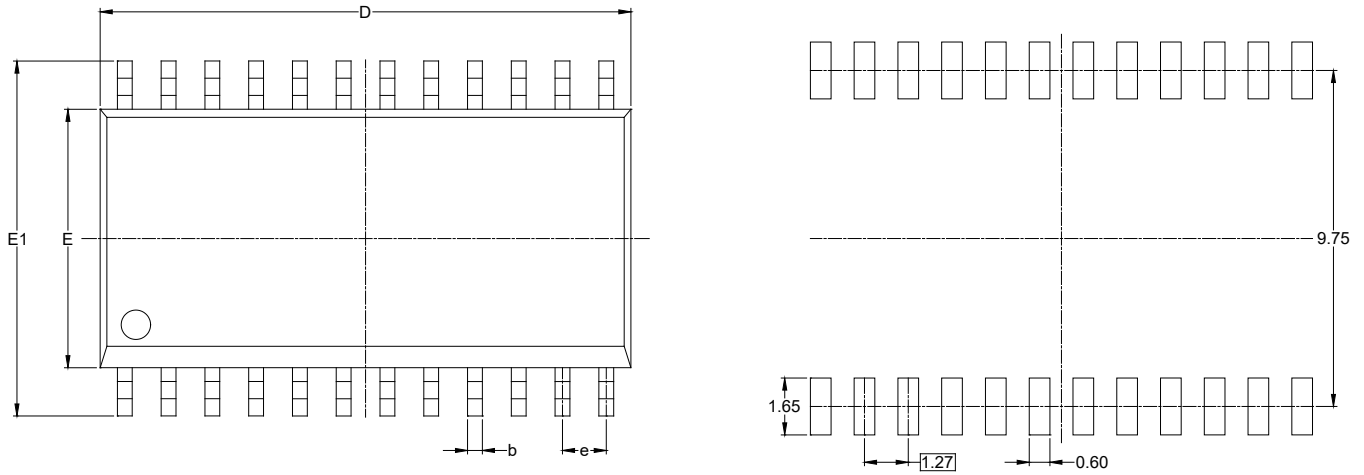
FEBRUARY 2026 – REV.A to REV.A.1	Page
Added TSSOP-24 and TQFN-3.5x5.5-24BL packages	All

Changes from Original to REV.A (SEPTEMBER 2025)	Page
Changed from product preview to production data	All

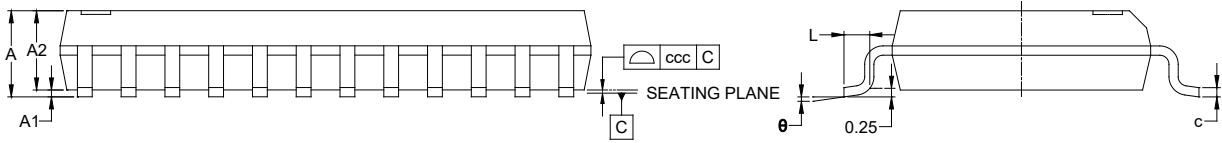
PACKAGE INFORMATION

PACKAGE OUTLINE DIMENSIONS

SOIC-24



RECOMMENDED LAND PATTERN (Unit: mm)



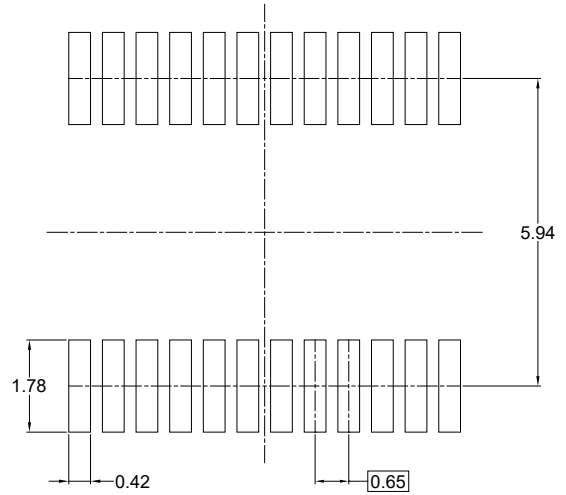
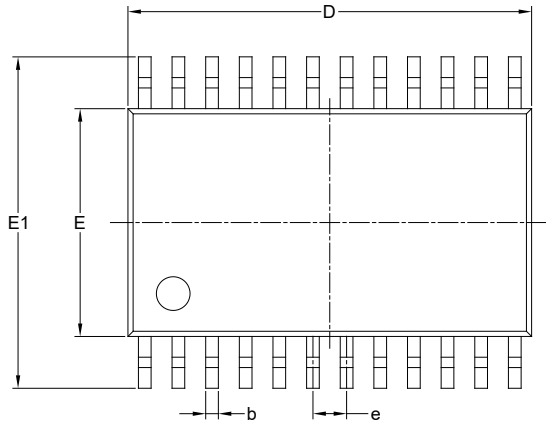
Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	-	-	2.650
A1	0.100	-	0.300
A2	2.300 REF		
b	0.310	-	0.510
c	0.200	-	0.330
D	15.300	-	15.500
E	7.400	-	7.600
E1	10.000	-	10.600
e	1.270 BSC		
L	0.400	-	1.270
theta	0°	-	8°
ccc	0.100		

NOTES:

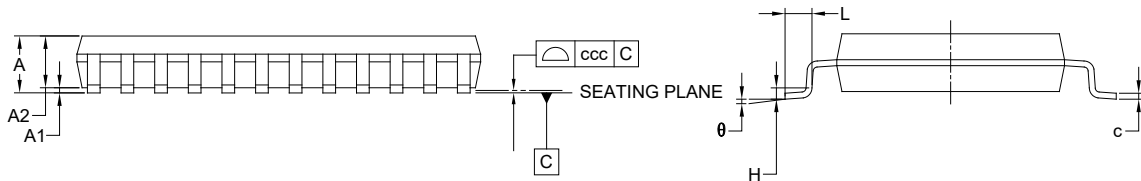
1. This drawing is subject to change without notice.
2. The dimensions do not include mold flashes, protrusions or gate burrs.
3. Reference JEDEC MS-013.

PACKAGE OUTLINE DIMENSIONS

TSSOP-24



RECOMMENDED LAND PATTERN (Unit: mm)



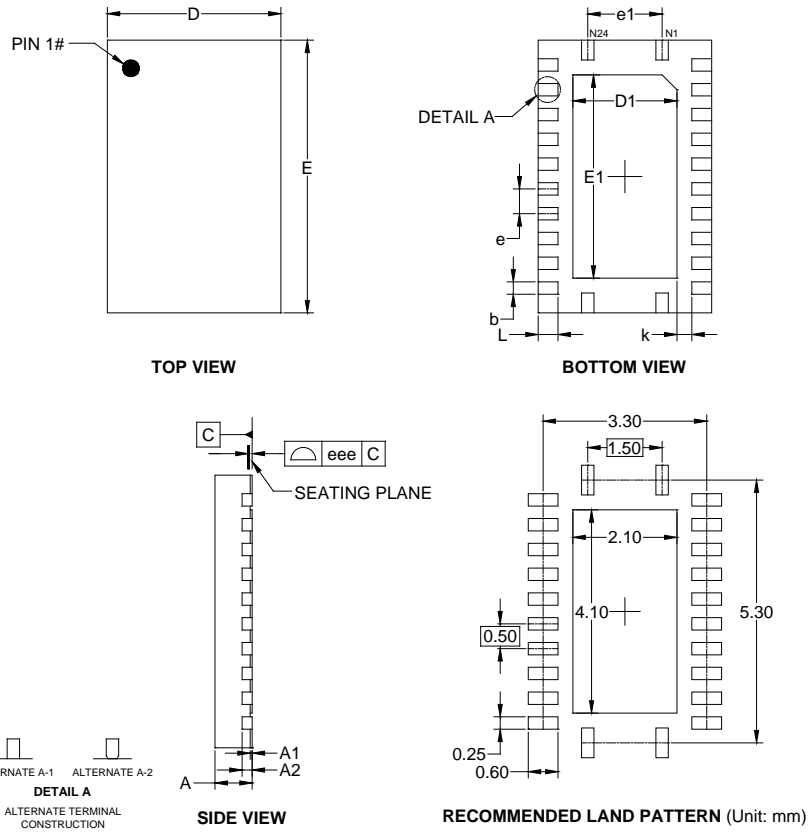
Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	-	-	1.200
A1	0.050	-	0.150
A2	0.800	-	1.050
b	0.190	-	0.300
c	0.090	-	0.200
D	7.700	-	7.900
E	4.300	-	4.500
E1	6.200	-	6.600
e	0.650 BSC		
L	0.450	-	0.750
H	0.250 TYP		
θ	0°	-	8°
ccc	0.100		

NOTES:

1. This drawing is subject to change without notice.
2. The dimensions do not include mold flashes, protrusions or gate burrs.
3. Reference JEDEC MO-153.

PACKAGE OUTLINE DIMENSIONS

TQFN-3.5x5.5-24BL



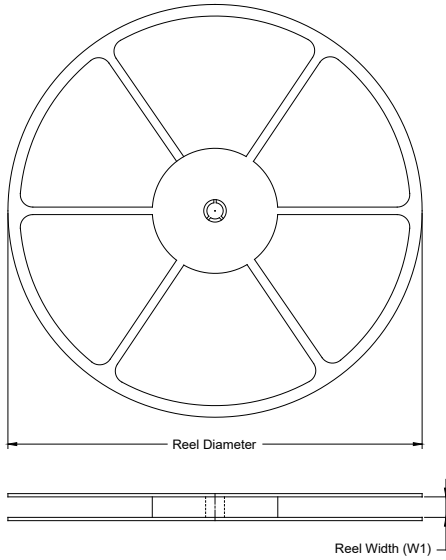
Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	0.700	-	0.800
A1	0.000	-	0.050
A2	0.203 REF		
b	0.200	-	0.300
D	3.400	-	3.600
D1	2.000	-	2.200
E	5.400	-	5.600
E1	4.000	-	4.200
e	0.500 BSC		
e1	1.500 BSC		
L	0.300	-	0.500
k	0.300 REF		
eee	0.080		

NOTE: This drawing is subject to change without notice.

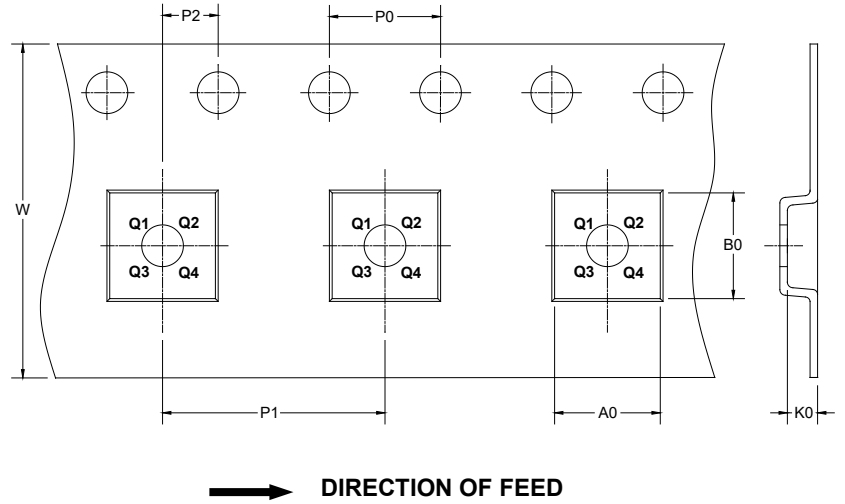
PACKAGE INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

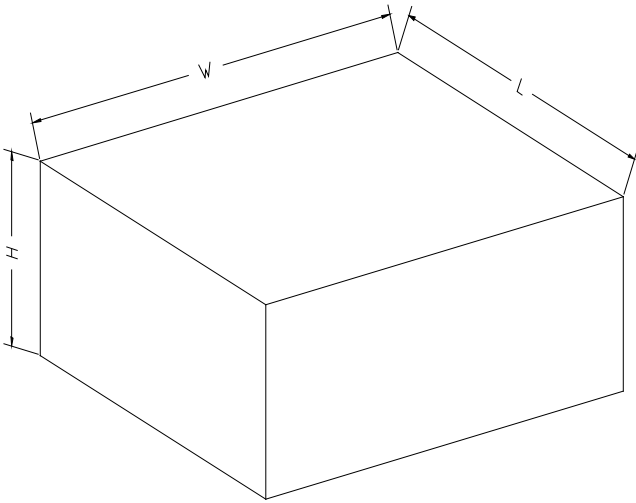
KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
SOIC-24	13"	24.4	10.80	15.90	3.00	4.0	12.0	2.0	24.0	Q1
TSSOP-24	13"	16.4	6.80	8.30	1.60	4.0	8.0	2.0	16.0	Q1
TQFN-3.5×5.5-24BL	13"	12.4	3.80	5.80	1.00	4.0	8.0	2.0	12.0	Q1

DD0001

PACKAGE INFORMATION

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13"	386	280	370	5

DD0002