# TD24C512-C1
# 512-Kbit I²C Serial EEPROM 8-Ball WLCSP

## GENERAL DESCRIPTION

The TD24C512-C1 is a 512-Kbit I²C-compatible serial EEPROM device. The device is designed to operate in a supply voltage range of 1.7V to 5.5V, with a maximum of 1MHz transfer rate, over an operating temperature range of -40℃ to +125℃. The device incorporates a Write Protection pin used for hardware Write Protection on the whole memory array, and offers Software Write Protection feature for users to write-protect the memory by blocks.

The serial EEPROM memory is organized as 512 pages of 128 bytes each, totaling 65536 × 8 bits. The device offers an additional 128-byte Identification Page for users to store sensitive application parameters. This page can be permanently locked in Read-only mode after the application data is written into this Page. The device also offers a separate memory block containing a factory programmed 128-bit Unique ID. This block is in Read-only mode and can be accessed by sending a specific Read command.

The TD24C512-C1 is delivered in a WLCSP-1.5×1.53-8B package.

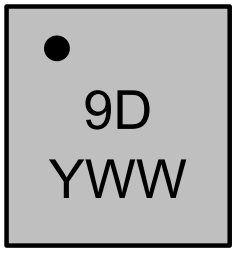
## FEATURES

- **Supply Voltage Range: 1.7V to 5.5V**
- **2-wire Serial Interface I²C Compatible**
  - **400kHz and High Speed 1MHz Transfer Rate Compatibility**
- **Byte and Page (up to 128 Bytes) Write Mode**
  - **Partial Page Write Allowed**
- **Self-timed Write Cycle (3ms MAX)**
- **Software Write Protection by Blocks**
  - **Quarter, Half or Whole Memory Array**
- **Hardware Write Protection on the Whole Memory Array**
- **Additional 128-byte Write Lockable Page and 128-bit Unique ID**
- **Schmitt Trigger, Filtered Inputs for Noise Suppression**
- **Low Operating Current**
  - **Write Current: 1mA (MAX)**
  - **Read Current: 0.5mA (MAX)**
  - **Standby Current: 2μA (MAX)**
- **High Reliability**
  - **Endurance: 1,000,000 Write Cycles at $T_A$ = +25℃**
  - **Data Retention: 100 Years at $T_A$ = +25℃**
  - **ESD Protection (HBM): 6000V**
- **Operating Temperature Range: -40℃ to +125℃**
- **RoHS Compliant and Halogen Free**
- **Available in a Green WLCSP-1.5×1.53-8B Package**

# PACKAGE/ORDERING INFORMATION

| MODEL | PACKAGE DESCRIPTION | SPECIFIED TEMPERATURE RANGE | ORDERING NUMBER | PACKAGE MARKING | PACKING OPTION |
|---|---|---|---|---|---|
| TD24C512-C1 | WLCSP-1.5×1.53-8B | -40℃ to +125℃ | TD24C512-C3LP1TR | 9D<br>YWW | Tape and Reel, 4000 |

## MARKING INFORMATION




9D: TD24C512-C3LP1

YWW: Date Code, Y = year, WW = week

*Example*: 410 = year 2024, week 10

Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

## ABSOLUTE MAXIMUM RATINGS

Supply Voltage, $V_{CC}$ ..... -0.5V to 6V
Voltage on Input Pins ..... -0.5V to 6V
Ambient Temperature with Power Applied ... -55℃ to +130℃
Storage Temperature Range ..... -65℃ to +150℃
ESD Susceptibility

HBM ..... 6000V

## RECOMMENDED OPERATING CONDITIONS

Operating Ambient Temperature Range ..... -40℃ to +125℃

## OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

## ESD SENSITIVITY CAUTION

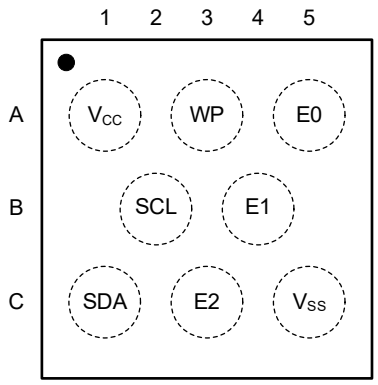
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

## DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

## PIN CONFIGURATION

(TOP VIEW)




WLCSP-1.5×1.53-8B

## PIN DESCRIPTION

| NAME | TYPE | FUNCTION |
|---|---|---|
| E0<br>E1<br>E2 | Input | Device Address Inputs. The E0, E1, and E2 pins are device address inputs for compatibility with other 2-wire serial EEPROM devices. These pins can be directly connected to $V_{CC}$ or GND in any combination, allowing up to eight devices on a single bus system.<br>If these pins are left floating, the E0, E1, and E2 pins will be internally pulled down to GND. |
| SDA | Input/Output | Serial Data. The SDA pin is an open-drain bidirectional input/output pin used to serially transfer data to and from the device. |
| SCL | Input | Serial Clock. The SCL pin is used to provide a clock to the device and is used to control the flow of data to and from the device. Command and input data present on the SDA pin is always latched in on the rising edge of SCL, while output data on the SDA pin is always clocked out on the falling edge of SCL. |
| $V_{CC}$ | Power | Device Power Supply. The $V_{CC}$ pin is used to supply the source voltage to the device. Operations at invalid $V_{CC}$ voltages may produce spurious results and should not be attempted. |
| $V_{SS}$ | Ground | Ground. The ground reference for the power supply. $V_{SS}$ should be connected to the system ground. |
| WP | Input | Write Protection. The WP pin is used to write protect the entire contents of the memory. When the WP pin is connected to Power Supply, the entire memory array becomes Write-protected, that is, the device becomes Read-only. When the WP pin is connected to GND, Write operations are enabled. If the pin is left floating, the WP pin will be internally pulled down to GND.<br>When the WP pin is driven high, the device address byte and the word address bytes are acknowledged, data bytes are not acknowledged. |

# ELECTRICAL CHARACTERISTICS

## DC Characteristics

(Operating range: $T_A$ = -40℃ to +125℃, $V_{CC}$ = 1.7V to 5.5V, unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | MAX | UNITS |
|---|---|---|---|---|---|
| Supply Voltage | $V_{CC}$ | | 1.7 | 5.5 | V |
| Supply Current (Read) | $I_{CC1}$ | $V_{CC}$ = 1.7V, Read at 1MHz | | 0.2 | mA |
| | | $V_{CC}$ = 5.5V, Read at 400 kHz | | 0.4 | |
| | | $V_{CC}$ = 5.5V, Read at 1MHz | | 0.5 | |
| Supply Current (Write) | $I_{CC2}$ | $V_{CC}$ = 1.7V, Write at 400 kHz | | 0.5 | mA |
| | | $V_{CC}$ = 5.5V, Write at 400 kHz | | 1 | |
| Standby Current | $I_{SB}$ | $V_{CC}$ = 1.7V, $V_{IN}$ = $V_{CC}$ or GND | | 1 | μA |
| | | $V_{CC}$ = 5.5V, $V_{IN}$ = $V_{CC}$ or GND | | 2 | |
| Input Leakage Current | $I_{LI}$ | $V_{IN}$ = $V_{CC}$ or GND | | 1 | μA |
| Output Leakage Current | $I_{LO}$ | $V_{OUT}$ = $V_{CC}$ or GND | | 1 | μA |
| Input Low-Level Voltage (SDA, SCL) | $V_{IL}$ | | -0.5 | 0.3 × $V_{CC}$ | V |
| Input High-Level Voltage (SDA, SCL) | $V_{IH}$ | | 0.7 × $V_{CC}$ | $V_{CC}$ + 0.5 | V |
| Low-Level Output Voltage | $V_{OL1}$ | $V_{CC}$ > 2V, $I_{OL}$ = 3mA | | 0.4 | V |
| Low-Level Output Voltage | $V_{OL2}$ | $V_{CC}$ ≤ 2V, $I_{OL}$ = 2mA | | 0.2 | V |

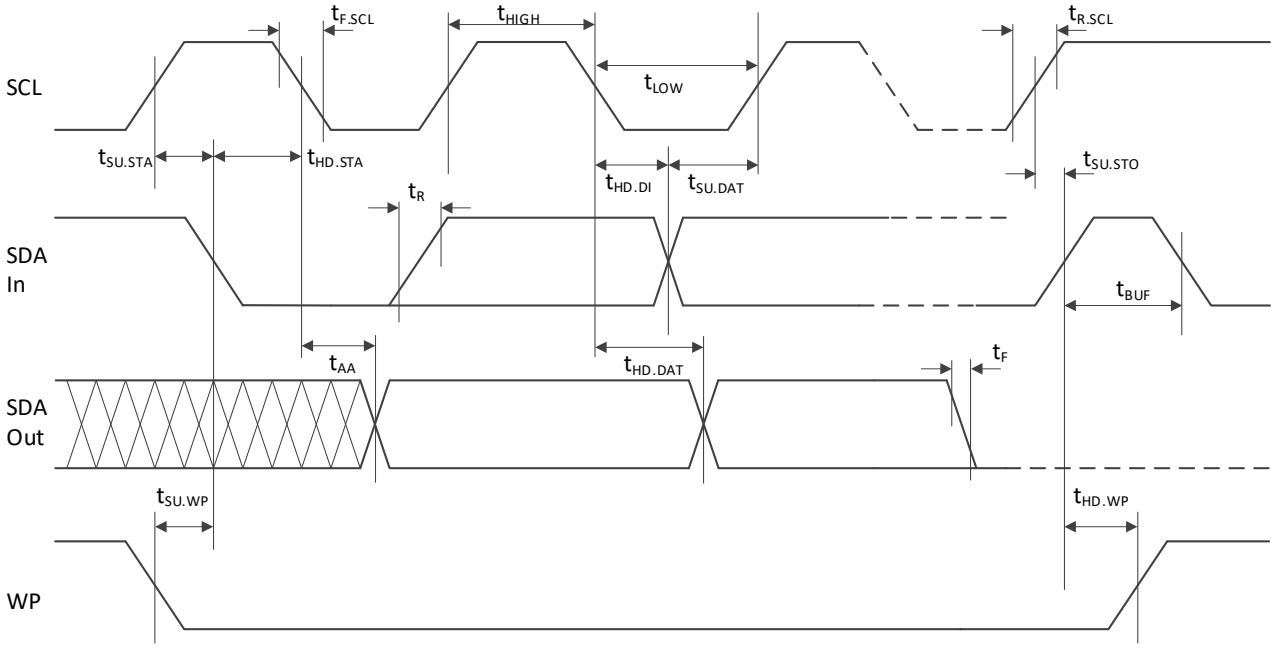
## AC Characteristics

(Operating range: $T_A$ = -40℃ to +125℃, $V_{CC}$ = 1.7V to 5.5V, $C_L$ = 100pF. Measurement conditions: input rise and fall time ≤ 50ns, input pulse voltages: 0.2 × $V_{CC}$ to 0.8 × $V_{CC}$; input and output timing reference voltages: 0.3 × $V_{CC}$ to 0.7 × $V_{CC}$, unless otherwise noted.)

| PARAMETER | SYMBOL | FAST MODE $V_{CC}$ = 1.7V to 5.5V | | HIGH SPEED MODE $V_{CC}$ = 1.7V to 5.5V | | UNITS |
|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | |
| Clock Frequency, SCL | $f_{SCL}$ | | 400 | | 1000 | kHz |
| Clock Pulse Width Low | $t_{LOW}$ | 1300 | | 600 | | ns |
| Clock Pulse Width High | $t_{HIGH}$ | 600 | | 260 | | ns |
| SDA Rise Time | $t_R$ (1) | | 300 | | 300 | ns |
| SDA (Out) Fall Time | $t_F$ (1) | | 300 | | 100 | ns |
| Start Hold Time | $t_{HD.STA}$ | 600 | | 250 | | ns |
| Start Setup Time | $t_{SU.STA}$ | 600 | | 250 | | ns |
| Stop Setup Time | $t_{SU.STO}$ | 600 | | 250 | | ns |
| Bus Free Time between Stop and Next Start | $t_{BUF}$ | 1300 | | 500 | | ns |
| Data In Hold Time | $t_{HD.DI}$ | 0 | | 0 | | ns |
| Data In Setup Time | $t_{SU.DAT}$ | 100 | | 50 | | ns |
| Data Out Hold Time | $t_{HD.DAT}$ | 50 | | 50 | | ns |
| SCL Low to Data Out Valid | $t_{AA}$ | 100 | 900 | 50 | 500 | ns |
| WP Pin Setup Time | $t_{SU.WP}$ | 1200 | | 600 | | ns |
| WP Pin Hold Time | $t_{HD.WP}$ | 1200 | | 600 | | ns |
| Write Cycle Time | $t_{WR}$ | | 3 | | 3 | ms |
| Noise Suppression Time | $t_I$ | | 50 | | 50 | ns |

NOTE: 1.This parameter is ensured by characterization only.

## ELECTRICAL CHARACTERISTICS (continued)




### Pin Capacitance

(Operating range for pin capacitance: $T_A$ = +25℃, $f_C$ = 1MHz, $V_{CC}$ = 1.7V to 5.5V.)

| PARAMETER (1) | SYMBOL | CONDITIONS | MAX | UNITS |
|---|---|---|---|---|
| Input/output Capacitance (SDA) | $C_{I/O}$ | $V_{I/O}$ = 0V | 8 | pF |
| Input Capacitance (Other Pins) | $C_{IN}$ | $V_{IN}$ = 0V | 6 | pF |

NOTE: 1. These parameters are ensured by characterization only.

### Reliability Characteristics

| PARAMETER | SYMBOL | CONDITIONS | MIN | UNITS |
|---|---|---|---|---|
| Write Cycle Endurance | $N_W$ | $T_A$ = +25℃, Page mode | $1 \times 10^6$ | cycle |
| | | $T_A$ = +125℃, Page mode | $1 \times 10^5$ | |
| Data Retention | $D_R$ | $T_A$ = +25℃ | 100 | year |

## FUNCTIONAL BLOCK DIAGRAM

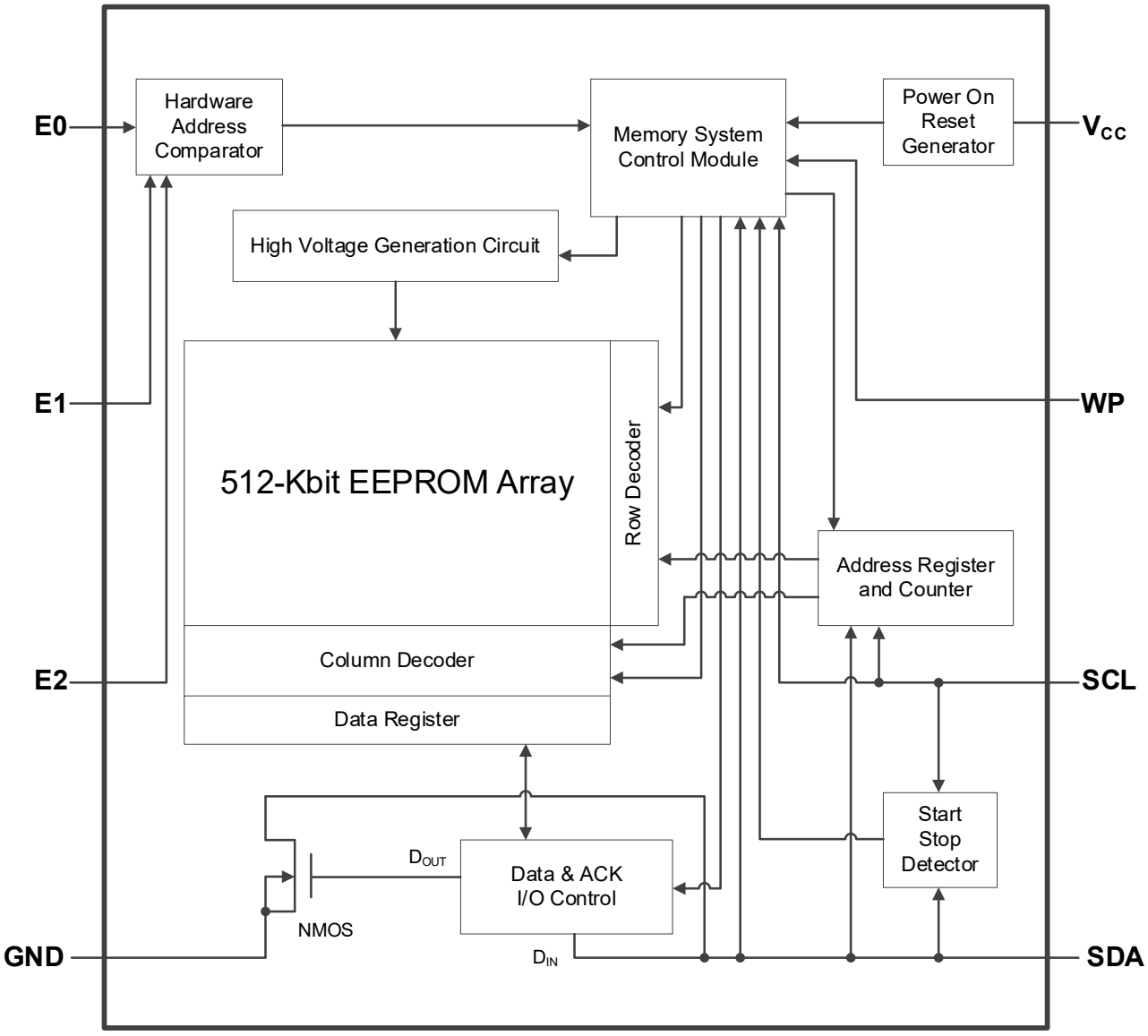



**Figure 1. Block Diagram**

# DEVICE COMMUNICATION

The TD24C512-C1 operates as a slave device and utilizes a 2-wire serial interface to communicate with the Master. The Master initiates and controls all Read and Write operations to the slave devices on the serial bus, and both the Master and the slave devices can transmit and receive data on the bus.

The serial interface is comprised of just two signal lines: the Serial Clock (SCL) and the Serial Data (SDA). Data is always latched into the TD24C512-C1 on the rising edge of SCL and is always output from the device on the falling edge of SCL. Both the SCL pin and SDA pin incorporate integrated spike suppression filters and Schmitt Triggers to minimize the effects of input spikes and bus noise.

All command and data information is transferred with the Most Significant Bit (MSB) first. During the bus communication, one data bit is transmitted every clock cycle, and after eight bits of data has been transferred, the receiving device must respond with an acknowledge or a no-acknowledge response bit during a ninth clock cycle generated by the Master. Therefore, nine clock cycles are required for every one byte of data transferred. There is no unused clock cycle during any Read or Write operation, so there must not be any interruptions or breaks during the data stream.

During data transfers, data on the SDA pin must only change while SCL is low, and the data must remain stable while SCL is high. If data on the SDA pin changes while SCL is high, then either a Start or a Stop condition will occur. The number of data bytes transferred between a Start and a Stop condition is not limited and is determined by the Master.

## Start Condition

A Start condition occurs when there is a high-to-low transition on the SDA pin while the SCL pin is stable in Logic 1 state. The Start condition must precede any command as the Master uses a Start condition to initiate any data transfer sequence (see Figure 2). The TD24C512-C1 will continuously monitor the SDA and SCL pins for a Start condition, and the device will not respond unless one is given.

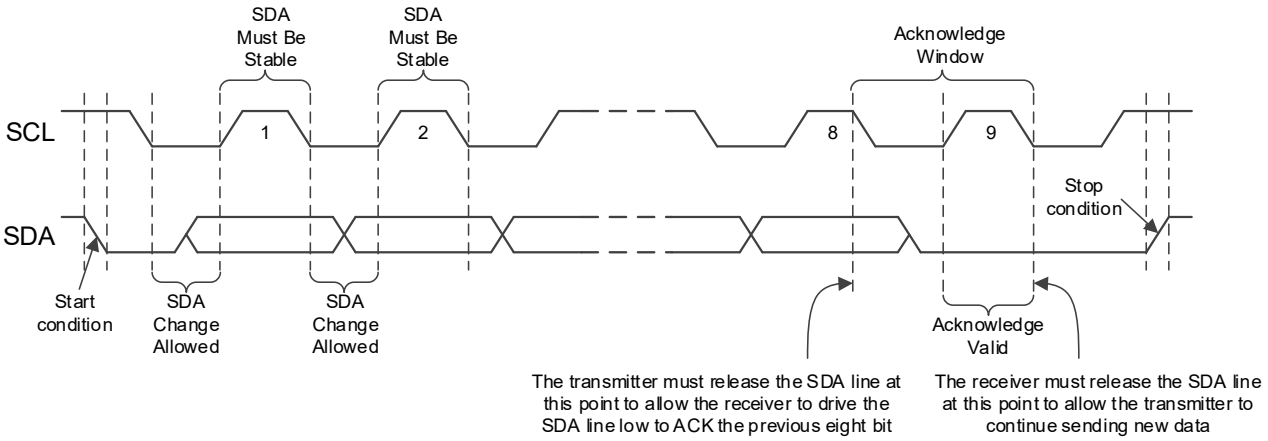



**Figure 2. Start, Stop, and ACK**

## Stop Condition

A Stop condition occurs when there is a low-to-high transition on the SDA pin while the SCL pin is stable in Logic 1 state (see Figure 2). A stop condition terminates communication between the TD24C512-C1 and the Master. A Stop condition at the end of a Write command triggers the EEPROM internal write cycle. Otherwise, the TD24C512-C1 subsequently returns to Standby mode after receiving a Stop condition.

## Acknowledge (ACK)

After each byte of data is received, the TD24C512-C1 should acknowledge to the Master that it has received the data byte successfully. This is accomplished by the Master first releasing the SDA line and providing the ACK/NACK clock cycle (a ninth clock cycle for every byte). During the ACK/NACK clock cycle, the TD24C512-C1 must output Logic 0 as ACK for the entire clock cycle so that the SDA line must be stable in Logic 0 state during the entire high period of the clock cycle (see Figure 2).

# DEVICE COMMUNICATION (continued)

## Standby Mode

The TD24C512-C1 features a low-power Standby mode which is enabled:

(1) Upon power-up;

(2) After the receipt of a Stop condition in Read operation;

(3) The completion of any internal operations.

## Software Reset

After an interruption in protocol, power loss, or system reset, any 2-wire part can be reset by following these steps: (1) Create a Start condition; (2) Clock nine cycles; (3) Create another Start condition followed by a Stop condition (see Figure 3).

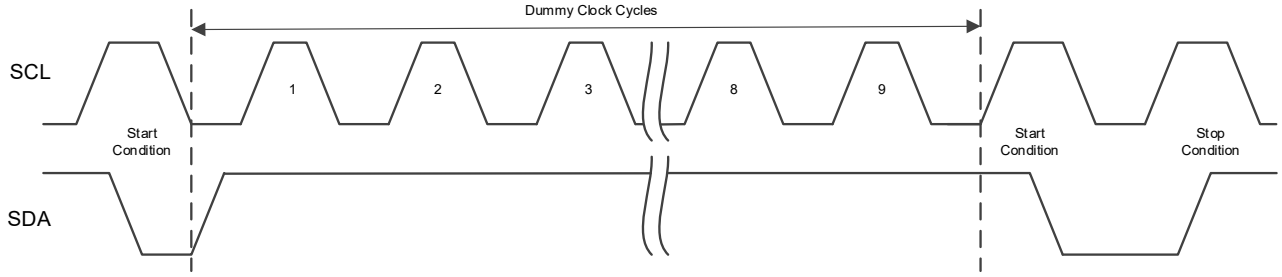



**Figure 3. 2-wire Software Reset**

## Device Reset and Initialization

The TD24C512-C1 incorporates a Power-On Reset (POR) circuit to prevent inadvertent operations during power-up. On a cold power-up, the device does not respond to any instructions until the supply voltage reaches the internal power-on reset threshold voltage ($V_{POR}$). The supply voltage must rise continuously between $V_{POR}$ and $V_{CC}$ (MIN) without any ring back to ensure a proper power-up. Once the supply voltage passes $V_{POR}$, the device is reset and enters Standby mode. However, no protocol should be issued to the device until a valid and stable supply voltage is applied for the time specified by the $t_{INIT}$ parameter. The supply voltage must remain stable and valid until the end of the protocol transmission, and for a Write instruction, until the end of the internal write cycle (see Figure 4).

This POR behavior is bi-directional. It protects the TD24C512-C1 against brown-out failure caused by a temporary loss of power. In a similar way, as soon as the supply voltage drops below the internal brown-out reset threshold voltage ($V_{BOR}$), the device is reset and stops responding to any instructions (see Figure 4). The $V_{BOR}$ level is set below the $V_{POR}$ level.

Parameters related to power-up and power-down conditions are listed in Table 1.

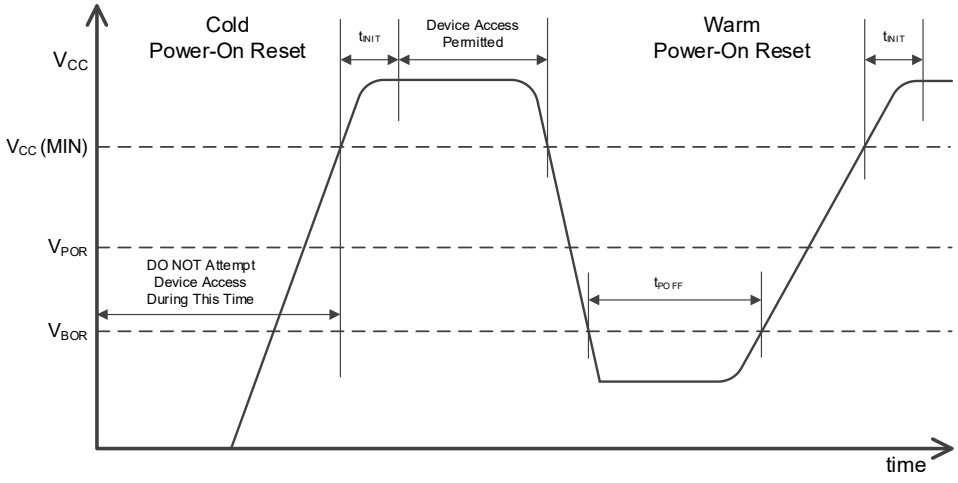



**Figure 4. Power-up and Power-down Timing**

# DEVICE COMMUNICATION (continued)

**Table 1. Power-up and Power-down Conditions**

| PARAMETER | SYMBOL | MIN | MAX | UNITS |
|---|---|---|---|---|
| Power-On Reset Voltage | $V_{POR}$ | | 1.5 | V |
| Brown-Out Reset Voltage | $V_{BOR}$ | 1.2 | | V |
| Time from $V_{CC}$ (MIN) to First Command | $t_{INIT}$ | 100 | | μs |
| Warm Power Cycle Off Time | $t_{POFF}$ | 100 | | μs |

## Data Security

The TD24C512-C1 incorporates a hardware data protection feature that allows the user to write protect the whole memory array (and Identification Page) when the WP pin is connected directly to $V_{CC}$.

The TD24C512-C1 also offers a Software Write Protection (SWP) feature that allows the user to write protect the memory array by blocks when writing specific values in the internal non-volatile SWP register (see ***Write Software Write Protection (SWP) Register*** for details).

# DEVICE ADDRESSING

The TD24C512-C1 requires a 7-bit device address and a Read/Write select bit following a Start condition from the Master to initiate communication with the Serial EEPROM. The device address byte is comprised of a 4-bit device type identifier followed by three device address bits (E2, E1, and E0) and a R/$\overline{W}$ select bit and is clocked by the Master on the SDA pin with the most significant bit (MSB, bit 7) first.

The TD24C512-C1 will respond to two unique device type identifiers. The device type identifier of '1010' is necessary to select the device memory for normal Read or Write operation. The device type identifier of '1011' is used (1) to select the Identification Page for Read or Write/Lock operation; (2) to select the Software Write Protection register for Read or Write operation; (3) for Read Unique ID (see Table 2).

The software device address bits (E2, E1 and E0) must match their corresponding hard-wired device address inputs (E2, E1 and E0), allowing up to eight devices on the bus at the same time. The eighth bit of the address byte is the R/$\overline{W}$ operation selection bit. A Read operation is selected if this bit is Logic 1, and a Write operation is selected if this bit is Logic 0. Upon a compare of the device address byte, the device outputs an ACK or an NACK during the ninth clock cycle if the compare is true or not true, respectively. The device will return to the low-power Standby mode after an NACK.

Once the TD24C512-C1 has acknowledged the device address byte, the device waits for the Master to send two word address bytes (first word address byte sent first, followed by the second word address byte) for a certain Read or Write instruction according to Table 3. The TD24C512-C1 responds to each address byte with an ACK.

**Table 2. TD24C512-C1 Device Address Byte**

| FUNCTION | DEVICE TYPE IDENTIFIER | | | | DEVICE ADDRESS | | | READ/WRITE |
|---|---|---|---|---|---|---|---|---|
| | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
| When accessing the 512-Kbit memory array | 1 | 0 | 1 | 0 | E2 | E1 | E0 | R/W |
| When accessing the Identification Page | 1 | 0 | 1 | 1 | E2 | E1 | E0 | R/W |
| When accessing the Lock Identification Page bit | 1 | 0 | 1 | 1 | E2 | E1 | E0 | 0 |
| When accessing the Software Write Protection register | 1 | 0 | 1 | 1 | E2 | E1 | E0 | R/W |
| When accessing the Unique ID | 1 | 0 | 1 | 1 | E2 | E1 | E0 | 1 |

**Table 3. TD24C512-C1 Word Address Bits**

| FUNCTION | FIRST WORD ADDRESS BYTE | | | | | | | | SECOND WORD ADDRESS BYTE | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | BIT 15 | BIT 14 | BIT 13 | BIT 12 | BIT 11 | BIT 10 | BIT 9 | BIT 8 | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
| Random Read | A15 (1) | A14 | A13 | A12 | A11 | A10 | A9 | A8 | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 |
| Byte/Page Write | A15 | A14 | A13 | A12 | A11 | A10 | A9 | A8 | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 |
| Read Identification Page | X (2) | X | X | X | X | 0 | 0 | X | X | A6 | A5 | A4 | A3 | A2 | A1 | A0 |
| Write Identification Page | X | X | X | X | X | 0 | 0 | X | X | A6 | A5 | A4 | A3 | A2 | A1 | A0 |
| Lock Identification Page | X | X | X | X | X | 1 | 0 | X | X | X | X | X | X | X | X | X |
| Read Lock Status | X | X | X | X | X | 0 | 0 | X | X | X | X | X | X | X | X | X |
| Write Software Write Protection Register | X | X | X | X | X | 1 | 1 | X | X | X | X | X | X | X | X | X |
| Read SWP Register | X | X | X | X | X | 1 | 1 | X | X | X | X | X | X | X | X | X |
| Read Unique ID | X | X | X | X | X | 0 | 1 | X | X | X | X | X | A3 | A2 | A1 | A0 |

NOTES:

1. A = Significant address bit.
2. X = Bit is Don't Care.

# READ AND WRITE OPERATIONS

## Write Operations

### Byte Write

For a Byte Write operation, the Master sends a Start condition followed by the device type identifier of '1010', the device address bits and the R/$\overline{W}$ select bit set to Logic 0. The TD24C512-C1 responds with an ACK during the ninth clock cycle and waits for the Master to send two word address bytes (first word address byte and second word address byte). Then the device responds to each word address byte with an ACK. After receiving ACKs from the TD24C512-C1, the Master transmits one data byte. If the addressed location has been Write-protected, by WP pin connected to $V_{CC}$, the device responds with an NACK, and the location is not modified. If the addressed location is not Write-protected, by WP pin set to GND, the device will respond with an ACK (see Figure 5 and Figure 6). The Master ends the Byte Write sequence with a Stop condition during the 10th clock cycle to initiate the internally self-timed write cycle. A Stop condition issued during any other clock cycle during the Write operation will not trigger the internal write cycle.

Once the write cycle begins, the preloaded data word will be programmed in the amount of time not to exceed the $t_{WR}$ specification (see Figure 9). During the time, the Master should wait a fixed time by the $t_{WR}$ specification, or for time sensitive applications, an ACK polling routine can be implemented. All inputs are ignored by the device during the write cycle and the device will not respond until the write cycle is completed. The Serial EEPROM will increment its internal address counter each time a byte is written.

### Page Write

The 512-Kbit Serial EEPROM is capable of writing up to 128 data bytes at a time by executing the Page Write protocol sequence. A partial or full Page Write operation is initiated the same as a Byte Write operation except that the Master does not send a Stop condition after the first data word is clocked in. Instead, after the device has acknowledged to the first data word, the Master can transmit up to 127 more data words. The device responds with an ACK after each data word is received if the WP pin is set to GND while the device is not acknowledged to each data word and the addressed locations are not modified if the WP pin is connected to $V_{CC}$ (see Figure 7 and Figure 8). After the device acknowledges to the last data word, the Master should terminate the Page Write sequence with a Stop condition to start the internal write cycle. A Stop condition issued at any other clock cycle will not initiate the internally self-timed write cycle and the Write sequence will have to be repeated again. Once the write cycle begins, the data words should be programmed in the amount of time not exceeding the $t_{WR}$ specification (see Figure 9). During this time, the Master should wait a fixed time by the specified $t_{WR}$ parameter, or for time sensitive applications, an ACK polling routine can be implemented.

The lower seven bits of the word address are internally incremented following the receipt of each data word. The higher word address bits are not incremented, retaining the memory page row location. When the internally generated word address reaches the page boundary, then the following data word is placed at the beginning of the same page. If more than 128 data words are transmitted to the device, the data word address will roll over and the previous data will be overwritten. The address roll-over during a Write sequence is from the last byte of the current page to the first byte of the same page.

## READ AND WRITE OPERATIONS (continued)

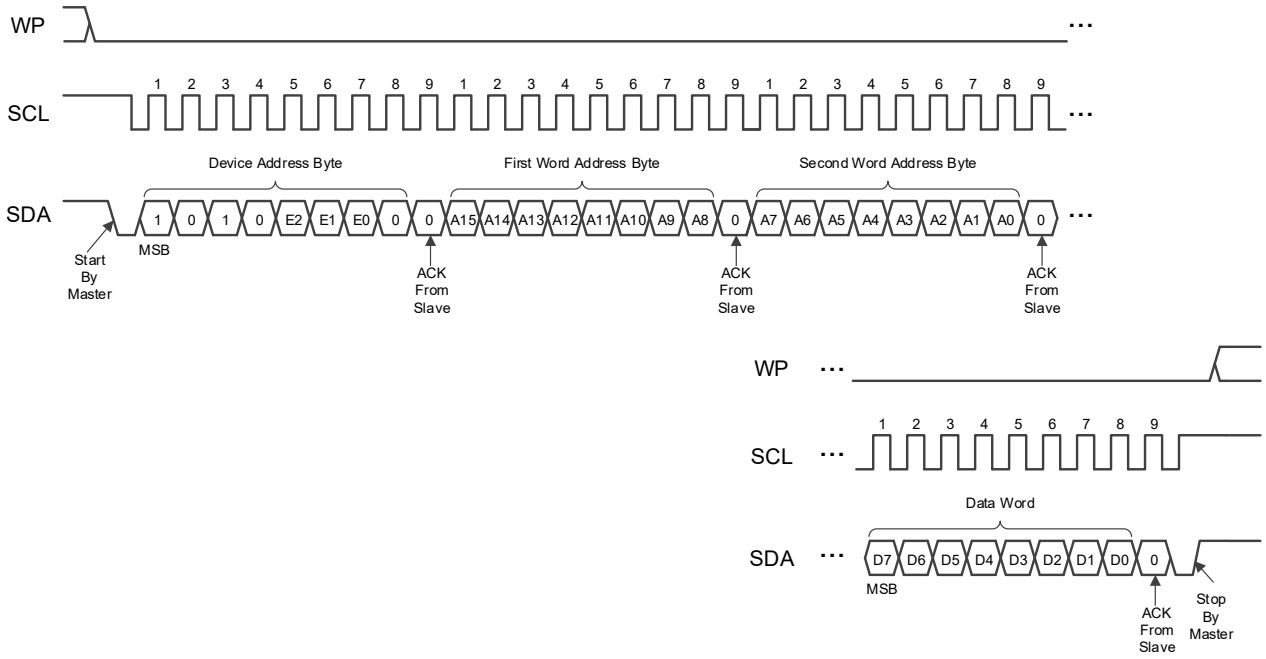



**Figure 5. Byte Write Operation with Write Protection Pin Set to Low**

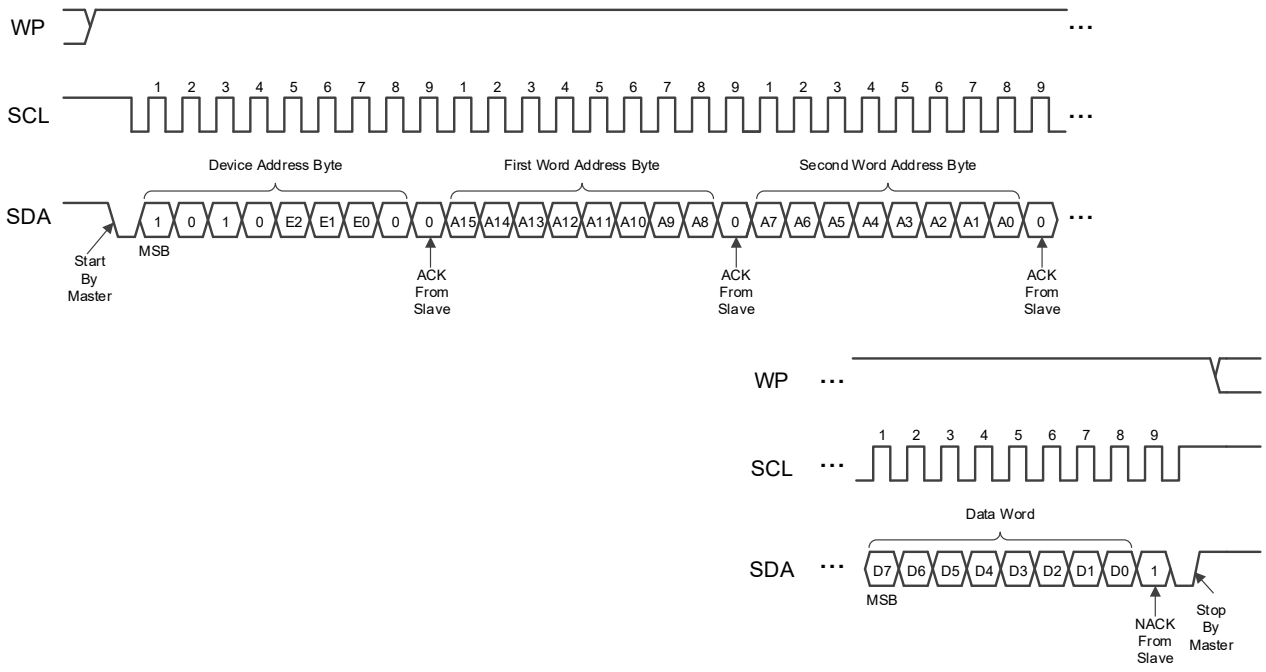



**Figure 6. Byte Write Operation with Write Protection Pin Set to High**

## READ AND WRITE OPERATIONS (continued)

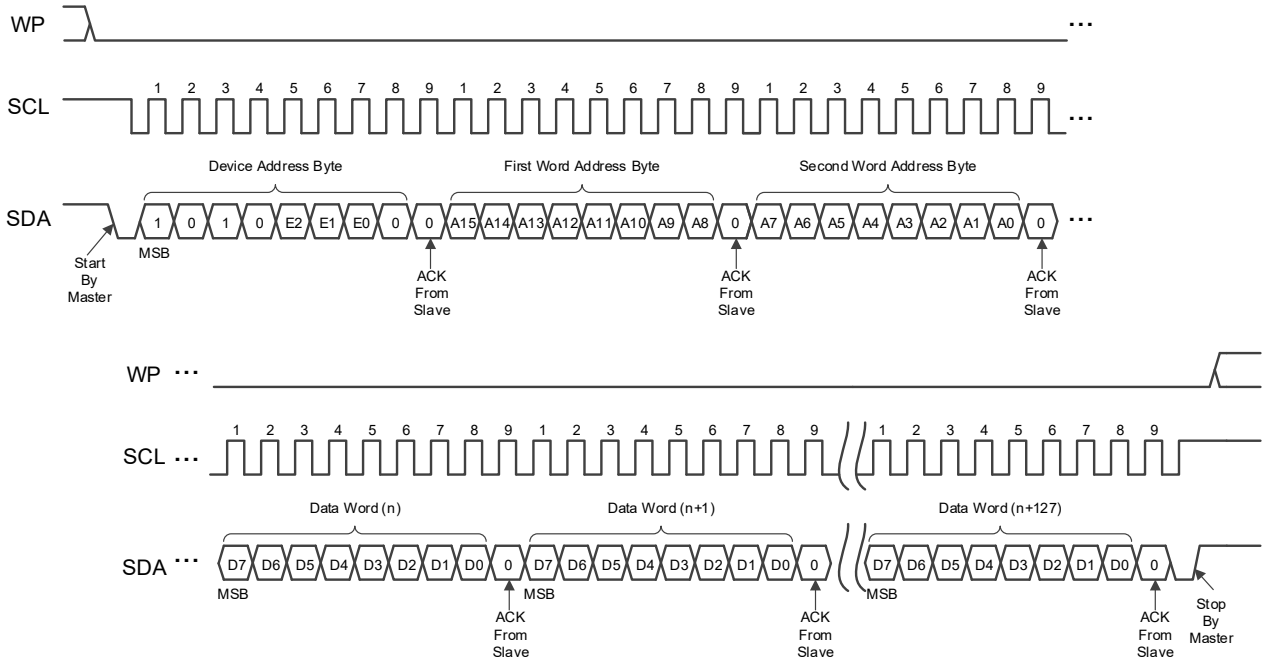



**Figure 7. Page Write Operation with Write Protection Pin Set to Low**

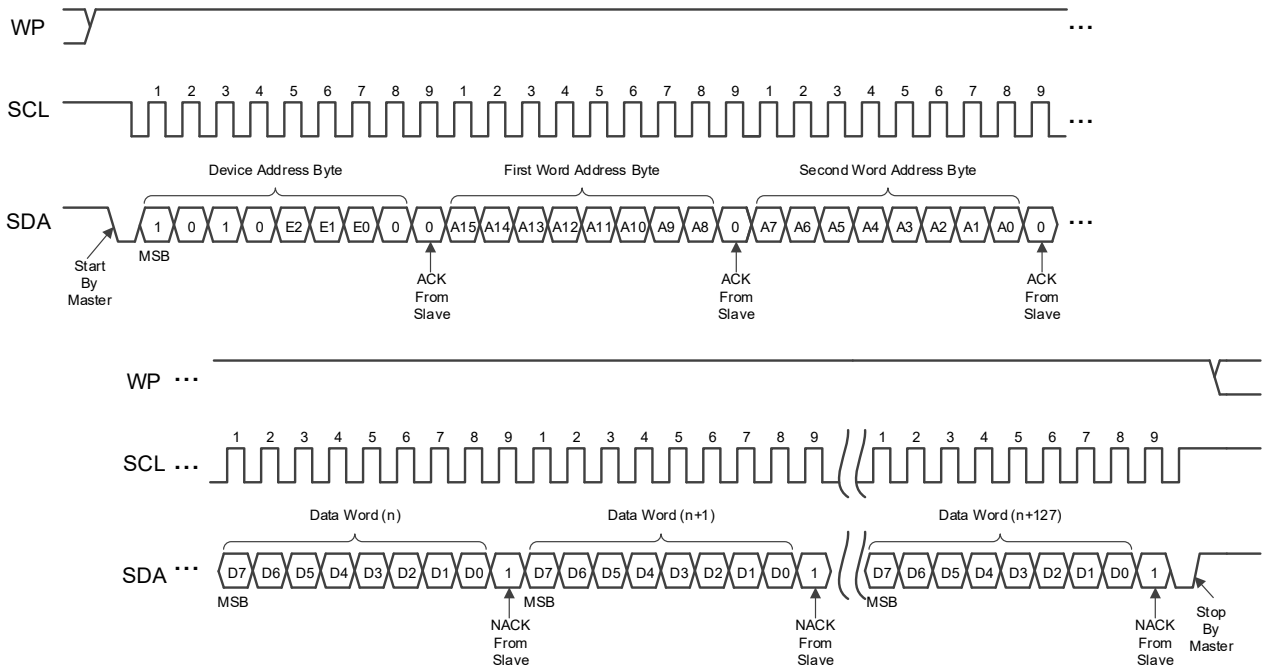



**Figure 8. Page Write Operation with Write Protection Pin Set to High**

# READ AND WRITE OPERATIONS (continued)

## Write Cycle Timing

The length of the self-timed write cycle, or $t_{WR}$, is defined as the amount of time from a valid Stop condition that begins the internal write sequence to the Start condition of the first device address byte sent to the TD24C512-C1 that it subsequently responds to with an ACK (see Figure 9).

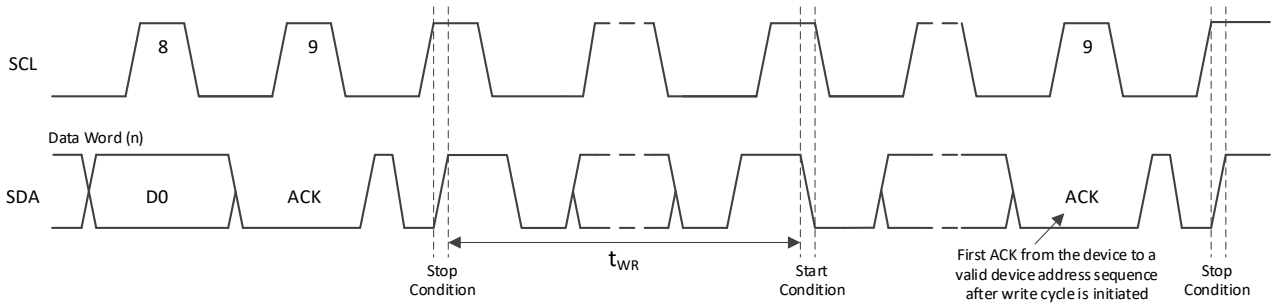



**Figure 9. Write Cycle Timing**

## Acknowledge (ACK) Polling

An ACK polling routine can be implemented to optimize time sensitive applications that would not prefer to wait the fixed maximum write cycle time but would prefer to know immediately when the Serial EEPROM write cycle has completed to start a subsequent operation. Once the internally self-timed write cycle has started, the device inputs are disabled and ACK polling can be initiated. An ACK polling routine involves sending a valid Start condition followed by the device address byte. While the write cycle is in progress, the device will not respond with an ACK, indicating the device is busy writing data. Once completed, the device returns an ACK and the next device operation can be started (see Figure 10).

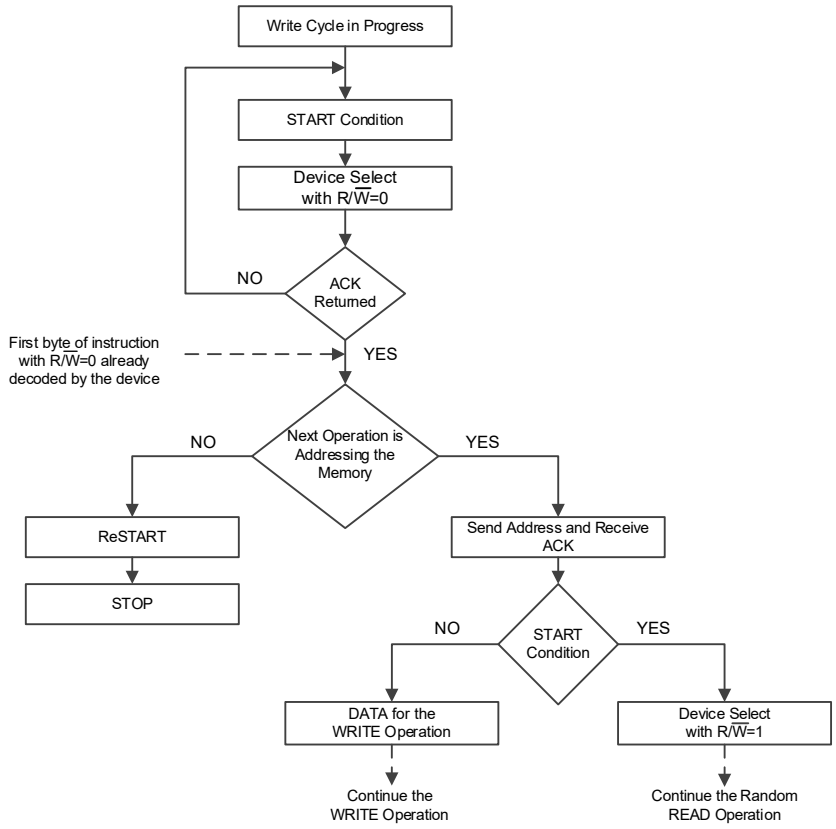



**Figure 10. Acknowledge Polling Flow Chart**

# READ AND WRITE OPERATIONS (continued)

## Write Identification Page

The TD24C512-C1 offers a 128-byte Identification Page (ID Page) in addition to the 512-Kbit memory array for storage of specific application data. This ID Page can be written and permanently locked in Read-only mode after the data is written into this Page. The Identification Page is written by issuing the Write Identification Page instruction (see Figure 11), which is similar to Page Write, except that:

- The device type identifier is defined as '1011';
- The word address bits A10:A9 must be '00', bits A15:A11 and A8:A7 are Don't Care;
- The word address bits A6:A0 define the byte locations inside the ID Page (see Table 3).

If the Identification Page has been locked, the data bytes transferred during the Write Identification Page instruction will not be acknowledged.

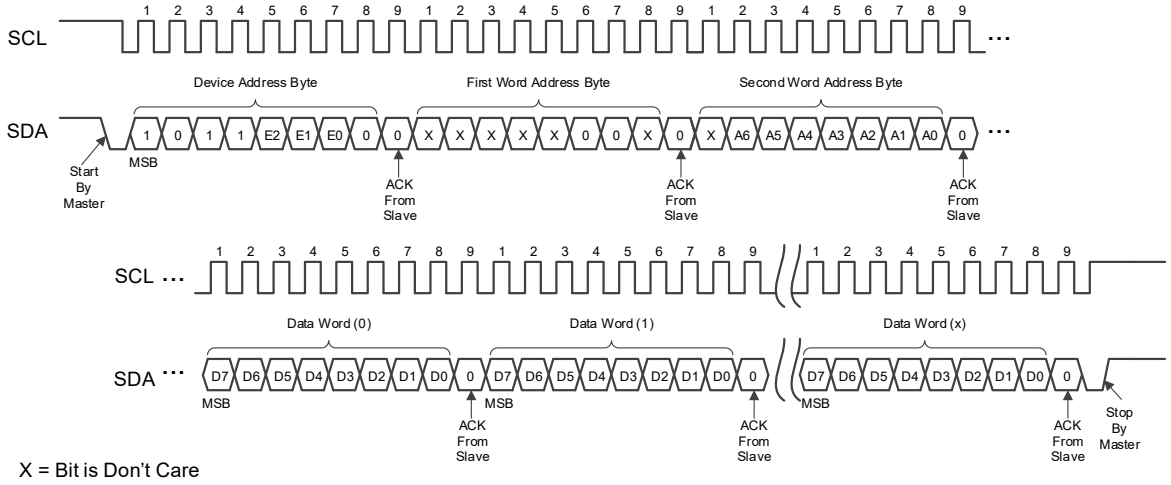



**Figure 11. Write Identification Page**

## Lock Identification Page

The Lock Identification Page (Lock ID) instruction permanently locks the Identification Page in Read-only mode. The Lock ID instruction is similar to Byte Write, except the following specific conditions:

- The device type identifier is defined as '1011';
- The word address bits A10:A9 must be '10' and other word address bits are Don't Care;
- The data byte must be equal to the binary value xxxx_xx1x, where x is Don't Care (see Figure 12).

Once a valid Lock ID instruction has been executed, if another Lock ID instruction is issued, the device will respond with an NACK to the data byte.

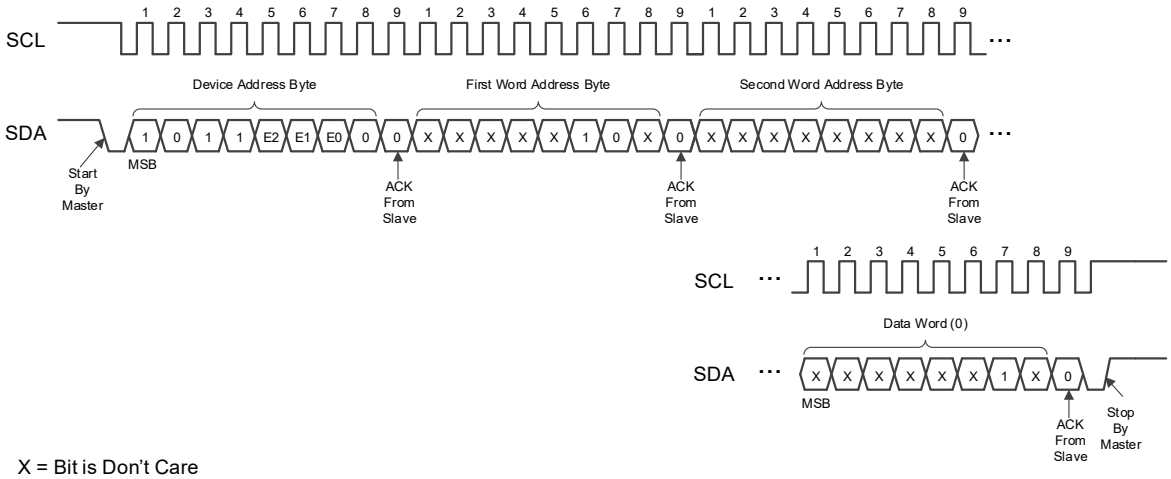



**Figure 12. Lock Identification Page**

# READ AND WRITE OPERATIONS (continued)

## Write Software Write Protection (SWP) Register

By writing specific values in the Software Write Protection (SWP) register, the 512-Kbit memory array can be Write-protected by blocks, which size can be defined as:

- The upper quarter memory array (memory address: C000h to FFFFh);
- The upper half memory array (memory address: 8000h to FFFFh);
- The whole memory array (memory address: 0000h to FFFFh).

Writing in the SWP register is performed with a Write SWP Register instruction (see Figure 13). This instruction is similar to Byte Write, except that:

- The device type identifier is defined as '1011';
- the word address bits A10:A9 must be '11' and other word address bits are Don't Care;
- The higher six bits of the data word byte are Don't Care; bit 1 and bit 0 (D1 and D0) define the size of Write-protected memory block to be against Write instructions (see Table 4).

Writing more than one byte will discard the write cycle and the content in the SWP register will not be changed. Writing the SWP register is performed independently of the state of the WP pin connection. Upon a certain instruction send by the Master, the device will automatically load the last configuration of the SWP register.

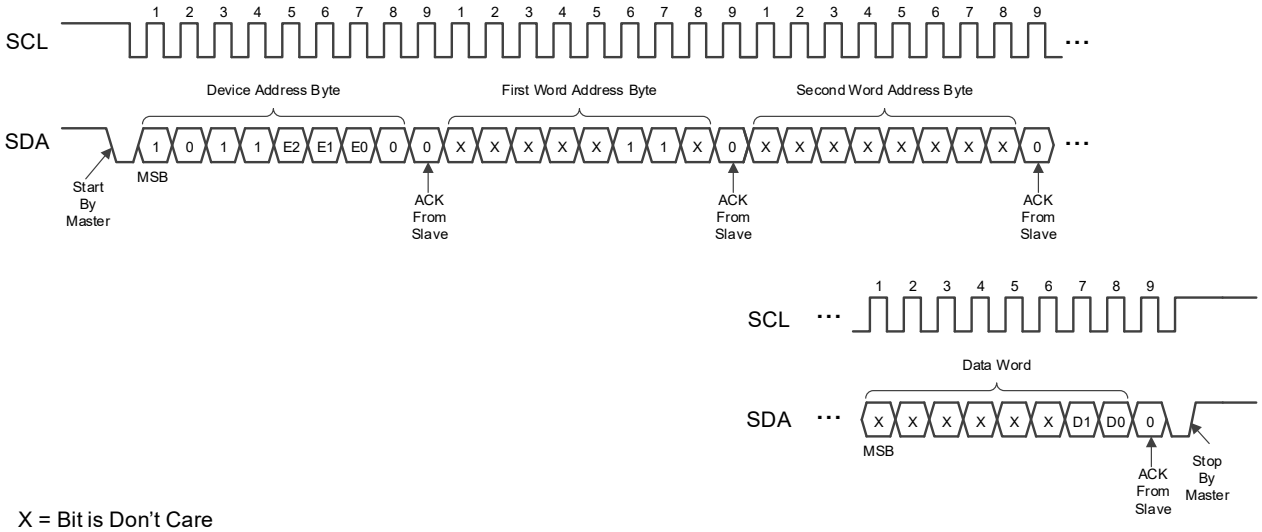



**Figure 13. Write Software Write Protection Register**

**Table 4. Software Write Protection Register**

| | REGISTER DATA BYTE | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
| Write | X (1) | X | X | X | X | X | Size of Write-protected Block<br>00: none<br>01: the upper quarter memory is write-protected<br>10: the upper half memory is write-protected<br>11: the whole memory is write-protected | |
| Read | 0 | 0 | 0 | 0 | 0 | 0 | | |

NOTE: 1. X = Bit is Don't Care.

# READ AND WRITE OPERATIONS (continued)

## Read Operations

All Read operations are initiated by the Master transmitting a Start condition, a device type identifier of '1010' or '1011', software device address bits (E2, E1, E0) that match corresponding hard-wired address pins (E2, E1, E0), and the R/W select bit with Logic 1 state. In the following clock cycle, the TD24C512-C1 should respond with an ACK. The subsequent protocol depends on the type of Read operation desired. There are three Read operations for memory array: Current Address Read, Random Address Read, and Sequential Read with the device type identifier of '1010'; four Read operations for Identification Page, SWP register and Unique ID: Read Identification Page, Read Lock Status, Read SWP Register and Read Unique ID with the device type identifier of '1011'. Read operations are performed independently of the state of the WP pin connection and the content in the SWP register.

## Current Address Read

For a Current Address Read operation, the Master sends a Start condition followed by transmitting the device address byte with the R/W bit set to Logic 1 (see Figure 14). The TD24C512-C1 should respond with an ACK and then serially transmits the data word addressed by the internal address counter. This address maintained by the internal address counter is the last address accessed during the last Read or Write operation. The counter is then incremented by one and the address will stay valid between operations as long as power to the device is supplied. The address roll-over during a Read operation is from the last byte of the last page to the first byte of the first page. To end the command, the Master responds with an NACK followed by a Stop condition.

Note that the internal address counter value is defined by instructions accessing the 512-Kbit memory or the Identification Page or the Unique ID. For example, when accessing the ID Page, the counter value is loaded with the byte location in the ID Page. Therefore the next Current Address Read in the memory uses this new address counter value. When accessing the memory, it is recommended to always use the Random Read instruction (see ***Random Read***) instead of the Current Address Read instruction.

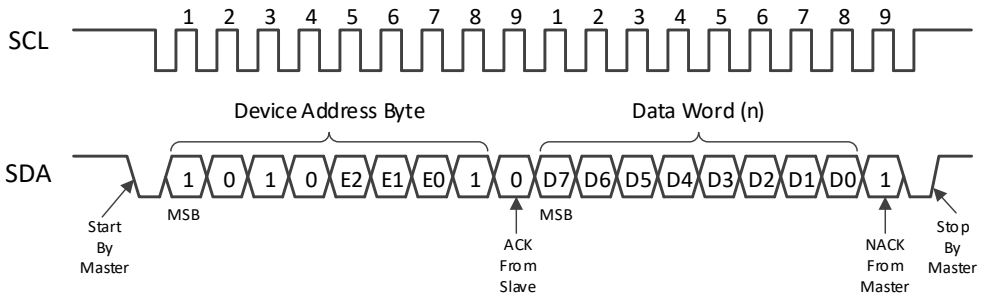



**Figure 14. Current Address Read**

# READ AND WRITE OPERATIONS (continued)

## Random Read

A Random Read operation allows the Master to access any memory location in a random manner and requires a dummy write sequence to preload the starting data word address. To perform a Random Read, the device address byte and the word address bytes are transmitted to the TD24C512-C1 as part of the dummy write sequence (see Figure 15). Once the device address byte and word address bytes are clocked in and acknowledged by the TD24C512-C1, the Master must generate another Start condition. The Master initiates a Current Address Read by sending another device address byte with the R/$\overline{W}$ bit set to Logic 1. The TD24C512-C1 responds with an ACK to the device address byte and serially clocks out the first data word and increments its internal address counter. The device will continue to transmit sequential data words as long as the Master continues to acknowledge each data word. To end the sequence, the Master responds with an NACK followed by a Stop condition.

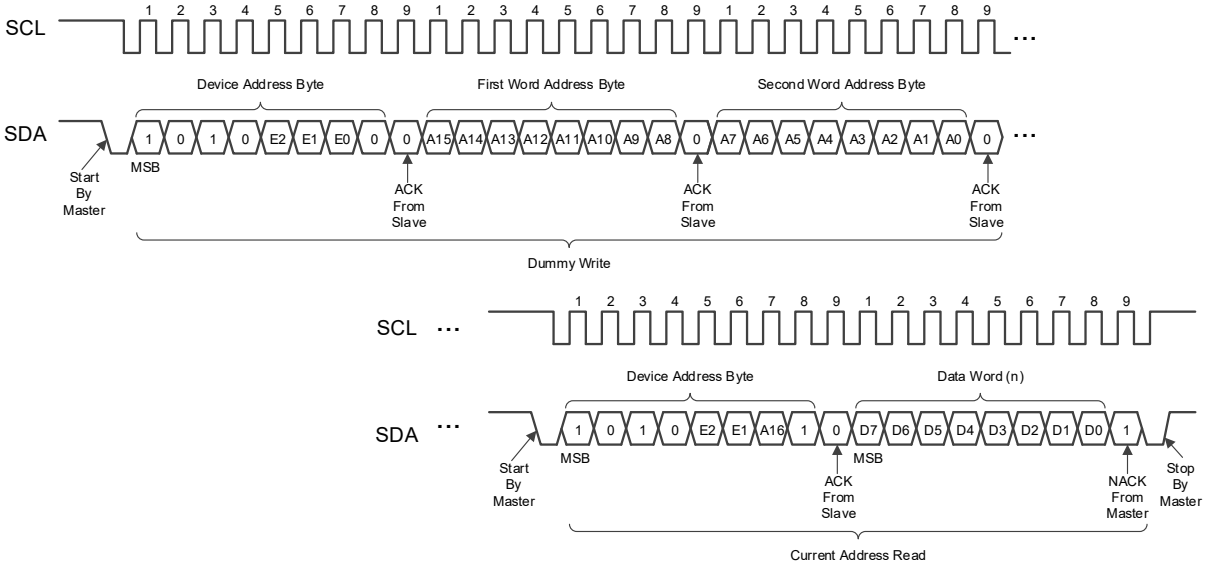



**Figure 15. Random Read**

## Sequential Read

A Sequential Read operation is initiated in the same way as either a Current Address Read or a Random Read, except that after the TD24C512-C1 transmitting the first data word, the Master responds with an ACK instead of an NACK. As long as the TD24C512-C1 receives an ACK, it will continue to increment the data word address and serially clock out the sequential data words (see Figure 16). When the internal address counter is at the last byte of the last page, the word address will roll over to the beginning of the memory array and the Sequential Read operation will continue. The Sequential Read operation is terminated by the Master responding with an NACK followed by a Stop condition.

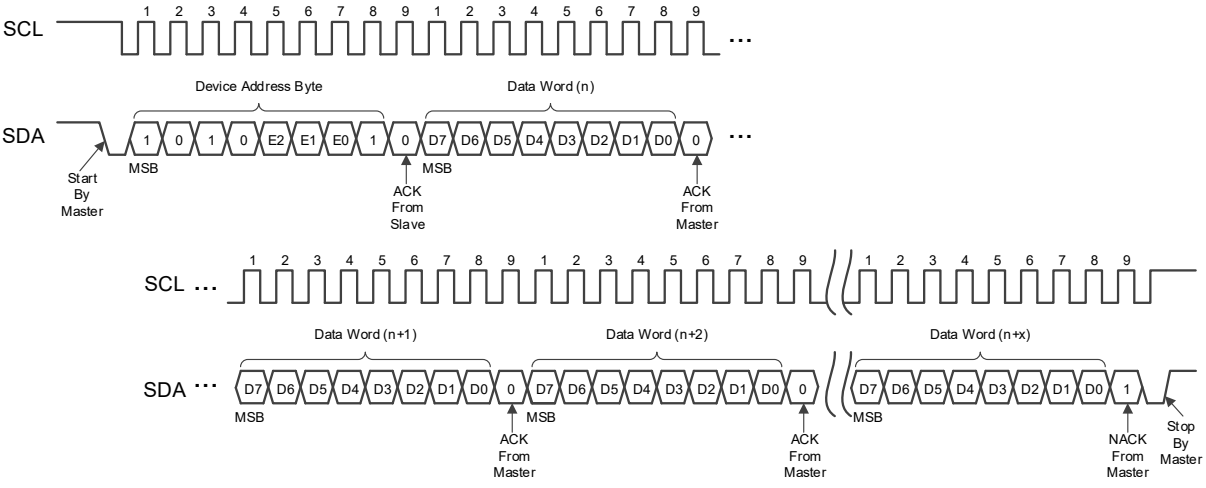



**Figure 16. Sequential Read**

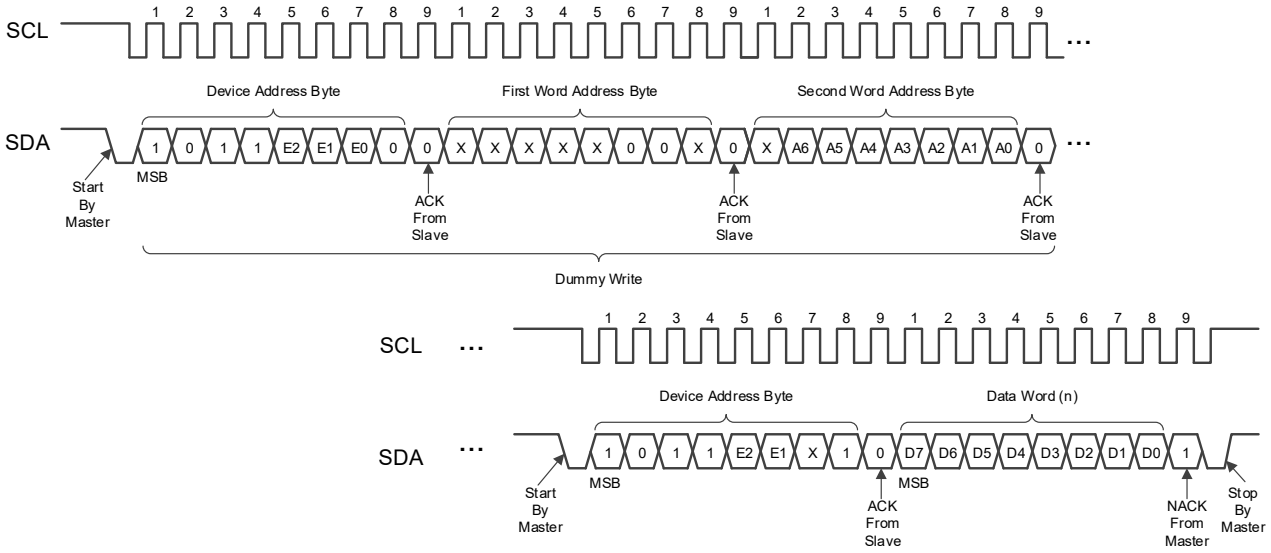
# READ AND WRITE OPERATIONS (continued)

## Read Identification Page

The Identification Page can be read by issuing a Read Identification Page instruction. This instruction uses the same protocol and format as Random Read, except that:

- The device type identifier is defined as '1011';
- The word address bits A10:A9 must be '00', bits A15:A11 and A8:A7 are Don't Care;
- The word address bits A6:A0 define the byte locations inside the ID Page (see Table 3).

When the end of Identification Page is reached, the word address will roll over to the beginning of the Identification Page. The Read Identification Page operation is terminated by the Master responding with an NACK followed by a Stop condition (see Figure 17).




X = Bit is Don't Care

**Figure 17. Read Identification Page**

# READ AND WRITE OPERATIONS (continued)

## Read Lock Status

The locked/unlocked status of the Identification Page can be checked by transmitting a specific truncated command, Write Identification Page instruction and one data byte to the device. The device responds with an ACK to the data byte if the Identification Page is unlocked, or responds with an NACK if the Identification Page has been locked. Right after this, it is recommended to transmit a Start condition to the device followed by a Stop condition (see Figure 18), so that the truncated Write command will not be executed because the Start condition resets the device internal logic, and the device is then set back into Standby mode by the Stop condition.

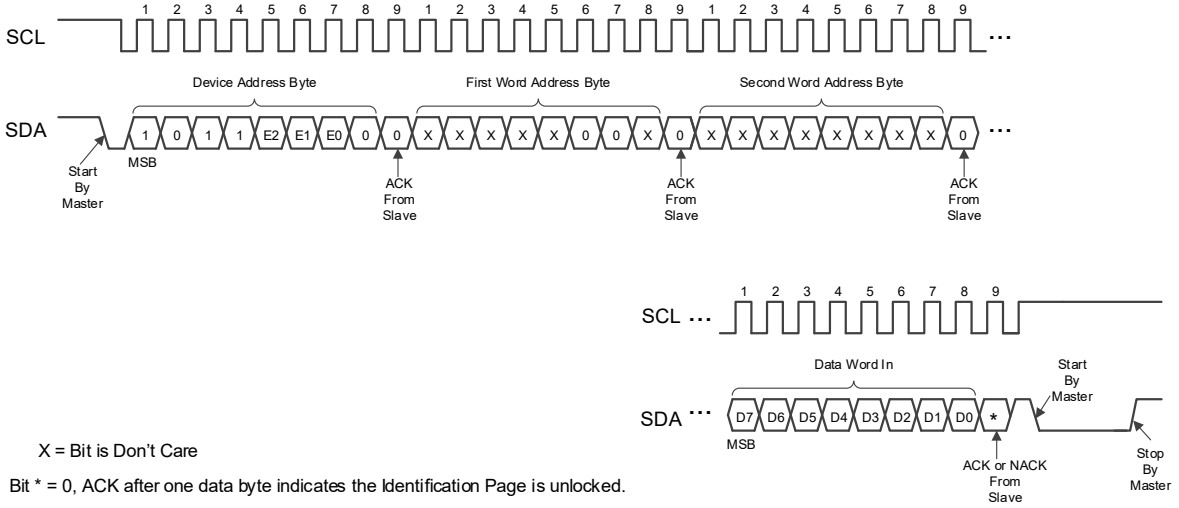



**Figure 18. Read Lock Status**

## Read SWP Register

Reading the SWP register is performed with a Read SWP Register instruction (see Figure 19), which is similar to Random Read except that:

- The device type identifier is defined as '1011';
- The word address bits A10:A9 must be '11' and other word address bits are Don't Care;
- The higher six bits of the SWP register content are read as '000000'. Bit 1 and bit 0 are defined in ***Write Software Write Protection (SWP) Register***.

Reading more than one byte will loop on reading the SWP register value.

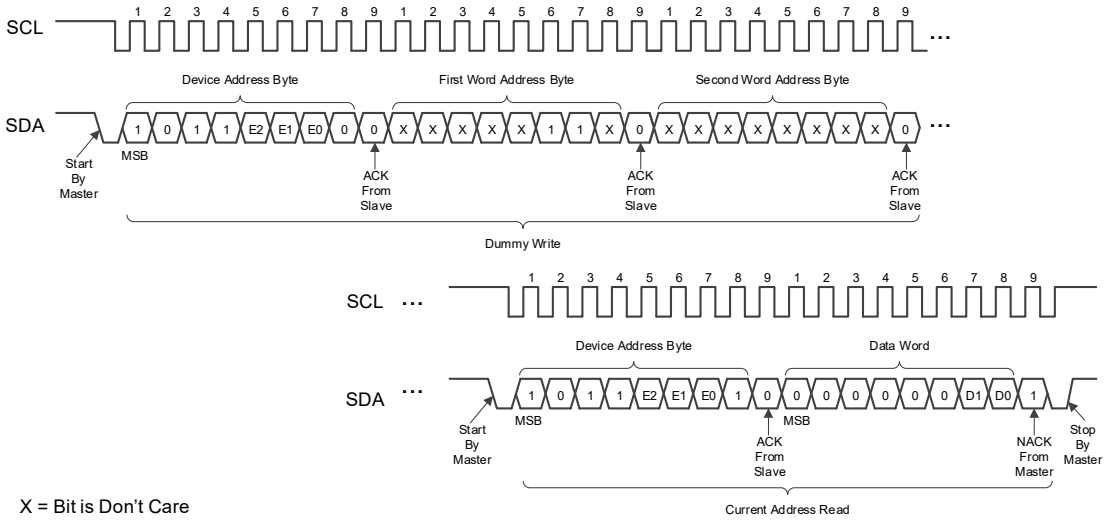



**Figure 19. Read SWP Register**

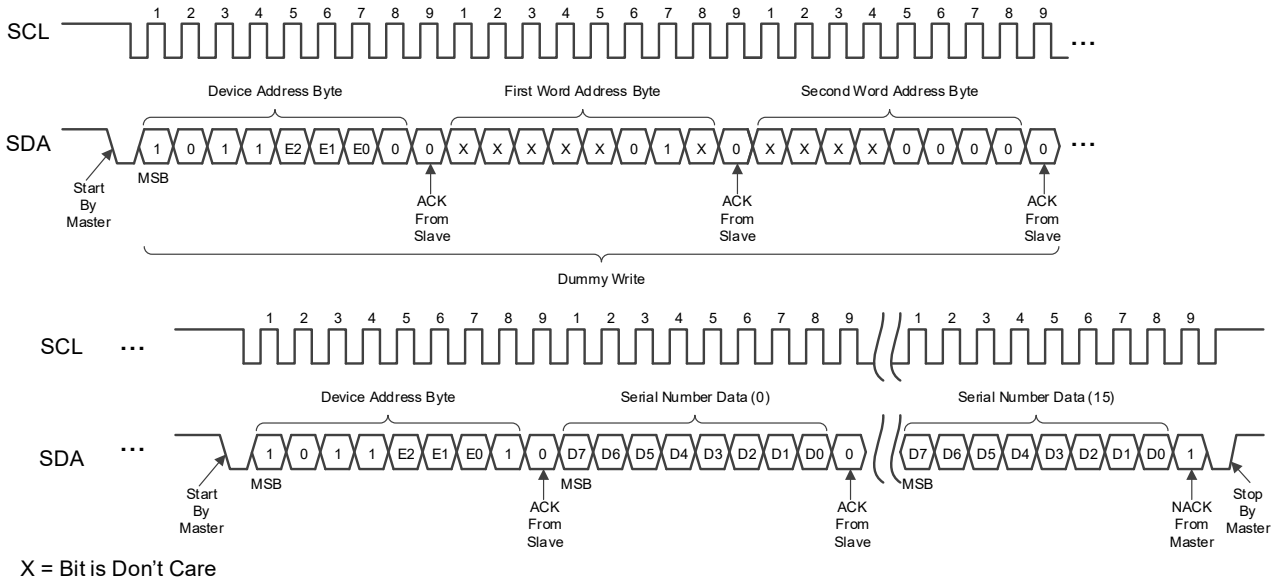
# READ AND WRITE OPERATIONS (continued)

## Read Unique ID

The TD24C512-C1 offers a separate memory block containing a factory programmed 128-bit Unique ID (UID), or Serial Number. Reading the Serial Number is similar to Sequential Read, except that:

- The device type identifier is defined as ‘1011’;
- The word address bits A10:A9 must be ‘01’, bits A15:A11 and A8:A4 are Don't Care;
- The word address bits A3:A0 define the byte locations inside the Unique ID (see Table 3).

In order to guarantee a unique number, the entire 128-bit value must be read from the starting address of the Serial Number block. Reading from a location other than the first address of the block will not result in a unique Serial Number. To read the first byte of the Serial Number, the word address bits A3:A0 need to be ‘0000’. Writing or altering the 128-bit Unique ID is not allowed. When the end of the 128-bit UID block is reached (16 bytes of data), the word address will roll over to the beginning of the 128-bit UID block. The Read Unique ID operation is terminated when the Master responds with an NACK to the data byte followed by a Stop condition (see Figure 20).




X = Bit is Don’t Care

**Figure 20. Read Unique ID**

# INITIAL DELIVERY STATE

The TD24C512-C1 serial EEPROM is delivered as follows:

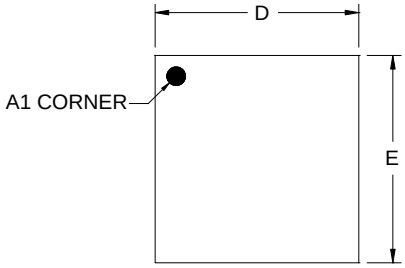
- All bits in the memory array are set to '1' (each byte contains FFh);
- All bits in the Identification Page are set to '1' (each byte contains FFh);
- All bits in the SWP register are set to '0'.

# REVISION HISTORY

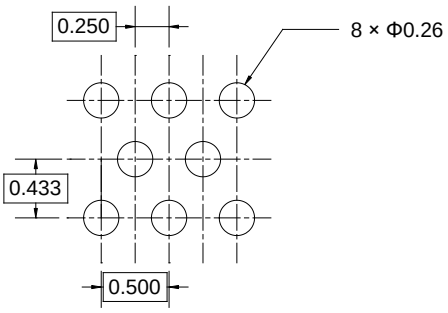
| REVISION | DATE | COMMENTS |
|---|---|---|
| REV.A | Mar. 2024 | Initial version release |
| REV.A.1 | Oct. 2026 | Updated:<br>— Operating Temperature Range<br>— Package Outline Dimensions<br>Added:<br>— $N_W$ at $T_A$ = +125℃, Page mode<br>— Tape and Reel Information |

# PACKAGE OUTLINE DIMENSIONS

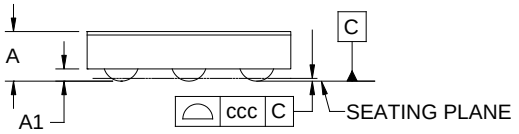
## WLCSP-1.5×1.53-8B



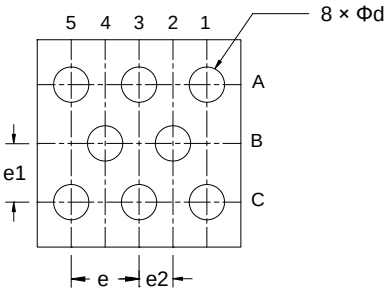

**TOP VIEW**




**RECOMMENDED LAND PATTERN** (Unit: mm)




**SIDE VIEW**



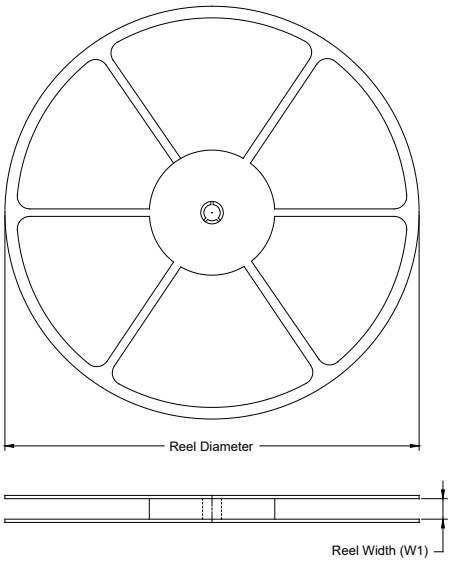

**BOTTOM VIEW**

| Symbol | Dimensions In Millimeters | | |
|---|---|---|---|
| | MIN | NOM | MAX |
| A | 0.340 | - | 0.390 |
| A1 | 0.070 | - | 0.110 |
| D | 1.471 | - | 1.531 |
| E | 1.498 | - | 1.558 |
| d | 0.230 | - | 0.290 |
| e | 0.500 BSC | | |
| e1 | 0.433 BSC | | |
| e2 | 0.250 BSC | | |
| ccc | 0.010 | | |

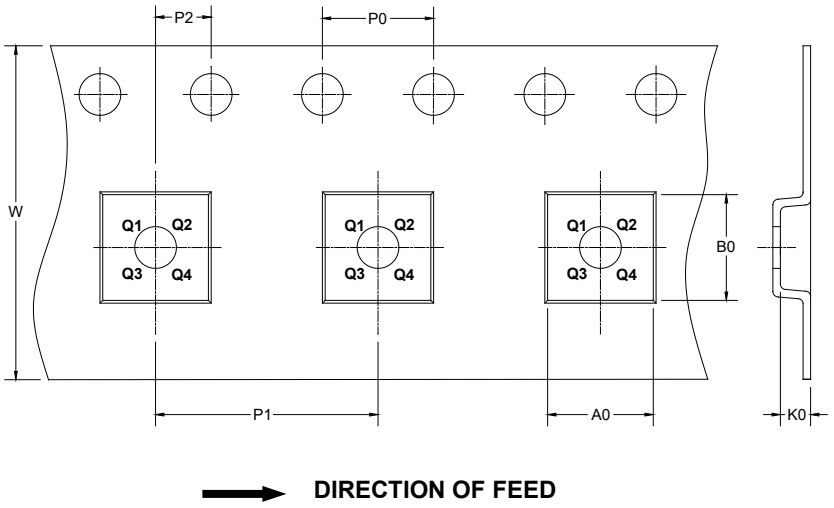
NOTE: This drawing is subject to change without notice.

# TAPE AND REEL INFORMATION

## REEL DIMENSIONS




## TAPE DIMENSIONS



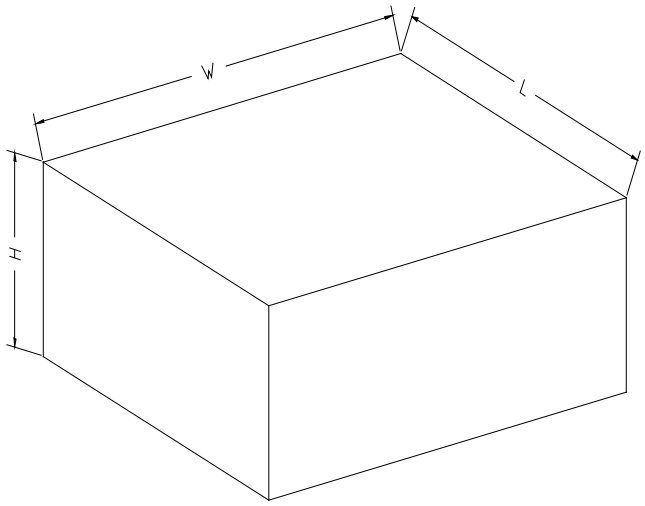

NOTE: The picture is only for reference. Please make the object as the standard.

## KEY PARAMETER LIST OF TAPE AND REEL

| Package Type | Reel Diameter | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P0 (mm) | P1 (mm) | P2 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|
| WLCSP-1.5×1.53-8B | 7" | 8.6 | 1.65 | 1.65 | 0.50 | 4.0 | 4.0 | 2.0 | 8.0 | Q1 |

DD0001

## CARTON BOX DIMENSIONS




NOTE: The picture is only for reference. Please make the object as the standard.

## KEY PARAMETER LIST OF CARTON BOX

| Reel Type | Length (mm) | Width (mm) | Height (mm) | Pizza/Carton |
|---|---|---|---|---|
| 7″ (Option) | 368 | 227 | 224 | 8 |
| 7″ | 442 | 410 | 224 | 18 |

DD0002