SGM839
85V, 16-Bit, High-Precision Power Monitor with SPI Interface

GENERAL DESCRIPTION

The SGM839 is a high-accuracy digital current sensor and power monitor with a 16-bit sigma-delta ADC inside. The device is capable of measuring a full-scale differential input of either ±163.84mV or ±40.96mV across a resistive shunt sense element, with -4V to +85V common-mode voltage.

The SGM839 features current, bus voltage, temperature and power monitoring along with an alert capability. The built-in temperature sensor has a typical accuracy of ±1℃ at +25℃ for measuring the die temperature and is helpful in monitoring the ambient temperature of the system.

Targeted at precision measurement applications, the SGM839 features low offset and low gain drift to maintain accuracy across temperature. Additionally, for wide-range current applications, its low offset voltage and low noise enable measurements from A to kA while ensuring low power loss. Furthermore, the low input bias current facilitates the use of high resistance sensing resistors, ensuring precise micro-amp range measurements.

The ADC conversion time of the device can be selected from 62μs to 2502μs and sample averaging can be selected from 1x to 1024x, which further contributes to reducing the noise.

The SGM839 is available in a Green MSOP-10 package.

FEATURES

- **High-Resolution, 16-Bit Sigma-Delta ADC**
- **Gain Accuracy:**
  - **Gain Error: ±0.25% (MAX)**
  - **Gain Drift: ±80ppm/℃ (MAX)**
- **Offset Accuracy:**
  - **Offset Voltage: ±25μV (MAX)**
  - **Offset Drift: ±400nV/℃ (MAX)**
- **Power Monitoring Accuracy: ±1.3% (MAX) at -40℃ to +125℃**
- **Fast Alert Response: 30μs**
- **Input Common-Mode Voltage Range: -4V to 85V**
- **Sense Bus Voltage Range: 0V to 85V**
- **Excellent CMRR: 145dB (TYP)**
- **Supply Voltage Range: 2.7V to 5.5V**
- **Shutdown Current: 3.8μA (TYP)**
- **Shunt Full-Scale Differential Range: ±163.84mV/±40.96mV**
- **Input Bias Current: 10nA (MAX)**
- **Temperature Sensor: ±1℃ (TYP at +25℃)**
- **Selectable Averaging and Conversion Times**
- **10MHz SPI Communication Interface**
- **Available in a Green MSOP-10 package**

APPLICATIONS

DC/DC Converters
Telecom Equipment Power Inverters
Industrial Battery Packs
Enterprise Servers
Power-over-Ethernet (PoE)

SIMPLIFIED SCHEMATIC

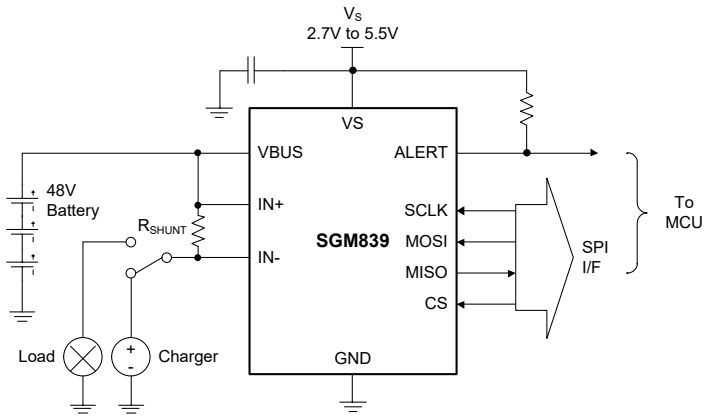


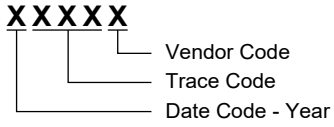
Figure 1. High-Side/Low-Side Sensing Simplified Schematic

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE TOP MARKING	PACKING OPTION
SGM839	MSOP-10	-40℃ to +125℃	SGM839XMS10G/TR	SGM839 XMS10 XXXXX	Tape and Reel, 4000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_S 6V
Analog Inputs, IN+, IN-
Differential (V_{IN+} - V_{IN-}) ..... -40V to 40V
Common-Mode ..... -4V to 85V
VBUS Voltage, V_{BUS} ..... -4V to 85V
MOSI, MISO, SCLK, ALERT Voltage, V_{IO} .....
..... -0.3V to V_S + 0.3V
Input Current into Any Pin, I_{IN} 5mA
Digital Output Current, I_{OUT} 10mA
Package Thermal Resistance
MSOP-10, θ_{JA} ..... 135.4℃/W
MSOP-10, θ_{JB} ..... 82.7℃/W
MSOP-10, θ_{JC} ..... 46.2℃/W
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility (1) (2)
HBM ..... ±4000V
CDM ..... ±1000V

NOTES:

1. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.

2. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

RECOMMENDED OPERATING CONDITIONS

Common-Mode Input Voltage, V_{CM} ..... -4V to 85V
Operating Supply Voltage, V_S ..... 2.7V to 5.5V
Operating Ambient temperature, T_A ..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

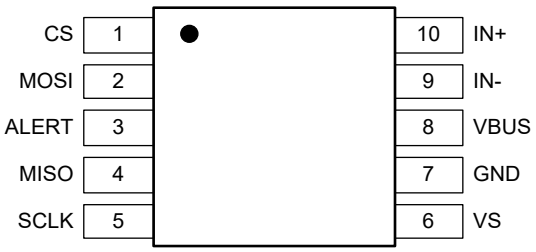
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

(TOP VIEW)



MSOP-10

PIN DESCRIPTION

PIN	NAME	TYPE	FUNCTION
1	CS	DI	SPI Chip Select (Active Low).
2	MOSI	DI	SPI Digital Data Input.
3	ALERT	DO	Multi-Functional Open-Drain Alert Output. Connect an external pull-up resistor from ALERT to VS. The typical application uses a 10kΩ pull-up resistor.
4	MISO	DO	SPI Digital Data Output (Push-Pull).
5	SCLK	DI	SPI Clock Input.
6	VS	P	Power Supply Pin. Connect a 0.1μF bypass capacitor between VS and GND, placed as close as possible to these pins.
7	GND	P	Ground.
8	VBUS	AI	Bus Voltage Input.
9	IN-	AI	Negative Input of the Device. Connect this pin to the low-voltage side of the sense resistor when positive current flows through it.
10	IN+	AI	Positive Input of the Device. Connect this pin to the high-voltage side of the sense resistor when positive current flows through it.

NOTE: AI: analog input, DI: digital input, DO: digital output, P: power.

ELECTRICAL CHARACTERISTICS

(T_A = +25℃, V_S = 3.3V, V_{SENSE} = V_{IN+} - V_{IN-} = 0mV and V_{CM} = V_{IN}- = 48V, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input						
Common-Mode Input Range	V_{CM}	T_A = -40℃ to +125℃	-4		85	V
Bus Voltage Input Range	V_{VBUS}		0		85	V
Common-Mode Rejection	CMRR	-4V < V_{CM} < 85V, T_A = -40℃ to +125℃	120	145		dB
Shunt Voltage Input Range	V_{DIFF}	T_A = -40℃ to +125℃, ADCRANGE = 0	-163.84		163.84	mV
		T_A = -40℃ to +125℃, ADCRANGE = 1	-40.96		40.96	mV
Shunt Offset Voltage	V_{OS}	V_{CM} = 48V		±5	±25	μV
		V_{CM} = 0V		±5	±25	μV
Shunt Offset Voltage Drift	dV_{OS}/dT	T_A = -40℃ to +125℃		±150	±400	nV/℃
Shunt Offset Voltage vs. Power Supply	PSRR	V_S = 2.7V to 5.5V		±1.8		μV/V
V_{BUS} Offset Voltage	V_{OS_BUS}	V_{BUS} = 200mV		±3.125	±25	mV
V_{BUS} Offset Voltage Drift	dV_{OS}/dT	T_A = -40℃ to +125℃		±150	±400	μV/℃
V_{BUS} Offset Voltage vs. Power Supply	PSRR	V_S = 2.7V to 5.5V		±2		mV/V
Input Bias Current	I_B	Either input, IN+ or IN-, V_{CM} = 30V		1.5	10	nA
VBUS Pin Input Impedance	Z_{VBUS}			1	1.4	MΩ
VBUS Pin Leakage Current	I_{VBUS}	V_{BUS} = 85V		85		μA
Input Differential Impedance	R_{DIFF}	Active mode, V_{IN+} - V_{IN-} < 164mV		280		kΩ
DC ACCURACY						
Shunt Voltage Gain Error	G_{SERR}			±0.04	±0.25	%
Shunt Voltage Gain Error Drift	G_{S_DRFT}			±40	±80	ppm/℃
VBUS Voltage Gain Error	G_{BERR}			±0.01	±0.25	%
VBUS Voltage Gain Error Drift	G_{B_DRFT}			±15	±40	ppm/℃
Power Total Measurement Error (TME)	P_{TME}	T_A = -40℃ to +125℃, at full scale		±0.02	±1.3	%
ADC Resolution				16		Bits
1 LSB Step Size		Shunt voltage, ADCRANGE = 0		5		μV
		Shunt voltage, ADCRANGE = 1		1.25		μV
		Bus voltage		3.125		mV
		Temperature		125		m℃
ADC Conversion-Time (1)	t_{CT}	Conversion time field = 0h		62		μs
		Conversion time field = 1h		80		
		Conversion time field = 2h		117		
		Conversion time field = 3h		193		
		Conversion time field = 4h		346		
		Conversion time field = 5h		654		
		Conversion time field = 6h		1269		
		Conversion time field = 7h		2502		
Integral Non-Linearity	INL			±3		m%
Differential Non-Linearity	DNL			0.5		LSB

NOTE: Subject to oscillator accuracy and drift.

ELECTRICAL CHARACTERISTICS (continued)

(T_A = +25℃, V_S = 3.3V, V_{SENSE} = V_{IN+} - V_{IN-} = 0mV and V_{CM} = V_{IN-} = 48V, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Clock Source						
Internal Oscillator Frequency	F_{OSC}			0.83		MHz
Internal Oscillator Frequency Tolerance	F_{OSC_TOL}	T_A = +25℃		±0.1	±5	%
		T_A = -40℃ to +125℃			±6	%
Temperature Sensor						
Measurement Range			-40		+125	℃
Temperature Accuracy		T_A = +25℃		±1		℃
		T_A = -40℃ to +125℃		±2		℃
Power Supply						
Supply Voltage	V_S		2.7		5.5	V
Quiescent Current	I_Q	V_{SENSE} = 0V		850	1200	μA
		V_{SENSE} = 0V, T_A = -40℃ to +125℃			1500	μA
Quiescent Current, Shutdown	I_{QSD}	Shutdown mode		3.8	6	μA
Device Startup Time	t_{POR}	Power-up (NPOR)		60		μs
		From shutdown mode		40		
Digital Input/Output						
Logic Input Level, High	V_{IH}		1.2			V
Logic Input Level, Low	V_{IL}				0.4	V
Logic Output Level, Low	V_{OL}	I_{OL} = 1mA		0.1	0.4	V
Logic Output Level, High	V_{OH}	I_{OL} = 1mA	V_S - 0.4		V_S	V
Digital Leakage Input Current	I_{IO_LEAK}	0V ≤ V_{IN} ≤ V_S		0.05	0.2	μA

TIMING REQUIREMENTS

PARAMETER	SYMBOL	MIN	NOM	MAX	UNIT
Serial Interface					
SPI Bit Frequency	f_{SPI}			10	MHz
SCLK High Time	t_{SCLK_H}	40			ns
SCLK Low Time	t_{SCLK_L}	40			ns
CS Fall to First SCLK Rise Time	t_{CSF_SCLKR}	10			ns
Last SCLK Fall to CS Rise Time	t_{SCLKF_CSR}	10			ns
Sequential Transfer Delay (1)	t_{FRM_DLY}	50			ns
MOSI Rise and Fall Time, 10MHz SCLK	t_{MOSI_RF}			15	ns
MOSI Data Setup Time	t_{MOSI_ST}	10			ns
MOSI Data Hold Time	t_{MOSI_HLD}	20			ns
MISO Rise and Fall Time, C_{LOAD} = 200pF	t_{MISO_RF}			15	ns
MISO Data Setup Time	t_{MISO_ST}	20			ns
MISO Data Hold Time	t_{MISO_HLD}	20			ns
CS Falling Edge to MISO Data Valid Delay Time	$t_{CS_MISO_DLY}$			25	ns
CS Rising Edge to MISO High Impedance Delay Time	$t_{CS_MISO_HIZ}$			25	ns

Timing Diagram

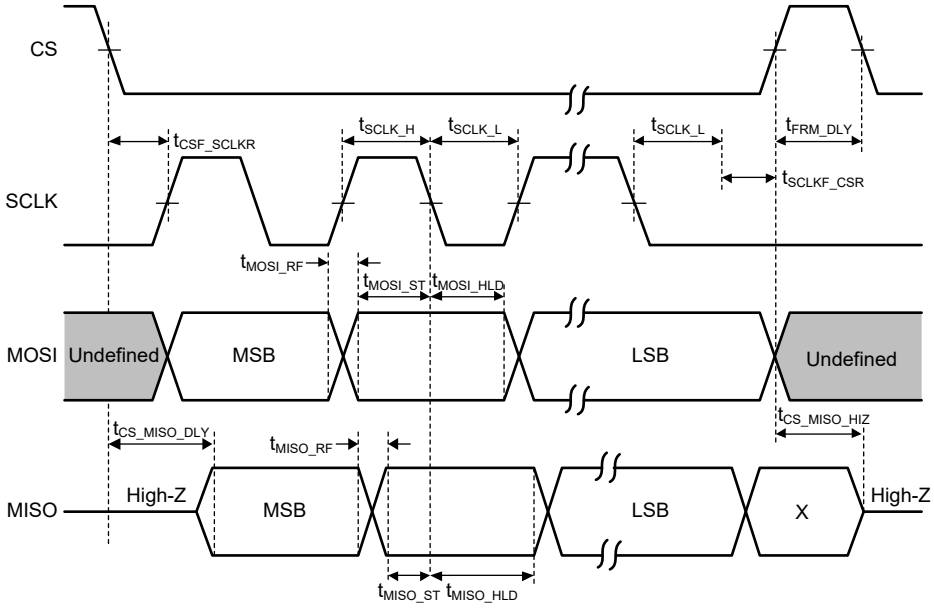
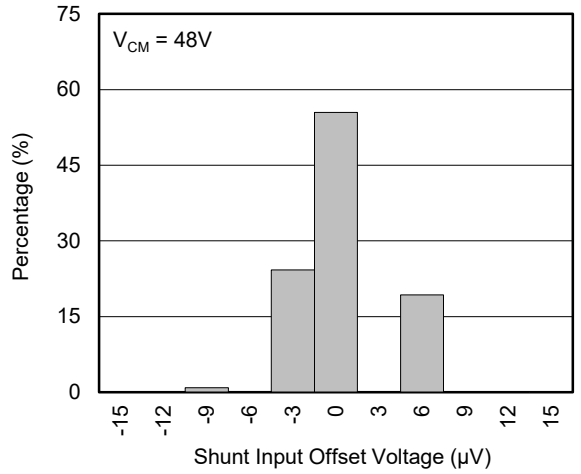


Figure 2. SPI Timing Diagram

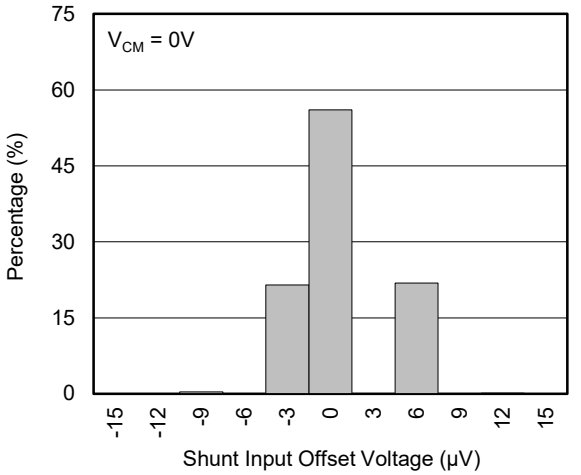
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = +25℃, V_S = 3.3V, V_{CM} = 48V, V_{SENSE} = 0V, and V_{VBUS} = 48V unless otherwise noted.

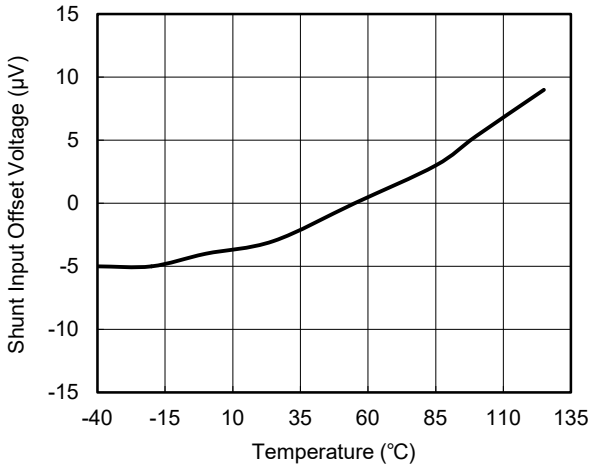
Shunt Input Offset Voltage Production Distribution



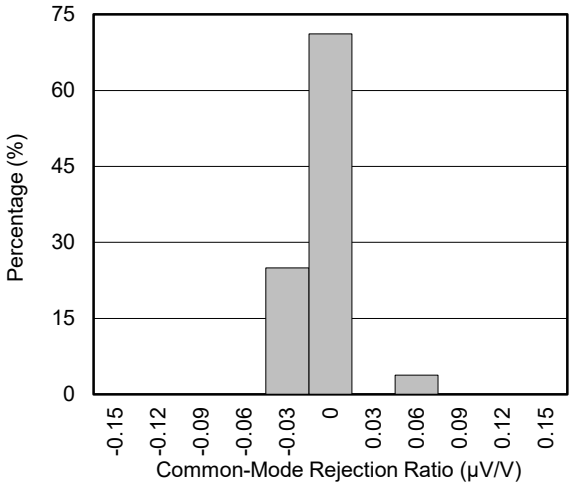
Shunt Input Offset Voltage Production Distribution



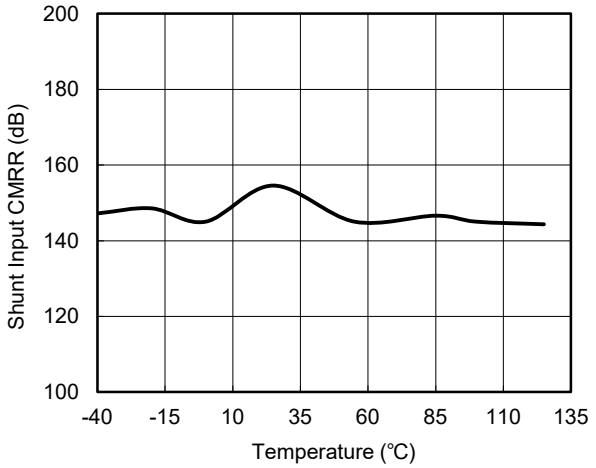
Shunt Input Offset Voltage vs. Temperature



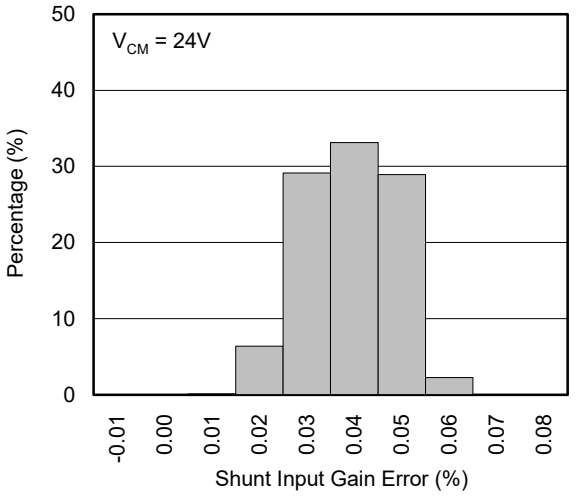
Common-Mode Rejection Ratio Production Distribution



Shunt Input Common-Mode Rejection Ratio vs. Temperature



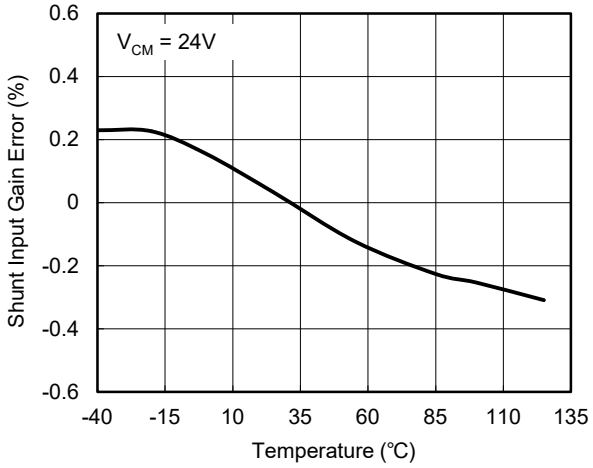
Shunt Input Gain Error Production Distribution



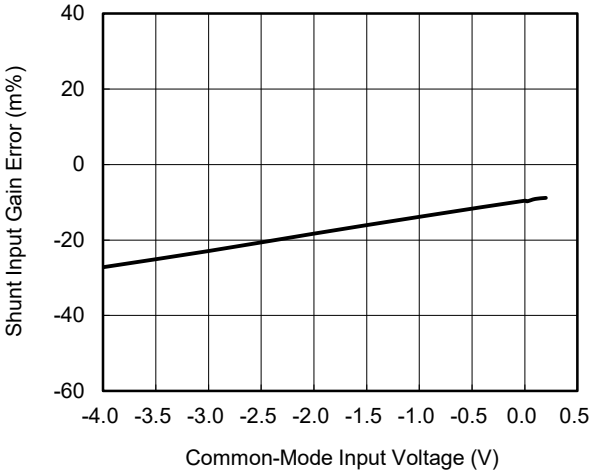
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, V_S = 3.3V, V_{CM} = 48V, V_{SENSE} = 0V, and V_{VBUS} = 48V unless otherwise noted.

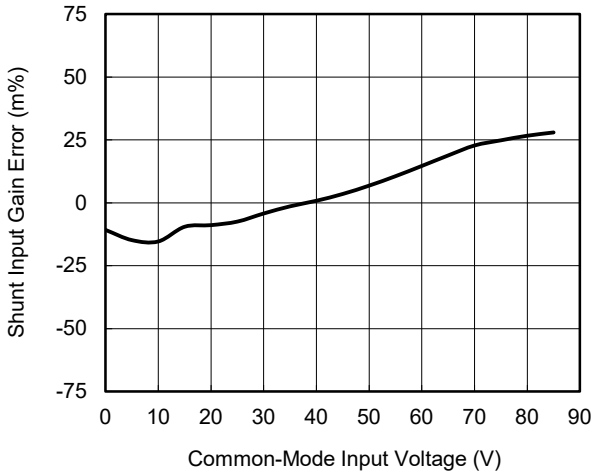
Shunt Input Gain Error vs. Temperature



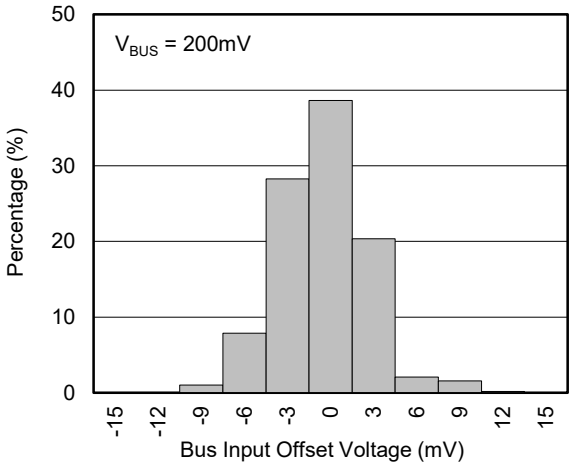
Shunt Input Gain Error vs. Common-Mode Voltage



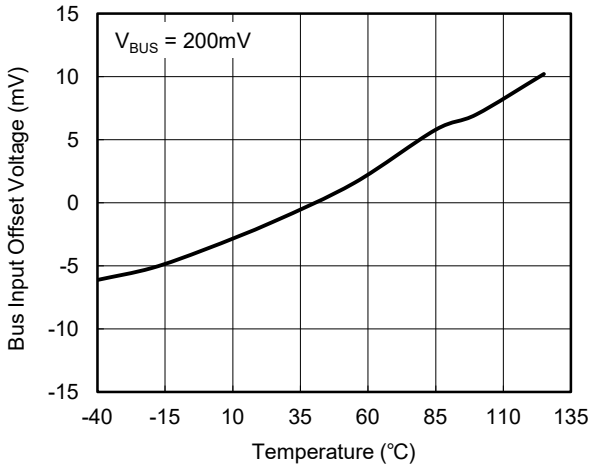
Shunt Input Gain Error vs. Common-Mode Voltage



Bus Input Offset Voltage Production Distribution



Bus Input Offset Voltage vs. Temperature



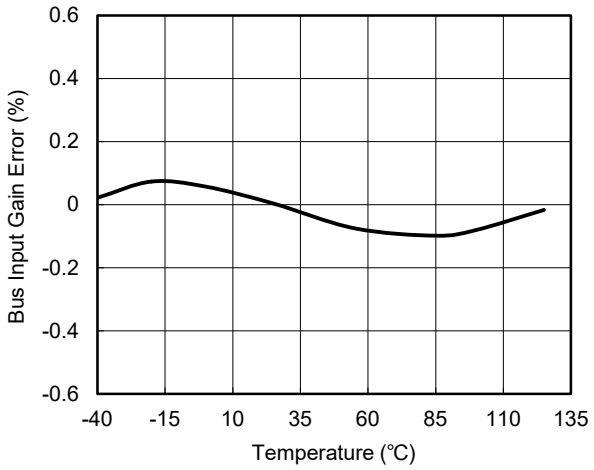
Bus Input Gain Error Production Distribution



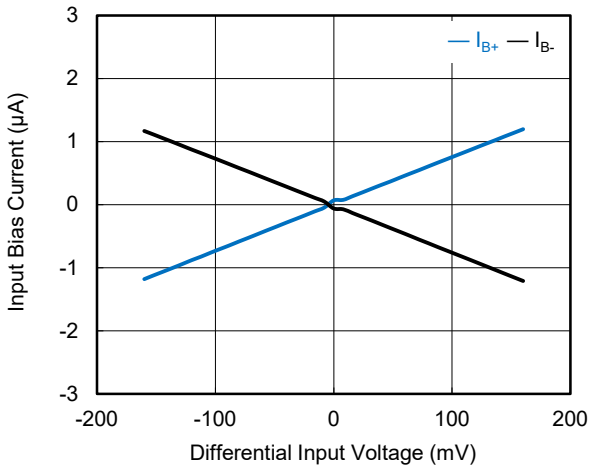
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, V_S = 3.3V, V_{CM} = 48V, V_{SENSE} = 0V, and V_{VBUS} = 48V unless otherwise noted.

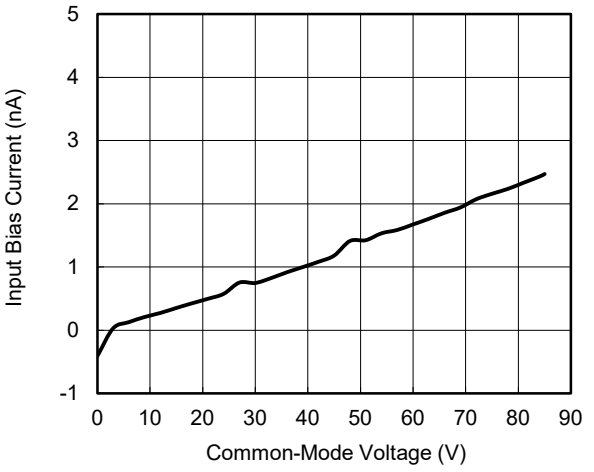
Bus Input Gain Error vs. Temperature



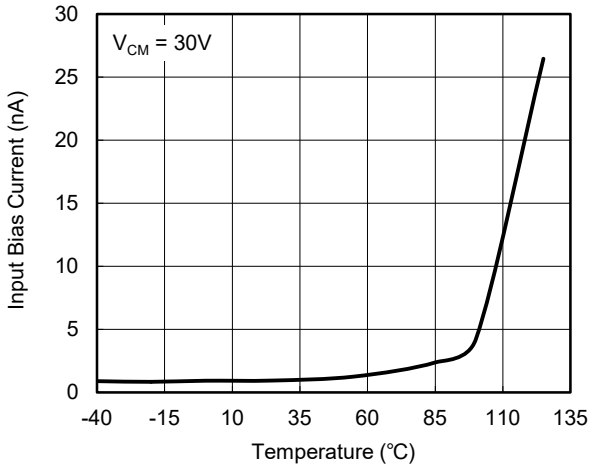
Input Bias Current vs. Differential Input Voltage



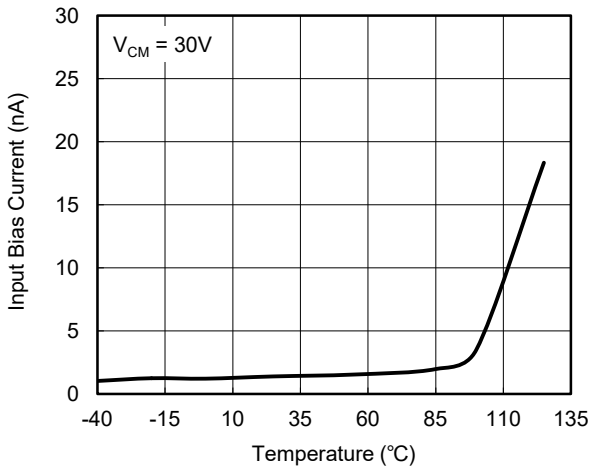
Input Bias Current (I_{B+} or I_{B-}) vs. Common-Mode Voltage



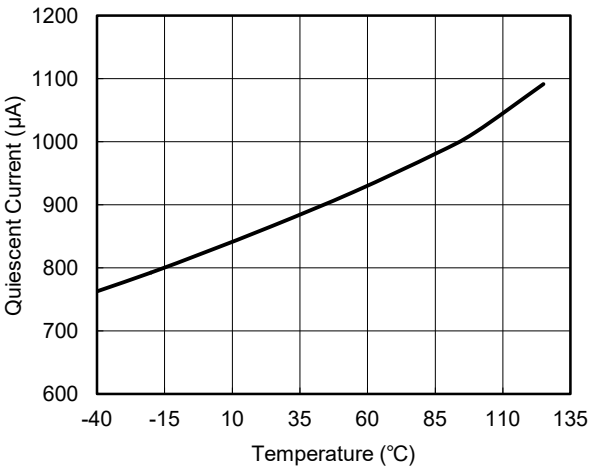
Input Bias Current vs. Temperature



Input Bias Current vs. Temperature, Shutdown



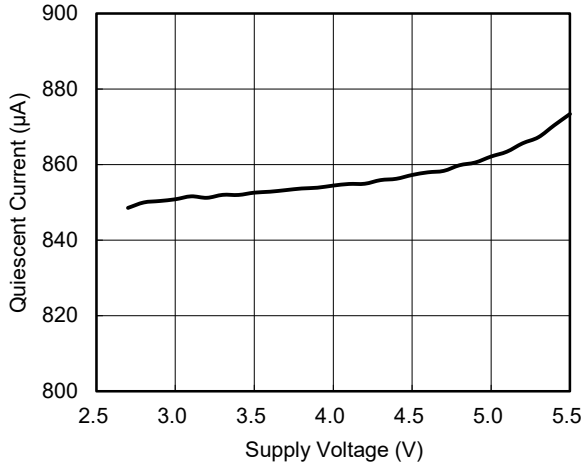
Quiescent Current vs. Temperature



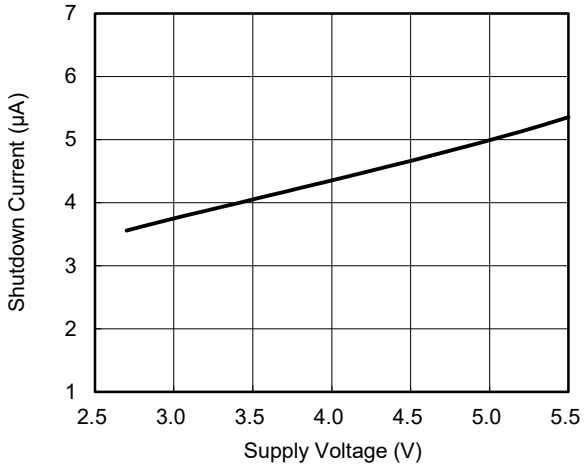
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, V_S = 3.3V, V_{CM} = 48V, V_{SENSE} = 0V, and V_{VBUS} = 48V unless otherwise noted.

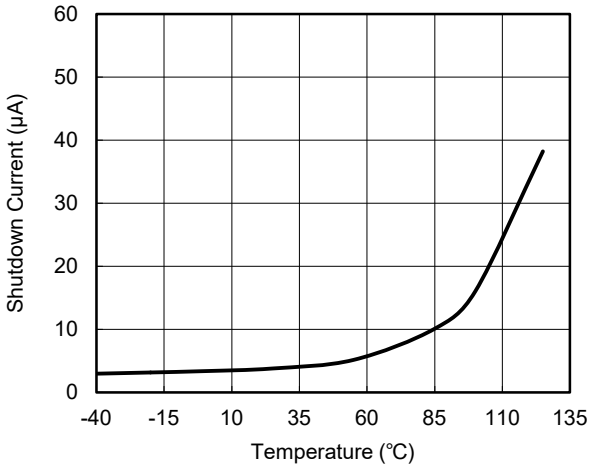
Quiescent Current vs. Supply Voltage



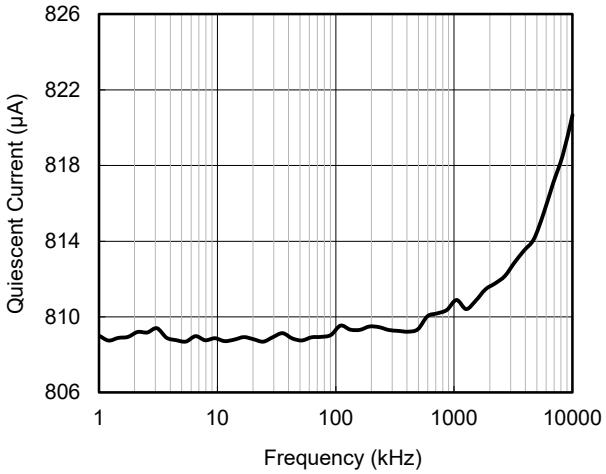
Shutdown Current vs. Supply Voltage



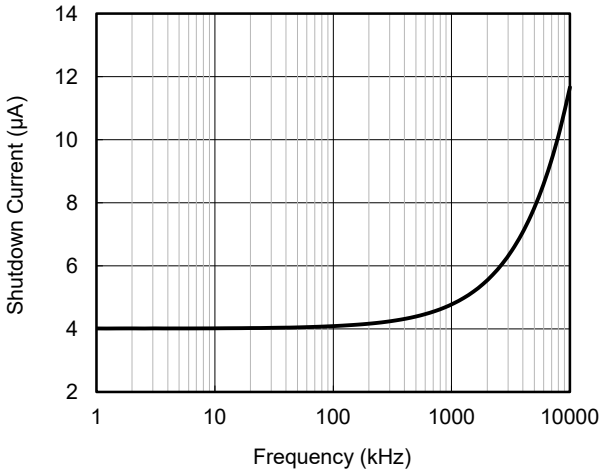
Shutdown Current vs. Temperature



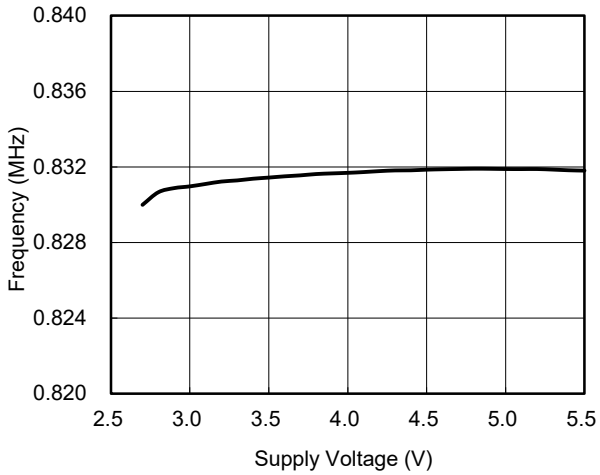
Quiescent Current vs. Clock Frequency



Shutdown Current vs. Clock Frequency

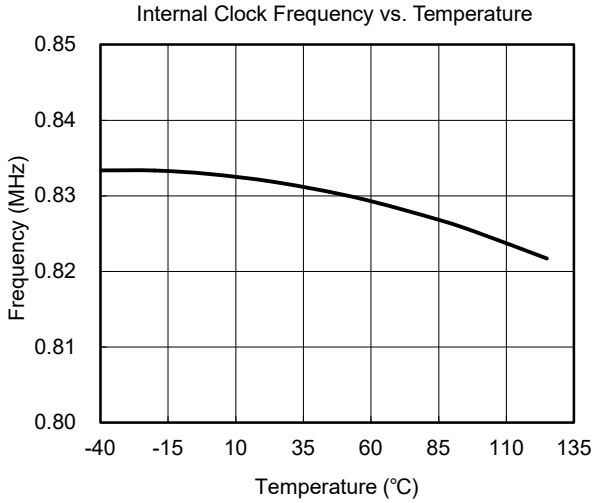


Internal Clock Frequency vs. Power Supply



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, V_S = 3.3V, V_{CM} = 48V, V_{SENSE} = 0V, and V_{VBUS} = 48V unless otherwise noted.



FUNCTIONAL BLOCK DIAGRAM

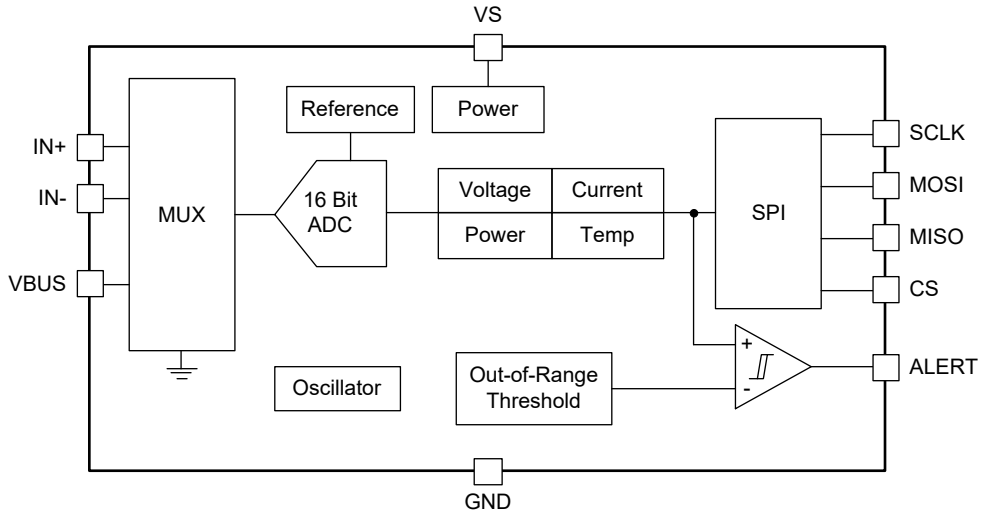


Figure 3. Functional Block Diagram

DETAILED DESCRIPTION

Overview

The SGM839 is a high-precision digital power monitor with an integrated 16-bit sigma-delta ADC and a 4-wire SPI interface. The device measures shunt voltage, bus voltage and die temperature, and internally calculates current and power. Programmable conversion modes, conversion times, averaging and alert functions provide flexible configuration for a wide range of power-monitoring applications. Detailed register information is provided in the Register Maps section.

Feature Description

Versatile High Voltage Measurement Capability

The SGM839 operates from a 2.7V to 5.5V supply and supports input common-mode voltages from -4V to +85V. It measures current by sensing the differential voltage developed across an external shunt resistor connected between the IN+ and IN- pins. The input stage supports common-mode voltages higher than the device supply voltage, allowing the SGM839 to be used for both high-side and low-side current sensing. The input common-mode voltage is independent of VS, allowing voltages within the specified input range to be present at the input pins even when VS is unpowered.

The device also measures bus voltage through the VBUS pin and die temperature with the integrated temperature sensor. Shunt voltage is measured differentially between the IN+ and IN- pins, while bus voltage is measured at the VBUS pin with respect to GND. The VBUS measurement range is 0V to 85V, and the specified die temperature measurement range is -40℃ to +125℃.

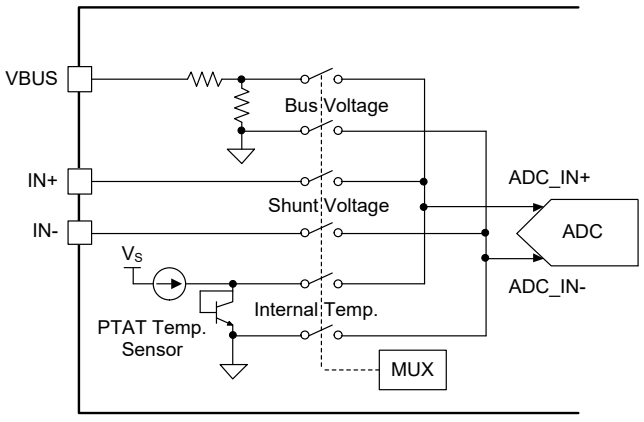
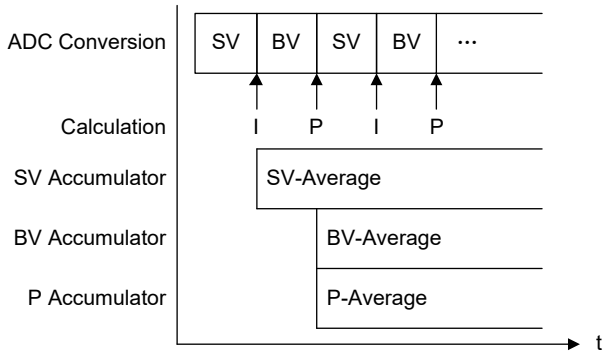


Figure 4. High-Voltage Input Multiplexer

Shunt voltage, bus voltage, and die temperature signals are multiplexed internally to a single ADC, as shown in Figure 4.

Power Calculation

The SGM839 calculates current from the measured shunt voltage and calculates power using the calculated current and measured bus voltage, as shown in Figure 5. Power is calculated using the most recent current result and bus voltage measurement. If the SHUNT_CAL register is set to zero, the reported current and power values are also zero.



Note: SV: Shunt Voltage; BV: Bus Voltage; I: Current; P: Power.

Figure 5. Power Calculation Scheme

When averaging is enabled, the calculated current and power values from each conversion sequence are accumulated internally. After the programmed number of samples has been completed, the averaged current and power results are transferred to the corresponding output registers. When averaging is set to 1, each calculated result is transferred directly to the corresponding output register. These calculations are performed in the background and do not increase the ADC conversion time.

Low Bias Current

The SGM839 features low input bias current, which helps minimize measurement error and enables the use of larger shunt resistors for low-current sensing applications. Low input bias current also reduces the error introduced by series resistance when an input filter is used to attenuate high-frequency noise.

Using a larger shunt resistance produces a larger differential input voltage for a given load current, improving measurement resolution at low current levels. Therefore, the low input bias current of the SGM839 allows accurate current measurements over a wide dynamic range, including sub-mA current levels.

DETAILED DESCRIPTION (continued)

The input bias current varies with the differential input voltage and common-mode voltage. Refer to the Typical Performance Characteristics for the corresponding input bias current curves.

High-Precision Sigma-Delta ADC

The SGM839 integrates a 16-bit sigma-delta ADC for shunt voltage, bus voltage, and die temperature measurements. An internal high-voltage multiplexer selects the enabled measurement inputs and routes them to the ADC, as shown in Figure 4. The low-offset ADC architecture supports bidirectional shunt voltage sensing and helps preserve the usable measurement range for signals close to zero.

The MODE bits in the ADC_CONFIG register determine the device operating mode and the measurements included in each conversion sequence. The SGM839 supports continuous and triggered operation. In continuous mode, the device repeatedly performs the selected measurements and updates the corresponding output registers as new results become available. In a triggered mode, the device performs the selected conversion and averaging sequence once and then returns to power-save mode. Another triggered conversion can be initiated by writing a triggered-mode value to the MODE bits. Writing the MODE bits while a triggered or continuous conversion is in progress interrupts the current sequence and starts a new sequence using the newly programmed mode.

The conversion times for shunt voltage, bus voltage, and die temperature are independently programmable through the ADC_CONFIG register. Each enabled measurement input can use one of eight conversion-time settings from 62μs to 2502μs. Enabled inputs are converted sequentially, so the time required to complete one conversion sequence depends on the enabled measurements and their individual conversion-time settings.

The AVG bits select averaging from 1 to 1024 samples and apply the same averaging setting to all enabled measurement inputs. When the averaging count is 1 (AVG = 0h), each completed measurement result is transferred directly to its corresponding output register. When averaging is enabled, the conversion sequence is repeated and intermediate results are accumulated internally until the programmed number of samples has been completed. The final averaged results are then transferred to the corresponding output registers. Previously completed results remain available through the SPI interface until new completed results become available. Reading the output registers does not interrupt a conversion in progress.

The Conversion Ready Flag (CNVRF) in the DIAG_ALRT register indicates completion of a conversion sequence. CNVRF is set after all selected conversions and programmed averaging operations are complete. The flag is cleared when the DIAG_ALRT register is read. Writing the ADC_CONFIG register also clears CNVRF, except when shutdown mode is selected.

Current and power calculations are performed by the internal digital calculation engine during continuous or triggered operation. These calculations run in the background and do not extend the ADC conversion time. Refer to the Power Calculation section for additional information.

For applications that require approximate synchronization with other monitoring devices, the conversion start can be delayed using the CONVDLY bits in the CONFIG register. The programmable delay ranges from 0ms to 510ms in 2ms steps, with a default setting of 0ms. Because individual devices operate from independent time bases, the relative timing between devices can gradually drift after the initial alignment.

Low Latency Digital Filter

The device incorporates a low-pass digital filter that performs decimation and filtering of the ADC output data to reduce noise. The filter automatically adapts to the selected output data rate and settles within a single conversion cycle. The user can select the output conversion time, t_{CT}, from 62μs to 2502μs. For a given conversion time, the first amplitude notch occurs at the Nyquist frequency of the output signal and is defined as $f_{NOTCH} = 1/(2 \times t_{CT})$. Therefore, the filter cut-off frequency scales proportionally with the selected output data rate.

DETAILED DESCRIPTION (continued)

Figure 6 shows the ADC frequency response for the selected conversion-time setting.

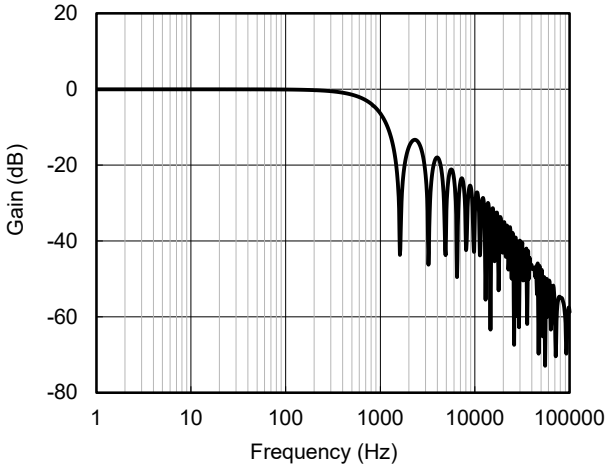


Figure 6. ADC Frequency Response

Flexible Conversion Times and Averaging

The ADC conversion times for shunt voltage, bus voltage, and temperature can be independently programmed from 62μs to 2502μs. This flexibility allows the device to provide robust measurement performance in a variety of noisy environments. The SGM839 also supports programmable averaging from a single conversion up to 1024 conversions. The selected averaging setting is applied uniformly to all enabled measurement inputs. Refer to the ADC_CONFIG register for additional information on the available conversion-time and averaging settings.

The effective ADC resolution can be improved by increasing the conversion time or the number of averaged samples. Figure 7 and Figure 8 illustrate the effects of conversion time and averaging on a constant input signal.

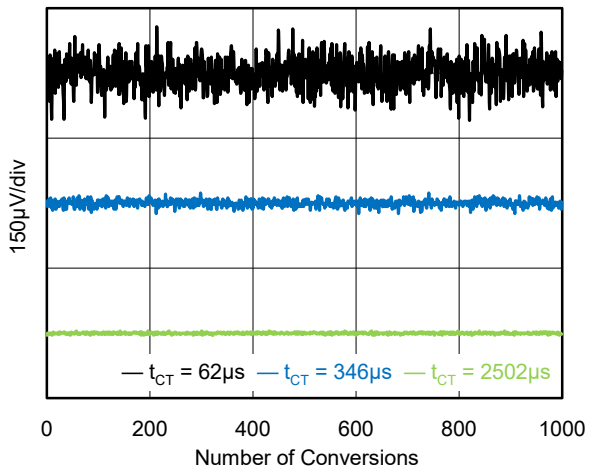


Figure 7. Noise vs. Conversion Time (Averaging = 1)

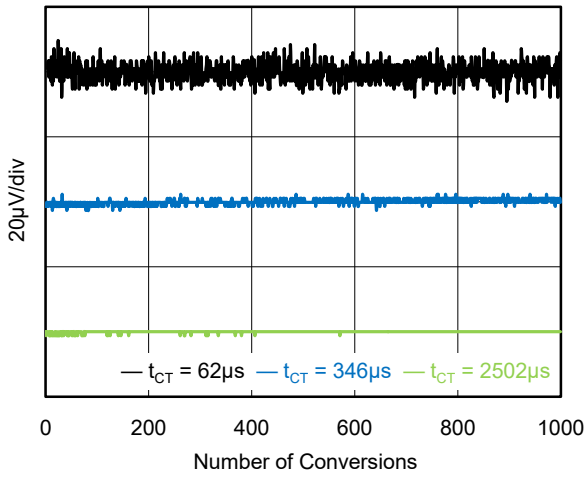


Figure 8. Noise vs. Conversion Time (Averaging = 128)

The selected conversion time and averaging count affect the effective measurement resolution. For additional information on the relationship between averaging, noise reduction, and effective number of bits (ENOB), refer to the ADC Output Data Rate and Noise Performance section.

Integrated Precision Oscillator

The SGM839 uses an internally trimmed oscillator as its time base, with a room-temperature tolerance of less than 5%. This oscillator provides the timing reference for ADC conversions. Because the digital filter characteristics depend on the selected conversion time, a stable clock helps maintain consistent filter response and notch-frequency behavior over temperature. After power-up, the internal oscillator and ADC require approximately 70μs to settle to within 1% error. Once this settling period is complete, the ADC output meets the specified electrical performance.

Multi-Alert Monitoring and Fault Detection

The SGM839 provides a multipurpose, open-drain ALERT output for fault monitoring and conversion-ready indication. Six fault conditions are supported: shunt over-voltage (SHNTOL), shunt under-voltage (SHNTUL), bus over-voltage (BUSOL), bus under-voltage (BUSUL), power over-limit (POL), and temperature over-limit (TMPOL). Each fault condition is evaluated against its corresponding programmable threshold. The ALERT output can also be configured to indicate completion of a conversion sequence.

DETAILED DESCRIPTION (continued)

The DIAG_ALRT register provides the status of the monitored fault conditions and also controls the operating behavior of the ALERT output. Reading this register allows the host controller to determine which diagnostic condition is active.

The ALATCH bit selects transparent or latched alert operation. When ALATCH = 0, the ALERT output and the corresponding diagnostic flag return to the inactive state after the fault condition is removed. When ALATCH = 1, the ALERT output and diagnostic flag remain asserted after the fault condition clears and are released when the DIAG_ALRT register is read.

The CNVR bit enables conversion-ready indication on the ALERT pin. When CNVR = 1, the ALERT output is asserted after the selected conversions and programmed averaging sequence are complete. Conversion completion can also be monitored through the CNVRF bit regardless of the CNVR setting.

The SLOWALERT bit determines whether alert thresholds are evaluated using individual conversion results or completed averaged results. When SLOWALERT = 0, each conversion result is compared with the programmed threshold. When SLOWALERT = 1, threshold comparison is performed using the averaged result. Using averaged data can reduce false alerts caused by measurement noise, but increases the fault-reporting latency because the averaging sequence must be completed first.

The APOL bit controls the active polarity of the ALERT output. The default setting is active low. Setting APOL = 1 configures ALERT as active high. Because the ALERT pin is an open-drain output, an external pull-up resistor is required.

The DIAG_ALRT register also contains diagnostic information that is not directly used as an ALERT threshold condition. The MATHOF bit indicates that an internal arithmetic operation has overflowed and that the calculated current or power result may be invalid. The MATHOF flag is cleared by triggering another conversion. The MEMSTAT bit indicates the status of the device nonvolatile trim memory and reads 1 during normal operation.

When conversion-ready indication is enabled together with the fault-monitoring functions, the ALERT pin operates as a shared status output. Figure 9 illustrates an example in which conversion-complete events are reported while shunt over-voltage, bus under-voltage, temperature over-limit, and power over-limit conditions occur.

Table 1. ALERT Diagnostics Description

Diagnostic	Status Bit in DIAG_ALRT Register (R)	Out-Of-Range Threshold Register (R/$\overline{W}$)	Register Default Value
Shunt Under-Voltage Limit	SHNTUL	SUVL	8000h (two's-complement)
Shunt Over-Voltage Limit	SHNTOL	SOVL	7FFFh (two's-complement)
Bus Voltage Over-Limit	BUSOL	BOVL	7FFFh (two's-complement, positive values only)
Bus Voltage Under-Limit	BUSUL	BUVL	0000h (two's-complement, positive values only)
Temperature Over-Limit	TMPOL	TEMP_LIMIT	7FF0h (two's-complement)
Power Over-Limit	POL	PWR_LIMIT	FFFFh (two's-complement, positive values only)

DETAILED DESCRIPTION (continued)

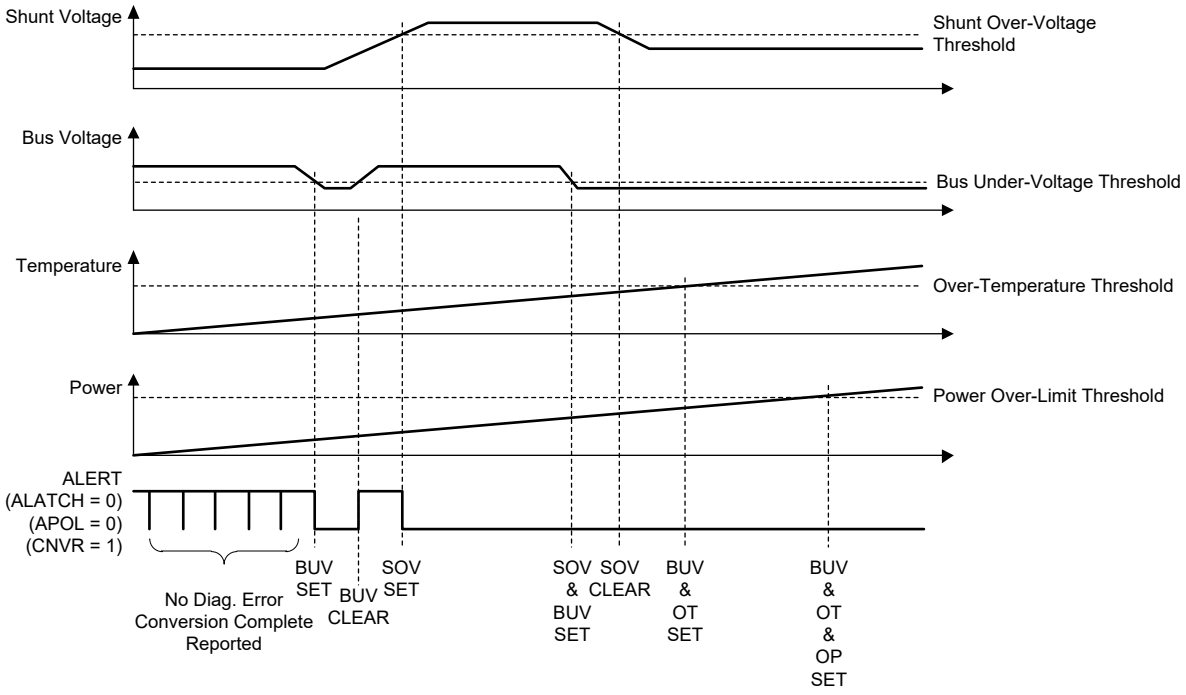


Figure 9. Multi-Alert Configuration

Device Functional Modes

Shutdown Mode

The SGM839 supports a shutdown mode in addition to continuous and triggered conversion modes. Shutdown mode is selected through the MODE bits in the ADC_CONFIG register. In this mode, ADC conversions are stopped and the device quiescent current is reduced to 3.8μA (TYP). The device registers remain accessible through the SPI interface while the device is in shutdown mode.

The SGM839 remains in shutdown mode until the MODE bits are programmed for a triggered or continuous conversion mode. When a triggered conversion is initiated from shutdown, the SGM839 will automatically enter power-save mode.

The specified shutdown current assumes that the SPI interface is inactive. SPI clock and data activity increase device current consumption as a function of the communication frequency.

Power-On Reset

Power-on reset (POR) resets the device registers to their default values when the supply voltage, V_S, falls below the POR threshold. A manual reset can also be initiated by setting the RST bit in the CONFIG register. A manual reset has the same effect on the register contents as a power-on reset, and the RST bit automatically clears after the reset is initiated. The default value of each register is listed in the corresponding register description.

Serial Interface

The SGM839 communicates with an external MCU through a 4-wire, full-duplex SPI interface. The MCU operates as the SPI controller, while the SGM839 operates as the peripheral device. Commands and write data are transferred to the SGM839 through MOSI, and register data are returned through MISO.

The SPI interface consists of the following signals:

- CS — Chip-select input, active low.
- SCLK — Serial clock input.
- MOSI — Serial data input to the SGM839.
- MISO — Serial data output from the SGM839. The output is push-pull while selected and high impedance when CS is high.

The SPI interface supports clock frequencies up to 10MHz. Command and data fields are transferred MSB first. MOSI data are sampled on the falling edge of SCLK, while MISO data are shifted out on the rising edge of SCLK.

DETAILED DESCRIPTION (continued)

An SPI transaction begins when CS transitions low and ends when CS returns high. While CS is high, the SPI interface remains idle and the MISO output is placed in the high-impedance state.

Because MISO is a push-pull output referenced to the SGM839 supply voltage, V_S, it is recommended that the MCU I/O supply use the same voltage as V_S. If the two devices operate from different logic-supply voltages, appropriate level translation should be used.

SPI Frame

Each SPI transaction begins with an 8-bit command byte consisting of a 6-bit register address, one reserved bit, and one read/write control bit. Bits [7:2] contain the register address, bit [1] must be written as 0, and bit [0] is the R/W bit. Setting the R/W bit to 1 selects a register read operation, while setting it to 0 selects a register write operation.

For a read operation, the MCU first transmits the 8-bit command byte and then continues providing SCLK cycles while the SGM839 shifts the contents of the selected register onto MISO. The number of data bits depends on the register width. Most SGM839 registers are 16 bits wide and therefore use a 24-bit read frame consisting of the 8-bit command byte followed by 16 data bits. The POWER register is 24 bits wide and therefore requires a 32-bit read frame.

All writable SGM839 registers are 16 bits wide. Therefore, an SPI write transaction always consists of an 8-bit command byte followed by 16 bits of write data, for a total frame length of 24 bits. During a write transaction, the new register value is shifted into the SGM839 through MOSI while the previous contents of the addressed register are simultaneously shifted out through MISO.

The command-byte format is summarized in Table 2. During a read transaction, the requested register data are returned by the SGM839 within the same SPI frame.

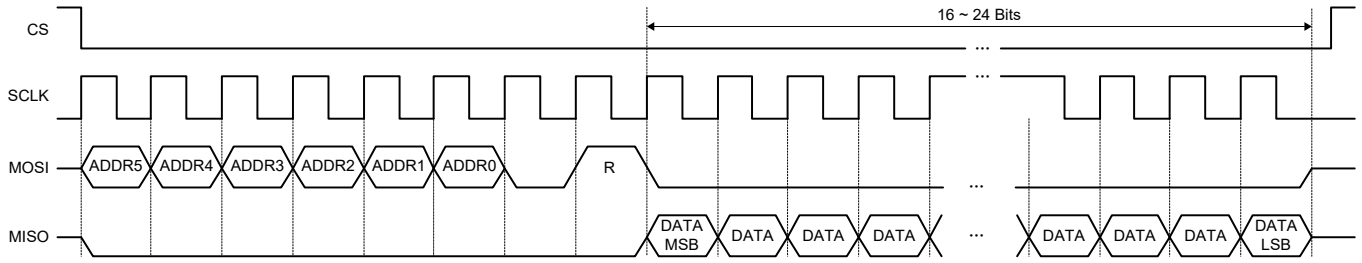


Figure 10. SPI Read Frame

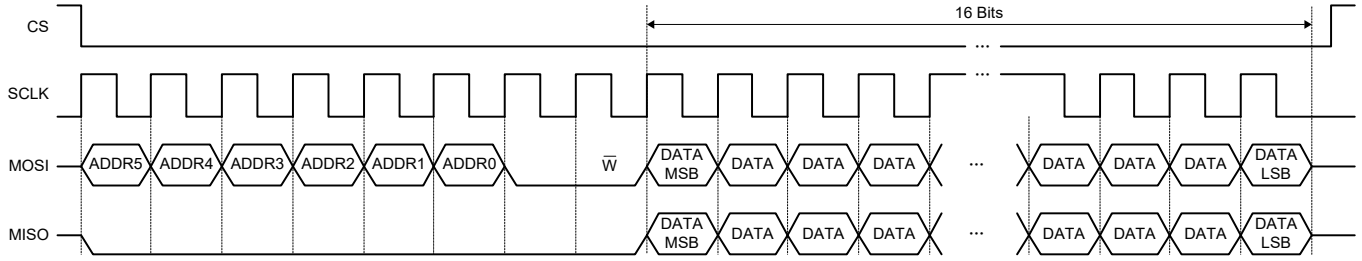


Figure 11. SPI Write Frame

Table 2. SPI Command Byte Format

COMMAND	B7	B6	B5	B4	B3	B2	B1	B0
READ	ADDR5	ADDR4	ADDR3	ADDR2	ADDR1	ADDR0	0	1
WRITE								0

REGISTER MAPS

All register addresses not listed in Table 3 are reserved. Reserved register addresses should not be written.

Table 3. SGM839 Registers Definition

ADDRESS	REGISTER NAME	ACRONYM	REGISTER SIZE (BITS)
0h	Configuration	CONFIG	16
1h	ADC Configuration	ADC_CONFIG	16
2h	Shunt Calibration	SHUNT_CAL	16
4h	Shunt Voltage Measurement	VSHUNT	16
5h	Bus Voltage Measurement	VBUS	16
6h	Temperature Measurement	DIETEMP	16
7h	Current Result	CURRENT	16
8h	Power Result	POWER	24
Bh	Diagnostic Flags and Alert	DIAG_ALRT	16
Ch	Shunt Over-Voltage Threshold	SOVL	16
Dh	Shunt Under-Voltage Threshold	SUVL	16
Eh	Bus Over-Voltage Threshold	BOVL	16
Fh	Bus Under-Voltage Threshold	BUVL	16
10h	Temperature Over-Limit Threshold	TEMP_LIMIT	16
11h	Power Over-Limit Threshold	PWR_LIMIT	16
3Eh	Manufacturer ID	MANUFACTURER_ID	16
3Fh	Device ID	DEVICE_ID	16

Bits Type: R = Read-Only, R/W = Read/Write.

0h: Configuration (CONFIG) Register [reset = 0h]

BITS	BIT NAME	TYPE	RESET	DESCRIPTION
D[15]	RST	W	0h	Device Reset Bit. Writing 1 to this bit initiates a device reset equivalent to a power-on reset and restores the registers to their default values. Writing 0 has no effect. This bit is self-clearing.
D[14]	RESERVED	R	0h	Reserved. Reads as 0.
D[13:6]	CONVDLY	R/W	0h	Sets the delay before the start of the ADC conversion sequence in 2ms steps. 00h = 0ms 01h = 2ms FFh = 510ms
D[5]	RESERVED	R	0h	Reserved. Always reads 0.
D[4]	ADCRANGE	R/W	0h	Selects the full-scale differential input range between IN+ and IN- pins. 0h = ±163.84mV 1h = ±40.96mV.
D[3:0]	RESERVED	R	0h	Reserved. Reads as 0.

REGISTER MAPS (continued)

1h: ADC Configuration (ADC_CONFIG) Register [reset = FB68h]

BITS	BIT NAME	TYPE	RESET	DESCRIPTION
D[15:12]	MODE	R/W	Fh	Selects the device operating mode and the measurement inputs enabled for conversion. In a triggered mode, the selected conversion and averaging sequence is performed once, after which the device returns to shutdown mode. 0h = Shutdown 1h = Triggered bus voltage conversion 2h = Triggered shunt voltage conversion 3h = Triggered shunt and bus voltage conversions 4h = Triggered temperature conversion 5h = Triggered temperature and bus voltage conversions 6h = Triggered temperature and shunt voltage conversions 7h = Triggered bus voltage, shunt voltage, and temperature conversions 8h = Shutdown 9h = Continuous bus voltage conversion Ah = Continuous shunt voltage conversion Bh = Continuous shunt and bus voltage conversions Ch = Continuous temperature conversion Dh = Continuous bus voltage and temperature conversions Eh = Continuous temperature and shunt voltage conversions Fh = Continuous bus voltage, shunt voltage, and temperature conversions
D[11:9]	VBUSCT	R/W	5h	Bus Voltage Conversion Time Setting Bits. 0h = 62μs 1h = 80μs 2h = 117μs 3h = 193μs 4h = 346μs 5h = 654μs 6h = 1269μs 7h = 2502μs
D[8:6]	VSHCT	R/W	5h	Shunt Voltage Conversion Time Setting Bits. 0h = 62μs 1h = 80μs 2h = 117μs 3h = 193μs 4h = 346μs 5h = 654μs 6h = 1269μs 7h = 2502μs
D[5:3]	VTCT	R/W	5h	Temperature Conversion Time Setting Bits. 0h = 62μs 1h = 80μs 2h = 117μs 3h = 193μs 4h = 346μs 5h = 654μs 6h = 1269μs 7h = 2502μs
D[2:0]	AVG	R/W	0h	Selects the number of ADC samples used for averaging. The selected averaging setting applies to all enabled measurement inputs. When averaging is enabled, the corresponding output registers are updated after the programmed averaging sequence is complete. 0h = 1 1h = 4 2h = 16 3h = 64 4h = 128 5h = 256 6h = 512 7h = 1024

REGISTER MAPS (continued)

2h: Shunt Calibration (SHUNT_CAL) Register [reset = 1000h]

BITS	BIT NAME	TYPE	RESET	DESCRIPTION
D[15]	RESERVED	R	0h	Reserved. Reads as 0.
D[14:0]	SHUNT_CAL	R/W	1000h	Stores the calibration coefficient used by the device to calculate current from the measured shunt voltage. The SHUNT_CAL value is programmed based on the selected CURRENT_LSB and the external shunt resistance, RSHUNT. Refer to the Current and Power Calculations section for the SHUNT_CAL calculation.

4h: Shunt Voltage Measurement (VSHUNT) Register [reset = 0h]

BITS	BIT NAME	TYPE	RESET	DESCRIPTION
D[15:0]	VSHUNT	R	0000h	Contains the measured differential voltage between the IN+ and IN- pins. The result is represented in 16-bit two's-complement format. Conversion factor: 5μV/LSB when ADCRANGE = 0 1.25μV/LSB when ADCRANGE = 1

5h: Bus Voltage Measurement (VBUS) Register [reset = 0h]

BITS	BIT NAME	TYPE	RESET	DESCRIPTION
D[15:0]	VBUS	R	0000h	Contains the measured bus voltage at the VBUS pin with respect to GND. Conversion factor: 3.125mV/LSB.

6h: Temperature Measurement (DIETEMP) Register [reset = 0h]

BITS	BIT NAME	TYPE	RESET	DESCRIPTION
D[15:4]	DIETEMP	R	000h	Contains the measured internal die temperature in 12-bit two's-complement format. Conversion factor: 125m℃/LSB.
D[3:0]	RESERVED	R	0h	Reserved. Reads as 0.

7h: Current Result (CURRENT) Register [reset = 0h]

BITS	BIT NAME	TYPE	RESET	DESCRIPTION
D[15:0]	CURRENT	R	0000h	Contains the calculated current result in 16-bit two's-complement format. Convert the signed register value to current in amperes using the programmed CURRENT_LSB. Refer to the Current and Power Calculations section for the conversion equation.

8h: Power Result (POWER) Register [reset = 0h]

BITS	BIT NAME	TYPE	RESET	DESCRIPTION
D[23:0]	POWER	R	000000h	Contains the calculated power result as a 24-bit unsigned value. Convert the register value to power in watts using the programmed CURRENT_LSB. Refer to the Current and Power Calculations section for the conversion equation.

REGISTER MAPS (continued)

Bh: Diagnostic Flags and Alert (DIAG_ALRT) Register [reset = 0001h]

BITS	BIT NAME	TYPE	RESET	DESCRIPTION
D[15]	ALATCH	R/W	0h	Selects the latch behavior of the ALERT output and diagnostic flags. 0h = Transparent mode 1h = Latched mode In transparent mode, the ALERT output and the corresponding diagnostic flag return to the inactive state when the fault condition is removed. In latched mode, the ALERT output and the corresponding diagnostic flag remain active after the fault condition is removed until the DIAG_ALRT register is read.
D[14]	CNVR	R/W	0h	Enables the conversion-ready indication on the ALERT pin. 0h = Conversion-ready indication disabled on ALERT 1h = Conversion-ready indication enabled on ALERT When enabled, the ALERT output is asserted when the CNVRF bit is set, indicating that the conversion sequence has completed.
D[13]	SLOWALERT	R/W	0h	Selects the data used for alert-threshold comparison. 0h = ALERT comparison uses individual ADC conversion results 1h = ALERT comparison uses completed averaged results Using averaged results can reduce alert responses caused by measurement noise, but increases the alert response time because the averaging sequence must first be completed.
D[12]	APOL	R/W	0h	Selects the active polarity of the ALERT pin. 0h = Active low 1h = Active high The ALERT pin is an open-drain output and requires an external pull-up resistor.
D[11:10]	RESERVED	R	0h	Reserved. Always reads 0.
D[9]	MATHOF	R	0h	Indicates that an internal arithmetic operation has resulted in an overflow. The calculated current or power result may be invalid when this flag is set. 0h = Normal operation 1h = Math overflow The flag is cleared by triggering another conversion.
D[8]	RESERVED	R	0h	Reserved. Always reads 0.
D[7]	TMPOL	R	0h	Indicates whether the measured die temperature exceeds the threshold programmed in the TEMP_LIMIT register. 0h = Normal 1h = Temperature over-limit event When ALATCH = 1, this flag is cleared by reading the DIAG_ALRT register.
D[6]	SHNTOL	R	0h	Indicates whether the measured shunt voltage exceeds the threshold programmed in the SOVL register. 0h = Normal 1h = Shunt over-voltage event When ALATCH = 1, this flag is cleared by reading the DIAG_ALRT register.
D[5]	SHNTUL	R	0h	Indicates whether the measured shunt voltage falls below the threshold programmed in the SUVL register. 0h = Normal 1h = Shunt under-voltage event When ALATCH = 1, this flag is cleared by reading the DIAG_ALRT register.

REGISTER MAPS (continued)

Bh: Diagnostic Flags and Alert (DIAG_ALRT) Register [reset = 0001h] (continued)

BITS	BIT NAME	TYPE	RESET	DESCRIPTION
D[4]	BUSOL	R	0h	Indicates whether the measured bus voltage exceeds the threshold programmed in the BOVL register. 0h = Normal 1h = Bus over-voltage event When ALATCH = 1, this flag is cleared by reading the DIAG_ALRT register.
D[3]	BUSUL	R	0h	Indicates whether the measured bus voltage falls below the threshold programmed in the BUVL register. 0h = Normal 1h = Bus under-voltage event When ALATCH = 1, this flag is cleared by reading the DIAG_ALRT register.
D[2]	POL	R	0h	Indicates whether the calculated power exceeds the threshold programmed in the PWR_LIMIT register. 0h = Normal 1h = Power over-limit event When ALATCH = 1, this flag is cleared by reading the DIAG_ALRT register.
D[1]	CNVRF	R	0h	Conversion-ready flag. This bit is set after all selected conversions and programmed averaging are complete. 0h = Conversion sequence not complete 1h = Conversion sequence complete The flag is cleared by reading the DIAG_ALRT register or by writing the ADC_CONFIG register, except when shutdown mode is selected.
D[0]	MEMSTAT	R	1h	Indicates the status of the device nonvolatile trim memory. 0h = Memory checksum error 1h = Normal operation

Ch: Shunt Over-Voltage Threshold (SOVL) Register [reset = 7FFFh]

If negative values are entered in this register, then a shunt voltage measurement of 0V will trip this alarm. When using negative values for the shunt under and over-voltage thresholds be aware that the over-voltage threshold must be set to the larger (that is, less negative) of the two values.

BITS	BIT NAME	TYPE	RESET	DESCRIPTION
D[15:0]	SOVL	R/W	7FFFh	Shunt over-voltage (over-current protection) threshold value in two's-complement. Conversion Factor: 5μV/LSB when ADCRANGE = 0 1.25μV/LSB when ADCRANGE = 1.

Dh: Shunt Under-Voltage Threshold (SUVL) Register [reset = 8000h]

BITS	BIT NAME	TYPE	RESET	DESCRIPTION
D[15:0]	SUVL	R/W	8000h	Shunt under-voltage (under-current protection) threshold value in two's-complement. Conversion Factor: 5μV/LSB when ADCRANGE = 0 1.25μV/LSB when ADCRANGE = 1.

Eh: Bus Over-Voltage Threshold (BOVL) Register [reset = 7FFFh]

BITS	BIT NAME	TYPE	RESET	DESCRIPTION
D[15]	Reserved	R	0h	Reserved. Always reads 0.
D[14:0]	BOVL	R/W	7FFFh	Bus over-voltage (over-voltage protection) threshold value in unsigned representation, positive value only. Conversion factor: 3.125mV/LSB.

REGISTER MAPS (continued)

Fh: Bus Under-Voltage Threshold (BUVL) Register [reset = 0h]

BITS	BIT NAME	TYPE	RESET	DESCRIPTION
D[15]	Reserved	R	0h	Reserved. Always reads 0.
D[14:0]	BUVL	R/W	0h	Bus under-voltage (under-voltage protection) threshold value in unsigned representation, positive value only. Conversion factor: 3.125mV/LSB.

10h: Temperature Over-Limit Threshold (TEMP_LIMIT) Register [reset = 7FF0h]

BITS	BIT NAME	TYPE	RESET	DESCRIPTION
D[15:4]	TOL	R/W	7FFh	Over-temperature threshold value in two's-complement. The value entered in this field compares directly against the value from the DIETEMP register to determine if an over temperature condition exists. Conversion factor: 125m°C/LSB.
D[3:0]	Reserved	R	0h	Reserved, always reads 0

11h: Power Over-Limit Threshold (PWR_LIMIT) Register [reset = FFFFh]

BITS	BIT NAME	TYPE	RESET	DESCRIPTION
D[15:0]	POL	R/W	FFFFh	Power over-limit threshold value Setting Bits. Unsigned representation, positive value only. The value entered in this field compares directly against the value from the POWER register to determine if an over power condition exists. Conversion factor: 256 × Power LSB.

3Eh: Manufacturer ID (MANUFACTURER_ID) Register [reset = 5449h]

BITS	BIT NAME	TYPE	RESET	DESCRIPTION
D[15:0]	MANFID	R	5449h	Manufacturer ID Bits. Store the manufacturer identification bits.

3Fh: Device ID (DEVICE_ID) Register [reset = 2391h]

BITS	BIT NAME	TYPE	RESET	DESCRIPTION
D[15:4]	DIEID	R	239h	Device ID Bits.
D[3:0]	REV_ID	R	1h	Device Revision ID Bits.

APPLICATION INFORMATION

Device Measurement Range and Resolution

The SGM839 supports two full-scale input ranges for shunt voltage measurement. The differential input range between the IN+ and IN- pins is ±163.84mV when ADCRANGE = 0 and ±40.96mV when ADCRANGE = 1. The bus voltage measurement range is 0V to 85V. The die temperature output uses a 12-bit two's-complement format with a resolution of 125m℃/LSB, corresponding to a representable code range of -256℃ to +255.875℃. The specified die temperature measurement range of the SGM839 is -40℃ to +125℃.

Table 4 summarizes the measurement ranges and corresponding LSB resolutions for shunt voltage, bus voltage, and die temperature.

Table 4. Measurement Ranges and Resolutions

Parameter	Measurement Range	Resolution
Shunt voltage	±163.84mV (ADCRANGE = 0)	5μV/LSB
	±40.96mV (ADCRANGE = 1)	1.25μV/LSB
Bus voltage	0V to 85V	3.125mV/LSB
Temperature	-40℃ to +125℃	125m℃/LSB

Shunt voltage, bus voltage, and die temperature results are available in the VSHUNT, VBUS, and DIETEMP registers, respectively. VSHUNT and VBUS are 16-bit registers, while the valid die temperature result occupies D[15:4] of the DIETEMP register.

The VSHUNT result is represented in two's-complement format and can therefore represent either positive or negative differential voltage. The VBUS result represents a nonnegative bus voltage over the specified measurement range. Convert the VSHUNT and VBUS register values to volts using their corresponding LSB resolutions.

The DIETEMP result is a 12-bit two's-complement value. After interpreting the signed code, multiply the result by 125m℃/LSB to obtain the die temperature in degrees Celsius.

The SGM839 also calculates current and power from the measured shunt and bus voltages. The CURRENT and POWER register scaling is described in the Current and Power Calculations section.

Current and Power Calculations

To calculate current and power correctly, the SHUNT_CAL register must be programmed according to the external shunt resistance and the selected CURRENT_LSB. CURRENT_LSB defines the current represented by one LSB of the CURRENT register and therefore determines the current-reporting resolution.

The minimum CURRENT_LSB value can be calculated from the maximum expected current using Equation 2. Using the minimum value provides the highest CURRENT register resolution. For simpler conversion between register codes and engineering units, a convenient rounded-up CURRENT_LSB value can be selected, provided that it does not exceed eight times the minimum value.

The SHUNT_CAL value is calculated from CURRENT_LSB and the external shunt resistance, RSHUNT, using Equation 1. R_{SHUNT} is the resistance of the external shunt connected between the IN+ and IN- pins. Equation 1 applies directly when ADCRANGE = 0. When ADCRANGE = 1, the calculated SHUNT_CAL value must be multiplied by 4.

$$SHUNT_CAL = 819.2 \times 10^6 \times CURRENT_LSB \times R_{SHUNT} \quad (1)$$

where:

- CURRENT_LSB is expressed in amperes per LSB.
- R_{SHUNT} is expressed in ohms.
- 819.2×10^6 is the internal scaling constant used for the current calculation.
- For ADCRANGE = 1, multiply the result of Equation 1 by 4.

The minimum CURRENT_LSB is calculated as:

$$CURRENT_LSB = \frac{\text{Maximum Expected Current}}{2^{15}} \quad (2)$$

where:

Current is calculated after a shunt voltage conversion using the calibration value programmed in the SHUNT_CAL register. If SHUNT_CAL is set to zero, the CURRENT register reports zero.

After SHUNT_CAL has been programmed, convert the signed CURRENT register value to amperes using Equation 3:

$$\text{Current (A)} = CURRENT_LSB \times CURRENT \quad (3)$$

where:

CURRENT is the signed value read from the CURRENT register.

APPLICATION INFORMATION (continued)

The POWER register contains a 24-bit unsigned power result. Convert the POWER register value to watts using Equation 4:

$$Power\ (W) = 0.2 \times CURRENT_LSB \times POWER \quad (4)$$

where:

- POWER is the value read from the POWER register.
- CURRENT_LSB is the current LSB selected using Equation 2.

Refer to the Configure the Device section for a design example using these equations.

ADC Output Data Rate and Noise Performance

The noise performance and effective resolution of the SGM839 depend on the selected ADC conversion time and averaging setting. Increasing the conversion time or the number of averaged samples reduces measurement noise and improves the effective resolution, at the expense of a longer measurement update time.

The SGM839 provides eight programmable conversion-time settings from 62μs to 2502μs and supports averaging from 1 to 1024 samples. The conversion time for each enabled measurement input can be programmed independently, while the selected averaging setting applies to all enabled inputs.

Table 5 summarizes the measured noise performance for the supported conversion-time and averaging configurations. Noise-free resolution is expressed as effective number of bits (ENOB) and is calculated from the measured peak-to-peak noise.

The fastest available conversion-time setting is 62μs. Longer conversion times and higher averaging counts generally provide higher ENOB, while shorter conversion times and lower averaging counts provide faster measurement response.

Table 5. Noise Performance

ADC Conversion Time Period (μs)	Output Sample Averaging (Samples)	Output Sample Period (ms)	Noise-Free ENOB (±163.84mV) (ADCRANGE = 0)	Noise-Free ENOB (±40.96mV) (ADCRANGE = 1)
62	1	0.062	10.71	8.64
80		0.08	11.25	9.11
117		0.117	11.54	9.54
193		0.193	12.09	10.02
346		0.346	12.83	10.61
654		0.654	13.42	11.25
1269		1.269	14	11.91
2502		2.502	14	12.42
62	4	0.248	11.54	9.22
80		0.32	12	10.07
117		0.468	12.68	10.68
193		0.772	13.42	11.3
346		1.384	13.68	11.75
654		2.616	14.42	12.3
1269		5.076	15	12.83
2502		10.008	15	14
62	16	0.992	12.54	10.51
80		1.28	13	11.19
117		1.872	13.68	11.68
193		3.088	14.42	12.09
346		5.536	15	12.68
654		10.464	15	13.19
1269		20.304	16	13.42
2502		40.032	16	15

APPLICATION INFORMATION (continued)

ADC Conversion Time Period (μs)	Output Sample Averaging (Samples)	Output Sample Period (ms)	Noise-Free ENOB (±163.84mV) (ADCRANGE = 0)	Noise-Free ENOB (±40.96mV) (ADCRANGE = 1)
62	64	3.968	13.42	11.54
80		5.12	14.42	12.19
117		7.488	14.42	12.42
193		12.352	16	13.19
346		22.144	16	14
654		41.856	16	14.42
1269		81.216	16	14.42
2502		160.128	16	15
62	128	7.936	14	12.19
80		10.24	15	12.42
117		14.976	16	13
193		24.704	16	13.68
346		44.288	16	14
654		83.712	16	15
1269		162.432	16	16
2502		320.256	16	16
62	256	15.872	14.42	12.54
80		20.48	15	13
117		29.952	16	13.68
193		49.408	16	14.42
346		88.576	16	15
654		167.424	16	15
1269		324.864	16	16
2502		640.512	16	16
62	512	31.744	15	13.19
80		40.96	16	13.68
117		59.904	16	14
193		98.816	16	15
346		177.152	16	15
654		334.848	16	16
1269		649.728	16	16
2502		1281.024	16	16
62	1024	63.488	16	13.68
80		81.92	16	14
117		119.808	16	14.42
193		197.632	16	15
346		354.304	16	16
654		669.696	16	16
1269		1299.456	16	16
2502		2562.048	16	16

APPLICATION INFORMATION (continued)

Input Filtering Considerations

The SGM839 provides programmable digital filtering through the conversion-time and averaging settings in the ADC_CONFIG register. The conversion times for shunt voltage, bus voltage, and die temperature measurements can be programmed independently, while the selected averaging setting is applied to all enabled measurement inputs.

The sigma-delta ADC provides inherent rejection of out-of-band noise. However, high-frequency transients near the ADC sampling-frequency harmonics can still affect measurement accuracy. When additional input filtering is required, a low-value series resistor can be placed in each of the IN+ and IN- paths together with a ceramic differential capacitor, as shown in Figure 12. Use the lowest practical series resistance to minimize measurement error. R_{FILTER} values of 100Ω or less and capacitor values from 0.1μF to 1μF are recommended.

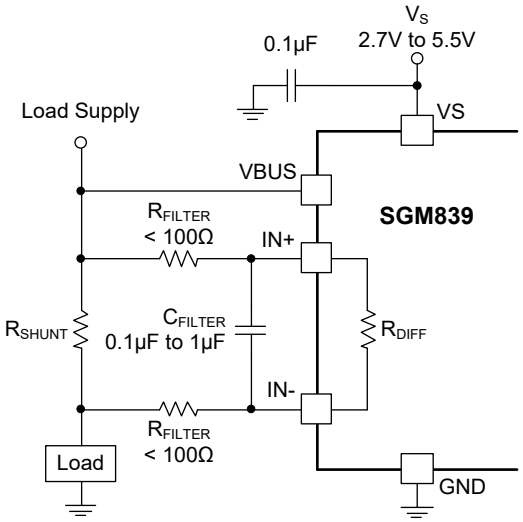


Figure 12. Input Filtering

Input overstress conditions must also be considered. The IN+ and IN- inputs are rated for a differential voltage of -40V to +40V, while the common-mode input voltage absolute maximum range is -4V to +85V. A fault such as a short-circuit on the load side of the shunt can temporarily produce a large differential voltage across the shunt resistor. When the fault is removed, parasitic inductance in the power path can generate kickback transients that exceed the device input ratings. Appropriate transient-suppression devices and energy-storage components should therefore be used as required by the application to keep the input voltages within the absolute maximum ratings.

Rapid input-voltage transitions can also produce high dV/dt stress at the device inputs. Series input resistance can help limit transient current into the input protection structures. The required protection network depends on the available fault current, source impedance, parasitic inductance, and transient environment of the application. The final input network should be verified under the expected system fault conditions.

Do not use R_{FILTER} values greater than 100Ω. Larger series resistance can increase measurement error and degrade linearity.

Typical Application

The low offset voltage and low input bias current of the SGM839 enable accurate current measurement over a wide dynamic range. To maximize measurement resolution, select the shunt resistance so that the differential voltage developed across the shunt at the maximum expected current approaches, but does not exceed, the selected shunt full-scale range. The available shunt full-scale ranges are ±163.84mV and ±40.96mV, as selected by the ADCRANGE bit in the CONFIG register.

Figure 13 shows a typical high-side current-sensing application using the SGM839.

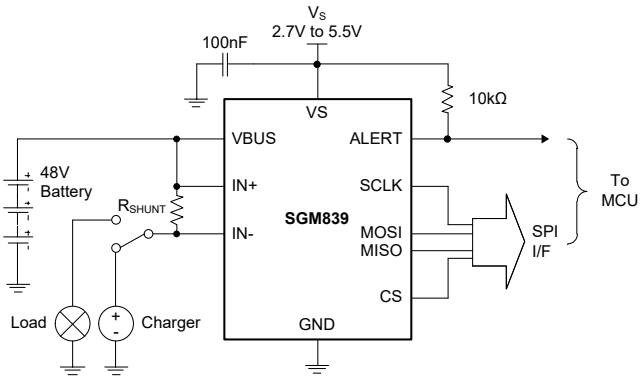


Figure 13. SGM839 High-Side Sensing Application Diagram

APPLICATION INFORMATION (continued)

Design Requirements

The SGM839 measures the differential voltage developed across an external current-sensing resistor, RSHUNT, and measures the bus voltage through the VBUS pin. After the SHUNT_CAL register is properly programmed, the device calculates current and power from the measured values.

The ALERT pin can be configured to indicate programmable out-of-range conditions or ADC conversion completion.

Table 6 lists the example design requirements for the circuit shown in Figure 13.

Table 6. Design Parameters

Design Parameter	Example Value
Power-Supply Voltage (V_S)	5V
Bus Supply Rail (V_{CM})	48V
Bus Supply Rail Over-Voltage Fault Threshold	52V
Average Current	6A
Over-Current Fault Threshold (I_{MAX})	10A
ADC Range Selection (V_{SENSE_MAX})	±163.84mV
Temperature	+25℃

Select the Shunt Resistor

The maximum allowable shunt resistance is determined from the maximum current to be measured, I_{MAX}, and the full-scale sense voltage, V_{SENSE_MAX}, selected for the ADC range. At I_{MAX}, the differential voltage developed across the shunt must remain within V_{SENSE_MAX}. Based on the design values in Table 6 and Equation 5, the calculated maximum R_{SHUNT} is 16.38mΩ. A standard value below this limit should be selected; in this example, 16.2mΩ is used. The selected shunt resistor must also have sufficient power-rating capability for the maximum load condition.

$$R_{SHUNT} < \frac{V_{SENSE_MAX}}{I_{MAX}} \quad (5)$$

Configure the Device

The CONFIG and ADC_CONFIG registers determine the primary operating and ADC conversion settings of the SGM839. After power-up or reset, these registers return to their default values.

By default, ADCRANGE = 0, selecting the ±163.84mV shunt full-scale range. The ADC_CONFIG register resets to FB68h, which selects continuous conversion of bus voltage, shunt voltage, and die temperature, with a conversion time of 654μs for each measurement and averaging set to 1.

If the default configuration does not meet the application requirements, program the CONFIG and ADC_CONFIG registers with the required settings after power-up or device reset.

Program the Shunt Calibration Register

The SHUNT_CAL register must be programmed with the appropriate calibration value for the device to report valid current and power results. After power-up or a device reset, SHUNT_CAL returns to its default value and should be reprogrammed if the application requires a different calibration value.

First, calculate CURRENT_LSB using Equation 2. For the maximum expected current of 10A in this example, the minimum CURRENT_LSB is 305.1758μA/LSB. Using this CURRENT_LSB and the selected shunt resistance of 16.2mΩ in Equation 1 gives:

SHUNT_CAL = 4050d = FD2h

If SHUNT_CAL is set to zero, the CURRENT register reports zero and the calculated power result is also zero.

Set Desired Fault Thresholds

Fault thresholds are configured by programming the corresponding limit registers listed in Table 1.

For over-current detection, program the SOVL register with the shunt voltage threshold corresponding to the desired current limit. The required threshold voltage is calculated from the over-current limit and the shunt resistance:

$$V_{SHUNT_LIMIT} = I_{MAX} \times R_{SHUNT}$$

For the example in Table 6:

$$V_{SHUNT_LIMIT} = 10A \times 16.2m\Omega = 162mV$$

With ADCRANGE = 0, the shunt voltage LSB is 5μV/LSB. Therefore, the required SOVL register value is:

SOVL = 162mV/5μV = 32400d = 7E90h

APPLICATION INFORMATION (continued)

For bus over-voltage detection, program the BOVL register with the desired bus voltage threshold. The BOVL register uses a resolution of 3.125mV/LSB. For the 52V threshold in this example:

BOVL = 52V/3.125mV = 16640d = 4100h

For power over-limit detection, the effective LSB of the PWR_LIMIT register is 256 times the LSB of the 24-bit POWER register. Since the POWER register LSB is:

POWER_LSB = 0.2 × CURRENT_LSB

The PWR_LIMIT threshold resolution is:

PWR_LIMIT_LSB = 256 × POWER_LSB
= 51.2 × CURRENT_LSB

The required PWR_LIMIT register value can therefore be calculated by dividing the desired power threshold by PWR_LIMIT_LSB.

The fault-threshold registers return to their default values after power-up or a device reset. Reprogram any application-specific thresholds after these events.

Calculate Returned Values

Convert the register results to engineering units using the corresponding LSB values. Table 7 shows example register values and the calculated measurement results for the operating conditions listed in Table 6.

The VSHUNT and CURRENT registers contain 16-bit two's-complement values, and the DIETEMP result in D[15:4] is a 12-bit two's-complement value. These measurements can therefore represent either positive or negative values. The VBUS result is nonnegative over the specified bus voltage measurement range, and the POWER register contains a 24-bit unsigned value.

For a two's-complement result, a value with the most significant bit set to 1 represents a negative number. To obtain its magnitude manually, invert all bits of the signed field and add 1, then apply a negative sign to the resulting value.

For example, assume the VSHUNT register returns:

1011 0100 0001 0000

Because the most significant bit is 1, the value is negative. Inverting the bits and adding 1 gives:

0100 1011 1111 0000 = 19440d

Using a shunt voltage resolution of 5μV/LSB:

V_{SHUNT} = -19440 × 5μV = -97.2mV

Application Curves

Figure 14 and Figure 15 illustrate the ALERT response to a bus over-voltage fault during bus voltage only conversions with averaging set to 1 and SLOWALERT = 0. Persistence is enabled on the ALERT waveform to show the variation in response time over multiple fault events.

For a fault that significantly exceeds the programmed threshold, the ALERT response can occur before the completion of a full conversion period, as illustrated in Figure 14. For a fault that only slightly exceeds the threshold, the ALERT response can vary from approximately 0.7 to 1.7 conversion periods, as shown in Figure 15.

This variation occurs because the external fault event is asynchronous to the internal ADC conversion sequence. The response time also depends on the signal level at the time the fault occurs and its distance from the programmed threshold. For applications in which the maximum alert response time is critical, use 1.7 times the selected conversion time as the design estimate for bus voltage only or shunt voltage only conversions.

Table 7. Example Register Values and Calculated Results

Parameter	Returned Value	LSB Value	Calculated Value
Shunt Voltage (V)	19440d	5μV/LSB	0.0972V
Current (A)	19660d	$10A/2^{15}$ = 305.176μA/LSB	5.9998A
Bus Voltage (V)	15360d	3.125mV/LSB	48V
Power (W)	4718604d	CURRENT_LSB × 0.2 = 61.035156μW/LSB	288W
Temperature (℃)	200d	125m℃/LSB	+25℃

APPLICATION INFORMATION (continued)

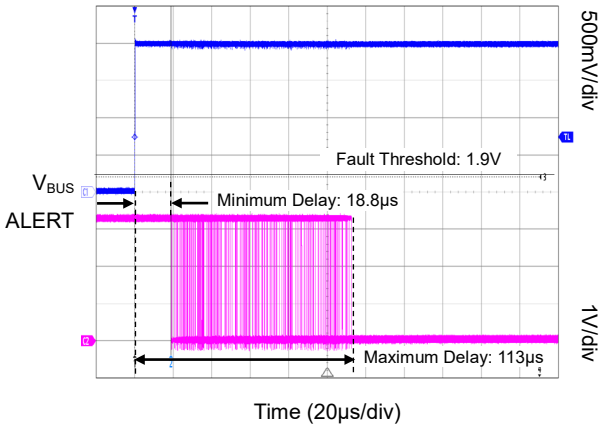


Figure 14. Alert Response Time (Sampled Values Significantly Above Threshold)

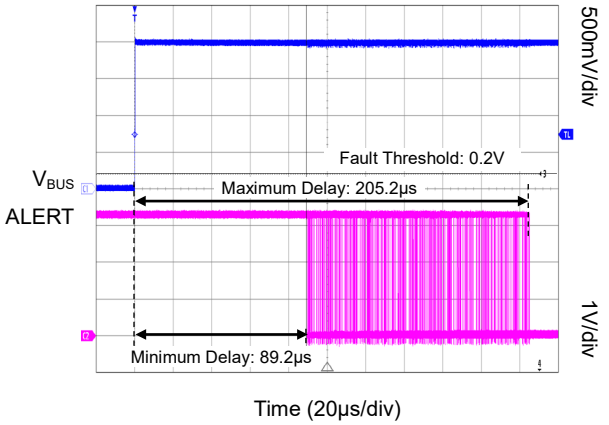


Figure 15. Alert Response Time (Sampled Values Slightly Above Threshold)

Power Supply Recommendations

The SGM839 input stage supports common-mode voltages higher than the device supply voltage, V_S. For example, the device can be powered from a 5V supply while monitoring a load supply with a common-mode voltage as high as 85V. The input terminals can also tolerate voltages over the full 0V to 85V range whether VS is applied or not. Do not disconnect the GND pin while the device is powered.

Place the power-supply bypass capacitor as close as possible to the VS and GND pins. A typical bypass capacitance is 0.1µF. For noisy or high-impedance supplies, evaluate whether additional decoupling capacitance is required to reduce power-supply noise.

Layout Guidelines

Use Kelvin, or 4-wire, connections between the IN+ and IN- pins and the current-sensing resistor. This connection method ensures that the voltage sensed between the input pins is developed only across the current-sensing resistor. Improper routing can introduce additional resistance into the sensed path. Because the current-sensing resistor typically has a very low resistance, even a small amount of additional impedance carrying the load current can introduce significant measurement error.

Place the power-supply bypass capacitor as close as possible to the VS and GND pins.

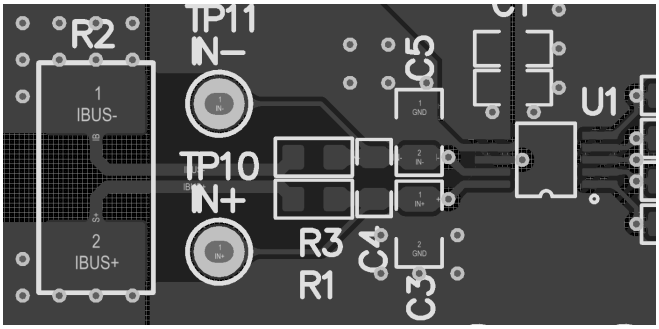


Figure 16. PCB Layout (Top View)

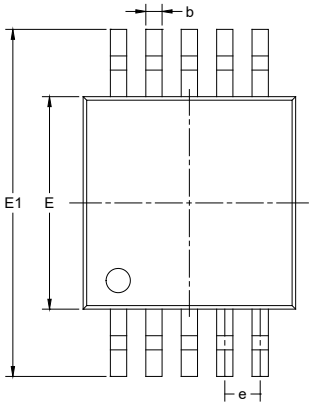
REVISION HISTORY

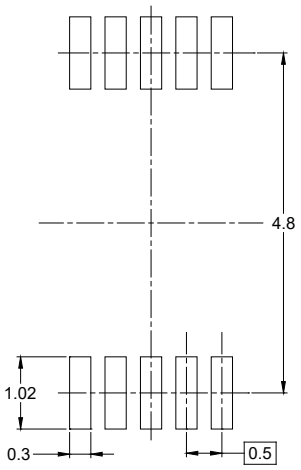
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original to REV.A (OCTOBER 2026)	Page
Changed from product preview to production data	All

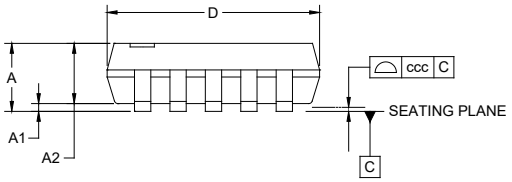
PACKAGE OUTLINE DIMENSIONS

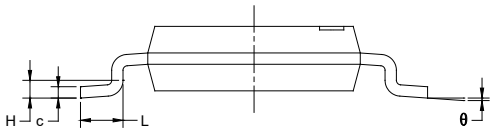
MSOP-10





RECOMMENDED LAND PATTERN (Unit: mm)



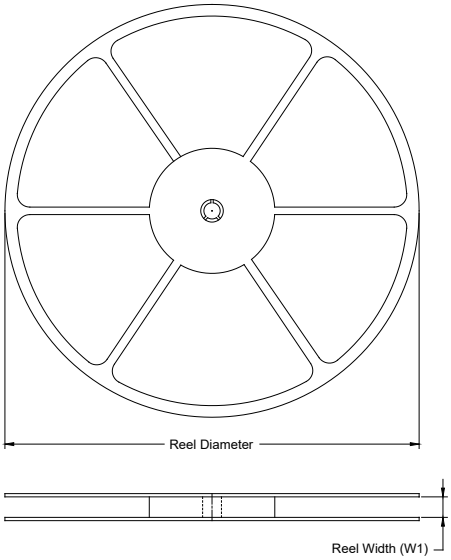


Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	-	-	1.100
A1	0.000	-	0.150
A2	0.750	-	0.950
b	0.170	-	0.330
c	0.080	-	0.230
D	2.900	-	3.100
E	2.900	-	3.100
E1	4.750	-	5.050
e	0.500 BSC		
H	0.250 TYP		
L	0.400	-	0.800
θ	0°	-	8°
ccc	0.100		

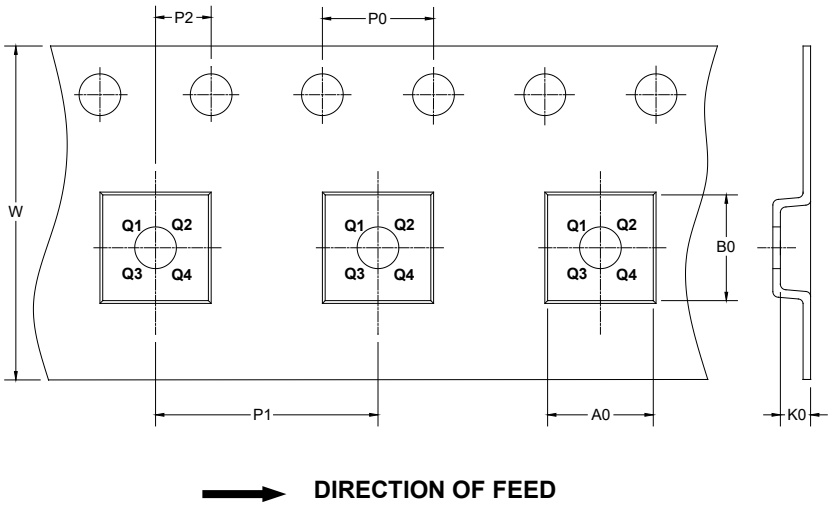
NOTES:
1. This drawing is subject to change without notice.
2. The dimensions do not include mold flashes, protrusions or gate burrs.
3. Reference JEDEC MO-187.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



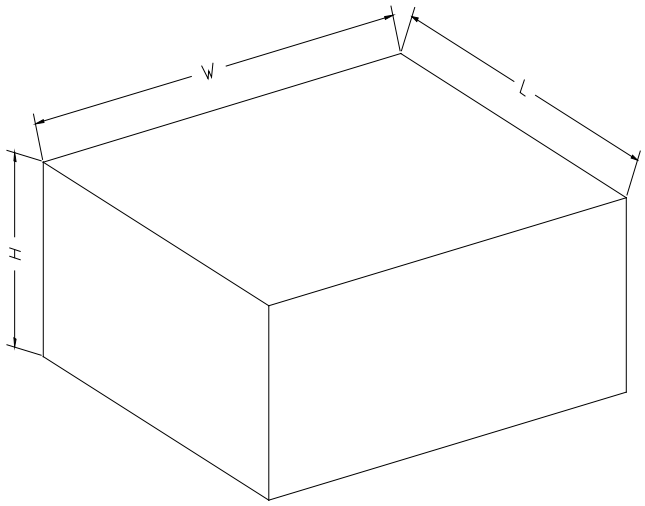
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
MSOP-10	13"	12.4	5.20	3.30	1.50	4.0	8.0	2.0	12.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002