SGM7220DRP
USB Type-C Configuration Channel Logic and Port Control

GENERAL DESCRIPTION

The SGM7220DRP is a configuration channel logic and port control device applied in USB Type-C interfaces. The single power supply range is from 2.7V to 5V. The SGM7220DRP is active low and enters low power mode when the $\overline{EN}$ pin is pulled to high.

The SGM7220DRP can be configured as a downstream facing port (DFP), an upstream facing port (UFP) or a dual role port (DRP) based on the Type-C specifications. Besides, it can support attachment detection, cable orientation detection, role detection, current mode detection and V_{BUS} voltage detection. The V_{BUS} detection is used to confirm whether the V_{BUS} voltage is normal when the SGM7220DRP is used as a UFP or DRP.

The SGM7220DRP contains a CC logic monitor block, which is used to monitor the voltage of CC1 and CC2. The SGM7220DRP advertises the Type-C current (default, medium or high) according to the CC logic monitor.

The SGM7220DRP is available in a Green UTQFN-1.6×1.6-12L package. It operates in industrial and commercial temperature range of -40℃ to +125℃.

FEATURES

- **Power Supply Range: 2.7V to 5V**
- **Supports USB Type-C Specification 1.0 and 1.1**
- **Supports Default, 1.5A and 3A Current Mode Detect and Control**
- **Role Configuration**
  - **DFP Mode: Source only**
  - **UFP Mode: Sink only**
  - **Support DRP with Try.SNK: Dual Role Port**
- **Supports Role and Cable Orientation Detection**
- **Attachment of USB Port Detection**
- **Supports I^2C or GPIO Control**
- **Supports up to 400kHz I^2C Clock Frequency**
- **Default UFP in Dead Battery**
- **V_{BUS} Voltage Detection**
- **Enable Pin Active Low**
- **Low Power Mode Control**
- **-40℃ to +125℃ Operating Temperature Range**
- **Available in a Green UTQFN-1.6×1.6-12L Package**

APPLICATIONS

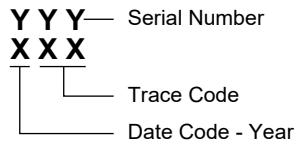
USB Type-C Interface Detection Applications
Consumer Electronics
Smart Phones
Laptops
USB Hubs

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM7220DRP	UTQFN-1.6×1.6-12L	-40℃ to +125℃	SGM7220DRPXUQT12G/TR	155 XXX	Tape and Reel, 3000

MARKING INFORMATION

NOTE: XXX = Date Code and Trace Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage Range, V_{DD} ..... -0.3V to 6V
Control Pins (CC1, CC2, ADDR, ID, $\overline{EN}$, INT_N/OUT3, NC)
..... -0.3V to (V_{DD} + 0.3V)
Control Pins (CC1, CC2, V_{DD} = 0V) ..... -0.3V to 6V
Control Pins (SDA/OUT1, SCL/OUT2) . -0.3V to (V_{DD} + 0.3V)
Control Pin (VBUS_DET)..... -0.3V to (V_{DD} + 0.3V)
Package Thermal Resistance
UTQFN-1.6×1.6-12L, θ_{JA} ..... 125.5℃/W
UTQFN-1.6×1.6-12L, θ_{JB} ..... 33.6℃/W
UTQFN-1.6×1.6-12L, θ_{JC} ..... 80.1℃/W
Junction Temperature.....+150℃
Storage Temperature Range .....-65℃ to +150℃
Lead Temperature (Soldering, 10s).....+260℃
ESD Susceptibility (1)(2)
HBM.....±4000V
CDM .....±1000V

NOTES:

1. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.

2. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

RECOMMENDED OPERATING CONDITIONS

Supply Voltage Range, V_{DD} .....2.7V to 5V
System V_{BUS} Voltage, V_{BUS} .....4.2V to 28V (5V TYP)
VBUS_DET Threshold Voltage on the Pin, V_{BUS_DET}
.....5V (MAX)
Operating Junction Temperature Range..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

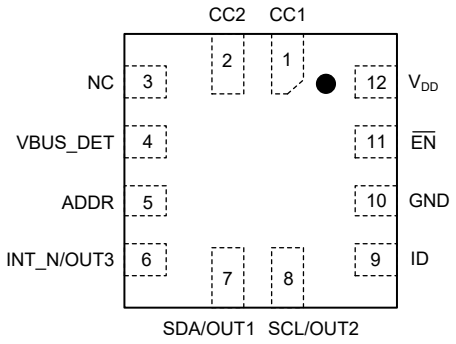
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

(TOP VIEW)



UTQFN-1.6×1.6-12L

PIN DESCRIPTION

PIN	NAME	TYPE	FUNCTION
1	CC1	I/O	Type-C CC logic signal Channel 1.
2	CC2	I/O	Type-C CC logic signal Channel 2.
3	NC	–	No Connection. Keep this pin floating if it is not used.
4	VBUS_DET	AI	The VBUS_DET pin is used to confirm whether the UFP is connected and it should be connected to system V_{BUS} through an external 866kΩ resistor. The V_{BUS} operating voltage range is from 4.2V to 28V.
5	ADDR	AI	I^2C Address and GPIO Mode Configuration Pin. H - I^2C 7-bit address is 0x67 in I^2C bus serial control mode. L - I^2C 7-bit address is 0x47 in I^2C bus serial control mode. Floating - GPIO mode.
6	INT_N/OUT3	DO	INT_N and OUT3 Dual-Function Pin. This pin only supports open-drain output. When used as INT_N, this pin can indicate the changes of I^2C register status in I^2C control mode and output low once the value of I^2C register changes. When used as OUT3 in GPIO mode, this pin can support audio accessory detection. H - No detection. L - The value of I^2C register changes or audio accessory connection detected.
7	SDA/OUT1	I/O	SDA and OUT1 Dual-Function Pin. This pin only supports open-drain output. When it is pulled to high or low, the SGM7220DRP is configured in I^2C mode and this pin is used as data signal in I^2C communication. When the ADDR pin is keep floating, the SGM7220DRP is configured in GPIO mode. This pin only supports Type-C current mode detection when the SGM7220DRP is in UFP mode as shown in Table 2.
8	SCL/OUT2	I/O	SCL and OUT2 Dual-Function Pin. This pin only supports open-drain output. When it is pulled to high or low, the SGM7220DRP is configured in I^2C mode and this pin is used as clock signal in I^2C communication. When the ADDR pin is keep floating, the SGM7220DRP is configured in GPIO mode. This pin only supports Type-C current mode detection when the SGM7220DRP is in UFP mode as shown in Table 2.
9	ID	DO	Open-Drain Output Pin. When the CC1 and CC2 pins detect device attachment, this pin is pulled to low when port is a source (DFP) or dual role (DRP) acting as source (DFP).
10	GND	G	Ground Pin. This pin must be connected to ground.
11	$\overline{EN}$	AI	Enable Input Pin. The SGM7220DRP is active Low ($\overline{EN}$ pin). Enable is pulled up to V_{DD} internally if no any external operations and the SGM7220DRP is disabled by default.
12	V_{DD}	P	Power Supply Pin.

NOTE: AI = analog input, AO = analog output, DO = digital output, I/O = input/output, P = power, G = ground.

ELECTRICAL CHARACTERISTICS

(V_{DD} = 2.7V to 5V, T_A = -40℃ to +125℃, typical values are at T_A = +25℃, unless otherwise noted.)

PARAMETER		SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Power Consumption							
Current Consumption	Unattached Mode	$I_{UNATTACHED\_UFP}$	V_{DD} = 4.5V, $\overline{EN}$ = L, ADDR = NC, configured as a UFP through I^2C interface, when port is unconnected and waiting for connection		70	85	μA
	Active Mode	I_{ACTIVE_UFP}	V_{DD} = 4.5V, $\overline{EN}$ = L, ADDR = NC, configured as a UFP through I^2C interface		70	90	
Leakage Current		$I_{SHUTDOWN}$	V_{DD} = 4.5V, $\overline{EN}$ = L, when V_{DD} is supplied but the SGM7220DRP is not enabled		0.04	0.5	μA
CC1 and CC2 Pins							
Pull-Down Resistor		R_{CC_DB}	In dead battery mode	4.80	5.1	5.60	kΩ
		R_{CC_D}	In UFP or DRP mode	4.85	5.1	5.45	
Voltage Threshold for Detecting a DFP Attachment		$V_{TH\_UFP\_CC\_USB}$	When configured as a UFP and DFP is advertising default current source capability	0.15		0.25	V
		$V_{TH\_UFP\_CC\_MED}$	When configured as a UFP and DFP is advertising medium (1.5A) current source capability	0.61		0.73	
		$V_{TH\_UFP\_CC\_HIGH}$	When configured as a UFP and DFP is advertising high (3A) current source capability	1.16		1.31	
Voltage Threshold for Detecting a UFP Attachment		$V_{TH\_DFP\_CC\_USB}$	When configured as a DFP and advertising default current source capability	1.49		1.67	V
		$V_{TH\_DFP\_CC\_MED}$	When configured as a DFP and advertising medium (1.5A) current source capability	1.49		1.67	
		$V_{TH\_DFP\_CC\_HIGH}$	When configured as a DFP and advertising high (3A) current source capability	2.45		2.74	
Pull-Up Current Source	Default Mode	$I_{CC\_DEFAULT\_P}$	When operating in DFP or DRP mode	64	80	96	μA
	Medium (1.5A) Mode	$I_{CC\_MED\_P}$		166	180	194	
	High (3A) Mode (1)	$I_{CC\_HIGH\_P}$		304	330	356	
Control Pins: ADDR, INT_N/OUT3, EN, ID							
Low-Level Control Signal Input Voltage (ADDR, $\overline{EN}$)		V_{IL}				0.4	V
Mid-Level Control Signal Input Voltage (ADDR)		V_{IM}		0.31 × V_{DD}		0.55 × V_{DD}	V
High-Level Control Signal Input Voltage (ADDR, $\overline{EN}$)		V_{IH}		V_{DD} - 0.3			V
High-Level Input Current		I_{IH}		-10		10	μA
Low-Level Input Current		I_{IL}		-10		10	μA
Internal Pull-Down Resistance for $\overline{EN}$		R_{EN_H}			0.66		MΩ
Internal Pull-Up Resistance (ADDR)		R_{PU}			1.4		MΩ
Internal Pull-Down Resistance (ADDR)		R_{PD}			1		MΩ
Low-Level Signal Output Voltage (Open-Drain) (INT_N/OUT3, ID)		V_{OL}	I_{OL} = 1.6mA			0.2	V
External Pull-Up Resistor on Open-Drain IOs (INT_N/OUT3, ID)		R_{P_ODEXT}			200		kΩ
Tri-Level Input External Pull-Up Resistor (ADDR)		R_{P_TLEXT}			4.7		kΩ

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 2.7V to 5V, T_A = -40℃ to +125℃, typical values are at T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
I^2C - SDA/OUT1, SCL/OUT2 can Operate from 1.8V to 3.3V (±10%) (2)						
Supply Range for I^2C (SDA/OUT1, SCL/OUT2)	V_{DD_I2C}		1.65	1.8	3.6	V
High-Level Signal Voltage	V_{IH}		1.05			V
Low-Level Signal Voltage	V_{IL}				0.4	V
Low-Level Signal Output Voltage (Open-Drain)	V_{OL}	I_{OL} = 1.6mA			0.25	V
VBUS_DET Pin (Connected to System V_{BUS} Signal)						
V_{BUS} Threshold Range	V_{BUS_THR}		2.1	3.1	4	V
External Resistor between V_{BUS} and VBUS_DET Pin	R_{VBUS}		857	866	875	kΩ
Internal Pull-Down Resistance for VBUS_DET	R_{VBUS_PD}			102		kΩ

NOTES:

1. V_{DD} must be 3.5V or greater to advertise 3A current.
2. When I^2C is pulled up to 3.3V with external resistor, the voltage of V_{DD} must be maintained above 3V.

TIMING REQUIREMENTS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
I^2C (SDA, SCL)					
Data Set-Up Time	$t_{SU:DAT}$	100			ns
Data Hold Time	$t_{HD:DAT}$	10			ns
Set-Up Time, SCL to Start Condition	$t_{SU:STA}$		600		ns
Hold Time, (Repeated) Start Condition to SCL	$t_{HD:STA}$		600		ns
Set-Up Time for Stop Condition	$t_{SU:STO}$		600		ns
Bus Free Time between a Stop and Start Condition	t_{BUF}		600		ns
SCL Clock Frequency; I^2C Mode for Local I^2C Control	f_{SCL}			400	kHz
Rise Time of both SDA and SCL Signals	t_R		100		ns
Fall Time of both SDA and SCL Signals	t_F		60		ns
Total Capacitive Load for Each Bus Line when Operating at ≤ 100kHz	C_{BUS_100kHz}			400	pF
Total Capacitive Load for Each Bus Line when Operating at ≤ 400kHz	C_{BUS_400kHz}			100	pF

SWITCHING CHARACTERISTICS

(T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Power-On Default of CC1 and CC2 Voltage Debounce Time	$t_{CCCB\_DEFAULT}$	DEBOUCE register = 2'b00		168		ms
Debounce of VBUS_DET Pin after Valid V_{BUS_THR}	t_{VBUS_DB}	See Figure 1		2		ms
Power-On Default of Percentage of Time DRP Advertises DFP during a t_{DRP}	$t_{DRP\_DUTY\_CYCLE}$	DRP_DUTY_CYCLE register = 2'b00		30		%
The Period During which SGM7220DRP in DFP Mode Completes a DFP to UFP and Back Advertisement	t_{DRP}		50	75	100	ms
Time from $\overline{EN}$ Low and V_{DD} Active to I^2C Access Available	t_{I2C_EN}				15	ms
Soft Reset Duration	t_{SOFT_RESET}		6	10	15	ms

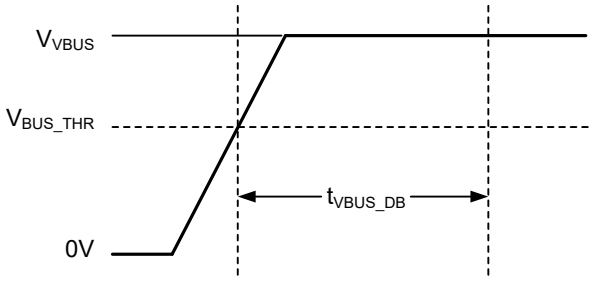


Figure 1. VBUS Detect and Debounce

FUNCTIONAL BLOCK DIAGRAM

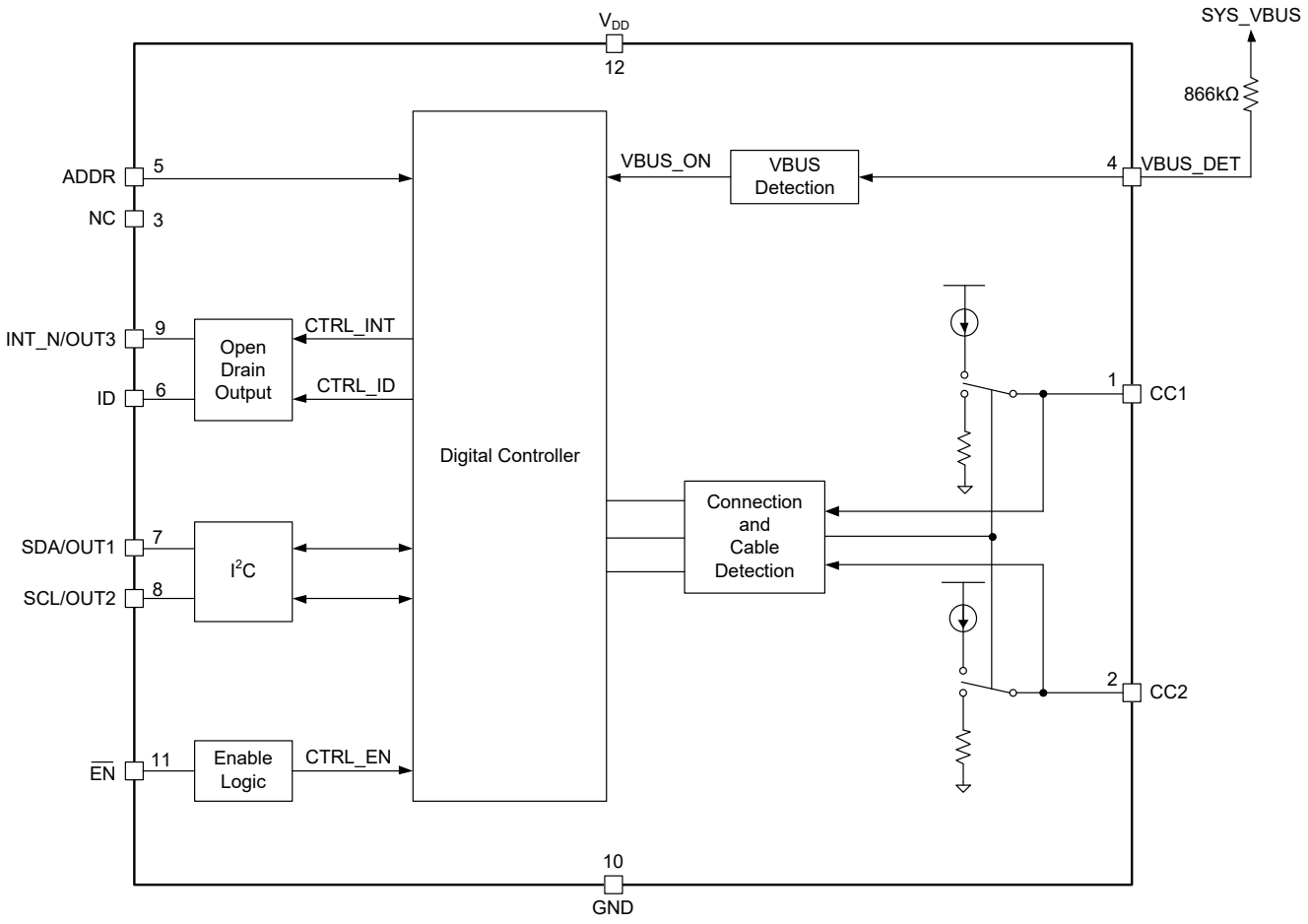


Figure 2. Block Diagram

DETAILED DESCRIPTION

Overview

The SGM7220DRP can be configured as a DFP, a UFP or a DRP based on the Type-C specifications. The SGM7220DRP can support attachment detection, cable orientation detection, role detection, current mode detection and V_{BUS} voltage detection. Additionally, the SGM7220DRP offers flexible operation modes, including mode configuration and low power consumption mode, making it an ideal choice for both sources and sinks in USB 2.0 applications.

USB Type-C Receptacles, Plugs, Cables and Adapters

The SGM7220DRP supports all USB Type-C receptacles, plugs, cables and adapters from the USB Type-C specification 1.1 defines. The SGM7220DRP does not support e-marking in UFP mode.

USB Type-C Receptacles and Plugs

The SGM7220DRP supports receptacles and plugs as follows:

- USB full-featured Type-C receptacle for USB 2.0, and full-featured platforms and devices
- USB full-featured Type-C plug
- USB2.0 Type-C plug

USB Type-C Cables

The SGM7220DRP supports Type-C cables as follows:

- USB full-featured Type-C cable
- USB2.0 Type-C cable with USB2.0 plug
- Captive cable with either a USB full-featured Type-C plug or USB 2.0 Type-C plug at one end

Legacy Cable Adapters

The SGM7220DRP can be applied to legacy cable adapters follow the Type-C specification. As shown in Figure 3, the cable adapter must match with the mode configuration of the SGM7220DRP.

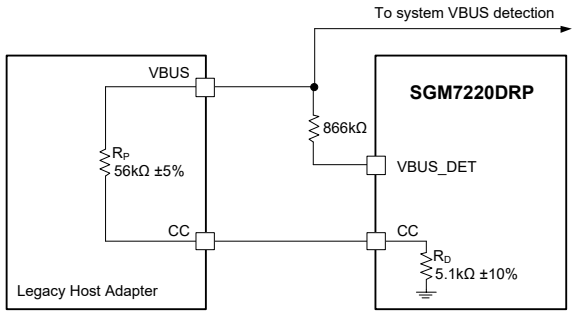


Figure 3. Legacy Adapter Implementation Circuit

Audio Adapters

The SGM7220DRP can be applied to audio adapters for audio accessory mode, include passive audio adapter and charge through audio adapter.

Direct Connect Devices

The SGM7220DRP supports the attaching and detaching of a direct-connect device.

Role Configuration

The SGM7220DRP can be set as an upstream facing port (UFP), a downstream facing port (DFP) or a dual-role port (DRP) by configuring the MODE_SELECT registers. After the SGM7220DRP is powered on, the default role is set to DRP.

Dual Role Port (DRP)

The DRP mode of SGM7220DRP can also be configured by operating the MODE_SELECT register. In this mode, the SGM7220DRP alternates between a DFP and a UFP and CC1 and CC2 pins are switches between the pull-up resistors (R_P) and the pull-down resistors (R_D). Based on the Type-C specification, when the SGM7220DRP presents as a DFP in DRP mode, it performs all operations as defined in the Type-C specification about DFP. When the SGM7220DRP presents as a UFP in DRP mode, it performs all operations as defined from the Type-C specification about UFP.

Downstream Facing Port (DFP) - Source

The DFP mode of SGM7220DRP can be configured by operating the MODE_SELECT register. In this mode, the CC1 and CC2 pins connect to two pull-up resistors (R_P) and the SGM7220DRP releases a default USB Type-C current after initial power on. The Type-C current advertisement can also be configured to high or medium when the SGM7220DRP is set to a DFP. The SGM7220DRP can adjust the pull-up resistors (R_P) to match the expected Type-C current advertisement according to the system requirements. If the SGM7220DRP is working in GPIO mode, it only advertises default Type-C current.

The SGM7220DRP can work with older USB Type-C 1.0 devices when applied as a DFP. But in this mode, it cannot work with a USB Type-C 1.0 DRP device because of backwards compatibility problem between a USB Type-C 1.1 DFP and a USB Type-C 1.0 DRP.

DETAILED DESCRIPTION (continued)

Upstream Facing Port (UFP) - Sink

The UFP mode of SGM7220DRP can be configured by operating the MODE_SELECT register. In this mode, the CC1 and CC2 pins connect to two pull-down resistors (R_D). The SGM7220DRP can advertise the Type-C mode current of DFP device according to the detected voltage on CC1 and CC2 pins when a DFP device is connected to it. The CC1 and CC2 pins keep toggling and the SGM7220DRP waits for VBUS detection before successfully attaching. As a UFP, the SGM7220DRP transmits the advertised current of the DFP to the system through the OUT1 and OUT2 pins in GPIO mode, or alternatively, through the I^2C CURRENT_MODE_DETECT register only once during the Attached.SNK state.

After initial connection, the advertised current by the connected DFP could change due to changes in its system power resource. For instance, a DFP advertises high current at the beginning of connection but then changes pull-up resistors (R_P) to reduce to default current due to user removing external power adapter from their notebook. Because the SGM7220DRP will only advertise on OUT1 and OUT2 the initial advertised current, it is recommended monitoring the advertised current through the I^2C interface from the CURRENT_MODE_DETECT register. System software must periodically perform an I^2C_SOFT_RESET register in order to update the CURRENT_MODE_ DETECT register based on the state of the CC1 and CC2 pins.

The SGM7220DRP's supported features in each mode are shown in Table 1.

Table 1. Supported Features for the SGM7220DRP

Supported Features	DFP Only	UFP Only	DRP
Port Attach and Detach	Yes	Yes	Yes
Cable Orientation (through I^2C)	Yes	Yes	Yes
Current Advertisement	Yes	-	Yes (DFP)
Current Detection	-	Yes	Yes (UFP)
Accessory Modes (Audio and Debug)	Yes	Yes	Yes
Try.SNK	-	-	Yes
Active Cable Detection	Yes	-	Yes (DFP)
I^2C/GPIO	Yes	Yes	Yes
Legacy Cables	Yes	Yes	Yes
V_{BUS} Detection	-	Yes	Yes (UFP)

Type-C Current Mode

When the USB Type-C port is connected to a valid cable and enters attached mode, the DFP needs to advertise the current capability of UFP can be sunk by Type-C port. The current advertisement default value is defined by the USB specification (500mA for USB 2.0 ports, 900mA for USB 3.1 ports). If a higher level of current is required, the 1.5A medium current and the 3A high current can be set through written appropriate value to CURRENT_MODE_ADVERTISE register. When the CURRENT_MODE_ ADVERTISE register has been operated to advertise higher default current, the DFP will adjust the pull-up resistors (R_P) to match the desired Type-C current advertisement. If the DFP advertises 3A, the V_{DD} supply is required at least 3.5V. The Type-C current advertisements in I^2C and GPIO mode are shown in Table 2.

Table 2. Type-C Current Advertisement for I^2C and GPIO Mode

<table>
<tr><th colspan="2">I^2C Mode (ADDR = H or L)</th><th colspan="2">GPIO Mode (ADDR = NC)</th></tr>
<tr><th>UFP</th><th>DFP</th><th>UFP</th><th>DFP</th></tr>
<tr><td rowspan="2">Current Mode Detected and Read through I^2C Register</td><td>I^2C Register Default is 500mA or 900mA (MAX)</td><td rowspan="2">Current Mode Detected and Output through OUT1/OUT2</td><td>Only Advertisement</td></tr>
<tr><td>Advertisement Selected through Writing I^2C Register</td><td>N/A</td></tr>
<tr><th colspan="4">Type-C Current Grade</th></tr>
<tr><td>Default</td><td colspan="3">500mA (MAX) for USB2.0
900mA (MAX) for USB3.1</td></tr>
<tr><td>Medium</td><td colspan="3">1.5A (MAX)</td></tr>
<tr><td>High</td><td colspan="3">3A (MAX)</td></tr>
</table>

DETAILED DESCRIPTION (continued)

I²C and GPIO Control

The SGM7220DRP can be set to I²C mode or GPIO mode by the ADDR pin. If the ADDR pin is left floating, The SGM7220DRP is configured in GPIO output mode. If the ADDR pin is connected to high or low, the SGM7220DRP is configured in I²C mode.

When the SGM7220DRP is configured in GPIO mode, the OUT1 and OUT2 pins are used to indicate the different current advertisement. The OUT1 and OUT2 configuration is shown in Table 3. The OUT3 pin is used to indicate changes in the connection status of audio accessory in GPIO mode. In addition, all outputs for the SGM7220DRP are designed as open-drain output.

Table 3. Simplified Operation for OUT1 and OUT2

OUT1	OUT2	State	Advertisement
H	H	Unattached State	Default Current
H	L	Attached State	Default Current
L	H	Attached State	Medium Current (1.5A)
L	L	Attached State	High Current (3A)

When the SGM7220DRP is configured in I²C mode, the SCL and SDA lines are used for serial clock and serial data communication. The INT_N pin is used to indicate the changes of I²C registers and this pin is output low once interruption occurs. The INT_N pin only supports open-drain output and changes from high to low when the SGM7220DRP registers are updated. If this pin output low, it means the INTERRUPT_STATUS register should be set. The end user can write one to reset the INTERRUPT_STATUS register by I²C communication.

In GPIO mode, the OUT3 pin is used to indicate the connection status of the audio accessory. Once an audio accessory is connected and detected, the OUT3 pin is output low.

NOTE: When SDA and SCL are pulled up to 3.3V with an external resistor, the V_{DD} will not be less than 3V to prevent the I²C from powering the device back.

Accessory Support

The SGM7220DRP supports audio and debug accessories detection in UFP, DFP and DRP mode. The type of accessory is determined through reading the ACCESSORY_CONNECTED register. Audio accessory can be detected when the SGM7220DRP is configured in GPIO output mode by setting IN_T/OUT3 pin.

Audio Accessory

Audio accessory contains the charge through accessory and the passive audio accessory.

The charge through accessory consists of a receptacle and a plug. The plug can supply the current of 500mA through V_{BUS} when the plug detects a connection as a DFP.

The passive audio accessory can be used to convert audio signal between Type-C port and audio port. The passive audio adapter can be detected effectively if the CC1 and CC2 pins detect a resistance < R_A respectively.

When the SGM7220DRP is configured in GPIO mode, the OUT3 pin is used to indicate the audio accessory is detected or attached. Once an audio accessory is detected, the OUT3 is output low.

Debug Accessory

The debug accessory detection is usually applied by users in test mode to match the software debug requirements. The SGM7220DRP supports the debug accessory detection only in DFP mode. When the SGM7220DRP is configured in DFP mode, CC1 and CC2 pins of the SGM7220DRP connect two pull-up resistors (R_P), CC1 and CC2 pins of debug accessories connect two pull-down resistors (R_D).

V_{BUS} Detection

The SGM7220DRP is designed with V_{BUS} detection function to match the Type-C specifications. V_{BUS} detection is used to confirm whether the UFP is connected and the entering or exiting of accessory modes. V_{BUS} detection is applied to identify the role in DRP mode as well.

The VBUS_DET pin must be connected to system V_{BUS} through an 866kΩ resistor if the SGM7220DRP is configured as a DRP or a UFP. When the SGM7220DRP is only used in DFP mode, the VBUS_DET pin cannot be connected.

DETAILED DESCRIPTION (continued)

The SGM7220DRP has 4 functional modes as shown in Table 4.

Table 4. USB Type-C States According to SGM7220DRP Functional Modes

Modes	General Behavior	Mode	States (1)
Unattached	USB port unattached. ID is operational. I^2C on. CC1 and CC2 pins configure according to MODE_SELECT registers.	UFP	Unattached.SNK
			AttachWait.SNK
		DRP	Toggle Unattached.SNK → Unattached.SRC
			AttachedWait.SRC or AttachedWait.SNK
		DFP	Unattached.SRC
			AttachWait.SRC
Active	USB port attached. All GPIOs are operational. I^2C on.	UFP	Attached.SNK
		DRP	Attached.SNK
			Attached.SRC
			Audio accessory
			Debug accessory
		DFP	Attached.SRC
			Audio accessory
			Debug accessory
Dead Battery	No operation. V_{DD} not available.	UFP/DRP/DFP	Default device state to UFP/SNK with R_D.
Shutdown	V_{DD} available. SGM7220DRP $\overline{EN}$ pin high.	UFP/DRP/DFP	Default device state to UFP/SNK with R_D.

NOTE: 1. Required; not in sequential order.

Unattached Mode

Unattached mode is defined as USB Type-C ports with no connections. In unattached mode, the V_{DD} supply is provided and all IOs and I^2C are configurable. At the beginning of power-on, the SGM7220DRP enters in the Unattached.SNK state and configures the port role as DRP. The SGM7220DRP toggles between the UFP and the DFP if it is configured as a DRP. In unattached mode, if the mode configuration or port role is undesired at the beginning of power-on, the user can change the mode configuration or port role through I^2C configuration. It should be noted that writing to the I^2C MODE_SELECT register is valid only in unattached mode. If the SGM7220DRP is in attached mode, I^2C operation is invalid.

Active Mode

Active mode indicates that the attachment is connected to the port. In this mode, all GPIOs are operational and I^2C is read/write (R/W). If the SGM7220DRP is used as a DFP or as a DFP in DRP mode, the SGM7220DRP delivers information to the processor about whether the USB port is attached by the ID pin. If the SGM7220DRP is used as a UFP or as sink in DRP mode, the OUT1/OUT2 and INT_N/OUT3 pins are operating. The SGM7220DRP exits active mode under the condition of as follows:

- Cable plugs removal.
- V_{BUS} removal if attached as a UFP.
- No power supply.
- $\overline{EN}$ pin has no any connection or it is pulled to high.

When the SGM7220DRP is operating in active mode, the Type-C port mode is not changed by I^2C configuration. The software implementation can only operate in the unattached state of the SGM7220DRP.

Shutdown Mode

Shutdown mode indicates that the SGM7220DRP is disabled and this mode has the following characteristics:

- The V_{DD} is provided and $\overline{EN}$ pin is pulled to high.
- The SGM7220DRP is disabled and CC1 and CC2 pins are connected to pull-down resistors (R_D) by default.
- $\overline{EN}$ pin has an internal pull-up resistor.

DETAILED DESCRIPTION (continued)

Dead Battery Mode

Dead battery mode is defined as V_{DD} no power supply. In this mode, CC1 and CC2 pins are connected to pull-down resistors (R_D) by default. Dead battery mode descriptions:

The CC1 and CC2 pins of the SGM7220DRP present 5.1kΩ ± 20% R_D. It is used as a UFP in dead battery mode and supports being charged from a source device. In this mode, if the SGM7220DRP is connected to a source device, the system will receive the default VBUS.

In this mode, the SGM7220DRP is used as UFP and CC1 and CC2 pins present 5.1kΩ ± 20% R_D. The V_{DD} may be connected to a discharged battery or power off.

NOTE: In application, the voltage of ADDR, INT_N/OUT3 and ID should not exceed the V_{DD}. If these pins need pulled up in practical application, they are required to pull up to the V_{DD} pin.

The SGM7220DRP is designed as I^2C interface for convenient communication between different devices. The I^2C interface of SGM7220DRP can be read or written after t_{I2C_EN} when the SGM7220DRP is powered on. The SCL and SDA terminals are used for serial clock bus and serial data bus respectively. If I^2C control mode is selected, the ADDR pin must be pulled up or pulled down and cannot be left floating. The SGM7220DRP I^2C addresses configuration is show in Table 5.

Table 5. SGM7220DRP I^2C Addresses

SGM7220DRP I^2C Target Address								
ADDR Pin	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (W/R)
H (0x67)	1	1	0	0	1	1	1	0/1
L (0x47)	1	0	0	0	1	1	1	0/1

Write Operation

The I^2C registers write operation steps are as follows:

1. Firstly, the controller sends a start condition (S) to the SGM7220DRP, and then the controller sends the 7-bit target address and a zero-value R/W bit to the SGM7220DRP.
2. The SGM7220DRP replies with an acknowledge (ACK) to the controller after receiving the target address.
3. The controller sends the register address of the register to which it wishes to write, the register address consists of one byte of data and an MSB-first.
4. The SGM7220DRP replies with an acknowledge (ACK) to the controller again after it received the register address.
5. Next, the controller will send the first byte of data to the SGM7220DRP.
6. The SGM7220DRP replies with an acknowledge (ACK) to the master once again.
7. The controller may continue presenting additional bytes of data to be written. The SGM7220DRP replies with an acknowledge (ACK) to the controller after each byte transfer is completed.
8. The controller sends a stop condition (P) to the SGM7220DRP in order to end the write operation.

Read Operation

The I^2C registers read operation steps are as follows:

1. Firstly, the controller sends a start condition (S) to the SGM7220DRP, and then the controller sends the 7-bit target address and a zero-value R/W bit to the SGM7220DRP.
2. The SGM7220DRP replies with an acknowledge (ACK) to the controller after receiving the target address.
3. The controller sends the register address of the register to which it wishes to read. The register address consists of one byte of data and an MSB-first.
4. The SGM7220DRP replies with an acknowledge (ACK) to the controller again after receiving the register address.
5. Next, the controller sends a start condition (S) to the SGM7220DRP again, and then the controller sends the 7-bit target address and a read-value R/W bit to indicate a read operation. After this, the SGM7220DRP will send an acknowledge (ACK) to the controller again.
6. The SGM7220DRP will transfer the first byte of data to the controller. At the end of every byte of data, the controller replies with an acknowledge (ACK) to the SGM7220DRP, letting the SGM7220DRP know that it is ready for more data.
7. The controller sends a not-acknowledge (NACK) to the SGM7220DRP after the data transfer is completed and sends a stop condition (P) to the SGM7220DRP in order to end the read operation.

REGISTER MAPS

All registers are 8-bit and individual bits are named from D[0] (LSB) to D[7] (MSB).

Bit Types:

R/W: Read/Write bit(s)

R: Read only bit(s)

W: Write only bit(s)

S: Set bits. Write 1 to clear. Writing zeros to a field is invalid.

C: Clear bits. Write 1 to clear. Writing zeros to a field is invalid.

U: Update. This field can be updated autonomously by hardware.

Table 6. CSR Registers Bit Address and Function Description

ADDRESS	BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
0x00 ~ 0x07	D[7:0]	DEVICE_ID	/	R	These bits return a string of ASCII characters returning the SGM7220DRP. Addresses 0x07 ~ 0x00 = {0x00, 0x54, 0x55, 0x53, 0x42, 0x33, 0x32 and 0x30}
0x08	D[7:6]	CURRENT_MODE_ ADVERTISE	00	R/W	These bits are configured according the application to raise the current advertisement from default. 00 = Default Current (500mA/900mA) value of initial power-on 01 = Medium Current (1.5A) 10 = High Current (3A) 11 = Reserved
	D[5:4]	CURRENT_MODE_ DETECT	00	RU	These bits will be set if an UFP determines the Type-C current mode. 00 = Default Current (default value of initial power-on) 01 = Medium Current 10 = Charge through accessory - 500mA 11 = High Current
	D[3:1]	ACCESSORY_ CONNECTED	000	RU	These bits are read by the application to confirm the type of attachment. 000 = No accessory attached (default) 001 = Do not use 010 = Do not use 011 = Do not use 100 = Audio accessory detected 101 = Audio charged thru accessory detected 110 = Debug accessory.SRC 111 = Debug accessory.SNK
	D[0]	ACTIVE_CABLE_ DETECTION	0	RU	This bit is used to indicate whether an active cable has been plugged into the Type-C connector. This bit will be set to 1 once an active cable is detected. 0 = Active cable is not attached (default) 1 = Active cable is attached
0x09	D[7:6]	ATTACHED_STATE	00	RU	This is an additional method to communicate attachment other than the ID pin. These bits can be read by the application to determine what was attached. 00 = Not attached (default) 01 = Attached.SRC (DFP) 10 = Attached.SNK (UFP) 11 = Attached to an accessory
	D[5]	CABLE_DIR	1	RU	This bit is used to indicate the orientation information of cable and supports read only. 0 = CC1 1 = CC2 (default)
	D[4]	INTERRUPT_ STATUS	0	RCU	This bit is used to indicate the changes of CSR registers. Whenever a CSR register changes, the INT pin will output low and the INTERRUPT_STATUS should be held at 1 until it is cleared by the system. 0 = Clear (This bit may be cleared by a write of one) 1 = Interrupt (When INT_N is output low, this bit will be set to 1)
	D[3]		0	R	Do not use.
	D[2:1]	DRP_DUTY_ CYCLE	00	R/W	Proportion of time that DFP is presented in the period of DRP (t_{DRP}). 00 = 30% (default) 01 = 40% 10 = 50% 11 = 60%

REGISTER MAPS (continued)

Table 6. CSR Registers Bit Address and Description (continued)

ADDRESS	BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
0x09	D[0]	DISABLE_UFP_ACCESSORY	0	R/W	Settings this bit will disable UFP accessory support. 0 = UFP accessory support enabled (default) 1 = UFP accessory support disabled
0x0A	D[7:6]	DEBOUNCE	00	R/W	The nominal amount of time the SGM7220DRP denounced the voltages on the CC1 and CC2 pins. 00 = 168ms (default) 01 = 118ms 10 = 134ms 11 = 152ms
	D[5:4]	MODE_SELECT	00	R/W	These bits are used to configure the role of the SGM7220DRP and the prerequisite for normal operation of these bits is that the ADDR pin is configured in I^2C mode. The SGM7220DRP is configured as DRP mode and these bits maintain the default value at the beginning of power on. In addition, the MODE_SELECT can only be effectively operated in the unattached state. These bits operation are invalid if the SGM7220DRP has been attached. 00 = DRP mode (start from unattached.SNK) (default) 01 = UFP mode (unattached.SNK) 10 = DFP mode (unattached.SRC) 11 = DRP mode (start from unattached.SNK)
	D[3]	I^2C_SOFT_RESET	0	RSU	This bit controls the function of I^2C registers reset and its initial value of power-on is 0. The following registers restore default value once this bit is set to 1: CURRENT_MODE_DETECT ACTIVE_CABLE_DETECTION ACCESSORY_CONNECTED ATTACHED_STATE CABLE_DIR INTERRUPT_STATUS
	D[2:1]	SOURCE_PREF	00	R/W	When the SGM7220DRP is configured as a DRP, these bits can be used to control its behaviors. 00 = Standard DRP (default) 01 = Try.SNK DRP. 10 = Do not use. 11 = Do not use.
	D[0]	DISABLE_TERM	0	R/W	When this bit is written to 1, both CC1 and CC2 pin are disabled. 0 = Both CC1 and CC2 pin are enabled (default). 1 = Both CC1 and CC2 pin are disabled and disconnect with R_P and R_D.
0x45	D[7:3]		0	R	Do not use.
	D[2]	DISABLE_RD_RP	0	R/W	When this bit is written to 1, R_D and R_P will stop toggle. 0 = Default value of initial power-on. (default) 1 = Disable R_D and R_P, R_D and R_P stop toggle.
	D[1:0]		0	R/W	Do not use.

APPLICATION INFORMATION

The SGM7220DRP is a Type-C connection detects and port configure controller. The SGM7220DRP can detect the connectivity of Type-C device, the type of attached device, the direction of the cable and power delivery capabilities (both detection and broadcast). The SGM7220DRP can be widely applied in a variety of applications, including source application (DFP), sink application (UFP) and combination source/sink application (DRP).

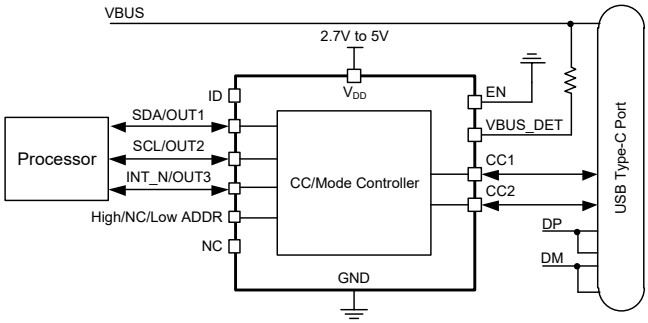


Figure 4. SGM7220DRP in UFP Mode Supporting Default Implementation

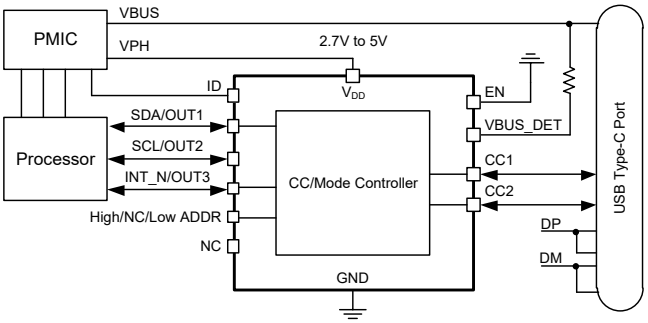


Figure 5. SGM7220DRP in UFP Mode Supporting Advanced Power Delivery

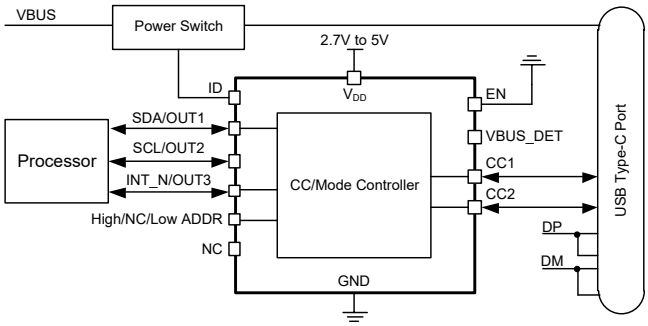


Figure 6. SGM7220DRP in DFP Mode Supporting Default Implementation

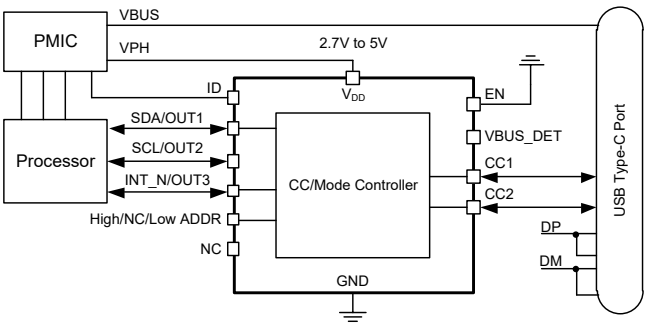


Figure 7. SGM7220DRP in DFP Mode Supporting Advanced Power Delivery

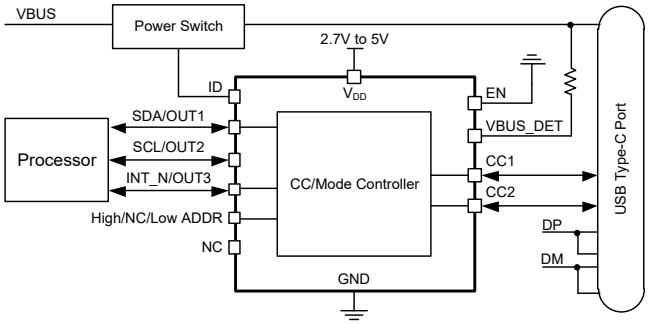


Figure 8. SGM7220DRP in DRP Mode Supporting Default Implementation

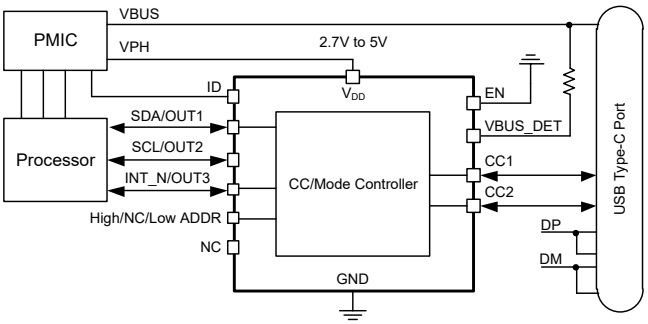


Figure 9. SGM7220DRP in DRP Mode Supporting Advanced Power Delivery

APPLICATION INFORMATION (continued)

DRP in I²C Mode

The SGM7220DRP is configured as a DRP in I²C mode as shown in Figure 10.

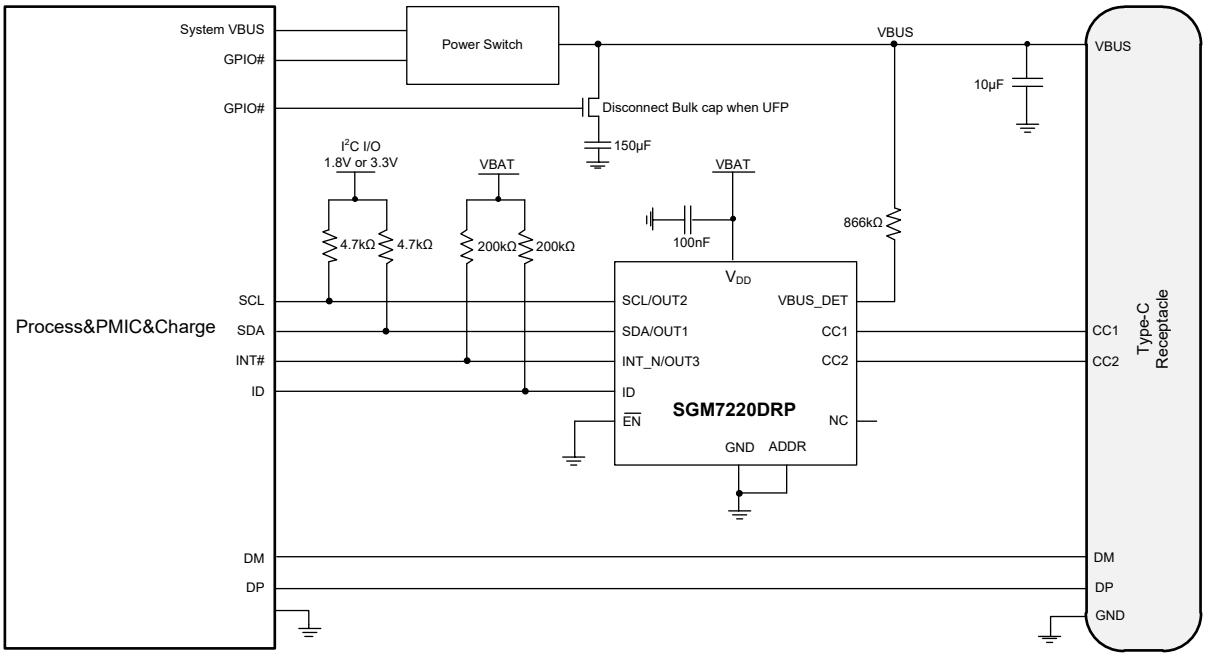


Figure 10. DRP in I²C Mode Reference Design

Design Descriptions

For this reference design, the parameters configuration is shown in Table 7.

Table 7. Design Description for DRP in I²C Mode

Design Parameter	Option	Circuit Design
V_{DD} Supply	2.75V to 5V	V_{DD} is tied to VBAT
Mode Select	I²C or GPIO	I²C: ADDR pin must be pulled down or pulled up.
I²C Address Select	0x47 or 0x67	0x47: ADDR is tied to GND.
Type-C Port Type	UFP, DFP or DRP	DRP: Configured through I²C interface.
$\overline{EN}$ Configuration	Active or shutdown	Active: $\overline{EN}$ pin is tied to GND

Detailed Descriptions of Reference Design

The SGM7220DRP V_{DD} range is required to between 2.75V and 5V. In this application, V_{BAT} is connected to the V_{DD} pin and its voltage range must be consistent with V_{DD} requirements. A 100nF decoupling capacitor is placed near the V_{DD} pin.

The SGM7220DRP is configured in I²C mode by pulling the ADDR pin high or low. In this application, the ADDR pin is connected to GND and the SGM7220DRP I²C address is set to 0x47. The SDA and SCL should be pulled up to 1.8V or 3.3V by a resistor. If the SDA and SCL are pulled up to 3.3V, the voltage of V_{DD} must be maintained above 3V to prevent the diode leakage between I²C port and V_{DD} pin.

The SGM7220DRP can be configured in shutdown mode by setting the $\overline{EN}$ pin to high and keep low power consumption in this mode. In this application, the $\overline{EN}$ pin is connected to V_{DD} pin and it can also be controlled externally if necessary for practical application.

The INT_N/OUT3 pin is an open-drain output and it used to indicate the change of the SGM7220DRP I²C registers. The INT_N/OUT3 pin needs an external 200kΩ pull-up resistor to ensure operating normally.

APPLICATION INFORMATION (continued)

The ID pin is an open-drain output and only works in DFP mode or presents as a DFP in DRP mode. This pin should be pulled to high by a resistor if the SGM7220DRP has no any connection. It will output low once a connection has occurred when the SGM7220DRP presents as a DFP in DRP mode. An OTG USB controller can distinguish itself operated as a USB host or USB device by the ID pin. The ID pin always keeps high if the SGM7220DRP is enabled and no connection occurs, this pin is output low if a device such as UFP is connected. When this pin is output low, the OTG USB controller functions as a host and then enables V_{BUS}. The Type-C specification requires that a DFP does not enable V_{BUS} until it is in the Attached.SRC state. When ID pin keeps high and VBUS is detected normally, then OTG USB controller functions as a device. This pin needs an external 200kΩ pull-up resistor to ensure it operates normally.

The Type-C port mode is controlled by software configuration. The software implementation operates the MODE_SELECT register through the I^2C interface. It is important that the SGM7220DRP must keep in unattached state if configured by software.

The VBUS_DET pin is used to detect V_{BUS} on the Type-C port and it has an internal pull-down resistor. An 866kΩ external resistor should be connected between VBUS_DET pin and VBUS pin. This large resistor plays an important role in protecting the SGM7220DRP from large V_{BUS} voltage that is possible in present systems. The external resistor along with internal pull-down resistor forms a voltage dividing network and it can ensure the V_{BUS_DET} voltage within the SGM7220DRP specification.

The USB2.0 specification requires that multiple decoupling capacitors should be connected to the VBUS pin. When the SGM7220DRP is used as a DRP, it will toggle between DFP and UFP. When the SGM7220DRP is configured as a UFP, the large bulk capacitance must be disconnected.

Table 8. USB2 Bulk Capacitance Requirements

Port Configuration	Min	Max	Units
Downstream Facing Port (DFP)	120		μF
Upstream Facing Port (UFP)	1	10	μF

Application Curve

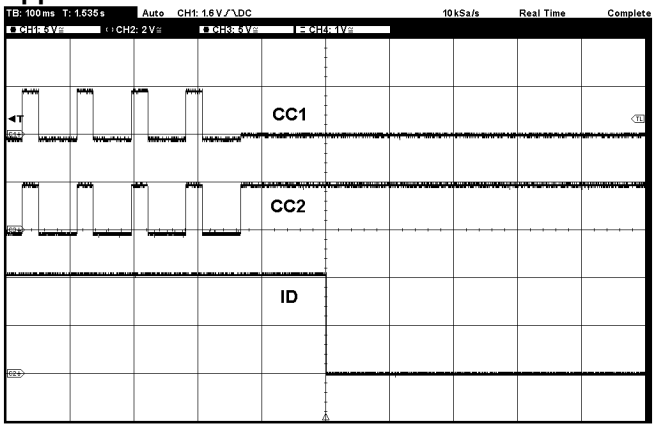


Figure 11. Application Curve for DRP in I^2C Mode

APPLICATION INFORMATION (continued)

DFP in I²C Mode

The SGM7220DRP is configured as a DFP in I²C mode as shown in Figure 12.

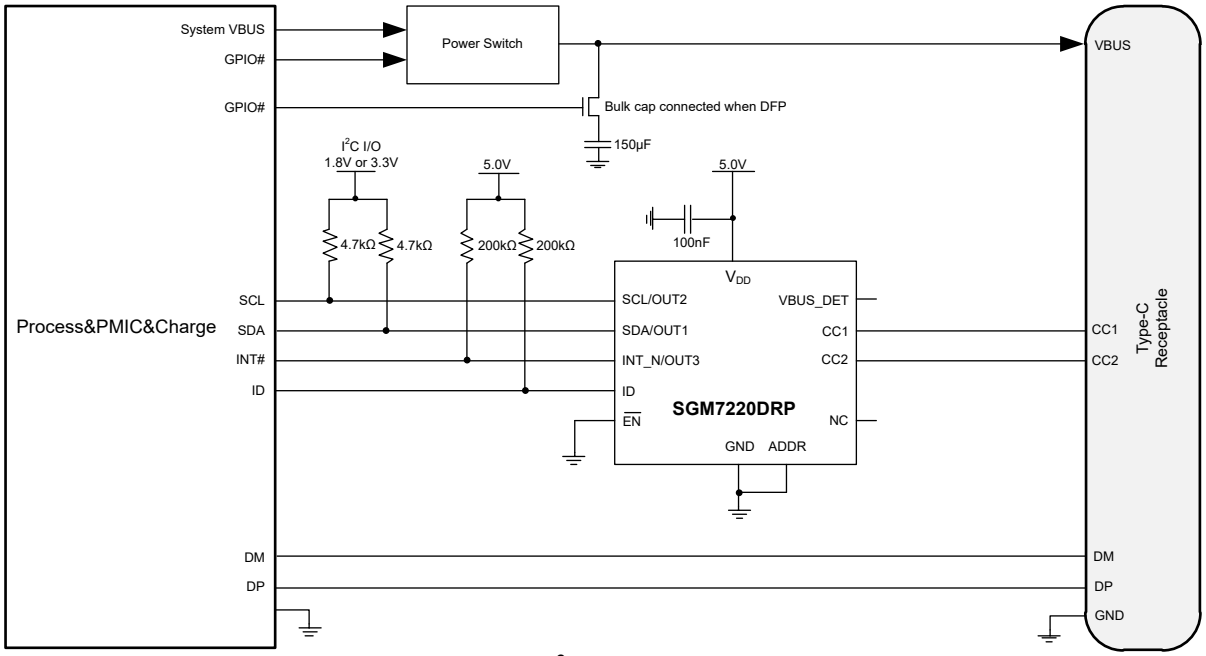


Figure 12. DFP in I²C Mode Reference Design

Design Descriptions

For this reference design, the parameters configuration is shown in Table 9.

Table 9. Design Description for DFP in I²C Mode

Design Parameter	Option	Circuit Design
V_{DD} Supply	2.75V to 5V	V_{DD} is tied to 5V
Mode Select	I²C or GPIO	I²C: ADDR pin must be pulled down or pulled up.
I²C Address Select	0x47 or 0x67	0x47: ADDR is tied to GND.
Type-C Port Type	UFP, DFP or DRP	DFP: Configured through I²C interface.
$\overline{EN}$ Configuration	Active or shutdown	Active: $\overline{EN}$ pin is tied to GND

Detailed Descriptions of Reference Design

The SGM7220DRP V_{DD} range is required to between 2.75V and 5V. In this application, V_{DD} is set to 5V. A 100nF decoupling capacitor is placed near the V_{DD} pin.

The SGM7220DRP is configured in I²C mode by pulling the ADDR pin high or low. In this application, the ADDR pin is connected to GND and the SGM7220DRP I²C address is set to 0x47. The SDA and SCL should be tied to 1.8V or 3.3V by a resistor.

The SGM7220DRP can be configured in shutdown mode by setting the $\overline{EN}$ pin low and the SGM7220DRP keeps low power consumption in this mode. In this application, the $\overline{EN}$ pin is connected to V_{DD} pin and it can also be controlled externally if it is necessary for practical application.

The INT_N/OUT3 pin is an open-drain output and it used to indicate the change of the SGM7220DRP I²C registers. The INT_N/OUT3 pin needs an external 200kΩ pull-up resistor to ensure operating normally.

The Type-C port mode is controlled by software configuration. The software implementation is operating the MODE_SELECT register through the I²C interface. It is important that the SGM7220DRP must keep in unattached state if configured by software.

APPLICATION INFORMATION (continued)

The VBUS_DET pin is used to detect V_{BUS} on the Type-C port and it has an internal pull-down resistor. An 866kΩ external resistor should be connected between VBUS_DET pin and VBUS pin. This large resistor plays an important role in protecting the SGM7220DRP from large V_{BUS} voltage that is possible in present systems. The external resistor along with internal pull-down resistor forms a voltage dividing network and it can ensure the VBUS_DET voltage within the SGM7220DRP specification.

The USB2.0 specification requires that multiple decoupling capacitors should be connected to VBUS. When the SGM7220DRP is used in DFP mode, the value of decoupling capacitor needs to keep 120μF at least. In this application, a 150μF capacitor was placed near V_{BUS}.

Application Curve

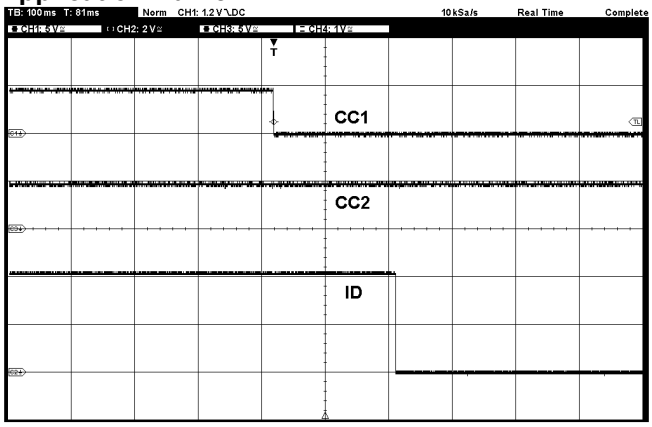


Figure 13. Application Curve for DFP in I^2C Mode

APPLICATION INFORMATION (continued)

UFP in I²C Mode

The SGM7220DRP is configured as a UFP in I²C mode as shown in Figure 14.

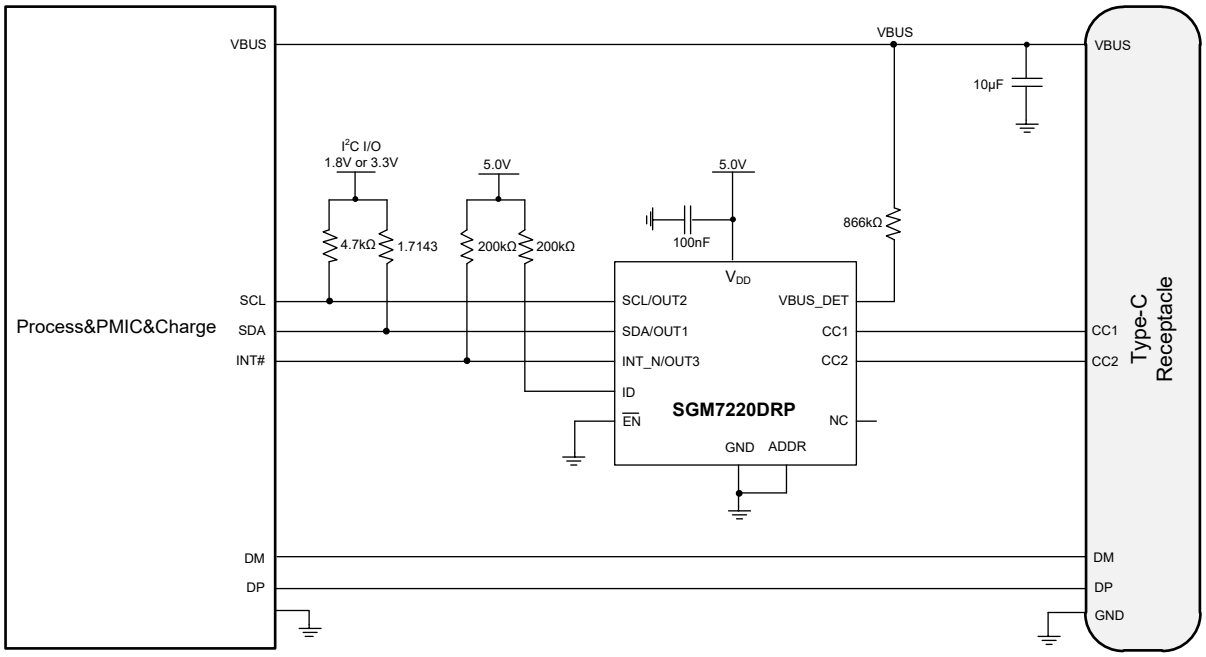


Figure 14. UFP in I²C Mode Schematic

Design Descriptions

For this reference design, the parameters configuration is shown in Table 10.

Table 10. Design Description for UFP in I²C Mode

Design Parameter	Option	Circuit Design
V_{DD} Supply	2.75V to 5V	V_{DD} is tied to 5V.
Mode Select	I²C or GPIO	I²C: ADDR pin must be pulled down or pulled up.
I²C Address Select	0x47 or 0x67	0x47: ADDR is tied to GND.
Type-C Port Type	UFP, DFP or DRP	UFP: Configured through I²C interface.
$\overline{EN}$ Configuration	Active or shutdown	Active: $\overline{EN}$ pin is tied to GND

Detailed Descriptions of Reference Design

The SGM7220DRP V_{DD} range is required to between 2.75V and 5V. In this application, V_{DD} is connected to 5V. A 100nF decoupling capacitor is placed near the V_{DD} pin. If V_{BUS} voltage is not more than 5.5V, the power supply of SGM7220DRP can be connected to V_{BUS} through a diode.

The SGM7220DRP is configured in I²C mode by pulling the ADDR pin high or low. In this application, the ADDR pin is connected to GND and the SGM7220DRP I²C address is set to 0x47. The SDA and SCL should be pulled up to 1.8V or 3.3V by a resistor. If the SDA and SCL are pulled up to 3.3V, the voltage of V_{DD} must be maintained above 3V to prevent the diode leakage between I²C port and V_{DD} pin.

The SGM7220DRP can be configured in shutdown mode by setting the $\overline{EN}$ pin high and keeps low power consumption in this mode. In this application, the $\overline{EN}$ pin is connected to V_{DD} pin and it can also be controlled externally if it is necessary for practical application.

The INT_N/OUT3 pin is an open-drain output and it used to indicate the changes of the SGM7220DRP I²C registers. The INT_N/OUT3 pin needs an external 200kΩ pull-up resistor to ensure operating normally.

APPLICATION INFORMATION (continued)

The Type-C port mode is controlled by software configuration. The software implementation operates the MODE_SELECT register through the I^2C interface. It is important that the SGM7220DRP must keep in unattached state if configured by software.

The VBUS_DET pin is used to detect V_{BUS} on the Type-C port and it has an internal pull-down resistor. An 866kΩ resistor should be connected between VBUS_DET and VBUS. This large resistor plays an important role in protecting the SGM7220DRP from large V_{BUS} voltage that is possible in present systems. The external resistor along with internal pull-down resistor forms a voltage dividing network and it can ensure the VBUS_DET voltage within the SGM7220DRP specification.

The USB2.0 specification requires that multiple decoupling capacitors should be connected to VBUS. When the SGM7220DRP is used in UFP mode, the value of decoupling capacitor needs to keep between 1μF to 10μF. In this application, a 1μF capacitor was placed near the V_{BUS}.

Application Curves

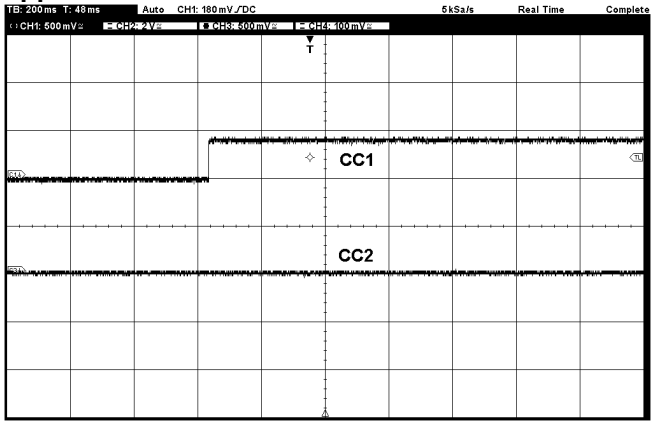


Figure 15. Application Curve for UFP in I^2C Mode

Initialization Process

The SGM7220DRP Initialization Process is as follows when the $\overline{EN}$ pin is pulled up to GND:

1. The system shuts down when V_{DD} is no power supply and the SGM7220DRP is autonomously configured as a UFP. Both CC1 and CC2 pin are internally connected to pull-down resistors (R_D) in dead battery.

2. V_{DD} powers on and the SGM7220DRP is enabled.

3. I^2C powers up.

4. The SGM7220DRP enters unattached mode and is autonomously configured as DRP mode.

5. The SGM7220DRP detects the state of CC1 and CC2 pins to determine as a DFP and V_{BUS} for attachment as a UFP.

6. The SGM7220DRP enters active mode when attachment has been successfully detected.

Power Supply Recommendations

The SGM7220DRP can work well in the power supply range from 2.7V to 5V. Also, the V_{DD} can be connected to a system power such as a battery.

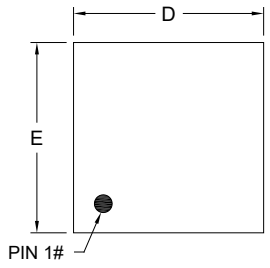
REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

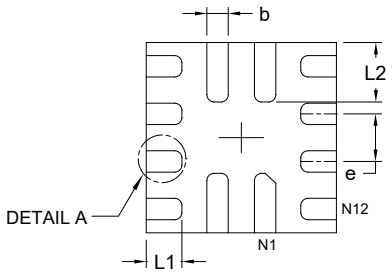
Changes from Original to REV.A (JUNE 2026)	Page
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

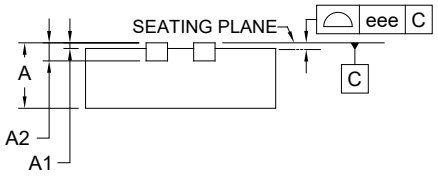
UTQFN-1.6×1.6-12L



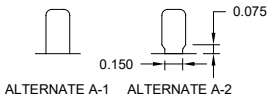
TOP VIEW



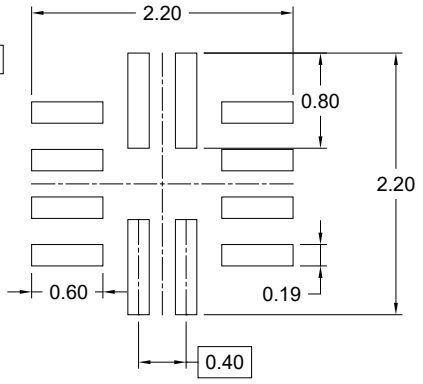
BOTTOM VIEW



SIDE VIEW



DETAIL A
ALTERNATE TERMINAL CONSTRUCTION



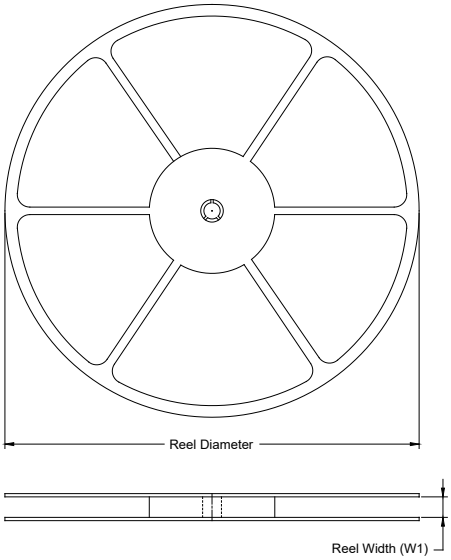
RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	0.450	-	0.600
A1	-	-	0.050
A2	0.152 REF		
e	0.400 BSC		
D	1.550	1.600	1.650
E	1.550	1.600	1.650
b	0.130	0.190	0.250
L1	0.250	0.300	0.350
L2	0.450	0.500	0.550
eee	-	0.080	-

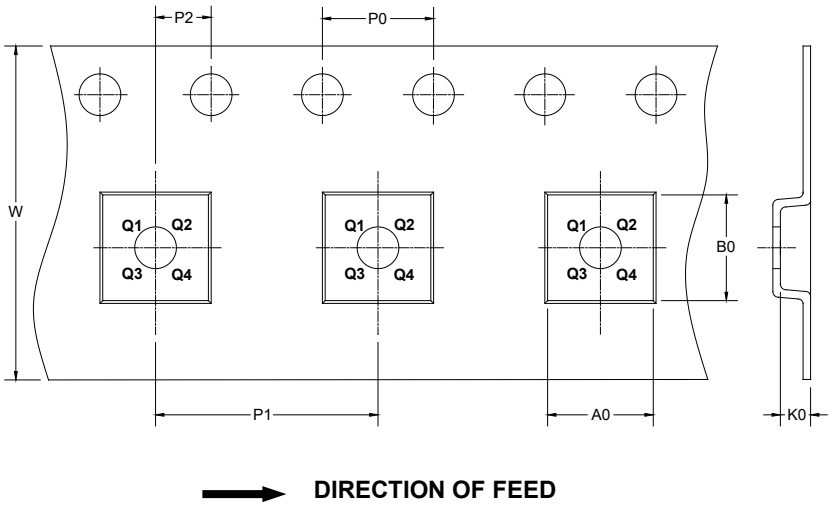
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



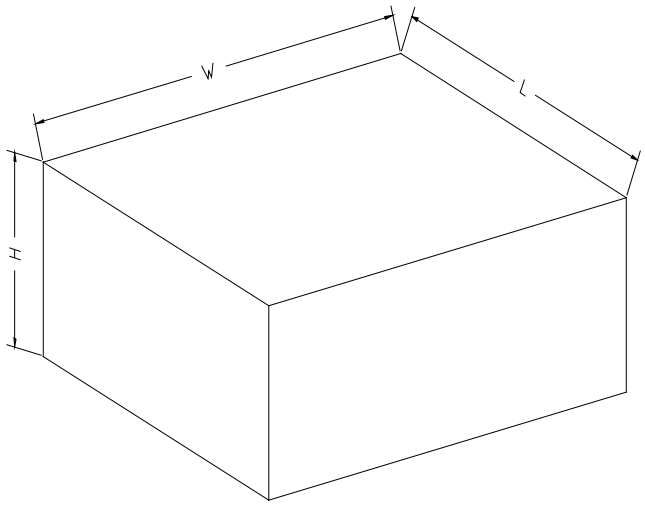
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
UTQFN-1.6×1.6-12L	7"	9.0	1.78	1.78	0.69	4.0	4.0	2.0	8.0	Q2

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18

DD0002