SGM41612YGA
I²C Controlled High Voltage 4:1 18A Switched-Capacitor Charger

GENERAL DESCRIPTION

The SGM41612YGA is an efficient 18A switched-capacitor battery charging device with I²C control that can be configured to 8 different operation modes: forward 4:1/3:1/2:1/1:1 step-down charging modes and reverse 1:4/1:3/1:2/1:1 step-up discharging modes. It can charge single-cell Li-Ion or Li-polymer battery in a wide 3.4V to 21V input voltage range (VBUS) from smart wall adapters or wireless charger. In 4:1 mode, the switched-capacitor architecture is optimized for 50% duty cycle to cut the input current to one-quarter of the battery current and reduce the wiring drops, losses and temperature rise in the application.

A two-channel switched-capacitor topology is used to reduce the required input capacitors and minimize the output ripple. It integrates a single channel driver for external OVPFETs.

The SGM41612YGA is available in a Green WLCSP-3.4×4.44-80B-A package.

APPLICATIONS

Smart Phone, Tablet PC

FEATURES

- **8 Different Operation Modes**
  - **Forward 4:1/3:1/2:1/1:1 Step-down Charging Modes**
  - **Reverse 1:4/1:3/1:2/1:1 Step-up Discharging Modes**
- **Efficiency Optimized Switched-Capacitor Architecture**
  - **Up to 18A Output Current**
  - **3.4V to 21V Input Voltage Range**
  - **200kHz to 1.5MHz Switching Frequency Setting**
  - **Above 97.2% Forward 4:1 Step-down Mode Efficiency (When V_{VOUT} = 5V, I_{VOUT} = 8A)**
  - **Above 96.1% Forward 4:1 Step-down Mode Efficiency (When V_{VOUT} = 5V, I_{VOUT} = 13A)**
  - **Above 97.9% Forward 2:1 Step-down Mode Efficiency (When V_{VOUT} = 5V, I_{VOUT} = 2A)**
  - **Above 97.4% Forward 2:1 Step-down Mode Efficiency (When V_{VOUT} = 5V, I_{VOUT} = 8A)**
- **Comprehensive Integrated Protection Features**
  - **External VUSB OVPFET Control**
  - **Input Over-Voltage and Over-Current Protection**
  - **Input Under-Current Protection**
  - **Output Over-Voltage Protection**
  - **Battery Over-Voltage and Over-Current Protection**
  - **C_{FLY} and Bootstrap Capacitor Diagnosis (PIN_DIAG)**
  - **Switch Peak Over-Current Protection**
  - **Thermal Shutdown Protection**
- **8-Channel 12-Bit (Effective) ADC Converter**
  - **VUSB, VBUS, IBUS, VOUT, VBAT1, VBAT2, IBAT, TDIE for Monitoring**

TYPICAL APPLICATION

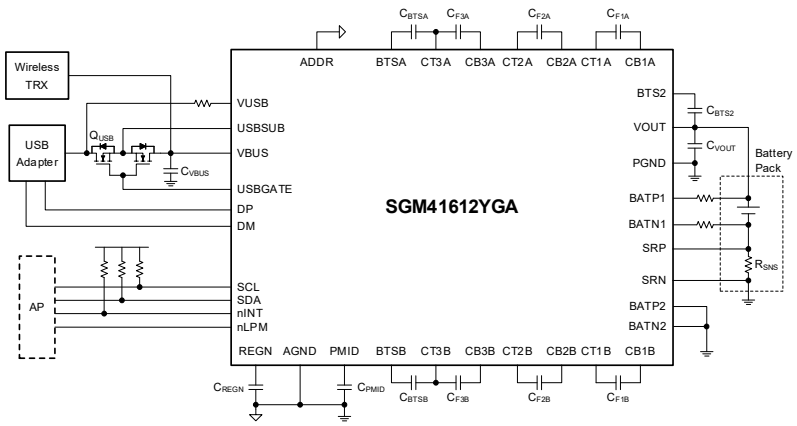


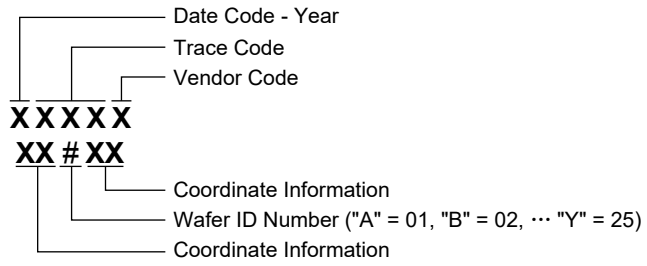
Figure 1. Simplified Schematic

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM41612YGA	WLCSP-3.4×4.44-80B-A	-40℃ to +85℃	SGM41612YGA/TR	SGM 41612 XXXXX XX#XX	Tape and Reel, 1500

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code. XX#XX = Coordinate Information and Wafer ID Number.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

VUSB (Converter not switching) ..... -0.3V to 35V
USBGATE..... -0.3V to 33V
USBGATE to USBSUB..... -0.3V to 12V
USBGATE to VBUS..... -27V to 12V
USBSUB, VBUS, PMID (Converter not Switching)
..... -0.3V to 27V
PMID to VBUS..... -0.3V to 6V
PMID to CT3A/CT3B ..... -0.3V to 20V
PMID to CT1A/CT1B ..... -0.3V to 20V
CB3A/CB3B to PGND, CT3A/CT3B to VOUT.... -0.3V to 18V
CB2A/CB2B to PGND, CT2A/CT2B to VOUT.... -0.3V to 18V
CT2A to CB3A, CT1A to CB2A, VOUT to CB1A.. -0.3V to 6V
CT2B to CB3B, CT1B to CB2B, VOUT to CB1B.. -0.3V to 6V
VOUT, CB1A/CB1B to PGND, BTSA-CT3A, BTSB-CT3B
..... -0.3V to 6V
BTS2 to VOUT..... -0.3V to 6V
SCL, SDA, nINT, nLPM, ADDR, REGN, BATP1, BATN1,
BATP2, BATN2, SRP, SRN, DP, DM ..... -0.3V to 6V
SRP to SRN..... -0.5V to 0.5V
Package Thermal Resistance
WLCSP-3.4×4.44-80B-A, θ_{JA}..... 25.7℃/W
WLCSP-3.4×4.44-80B-A, θ_{JB}..... 1.1℃/W
WLCSP-3.4×4.44-80B-A, θ_{JC}..... 4.7℃/W
Junction Temperature.....+150℃
Storage Temperature Range .....-65℃ to +150℃
Lead Temperature (Soldering, 10s).....+260℃
ESD Susceptibility (1) (2)
HBM.....±3000V
CDM .....±1000V

NOTES:

1. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.

2. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

RECOMMENDED OPERATING CONDITIONS

VUSB .....3.4V to 21V
VBUS (Forward 4:1 Mode) .....10.8V to 21V
VBUS (Forward 3:1 Mode) .....8.1V to 16V
VBUS (Forward 2:1 Mode) .....5.4V to 11V
VBUS (Forward 1:1 Mode) .....3.4V to 5.5V
VOUT, BATP (Forward 4:1/3:1/2:1 Mode).....2.7V to 5.5V
VOUT, BATP (Forward 1:1 Mode).....3.4V to 5.5V
(SRP - SRN).....-0.05V to 0.05V
Junction Temperature Range..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

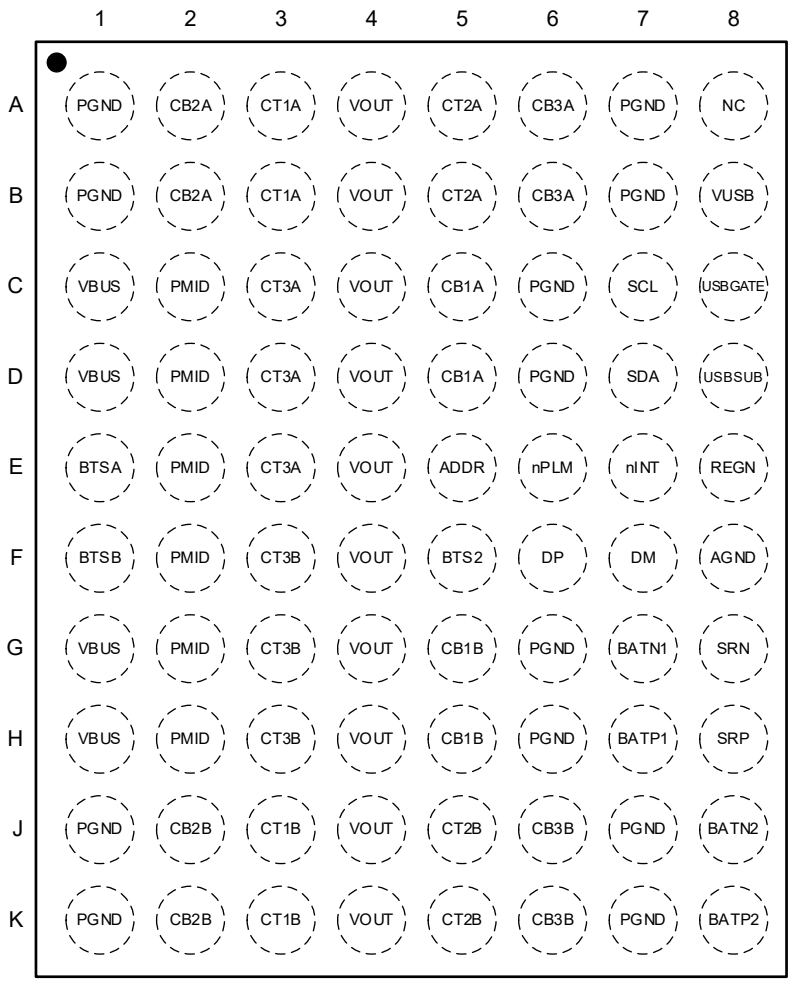
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

(TOP VIEW)



WLCSP-3.4×4.44-80B-A

PIN DESCRIPTION

PIN	NAME	TYPE (1)	FUNCTION
A1, A7, B1, B7 C6, D6, G6, H6 J1, J7, K1, K7	PGND	P	Power Ground Pins.
A2, B2	CB2A	P	Channel-A Flying Capacitor C_{F2A} Bottom Plate Pins. Connect three 22μF or larger parallel capacitors between CT2A and CB2A pins as close as possible to the device.
A3, B3	CT1A	P	Channel-A Flying Capacitor C_{F1A} Top Plate Pins. Connect three 22μF or larger parallel capacitors between CT1A and CB1A pins as close as possible to the device.
A4, B4, C4, D4 E4, F4, G4, H4 J4, K4	VOUT	P	Output Pins. Connect to the battery pack positive terminal. At least three 10μF capacitors between VOUT and PGND pins are recommended.
A5, B5	CT2A	P	Channel-A Flying Capacitor C_{F2A} Top Plate Pins. Connect three 22μF or larger parallel capacitors between CT2A and CB2A pins as close as possible to the device.
A6, B6	CB3A	P	Channel-A Flying Capacitor C_{F3A} Bottom Plate Pins. Connect three 22μF or larger parallel capacitors between CT3A and CB3A pins as close as possible to the device.
A8	NC	N/A	No Connection.
B8	VUSB	AI	USB Charging DC Voltage Sense Input Pin. Connect it to the drain of the external N-MOSFET, or short it together with VBUS when USBGATE control function is disabled.
C1, D1, G1, H1	VBUS	P	Device Power Input Pins. Use at least two 4.7μF capacitors between VBUS and PGND pins close to the device.
C2, D2, E2, F2 G2, H2	PMID	P	Power Stage Supply Input Pins. Bypass them with at least two 10μF ceramic capacitors to PGND.
C3, D3, E3	CT3A	P	Channel-A Flying Capacitor C_{F3A} Top Plate Pins. Connect three 22μF or larger parallel capacitors between CT3A and CB3A pins as close as possible to the device.
C5, D5	CB1A	P	Channel-A Flying Capacitor C_{F1A} Bottom Plate Pins. Connect three 22μF or larger parallel capacitors between CT1A and CB1A pins as close as possible to the device.
C7	SCL	DI	I²C Interface Clock Line.
C8	USBGATE	AO	External Dual N-MOSFET Gate Control Pin. Connect to the gate of the external back-to-back N-MOSFET in the USB charging path, or leave it shorted to ground to disable USBGATE control function.
D7	SDA	DIO	I²C Interface Data Line. The SDA line is forced to release when the I²C timeout fault occurs.
D8	USBSUB	AI	External Back-to-Back N-MOSFET Common Source Input Pin. Connect it to VBUS pin when drive the GaN FET as OVPFET (Q_{USB}). Leave it shorted to ground when USBGATE function is disabled.
E1	BTSA	P	Channel-A Bootstrap Pin. It is the bootstrap pin to supply Q_{1A} gate driver. Use a 0.1μF or larger MLCC capacitor from this pin to CT3A pin.
E5	ADDR	AIO	This pin is used to assign the I²C address of the device during POR period. Connect ADDR pin directly to AGND to select address 0x67. Leave ADDR pin floating to select address 0x68.
E6	nLPM	AI	Low Power Mode Enable Input Pin with an internal 1MΩ pull-down resistor. When battery only, the logic low actives the low power mode with low quiescent current, and the I²C bus does not need to respond; when the VUSB is inserted or VBUS is present, the state of nLPM pin is ignored and the device exits low power mode. A rising edge on nLPM pin and keeping high for more than 10μs triggers a hard reset of the device. Excepted for the specified bits, all other register bits are reset to their default values if a hard reset is triggered.
E7	nINT	DO	Open-Drain Interrupt Output Pin. Use a 10kΩ pull up to the logic high rail. The nINT pin is active low and sends a negative 256μs pulse to inform the AP about a new charger status update or a fault.
E8	REGN	AO	Internal Circuit Power Supply. Internal connected to VOUT after enable SCC_EN. Connect a 4.7μF MLCC capacitor between this pin and AGND. It is recommended not to connect any external load to REGN.
F1	BTSB	P	Channel-B Bootstrap Pin. It is the bootstrap pin to supply Q_{1B} gate driver. Use a 0.1μF or larger MLCC capacitor from this pin to CT3B pin.
F3, G3, H3	CT3B	P	Channel-B Flying Capacitor C_{F3B} Top Plate Pins. Connect three 22μF or larger parallel capacitors between CT3B and CB3B pins as close as possible to the device.

PIN DESCRIPTION (continued)

PIN	NAME	TYPE (1)	FUNCTION
F5	BTS2	AIO	Charge Pump for Gate Drive. Connect a 0.22μF MLCC capacitor between BTS2 and VOUT.
F6	DP	AIO	USB Communication Interface Positive Line. Connect to the USB D+ data line.
F7	DM	AIO	USB Communication Interface Negative Line. Connect to the USB D- data line.
F8	AGND	P	Analog Ground Pin.
G5, H5	CB1B	P	Channel-B Flying Capacitor C_{F1B} Bottom Plate Pins. Connect three 22μF or larger parallel capacitors between CT1B and CB1B pins as close as possible to the device.
G7	BATN1	AI	Battery 1 Voltage Sensing Negative Input. Connect a 100Ω resistor between BATN1 and negative terminal of the battery pack. Connect this pin to ground if not used.
G8	SRN	AI	High-side or Low-side Battery Current Sensing Negative Input. Place a 0.5mΩ, 1mΩ or 2mΩ (R_{SNS}) shunt resistor between SRP and SRN pins. Short SRN to ground if not used.
H7	BATP1	AI	Battery 1 Voltage Sensing Positive Input. Connect a 100Ω resistor between BATP1 and positive terminal of the battery pack. Connect this pin to ground if not used.
H8	SRP	AI	High-side or Low-side Battery Current Sensing Positive Input. Place a 0.5mΩ, 1mΩ or 2mΩ (R_{SNS}) shunt resistor between SRP and SRN pins. Short SRP to ground if not used.
J2, K2	CB2B	P	Channel-B Flying Capacitor C_{F2B} Bottom Plate Pins. Connect three 22μF or larger parallel capacitors between CT2B and CB2B pins as close as possible to the device.
J3, K3	CT1B	P	Channel-B Flying Capacitor C_{F1B} Top Plate Pins. Connect three 22μF or larger parallel capacitors between CT1B and CB1B pins as close as possible to the device.
J5, K5	CT2B	P	Channel-B Flying Capacitor C_{F2B} Top Plate Pins. Connect three 22μF or larger parallel capacitors between CT2B and CB2B pins as close as possible to the device.
J6, K6	CB3B	P	Channel-B Flying Capacitor C_{F3B} Bottom Plate Pins. Connect three 22μF or larger parallel capacitors between CT3B and CB3B pins as close as possible to the device.
J8	BATN2	AI	Battery 2 Voltage Sensing Negative Input. Connect a 100Ω resistor between BATN2 and negative terminal of the battery pack. Connect this pin to ground if not used.
K8	BATP2	AI	Battery 2 Voltage Sensing Positive Input. Connect a 100Ω resistor between BATP2 and positive terminal of the battery pack. Connect this pin to ground if not used.

NOTE: P = power, AI = analog input, AO = analog output, AIO = analog input/output, DI = digital input, DIO = digital input/output.

TYPICAL APPLICATION CIRCUITS

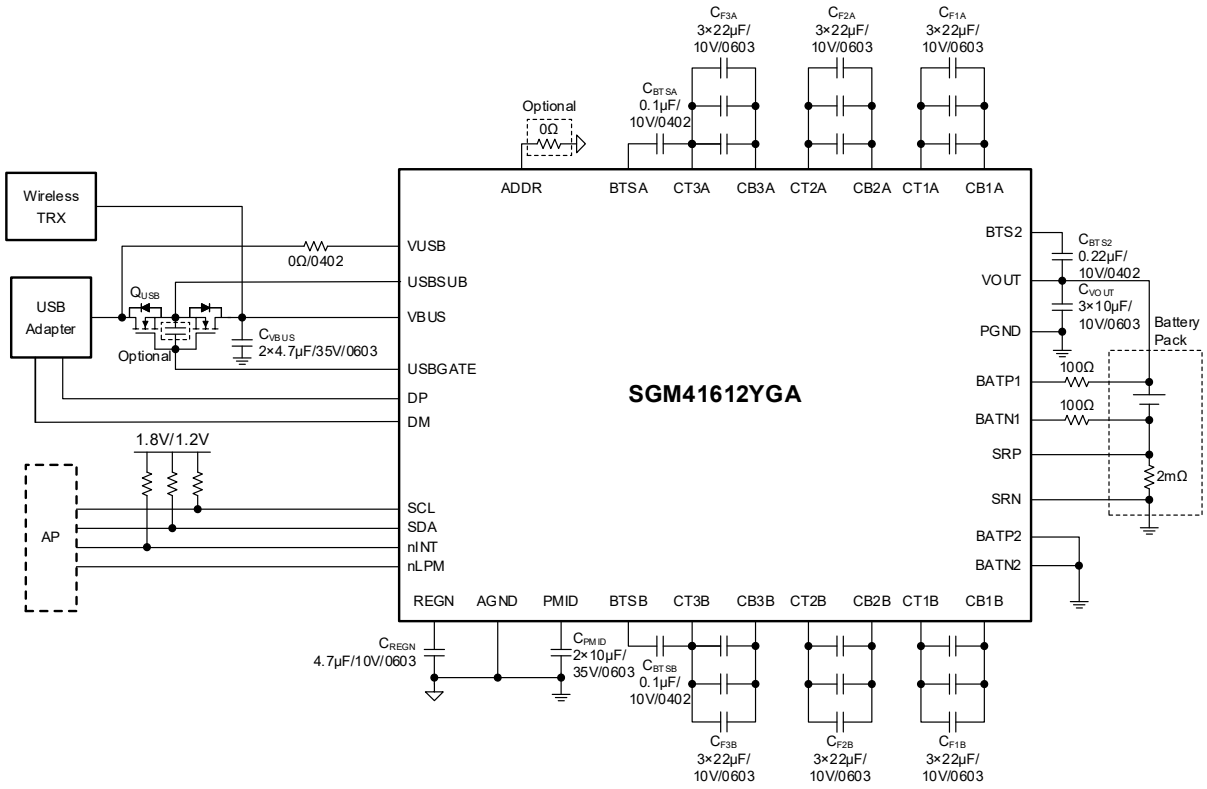


Figure 2. Single SGM41612YGA Typical Application Circuit

TYPICAL APPLICATION CIRCUITS (continued)

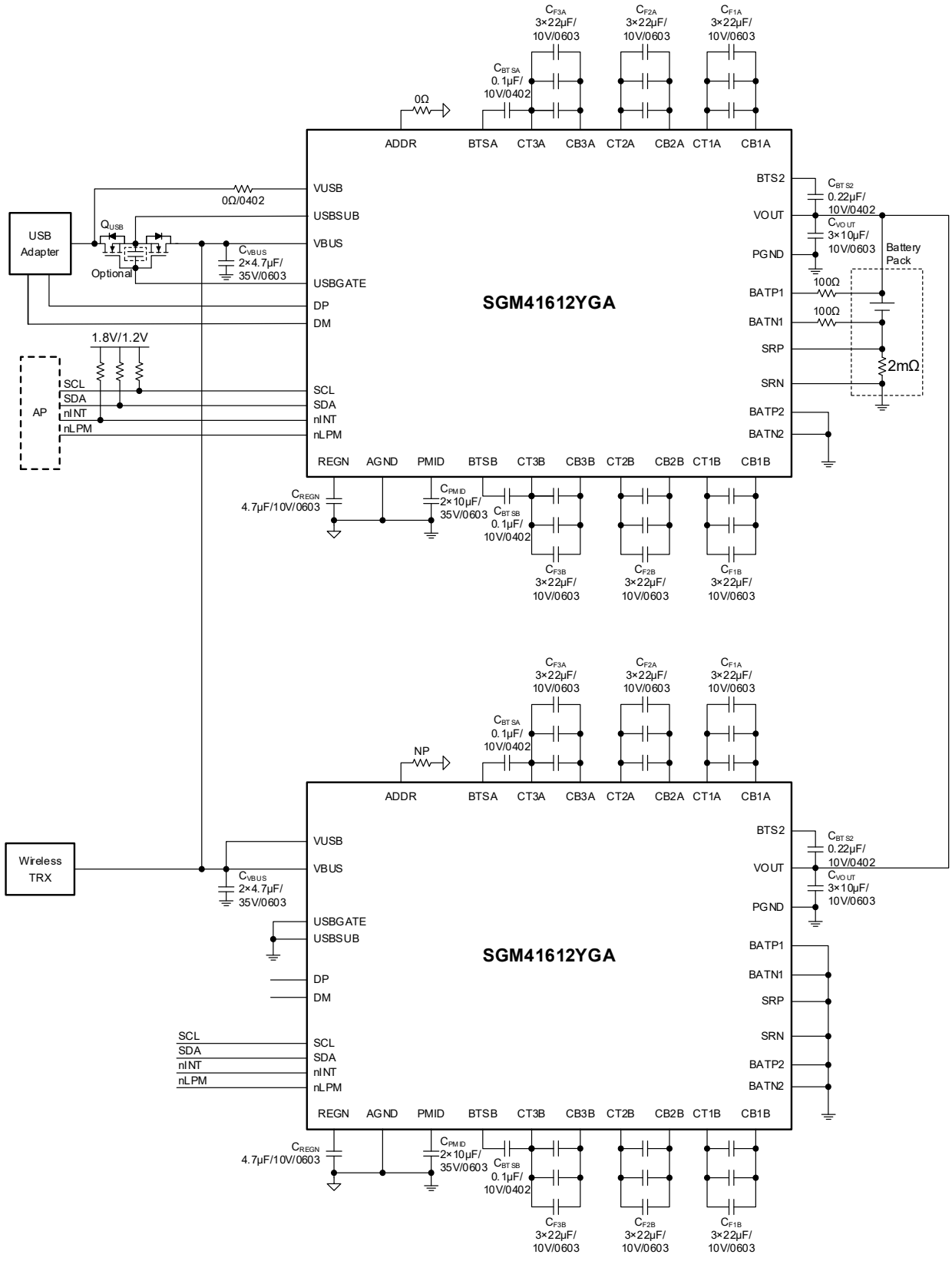


Figure 3. Dual SGM41612YGA Typical Application Circuit

ELECTRICAL CHARACTERISTICS

(T_J = -40℃ to +85℃, typical values are measured at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Currents						
VUSB Quiescent Current	I_{Q_VUSB}	ADC disabled, SCC disabled, Q_{USB} used with driver disabled (USBGATE_EN = 0, USBGATE_MODE = 1), $V_{USB_OVP_R}$ = 23V (VUSB_OVP[3:0] bits = 4'b1100), V_{VUSB} = 21V		0.3	0.5	mA
		ADC disabled, SCC disabled, Q_{USB} used with driver enabled (USBGATE_MODE = 0) $V_{USB_OVP_R}$ = 23V (VUSB_OVP[3:0] bits = 4'b1100), V_{VUSB} = 21V		0.9	1.5	mA
VBUS Quiescent Current	I_{Q_VBUS}	SCC enabled (SCC_MODE[2:0] = 3'b000, SCC_EN = 1), Q_{USB} used with both drivers disabled, no load, V_{VBUS} = 20V > (4 × V_{VOUT}), f_{SW} = 600kHz		15		mA
Battery Only Quiescent Current	I_{Q_VOUT}	ADC disabled, SCC disabled, nLPM pin = high, VUSB and VBUS not present, V_{VOUT} = 4.2V		10	20	μA
Battery Only Shutdown Current	I_{SHDN_VOUT}	ADC disabled, SCC disabled, nLPM pin = low, VUSB and VBUS not present, V_{VOUT} = 4.2V		5	10	μA
Leakage Current at pin BATP1, BATP2, BATN1, BATN2	I_{LKG_BAT}	V_{VOUT} < $V_{VOUT_PRESENT_F}$			1	μA
		ADC enabled			5	
VUSB UVLO Rising Threshold	$V_{USB_UVLO_R}$	V_{VUSB} rising, for active I²C		2.9	3.15	V
VUSB UVLO Falling Threshold	$V_{USB_UVLO_F}$	V_{VUSB} falling		2.7		V
VUSB UVLO Hysteresis	$V_{USB_UVLO_HYS}$			200		mV
VBUS UVLO Rising Threshold	$V_{BUS_UVLO_R}$	V_{VBUS} rising, for active I²C		2.9	3.15	V
VBUS UVLO Falling Threshold	$V_{BUS_UVLO_F}$	V_{VBUS} falling		2.7		V
VBUS UVLO Hysteresis	$V_{BUS_UVLO_HYS}$			200		mV
VOUT UVLO Rising Threshold	$V_{VOUT_UVLO_R}$	VOUT pin, V_{VOUT} rising, for active I²C		2.5		V
VOUT UVLO Falling Threshold	$V_{VOUT_UVLO_F}$	VOUT pin, V_{VOUT} falling		2.3		V
VOUT UVLO Hysteresis	$V_{VOUT_UVLO_HYS}$			200		mV
VBAT Insert Threshold	$V_{BAT_INSERT_R}$	VOUT pin, V_{VOUT} rising, forward mode		2.8		V
	$V_{BAT_INSERT_F}$	VOUT pin, V_{VOUT} falling, forward mode		2.7		V
	$V_{BAT_INSERT_HYS}$	Hysteresis		100		mV
External OVPFET Control						
External OVPFET Gate Drive Voltage (Initialization)	V_{QOVP_GATE}	I²C programmable, GATE_HI_SET bit = 0, $V_{USBGATE}$ - V_{USBSUB} when V_{VUSB} ≥ 3V	4.6	5	5.25	V
		I²C programmable, GATE_HI_SET bit = 1, $V_{USBGATE}$ - V_{USBSUB} when V_{VUSB} ≥ 4.75V	8	9	10	
VUSB Insert Rising Threshold	$V_{USB_INSERT_R}$	VUSB pin, V_{VUSB} rising		3.2	3.4	V
VUSB Insert Falling Threshold	$V_{USB_INSERT_F}$	VUSB pin, V_{VUSB} falling		3.1		V
VUSB Insert Hysteresis	$V_{USB_INSERT_HYS}$			100		mV
VUSB Insert Rising Threshold Deglitch Time	$t_{USBGATE_ON_DEG}$	Deglitch between V_{VUSB} rising above $V_{USB_INSERT_R}$ and sending an nINT pulse, then to start external Q_{USB} turn-on (USBGATE_MODE = 0, USBGATE_ON_DEG[1:0] = 2'b00), R_{PDN_VUSB} PoorSRC qualification during $t_{USBGATE_ON_DEG}$		10		ms
VUSB Insert Falling Threshold Deglitch Time	$t_{USBGATE_OFF_DEG}$	Deglitch between V_{VUSB} falling below $V_{USB_INSERT_F}$ and sending an nINT pulse		2		ms
VUSB OVP Rising Threshold Range	$V_{USB_OVP_R}$	I²C programmable, 11V by default	6.5		25	V
VUSB OVP Threshold Accuracy	$V_{USB_OVPR_ACC}$	$V_{USB_OVP_R}$ = 12V or 22V	-2		2	%
VUSB OVP Threshold Hysteresis	$V_{USB_OVP_HYS}$	V_{VUSB} falling to turn on Q_{USB} again after VUSB OVP active		1		V
VUSB OVP Rising Deglitch Time	$t_{VUSB_OVP_DEG}$	Deglitch between V_{VUSB} rising above $V_{USB_OVP_R}$ and triggering the protection action		100		ns

ELECTRICAL CHARACTERISTICS (continued)

(T_J = -40℃ to +85℃, typical values are measured at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
VUSB Pull-down Resistor	R_{PDN_VUSB}	V_{VUSB} = 5V, VUSB_PDN_EN = 1, VUSB_PDN_MODE = 0			350		Ω
VBUS Pull-down Resistor	R_{PDN_VBUS}	VBUS and PMID pins V_{VBUS} = 5V, VBUS_PDN_EN = 1			10		kΩ
Switched-Cap Converter							
VBUS to VOUT Resistance	$R_{VBUS2VOUT}$	Forward 1:1 mode			17		mΩ
R_{DSON} of Reverse Blocking FET	R_{DS_QRB}	V_{VBUS} = 18V, V_{VOUT} = 4.5V, I_{DS} = 1A (including package resistance)			4		mΩ
R_{DSON} of $Q_{1A/1B}$	R_{DS_Q1}	V_{VBUS} = 18V, V_{VOUT} = 4.5V, I_{DS} = 1A (including package resistance)			15		mΩ
R_{DSON} of $Q_{2A/2B}$	R_{DS_Q2}	V_{VBUS} = 18V, V_{VOUT} = 4.5V, I_{DS} = 1A (including package resistance)			10		mΩ
R_{DSON} of $Q_{3A/3B}$	R_{DS_Q3}	V_{VBUS} = 18V, V_{VOUT} = 4.5V, I_{DS} = 1A (including package resistance)			12		mΩ
R_{DSON} of $Q_{4A/4B}$	R_{DS_Q4}	V_{VBUS} = 18V, V_{VOUT} = 4.5V, I_{DS} = 1A (including package resistance)			14		mΩ
R_{DSON} of $Q_{5A/5B}$	R_{DS_Q5}	V_{VBUS} = 18V, V_{VOUT} = 4.5V, I_{DS} = 1A (including package resistance)			13		mΩ
R_{DSON} of $Q_{6A/6B}$	R_{DS_Q6}	V_{VBUS} = 18V, V_{VOUT} = 4.5V, I_{DS} = 1A (including package resistance)			11		mΩ
R_{DSON} of $Q_{7A/7B}$	R_{DS_Q7}	V_{VBUS} = 18V, V_{VOUT} = 4.5V, I_{DS} = 1A (including package resistance)			8		mΩ
R_{DSON} of $Q_{8A/8B}$	R_{DS_Q8}	V_{VBUS} = 18V, V_{VOUT} = 4.5V, I_{DS} = 1A (including package resistance)			8		mΩ
R_{DSON} of $Q_{9A/9B}$	R_{DS_Q9}	V_{VBUS} = 18V, V_{VOUT} = 4.5V, I_{DS} = 1A (including package resistance)			8		mΩ
R_{DSON} of $Q_{10A/10B}$	R_{DS_Q10}	V_{VBUS} = 18V, V_{VOUT} = 4.5V, I_{DS} = 1A (including package resistance)			8		mΩ
VBUS Present Rising Threshold	$V_{BUS_PRESENT_R}$	V_{VBUS} rising			3.2	3.4	V
VBUS Present Falling Threshold	$V_{BUS_PRESENT_F}$	V_{VBUS} falling			3.1		V
VBUS Present Hysteresis	$V_{BUS_PRESENT_HYS}$				100		mV
VBUS Present Falling Threshold Deglitch Time	$t_{VBUS_OUT_DEG}$	Deglitch between V_{VBUS} falling below $V_{BUS_PRESENT_F}$ and sending an nINT pulse			2		ms
VBAT Brown-In Threshold for Reverse Mode	$V_{BAT_BRN_IN}$	VOUT pin, V_{VOUT} rising, reverse mode			3.2		V
VBAT Brown-Out Threshold for Reverse Mode	$V_{BAT_BRN_OUT}$	VOUT pin, V_{VOUT} falling, reverse mode			2.8		V
VBAT Brown-In/Out Threshold Hysteresis	$V_{BAT_BRN_HYS}$	VOUT pin			400		mV
VBAT Brown-In Threshold Deglitch Time	$t_{VBAT_BRN_IN_DEG}$	Deglitch between V_{VOUT} rising above $V_{BAT_BRN_IN}$ and enabling the AP to read to reset the flag bit			1		ms
VBAT Brown-Out Threshold Deglitch Time	$t_{VBAT_BRN_OUT_DEG}$	Deglitch between V_{VOUT} falling below $V_{BAT_BRN_OUT}$ and exit reverse mode switching			48		ms
Converter Switching Frequency Range	f_{SW}	I²C programmable Range, 600kHz by default		200		1500	kHz
Converter Switching Frequency Initial Accuracy	f_{SW_ACC}	f_{SW} = 600kHz		-5		5	%
Protection							
nINT Low Pulse Duration when a Protection Occurs	t_{INT}				256		μs
VBUS OVP Rising Threshold Range	$V_{BUS_OVP_R}$	In forward 4:1 /reverse 1:4 mode	I²C programmable, 22V by default	14		26.6	V
			Accuracy at 22V $V_{BUS_OVP_R}$	-2		2	%
			V_{BUS_OVP} hysteresis		800		mV
		In forward 3:1 /reverse 1:3 mode	I²C programmable, 16.5V by default	10.5		19.95	V
			Accuracy at 16.5V $V_{BUS_OVP_R}$	-2		2	%
			V_{BUS_OVP} hysteresis		600		mV

ELECTRICAL CHARACTERISTICS (continued)

(T_J = -40℃ to +85℃, typical values are measured at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
VBUS OVP Rising Threshold Range	$V_{BUS_OVP_R}$	In forward 2:1 /reverse 1:2 mode	I²C programmable, 11V by default	7		13.3	V
			Accuracy at 11V $V_{BUS_OVP_R}$	-2		2	%
			V_{BUS_OVP} hysteresis		400		mV
		In forward 1:1 /reverse 1:1 mode	I²C programmable, 5.5V by default	3.5		6.65	V
			Accuracy at 5.5V $V_{BUS_OVP_R}$	-1.5		2.5	%
			V_{BUS_OVP} hysteresis		200		mV
VBUS OVP Rising Deglitch Time	$t_{VBUS_OVPR_DEG}$	Deglitch between V_{VBUS} rising above $V_{BUS_OVP_R}$ and triggering protection action			1		ms
IBUS UCP Rising Threshold	$I_{BUS_UCP_R}$			100	200	300	mA
IBUS UCP Falling Threshold	$I_{BUS_UCP_F}$	Falling, $I_{BUS_UCP_F}$ = 100mA		50	100	150	mA
IBUS UCP Falling Deglitch Time	$t_{IBUS_UCPF_DEG}$	Deglitch between I_{BUS} falling below $I_{BUS_UCP_F}$ and triggering protection action I²C programmable, 8μs by default		0.002		256	ms
IBUS UCP Blanking Time	$t_{IBUS_UCP_BLK}$	Duration from charging beginning I²C programmable, 100ms by default		12.5		10240	ms
IBUS OCP Threshold Range	I_{BUS_OCP}	I²C programmable, forward mode, 3.4A by default		1		7.2	A
		I²C programmable, reverse mode, 3.4A by default		1		5	A
IBUS OCP Threshold Accuracy	$I_{BUS_OCP_ACC}$	I_{BUS_OCP} = 3.4A, forward mode		-5		5	%
		I_{BUS_OCP} = 3.4A, reverse mode		-5		5	%
IBUS OCP Deglitch Time	$t_{IBUS_OCP_DEG}$	Deglitch between I_{BUS} rising above I_{BUS_OCP} and trigger protection action, I²C programmable, 4μs by default		4		64	μs
PMID2VOUT OVP Rising Threshold Range	$V_{PMID2VOUT_OVP}$	PMID pin, I²C programmable, n × (V_{VOUT} + 400mV) by default (n = 1, 2, 3, or 4, depending on the operation mode)		n × (V_{VOUT} + 200mV)		n × (V_{VOUT} + 900mV)	mV
PMID2VOUT OVP Threshold Accuracy	$V_{PMID2VOUT_OVP_ACC}$	PMID pin, PMID2VOUT_OVP[2:0] = 3'b010, V_{VOUT} = 4.5V, forward 4:1 charger mode (n = 4)		19.12		20.08	V
PMID2VOUT OVP Rising Deglitch Time	$t_{PMID2VOUT_OVPR_DEG}$	Deglitch between V_{PMID} rising above $V_{PMID2VOUT_OVP_R}$ and triggering protection action, I²C programmable, 100ns by default		0.1		128	μs
PMID2VOUT UVP Falling Threshold Range	$V_{PMID2VOUT_UVP}$	PMID pin, I²C programmable, n × (V_{VOUT} - 150mV) by default (n = 1, 2, 3, or 4, depending on the operation mode)		n × (V_{VOUT} - 450mV)		n × (V_{VOUT} - 100mV)	mV
PMID2VOUT UVP Threshold Accuracy	$V_{PMID2VOUT_UVP_ACC}$	PMID pin, PMID2VOUT_UVP[2:0] = 3'b001, V_{VOUT} = 4.5V, forward 4:1 charger mode (n = 4)		17.02		17.78	V
PMID2VOUT UVP Falling Deglitch Time	$t_{PMID2VOUT_UVP_DEG}$	Deglitch between V_{PMID} falling below $V_{PMID2VOUT_UVP_F}$ and triggering protection action, I²C programmable, 100ns by default		0.1		10	μs
VOUT OVP Rising Threshold Range	$V_{VOUT_OVP_R}$	I²C programmable, 200mV per step, 5V by default		4.8		5.4	V
VOUT OVP Threshold Accuracy	$V_{VOUT_OVP_ACC}$	$V_{VOUT_OVP_R}$ = 5V		-2		2	%
VOUT OVP Threshold Hysteresis	$V_{VOUT_OVP_HYS}$				100		mV
VOUT OVP Rising Deglitch Time	$t_{VOUT_OVPR_DEG}$	Deglitch between V_{VOUT} rising above $V_{VOUT_OVP_R}$ and triggering protection action			1		μs
VBATx OVP Rising Threshold Range	$V_{BATx_OVP_R}$	I²C programmable, 25mV per step, 4.5V by default		4.5		5.275	V
VBATx OVP Threshold Initial Accuracy	$V_{BATx_OVP_ACC}$	$V_{BATx_OVP_R}$ = 4.5V		-0.5		0.5	%
VBATx OVP Threshold Hysteresis	$V_{BATx_OVP_HYS}$				100		mV
VBATx OVP Rising Deglitch Time	$t_{VBAT_OVPR_DEG}$	Deglitch between V_{BATx} rising above $V_{BATx_OVP_R}$ and triggering protection action I²C programmable, 100ns by default		0.1		10	μs
IBAT OCP Threshold Range	I_{BAT_OCP}	Bidirectional I_{BAT} I²C programmable, 10A by default		8		20.5	A
IBAT OCP Threshold Initial Accuracy	$I_{BAT_OCP_ACC}$	I_{BAT_OCP} = 10A, R_{SNS} = 2mΩ, forward mode		-2.5		2.5	%
		I_{BAT_OCP} = 10A, R_{SNS} = 2mΩ, reverse mode		-2.5		2.5	%

ELECTRICAL CHARACTERISTICS (continued)

(T_J = -40℃ to +85℃, typical values are measured at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
IBAT OCP Deglitch Time	$t_{IBAT_OCP_DEG}$	Deglitch between I_{BAT} rising above I_{BAT_OCP} and triggering protection action I^2C programmable, 1ms by default	0.1		1	ms
Reverse Mode Soft-start Timeout	$t_{RVS_SS_TMO}$	Range, I^2C programmable, 128ms by default	128		256	ms
TDIE OTP Rising Threshold	$T_{DIE_OTP_R}$			150		℃
TDIE OTP Threshold Hysteresis	$T_{DIE_OTP_HYS}$			20		℃
Watchdog Timeout Range	t_{WDT}	I^2C programmable, disabled by default	0.2		30	s
ADC Specification						
ADC Resolution	ADC_{RES}			12		bits
ADC VUSB Voltage Readable in REG0x1B and REG0x1C	V_{USB_ADC}	Effective Range	0		25.6	V
		LSB		6.25		mV
VUSB ADC Initial Accuracy	$V_{USB_ADC_ACC}$	V_{VUSB} = 10V, T_J = +25℃	-0.5		0.5	%
		V_{VUSB} = 10V	-1		1	%
		V_{VUSB} = 20V, T_J = +25℃	-0.5		0.5	%
		V_{VUSB} = 20V	-1		1	%
ADC VBUS Voltage Readable in REG0x19 and REG0x1A	V_{BUS_ADC}	Effective Range	0		25.6	V
		LSB		6.25		mV
VBUS ADC Initial Accuracy	$V_{BUS_ADC_ACC}$	V_{VBUS} = 10V, T_J = +25℃	-0.5		0.5	%
		V_{VBUS} = 10V	-1		1	%
		V_{VBUS} = 20V, T_J = +25℃	-0.5		0.5	%
		V_{VBUS} = 20V	-1		1	%
ADC IBUS Current Readable in REG0x17 and REG0x18	I_{BUS_ADC}	Effective Range	0		6.4	A
		LSB		1.5625		mA
IBUS ADC Initial Accuracy	$I_{BUS_ADC_ACC}$	I_{BUS} = 1A	-7		7	%
		I_{BUS} = 2A	-5		5	%
		I_{BUS} = 5A	-4		4	%
ADC VBAT1 Voltage Readable in REG0x1F and REG0x20	V_{BAT1_ADC}	Effective Range	0		5.12	V
		LSB		1.25		mV
ADC VBAT2 Voltage Readable in REG0x23 and REG0x24	V_{BAT2_ADC}	Effective Range	0		5.12	V
		LSB		1.25		mV
VBAT1/2 ADC Initial Accuracy	$V_{BAT1/2_ADC_ACC}$	$V_{BAT1/2}$ = 2.7V to 4.6V	-0.5		0.5	%
ADC IBAT Current Readable in REG0x21 and REG0x22	I_{BAT_ADC}	Effective Range	0		20	A
		LSB		5		mA
IBAT ADC Initial Accuracy	$I_{BAT_ADC_ACC}$	I_{BAT} = 1A, R_{SNS} = 2mΩ	-10		10	%
		I_{BAT} = 2A, R_{SNS} = 2mΩ	-5		5	%
		I_{BAT} = 10A, R_{SNS} = 2mΩ	-2		2	%
ADC VOUT Voltage Readable in REG0x1D and REG0x1E	V_{OUT_ADC}	Effective Range	0		5.12	V
		LSB		1.25		mV
VOUT ADC Initial Accuracy	$V_{OUT_ADC_ACC}$	V_{VOUT} = 2.7V to 5V	-0.5		0.5	%
ADC DIE Temperature Readable in REG0x25 and REG0x26	T_{DIE_ADC}	Effective Range	0		150	℃
		LSB		0.5		℃
TDIE ADC Accuracy	$T_{DIE_ADC_ACC}$			±7		℃

ELECTRICAL CHARACTERISTICS (continued)

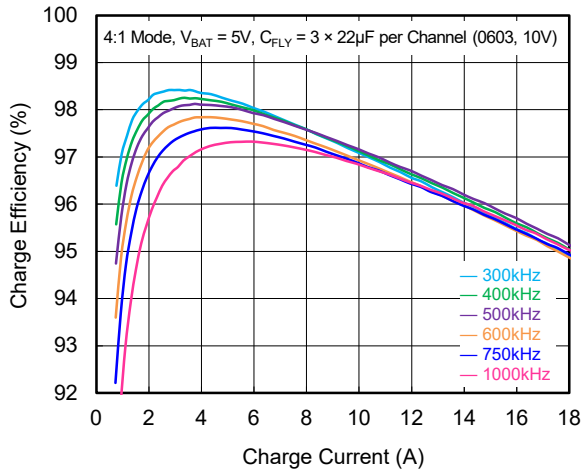
(T_J = -40℃ to +85℃, typical values are measured at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
I²C Interface (SCL and SDA Pins)						
High Level Input Voltage	V_{IH_I2C}	SCL and SDA pins	0.825			V
Low Level Input Voltage	V_{IL_I2C}	SCL and SDA pins			0.4	V
Low Level Output Voltage	V_{OL_SDA}	Sink 2mA, SDA pin			0.4	V
SCL Clock Frequency	f_{CLK}				1000	kHz
Logic I/O Threshold (nLPM, nINT Pins)						
High Level Input Voltage	V_{IH}	nLPM pin	0.825			V
Low Level Input Voltage	V_{IL}	nLPM pin			0.4	V
nLPM Pull-down Resistance	R_{PDN_nLPM}	Pulled down to AGND		1		MΩ
Low Level Output Voltage	V_{OL}	Sink 2mA, nINT pin			0.4	V
BC1.2 Detection (DP and DM Pins)						
Data Contact Detect Current Source	I_{DP_SRC}	DP pin	7	10	13	μA
DM Pull-down Resistance	R_{DM_DWN}	DM pin	16	20	24	kΩ
Data Contact Detect Logic Low Threshold	V_{LGC_LOW}	DP pin			0.8	V
Data Contact Detect Debounce Time	t_{DCD_DBNC}		10	15		ms
DP Force Detect Voltage	V_{DP_SRC}	DP pin	0.5	0.6	0.7	V
DM Sink Current	I_{DM_SNK}	DM pin	50	100	150	μA
DP Voltage Source On Time	t_{VDPSRC_ON}	DP pin	40	60	80	ms
Pull-down Detect Threshold	V_{DAT_REF}		0.25	0.325	0.4	V
DM Force Detect Voltage	V_{DM_SRC}	DM pin	0.5	0.6	0.7	V
DP Sink Current	I_{DP_SNK}	DP pin	50	100	150	μA
DM Voltage Source On Time	t_{VDMSRC_ON}	DM pin	40	60	80	ms
UFCS (DP and DM Pins)						
High Level Input Voltage	V_{IH_DP}	DP pin	2.31	3.3	3.6	V
Low Level Input Voltage	V_{IL_DP}	DP pin	-0.3		0.54	V
High Level Output Voltage	V_{OH_DM}	DM pin, source 0.5mA, V_{VUSB} ≥ 3.3V	1.44	3.3	3.6	V
Low Level Output Voltage	V_{OL_DM}	DM pin, sink 0.5mA			0.5	V
High Level Output Rise Time (1)	t_{RISE}	DM pin, from 20% to 80%, C_L = 200pF			1	μs
Low Level Output Fall Time (1)	t_{FALL}	DM pin, from 80% to 20%, C_L = 200pF			1	μs

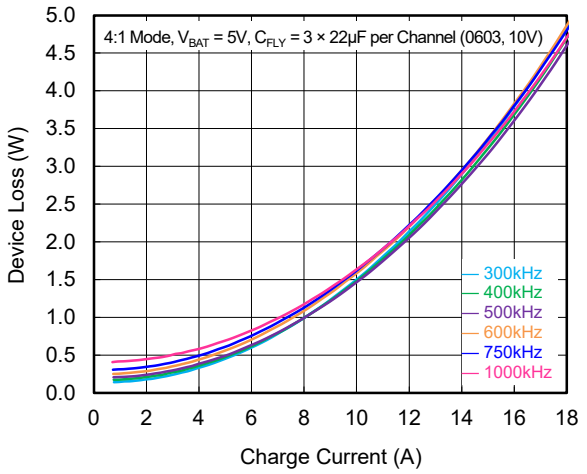
NOTE: 1. Guaranteed by design.

TYPICAL PERFORMANCE CHARACTERISTICS

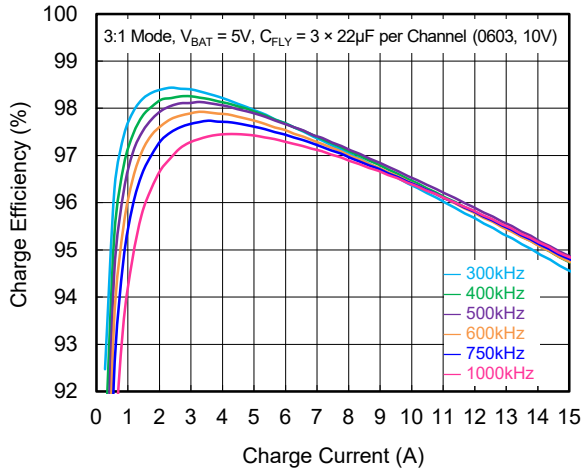
Charge Efficiency vs. Charge Current



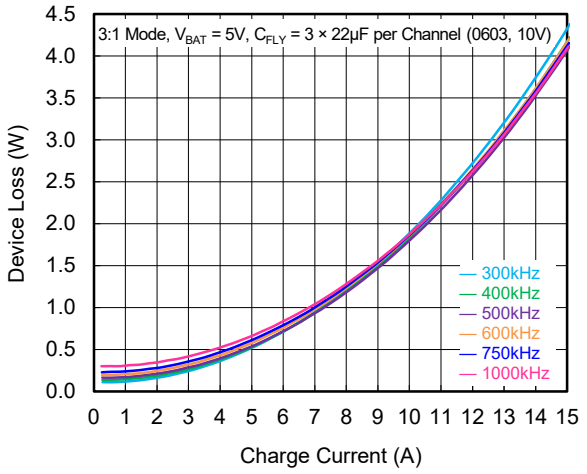
Device Loss vs. Charge Current



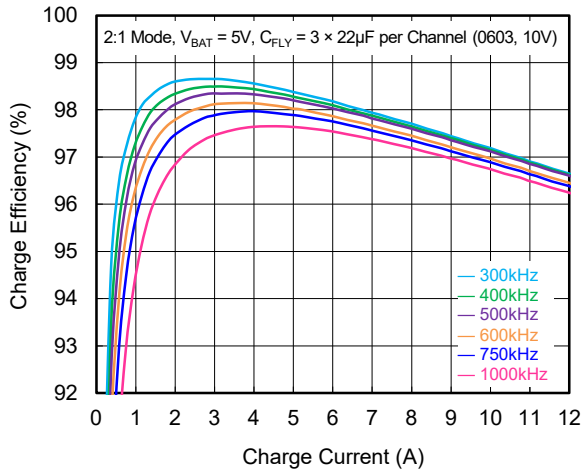
Charge Efficiency vs. Charge Current



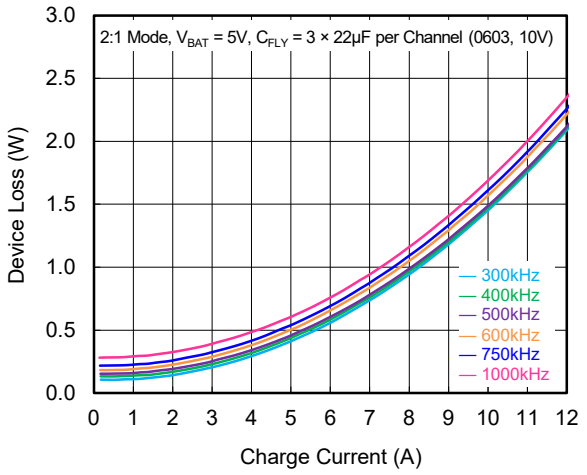
Device Loss vs. Charge Current



Charge Efficiency vs. Charge Current

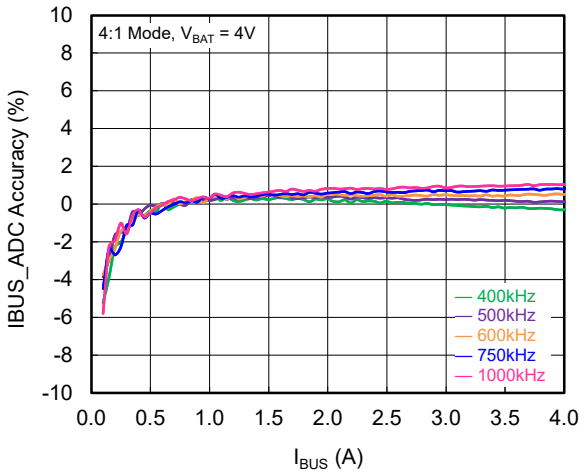


Device Loss vs. Charge Current

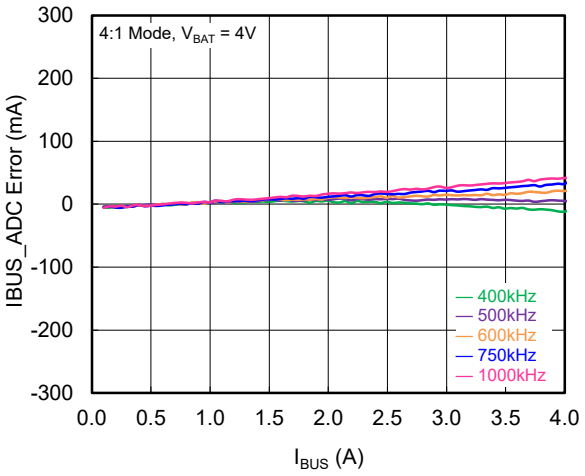


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

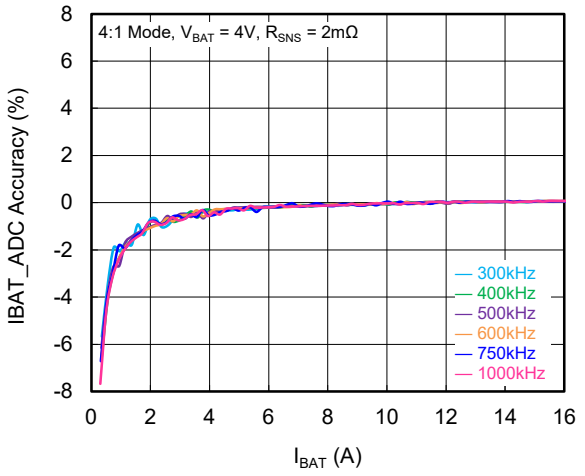
IBUS_ADC Accuracy vs. BUS Current



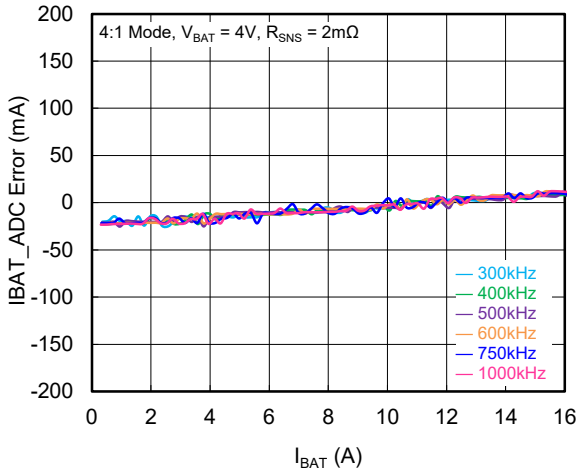
IBUS_ADC Error vs. BUS Current



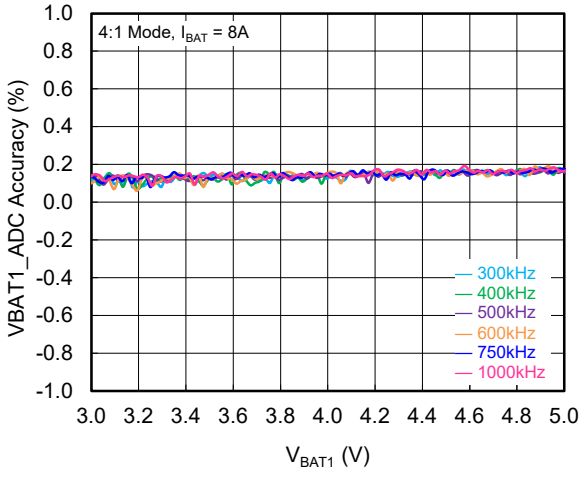
IBAT_ADC Accuracy vs. BAT Current



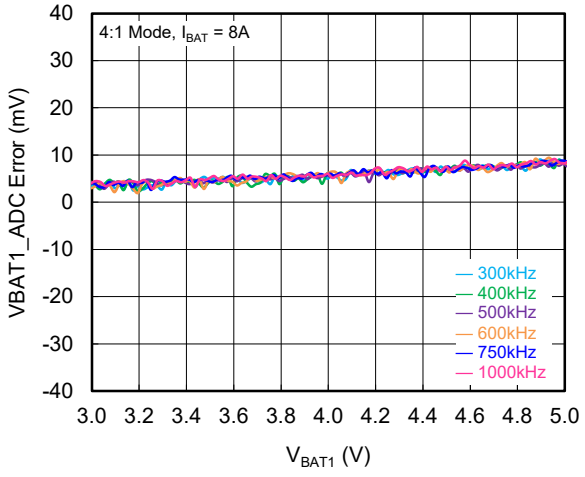
IBAT_ADC Error vs. BAT Current



VBAT1_ADC Accuracy vs. VBAT1 Voltage

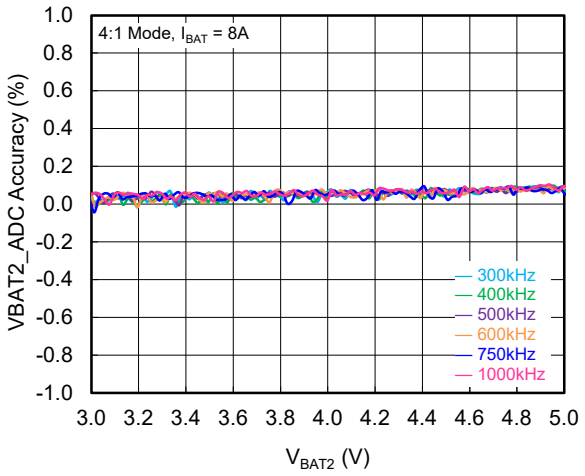


VBAT1_ADC Error vs. VBAT1 Voltage

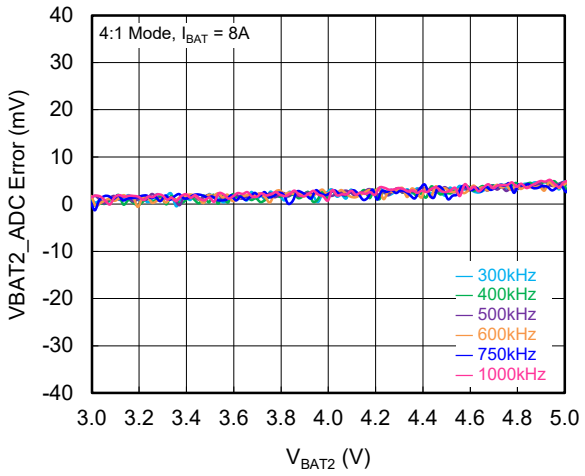


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

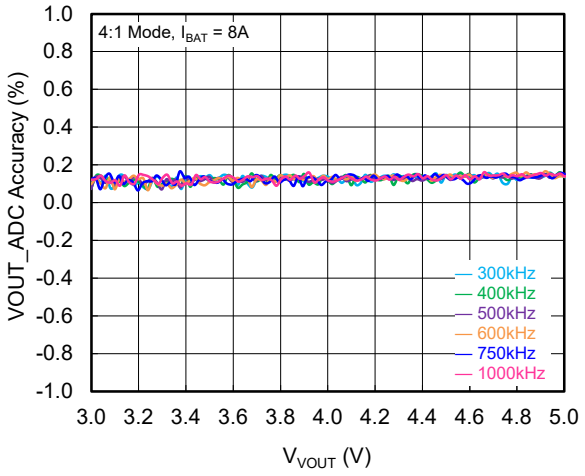
VBAT2_ADC Accuracy vs. VBAT2 Voltage



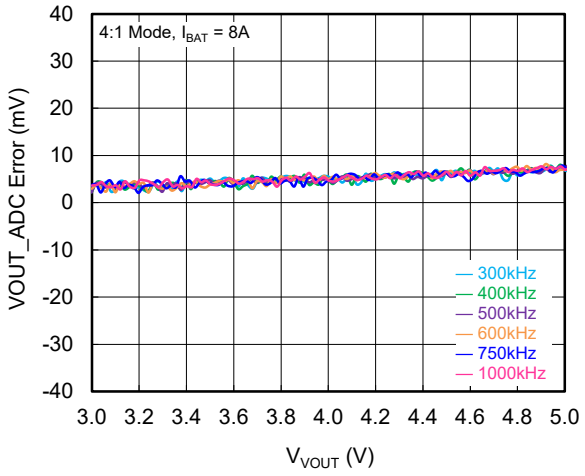
VBAT2_ADC Error vs. VBAT2 Voltage



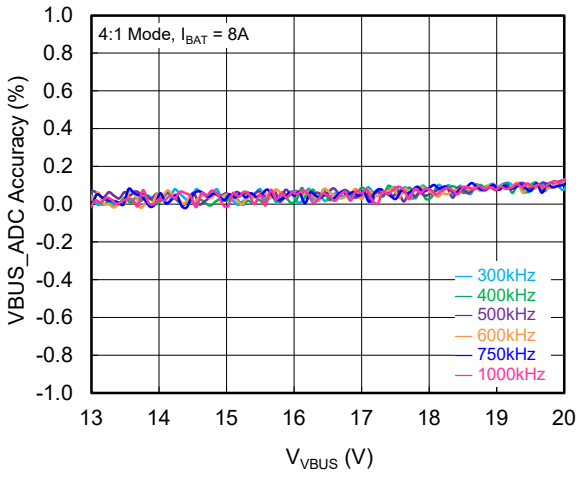
VOUT_ADC Accuracy vs. VOUT Voltage



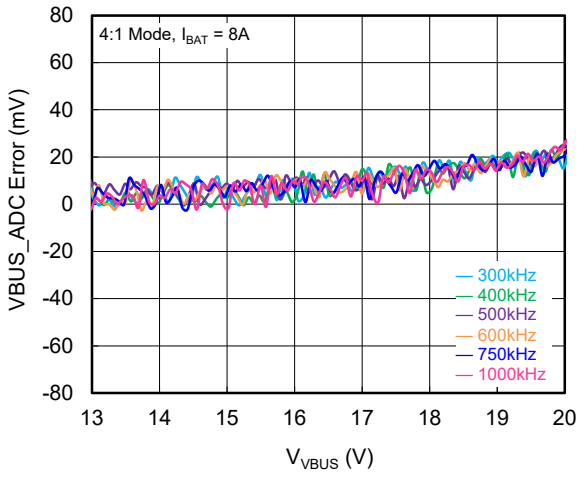
VOUT_ADC Error vs. VOUT Voltage



VBUS_ADC Accuracy vs. VBUS Voltage

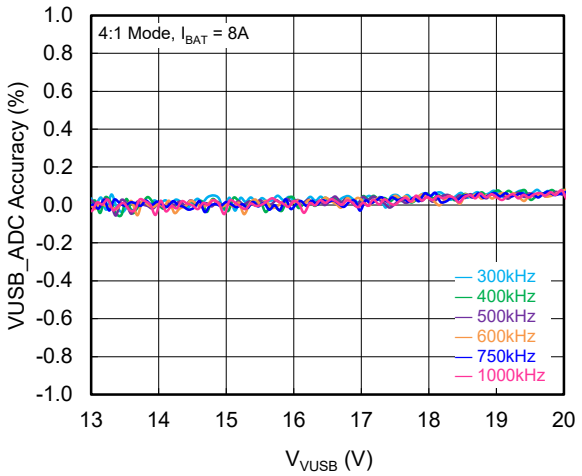


VBUS_ADC Error vs. VBUS Voltage

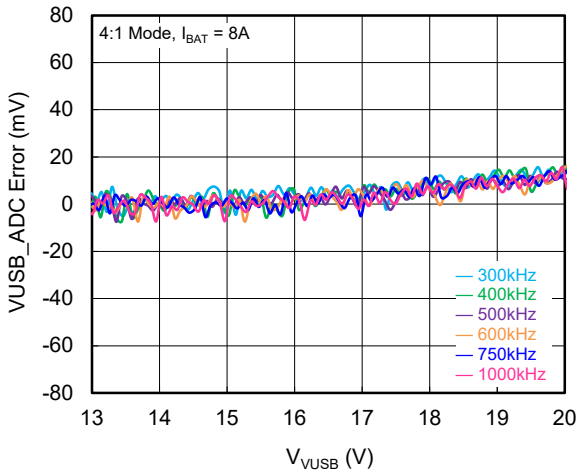


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

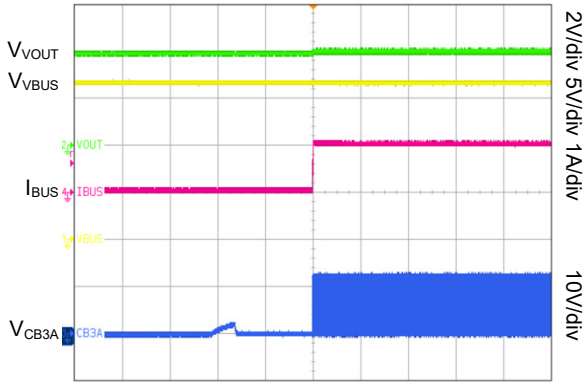
VUSB_ADC Accuracy vs. VUSB Voltage



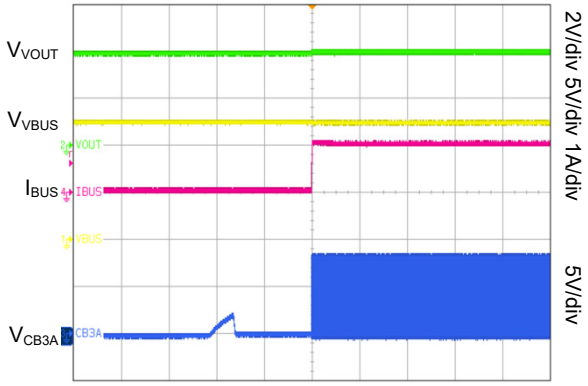
VUSB_ADC Error vs. VUSB Voltage



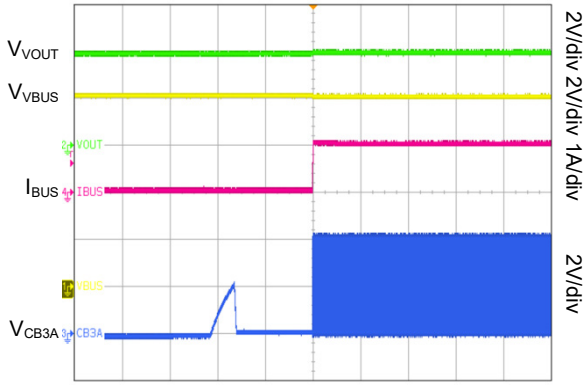
Forward 4:1 Charger Mode Power Up



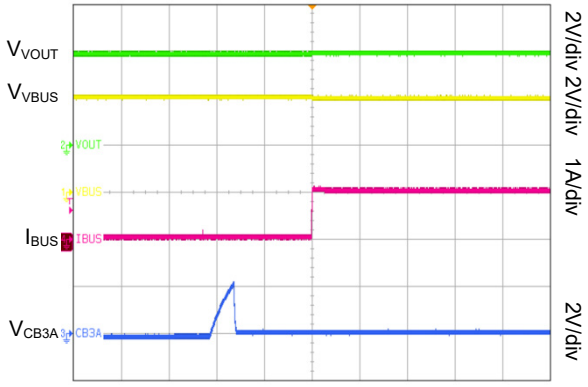
Forward 3:1 Charger Mode Power Up



Forward 2:1 Charger Mode Power Up

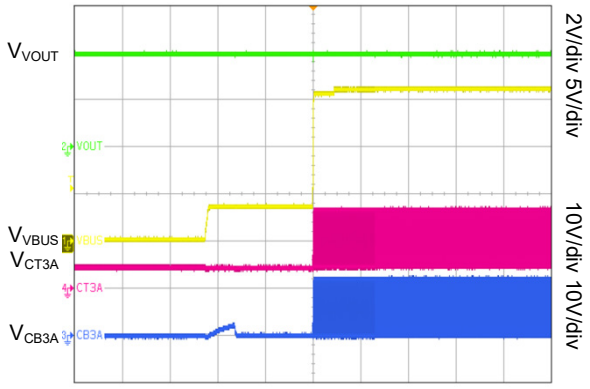


Forward 1:1 Charger Mode Power Up

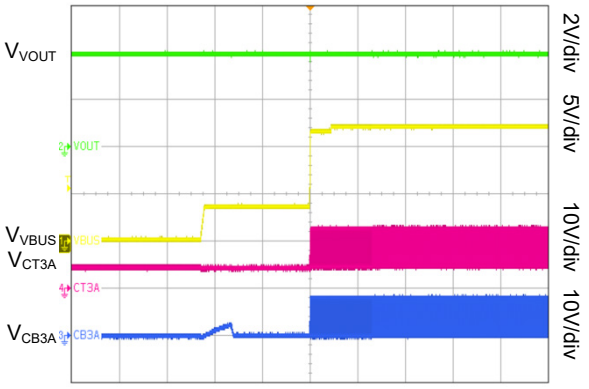


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

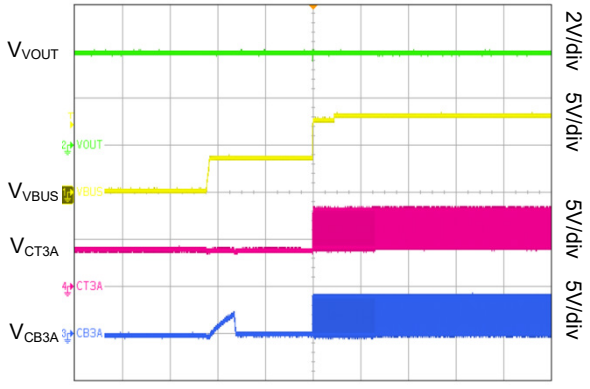
Reverse 1:4 Converter Mode Power Up



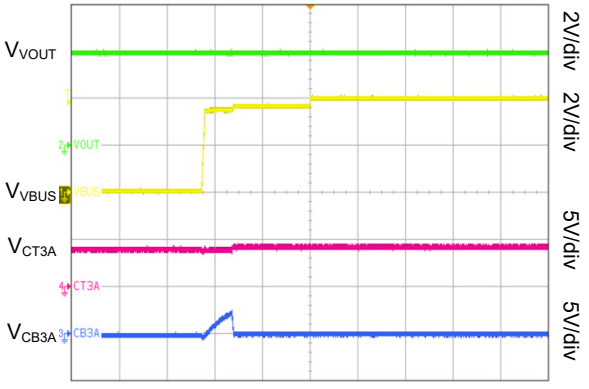
Reverse 1:3 Converter Mode Power Up



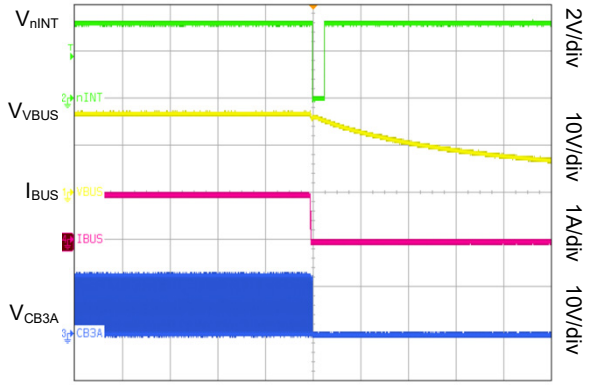
Reverse 1:2 Converter Mode Power Up



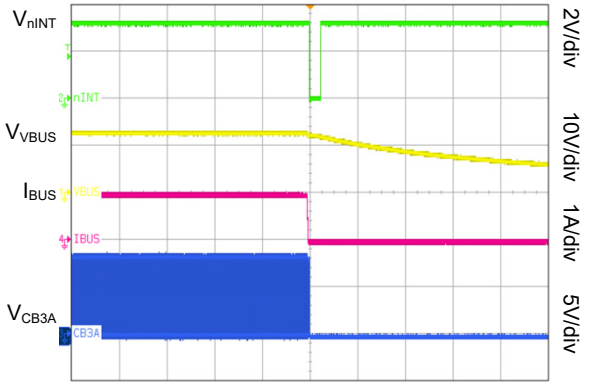
Reverse 1:1 Converter Mode Power Up



Adapter Unplug in Forward 4:1 Charger Mode

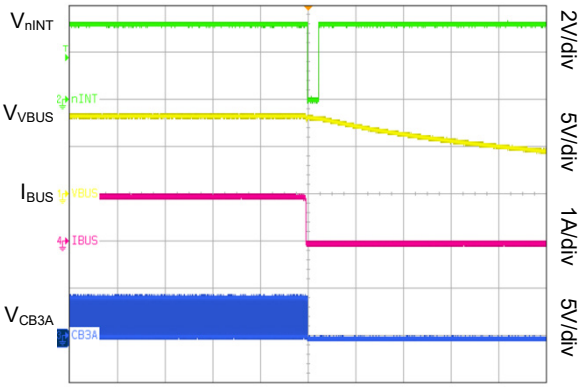


Adapter Unplug in Forward 3:1 Charger Mode



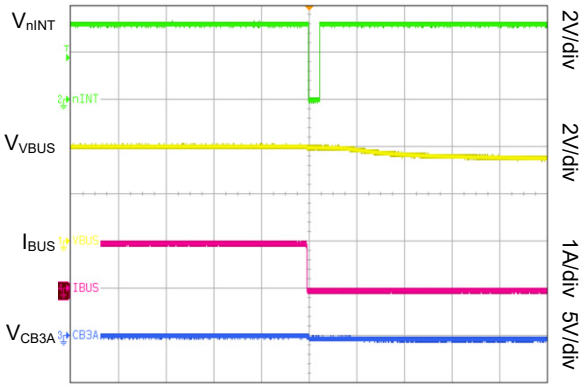
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Adapter Unplug in Forward 2:1 Charger Mode



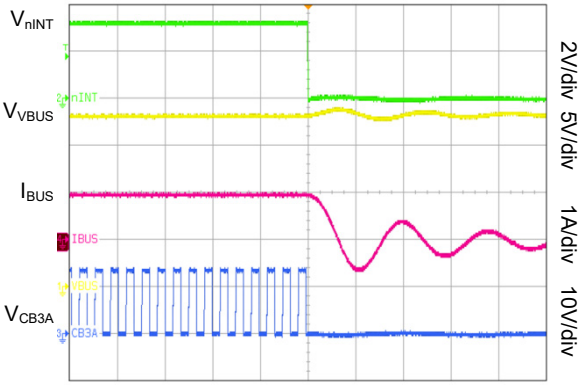
Time (1ms/div)

Adapter Unplug in Forward 1:1 Charger Mode



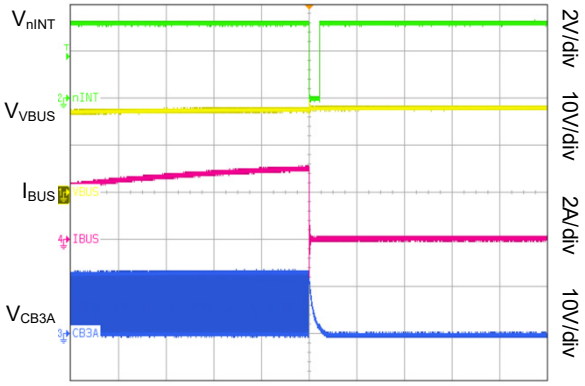
Time (1ms/div)

VBUS_OVP in Forward 4:1 Charger Mode



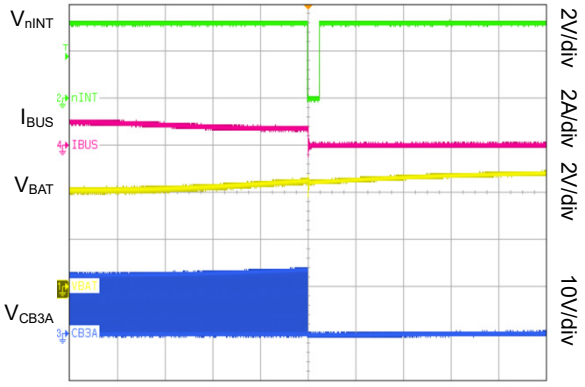
Time (5μs/div)

IBUS_OCP in Forward 4:1 Charger Mode



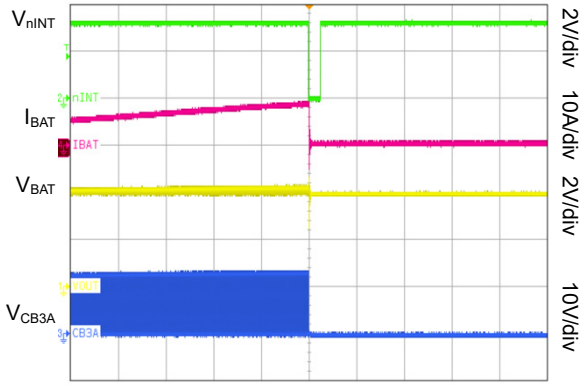
Time (1ms/div)

VBAT_OVP in Forward 4:1 Charger Mode



Time (1ms/div)

IBAT_OCP in Forward 4:1 Charger Mode



Time (1ms/div)

FUNCTIONAL BLOCK DIAGRAM

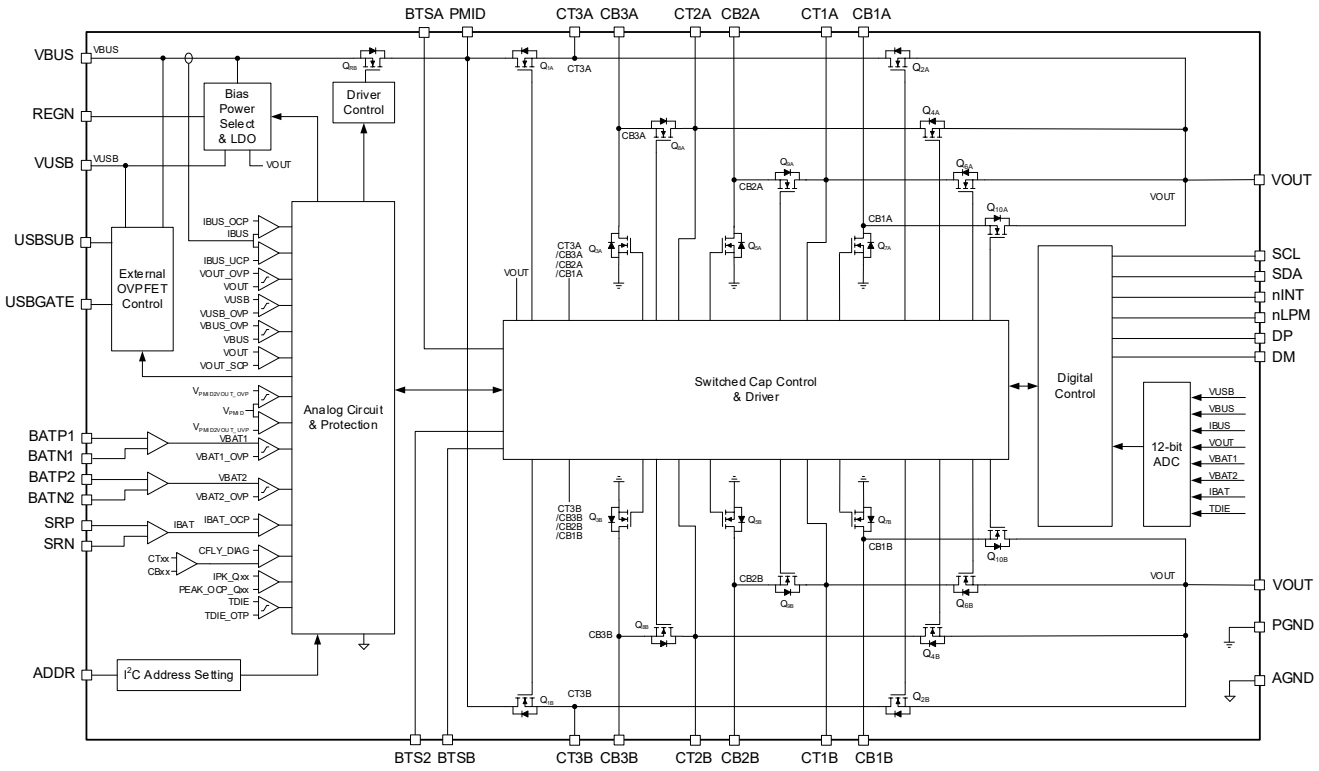


Figure 4. Functional Block Diagram

DETAILED DESCRIPTION

The SGM41612YGA is an efficient 18A battery charger that can operate in 8 different modes (forward 4:1/3:1/2:1/1:1 step-down charging modes and reverse 1:4/1:3/1:2/1:1 step-up discharging modes). A two-channel switched-capacitor core is integrated in the device to minimize the ripples and improve efficiency. Two power paths control, a reverse blocking NFET and all other necessary protection features for safe charging are included. A high speed 12-bit ADC converter is also included to provide bus voltage, bus current, battery voltage, battery current, and die temperature information for the charge management host via I²C serial interface.

Forward 4:1 Mode & Reverse 1:4 Mode

In forward 4:1 mode, ignoring small energy loss in each switching period in steady state operation, the SGM41612YGA generates a VOUT voltage of $V_{PMID}/4$ and is capable of supplying up to 18A output current. In reverse 1:4 operation, it generates a PMID voltage of $4V_{VOUT}$. Each channel of the 180° interleaved switched-capacitor charger operates with a fixed 50% duty cycle and reduces the ripple on the output voltage and current. The simplified single channel 4:1/1:4 switched-capacitor charger is shown in Figure 5.

Selecting high quality C_{FLY} capacitors and proper switching frequency are the key factors for a well performing capacitor voltage divider. Switching frequency selection is a trade-off between efficiency and capacitor size. An optimum switching frequency can be found for any selected C_{FLY} capacitor to minimize losses.

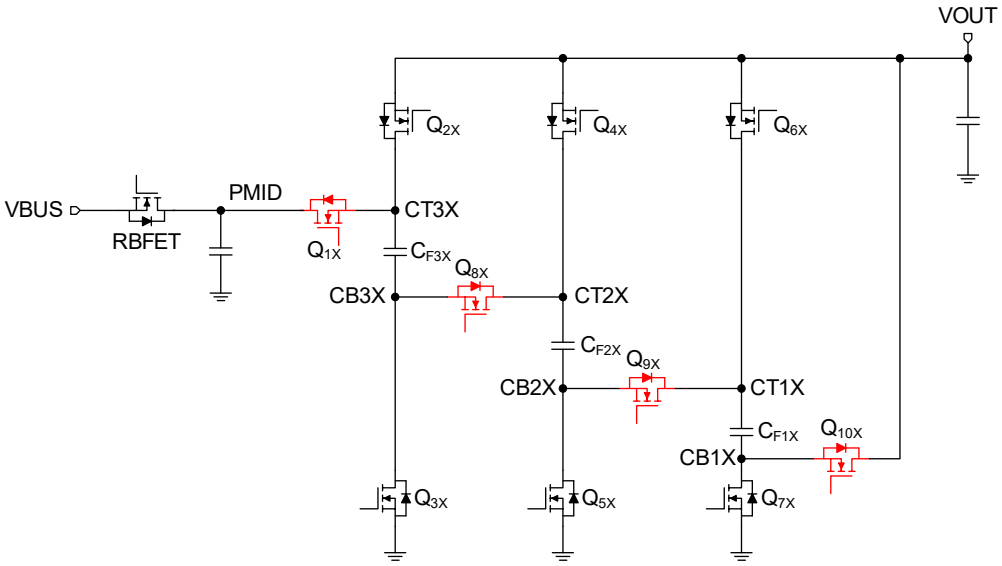


Figure 5. Power Stage of Single Channel 4:1/1:4 Switched-Capacitor Charger

DETAILED DESCRIPTION (continued)

Forward 3:1 Mode & Reverse 1:3 Mode

The SGM41612YGA can be configured to operate in forward 3:1 mode or in reverse 1:3 mode, where $Q_{6A}/Q_{6B}/Q_{7A}/Q_{7B}$ are always on, Q_{10A}/Q_{10B} are always off. It generates a VOUT voltage of $V_{PMID}/3$ and is capable of supplying up to 14A output current. In reverse 1:3 operation, it generates a PMID voltage of $3V_{VOUT}$. Each channel of the 180° interleaved switched-capacitor charger operates with a fixed 50% duty cycle and reduces the ripple on the output voltage and current. The simplified single channel 3:1/1:3 switched-capacitor charger is shown in Figure 6.

Forward 2:1 Mode & Reverse 1:2 Mode

The SGM41612YGA can be configured to operate in forward 2:1 mode or in reverse 1:2 mode, where $Q_{5A}/Q_{5B}/Q_{9A}/Q_{9B}$ are always off and Q_{4A}/Q_{4B} are always on. It generates a VOUT voltage of $V_{PMID}/2$ and is capable of supplying up to 12A output current. In reverse 1:2 operation, it generates a PMID voltage of $2V_{VOUT}$. Each channel of the 180° interleaved switched-capacitor charger operates with a fixed 50% duty cycle and reduces the ripple on the output voltage and current. The simplified single channel 2:1/1:2 switched-capacitor charger is shown in Figure 7.

The SGM41612YGA supports startup with a 3A load in reverse 1:2 mode when R1T2_SWL_CTRL = 1 and V_{VBUS} = 5V.

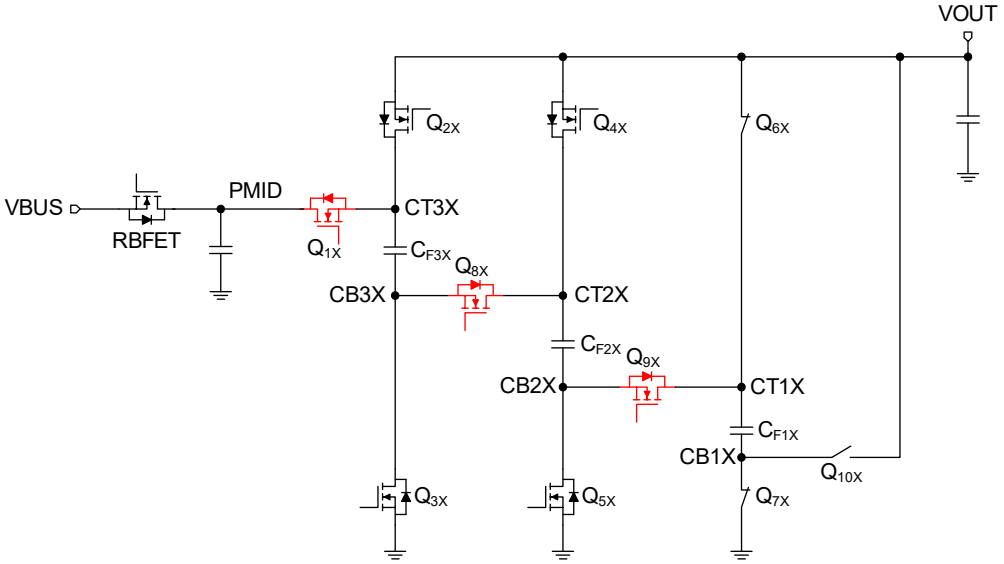


Figure 6. Power Stage of Single Channel 3:1/1:3 Switched-Capacitor Charger

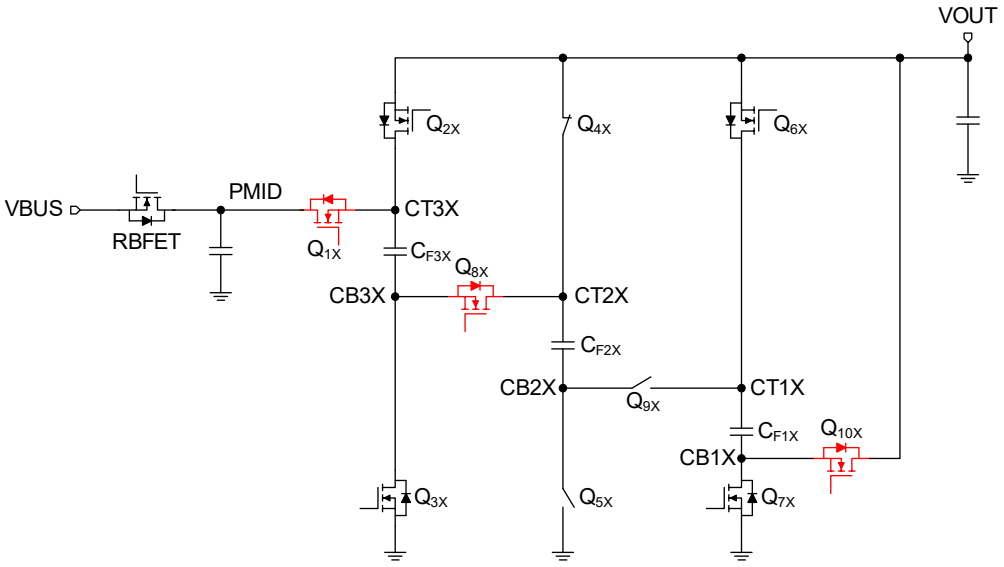


Figure 7. Power Stage of Single Channel 2:1/1:2 Switched-Capacitor Charger

DETAILED DESCRIPTION (continued)

Forward 1:1 Mode & Reverse 1:1 Mode

The SGM41612YGA is designed to operate in bidirectional bypass mode when V_{VBUS} is close to the V_{VOUT}. Here, $Q_{1A}/Q_{1B}/Q_{2A}/Q_{2B}/Q_{3A}/Q_{3B}/Q_{4A}/Q_{4B}/Q_{5A}/Q_{5B}/Q_{6A}/Q_{6B}/Q_{7A}/Q_{7B}$ are always on and $Q_{8A}/Q_{8B}/Q_{9A}/Q_{9B}/Q_{10A}/Q_{10B}$ are always off. With proper settings, the device enters bypass mode, all switches between VBUS and VOUT are fully turned on. When V_{BUS} is near V_{VOUT}, the bypass mode offers the best efficiency and the device is capable of sourcing up to 5A. The simplified single channel bypass mode switched-capacitor charger is shown in Figure 8.

The output voltage is close to the input minus a voltage drop caused by the on-resistances of the RBFET plus the four high-side switches of the two channels in parallel:

$$R_{EFF}\ (\text{Bypass mode}) \approx R_{DS_QRB} + (R_{DS_Q1A} + R_{DS_Q2A}) \,||\, (R_{DS_Q1B} + R_{DS_Q2B})$$

where R_{DS_QXX} is the on-resistance of the switch Q_{XX}.

Charge System

The SGM41612YGA is a slave charger device and needs a host. The host must set up all protection functions and disable the main charger before enabling the SGM41612YGA. The host must monitor the nINT interrupts especially during high current charging. It must also communicate with the wall adapter to control the charge current.

Figure 9 shows the block diagram of a charge system using the SGM41612YGA along with other devices. In this system, the SGM41612YGA can be used to detect the adapter by BC1.2 and the PD controller is used to communicate with adapter by PD protocol. When the smart wall adapter is detected, the AP unit controls the switching charger (SGM41516) that powers the load system and the switched capacitor charger (SGM41612YGA) that provides high current charging. The communication between those devices is through I²C interface.

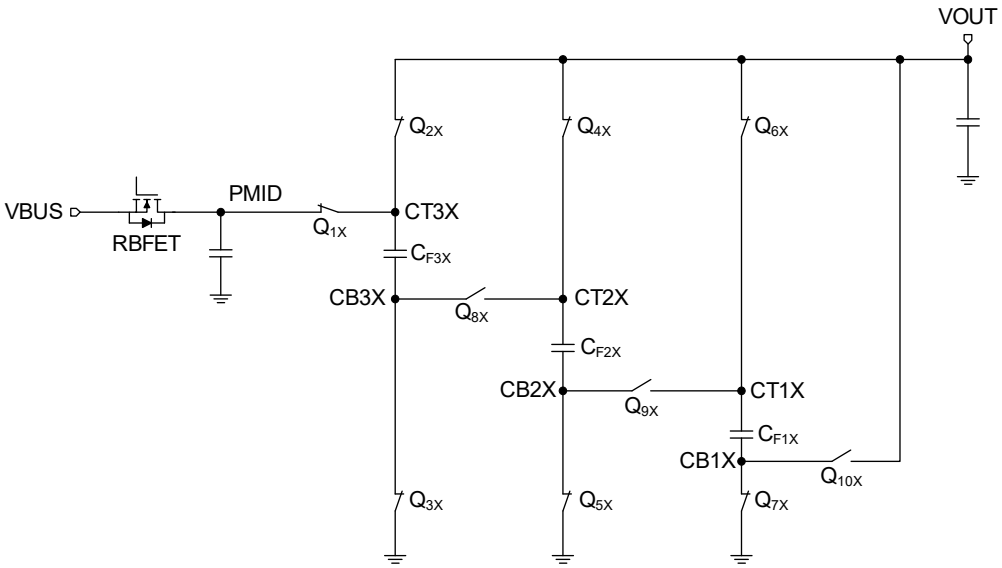


Figure 8. Power Stage of Single Channel 1:1 Switched-Capacitor Charger

DETAILED DESCRIPTION (continued)

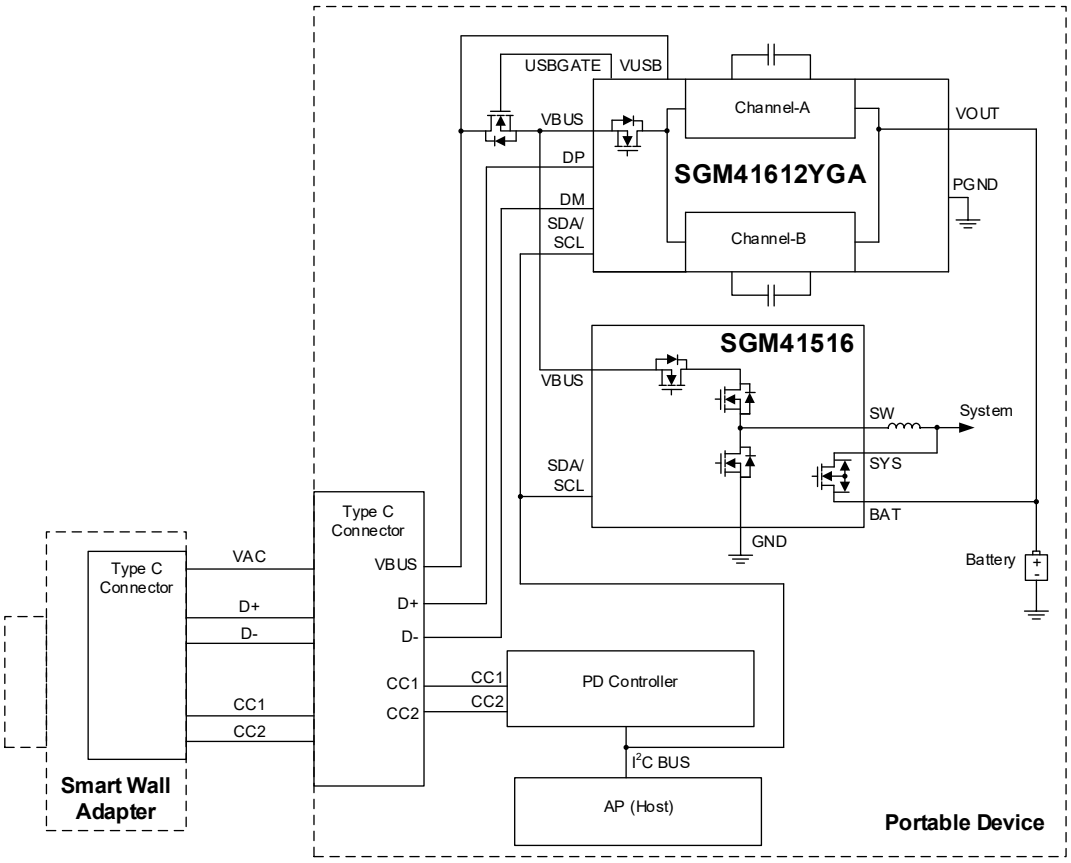


Figure 9. Simplified Charge System

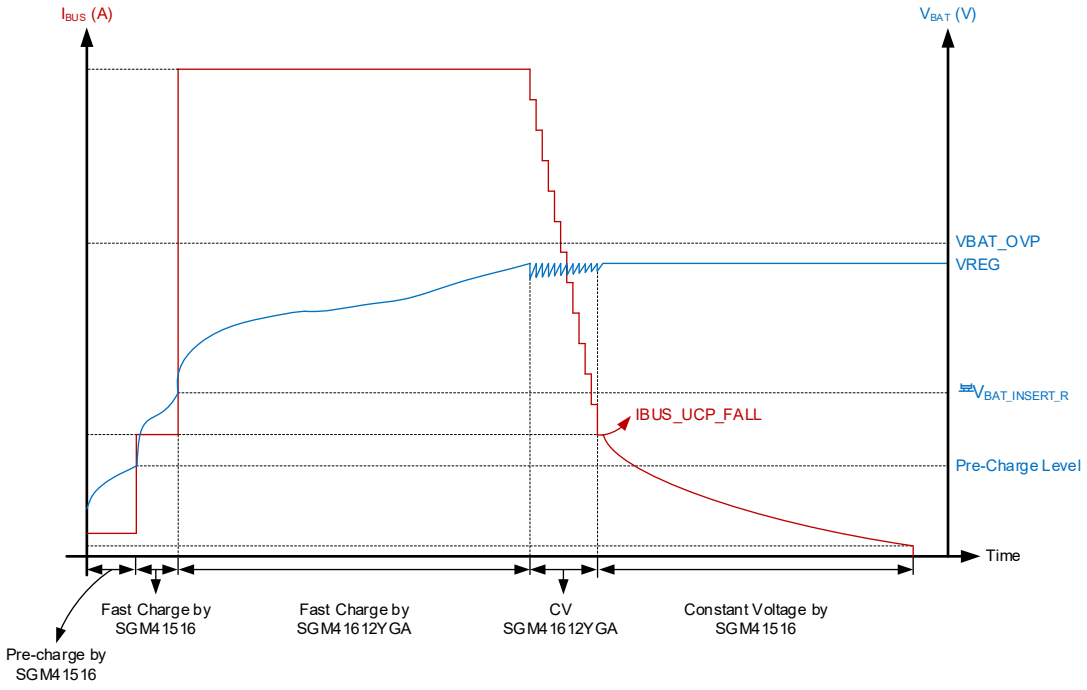


Figure 10. SGM41612YGA System Charging Profile

DETAILED DESCRIPTION (continued)

A typical charge profile for a high-capacity battery using switching charger and switched capacitor charger together is shown in Figure 10. During the trickle charge and pre-charge, the charging is controlled by the switching charger. Once the battery voltage reaches $V_{BAT_INSERT_R}$, the adapter can negotiate for a higher bus voltage and enable the SGM41612YGA for charging (4:1, 3:1, 2:1 or 1:1 mode). Once the battery voltage approaches the constant charging voltage point (VREG), the SGM41612YGA will notify the AP to reduce the IBUS current, and the AP will negotiate with adapter for a lower bus voltage to effectively taper the current until a point where the IBUS current ramps down below $I_{BUS_UCP_F}$.

Startup Sequence in Forward Charge Mode

The SGM41612YGA is powered from the greater of VUSB, VBUS or VOUT. When V_{VOUT} rises above $V_{VOUT_UVLO_R}$ and the nLPM pin is connected to high, or V_{VUSB}/V_{VBUS} rises above its UVLO rising threshold, the I²C interface is ready for communication and all the registers are reset to default values.

The device does not start charging after powered up, because by default the charger is disabled but the ADC can be enabled and the AP can read the system parameters before enabling charge. The charge can be enabled only if V_{VBUS} > $V_{BUS_PRESENT_R}$ and V_{VOUT} > $V_{BAT_INSERT_R}$.

Startup Sequence in Reverse Converter Mode

When only battery is present, the SGM41612YGA can work in reverse converter mode, and provide the power input to wireless transmitter circuit. If the V_{VOUT} > $V_{BAT_BRN_IN}$ and reverse mode setting is set properly, device turn on RBFET firstly, and then start the reverse mode soft-start by controlling the MOSFET, a controlled current will charge the PMID until V_{PMID} > n × (V_{VOUT} - 100mV) (n = 1, 2, 3, 4, depending on the operation mode). During startup stage, any fault such as VBUS short, reverse mode soft-start timeout can reset the SCC_EN bit and set the corresponding flag bit to 1.

Device Power up from Battery without Input Source

To reduce the quiescent current and maximize the battery run time when it is the only available source, low power mode can be set by pulling low the nLPM pin to achieve very small battery leakage. In low power mode, the REGN LDO and most of the sensing circuits are turned off, except VUSB_INSERT and VBUS_PRESENT functions. The SGM41612YGA exits low power mode when nLPM pin is pulled high or V_{VUSB}/V_{VBUS} rises above its UVLO rising threshold.

Device Power up from Input Source

When an input source is plugged-in and the conditions of V_{VBUS} > $V_{BUS_PRESENT_R}$ and V_{VOUT} > $V_{BAT_INSERT_R}$ are valid, the AP must initialize all protections to the desired thresholds before enabling charge. The protection thresholds that need to be set are VUSB_OVP, PMID2VOUT_OVP, PMID2VOUT_UVP, VBUS_OVP, IBUS_OCP, IBUS_UCP, VOUT_OVP, VBAT_OVP, IBAT_OCP, and TDIE_OTP. If one of the protection trigger conditions is met, the charger stops switching. It will also be turned off the corresponding external OVPFETs Q_{USB} when VUSB_OVP or VBUS_SCP event occurs.

After setting protections, the VBUS voltage is checked to be between V_{BUS_LO} and V_{BUS_HI} to allow forward charge mode operation. Charging is enabled and current flows into the battery when the AP sets forward mode by writing the corresponding bits in the SCC_MODE[2:0] bits. Then raising the VBUS voltage will increase the battery charge current. When the converter is on, any command to change the charge mode is ignored. To do so, the charging must be disabled first, and then the charge mode can be changed by I²C serial interface.

DETAILED DESCRIPTION (continued)

Input Power Path Management

The SGM41612YGA has the USBGATE pin to drive the back-to-back N-channel FETs or GaN FET. Once the battery voltage, VUSB or VBUS voltage is over the UVLO threshold, POR occurs, the device will check whether the USBGATE is shorted to ground for one time. If the USBGATE is shorted to ground, then the USBGATE function is disabled and update the USBGATE_CONFIG_STAT bit to 0; On the contrary, the USBGATE function is enabled and update the USBGATE_ CONFIG_STAT bit to 1.

Furthermore, the USBGATE drive capability can be programmed by USBGATE_SRC_CURR[1:0] for supporting the GaN FET with high gate to source/drain leakage current. Once USBGATE start to turn on the OVPFET, a soft-start timer (set by OVPFET_SS_TMO bit, 10ms by default) is initiated too. If the V_{VBUS} is less than 95% of the V_{VUSB} in forward mode (or V_{VUSB} is less than 95% of the V_{VBUS} in reverse mode) after timeout, the OVPFET_SS_TMO_FLAG bit is set to 1, and an INT pulse is asserted, USBGATE will turn off OVPFET immediately and try to turn on it after 512ms delay.

For forward charging operation (Adaptor power the mobile device through USB port), USBGATE can operate in two modes: auto-mode and manual mode. In reverse mode (mobile device power to the USB port), OVPFET can only operate in manual mode. The table below summarizes the turn-on and turn-off conditions for USBGATE control.

Table 1. USBGATE Configuration

Operation Mode	USBGATE Turn-on Conditions	USBGATE Turn-off Conditions
Forward	V_{VUSB} > $V_{USB_INSERT_R}$ and V_{VUSB} < $V_{USB_OVP_F}$ and {USBGATE_MODE = 0 or (USBGATE_MODE = 1 and USBGATE_EN = 1) } and V_{VBUS} < $V_{BUS_PRESENT_F}$ before turn-on action	V_{VUSB} < $V_{USB_INSERT_F}$ or V_{VUSB} > $V_{USB_OVP_R}$ or (USBGATE_MODE = 1 and USBGATE_EN = 0) or V_{VBUS} > $V_{BUS_PRESENT_R}$ before turn-on action
Reverse	V_{VBUS} > $V_{BUS_PRESENT_R}$ and {USBGATE_MODE = 1 and USBGATE_EN = 1} and V_{VUSB} < $V_{USB_INSERT_F}$ before turn-on action	V_{VBUS} < $V_{BUS_PRESENT_F}$ or V_{VUSB} > $V_{USB_OVP_R}$ or {(USBGATE_MODE = 1 and USBGATE_EN = 0) or USBGATE_MODE = 0} or V_{VUSB} > $V_{USB_INSERT_R}$ before turn-on action

Forward Auto-Mode

For the OVPFET forward operation, USBGATE can operates in auto-mode by setting USBGATE_MODE to 0. In this mode, USBGATE is automatically turned on and off according to the conditions as shown in Table 1. Once the VUSB input source is inserted, only when the VUSB voltage is in the valid range (exceeds V_{USB_INSERT} and lower than V_{USB_OVP} thresholds) and VBUS voltage is lower than $V_{BUS_PRESENT_F}$, the USBGATE will be turned on after $t_{USBGATE_ON_DEG}$ deglitch time. When VUSB is outside of the valid range, USBGATE will be automatically turned off.

Manual Mode

For the OVPFET forward operation, USBGATE can operates in manual-mode by setting USBGATE_MODE to 1. In this mode, when the VUSB voltage is in the valid range (exceeds V_{USB_INSERT} and lower than V_{USB_OVP} threshold) and VBUS voltage is lower than $V_{BUS_PRESENT_F}$, the USBGATE will turn on the OVPFET after $t_{USBGATE_ON_DEG}$ deglitch time. If VUSB OVP occurs, USBGATE will be turned off immediately.

For the OVPFET reverse operation, USBGATE can only operates in manual-mode by setting USBGATE_MODE to 1. In this mode, if the USBGATE_EN bit are equal to 1, the USBGATE will turned on the OVPFET when VBUS is present and VUSB voltage is lower than $V_{USB_INSERT_F}$. If VUSB OVP occurs, USBGATE will be turned off immediately.

I²C Address Setting

The ADDR pin is used to set the default I²C address during the POR procedure. Connect ADDR pin directly to AGND to select address 0x67. Leave ADDR pin floating to select address 0x68. Changes are not allowed after the startup procedure.

ADC

The SGM41612YGA integrates a fast 8-channel, 12-bit ADC converter to monitor input/output currents and voltages and the temperature of the device. The ADC is controlled by the ADC_CTRLx registers. Setting the ADC_EN bit to 1 enables the ADC. This bit can be used to turn off the ADC and save power when it is not needed. The ADC_RATE bit allows choosing continuous conversion or 1-shot conversion mode. The ADC operates independent of the faults, unless the AP sets the ADC_EN bit to 0.

The ADC can operate if V_{VUSB} > $V_{USB_INSERT_R}$ or V_{VBUS} > $V_{BUS_PRESENT_R}$ or V_{VOUT} > $V_{BAT_INSERT_R}$ condition is valid. Otherwise the ADC conversion is postponed until one of them is satisfied. The ADC readings are valid only for DC values and not for transients.

DETAILED DESCRIPTION (continued)

By default, all ADC channels are converted in continuous conversion mode except the channels disabled by the ADC_CTRLx registers. If the 1-shot conversion mode is selected, the ADC_DONE_FLAG bit is set to 1 when all channels are converted, then the ADC_EN bit is reset to 0. In the continuous conversion mode, the ADC_DONE_FLAG bit is set to 0.

nINT Pin, flag and Mask Bits

The nINT pin is an open-drain output and must be pulled up to a logic high rail. It is pulled low with a duration of t_{INT} to notify the AP when it is triggered by an event. See the register map for all event flag bit and control bits.

When an event occurs, a nINT signal is sent to the AP and the corresponding flag bit is set to 1. The flag bit can be read and some of them can be reset only after the fault is cleared. The nINT signal is not re-sent if an event is still present after the flag bit is read, unless another kind of event occurs. If an event mask bit is set, that event will not send nINT signal, but the flag bit is still updated independent of the mask bit.

The INT pulse generation behavior examples are shown in Figure 11.

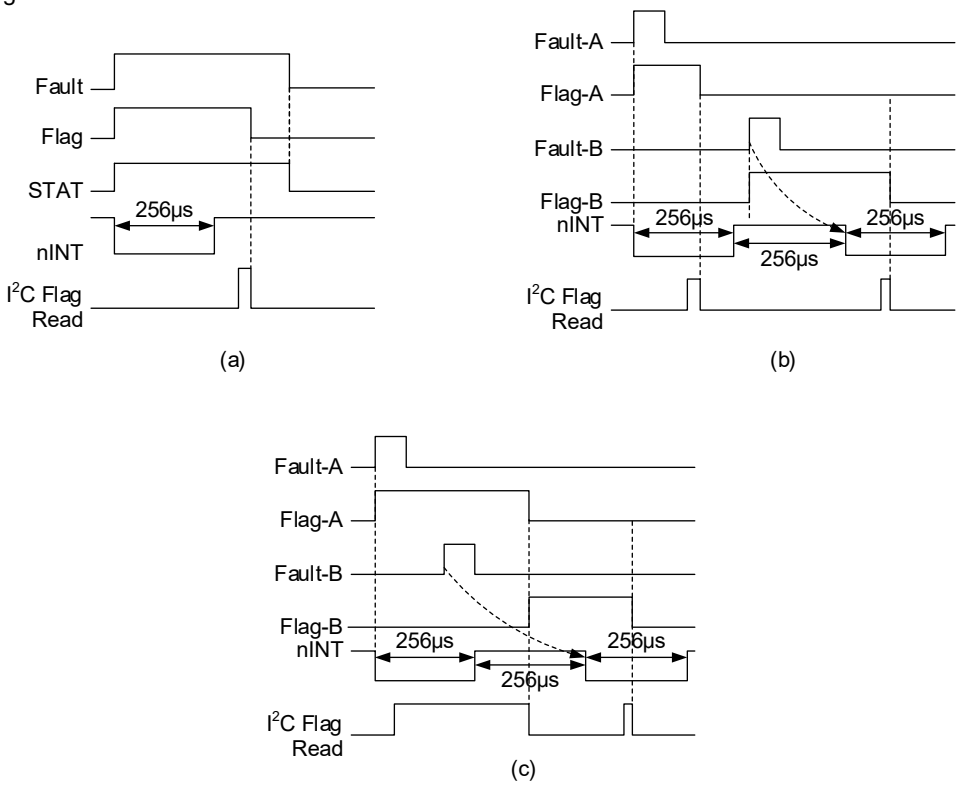


Figure 11. nINT Pulse Generation Behavior Examples

DETAILED DESCRIPTION (continued)

Input Over-Voltage Protection (VUSB_OVP)

The SGM41612YGA monitors the adapter voltage on the VUSB pin to use the USBGATE output to control the external OVPFETs Q_{USB} respectively. Taking VUSB_OVP as an example, the VUSB over-voltage protection circuit is powered by VUSB and is enabled if V_{VUSB} rises above $V_{USB_INSERT_R}$. If V_{VUSB} is above $V_{USB_INSERT_R}$ for at least $t_{USBGATE_ON_DEG}$ time, when USBGATE_MODE bit is set to forward auto-mode, the USBGATE will output drive signal to turn on the external OVPFET Q_{USB}. If the V_{VUSB} reaches the $V_{USB_OVP_R}$ threshold, the gate voltage starts to drop and eventually the OVPFET Q_{USB} is fully turned off. $t_{USB_OVP_RSM}$ (128ms) is deglitch time between V_{VUSB} falling below $V_{USB_OVP_F}$ and USBGATE restarting to turn on. Figure 12 shows the VUSB_OVP and USBGATE operation timings. The $V_{USB_OVP_R}$ threshold can be set by I²C serial interface. The adapter voltage must never exceed the absolute maximum rating of the VUSB pin and the external OVPFETs.

Input Short-Circuit Protection (VBUS_SCP)

The VBUS_SCP function monitors the VBUS pin for short-circuit. This function is enabled if the external OVPFETs are turned on or if V_{VBUS} rises above $V_{BUS_PRESENT_R}$. If the V_{VBUS} falls below 2.5V, the OVPFETs are turned off, and operation is stopped. SCC_EN bit is reset to 0 (disable). Also, VBUS_ABSENT_FLAG bit is set to 1, and an INT pulse is asserted. The device will wait for 512ms before automatically re-enabling and initiating startup sequence.

VBUS Charge Voltage Range (VBUS_LO & VBUS_HI)

The VBUS_LO and VBUS_HI functions are included to avoid problems due to wrong VBUS setting for forward charging. If V_{VBUS} is beyond the range between V_{BUS_LO} (= n × 0.99 × V_{VOUT}) and V_{BUS_HI} (= n × 1.15 × V_{VOUT}, n = 1, 2, 3, 4, depending on the operation mode), the device remains in charge initiation operation. Once V_{VBUS} is within the charge range, forward charging will start and VBUS_LO and VBUS_HI functions will be disabled.

Input, Output and Battery Over-Voltage Protection (VBUS_OVP, VOUT_OVP and VBATx_OVP)

The VBUS_OVP, VOUT_OVP and VBAT_OVP functions detect input and output voltage conditions. If either input or output voltage is higher than the protection threshold, the operation is stopped and the SCC_EN bit is reset to 0 (disable). The VBUS_OVP functions monitor VBUS pin voltage. The VOUT_OVP function monitors VOUT pin voltage. The VBATx_OVP uses BATPx and BATNx remote sense pins to monitor differential voltage between the battery terminals. To minimize the risk of battery terminal short in the manufacturing process, a 100Ω resistor needs to be connected in series to the BATPx and BATNx pin respectively. The VBUS_OVP, VOUT_OVP and VBATx_OVP thresholds can be set by I²C serial interface.

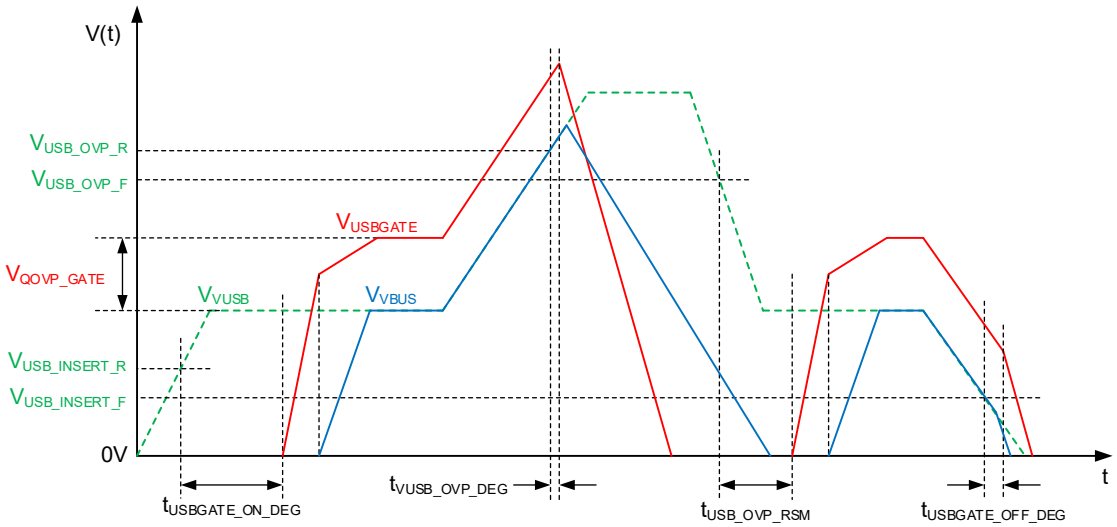


Figure 12. USBGATE Operation Timing

DETAILED DESCRIPTION (continued)

Bidirectional Bus and Battery Over-Current Protection (IBUS_OCP and IBAT_OCP)

The IBUS_OCP function monitors the bidirectional current via Q_{RB}. If SCC_EN bit is set to enable forward/reverse operation, the Q_{RB} is turned on and the IBUS_OCP function starts detecting the current. If the I_{BUS} reaches I_{BUS_OCP} threshold, the device stops operation and resets SCC_EN bit to 0 (disable). The bidirectional battery current is monitored by the voltage across an external series shunt resistor. This differential voltage is measured between SRP and SRN pins. If I_{BAT_OCP} threshold is reached, the device stops operation and resets SCC_EN bit to 0 (disable). The IBUS_OCP and IBAT_OCP thresholds can be set by I²C serial interface.

Input Under-Current Protection (IBUS_UCP)

The IBUS_UCP function detects the input current via Q_{RB} during forward charging. After charging is started, the $t_{IBUS_UCP_BLK}$ timer is enabled and I_{BUS} current is compared with $I_{BUS_UCP_R}$. If I_{BUS} cannot exceed $I_{BUS_UCP_R}$ within $t_{IBUS_UCP_BLK}$, the charging will be stopped and SCC_EN bit is reset to 0 (disable). If I_{BUS} exceeds $I_{BUS_UCP_R}$ when $t_{IBUS_UCP_BLK}$ times out, from then on, if I_{BUS} falls below the $I_{BUS_UCP_F}$ threshold, the charging will be stopped and SCC_EN bit is reset to 0 (disable). The $t_{IBUS_UCP_BLK}$ timer can be set by I²C serial interface.

PMID Charge Voltage Range (PMID2VOUT_UVP & PMID2VOUT_OVP)

The PMID2VOUT_UVP and PMID2VOUT_OVP functions are included to avoid problems caused by abnormal input or output transients during forward or reverse operation. If V_{PMID} is beyond the range between $V_{PMID2VOUT_UVP}$ and $V_{PMID2VOUT_OVP}$, the operation will be stopped and SCC_EN bit is reset to 0 (disable). The $V_{PMID2VOUT_UVP}$ and $V_{PMID2VOUT_OVP}$ thresholds can be set by I²C serial interface.

CFLY and Bootstrap Capacitor Diagnosis (PIN_DIAG)

The CFLY diagnosis function identifies the health of flying capacitors before and during forward or reverse operation. The device initialization process is started after SCC_EN bit is set to 1. When V_{VBUS}/V_{VOUT} is in the charge range, the flying capacitors in both channels are pre-charged. A C_{FLY}, C_{BTSA}, C_{BTSB}, C_{BTS2} open/short-circuit is detected if they cannot be charged. If so, the initialization process is stopped and SCC_EN bit is reset to 0 (disable). Even if CFLY capacitors pass the open/short-circuit test in the initialization process, the CFLY diagnosis function remains active and whenever a V_{CFXX} voltage falls, the operation is stopped and SCC_EN bit is reset to 0 (disable). The PIN_DIAG_FAIL_FLAG bit is set to 1 and an INT pulse is generated as well. During a CFLY short-circuit event, other protection events such as IBUS_OCP, VBAT_OVP or PEAK_OCP may occur.

A CFLY discharge circuit is activated before the flying capacitors are pre-charged to prevent over-current stress at the start of charging.

VOUT Short-Circuit Protection (VOUT_SCP)

The VOUT_SCP function monitors the VOUT pin for short-circuit. This function is enabled during forward or reverse operation. If V_{VOUT} falls below 2.6V, the operation is stopped and SCC_EN bit is reset to 0 (disable). Also, the VOUT_SCP_FLAG bit is set to 1, and an INT pulse is generated.

Bidirectional Converter Peak Over-Current Protection (PEAK_OCP)

The PEAK_OCP function monitors the converter switch operating currents. If the bidirectional Q_{1X}, Q_{3X}, Q_{5X}, Q_{7X} and Q_{10X} current reach switch peak OCP threshold during forward or reverse operation, the PEAK_OCP_FLAG bit is set to 1 and an INT pulse is generated, the operation is stopped and SCC_EN bit is reset to 0 (disable).

TDIE Over-Temperature Protection (TDIE_OTP)

The TDIE_OTP function prevents operation in over-temperature condition. The die temperature is monitored and if the $T_{DIE_OTP_R}$ threshold is reached, the operation is stopped and SCC_EN bit is reset to 0 (disable). The startup sequence cannot be initiated again until the die temperature falls down with a 20℃ hysteresis.

I²C REGISTER ADDRESS MAP

All registers are 8-bit and individual bits are named from D[0] (LSB) to D[7] (MSB).

The device I²C Address is determined by the state of ADDR pin in the POR sequence, as described in I²C Address Setting section.

FUNCTION	STAT	FLAG	MASK	THRESHOLD SETTING	ENABLE	DEGLITCH
REG_RST	--	--	--	--	0x0E[3]	--
SCC_MODE	0x0A[1]	--	--	0x0E[2:0]	0x0B[7]	--
WATCHDOG	--	0x13[4]	0x14[4]	0x0D[2:0]	0x0D[2:0]	--
FSW_SET	--	--	--	0x0C[7:3]	--	--
FSW_DITHER	--	--	--	0x0C[1]	0x0C[1]	--
USBGATE	0x10[7]	--	--	0x2B[3]	0x0B[4] & 0x0B[3]	0x0B[6:5]
VUSB_OVP	0x03[4]	0x03[5]	0x03[6]	0x03[3:0]	0x0F[2]	--
VUSB_REMOVE	0x10[0]	0x11[1]	0x12[1]	--	--	--
VUSB_INSERT	0x10[0]	0x11[0]	0x12[0]	--	--	--
VUSB_PDN	0x0A[6]	--	--	--	0x0B[1] & 0x0B[0]	--
VBUS_OVP	--	0x13[1]	0x14[1]	0x05[7:2]	0x0F[1]	--
VBUS_PRESENT	0x10[2]	0x11[2]	0x12[2]	--	--	--
VBUS_PDN	--	--	--	--	0x0B[2]	--
VBUS_ABSENT	0x10[2]	0x11[7]	0x12[7]	--	--	--
VBUS_LO	0x0A[4]	--	--	--	0x0D[7]	--
VBUS_HI	0x0A[3]	--	--	--	0x0D[7]	--
PMID2VOUT_UVP	--	0x09[3]	0x09[4]	0x09[2:0]	0x09[7]	0x09[5]
PMID2VOUT_OVP	--	0x08[3]	0x08[4]	0x08[2:0]	0x08[7]	0x08[5]
IBUS_OCP	--	0x06[5]	0x06[6]	0x06[4:0]	0x06[7]	0x2B[5]
IBUS_UCP_FALL	--	0x07[0]	0x07[1]	--	0x07[7]	0x07[5:4]
IBUS_UCP_RISE	--	0x07[2]	0x07[3]	--	--	--
IBUS_UCP_BLK_TMO	--	0x13[5]	0x14[5]	0x0D[5:3]	--	--
RVS_SS_OK	--	0x27[5]	0x28[5]	--	--	--
RVS_SS_FAIL	--	0x13[2]	0x14[2]	--	--	--
VOUT_OVP	--	0x13[0]	0x14[0]	0x05[1:0]	0x0F[0]	--
VOUT_SCP	--	0x27[3]	0x28[3]	--	--	--
VBAT_INSERT	0x10[4]	0x11[4]	0x12[4]	--	--	--
VBAT_OVP	--	0x01[5]	0x01[6]	VBAT1: 0x01[4:0]	0x01[7]	0x0E[6]
	--	0x04[5]	0x04[6]	VBAT2: 0x04[4:0]	0x04[7]	
IBAT_OCP	--	0x02[4]	0x02[5]	0x02[6] & 0x02[3:0]	0x02[7]	0x2A[5]
PEAK_OCP (Bidirectional)	--	0x13[3]	0x14[3]	--	0x0F[3]	0x29[7]
PIN_DIAG	--	0x0A[0]	--	--	--	--
TDIE_OTP	--	0x13[6]	0x14[6]	--	0x0F[4]	--
ADC	0x15[5]	0x15[4]	0x15[3]	0x15[6]	0x15[7]	--
OVPFET_SS_TMO	--	0x27[6]	0x28[6]	0x2A[4]	--	--

I²C REGISTER ADDRESS MAP (continued)

FUNCTION	STAT	FLAG	MASK	THRESHOLD SETTING	ENABLE	DEGLITCH
RVS_SS_LMT	--	--	--	0x2A[0]	--	--
VBAT_BRN_IN_REV	0x10[5]	0x11[5]	0x12[5]	--	--	--
USBGATE_SRC_CURR	--	--	--	0x2B[1:0]	--	--
POR	--	0x0A[7]	--	--	--	--
VOUT UVLO	0x10[3]	0x11[3]	0x12[3]	--	--	--
VOUT_OK_SW_REGN	0x10[6]	0x11[6]	0x12[6]	--	--	--

REGISTER AND DATA

Bit Types:
R: Read only
R/W: Read/Write
RC: Read clears the bit
R/WC: Read/Write. Writing a '1' clears the bit. Writing a 0 has no effect.
NOTE: Excepted for the specified bits, all other register bits are reset to their default values if a hard reset is triggered.

Charge Pump Control

REG0x00: DEVICE_VER Register [Reset = 0x0A]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:4]	DEVICE_VER[3:0]	0000	R	Device Version	N/A
D[3:0]	DEVICE_ID[3:0]	1010	R	Device ID 1010 = SGM41612YGA	N/A

REG0x01: VBAT1_OVP Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	VBAT1_OVP_DIS	0	R/W	VBAT1 OVP Disable Bit 0 = Enabled (default) 1 = Disabled	Hard-reset or REG_RST
D[6]	VBAT1_OVP_MASK	0	R/W	Mask VBAT1 OVP Fault Interrupt 0 = Not masked (default) 1 = Masked	Hard-reset or REG_RST
D[5]	VBAT1_OVP_FLAG	0	RC	VBAT1 OVP Event Flag Bit 0 = No VBAT1 OVP event 1 = VBAT1 OVP event has ever occurred. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0.	N/A
D[4:0]	VBAT1_OVP[4:0]	0 0000	R/W	Battery 1 Over-Voltage Protection Setting When the battery 1 voltage exceeds the OVP threshold, an INT is sent and SCC_EN bit is set to 0. n = VBAT1_OVP[4:0] $V_{BAT1_OVP_R}$ (V) = 4.5V + n × 25mV Default: 4.5V (5'b00000)	Hard-reset or REG_RST

REGISTER AND DATA (continued)

REG0x02: IBAT_OCP Register [Reset = 0x04]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	IBAT_OCP_DIS	0	R/W	IBAT OCP Disable Bit 0 = Enable the IBAT_OCP protection (default) 1 = Disable the IBAT_OCP protection	Hard-reset or REG_RST
D[6]	IBAT_OCP_OFFSET	0	R/W	IBAT OCP Offset Bit 0 = 0A (default) 1 = 5A	Hard-reset or REG_RST
D[5]	IBAT_OCP_MASK	0	R/W	Mask IBAT OCP Fault Interrupt 0 = Not masked (default) 1 = Masked	Hard-reset or REG_RST
D[4]	IBAT_OCP_FLAG	0	RC	IBAT OCP Event Flag Bit 0 = No IBAT OCP event 1 = IBAT OCP event has ever occurred. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0.	N/A
D[3:0]	IBAT_OCP[3:0]	0100	R/W	BAT Over-Current Protection Setting for Forward mode or Reverse Mode. When the battery current exceeds the OCP threshold, an INT is sent and SCC_EN bit is set to 0. n = IBAT_OCP[3:0] k = IBAT_OCP_OFFSET $I_{BAT_OCP_R}$ (A) = 8A + n × 0.5A + k × 5A Default: 10A (4'b0100)	Hard-reset or REG_RST

REG0x03: VUSB_OVP Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	Reserved	0	R	Reserved	N/A
D[6]	VUSB_OVP_MASK	0	R/W	Mask VUSB OVP Fault Interrupt 0 = Not masked (default) 1 = Masked	Hard-reset or REG_RST
D[5]	VUSB_OVP_FLAG	0	RC	VUSB OVP Event Flag Bit 0 = No VUSB OVP event 1 = VUSB OVP event has ever occurred. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0.	N/A
D[4]	VUSB_OVP_STAT	0	R	VUSB OVP Status Bit 0 = Not in VUSB OVP status 1 = In VUSB OVP status.	N/A
D[3:0]	VUSB_OVP[3:0]	0000	R/W	VUSB Over-Voltage Protection Setting When the VUSB voltage exceeds the OVP threshold, the external OVPFET will be turned off by USBGATE. n = VUSB_OVP[3:0] $V_{USB_OVP_R}$ (V) = 11V + n × 1V when n < 15 $V_{USB_OVP_R}$ (V) = 6.5V when n = 15 Default: 11V (4'b0000)	Hard-reset or REG_RST

REGISTER AND DATA (continued)

REG0x04: VBAT2_OVP Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	VBAT2_OVP_DIS	0	R/W	VBAT2 OVP Disable Bit 0 = Enabled (default) 1 = Disabled	Hard-reset or REG_RST
D[6]	VBAT2_OVP_MASK	0	R/W	Mask VBAT2 OVP Fault Interrupt 0 = Not masked (default) 1 = Masked	Hard-reset or REG_RST
D[5]	VBAT2_OVP_FLAG	0	RC	VBAT2 OVP Event Flag Bit 0 = No VBAT2 OVP event 1 = VBAT2 OVP event has ever occurred. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0.	N/A
D[4:0]	VBAT2_OVP[4:0]	0 0000	R/W	Battery 2 Over-Voltage Protection Setting When the battery 2 voltage exceeds the OVP threshold, an INT is sent and SCC_EN bit is set to 0. n = VBAT2_OVP[4:0] $V_{BAT2_OVP_R}$ (V) = 4.5V + n × 25mV Default: 4.5V (5'b00000)	Hard-reset or REG_RST

REG0x05: VOUT_VBUS_OVP Register [Reset = 0xA1]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:2]	VBUS_OVP[5:0]	10 1000	R/W	VBUS Over-Voltage Protection Setting. When the VBUS pin voltage exceeds the OVP threshold, an INT is sent and SCC_EN bit is set to 0. n = VBUS_OVP[5:0] 4:1 charger mode/1:4 converter mode $V_{BUS_OVP_R}$ (V) = 14V + n × 0.2V Default: 22V (6'b101000) 3:1 charger mode/1:3 converter mode $V_{BUS_OVP_R}$ (V) = 10.5V + n × 0.15V Default: 16.5V (6'b101000) 2:1 charger mode/1:2 converter mode $V_{BUS_OVP_R}$ (V) = 7V + n × 0.1V Default: 11V (6'b101000) 1:1 mode $V_{BUS_OVP_R}$ (V) = 3.5V + n × 0.05V Default: 5.5V (6'b101000)	Hard-reset or REG_RST
D[1:0]	VOUT_OVP[1:0]	01	R/W	VOUT Over-Voltage Protection Setting. When the VOUT pin voltage exceeds the OVP threshold, an INT is sent and SCC_EN bit is set to 0. n = VOUT_OVP[1:0] $V_{VOUT_OVP_R}$ = 4.8V + n × 0.2V Default: 5V (2'b01)	Hard-reset or REG_RST

REGISTER AND DATA (continued)

REG0x06: IBUS_OCP Register [Reset = 0x0C]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	IBUS_OCP_DIS	0	R/W	IBUS OCP Disable Bit 0 = Enabled (default) 1 = Disabled	Hard-reset or REG_RST
D[6]	IBUS_OCP_MASK	0	R/W	Mask IBUS OCP Fault Interrupt 0 = Not masked (default) 1 = Masked	Hard-reset or REG_RST
D[5]	IBUS_OCP_FLAG	0	RC	IBUS OCP Event Flag Bit 0 = No IBUS OCP event 1 = IBUS OCP event has ever occurred. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0.	N/A
D[4:0]	IBUS_OCP[4:0]	0 1100	R/W	IBUS OCP Setting for Forward mode or Reverse Mode. When the IBUS exceeds the OCP threshold, an INT is sent and SCC_EN bit is set to 0. n = IBUS_OCP[4:0] Forward charger mode: $I_{BUS_OCP_R}$ (A) = 1A + n × 0.2A Reverse converter mode: $I_{BUS_OCP_R}$ (A) = 1A + n × 0.2A when n < 20 $I_{BUS_OCP_R}$ (A) = 5A when n ≥ 20 Default: 3.4A (5'b01100)	Hard-reset or REG_RST

REG0x07: IBUS_UCP Register [Reset = 0x10]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	IBUS_UCP_DIS	0	R/W	IBUS UCP Disable Bit 0 = Enabled (default) 1 = Disabled	Hard-reset or REG_RST
D[6]	Reserved	0	R	Reserved	N/A
D[5:4]	IBUS_UCP_FALL_DEG[1:0]	01	R/W	IBUS UCP Protection Falling Deglitch Time Setting Bit This is deglitch time ($t_{IBUS_UCPF_DEG}$) between the moment I_{BUS} falling below $I_{BUS_UCP_F}$ threshold and triggering protection action. 00 = 2μs 01 = 8μs (default) 10 = 32ms 11 = 256ms	Hard-reset or REG_RST
D[3]	IBUS_UCP_RISE_MASK	0	R/W	Mask IBUS UCP Rise Interrupt 0 = Not masked (default) 1 = Masked	Hard-reset or REG_RST
D[2]	IBUS_UCP_RISE_FLAG	0	RC	IBUS UCP Rise Event Flag Bit 0 = No IBUS UCP Rise event 1 = IBUS UCP Rise event has ever occurred. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0.	N/A
D[1]	IBUS_UCP_FALL_MASK	0	R/W	Mask IBUS UCP Fall Interrupt 0 = Not masked (default) 1 = Masked	Hard-reset or REG_RST
D[0]	IBUS_UCP_FALL_FLAG	0	RC	IBUS UCP Fall Flag Bit 0 = No IBUS UCP Fall event 1 = IBUS UCP Fall event has ever occurred. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0.	N/A

REGISTER AND DATA (continued)

REG0x08: PMID2VOUT_OVP Register [Reset = 0x02]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	PMID2VOUT_OVP_DIS	0	R/W	PMID2VOUT OVP Disable Bit 0 = Enable the PMID2VOUT OVP protection (default) 1 = Disable the PMID2VOUT OVP protection	Hard-reset or REG_RST
D[6]	Reserved	0	R	Reserved	N/A
D[5]	PMID2VOUT_OVP_DEG	0	R/W	PMID2VOUT OVP Protection Deglitch Time Setting Bit This is deglitch time ($t_{PMID2VOUT_OVP_DEG}$) between the moment V_{PMID} exceeding $V_{PMID2VOUT_OVP}$ threshold and triggering protection action. 0 = 100ns (default) 1 = 128μs	Hard-reset or REG_RST
D[4]	PMID2VOUT_OVP_MASK	0	R/W	Mask PMID2VOUT OVP Interrupt 0 = Not masked (default) 1 = Masked	Hard-reset or REG_RST
D[3]	PMID2VOUT_OVP_FLAG	0	RC	PMID2VOUT OVP Flag Bit 0 = No PMID2VOUT OVP event 1 = PMID2VOUT OVP event has ever occurred. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0.	N/A
D[2:0]	PMID2VOUT_OVP[2:0]	010	R/W	PMID2VOUT OVP Protection Rising Threshold Setting Bits n = 1, 2, 3, or 4 for forward 1:1/2:1/3:1/4:1 charger mode respectively n = 1, 2, 3, or 4 for reverse 1:1/1:2/1:3/1:4 mode respectively k = PMID2VOUT_OVP[2:0] $V_{PMID2VOUT_OVP}$ (V) = n × V_{VOUT} + n × (k+2) ×100mV Default: n × (V_{VOUT} + 400mV) (3'b010)	Hard-reset or REG_RST

REG0x09: PMID2VOUT_UVP Register [Reset = 0x01]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	PMID2VOUT_UVP_DIS	0	R/W	PMID2VOUT UVP Disable Bit 0 = Enable the PMID2VOUT UVP protection (default) 1 = Disable the PMID2VOUT UVP protection	Hard-reset or REG_RST
D[6]	Reserved	0	R	Reserved	N/A
D[5]	PMID2VOUT_UVP_DEG	0	R/W	PMID2VOUT UVP Protection Deglitch Time Setting Bit This is deglitch time ($t_{PMID2VOUT_UVP_DEG}$) between the moment V_{PMID} exceeding $V_{PMID2VOUT_UVP}$ threshold and triggering protection action. 0 = 100ns (default) 1 = 10μs	Hard-reset or REG_RST
D[4]	PMID2VOUT_UVP_MASK	0	R/W	Mask PMID2VOUT UVP Interrupt 0 = Not masked (default) 1 = Masked	Hard-reset or REG_RST
D[3]	PMID2VOUT_UVP_FLAG	0	RC	PMID2VOUT UVP Flag Bit 0 = No PMID2VOUT UVP event 1 = PMID2VOUT UVP event has ever occurred. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0.	N/A
D[2:0]	PMID2VOUT_UVP[2:0]	001	R/W	PMID2VOUT UVP Protection Rising Threshold Setting Bits n = 1, 2, 3, or 4 for forward 1:1/2:1/3:1/4:1 charger mode respectively n = 1, 2, 3, or 4 for reverse 1:1/1:2/1:3/1:4 mode respectively k = PMID2VOUT_UVP[2:0] $V_{PMID2VOUT_UVP}$ (V) = n × V_{VOUT} - n × (k+2) × 50mV Default: n × (V_{VOUT} - 150mV) (3'b001)	Hard-reset or REG_RST

REGISTER AND DATA (continued)

REG0x0A: CONVERTER STATE Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	POR_FLAG	0	RC	Device POR Flag Bit 0 = No POR 1 = POR has ever occurred. Indicate a POR event has ever occurred. An INT is sent when this occurs and is cleared upon read.	N/A
D[6]	VUSB_PDN_STAT	0	R	VUSB Pull-down Status Bit 0 = VUSB Pull-down is not on-going 1 = VUSB Pull-down is on-going	N/A
D[5]	USBGATE_ CONFIG_STAT	0	R	USBGATE Configuration Status Bit 0 = USBGATE pin is tied to GND 1 = USBGATE pin is not tied to GND This bit is updated only when the POR occurs.	N/A
D[4]	VBUS_LO_STAT	0	R	VBUS Low Status Bit 0 = V_{VBUS} is above the low threshold of VBUS range detection 1 = V_{VBUS} is below the low threshold of VBUS range detection	N/A
D[3]	VBUS_HI_STAT	0	R	VBUS High Status Bit 0 = V_{VBUS} is below the high threshold of VBUS range detection 1 = V_{VBUS} is above the high threshold of VBUS range detection	N/A
D[2]	RBFET_ON_STAT	0	R	RBFET On/Off Status Bit 0 = RBFET is OFF 1 = RBFET is ON	N/A
D[1]	SCC_SW_STAT	0	R	Charger or Converter is Active Status Bit 0 = Charge-pump is not switching 1 = Charge-pump is switching	N/A
D[0]	PIN_DIAG_FAIL_ FLAG	0	RC	Pin Diagnosis Fail Event Flag Bit Trigger conditions: 1) C_{FXX} is short or open before switching. 2) C_{FXX} is short after switching. 3) VBUS is found short when turn on RBFET in reverse mode. 4) C_{BTSA}, C_{BTSB}, C_{BTS2} capacitor is found short before switching. 0 = No Pin Diagnosis Fail event 1 = Pin Diagnosis Fail event has ever occurred. It generates an interrupt on nINT pin. Reading this bit will reset it to 0.	N/A

REGISTER AND DATA (continued)

REG0x0B: CTRL1 Register [Reset = 0x20]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	SCC_EN	0	R/W	Switched Capacitor Converter Enable Bit 0 = Disabled (default) 1 = Enabled. If any fault has ever occurred, device returns to standby mode and this bit is automatically cleared to 0.	Hard-reset or REG_RST or WDT
D[6:5]	USBGATE_ON_DEG[1:0]	01	R/W	USBGATE Turn on Deglitch Time ($t_{USBGATE_ON_DEG}$) Setting Bit 00 = 10ms 01 = 20ms (default) 10 = 40ms 11 = 80ms Note: only valid when VUSB is inserted in forward mode.	Hard-reset or REG_RST
D[4]	USBGATE_MODE	0	R/W	USBGATE Operation Mode Setting Bit 0 = Auto mode (default) 1 = Manual mode	Hard-reset or REG_RST or VBUS Present Falling Edge
D[3]	USBGATE_EN	0	R/W	USBGATE Driver Enable Bit 0 = Disable USBGATE output 1 = Enable USBGATE output high (default) Note: Ignore this bit when USBGATE_MODE = 0.	Hard-reset or REG_RST
D[2]	VBUS_PDN_EN	0	R/WC	VBUS Pull-Down Resistor Enable Bit 0 = Pull-down disabled (default) 1 = Pull-down enabled. When enabled, the device pull down the VBUS by R_{PDN_VUSB} for 512ms, and pull down the PMID by R_{PDN_PMID} respectively for 512ms, then this bit is automatically reset to 0.	Hard-reset or REG_RST
D[1]	VUSB_PDN_MODE	0	R/W	Mode Bit for VUSB Pull-down function 0 = Manual Mode (default) 1 = Auto Mode. Pull down for t_{VUSB_PDN} when VUSB drop below VUSB INSERT falling edge	Hard-reset or REG_RST
D[0]	VUSB_PDN_EN	0	R/WC	VUSB Pull-Down Resistor Enable Bit (Only valid in manual mode) 0 = Pull-down disabled (default) 1 = Pull-down enabled. When enabled, the device pull down the VUSB by R_{PDN_VUSB} for t_{VUSB_PDN}, then this bit is automatically reset to 0.	Hard-reset or REG_RST

REG0x0C: CTRL2 Register [Reset = 0x40]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:3]	FSW_SET[4:0]	0 1000	R/W	Switched-Cap Converter Switching Frequency Setting Bits 00000 = 200kHz 00001 = 250kHz 00010 = 300kHz 00011 = 350kHz 00100 = 400kHz 00101 = 450kHz 00110 = 500kHz 00111 = 550kHz 01000 = 600kHz (default) 01001 = 650kHz 01010 = 700kHz 01011 = 750kHz 01100 = 800kHz 01101 = 850kHz 01110 = 900kHz 01111 = 950kHz 10000 = 1000kHz 10001 = 1100kHz 10010 = 1200kHz 10011 = 1300kHz 10100 = 1400kHz 10101, others = 1500kHz Note: These bits are allowed to change during in switching status.	Hard-reset or REG_RST
D[2]	Reserved	0	R	Reserved	N/A
D[1]	FSW_DITHER_EN	0	R/W	Switching Frequency Dithering Enable Bit 0 = Disabled (default) 1 = Enabled. Dither varies switching frequency ±10%	Hard-reset or REG_RST
D[0]	Reserved	0	R	Reserved	N/A

REGISTER AND DATA (continued)

REG0x0D: CTRL3 Register [Reset = 0x18]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	VBUS_HI_LO_DIS	0	R/W	VBUS High and Low Range Detection Disable Bit 0 = Enabled (default) 1 = Disabled	Hard-reset or REG_RST
D[6]	VUSB_PDN_TMO	0	R/W	VUSB Pull-down Timeout (t_{VUSB_PDN}) Setting Bit 0 = 512ms (default) 1 = 32ms	Hard-reset or REG_RST
D[5:3]	IBUS_UCP_BLK[2:0]	011	R/W	Blanking Time ($t_{IBUS_UCP_BLK}$) Setting Bits to Enable the IBUS UCP Protection in Forward Mode 000 = 12.5ms 001 = 25ms 010 = 50ms 011 = 100ms (default) 100 = 200ms 101 = 400ms 110 = 800ms 111 = 10.24s Device starts the blanking timer after switching, and enables the IBUS UCP protection after the timeout occurs.	Hard-reset or REG_RST
D[2:0]	WDT_TIMER[2:0]	000	R/W	Watchdog Timeout Protection Bit 000 = Disable watchdog (default) 001 = 0.2s 010 = 0.5s 011 = 1s 100 = 5s 101 = 30s 110, 111 = Disable watchdog. If the watchdog timer is enabled, the timer will be reset by any I²C read/write.	Hard-reset or REG_RST

REG0x0E: CTRL4 Register [Reset = 0x20]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	IBAT_RSNS_POS	0	R/W	External IBAT Current Sense Resistor Position Setting Bit 0 = Low side (default) 1 = High side	Hard-reset or REG_RST
D[6]	VBAT_OVP_DEG	0	R/W	Deglitch time for VBAT1 and VBAT2 OVP protection 0 = 100ns (default) 1 = 10μs	Hard-reset or REG_RST
D[5:4]	IBAT_RSNS	10	R/W	External IBAT Current Sense Resistor Setting Bit 00 = 0.5mΩ 01 = 1mΩ 10 = 2mΩ (default) 11 = 2mΩ	Hard-reset or REG_RST
D[3]	REG_RST	0	R/WC	Register Reset Bit 0 = No register reset (default) 1 = Reset registers to their default values. When enabled, the associated register bits are reset to their default values and then this bit is automatically reset to 0.	Hard-reset or REG_RST
D[2:0]	SCC_MODE[2:0]	000	R/W	Switched-Cap Converter Operation Mode Control Bits 000 = Forward 4:1 charger mode (default) 001 = Forward 3:1 charger mode 010 = Forward 2:1 charger mode 011 = Forward 1:1 charger mode 100 = Reverse 1:4 converter mode 101 = Reverse 1:3 converter mode 110 = Reverse 1:2 converter mode 111 = Reverse 1:1 converter mode Note: These bits are not allowed to change when SCC_EN =1'b1.	Hard-reset or REG_RST or WDT

REGISTER AND DATA (continued)

REG0x0F: CTRL5 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	VBUS_PRE_RVS_DIS	0	R/W	Disable Bit for Verifying V_{VBUS} < $V_{BUS_PRESENT_F}$ before Reverse Mode Startup 0 = Enabled. Reverse mode cannot start until V_{VBUS} < $V_{BUS_PRESENT_F}$ (default) 1 = Disabled. Reverse mode can start with V_{VBUS} > $V_{BUS_PRESENT_R}$	Hard-reset or REG_RST
D[6]	VBUS_SCP_DIS	0	R/W	VBUS SCP Disable Bit 0 = Enabled (default) 1 = Disabled	Hard-reset or REG_RST
D[5]	CFLY_SHORT_DIS	0	R/W	CFLY Short Protection Disable Bit in Normal Switching Status 0 = Enabled (default) 1 = Disabled	Hard-reset or REG_RST
D[4]	TDIE_OTP_DIS	0	R/W	TDIE OTP Disable Bit 0 = Enabled (default) 1 = Disabled	Hard-reset or REG_RST
D[3]	PEAK_OCP_DIS	0	R/W	Peak OCP Disable Bit 0 = Enabled (default) 1 = Disabled	Hard-reset or REG_RST
D[2]	VUSB_OVP_DIS	0	R/W	VUSB OVP Disable Bit 0 = Enabled (default) 1 = Disabled	Hard-reset or REG_RST
D[1]	VBUS_OVP_DIS	0	R/W	VBUS OVP Disable Bit 0 = Enabled (default) 1 = Disabled	Hard-reset or REG_RST
D[0]	VOUT_OVP_DIS	0	R/W	VOUT OVP Disable Bit 0 = Enabled (default) 1 = Disabled	Hard-reset or REG_RST

REG0x10: INT1_STAT Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	USBGATE_STAT	0	R	Status Bit of USBGATE Driver 0 = USBGATE Driver is OFF (default) 1 = USBGATE Driver is ON	N/A
D[6]	VOUT_OK_SW_REGN_STAT	0	R	Power Source for REGN Status Bit 0 = PMID power the REGN 1 = VOUT power the REGN	N/A
D[5]	VBAT_BRN_IN_REV_STAT	0	R	Status Bit indicates that the VOUT is higher than the brown-in threshold or not in the reverse mode 0 = VOUT is less than the brown-in threshold 1 = VOUT is higher than the brown-in threshold	N/A
D[4]	VBAT_INSERT_STAT	0	R	Status Bit indicates that the VBAT is inserted or not in forward mode 0 = VOUT is less than the insert threshold in the forward mode 1 = VOUT is higher than the insert threshold in the forward mode	N/A
D[3]	VOUT_UVLO_STAT	0	R	Status Bit indicates that the VOUT is above the UVLO threshold or not 0 = VOUT is less than the UVLO threshold 1 = VOUT is greater than the UVLO threshold	N/A
D[2]	VBUS_PRESENT_STAT	0	R	Status Bit indicates that the VBUS is above the present threshold or not 0 = VBUS is less than the present threshold 1 = VBUS is greater than the present threshold	N/A
D[1]	Reserved	0	R	Reserved	N/A
D[0]	VUSB_INSERT_STAT	0	R	Status Bit indicates that the VUSB is inserted or not 0 = VUSB is less than the inserted threshold 1 = VUSB is greater than the inserted threshold	N/A

REGISTER AND DATA (continued)

REG0x11: INT1_FLAG Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	VBUS_ABSENT_FLAG	0	RC	VBUS Absent (Lower than present falling threshold) Event Flag Bit 0 = No VBUS absent event 1 = VUSB absent event has ever occurred. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0.	N/A
D[6]	VOUT_OK_SW_REGN_FLAG	0	RC	VOUT Power the REGN Event Flag Bit 0 = No VOUT power the REGN event 1 = VOUT has ever power the REGN. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0.	N/A
D[5]	VBAT_BRN_IN_REV_FLAG	0	RC	VBAT Brown-in Event Flag Bit in the reverse mode 0 = No battery brown-in event 1 = VBAT brown-in event has ever occurred. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0.	N/A
D[4]	VBAT_INSERT_FLAG	0	RC	VBAT INSERT Event Flag Bit in the forward mode 0 = No battery inserted event 1 = VBAT inserted event has ever occurred. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0.	N/A
D[3]	VOUT_CHG_FLAG	0	RC	VOUT Change Event Flag Bit (VOUT UVLO Rising/Falling edge) 0 = No VOUT Change event 1 = VOUT Change event has ever occurred. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0.	N/A
D[2]	VBUS_PRESENT_FLAG	0	RC	VBUS Present Event Flag Bit 0 = No VBUS present event 1 = VBUS present event has ever occurred. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0.	N/A
D[1]	VUSB_REMOVE_FLAG	0	RC	VUSB Removal (Lower than insert falling threshold) Event Flag Bit 0 = No VUSB removal event 1 = VUSB removal event has ever occurred. It generates an interrupt on nINT pin. Reading this bit will reset it to 0.	N/A
D[0]	VUSB_INSERT_FLAG	0	RC	VUSB Insert Event Flag Bit 0 = No VUSB inserted event 1 = VUSB inserted event has ever occurred. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0.	N/A

REGISTER AND DATA (continued)

REG0x12: INT1_MASK Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	VBUS_ABSENT_MASK	0	R/W	Mask VBUS_ABSENT Interrupt 0 = Not masked (default) 1 = Masked	Hard-reset or REG_RST
D[6]	VOUT_OK_SW_REGN_MASK	0	R/W	Mask VOUT_OK_SW_REGN Interrupt 0 = Not masked (default) 1 = Masked	Hard-reset or REG_RST
D[5]	VBAT_BRN_IN_REV_MASK	0	R/W	Mask VBAT_BRN_IN_REV Interrupt 0 = Not masked (default) 1 = Masked	Hard-reset or REG_RST
D[4]	VBAT_INSERT_MASK	0	R/W	Mask VBAT_INSERT Interrupt 0 = Not masked (default) 1 = Masked	Hard-reset or REG_RST
D[3]	VOUT_CHG_MASK	0	R/W	Mask VOUT_CHG Interrupt 0 = Not masked (default) 1 = Masked	Hard-reset or REG_RST
D[2]	VBUS_PRESENT_MASK	0	R/W	Mask VBUS_PRESENT Interrupt 0 = Not masked (default) 1 = Masked	Hard-reset or REG_RST
D[1]	VUSB_REMOVE_MASK	0	R/W	Mask VUSB_REMOVE Interrupt 0 = Not masked (default) 1 = Masked	Hard-reset or REG_RST
D[0]	VUSB_INSERT_MASK	0	R/W	Mask VUSB_INSERT Interrupt 0 = Not masked (default) 1 = Masked	Hard-reset or REG_RST

REG0x13: INT2_FLAG Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	Reserved	0	R	Reserved	N/A
D[6]	TDIE_OTP_FLAG	0	RC	TDIE OTP Event Flag Bit 0 = No TDIE OTP event 1 = TDIE OTP event has ever occurred. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0.	N/A
D[5]	IBUS_UCP_BLK_TMO_FLAG	0	RC	IBUS UCP BLK Timeout Event Flag Bit 0 = No IBUS UCP blanking timeout event 1 = IBUS UCP blanking timeout event has ever occurred. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0.	N/A
D[4]	WD_TIMEOUT_FLAG	0	RC	Watchdog Timeout Event Flag Bit 0 = No watchdog timeout event 1 = Watchdog timeout event has ever occurred. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0.	N/A
D[3]	PEAK_OCP_FLAG	0	RC	Peak OCP Event Flag Bit (Any one for Q1x,Q3x,Q5x,Q7x,Q10x) 0 = No peak OCP event 1 = Peak OCP event has ever occurred. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0.	N/A
D[2]	RVS_SS_FAIL_FLAG	0	RC	Reverse Mode Soft-start Failure Event Flag Bit 0 = No reverse mode soft-start failure event 1 = Reverse mode soft-start failure event has ever occurred. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0.	N/A
D[1]	VBUS_OVP_FLAG	0	RC	VBUS OVP Event Flag Bit 0 = No VBUS OVP event 1 = VBUS OVP event has ever occurred. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0.	N/A
D[0]	VOUT_OVP_FLAG	0	RC	VOUT OVP Event Flag Bit 0 = No VOUT OVP event 1 = VOUT OVP event has ever occurred. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0.	N/A

REGISTER AND DATA (continued)

REG0x14: INT2_MASK Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	Reserved	0	R	Reserved	N/A
D[6]	TDIE_OTP_MASK	0	R/W	Mask TDIE_OTP Interrupt 0 = Not masked (default) 1 = Masked	Hard-reset or REG_RST
D[5]	IBUS_UCP_BLK_ TMO _MASK	0	R/W	Mask IBUS UCP BLK TIMEOUT Interrupt 0 = Not masked (default) 1 = Masked	Hard-reset or REG_RST
D[4]	WD_TIMEOUT_ MASK	0	R/W	Mask WD_TIMEOUT Interrupt 0 = Not masked (default) 1 = Masked	Hard-reset or REG_RST
D[3]	PEAK_OCP_MASK	0	R/W	Mask PEAK_OCP Interrupt 0 = Not masked (default) 1 = Masked	Hard-reset or REG_RST
D[2]	RVS_SS_FAIL_ MASK	0	R/W	Mask RVS_SS_ FAIL Interrupt 0 = Not masked (default) 1 = Masked	Hard-reset or REG_RST
D[1]	VBUS_OVP_MASK	0	R/W	Mask VBUS_OVP Interrupt 0 = Not masked (default) 1 = Masked	Hard-reset or REG_RST
D[0]	VOUT_OVP_MASK	0	R/W	Mask VOUT_OVP Interrupt 0 = Not masked (default) 1 = Masked	Hard-reset or REG_RST

REG0x15: ADC_CTRL1 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	ADC_EN	0	R/W	ADC Conversion Enable 0 = Disabled (default) 1 = Enabled Note: In 1-shot mode when the selected channel conversions are completed, the ADC_EN bit is automatically reset to 0. Note1: All channel conversions can be enabled separately even when the device is not in switching status.	Hard-reset or REG_RST or WDT
D[6]	ADC_RATE	0	R/W	ADC Conversion Mode Control 0 = Continuous conversion (default) 1 = 1-shot conversion	Hard-reset or REG_RST
D[5]	ADC_DONE_STAT	0	R	Status Bit indicate that ADC conversion is on-going in 1-shot conversion mode 0 = ADC conversion is on-going 1 = ADC conversion is done	N/A
D[4]	ADC_DONE_FLAG	0	RC	ADC Conversion Done Event Flag Bit in 1-shot conversion mode 0 = No ADC Conversion Done event 1 = ADC Conversion Done event has ever occurred. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0.	N/A
D[3]	ADC_DONE_MASK	0	R/W	Mask ADC_DONE Interrupt 0 = Not masked 1 = Masked	Hard-reset or REG_RST
D[2]	ADC_AVG	0	R/W	Average Times of ADC Sampling 0 = 1 time (default) 1 = 8 times	Hard-reset or REG_RST
D[1]	VBAT2_ADC_EN	0	R/W	VBAT2 ADC Control Bit 0 = Disable conversion (default) 1 = Enable conversion	Hard-reset or REG_RST
D[0]	IBUS_ADC_DIS	0	R/W	IBUS ADC Control Bit 0 = Enable conversion (default) 1 = Disable conversion	Hard-reset or REG_RST

REGISTER AND DATA (continued)

REG0x16: ADC_CTRL2 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	VBUS_ADC_DIS	0	R/W	VBUS ADC Control Bit 0 = Enable conversion (default) 1 = Disable conversion	Hard-reset or REG_RST
D[6]	VUSB_ADC_DIS	0	R/W	VUSB ADC Control Bit 0 = Enable conversion (default) 1 = Disable conversion	Hard-reset or REG_RST
D[5]	Reserved	0	R	Reserved	N/A
D[4]	VOUT_ADC_DIS	0	R/W	VOUT ADC Control Bit 0 = Enable conversion (default) 1 = Disable conversion	Hard-reset or REG_RST
D[3]	VBAT1_ADC_DIS	0	R/W	VBAT1 ADC Control Bit 0 = Enable conversion (default) 1 = Disable conversion	Hard-reset or REG_RST
D[2]	IBAT_ADC_DIS	0	R/W	IBAT ADC Control Bit 0 = Enable conversion (default) 1 = Disable conversion	Hard-reset or REG_RST
D[1]	Reserved	0	R	Reserved	N/A
D[0]	TDIE_ADC_DIS	0	R/W	TDIE ADC Control Bit 0 = Enable conversion (default) 1 = Disable conversion	Hard-reset or REG_RST

REG0x17: IBUS_ADC1 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:4]	Reserved	0000	R	Reserved	N/A
D[3:0]	IBUS_ADC[11:8]	0000	R	Higher 4 Bits of the 12-bit ADC IBUS Data (1.5625mA resolution) MSB<3:0>: 3200mA, 1600mA, 800mA, 400mA	Hard-reset or REG_RST

REG0x18: IBUS_ADC0 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	IBUS_ADC[7:0]	0000 0000	R	Low Byte of the 12-bit ADC IBUS Data (1.5625mA resolution) LSB<7:0>: 200mA, 100mA, 50mA, 25mA, 12.5mA, 6.25mA, 3.125mA, 1.5625mA	Hard-reset or REG_RST

REG0x19: VBUS_ADC1 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:4]	Reserved	0000	R	Reserved	N/A
D[3:0]	VBUS_ADC[11:8]	0000	R	Higher 4 Bits of the 12-bit ADC VBUS Data (6.25mV resolution) MSB<3:0>: 12800mV, 6400mV, 3200mV, 1600mV	Hard-reset or REG_RST

REG0x1A: VBUS_ADC0 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	VBUS_ADC[7:0]	0000 0000	R	Low Byte of the 12-bit ADC VBUS Data (6.25mV resolution) LSB<7:0>: 800mV, 400mV, 200mV, 100mV, 50mV, 25mV, 12.5mV, 6.25mV	Hard-reset or REG_RST

REG0x1B: VUSB_ADC1 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:4]	Reserved	0000	R	Reserved	N/A
D[3:0]	VUSB_ADC[11:8]	0000	R	Higher 4 Bits of the 12-bit ADC VUSB Data (6.25mV resolution) MSB<3:0>: 12800mV, 6400mV, 3200mV, 1600mV	Hard-reset or REG_RST

REGISTER AND DATA (continued)

REG0x1C: VUSB_ADC0 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	VUSB_ADC[7:0]	0000 0000	R	Low Byte of the 12-bit ADC VUSB Data (6.25mV resolution) LSB<7:0>: 800mV, 400mV, 200mV, 100mV, 50mV, 25mV, 12.5mV, 6.25mV	Hard-reset or REG_RST

REG0x1D: VOUT_ADC1 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:4]	Reserved	0000	R	Reserved	N/A
D[3:0]	VOUT_ADC[11:8]	0000	R	Higher 4 Bits of the 12-bit ADC VOUT Data (1.25mV resolution) MSB<3:0>: 2560mV, 1280mV, 640mV, 320mV	Hard-reset or REG_RST

REG0x1E: VOUT_ADC0 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	VOUT_ADC[7:0]	0000 0000	R	Low Byte of the 12-bit ADC VOUT Data (1.25mV resolution) LSB<7:0>: 160mV, 80mV, 40mV, 20mV, 10mV, 5mV, 2.5mV, 1.25mV	Hard-reset or REG_RST

REG0x1F: VBAT1_ADC1 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:4]	Reserved	0000	R	Reserved	N/A
D[3:0]	VBAT1_ADC[11:8]	0000	R	Higher 4 Bits of the 12-bit ADC VBAT1 Data (1.25mV resolution) MSB<3:0>: 2560mV, 1280mV, 640mV, 320mV	Hard-reset or REG_RST

REG0x20: VBAT1_ADC0 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	VBAT1_ADC[7:0]	0000 0000	R	Low Byte of the 12-bit ADC VBAT1 Data (1.25mV resolution) LSB<7:0>: 160mV, 80mV, 40mV, 20mV, 10mV, 5mV, 2.5mV, 1.25mV	Hard-reset or REG_RST

REG0x21: IBAT_ADC1 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:4]	Reserved	0000	R	Reserved	N/A
D[3:0]	IBAT_ADC[11:8]	0000	R	Higher 4 Bits of the 12-bit ADC IBAT Data (5mA resolution) MSB<3:0>: 10240mA, 5120mA, 2560mA, 1280mA	Hard-reset or REG_RST

REG0x22: IBAT_ADC0 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	IBAT_ADC[7:0]	0000 0000	R	Low Byte of the 12-bit ADC IBAT Data (5mA resolution) LSB<7:0>: 640mA, 320mA, 160mA, 80mA, 40mA, 20mA, 10mA, 5mA	Hard-reset or REG_RST

REG0x23: VBAT2_ADC1 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:4]	Reserved	0000	R	Reserved	N/A
D[3:0]	VBAT2_ADC[11:8]	0000	R	Higher 4 Bits of the 12-bit ADC VBAT2 Data (1.25mV resolution) MSB<3:0>: 2560mV, 1280mV, 640mV, 320mV	Hard-reset or REG_RST

REGISTER AND DATA (continued)

REG0x24: VBAT2_ADC0 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	VBAT2_ADC[7:0]	0000 0000	R	Low Byte of the 12-bit ADC VBAT2 Data (1.25mV resolution) LSB<7:0>: 160mV, 80mV, 40mV, 20mV, 10mV, 5mV, 2.5mV, 1.25mV	Hard-reset or REG_RST

REG0x25: TDIE_ADC1 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:1]	Reserved	000 0000	R	Reserved	N/A
D[0]	TDIE_ADC[8]	0	R	Higher 1 Bit of the 9-bit ADC TDIE Data (0.5℃ resolution) MSB: 128℃	Hard-reset or REG_RST

REG0x26: TDIE_ADC0 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	TDIE_ADC[7:0]	0000 0000	R	Low Byte of the 9-bit ADC TDIE Data (0.5℃ resolution) LSB<7:0>: 64℃, 32℃, 16℃, 8℃, 4℃, 2℃, 1℃, 0.5℃ TDIE(℃) = TDIE_ADC[8:0] × 0.5℃	Hard-reset or REG_RST

REG0x27: INT3_FLAG Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	Reserved	0	R	Reserved	N/A
D[6]	OVPFET_SS_TMO_FLAG	0	RC	External OVPFETs (Q_{USB}) Soft-start Timeout Event Flag Bit 0 = No OVPFET soft-start timeout event 1 = OVPFET soft-start timeout event has ever occurred. It generates an interrupt on nINT pin if unmasked. Reading this bit will be reset it to 0.	N/A
D[5]	RVS_SS_OK_FLAG	0	RC	Reverse Mode Soft-start Success Flag Bit 0 = No successfully reverse mode soft-start event 1 = Successfully reverse mode soft-start has ever occurred. When reverse mode soft-start successfully, It generates an interrupt on nINT pin. Reading this bit will reset it to 0.	N/A
D[4]	Reserved	0	R	Reserved	N/A
D[3]	VOUT_SCP_FLAG	0	RC	VOUT SCP Event Flag Bit 0 = No VOUT SCP event 1 = VOUT SCP event has ever occurred. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0.	N/A
D[2:0]	Reserved	000	RC	Reserved	N/A

REG0x28: INT3_MASK Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	Reserved	0	R	Reserved	N/A
D[6]	OVPFET_SS_TMO_MASK	0	R/W	Mask OVPFET_SS_TMO Interrupt 0 = Not masked (default) 1 = Masked	Hard-reset or REG_RST
D[5]	RVS_SS_OK_MASK	0	R/W	Mask RVS_SS_OK Interrupt 0 = Not masked (default) 1 = Masked	Hard-reset or REG_RST
D[4]	Reserved	0	R	Reserved	N/A
D[3]	VOUT_SCP_MASK	0	R/W	Mask VOUT_SCP Interrupt 0 = Not masked (default) 1 = Masked	Hard-reset or REG_RST
D[2]	R1T2_SWL_CTRL	0	R/W	Reverse 1:2 Mode Startup with Load Control Bit 0 = Do not support startup with load in reverse 1:2 mode (default) 1 = Support startup with load in reverse 1:2 mode	Hard-reset or REG_RST
D[1:0]	Reserved	00	R	Reserved	N/A

REGISTER AND DATA (continued)

REG0x29: PEAK_OCP Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	PEAK_ OCP_BLK	0	R/W	Peak OCP Blanking Time Setting Bit 0 = 50ns (default) 1 = 100ns	Hard-reset or REG_RST
D[6]	Reserved	0	R	Reserved	N/A
D[5]	VUSB_ABSENT_ GATEON_DIS	0	R/W	Disable Bit for Detecting VUSB Absent (V_{VUSB} < $V_{USB_INSERT_F}$) before Turning on USBGATE in Reverse Mode 0 = Enable, USBGATE cannot turn on until V_{VUSB} < $V_{USB_INSERT_F}$ (default) 1 = Disable, USBGATE can turn on with V_{VUSB} > $V_{USB_INSERT_R}$	Hard-reset or REG_RST
D[4:0]	Reserved	0 0000	R	Reserved	N/A

REG0x2A: MISC_CTRL1 Register [Reset = 0x24]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:6]	Reserved	00	R	Reserved	N/A
D[5]	IBAT_OCP_DEG	1	R/W	IBAT Bidirectional OCP Protection Deglitch Time Setting Bit 0 = 0.1ms 1 = 1ms (default) This is deglitch time ($t_{IBAT_OCP_DEG}$) between the moment IBAT exceeding IBAT_OCP threshold and triggering protection action.	Hard-reset or REG_RST
D[4]	OVPFET_SS_TMO	0	R/W	USBGATE Soft-start Timeout Setting Bits 0 = 10ms (default) 1 = 5ms	Hard-reset or REG_RST
D[3:2]	Reserved	01	R	Reserved	N/A
D[1]	RVS_SS_TIMER	0	R/W	Soft-Start Timeout Timer in Reverse Mode 0 = 128ms (default) 1 = 256ms When the RBFET is turn on in reverse mode, the timer is initiated and stop to count when V_{PMID} > n × (V_{VOUT} - 100mV) (n = 1, 2, 3, 4 for reverse 1:1/1:2/1:3/1:4 mode respectively) and timeout does not occur; If V_{PMID} < n × (V_{VOUT} - 100mV) after timeout, RVS_SS_FAIL_FLAG bit is set to 1, an INT is sent out and SCC_EN bit is cleared to 0.	Hard-reset or REG_RST
D[0]	RVS_SS_LMT	0	R/W	Soft-start Current Limit Setting Bits in Reverse Mode (For Q8x, Q9x,Q10x) 0 = 100mA (default) 1 = 200mA	Hard-reset or REG_RST

REGISTER AND DATA (continued)

REG0x2B: MISC_CTRL2 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	VBUS_PRESENT_DEG	0	R/W	Deglitch Time for VBUS Present Rising Edge 0 = 5ms (default) 1 = 10ms	Hard-reset or REG_RST
D[6]	RST_USBGATE_ON_VBUSF_DIS	0	R/W	Disable Bit for Resetting the USBGATE_MODE bit 0 = Enabled (default) 1 = Disabled When the bit is 0, the USBGATE MODE bit is reset to 0 at VBUS present falling edge.	Hard-reset or REG_RST
D[5]	IBUS_OCP_DEG	0	R/W	Deglitch Time for IBUS OCP 0 = 4μs (default) 1 = 64μs	Hard-reset or REG_RST
D[4]	Reserved	0	R	Reserved	N/A
D[3]	GATE_HI_SET	0	R/W	External OVPFET Gate Driver Voltage Setting Bit V_{QOVP_GATE} = ($V_{USBGATE}$ - V_{USBSUB}) 0 = The driver high level voltage is 5V (default) 1 = The driver high level voltage is 9V	Hard-reset or REG_RST
D[2]	Reserved	0	R	Reserved	N/A
D[1:0]	USBGATE_SRC_CURR[1:0]	00	R/W	USBGATE Source Current Setting Bits 00 = 10μA (default) 01 = 20μA 10 = 40μA 11 = 120μA	Hard-reset or REG_RST

REGISTER AND DATA (continued)

UFCS Control

REG0x30: UFCS_CTRL1 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	UFCS_EN	0	R/W	UFCS PHY Enable Control Bit 0 = Disable UFCS block (default) 1 = Enable UFCS block This bit will be reset to the default value on a VUSB remove falling edge.	Hard-reset or REG_RST or VUSB_ REMOVE
D[6]	Reserved	0	R	Reserved	N/A
D[5]	UFCS_ HANDSHAKE_EN	0	R/W	Enable Bit for UFCS Handshaking 0 = Disable UFCS handshake (default) 1 = Enable UFCS handshake	Hard-reset or REG_RST
D[4:3]	BAUD_RATE[1:0]	00	R/W	Baud Rate Control Bits for Outing Data 00 = 115200 bps (default) 01 = 57600 bps 10 = 38400 bps 11 = 115200 bps	Hard-reset or REG_RST
D[2]	SND_CMD	0	WC	Master Transmission Start Bit 0 = Not transaction (default) 1 = Start transaction This bit is cleared to 0 when UFCS_EN = 0.	Hard-reset or REG_RST
D[1]	CABLE_ HARDRESET	0	WC	Send Reset Command to Cable 0 = Not sent hard-reset cable (default) 1 = Sent hard-reset cable	Hard-reset or REG_RST
D[0]	SOURCE_ HARDRESET	0	WC	Send Reset Command to Source 0 = Not sent hard-reset source (default) 1 = Sent hard-reset source	Hard-reset or REG_RST

REG0x31: UFCS_CTRL2 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	UFCS_DP_ PULLUP_EN	0	R/W	Pull-up Resistor Setting Bit for DP pin 0 = No 50kΩ resistor pull-up to 3.3V (default) 1 = 50kΩ resistor pull-up to 3.3V	Hard-reset or REG_RST
D[6]	Reserved	0	R	Reserved	N/A
D[5]	TX_BUFFER_CLR	0	WC	Clear Transmission Buffer Bit 0 = Not clear TX_BUFFER data (default) 1 = Clear TX_BUFFER data when it's not locked	Hard-reset or REG_RST
D[4]	RX_BUFFER_CLR	0	WC	Clear Receive Buffer Bit 0 = Not clear RX_BUFFER data (default) 1 = Clear RX_BUFFER data when it's not locked	Hard-reset or REG_RST
D[3:2]	DETECTED_ BAUD_RATE[1:0]	00	R	Baud Rate Bits for Incoming Data 00 = 115200 bps (default) 01 = 57600 bps 10 = 38400 bps 11 = Not used	Hard-reset or REG_RST
D[1]	ACK_CABLE	0	R/W	UFCS Reply Setting Bit 0 = UFCS reply ACK or NCK to source (default) 1 = UFCS reply ACK or NCK to cable	Hard-reset or REG_RST
D[0]	EN_DM_HIZ	0	R/W	DM Pin HIZ-Mode Enable Bit 0 = UFCS drive DM when enable UFCS block (default) 1 = UFCS doesn't drive DM when enable UFCS block	Hard-reset or REG_RST

REG0x32: Reserved Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	Reserved	0000 0000	R	Reserved	N/A

REGISTER AND DATA (continued)

REG0x33: UFCS_INT_FLAG1 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	UFCS_ HANDSHAKE_ FAIL_FLAG	0	RC	Error Flag of UFCS Failed Handshake 0 = UFCS handshake success or not complete (default) 1 = UFCS handshake fail. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0.	N/A
D[6]	UFCS_ HANDSHAKE_ SUCC_FLAG	0	RC	Event Flag of UFCS Successful Handshake 0 = UFCS handshake fail or not complete (default) 1 = UFCS handshake success. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0.	N/A
D[5]	SENT_PACKET_ COMPLETE_ FLAG	0	RC	Event Flag of UFCS Data Packet Transmission Complete 0 = Sent packet not complete or fail (default) 1 = Sent packet complete. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0.	N/A
D[4]	DATA_READY_ FLAG	0	RC	Received Slave Data is Ready for I²C Read by Master 0 = Received data is not ready (default) 1 = Received data is ready. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0.	N/A
D[3]	RX_OVERFLOW_ FLAG	0	RC	Error Flag of UFCS Receive Buffer Overflow 0 = RX data don't exceed RX buffer length (default) 1 = RX data exceed RX buffer length. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0.	N/A
D[2]	RX_BUFFER_ BUSY_FLAG	0	RC	Event Flag of RX Buffer Busy when Receiving Message 0 = The last RX buffer data has been read while a new DATA_READY_FLAG received 1 = The last RX buffer data has not been read while a new DATA_READY_FLAG received. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0.	N/A
D[1]	MSG_TRANS_ FAIL_FLAG	0	RC	Error Flag of UFCS Failed Data Transmission 0 = No message sent fail 1 = Message sent fail after retry three times. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0.	N/A
D[0]	ACK_RECEIVE_ TIMEOUT_FLAG	0	RC	Error Flag of Receiving ACK Signal Timeout 0 = No ACK receive timeout event (default) 1 = ACK receive timeout. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0.	N/A

REGISTER AND DATA (continued)

REG0x34: UFCS_INT_FLAG2 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	BAUD_RATE_ ERROR_FLAG	0	RC	Error Flag of UFCS Baud Rate 0 = BAUD_RATE_CHECK OK (default) 1 = BAUD_RATE error. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0.	N/A
D[6]	TRAINING_ BYTES_ERROR_ FLAG	0	RC	Error Flag of UFCS Receiving Training Byte 0 = Training byte is right (default) 1 = Training byte is error. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0.	N/A
D[5]	DATA_BYTE_ TMOUT_FLAG	0	RC	Error Flag of Data Byte Duration 0 = Data byte duration is within 600μs (default) 1 = Data byte duration is beyond 600μs. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0.	N/A
D[4]	LENGTH_ERROR_ FLAG	0	RC	Error Flag of Received Data Length 0 = Received Data length is right (default) 1 = Received Data length is error. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0.	N/A
D[3]	START_FAIL_ FLAG	0	RC	Error Flag of Received Data Start Byte 0 = Received Data start byte is right (default) 1 = Received Data start byte detects fail. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0.	N/A
D[2]	STOP_ERROR_ FLAG	0	RC	Error Flag of Received Data Stop Byte 0 = Received Data stop byte is right (default) 1 = Received Data stop byte is error. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0.	N/A
D[1]	CRC_ERROR_ FLAG	0	RC	Error Flag of CRC Check 0 = CRC_check OK (default) 1 = CRC error. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0.	N/A
D[0]	HARD_RESET_ FLAG	0	RC	Event Flag of UFCS Receiving Hard Reset Signal 0 = Do not receive hard reset (default) 1 = Receive hard reset. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0.	N/A

REG0x35: UFCS_INT_FLAG3 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	BUS_CONFLICT_ FLAG	0	RC	Event Flag of Bus Conflict 0 = DP and DM bus don't work conflict 1 = DP and DM bus work conflict. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0.	N/A
D[6]	BAUDRATE_CHG_ FLAG	0	RC	Event Flag of UFCS Baud Rate Change 0 = Baud-rate not changed 1 = Baud-rate is changed after RX ping message with different baud-rate. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0.	N/A
D[5]	DATA_BIT_ERR_ FLAG	0	RC	Error Flag of Data Bit 0 = Data bit doesn't changes in the range 1/4~3/4 of bit count 1 = Data bit changes in the range 1/4~3/4 of bit count. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0.	N/A
D[4:2]	Reserved	000	RC	Reserved	N/A
D[1]	TX_BUSY	0	R	TX Transmit Status Bit 0 = UFCS PHY TX is not in transmit process 1 = UFCS PHY TX is during transmit process	N/A
D[0]	RX_BUSY	0	R	RX Transmit Status Bit 0 = UFCS PHY RX is not in transmit process 1 = UFCS PHY RX is during transmit process	N/A

REGISTER AND DATA (continued)

REG0x36: UFCS_INT_MASK1 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	UFCS_ HANDSHAKE_ FAIL_MASK	0	R/W	Mask UFCS_HANDSHAKE_FAIL Interrupt 0 = Not masked 1 = Masked	Hard-reset or REG_RST
D[6]	UFCS_ HANDSHAKE_ SUCC_MASK	0	R/W	Mask UFCS_HANDSHAKE_SUCCESS Interrupt 0 = Not masked 1 = Masked	Hard-reset or REG_RST
D[5]	SENT_PACKET_ COMPLETE_ MASK	0	R/W	Mask SENT_PACKET_COMPLETE Interrupt 0 = Not masked 1 = Masked	Hard-reset or REG_RST
D[4]	DATA_READY_ MASK	0	R/W	Mask DATA_READY Interrupt 0 = Not masked 1 = Masked	Hard-reset or REG_RST
D[3]	RX_OVERFLOW_ MASK	0	R/W	Mask RX_OVERFLOW Interrupt 0 = Not masked 1 = Masked	Hard-reset or REG_RST
D[2]	RX_BUFF_BUSY_ MASK	0	R/W	Mask RX_BUFF_BUSY Interrupt 0 = Not masked 1 = Masked	Hard-reset or REG_RST
D[1]	MSG_TRANS_ FAIL_MASK	0	R/W	Mask MSG_TRANS_FAIL Interrupt 0 = Not masked 1 = Masked	Hard-reset or REG_RST
D[0]	ACK_RECEIVE_ TIMEOUT_MASK	0	R/W	Mask ACK_RECEIVE_TIMEOUT Interrupt 0 = Not masked 1 = Masked	Hard-reset or REG_RST

REG0x37: UFCS_INT_MASK2 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	BAUD_RATE_ ERROR_MASK	0	R/W	Mask BAUD_RATE_ERROR Interrupt 0 = Not masked 1 = Masked	Hard-reset or REG_RST
D[6]	TRAINING_ BYTES_ERROR_ MASK	0	R/W	Mask TRAINING_BYTES_ERROR Interrupt 0 = Not masked 1 = Masked	Hard-reset or REG_RST
D[5]	DATA_BYTE_ TMOUT_MASK	0	R/W	Mask DATA_BYTE_TMOUT Interrupt 0 = Not masked 1 = Masked	Hard-reset or REG_RST
D[4]	LENGTH_ERROR_ MASK	0	R/W	Mask LENGTH_ERROR Interrupt 0 = Not masked 1 = Masked	Hard-reset or REG_RST
D[3]	START_FAIL_ MASK	0	R/W	Mask START_FAIL Interrupt 0 = Not masked 1 = Masked	Hard-reset or REG_RST
D[2]	STOP_ERROR_ MASK	0	R/W	Mask STOP_ERROR Interrupt 0 = Not masked 1 = Masked	Hard-reset or REG_RST
D[1]	CRC_ERROR_ MASK	0	R/W	Mask CRC_ERROR Interrupt 0 = Not masked 1 = Masked	Hard-reset or REG_RST
D[0]	HARD_RESET_ MASK	0	R/W	Mask HARD_RESET Interrupt 0 = Not masked 1 = Masked	Hard-reset or REG_RST

REGISTER AND DATA (continued)

REG0x38: UFCS_INT_MASK3 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	BUS_CONFLICT_MASK	0	R/W	Mask BUS_CONFLICT Interrupt 0 = Not masked 1 = Masked	Hard-reset or REG_RST
D[6]	BAUDRATE_CHG_MASK	0	R/W	Mask BAUDRATE_CHG Interrupt 0 = Not masked 1 = Masked	Hard-reset or REG_RST
D[5]	DATA_BIT_ERR_MASK	0	R/W	Mask DATA_BIT_ERR Interrupt 0 = Not masked 1 = Masked	Hard-reset or REG_RST
D[4:0]	Reserved	0 0000	R	Reserved	N/A

REG0x39: TX_LENGTH Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	TX_LENGTH[7:0]	0000 0000	R/W	TX Data Length, except Training Byte and CRC Byte	Hard-reset or REG_RST

REG0x3A ~ REG0x5D: TX_BUFFERx (x: 0 ~ 35) Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	TX_BUFFERx[7:0]	0000 0000	R/W	TX Data Buffer	Hard-reset or REG_RST

REG0x5E: RX_LENGTH Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	RX_LENGTH[7:0]	0000 0000	R	RX Data Length, except Training Byte	N/A

REG0x5F ~ REG0x9E: RX_BUFFERx (x: 0 ~ 63) Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	RX_BUFFERx[7:0]	0000 0000	R	RX Data Buffer	N/A

REGISTER AND DATA (continued)

BC1.2 Control

REG0xA1: BC1.2_FLAG Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:6]	Reserved	00	R	Reserved	N/A
D[5]	VUSB_CHG_FLAG	0	RC	Event Flag Bit of VUSB Voltage Change 0 = No VUSB voltage change event 1 = VUSB voltage change event has ever occurred, namely that VUSB insert or absent event has ever occurred. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0.	Hard-reset
D[4]	USB_DEVICE_CHG_FLAG	0	RC	Event Flag Bit of USB BC1.2 Device Status Bits Change 0 = No USB_DEVICE_STAT[2:0] bits change event 1 = USB_DEVICE_STAT[2:0] bits change event has ever occurred. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0.	Hard-reset
D[3:0]	Reserved	0000	R	Reserved	N/A

REG0xA2: BC1.2_MASK Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:6]	Reserved	00	R	Reserved	N/A
D[5]	VUSB_CHG_MASK	0	R/W	Mask Interrupt of VUSB Voltage Change Event 0 = Interrupt of VUSB voltage change event can work. (default) 1 = Mask interrupt of VUSB voltage change event. VUSB_CHG_FLAG bit sets after the fault, but this bit suppresses the interrupt signal on nINT pin.	Hard-reset
D[4]	USB_DEVICE_CHG_MASK	0	R/W	Mask Interrupt of USB BC1.2 Device Status Bits Change Event 0 = Interrupt of USB_DEVICE_STAT[2:0] bits change event can work. (default) 1 = Mask interrupt of USB_DEVICE_STAT[2:0] bits change event. USB_DEVICE_CHG_FLAG bit sets after the fault, but this bit suppresses the interrupt signal on nINT pin.	Hard-reset
D[3:0]	Reserved	0000	R	Reserved	N/A

REGISTER AND DATA (continued)

REG0xA3: DPDM_DETC Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	DPDM_DETC_EN	0	R/W	Enable Bit of DP/DM Detection for Debug 0 = Disabled (default) 1 = Enabled. The DP/DM detection results are updated every 8ms.	Hard-reset
D[6:4]	DP_RSLT[2:0]	000	R	DP Pin Voltage Detection Result Bits 000 = 0V. The DP pin voltage is in the range of 0 to 0.05V. 001 = 0.2V. The DP pin voltage is in the range of 0.15V to 0.25V. 010 = 0.6V. The DP pin voltage is in the range of 0.55V to 0.65V. 011 = 1.8V. The DP pin voltage is in the range of 1.65V to 1.95V. 100 = 3.3V.The DP pin voltage is in the range of 3V to 3.6V. 111 = Error. The DP pin voltage is not listed above. Only valid when DPDM_DETC_EN bit is set to 1.	Hard-reset
D[3]	Reserved	0	R	Reserved	N/A
D[2:0]	DM_RSLT[2:0]	000	R	DM Pin Voltage Detection Result Bits 000 = 0V. The DM pin voltage is in the range of 0 to 0.05V. 001 = 0.2V. The DM pin voltage is in the range of 0.15V to 0.25V. 010 = 0.6V. The DM pin voltage is in the range of 0.55V to 0.65V. 011 = 1.8V. The DM pin voltage is in the range of 1.65V to 1.95V. 100 = 3.3V.The DM pin voltage is in the range of 3V to 3.6V. 111 = Error. The DM pin voltage is not in the ranges listed above. Only valid when DPDM_DETC_EN bit is set to 1.	Hard-reset

REG0xA4: BC1.2_CTRL Register [Reset = 0x18]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:6]	Reserved	00	R	Reserved	N/A
D[5:4]	DCD_TIMER[1:0]	01	R/W	DCD Timer $t_{DCD_TIMEOUT}$ Setting Bits 00 = The DCD detection is disabled. 01 = 600ms (default) 10 = 900ms 11 = The DCD timer is infinite. The BC1.2 detection cannot step forward until DP voltage is detected below V_{LGC_LOW}.	Hard-reset
D[3]	DCD_DELAY	1	R/W	DCD Detection Delay Time Setting Bit for BC1.2 This is delay time (t_{DCD_DLY}) from when BC1.2 is enabled and VBUS is present to when the DCD detection starts. 0 = 150ms 1 = 300ms (default)	Hard-reset
D[2]	BC_AUTO_EN	0	R/W	BC1.2 Automatic Detection Enable Bit 0 = Disabled (default) 1 = Enabled. When VBUS is present, it will automatically start BC1.2 detection.	Hard-reset
D[1:0]	Reserved	00	R	Reserved	N/A

REGISTER AND DATA (continued)

REG0xA5: DPDM_CTRL Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:6]	Reserved	00	R	Reserved	N/A
D[5:4]	DP_DAC[1:0]	00	R/W	DP Pin Output Driver Voltage Setting Bits 00 = HiZ mode (default) 01 = 0V (V_{0P0_VSRC}) 10 = 0.6V (V_{0P6_VSRC}) 11 = 3.3V (V_{3P3_VSRC}) Note: The bit configurations are invalid during BC1.2 detection.	Hard-reset or VUSB REMOVE
D[3:2]	DM_DAC[1:0]	00	R/W	DM Pin Output Driver Voltage Setting Bits 00 = HiZ mode (default) 01 = 0V (V_{0P0_VSRC}) 10 = 0.6V (V_{0P6_VSRC}) 11 = 3.3V (V_{3P3_VSRC}) Note: The bit configurations are invalid during BC1.2 detection.	Hard-reset or VUSB REMOVE
D[1]	DPDM_DAC_EN	0	R/W	Enable Bit of DP/DM DAC 0 = Disabled (default) 1 = Enabled	Hard-reset or VUSB REMOVE
D[0]	Reserved	0	R	Reserved	N/A

REG0xA8: USB_STAT Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	Reserved	0	R	Reserved	N/A
D[6:4]	USB_DEVICE_STAT[2:0]	000	R	Status Bit of USB BC1.2 Device Detection 000 = No Input 001 = BC1.2 detection in progress 010 = SDP device detected 011 = Non-standard adapter detected 100 = DCP device detected 101 = CDP device detected 110 ~ 111 = Reserved	Hard-reset
D[3:1]	Reserved	000	R	Reserved	N/A
D[0]	DCD_TIMEOUT_FLAG	0	RC	BC1.2 DCD Timeout Fault flag 0 = No BC1.2 DCD timeout fault 1 = BC1.2 DCD timeout fault has ever occurred. Generate an interrupt on nINT pin. Read this bit to reset it to 0.	Hard-reset

APPLICATION INFORMATION

Input Capacitors (C_{VUSB}, C_{VBUS} and C_{PMID})

Input capacitors are selected by considering two main factors:

1. Adequate voltage margin above maximum surge voltage;
2. Not too large voltage margin in order to limit the peak currents drawn from the source and reduce the input noise.

For C_{VUSB}, use a 1μF/25V ceramic capacitor with low ESR placed close to the VUSB and PGND pin; For C_{VBUS}, use a 10μF/25V ceramic capacitor with low ESR placed close to the VBUS and PGND pin. The C_{PMID} are determined by the minimum capacitance needed for stable operation and the required ESR to minimize the voltage ripple and load step transients. Typically, two 10μF/35V or larger X5R ceramic capacitors are sufficient to meet the C_{PMID} requirements of two channels. Consider the DC bias derating of the ceramic capacitors. The X5R and X7R capacitors are relatively stable against DC bias and high temperature. Note that the bias effect is more severe with smaller package sizes, so choose the largest affordable package size. Also consider a large margin for the voltage rating for the worst-case transient input voltages.

External OVPFETs (Q_{USB})

The maximum recommended input range is 21V. If the supplied VUSB voltage is above 21V, two sets of back-to-back N-CH OVPFETs are recommended between the adapter inputs and the SGM41612YGA. Choose a low R_{DSON} MOSFET for the OVPFET to minimize power losses.

Flying Capacitors C_{FLY} ($C_{F3A/B}$, $C_{F2A/B}$, $C_{F1A/B}$)

For selection of the C_{FLY} capacitors, the current rating, ESR and the bias voltage derating are critical parameters. The C_{FLY} capacitors are biased to different DC voltages according to the operation mode. To trade-off between efficiency and power density, set the C_{FLY} voltage ripple to the 2% of its DC bias voltage as a good starting point. The C_{FLY} for each phase can be calculated by Equation 1:

$$C_{FLY} = \frac{I_{BAT}}{8 f_{SW} V_{CFLY_RPP}} = \frac{I_{BAT}}{16\% f_{SW} V_{DC_CFLY}} \quad (1)$$

where I_{BAT} is the charging current and V_{CFLY_RPP} is the peak-to-peak voltage ripple of the C_{FLY}.

Choosing a too small capacitor for C_{FLY} results in lower efficiency and high output voltage/current ripples. However choosing a too large C_{FLY} only provides minor efficiency and output ripple improvements.

The default switching frequency is f_{SW} = 600kHz. It can be adjusted by FSW_SET[4:0] bits in REG0x0C. Lower frequency increases efficiency by reducing switching losses but requires larger capacitance to maintain low output ripple and low output impedance. An optimum switching frequency can be found for any selected C_{FLY} capacitor to minimize losses. Typically three 22μF, X5R or better grade ceramic capacitors placed close to the CTxy (x = 1, 2, 3, y = A or B) and CBxy pins provide stable performance of two channels.

Output Capacitor (C_{VOUT})

C_{VOUT} selection criteria are similar to the C_{FLY} capacitor. Larger C_{VOUT} value results in less output voltage ripple, but due to the dual-phase operation, the C_{VOUT} RMS current is much smaller than C_{FLY}, so smaller capacitance value can be chosen for C_{VOUT} as given in Equation 2:

$$C_{VOUT} = \frac{I_{BAT} \times t_{DEAD}}{0.5 \times V_{VOUT_RPP}} \quad (2)$$

where t_{DEAD} is the dead time between the two phases and V_{VOUT_RPP} is the peak-to-peak output voltage ripple and is typically set to the 2% of V_{OUT}.

C_{VOUT} is biased to the battery voltage and its nominal value should be derated for battery voltage DC bias. Typically three 10μF, X5R or better grade ceramic capacitors placed close to the VOUT and PGND pins provide stable performance of two channels.

External Bootstrap Capacitor (C_{BTSA}, C_{BTSB} and C_{BTS2})

The bootstrap capacitors provide the gate driver supply voltage for the internal switches. It is recommended that place a 220nF low ESR ceramic capacitor between BTS2 and VOUT pin, and two 100nF low ESR ceramic capacitors between BTSA and CT3A pin and between BTSB and CT3B pin respectively.

APPLICATION INFORMATION (continued)

PCB Layout Guidelines

A good PCB layout is critical for stable operation of the SGM41612YGA. Follow these guidelines for the best results:

1. Use short and wide traces for VBUS as it carries high current.
2. Minimize connectors wherever possible. Connector losses are significant especially at high currents.
3. Use solid thermal vias for better thermal relief.
4. Bypass VBUS, PMID and VOUT pins to PGND with ceramic capacitors as close to the device pins as possible.
5. Place C_{FLY} capacitors as close as possible to the device with small pad areas to reduce switching noise and EMI.
6. Use wider copper plane to reduce the connection resistance for C_{FLY} capacitors.
7. Connect or reference all quiet signals to the AGND pin.
8. Connect and reference all power signals to the PGND pins (preferably the nearest ones).
9. Try not to interrupt or break the power planes by signal traces.

The recommended layout is shown in Figure 13.

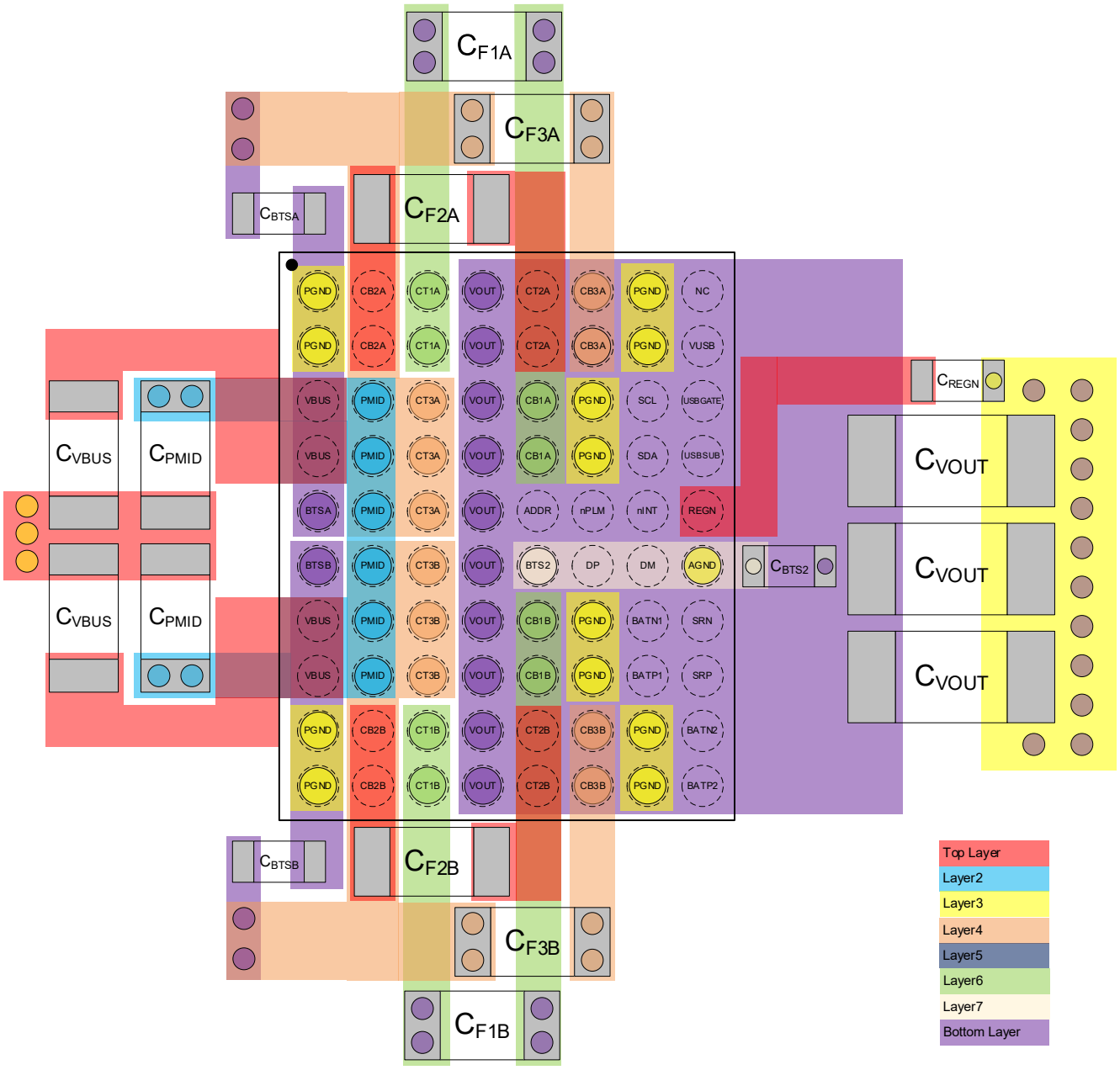


Figure 13. PCB Layout Reference

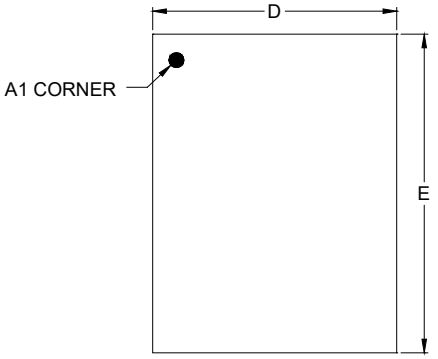
REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

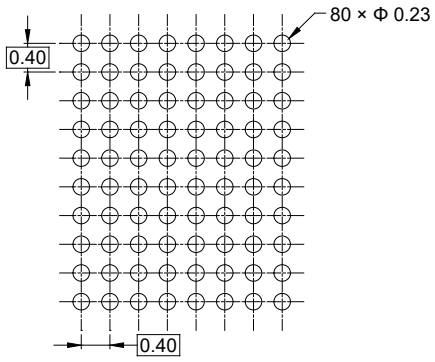
Changes from Original to REV.A (NOVEMBER 2026)	Page
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

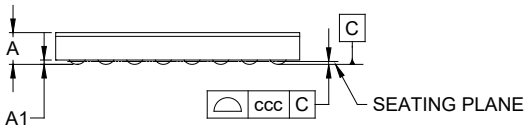
WLCSP-3.4×4.44-80B-A



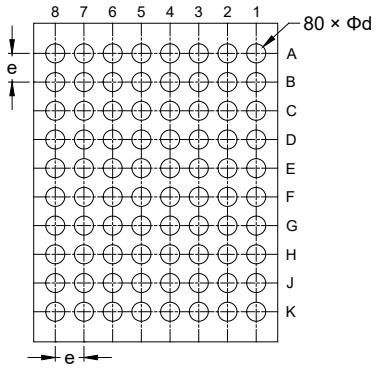
TOP VIEW



RECOMMENDED LAND PATTERN (Unit: mm)



SIDE VIEW



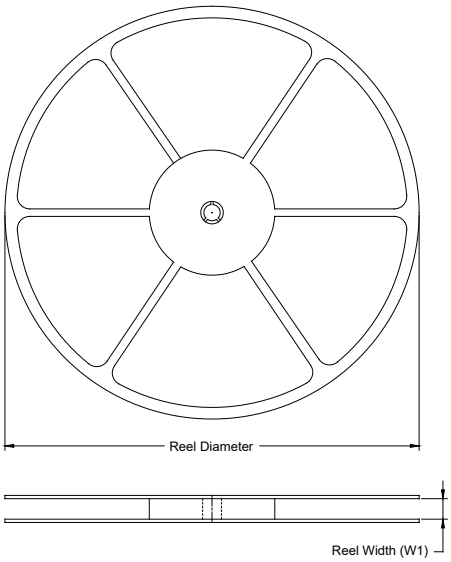
BOTTOM VIEW

Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	-	-	0.463
A1	0.054	-	0.066
D	3.370	-	3.430
E	4.410	-	4.470
d	0.235	-	0.295
e	0.400 BSC		
ccc	0.050		

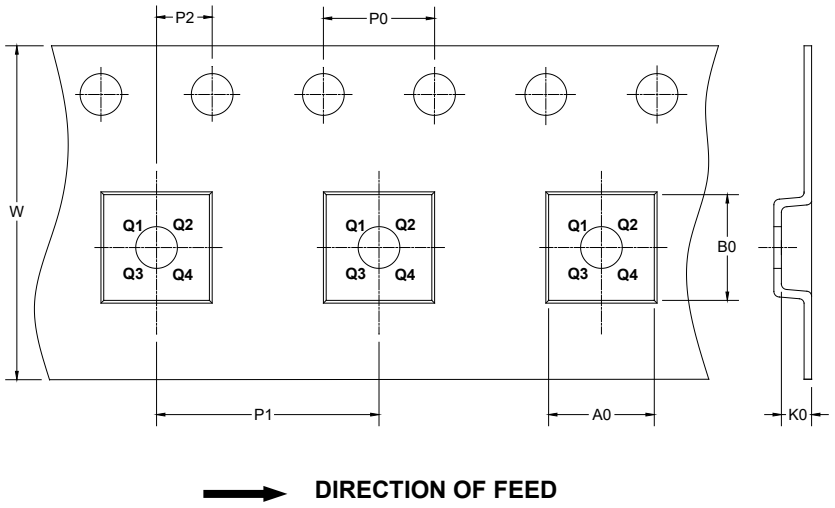
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



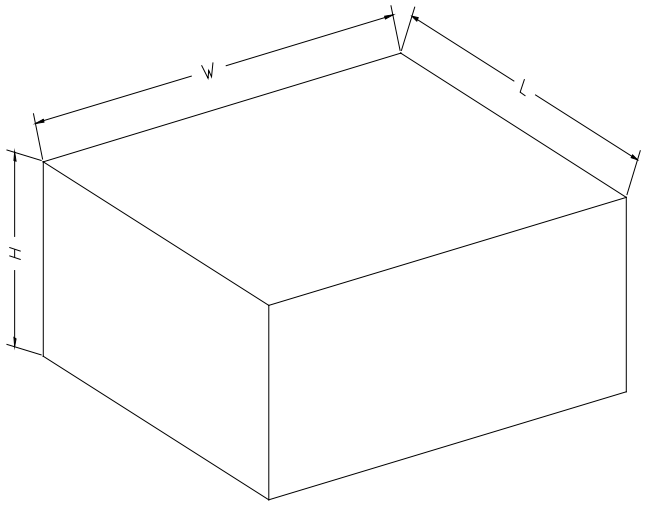
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
WLCSP-3.4×4.44-80B-A	7"	12.4	3.70	4.70	0.70	4.0	8.0	2.0	12.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18

DD0002