SGM25715
Negative Hot-Swap/Inrush Current Controller with Power Limiting

GENERAL DESCRIPTION

The SGM25715 negative hot-swap controller features highly robust system protection capabilities, rendering it suitable for hot-swap applications involving live power supplies or other energized systems.

The SGM25715 supports inrush current control to limit voltage droop and transients in the system. It features programmable current limiting and power limiting functions, ensuring the external series N-Channel MOSFET operates within its Safe Operating Area (SOA). The SGM25715 provides comprehensive circuit protection and indication functions. It monitors the external MOSFET for over-current and over-voltage conditions. The under-voltage lockout, over-voltage lockout and fault detection time are all programmable.

The PGD pin indicates whether the device is in a normal operating state by comparing the input and output voltages. If a fault condition occurs, the internal fault detection timer is activated. Upon timer expiration, the SGM25715L latches off, and the SGM25715R restarts following a fixed duty cycle period.

The SGM25715 is available in a Green MSOP-10 package.

SIMPLIFIED SCHEMATIC

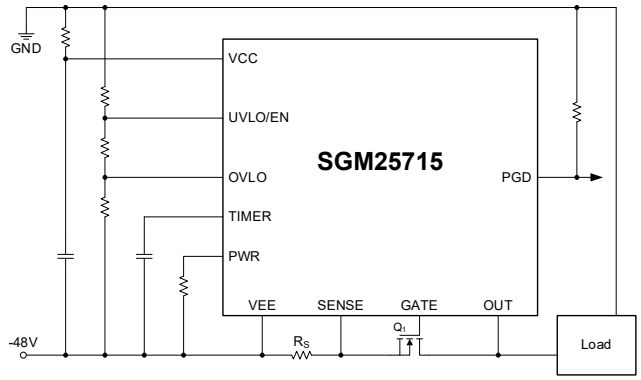


Figure 1. Simplified Schematic

FEATURES

- **-9V to -80V Operating Voltage Range**
- **Inrush Current Control for Hot Swapping of Live Equipment**
- **Programmable Power Limiting Function for the External MOSFET**
- **Adjustable Current Limit**
- **Circuit Breaker Protection against for Severe Over-Current Events**
- **Adjustable Under-Voltage Lockout and Over-Voltage Lockout**
- **Initial Insertion Timer Provides Time for the Input to Recover and Stabilize after Device Connection**
- **Programmable Fault Timer Prevents Nuisance Trips**
- **Active High Open-Drain Power Good Output**
- **Available in Fault Latch and Auto-Restart Versions**
- **Available in a Green MSOP-10 Package**

APPLICATIONS

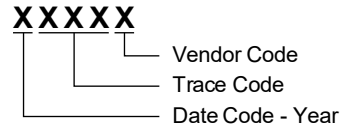
Solid State Circuit Breaker
Inrush Current Limiting
Solid State Relay
Under-Voltage Lockout
Transient Voltage Protector
Server Backplane System
Power Good Detector and Indicator

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM25715L	MSOP-10	-40℃ to +125℃	SGM25715LXMS10G/TR	SGM2KZ XMS10 XXXXX	Tape and Reel, 4000
SGM25715R	MSOP-10	-40℃ to +125℃	SGM25715RXMS10G/TR	SGM2L0 XMS10 XXXXX	Tape and Reel, 4000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Input Voltage:
- OUT, PGD to VEE ..... -0.3V to 100V
- UVLO, OVLO to VEE ..... -0.3V to 17V
- SENSE to VEE ..... -0.3V to 0.3V

Current:
- Into VCC (100μs Pulse) ..... 100mA (MAX)

Package Thermal Resistance
- MSOP-10, θ_{JA} ..... 133.1℃/W
- MSOP-10, θ_{JB} ..... 80.7℃/W
- MSOP-10, θ_{JC} ..... 47.2℃/W

Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility (1) (2)
HBM ..... ±4000V
CDM ..... ±1000V

NOTES:

1. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.

2. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

RECOMMENDED OPERATING CONDITIONS

Current into VCC ..... 2mA (MIN)
OUT Voltage above VEE ..... 0V to 80V
PGD Off Voltage above VEE ..... 0V to 80V
Operating Junction Temperature Range ..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

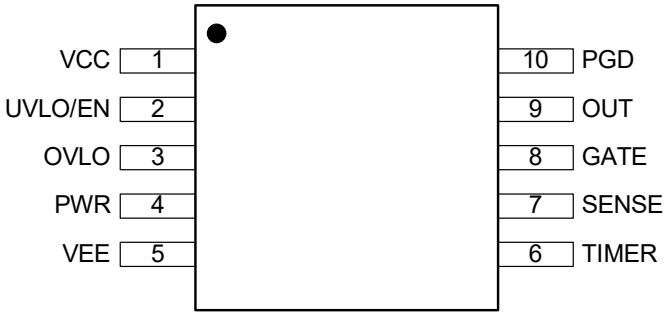
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

(TOP VIEW)



MSOP-10

PIN DESCRIPTION

PIN	NAME	TYPE	FUNCTION
1	VCC	I	Positive Supply Input. Use a resistor to connect to system ground, and place a bypass capacitor between VEE and this pin. The internal Zener diode maintains voltage stability from VCC to VEE, with a nominal value of 13V.
2	UVLO/EN	I	Under-Voltage Lockout. The UVLO threshold is set by an external resistor divider connected to the system input voltage. The enable threshold at the pin is 2.5V relative to VEE. The hysteresis is supplied by an internal 20μA current source. This pin supports remote enable and disable functions.
3	OVLO	I	Over-Voltage Lockout. The OVLO threshold is set by an external resistor divider connected to the system input voltage. The disable threshold at the pin is 2.5V relative to VEE. The hysteresis is supplied by an internal 20μA current source.
4	PWR	I	Power Limit Set. The external resistor on this pin, together with the current sense resistor (R_S), programs the maximum power dissipation of the external MOSFET.
5	VEE	I	Negative Supply Pin. It should be connected to the system's negative voltage source, typically -48V.
6	TIMER	I/O	Timing Capacitor. Connect a capacitor between this pin and VEE which determines the initial insertion time and the fault detection time. This capacitor also determines the fault restart time of SGM25715R.
7	SENSE	I	Current Sense Input. Over-current is detected by sensing the voltage across the current sense resistor (R_S) from VEE to this pin. When this voltage reaches 50mV, the current limiting function is activated, and the fault timer starts counting.
8	GATE	O	Gate Drive Signal. Connect this pin to the gate of the MOSFET to control its switching.
9	OUT	I	Output Feedback. The voltage at this pin is used to determine the V_{DS} of the MOSFET for power limiting. It is also used to control the PGD voltage.
10	PGD	O	Power Good Indicator. Open-drain output that can withstand 80V in the off-state. The PGD pin goes high when the MOSFET V_{DS} drops below 1.2V, and goes low when V_{DS} rises above approximately 2.42V.

NOTE: I = input, O = output, I/O = input/output.

ELECTRICAL CHARACTERISTICS

(T_J = -40℃ to +125℃, I_{CC} = 2mA, OUT pin = 48V above VEE, all voltages are with respect to VEE, typical values are measured at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input						
Operating Voltage, VCC - VEE	V_Z	I_{CC} = 2mA, UVLO = 5V	12.5	13	13.5	V
Internal Operating Current, Enabled	I_{CC_EN}	VCC - VEE = 11V, UVLO = 5V		0.23	0.35	mA
Internal Operating Current, Disabled	I_{CC_DIS}	VCC - VEE = 11V, UVLO = 2V		53	80	μA
Initial Insertion Timer Start Threshold Voltage	POR_{IT}	VCC - VEE increasing		7.6	8	V
All Functions Enable Threshold Voltage	POR_{EN}	VCC - VEE increasing		8.4	8.7	V
POR_{EN} Hysteresis	POR_{EN_HYS}	VCC - VEE decreasing		115		mV
OUT Pin						
OUT Bias Current, Enabled	I_{OUT_EN}	OUT = VEE, normal operation		0		μA
OUT Bias Current, Disabled	I_{OUT_DIS}	Disabled, OUT = VEE + 48V		0.1		μA
SENSE Pin						
SENSE Bias Current, Enabled	I_{SNS_EN}	OUT = VEE, normal operation		-4		μA
SENSE Bias Current, Disabled	I_{SNS_DIS}	Disabled, OUT = VEE + 48V		0		μA
UVLO, OVLO Pins						
UVLO Threshold	$UVLO_{TH}$		2.44	2.5	2.58	V
UVLO Hysteresis Current	$UVLO_{HYS}$	UVLO = VEE + 2V	10	20	30	μA
UVLO Bias Current	$UVLO_{BIAS}$	UVLO = VEE + 5V			1	μA
OVLO Threshold	$OVLO_{TH}$		2.44	2.5	2.58	V
OVLO Hysteresis Current	$OVLO_{HYS}$	OVLO = VEE + 2.8V	-30	-20	-10	μA
OVLO Bias Current	$OVLO_{BIAS}$	OVLO = VEE + 2.4V			1	μA
Gate Control (GATE Pin)						
Source Current	I_{GATE}	Normal operation	-75	-55	-35	μA
Sink Current		UVLO < 2.5V	1.8	2.1	2.4	mA
		SENSE - VEE = 150mV or VCC - VEE < POR_{IT}, V_{GATE} = 5V	50	90	140	
Gate Output Voltage in Normal Operation	V_{GATE}	GATE - VEE voltage		V_Z		V
Current Limit						
Threshold Voltage	V_{CL}	SENSE - VEE voltage	46	50	54	mV
Circuit Breaker						
Threshold Voltage	V_{CB}	SENSE - VEE voltage	80	100	120	mV
Power Limit (PWR Pin)						
Power Limit Sense Voltage (SENSE - VEE)	PWR_{LIM}	OUT - SENSE = 24V, R_{PWR} = 75kΩ	18	22	26	mV
PWR Pin Current	I_{PWR}	V_{PWR} = 2.5V		23		μA

ELECTRICAL CHARACTERISTICS (continued)

(T_J = -40℃ to +125℃, I_{CC} = 2mA, OUT pin = 48V above VEE, all voltages are with respect to VEE, typical values are measured at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Timer (TIMER Pin)						
Upper Threshold	V_{TMRH}		3.88	4	4.12	V
Lower Threshold	V_{TMRL}	Restart cycles (SGM25715R)	1.2	1.25	1.3	V
		End of 8th cycle (SGM25715R)		0.3		
		Re-enable threshold (SGM25715L)		0.3		
Insertion Time Current	I_{TIMER}	TIMER pin = 2V	-9	-6.1	-3.2	μA
End of Insertion Time Sink Current		TIMER pin = 2V	1.3	1.6	1.9	mA
Fault Detection Time Current		TIMER pin = 2V	-115	-95	-75	μA
Fault Sink Current			1.4	2.5	3.6	μA
Fault Restart Duty Cycle	DC_{FAULT}	SGM25715R		0.5		%
Power Good (PGD Pin)						
Threshold Measured at OUT - SENSE	PGD_{TH}	Decreasing	0.95	1.2	1.45	V
		Increasing, relative to decreasing threshold	0.94	1.22	1.5	
Output Low Voltage	PGD_{VOL}	I_{SINK} = 2mA		60	120	mV
Off Leakage Current	PGD_{IOH}	V_{PGD} = 80V			1	μA

NOTE: 1. Negative values indicate current flowing out of a pin.

SWITCHING CHARACTERISTICS

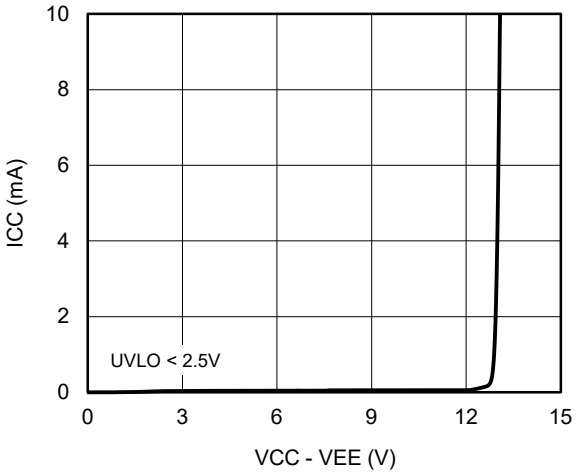
(T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
UVLO, OVLO Pins						
UVLO Delay Time	$UVLO_{DEL}$	Delay to GATE high		31		μs
		Delay to GATE low		14		
OVLO Delay Time	$OVLO_{DEL}$	Delay to GATE high		31		μs
		Delay to GATE low		14		
Current Limit						
Response Time	t_{CL}	SENSE - VEE stepped from 0mV to 80mV		1		μs
Circuit Breaker						
Response Time	t_{CB}	SENSE - VEE stepped from 0mV to 150mV, time to GATE low, no load		0.16	1.5	μs
Timer (TIMER Pin)						
Fault to GATE Low Delay	t_{FAULT}	TIMER pin reaches 4V		1		μs

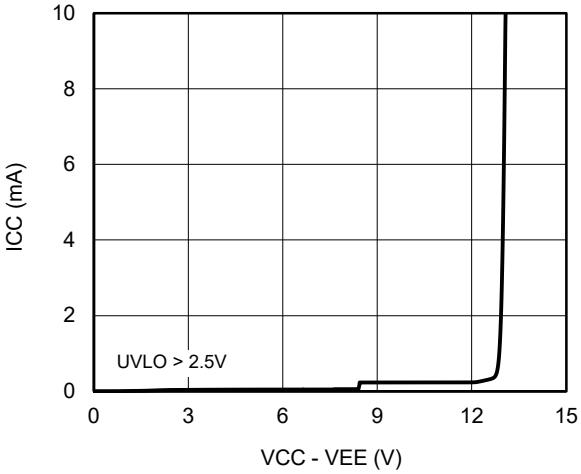
TYPICAL PERFORMANCE CHARACTERISTICS

T_J = +25℃, unless otherwise noted.

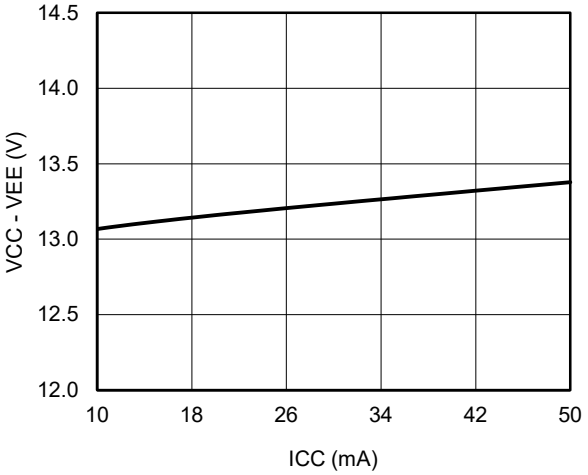
ICC vs. Operating Voltage - Disabled



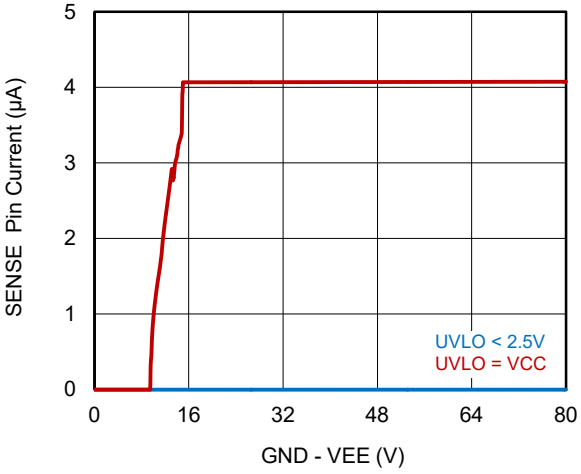
ICC vs. Operating Voltage - Enabled



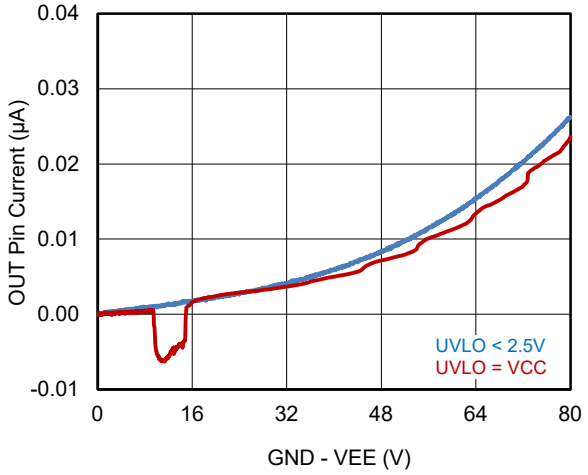
Operating Voltage vs. ICC



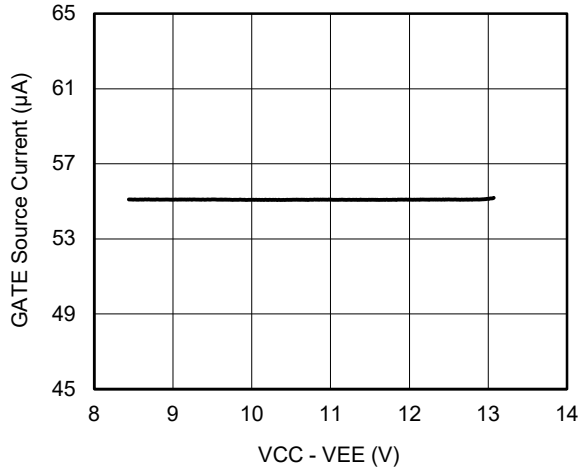
SENSE Pin Current vs. System Voltage



OUT Pin Current vs. System Voltage



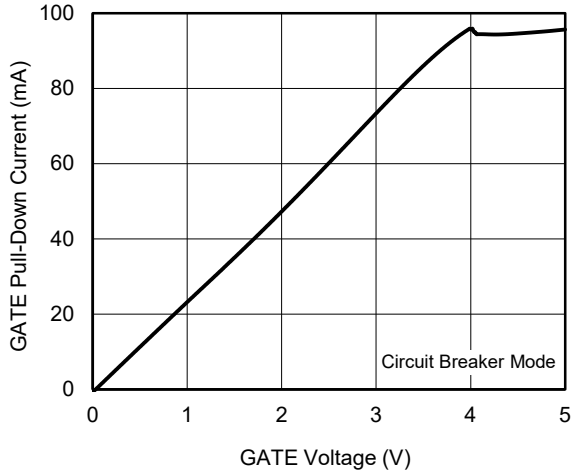
GATE Source Current vs. Operating Voltage



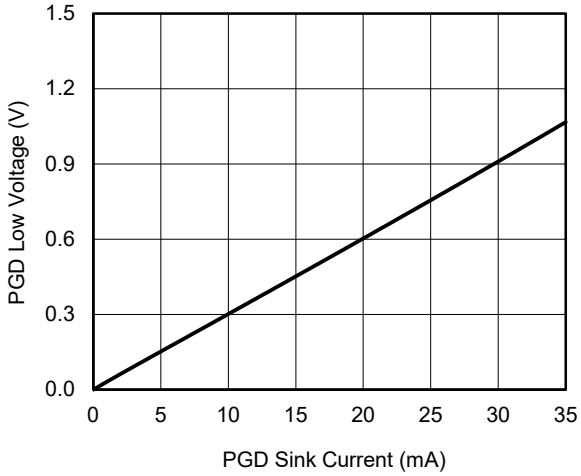
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_J = +25℃, unless otherwise noted.

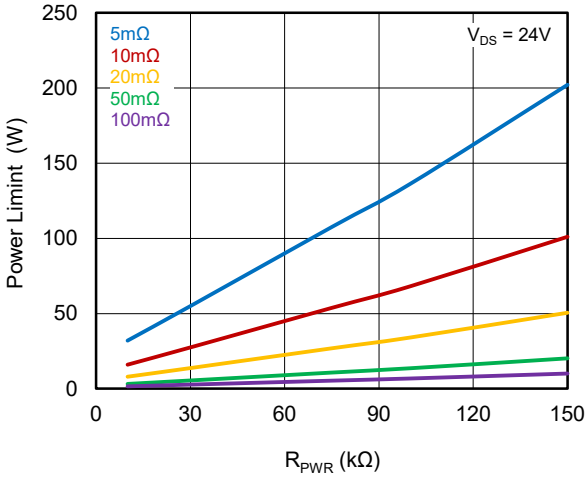
GATE Pull-Down Current, Circuit Breaker vs. GATE Voltage



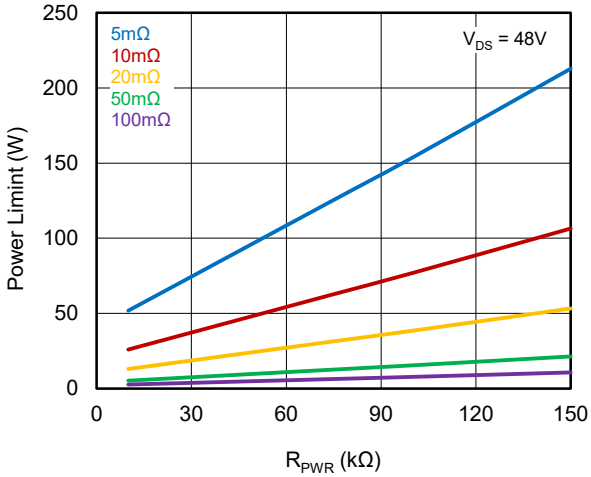
PGD Low Voltage vs. PGD Sink Current



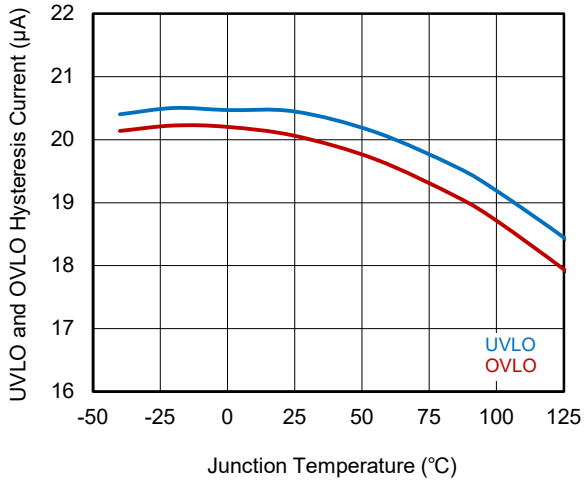
MOSFET Power Dissipation Limit vs. R_{PWR} and R_S (V_{DS} = 24V)



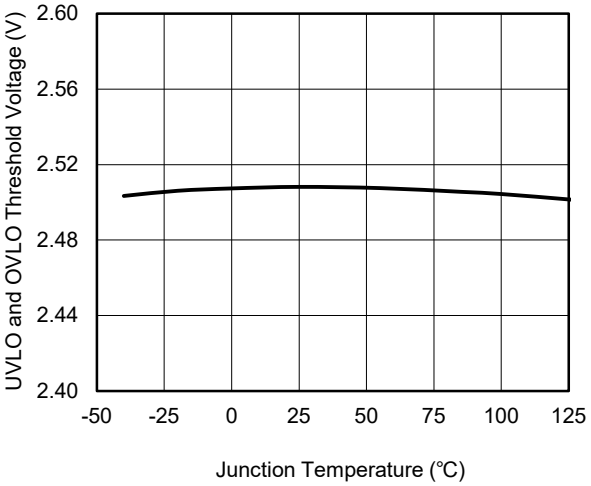
MOSFET Power Dissipation Limit vs. R_{PWR} and R_S (V_{DS} = 48V)



UVLO and OVLO Hysteresis Current vs. Junction Temperature



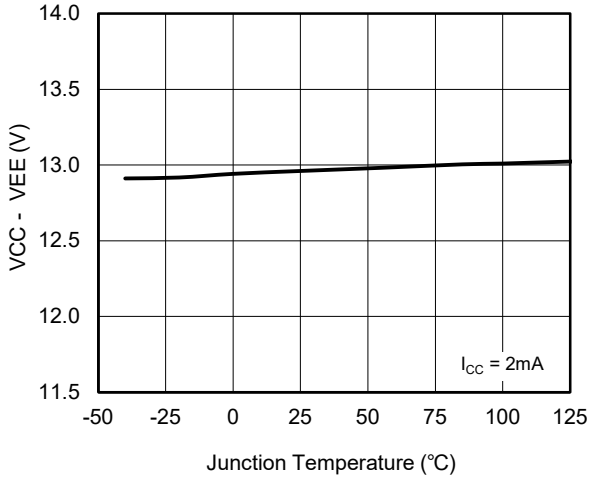
UVLO and OVLO Threshold Voltage vs. Junction Temperature



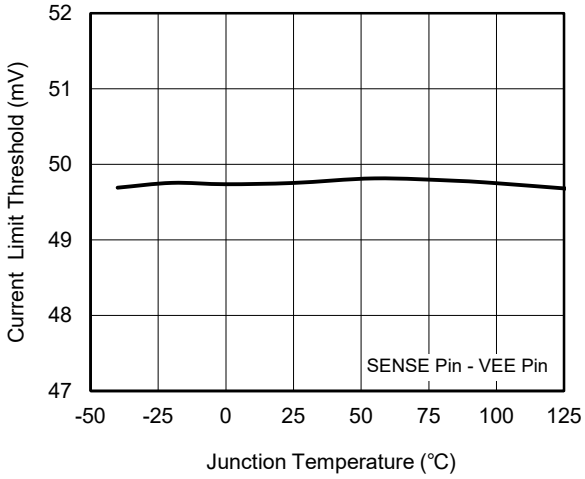
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_J = +25℃, unless otherwise noted.

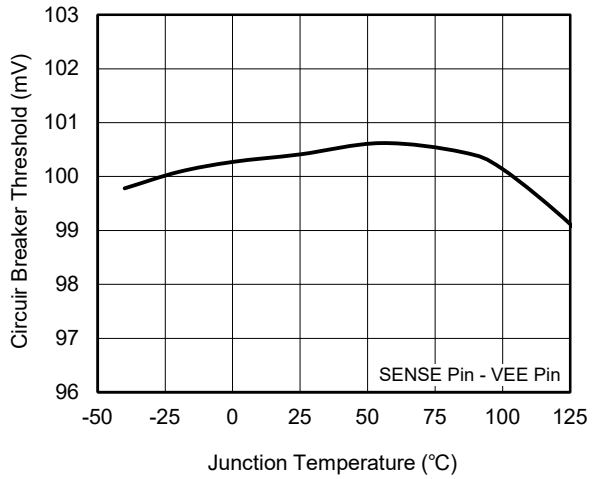
Operating Voltage vs. Junction Temperature



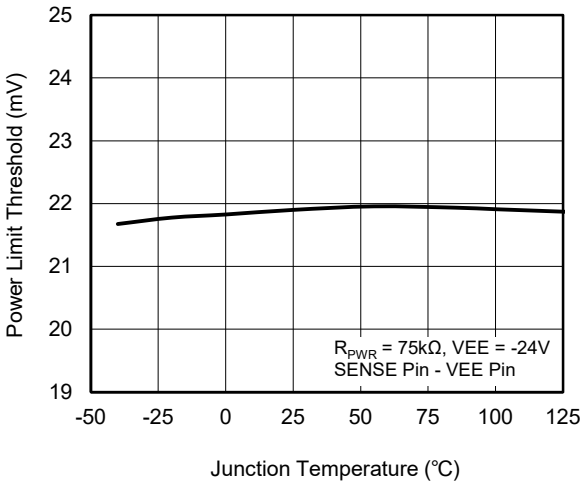
Current Limit Threshold vs. Junction Temperature



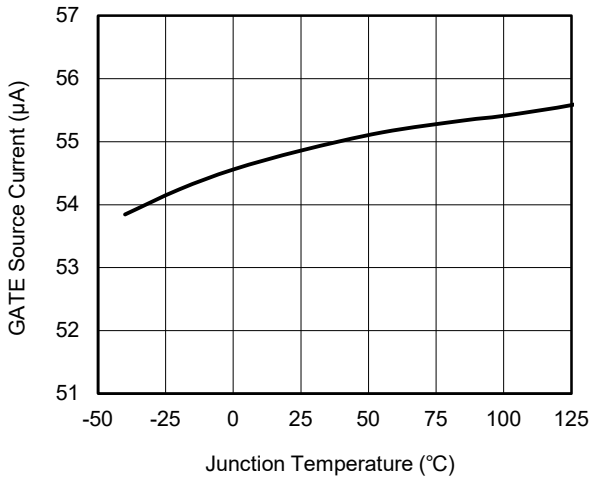
Circuit Breaker Threshold vs. Junction Temperature



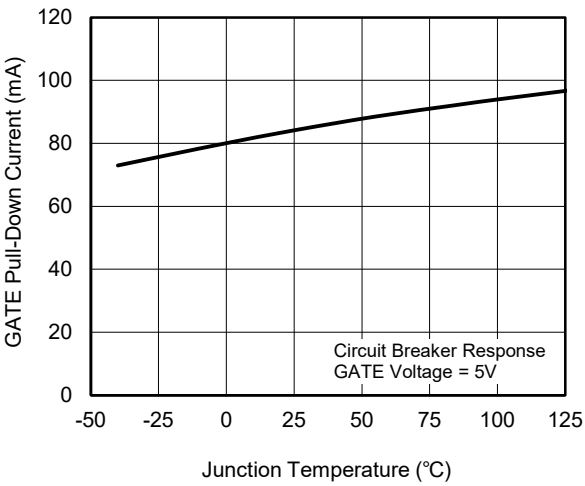
Power Limit Threshold vs. Junction Temperature



GATE Source Current vs. Junction Temperature



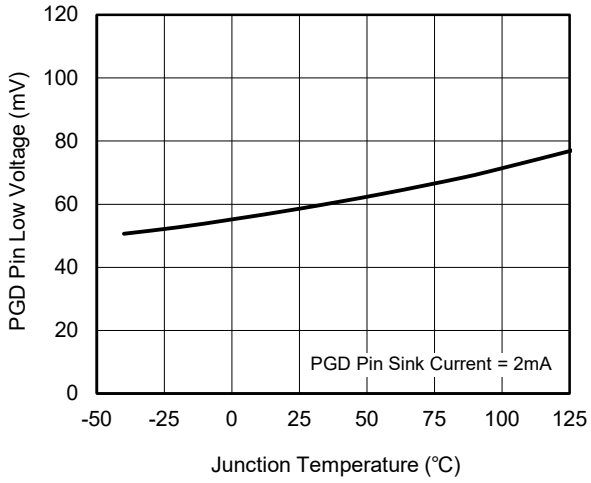
GATE Pull-Down Current, Circuit Breaker vs. Junction Temperature



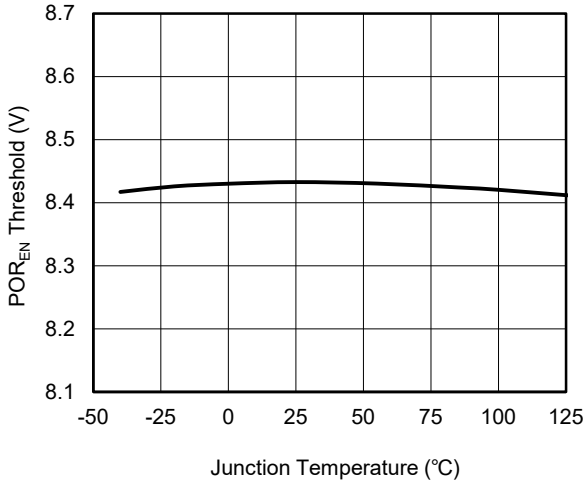
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_J = +25℃, unless otherwise noted.

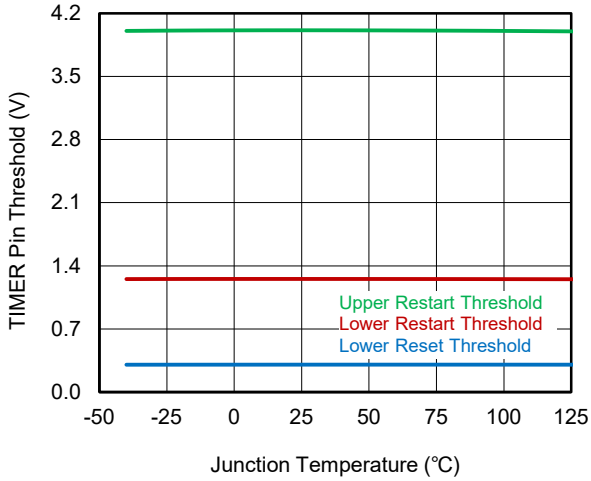
PGD Pin Low Voltage vs. Junction Temperature



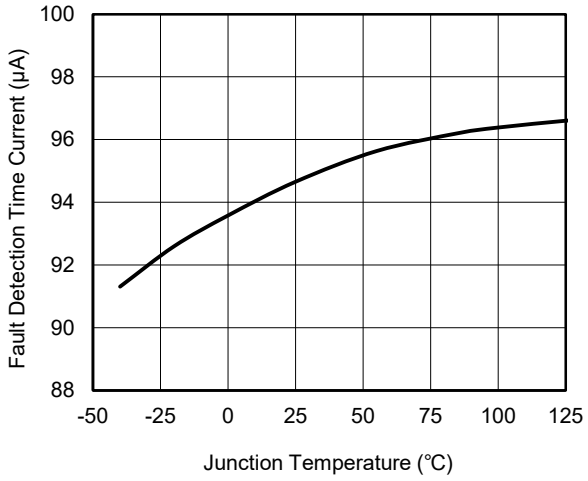
POR_{EN} Threshold vs. Junction Temperature



TIMER Pin Threshold vs. Junction Temperature



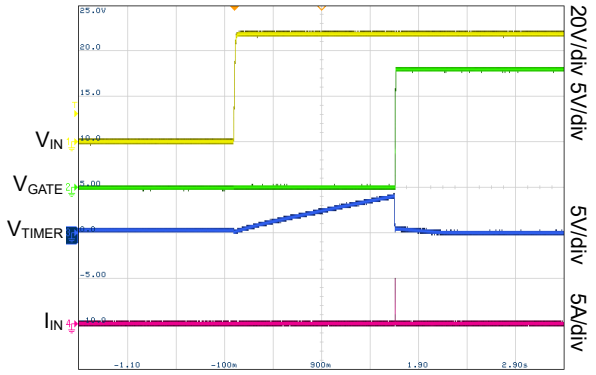
TIMER Pin Fault Detection Current vs. Junction Temperature



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

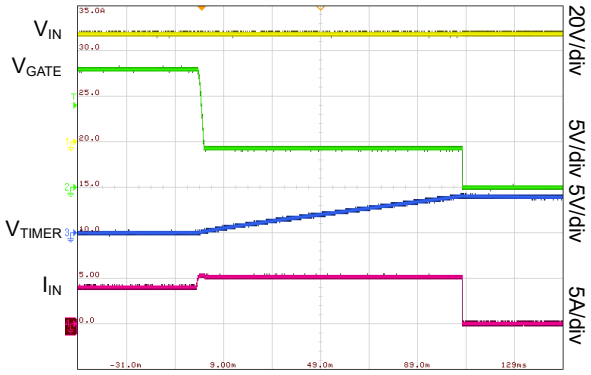
T_A = +25℃, V_{IN} = 48V, R_{PWR} = 75kΩ, R_S = 10mΩ, C_T = 2.2μF. The version used in the test is SGM25715R.

Insertion Delay



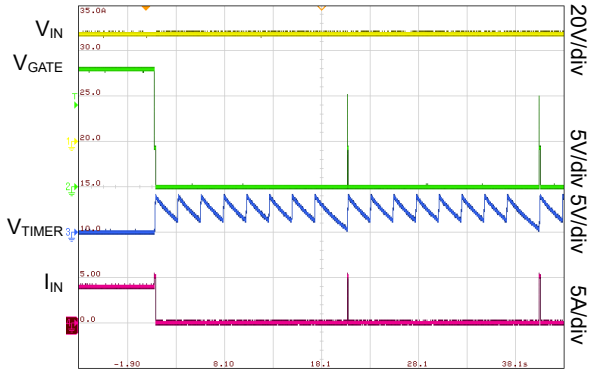
Time (500ms/div)

Overload during Steady State



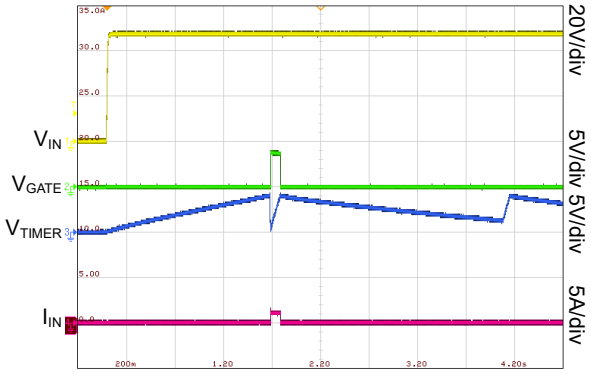
Time (20ms/div)

Overload with Retry



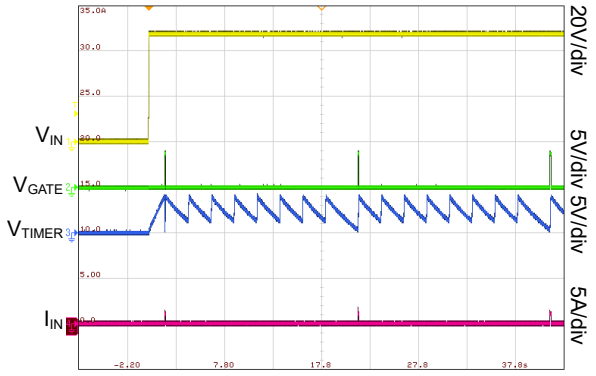
Time (5s/div)

Power into Short



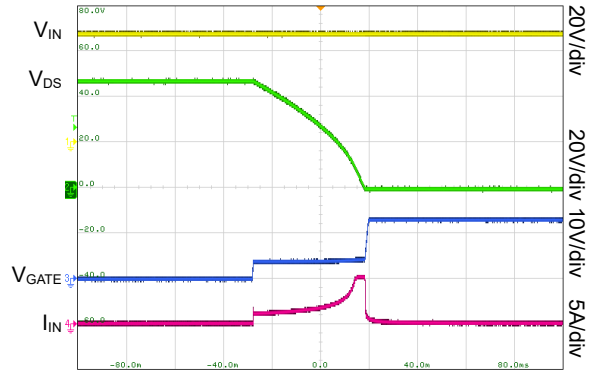
Time (500ms/div)

Power into Short Retry Zoomed Out



Time (5s/div)

Power Limited Startup

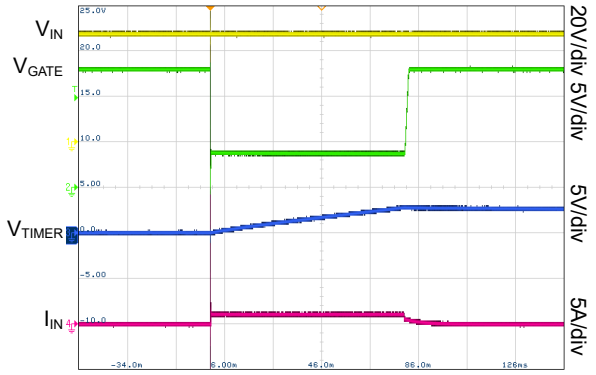


Time (20ms/div)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

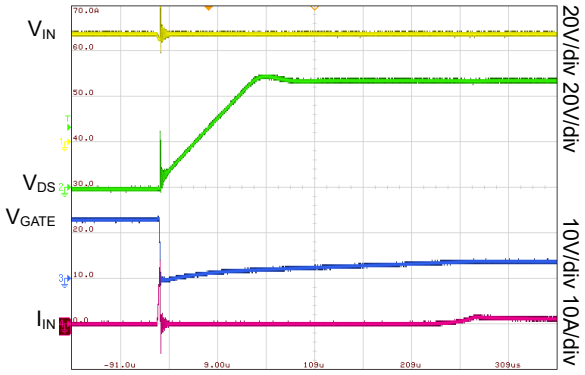
T_A = +25℃, V_{IN} = 48V, R_{PWR} = 75kΩ, R_S = 10mΩ, C_T = 2.2μF. The version used in the test is SGM25715R.

Short-Circuit and Release



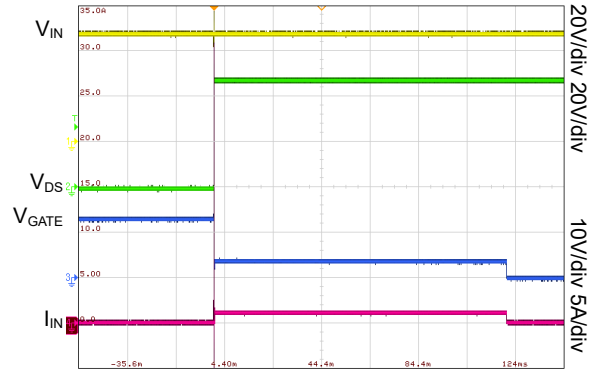
Time (20ms/div)

Short-Circuit Zoomed In



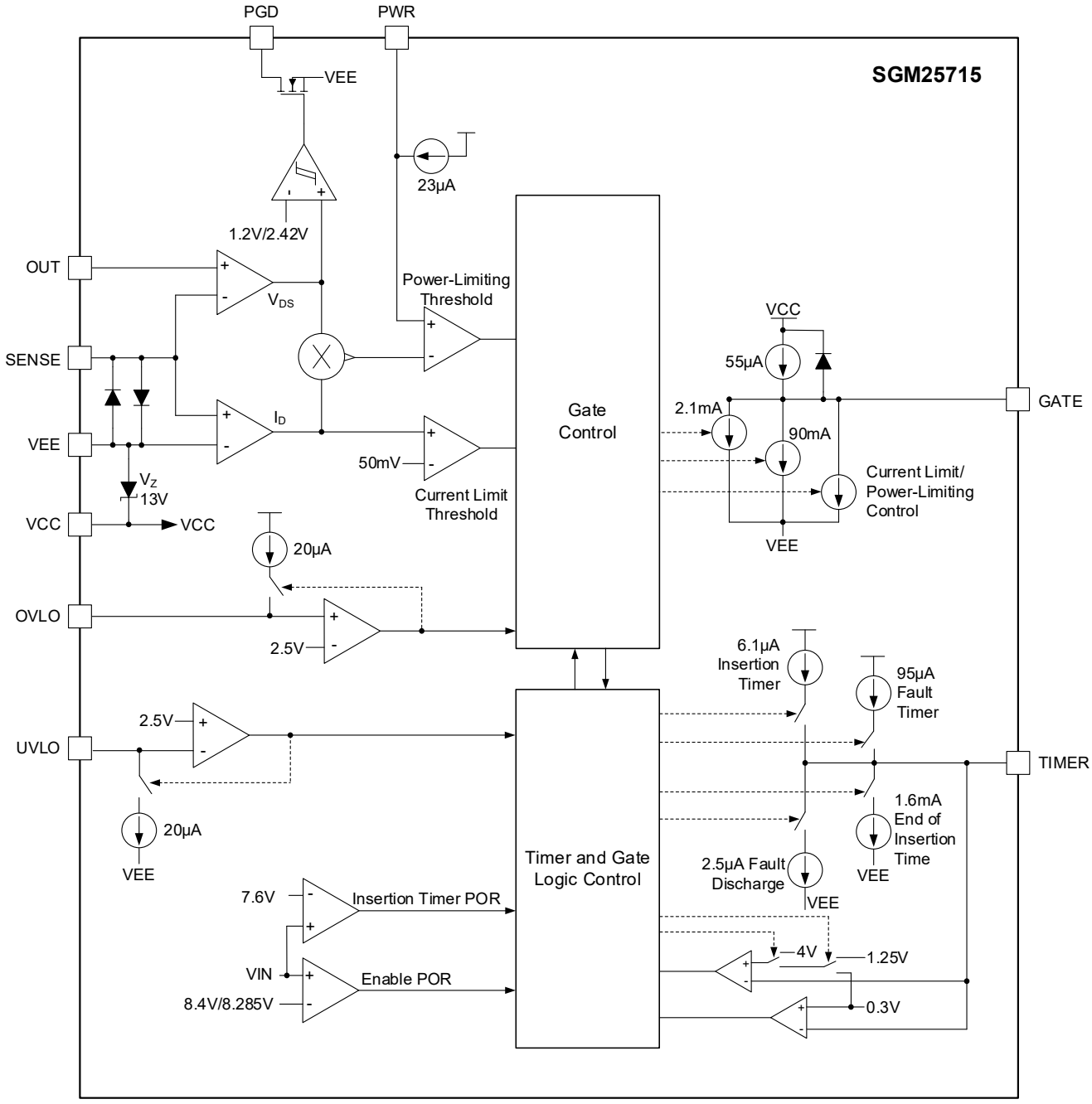
Time (50μs/div)

Short-Circuit Zoomed Out



Time (20ms/div)

FUNCTIONAL BLOCK DIAGRAM



NOTE: All voltages are with respect to VEE.

Figure 2. Block Diagram

DETAILED DESCRIPTION

Overview

The SGM25715 is designed to deliver protection for hot-swap operations of live powered equipment. The SGM25715 suppresses sudden supply voltage drops and excessive dV/dt of the load input by controlling the magnitude of load inrush current. This minimizes interference with other circuits within the system and prevents potential unintended resets. During system power up, the SGM25715 limits the maximum power dissipation and current of the series pass device to ensure the component operates within its Safe Operating Area (SOA). The SGM25715 evaluates operating conditions by monitoring the V_{DS} voltage and conducting current of the MOSFET. If the power/current limit exceeds the allowable time, the SGM25715 identifies a fault condition and shuts down the series pass MOSFET. Upon a fault occurrence, the SGM25715L latches off, and the SGM25715R automatically restarts after a predefined time interval. When severe faults such as output short circuits are detected, the SGM25715 activates its circuit breaker function to turn off the series MOSFET quickly. Device SGM25715 features a PGD pin to signal whether the VOUT has reached its nominal operating level. It integrates programmable under-voltage lockout (UVLO) and over-voltage lockout (OVLO) functions, which shut down the SGM25715 when the input voltage deviates outside the configured operating range. Figure 3 shows the typical configuration of SGM25715 for hot-swap protection.

The SGM25715 supports a wide range of applications beyond plug-in circuit boards. It can monitor overload current, provide transient surge protection, and ensure the load voltage within the desired operating range. Its integrated circuit breaker function protects the system from abrupt load short-circuit faults. The PGD output pin reports the status of the load voltage compared to the system input supply.

Feature Description

Power-Up Sequence

The V_{SYS} input voltage of SGM25715 is -9V to -80V, with a transient capability of -100V. Referring to the Figure 2, Figure 4, and Figure 10, before the operating voltage of the SGM25715 (VCC - VEE) rises from zero to the POR_{IT} threshold, GATE pin has an internal strong pull-down of 90mA to prevent inadvertent turn-on during the charging of the gate to drain capacitance of the external MOSFET (Q_1). When the operating voltage achieves the threshold, it will enter the insertion time, and the pull-down current of the GATE pin switches to 2.1mA. The function of the insertion time is to ensure that the ringing and transient of V_{SYS} reach stability before MOSFET operation. When the TIMER pin voltage exceeds VEE 4V, the insertion time ends and it rapidly discharges by an internal 1.6mA pull-down current. After the insertion time, when the operating voltage reaches the POR_{EN} threshold, the chip control circuit is enabled. The operating voltage will continue to increase with the system voltage until reaches the clamp voltage of the internal Zener diode (≈13V), so that an input resistor R_{IN} is necessary to bear the residual voltage.

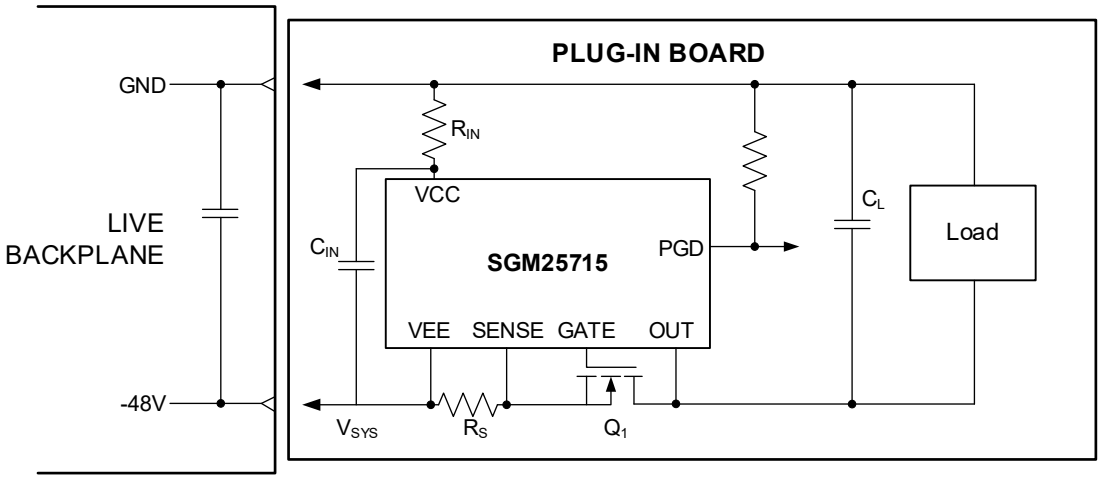


Figure 3. SGM25715 Application

DETAILED DESCRIPTION (continued)

When both V_{SYS} values exceed the UVLO threshold and the insertion delay period expires, the IC turns on Q_1. The GATE pin charges the gate capacitance of Q_1 with a 55μA current source. The gate-to-source voltage of Q_1 will eventually be charged to a voltage close to the operating voltage V_Z. During start-up, the SGM25715 continuously monitors the current flowing through Q_1 as well as its power dissipation. The inrush current limit and power limit loops regulate the source voltage of Q_1 to manage the output load current. When the current or power is limited, the timing capacitor C_T will also be charged. The PGD pin switches to a high logic level when the voltage between OUT pin and VEE pin reduces to within 1.2V.

If the SGM25715 stays in current limit or power limit operation until the timer pin voltage rises to 4V, it will determine that a fault has occurred and shut down Q_1. Specific instructions can be found in the Fault Timer and Restart section.

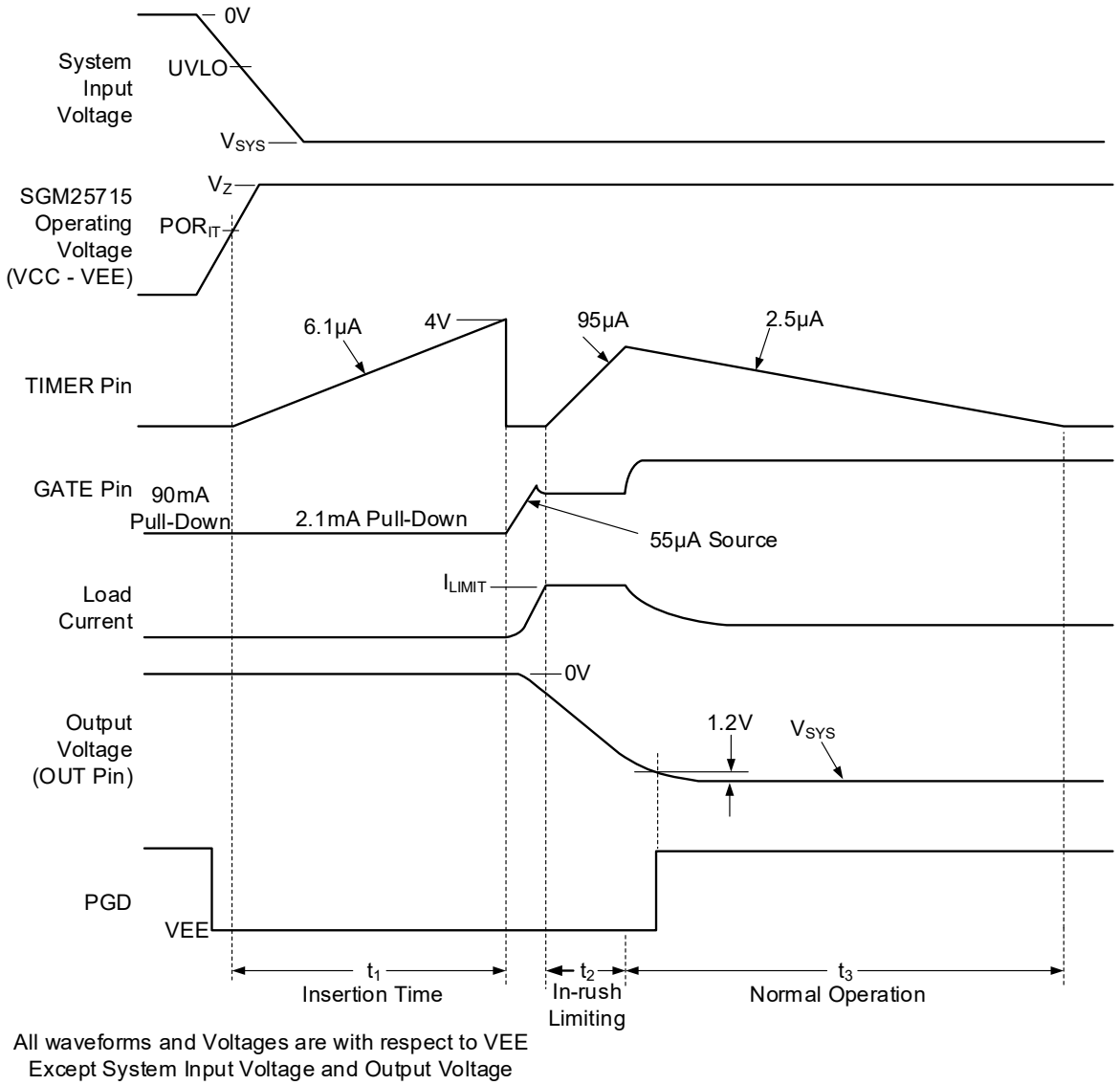


Figure 4. Power-Up Sequence (Current Limit Only)

DETAILED DESCRIPTION (continued)

Gate Control

The GATE pin is pulled down via a 90mA pull-down current until the operating voltage (VCC - VEE) reaches the POR_{IT} threshold. This pull-down current avoids spurious MOSFET turn-on caused by its drain-gate capacitance during the ramp-up of the system supply voltage.

The GATE pin sources 55μA to drive the MOSFET gate into conduction. Under steady-state conditions, the gate voltage is regulated to a voltage higher than VEE by about 13V, close to the VCC voltage. An additional Zener diode for voltage division needs to be added for driving MOSFET with a maximum drive voltage below 13V. The forward current rating of the external Zener diode shall be a minimum of 90mA.

If UVLO or OVLO fails to meet the turn-on conditions, the Q_1 will be turned off and the GATE pin will be pulled down by the internal 2.1mA current.

The time t_1 in the figure is the insertion time, in which a 2.1mA pull-down current clamps the GATE pin low to keep Q_1 off until the insertion time expires.

After the insertion time, during t_2, the SGM25715 modulates the gate voltage of Q_1 to restrict Q_1's current and power dissipation below the programmed limits. When current limit or power limit is activated, the voltage across the external capacitor on the TIMER pin rises continuously. When the fault condition is removed before the fault timer timeout threshold is achieved, the external timing capacitor begins discharging automatically.

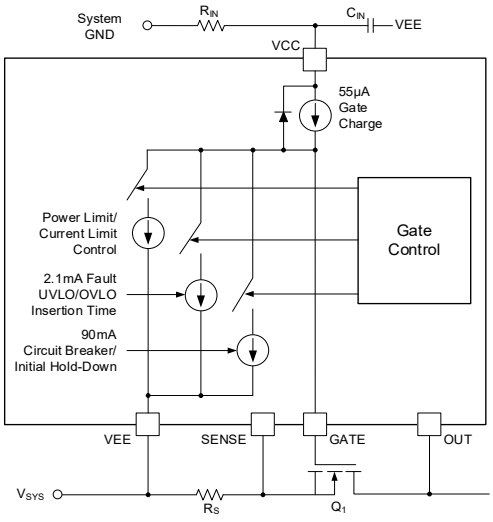


Figure 5. Gate Control

Current Limit

The SGM25715 begins to modulate the gate voltage of MOSFET Q_1 to implement current limiting once the voltage across SENSE and VEE rises to the 50mV current-limit threshold. Concurrently, the fault timer is triggered, refer to the Fault Timer and Restart section for details. When the SGM25715 exits the current limiting state before the voltage at the TIMER achieves 4V, the capacitance discharges and the SGM25715 returns to normal operation. For proper operation, the resistance value of R_S should not exceed 100mΩ.

Circuit Breaker

If the load current suddenly increases and causes the sensing resistor R_S voltage to exceed twice the current limit threshold (100mV), the SGM25715 will use a 90mA pull-down current to quickly discharge the GATE of the MOSFET, and the Fault Timeout Period will begin. When the voltage on the R_S drops below 100mV, the 90mA pull-down current is released, and the current or power limiting regulation circuit begins to operate.

Power Limit

The SGM25715 features a power dissipation limiting function for the MOSFET to maintain operation within the SOA rating. The SGM25715 determines whether the power consumption on Q_1 has reached the set threshold based on the voltage of the current sensing resistor R_S and the external MOSFET source drain voltage. When Q_1 power dissipation reaches the power limit threshold programmed by the resistor tied to the PWR pin, the GATE drive voltage is modulated to suppress Q_1 drain current. Concurrently, the Fault Timeout Period begins to count.

Fault Timer and Restart

When the SGM25715 triggers current or power limiting thresholds, two actions are taken. The GATE voltage is modulated to control the load current and power consumption of the external MOS, and the internal 95μA current source charges the external capacitor (C_T) at the TIMER pin. If the fault state is resolved before the C_T voltage reaches 4V, the SGM25715 will resume normal operation and the C_T will discharge through 2.5μA. If the timer pin voltage rises to 4V, Q_1 will be turned off by a 2.1mA pull-down current. The subsequent restart process varies depending on the SGM25715 version.

DETAILED DESCRIPTION (continued)

For SGM25715L, the MOSFET is turned off when the C_T voltage reaches 4V at the end of the Fault Timeout Period, and the C_T is discharged by a 2.5μA current sink. After the C_T voltage is discharged to below 0.3V, the latch state can be released by cycling the input power supply voltage (V_{SYS}) or briefly lowering and restoring the UVLO/EN voltage, as shown in Figure 6.

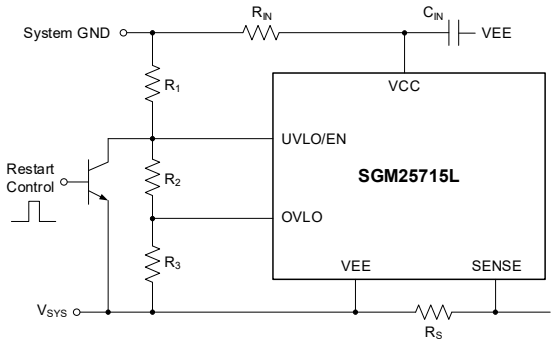


Figure 6. Latched Fault Restart Control

The SGM25715R integrates an auto-restart sequence. After the voltage of C_T achieves 4V, the TIMER pin voltage cycles between 4V and 1.25V for seven times, driven by a 95μA charging current and a 2.5μA discharge current, as shown in Figure 7. When the TIMER pin ramps down to 0.3V on the eighth falling ramp, the Q_1 turns on with a 55μA current source at the GATE pin. The Fault Timeout Period and auto-restart cycle will repeat if the fault condition continues.

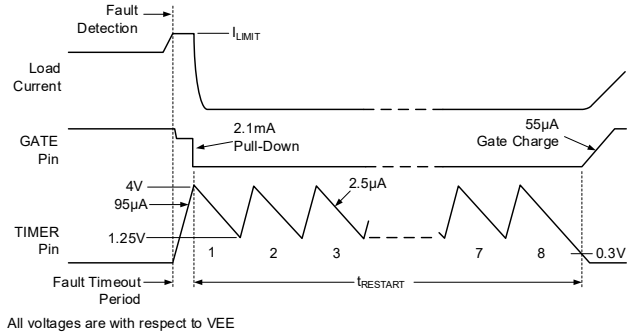


Figure 7. Restart Sequence (SGM25715R)

Under-Voltage Lockout (UVLO)

The operating range of the input voltage of the SGM25715 is determined by programmable under-voltage lockout (UVLO) and over-voltage lockout (OVLO). When in this working range, the series MOSFET will be turned on. Resistance voltage divider is a commonly used UVLO setting method, as shown in Figure 10.

When the UVLO/EN voltage is below the 2.5V threshold, a 20μA current sink at this pin will take effect and a 2.1mA pull-down current holds the gate voltage of Q_1. When the voltage rises to 2.5V above VEE, the 20μA UVLO/EN current sink deactivates, raising the pin voltage and providing hysteresis for UVLO.

Over-Voltage Lockout (OVLO)

The operating range of the input voltage of the SGM25715 is determined by programmable under-voltage lockout (UVLO) and over-voltage lockout (OVLO). When in this working range, the series MOSFET will be turned on. Resistance voltage divider is a commonly used OVLO setting method, as shown in Figure 10.

When the OVLO voltage is 2.5V above V_{SYS}, a 20μA current source at this pin will take effect, raising the pin voltage and providing hysteresis for OVLO. Meanwhile, a 2.1mA pull-down current holds the gate voltage of Q_1. When the voltage between OVLO and VEE reduces to less than 2.5V, the 20μA OVLO current source deactivates.

Power Good Pin

The Power Good output indicator pin (PGD) is an open-drain pin. This pin needs to be equipped with a pull-up resistor to limit the current. The PGD pin off-state voltage shall be positive relative to VEE, with a maximum steady-state rating of 80V above VEE and a 100V transient withstand voltage. At the completion of the turn-on sequence, PGD pulls high once the voltage across the external MOSFET (OUT to SENSE) falls below 1.2V. If the external MOSFET V_{DS} rises above 2.42V, or the system voltage exceeds the operating range set by UVLO and OVLO, or any fault condition is detected, PGD will switch to low level. If the operating voltage is less than 2V, the PGD output remains high.

DETAILED DESCRIPTION (continued)

Device Functional Modes

Shutdown/Enable Control

Figure 8 shows the method of implementing remote on/off control via the UVLO/EN pin. When the voltage of the UVLO/EN pin falls below the 2.5V threshold relative to VEE, the load current is shuts off. After the UVLO/EN pin returns to normal level, the SGM25715 turns on the external MOSFET Q_1 and activates inrush current limiting and power limiting functions.

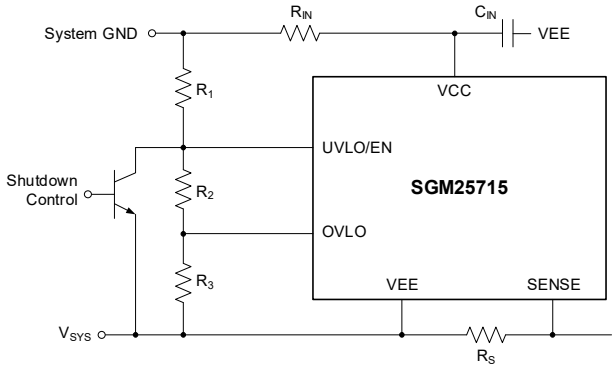


Figure 8. Shutdown/Enable with the UVLO/EN Pin

Figure 9 shows the method of implementing remote on/off control via the OVLO pin. If the transistor connected to the OVLO pin is turned off, the voltage of this pin will be higher than the 2.5V threshold relative to VEE, resulting in no load output. Once the external transistor conducts, the OVLO pin voltage drops below 2.5V, the SGM25715 resumes output and enables the inrush current limiting and power limiting functions.

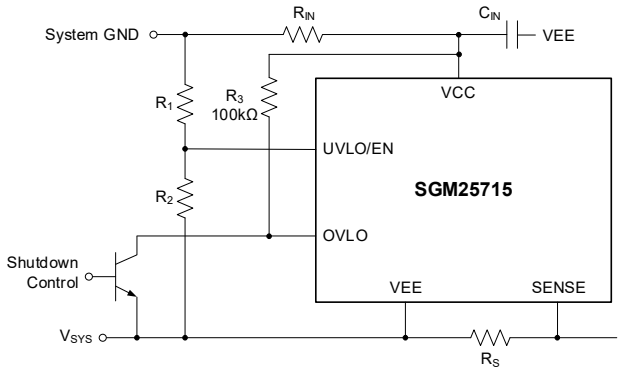


Figure 9. Shutdown/Enable with the OVLO Pin

APPLICATION INFORMATION

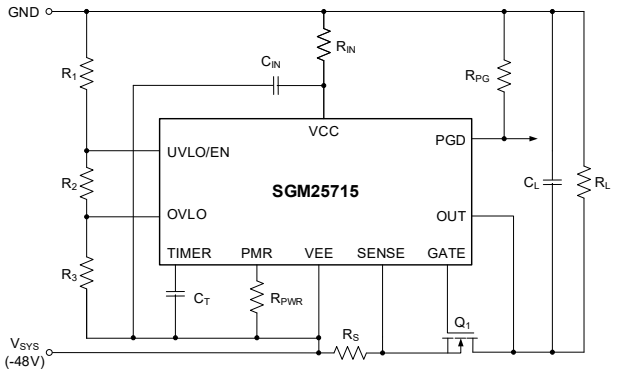


Figure 10. Basic Application Circuit

Application Information

The SGM25715 is a hot-swap controller which is used to manage inrush current and provide fault protection. Three critical operating scenarios need to be taken into account during hot-swap circuit design:

- Startup process, especially for scenarios with large output capacitance or heavy loads.
- Power-up under output short-circuit condition.
- Output short-circuit during normal operation.

The SGM25715 is a hot-swap controller that protects hot-swap MOSFET by limiting load current and power. In order to ensure that the series pass MOSFET can operate within the SOA under the above operating conditions, it is necessary to design the circuit reasonably. The following section provides a complete design process for reference.

Detailed Design Procedure

Choose R_{IN}, C_{IN}

When the system voltage is higher than 13V, the operating voltage (VCC - VEE) of SGM25715 is clamped by an internal 13V Zener diode. The residual system voltage is sustained by the resistor R_{IN} between VCC and GND. The R_{IN} resistor needs to provide a minimum current of 2mA to SGM25715 under the minimum system voltage condition, and ensure that the power consumption on the resistor meets the requirements under the maximum system voltage, with the calculation formula shown below:

$$P_{RIN} = (V_{SYS\_MAX} - 13V)^2/R_{IN} \quad (1)$$

Placing a capacitor C_{IN} between VEE and VCC helps maintain stable operating voltage.

Current Limit, R_S

The SGM25715 monitors the current in the MOSFET based on the voltage between SENSE and VEE. The current limiting threshold voltage is 50mV, and the required R_S resistance value can be calculated as follows:

$$R_S = \frac{50mV}{I_{LIM}} \quad (2)$$

where

I_{LIM}: the current limit threshold

When this sampling voltage reaches the current limiting threshold, the SGM25715 controls the gate voltage of the MOSFET to limit the load current. At the same time, the C_T capacitor begins charging, and fault timing initiates. For proper device operation, R_S must not exceed 100mΩ.

It is recommended to specify the required power rating of sense resistor R_S based on the current limit value, to avoid prolonged operation near the current limit threshold during fault conditions. The threshold of the circuit breaker is approximately 100mV, so the surge current capability of R_S needs to be considered. Kelvin four-wire routing is recommended for the connections. The layout that can be referred to is shown in Figure 11, where the wire between the SGM25715 and the sensing resistor does not flow through the load current. This routing scheme feeds only the true voltage drop across R_S into the VEE and SENSE pins, eliminating voltage errors introduced by parasitic resistance on high-current solder joints.

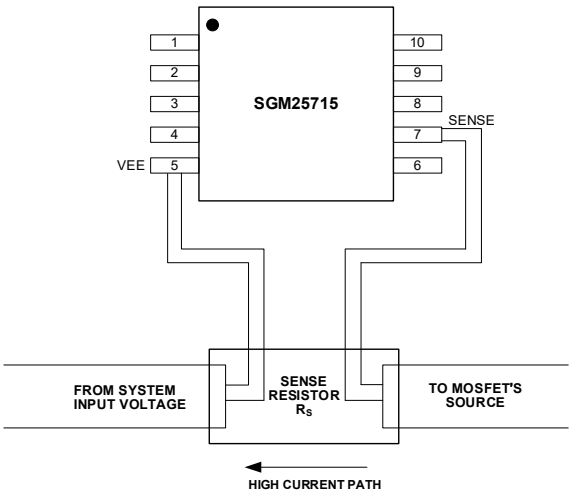


Figure 11. Sense Resistor Connections

APPLICATION INFORMATION (continued)

Power Limit Threshold

Power limiting is typically triggered during startup, or when excessive V_{DS} arises from severe overload or short-circuit conditions. The SGM25715 calculates the power dissipation of the external MOSFET Q_1 by monitoring two parameters: the drain current sensed across resistor R_S, and the drain-source voltage V_{DS} of Q_1 between the OUT and SENSE pins. The power limit of MOSFET is set by the resistor (R_{PWR}) at the PWR pin.

The calculation formula for the power limit value is related to the V_{DS} voltage of Q_1, and can be designed with reference to the following formula and MOSFET Power Dissipation Limit vs. R_{PWR} and R_S figure. The following formula calculates the power limit of V_{DS} at 24V/48V. As the V_{DS} voltage decreases, the power limit value also decreases accordingly. Testing and verification should be performed during the design process.

$$P_{FET\_LIM} \times R_S = 6.04 \times R_{PWR} + 92,\ V_{DS} = 24V$$
$$P_{FET\_LIM} \times R_S = 5.74 \times R_{PWR} + 200,\ V_{DS} = 48V \quad (3)$$

where

P_{FET_LIM} (W): the programmed power limit threshold

R_S (mΩ): the current sense resistor

R_{PWR} (kΩ): the power limit resistor at the PWR pin

Design should follow the formula corresponding to the maximum system voltage. For example, with a maximum V_{DS} of 48V, R_S = 10mΩ and a set MAX power limit threshold of 50W, the calculated R_{PWR} equals 52.3kΩ. R_{PWR} must be less than 150kΩ to ensure valid power limiting operation. When the SGM25715 detects that the power dissipation reaches the threshold, the circuit modulates the V_{GS} of Q_1 to limit the load current and Q_1 power dissipation. Meanwhile, the fault timer starts counting.

The configured maximum power dissipation should incorporate a suitable margin against the power limit specified on the MOSFET SOA curve when using the SGM25715R, because the power FET will endure repeated stress across fault restart cycles. It is advised to refer to the MOSFET supplier's official design guidelines. Leave the PWR pin floating if power limiting is unnecessary for the application.

Turn-On Time

The output turn-on time is determined by whether the SGM25715 uses only current limiting or both current and power limiting when turning on the load.

Turn-On with Current Limit Only

When the current limit threshold defined by R_S is lower than the current value defined by the power limit threshold under maximum V_{DS} conditions, the circuit remains at the current limit threshold over the full startup sequence. As shown in Figure 14, the SGM25715 regulates the V_{GS} to V_{GSL} to hold the current at I_{LIM}. After the output voltage rises to its steady-state value (V_{DS} ≈ 0V), the drain current falls to the nominal load current, and the gate is charged to roughly 13V (V_{GATE}). The time required for output startup completion is given by:

$$t_{ON} = \frac{V_{SYS} \times C_L}{I_{LIM}} \quad (4)$$

where

C_L: the load capacitance

As an example, if V_{SYS} = -48V, I_{LIM} = 2A, and C_L = 2200μF, t_{ON} calculates to 53ms. The maximum power loss on MOSFET during this process is 96W. This calculation is based on two assumptions: the time for current rising from 0 to the current limit value (t_1 to t_2) in Figure 14 is negligible compared with t_{ON}, and no load current is drawn before the turn-on sequence has ended. The Fault Timeout Period must be longer than t_{ON}, otherwise it will shut down before turn-on finishes.

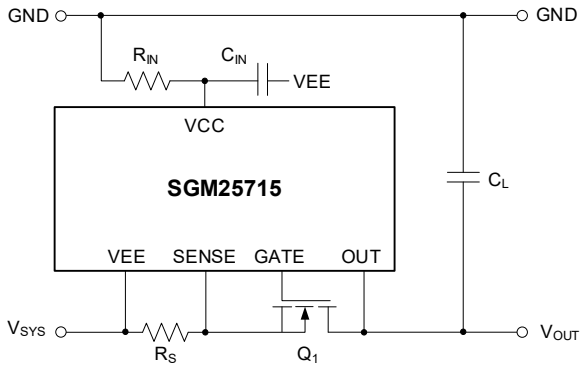


Figure 12. Output without Load Current during Turn-On

APPLICATION INFORMATION (continued)

If load current exists during turn-on (Figure 13), the turn-on time becomes longer than the previously computed result and is roughly given by:

$$t_{ON} = R_L \times C_L \times \ln\left(\frac{I_{LIM} \times R_L}{I_{LIM} \times R_L - V_{SYS}}\right) \quad (5)$$

where

R_L: the load resistance

V_{SYS}: the absolute value of the V_{SYS}

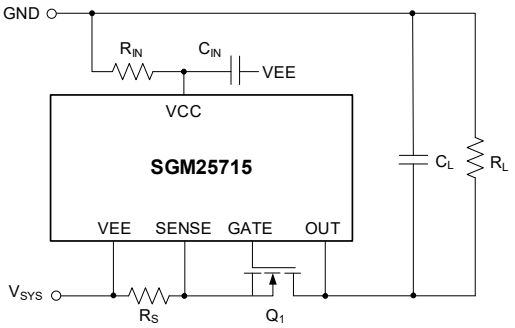


Figure 13. Output with Load Current during Turn-On

Turn-On with Power Limit and Current Limit

When the current limit threshold defined by R_S is higher than the current value defined by the power limit threshold under maximum V_{DS} conditions, the circuit initially operates in power limiting mode. As V_{DS} drops and the drain current rises to I_{LIM}, the device transitions into current limiting mode, as illustrated in Figure 14. When no load resistance R_L is connected during startup, output voltage steady-state settling time can be approximated as:

$$t_{ON} = \frac{C_L \times V_{SYS}^2}{2 \times P_{FET\_LIM}} + \frac{C_L \times P_{FET\_LIM}}{2 \times I_{LIM}^2} \quad (6)$$

As an example, if V_{SYS} = -48V, C_L = 2200μF, I_{LIM} = 5A, and P_{FET_LIM} = 100W, then t_{ON} ≈ 30ms.

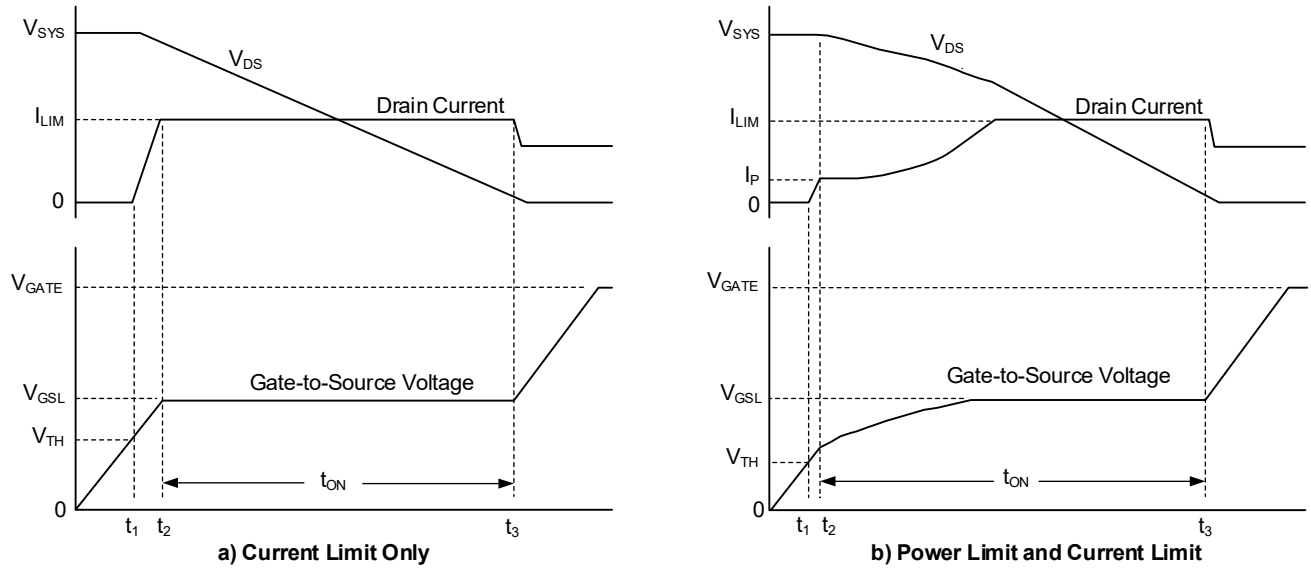


Figure 14. MOSFET Power-Up Waveforms

APPLICATION INFORMATION (continued)

MOSFET Selection

The selection of external MOSFET is very important, and the following selection criteria are recommended:

- The BV_{DSS} rating must exceed the maximum system voltage (V_{SYS}), and consider the transient spikes that exist during the hot plugging process of the boards.
- The maximum steady-state operating current must be higher than the current limit threshold, since the current in the MOSFET may remain at the current limit value for a specified period.
- The pulsed drain current specification (I_{DM}) must exceed the current defined by the circuit breaker function (100mV/R_S).
- Select a MOSFET whose SOA satisfies the actual operating requirements. The configured maximum power dissipation should incorporate suitable margin against the power limit specified on the MOSFET SOA curve when using the SGM25715R, because the power FET will endure repeated stress across fault restart cycles. It is advised to refer to the MOSFET supplier's official design guidelines.
- R_{DSON} should be low enough to ensure that the junction temperature does not exceed the allowable value under prolonged steady-state maximum power operation.

It is necessary to check if the MOSFET's maximum permissible V_{GS} voltage is higher than 13V. If this value is lower than 13V, a Zener diode needs to be used to limit the V_{GS} voltage. Meanwhile, the forward current rating of the external Zener diode must be large enough as the pull-down current of GATE pin during circuit breaker protection events can be 90mA.

Timer Capacitor, C_T

The SGM25715 uses various internal current sources and sinks at the TIMER pin for charging and discharging the external C_T capacitor, and determines the timing status based on the C_T voltage. Three time intervals can be configured via the C_T capacitor: insertion delay, Fault Timeout Period, and auto-restart timing of SGM25715R.

Insertion Delay

The external MOSFET Q_1 remains off during the insertion delay t_1 (refer to Figure 4) to enable full stabilization of voltage ringing and transients. As the required settling time differs from one application to another, it is necessary to determine the worst-case settling time corresponding to each specific design. The insertion time begins once the operating voltage rises above the POR_{IT} threshold. At this stage, an internal 6.1μA current source charges the timing capacitor C_T from 0V to 4V. After the C_T voltage reaches 4V, the insertion time ends. After that the C_T is discharged by a 1.6mA current sink. The required capacitance value is calculated using the formula shown below:

$$C_T = \frac{t_1 \times 6.1\mu A}{4V} = t_1 \times 1.525 \times 10^{-6} \quad (7)$$

where

t_1: the set insertion delay

As an example, if the insertion delay is configured as 220ms, then C_T = 335.5nF.

Fault Timeout Period

When the current limit or power limit function is triggered, the 95μA fault timer current source starts charging C_T. The time for TIMER pin to charge to 4V with the 95μA, is defined as Fault Timeout Period. After timing expires, Q_1 turns off. The capacitance required for a target Fault Timeout Period can be calculated using the formula below:

$$C_T = \frac{t_{FAULT} \times 95\mu A}{4V} = t_{FAULT} \times 2.375 \times 10^{-5} \quad (8)$$

As an example, the desired t_{FAULT} is 20ms, then C_T = 0.47μF. When the fault timeout expires or the fault is cleared, the C_T is discharged by 2.5μA current sink. For the SGM25715L, C_T must be discharged below 0.3V, then an external circuit can start the power-up sequence. Refer to Fault Timer and Restart section and Figure 6. For the SGM25715R, restart after the time set by C_T.

As the SGM25715 typically operates under power and current limiting conditions during power up, the Fault Timeout Period must exceed the settling time of the output voltage to its final value. See Turn-On Time section.

APPLICATION INFORMATION (continued)

Restart Timing

For the SGM25715R, once the Fault Timeout Period expires, a 2.5μA current sink discharges C_T from 4V to 1.25V. The TIMER pin then executes seven additional charge and discharge cycles ranging from 1.25V to 4V (Figure 7). The TIMER pin voltage drops to 0.3V during the last drop, and the SGM25715R completes the restart. The total restart time is calculated as shown in the equation below:

$$t_{RESTART} = C_T \times \left(\frac{7 \times 2.75V}{2.5\mu A} + \frac{7 \times 2.75V}{95\mu A} + \frac{3.7V}{2.5\mu A} \right) = C_T \times 9.4 \times 10^6 \quad (9)$$

As an example, if C_T = 0.47μF, then $t_{RESTART}$ = 4.4s. When the restart time expires, Q_1 is turned on. If the fault persists, the SGM25715R will perform fault timing and restart timing again. The Fault Timeout Period accounts for approximately 0.5% of the total restart cycle in this persistent fault condition.

UVLO, OVLO

Programmable UVLO and OVLO thresholds allow the SGM25715 to activate the series pass MOSFET (Q_1) within the desired input supply voltage (V_{SYS}) operating range. When V_{SYS} drops below UVLO threshold or exceeds OVLO threshold, Q_1 is shut down. Hysteresis is provided for both UVLO and OVLO thresholds. All of the following voltages are referenced to VEE. It is necessary to ensure that the voltages of UVLO and OVLO are always below than the Absolute Maximum Ratings for these pin. All voltages used in the formula of the section are absolute values.

Option A:

Three resistors (R_1, R_2, R_3) are required to configure the thresholds as shown in Figure 15.

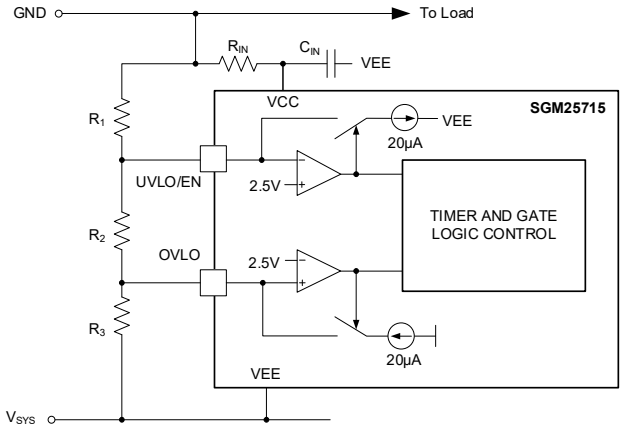


Figure 15. Programming the Thresholds with R_1-R_3

The resistor value calculation steps are as follows:

- Select the upper UVLO threshold (V_{UVH}) at which Q_1 turns on,
- Select the lower UVLO threshold (V_{UVL}) at which Q_1 turns off.
- Select the upper OVLO threshold (V_{OVH}) at which Q_1 turns off.
- The lower OVLO threshold (V_{OVL}) can be calculated using R_1-R_3. If precise setting of V_{OVL} is required alongside the other three thresholds, refer to Option B described.

The resistor values can be calculated using the equations below:

$$R_1 = \frac{V_{UVH} - V_{UVL}}{20\mu A} = \frac{V_{UV\_HYS}}{20\mu A}$$

$$R_3 = \frac{2.5V \times R_1 \times V_{UVL}}{V_{OVH} \times (V_{UVL} - 2.5V)}$$

$$R_2 = \frac{2.5V \times R_1}{V_{UVL} - 2.5V} - R_3 \quad (10)$$

The lower OVLO threshold can be calculated as follows:

$$V_{OVL} = (R_1 + R_2) \times \left(\frac{2.5V}{R_3} - 20\mu A \right) + 2.5V \quad (11)$$

For example, the selected voltage thresholds are V_{UVH} = -36V, V_{UVL} = -32V, V_{OVH} = -60V.

$$R_1 = \frac{36V - 32V}{20\mu A} = \frac{4V}{20\mu A} = 200k\Omega$$

$$R_3 = \frac{2.5V \times 200k\Omega \times 32V}{60V \times (32V - 2.5V)} = 9.04k\Omega$$

$$R_2 = \frac{2.5V \times 200k\Omega}{32V - 2.5V} - 9.04k\Omega = 7.91k\Omega \quad (12)$$

The resulting V_{OVL} is -55.8V, with an OVLO hysteresis of 4.2V. It should be noted that for this circuit configuration, the OVLO hysteresis is consistently larger than the UVLO hysteresis.

APPLICATION INFORMATION (continued)

If the resistance values of R_1 through R_3 are known, the UVLO and OVLO voltages can be derived using the formulas shown below:

$$V_{UVH} = 2.5V + R_1 \times \left(20\mu A + \frac{2.5V}{R_2 + R_3} \right)$$

$$V_{UVL} = \frac{2.5V \times (R_1 + R_2 + R_3)}{R_2 + R_3}$$

$$V_{UV\_HYS} = R_1 \times 20\mu A$$

$$V_{OVH} = \frac{2.5V \times (R_1 + R_2 + R_3)}{R_3}$$

$$V_{OVL} = (R_1 + R_2) \times \left(\frac{2.5V}{R_3} - 20\mu A \right) + 2.5V$$

$$V_{OV\_HYS} = (R_1 + R_2) \times 20\mu A \quad (13)$$

Option B:

This section introduces the method of accurately configuring four voltage thresholds using four resistors, as shown in Figure 16.

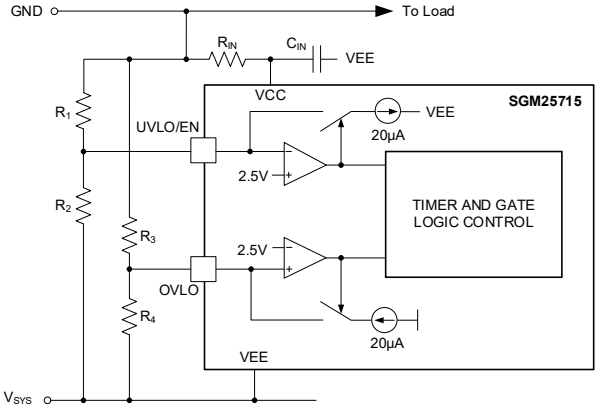


Figure 16. Programming the Thresholds with R_1-R_4

This design allows flexible selection of UVLO, OVLO and their hysteresis values. The resistor value calculation steps are as follows:

$$R_1 = \frac{V_{UVH} - V_{UVL}}{20\mu A} = \frac{V_{UV\_HYS}}{20\mu A}$$

$$R_2 = \frac{2.5V \times R_1}{V_{UVL} - 2.5V}$$

$$R_3 = \frac{V_{OVH} - V_{OVL}}{20\mu A} = \frac{V_{OV\_HYS}}{20\mu A}$$

$$R_4 = \frac{2.5V \times R_3}{V_{OVL} - 2.5V} \quad (14)$$

As an example, the target threshold values are set as V_{UVH} = -36V, V_{UV_HYS} = 4V, V_{OVH} = -60V, and V_{OV_HYS} = 4V. The resistors are: R_1 = 200kΩ, R_2 = 16.9kΩ, R_3 = 200kΩ, R_4 = 9.35kΩ.

If the resistance values of R_1 through R_4 are known, the UVLO and OVLO voltages can be derived using the formulas shown below:

$$V_{UVH} = 2.5V + R_1 \times \left(\frac{2.5V}{R_2} + 20\mu A \right)$$

$$V_{UVL} = \frac{2.5V \times (R_1 + R_2)}{R_2}$$

$$V_{UV\_HYS} = R_1 \times 20\mu A$$

$$V_{OVH} = \frac{2.5V \times (R_3 + R_4)}{R_4}$$

$$V_{OVL} = 2.5V + R_3 \times \left(\frac{2.5V}{R_4} - 20\mu A \right)$$

$$V_{OV\_HYS} = R_3 \times 20\mu A \quad (15)$$

Option C:

Based on the method introduced by Option B, further adjustments can be made according to application requirements. To achieve the minimum UVLO voltage, connect the UVLO/EN pin to VCC, as shown in Figure 17. In this case, the UVLO threshold is the same as the POR_{EN} threshold (approximately 8.4V). The OVLO threshold can be configured separately according to Option B. Connected OVLO pin to VEE when the OVLO function is unused.

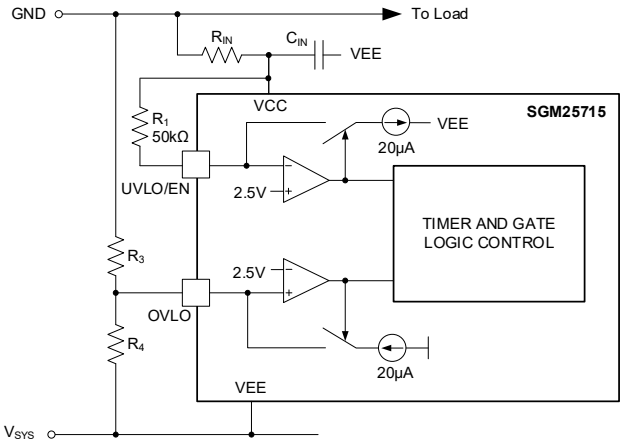


Figure 17. Minimum UVLO Voltage

APPLICATION INFORMATION (continued)

Thermal Considerations

The SGM25715 requires operation with junction temperature below +125℃. This parameter must be observed during application. The junction temperature is calculated as:

$$T_J = T_A + (\theta_{JA} \times P_D) \quad (16)$$

$$P_D = 13V \times I_{CC} \quad (17)$$

where

T_A: the ambient temperature

θ_{JA}: the thermal resistance of the SGM25715

P_D: the power dissipation of the SGM25715

I_{CC}: the current into the VCC pin

System Considerations

It is necessary to place capacitor on the supply side of the connector where this hot-swap circuit interfaces, as shown in Figure 3. The capacitor on the live backplane absorbs transients created during load current hot-swap shutdown. The inductance inherent in power traces creates large voltage spikes during current shutdown. These transients may exceed the SGM25715's Absolute Maximum Ratings and permanently damage the device if not suppressed by a capacitor.

Placing diodes on the output side can provide a freewheeling path for inductive loads. This diode protects the SGM25715 from potential damage, since the OUT pin voltage can rise significantly above GND during shutdown. Refer to Figure 18.

Surge Event System Considerations

The control MOSFET Q_1 incorporates an intrinsic body diode that permits reverse current conduction, as shown in Figure 19. Reverse current primarily arises from input-side discharge transients of the hot-swap circuit, triggered when output capacitance discharges back toward the input supply. Under typical operating conditions including shutdown and minor input voltage fluctuations, reverse current imposes no adverse effects on hot-swap controllers. Nevertheless, under extreme operating conditions including high-energy lightning surges and line disturbances, the hot-swap circuit may be subjected to ultra-fast, high-magnitude reverse current pulses. Current peaks as high as 1000A may be encountered in such extreme scenarios. Figure 19 depicts the waveform of a severe input discharge event and its impact on the circuit.

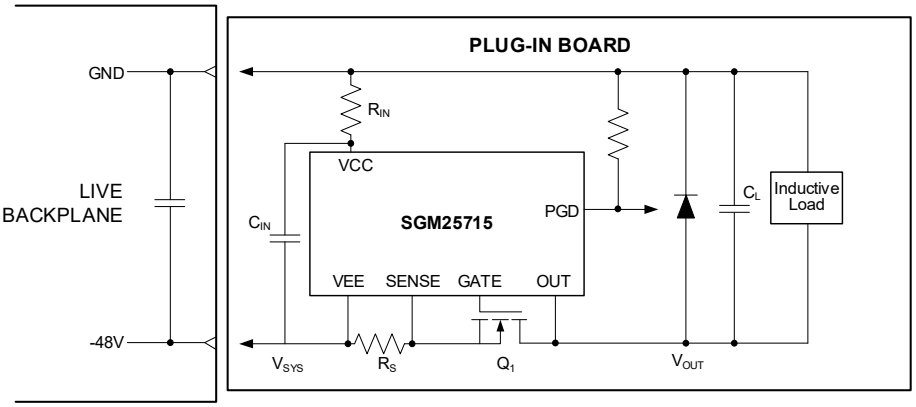


Figure 18. Output Diode Required for Inductive Loads

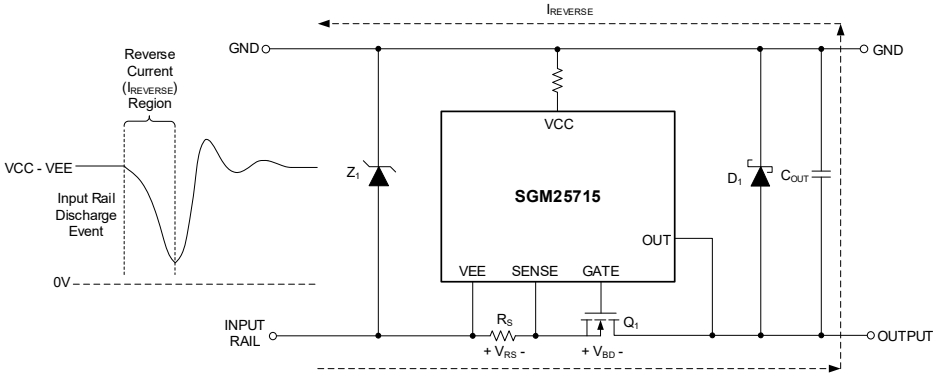


Figure 19. Differential Voltage across Sense Resistor

APPLICATION INFORMATION (continued)

When a reverse current spike occurs during chip operation, a differential voltage will appear across the sensing resistor (R_S) and the intrinsic body diode of Q_1. The transient reverse current follows the relation $I_{REVERSE} = C_{OUT} \times dV_{IN}/dt$, as the output capacitance discharges back into the input rail. A higher discharge slew rate dV_{IN}/dt produces larger $I_{REVERSE}$ currents. $I_{REVERSE}$ currents cause negative voltages relative to the SGM25715's VEE pin at the SENSE pin and OUT pin. If the negative voltage surpasses the negative maximum rating of the pins, destructive currents may flow into these pins and lead to damage. To mitigate risks arising from negative voltage conditions, place a resistor between the pins and the circuits to limit the current caused by negative voltage. In addition, Schottky diodes can be utilized to clamp voltages, Figure 20 shown this.

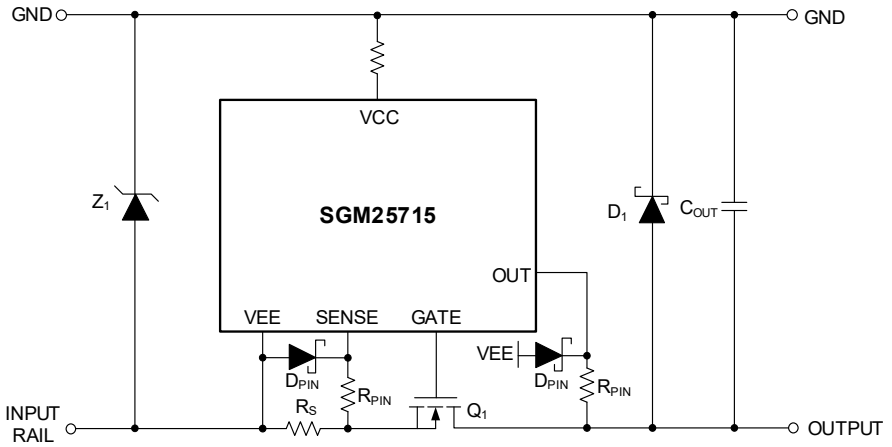
A 22Ω typical R_{PIN} resistor can be used for pin current limiting under severe negative voltage spikes. When a Schottky diode is used, it should be installed between the VEE pin and the SENSE pin, as well as between the VEE pin and the OUT pin. The anode of each Schottky diode must be closely connected to the VEE plane to achieve optimal clamping performance. The Schottky diode for the OUT pin should have a minimum voltage rating of 100V.

Suppressing negative voltage spikes on the SENSE and OUT pins delivers a highly robust hot-swap design and ensures stable operation amid extreme reverse current surges.

Power Good Pin

During initial system voltage power up, the Power Good pin (PGD) remains high before the operating voltage (VCC − VEE) rises above approximately 2V, then the pin pulls low and remains as the Q_1 is in the off-state. After Q_1 turns on, PGD transitions high when the voltage between the OUT pin and SENSE pin drops below 1.2V (Q_1 V_{DS} < 1.2V). This high state signals that the output voltage has reached or is close to its steady state target value. PGD will drop low within roughly 10μs under any of the following conditions:

- The V_{DS} voltage of Q_1 exceeds 2.42V.
- The system voltage fails to meet the UVLO and OVLO requirements.
- The Fault Timeout Period expires.



Series resistors are used to limit harmful negative pin currents and Schottky diodes are used to clamp the voltage at each pin.

Figure 20. Schottky Diodes Used to Clamp Pin Voltage

APPLICATION INFORMATION (continued)

The PGD pin is pulled up to the external voltage V_{PGD} through a resistor as shown in Figure 21. The V_{PGD} can reach up to 80V above VEE, with a transient capability of 100V. The pull-up voltage is referenced only to VEE and can exceed GND potential.

If additional delay is required for the PGD signal indication, the circuits shown in the following figures may be implemented. In Figure 22, the additional C_{PG} needs charging time during the PGD rising edge, while it does not affect PGD pull-down. In Figure 23, the added CPG and RPG introduce delay on both the rising and falling edges of PGD, where the rising delay is longer than falling delay. In Figure 24, the diode connected across R_{PG2} helps to separately configure the delay time for the rising and falling edges, and allow the falling edge delay to be longer than the rising edge delay.

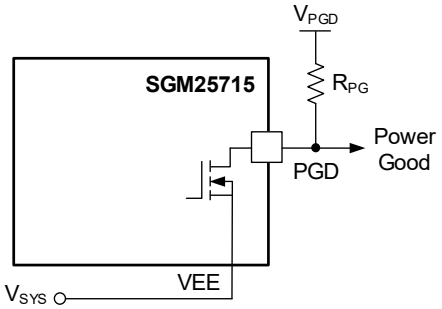


Figure 21. Power Good Output

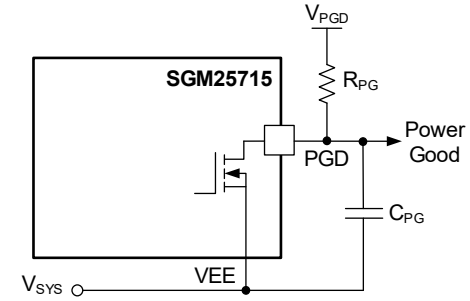


Figure 22. Adding Rising Delay to the PGD Pin

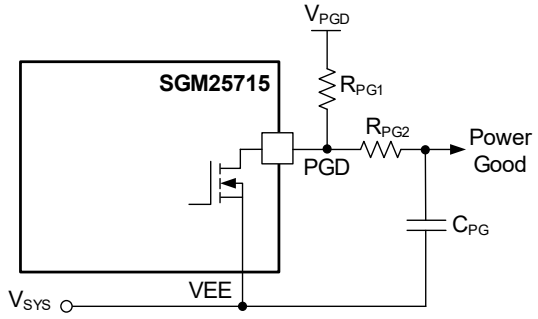


Figure 23. Adding Rising and Falling Delay to the PGD Pin (Rising Delay > Falling Delay)

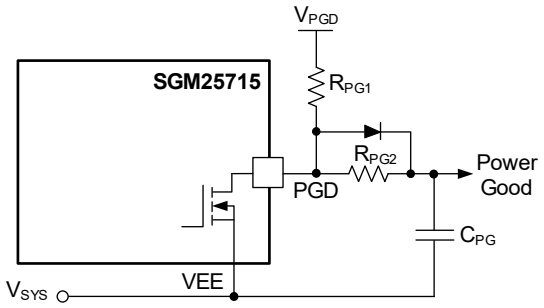


Figure 24. Adding Rising and Falling Delay to the PGD Pin (Delay Relationship Determined by Resistance Values)

APPLICATION INFORMATION (continued)

Operating Voltage

The SGM25715 operating voltage is the voltage from VCC to VEE, and is determined by an internal 13V Zener diode. When the system voltage exceeds 13V, the operating voltage will be clamped between VEE and VEE + 13V, and the residual system voltage is sustained by the resistor R_{IN} between VCC and GND. R_{IN} must be selected to supply a minimum current of 2mA to the SGM25715 under the minimum system voltage condition.

Layout Guidelines

There are some PCB design suggestions for SGM25715 as follows:

- The SGM25715 should be placed close to the board input connector and the PCB routing should be optimized to reduce parasitic inductance in the circuit.
- Place R_{IN} and C_{IN} near the VCC and VEE pins to suppress transients. Make sure that transient voltages are within the Absolute Maximum Ratings of the SGM25715. Load current shutdown can readily generate voltage transients of several volts.
- Place the sense resistor (R_S) close to the SESNE and VEE pins, and use the Kelvin techniques. The resistor should not exceed 100mΩ.
- The R_{PWR} resistor must be less than 150kΩ to ensure valid power limiting operation.
- Route the forward current path from board input to load and the return path in parallel and close to one another. This minimizes loop inductance.
- Do not connect peripheral components of the SGM25715 that require VEE connection directly to the high-current VEE traces. Tie these components to the VEE pin of the SGM25715 and route a single connection from this pin to the input VEE.
- For high power/current applications, it is necessary to provide sufficient heat dissipation for series pass MOSFET.
- In cases of high internal power dissipation within the SGM25715, implement an exposed thermal copper pad under the package. Connect this pad to large exposed copper planes on the opposite PCB layer using through hole. See Thermal Considerations section.
- Protective components such as TVS or Schottky diodes are recommended to be connected to the equipment through short paths to avoid voltage spikes caused by excessive line inductance.

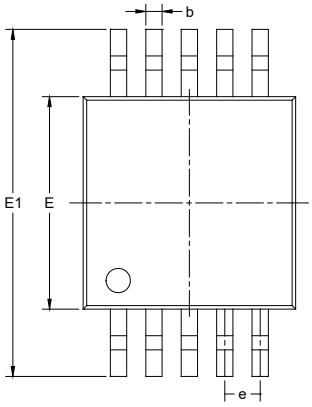
REVISION HISTORY

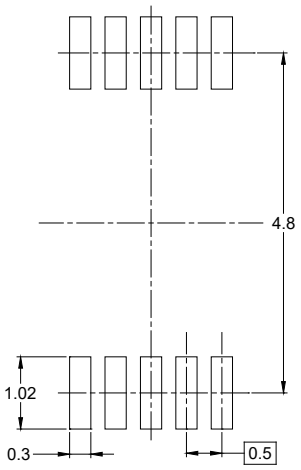
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original to REV.A (AUGUST 2026)	Page
Changed from product preview to production data	All

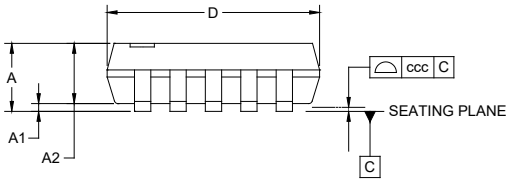
PACKAGE OUTLINE DIMENSIONS

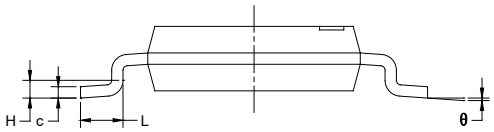
MSOP-10





RECOMMENDED LAND PATTERN (Unit: mm)



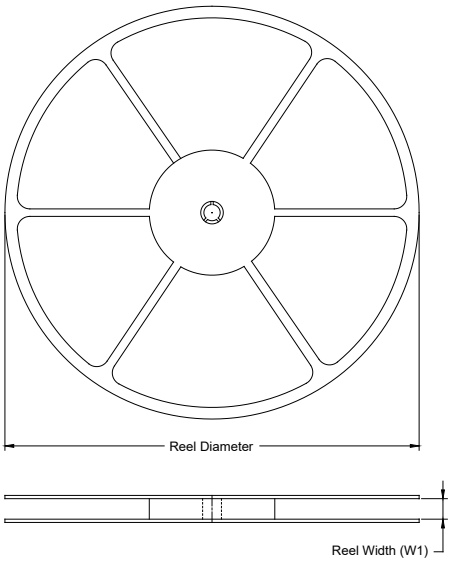


Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	-	-	1.100
A1	0.000	-	0.150
A2	0.750	-	0.950
b	0.170	-	0.330
c	0.080	-	0.230
D	2.900	-	3.100
E	2.900	-	3.100
E1	4.750	-	5.050
e	0.500 BSC		
H	0.250 TYP		
L	0.400	-	0.800
θ	0°	-	8°
ccc	0.100		

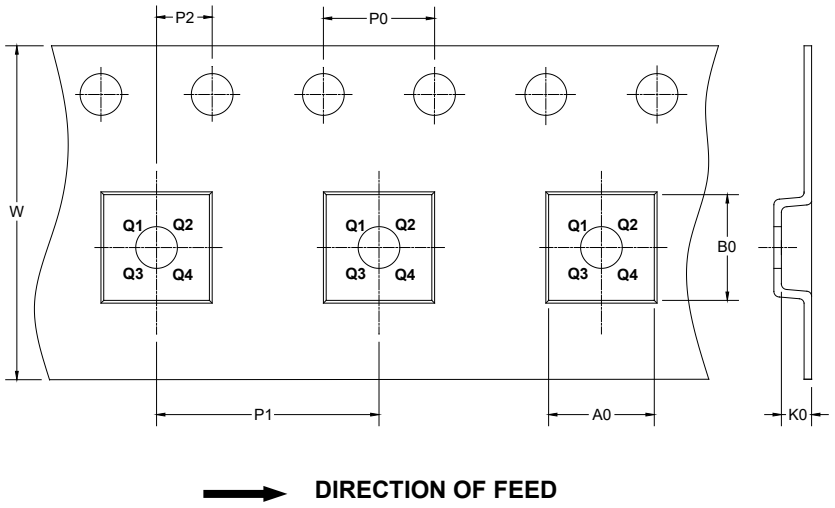
NOTES:
1. This drawing is subject to change without notice.
2. The dimensions do not include mold flashes, protrusions or gate burrs.
3. Reference JEDEC MO-187.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



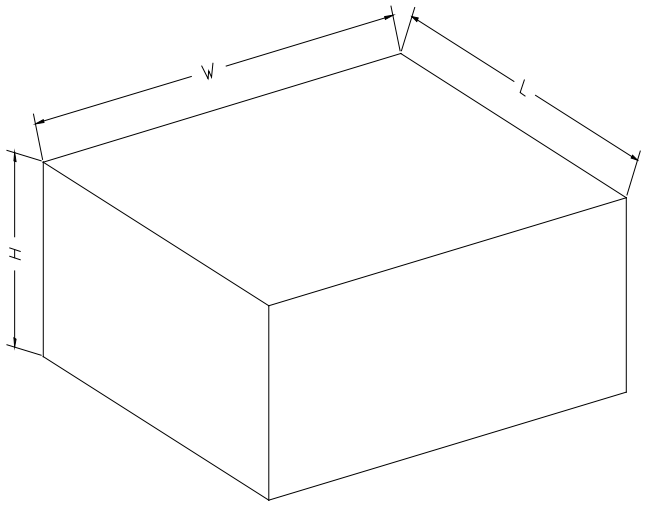
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
MSOP-10	13"	12.4	5.20	3.30	1.50	4.0	8.0	2.0	12.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002