



SGMCD1024xQ

24-Channel Multiple Switch Detection Interface with Adjustable Wetting Current for Automotive Applications

GENERAL DESCRIPTION

The SGMCD1024xQ is an advanced multiple switch detection interface (MSDI) designed to detect external switch status for automotive applications.

The SGMCD1024DQ integrates a 10-bit ADC for multi-position analog switch monitoring and a comparator for digital switch detection independent of the MCU. It features programmable thresholds to accommodate diverse switch types and system tolerances, ensuring precise operation in real-world conditions.

The SGMCD1024AQ features a comparator with adjustable thresholds to monitor digital switches independently of the MCU.

The SGMCD1024xQ device features 24 direct switch inputs, with 10 switch-to-power (SP) inputs, which are configurable to either switch-to-ground (SG) or switch-to-battery (SB), and 14 channels configurable to SG only. Each input supports multiple distinct programmable wetting current configurations, enabling optimized performance across diverse applications. To enhance energy efficiency, the system incorporates wake-up functionality for all switches, minimizing the need for sustained MCU activity. This solution integrates advanced protection features including fault detection, ESD protection, and diagnostic capabilities to ensure robust system operation. The device offers dual operational modes — continuous mode and polling mode. Continuous mode provides constant wetting current to detect the switch status. Polling mode employs periodic wetting current activation through a programmable timing interval, drastically reducing power consumption by sampling input statuses at scheduled intervals.

The device is AEC-Q100 qualified (Automotive Electronics Council (AEC) standard Q100 Grade 1) and it is suitable for automotive applications.

The SGMCD1024xQ is available in a Green TSSOP-38 (Exposed Pad) package.

FEATURES

- **AEC-Q100 Qualified for Automotive Applications**
Device Temperature Grade 1
 $T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$
- **Functional Safety**
 - ♦ Available Documentation in the Design of Functional Safety Systems
- **Detect Over-Voltage and Under-Voltage Faults for 12V Automotive Applications**
- **Monitor Up to 24 Direct Switch Inputs:**
 - ♦ 10 Switch-to-Power (SP) Inputs
 - ♦ 14 Switch-to-Ground (SG) Inputs
- **Switch Input Detection Ranging from -24V to 40V**
- **Selectable Wetting Current Levels:**
 - ♦ SGMCD1024AQ: 0mA, 1mA, 2mA and 5mA
 - ♦ SGMCD1024DQ: 0mA, 1mA, 2mA, 5mA, 10mA, and 15mA
- **Integrated 10-bit ADC for Multi-Position Analog Switch Monitoring (SGMCD1024DQ Only)**
- **Integrated Comparator with 4 Programmable Thresholds for Digital Switch Monitoring**
- **Ultra-Low Standby Current in Polling Mode:**
 - ♦ SGMCD1024AQ: 110 μA (TYP)
 - ♦ SGMCD1024DQ: 120 μA (TYP)
- **Use 3.3V/5.0V SPI Protocol to Communicate Directly with MCU**
- **Wake-up Functionality for All Inputs**
- **Integrated Battery and Temperature Sensing**
- **$\pm 8\text{kV}$ ISO-10605 Contact Discharge on Input Pins, with Required External Components**
- **Available in a Green TSSOP-38 (Exposed Pad) Package**

APPLICATIONS

Body Control and Gateway
Lighting and Mirrors
Air Conditioning System
Power Seats

24-Channel Multiple Switch Detection Interface with SGMCD1024xQ Adjustable Wetting Current for Automotive Applications

TYPICAL APPLICATION

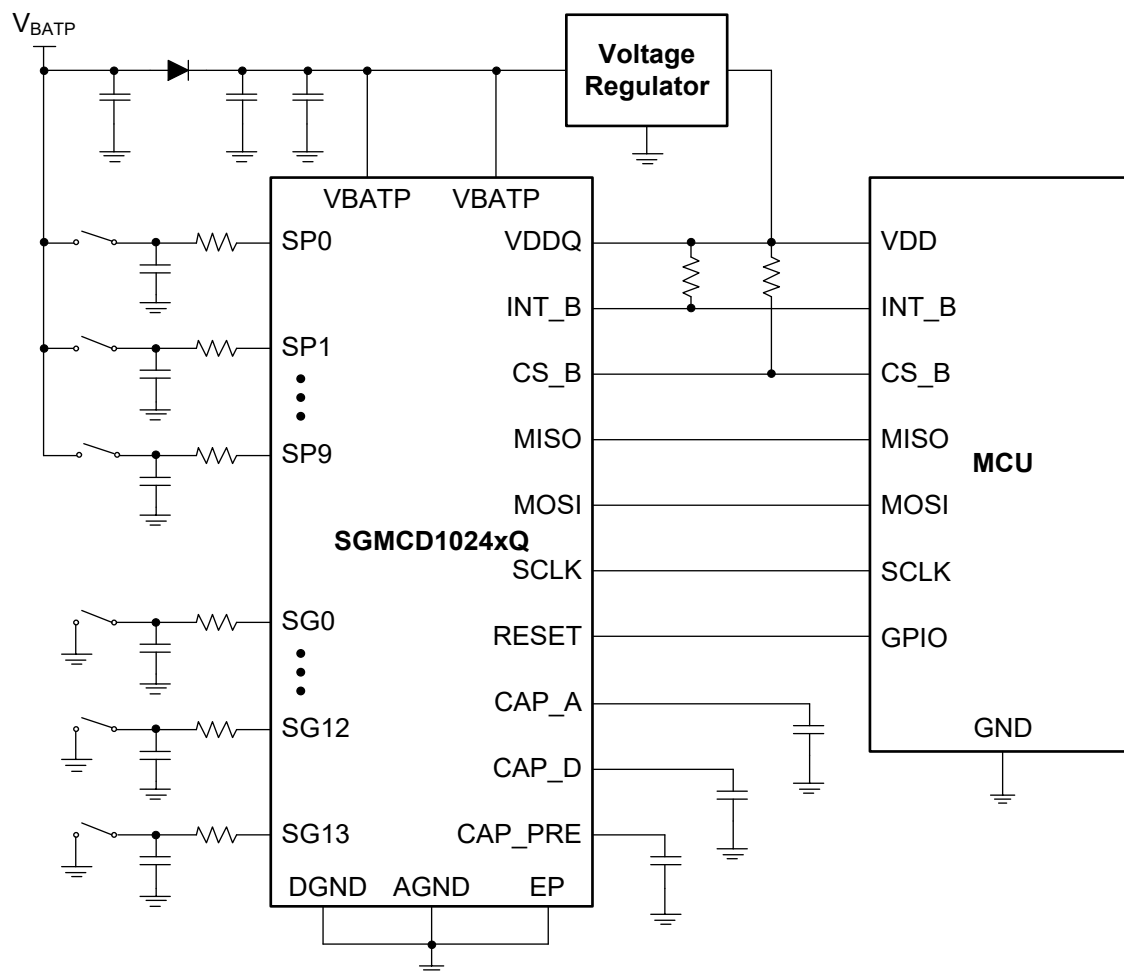


Figure 1. Typical Application Circuit

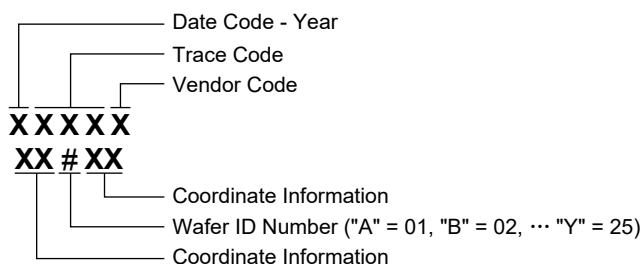
24-Channel Multiple Switch Detection Interface with SGMCD1024xQ Adjustable Wetting Current for Automotive Applications

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGMCD1024AQ	TSSOP-38 (Exposed Pad)	-40°C to +125°C	SGMCD1024AQPTS38G/TR	31QPTS38 XXXXX XX#XX	Tape and Reel, 4000
SGMCD1024DQ	TSSOP-38 (Exposed Pad)	-40°C to +125°C	SGMCD1024DQPTS38G/TR	2M3PTS38 XXXXX XX#XX	Tape and Reel, 4000

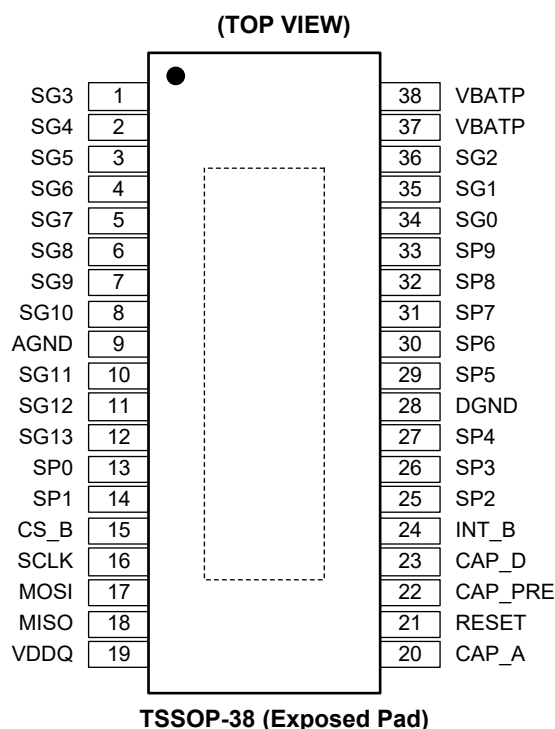
MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code. XX#XX = Coordinate Information and Wafer ID Number.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

PIN CONFIGURATION



24-Channel Multiple Switch Detection Interface with SGMCD1024xQ Adjustable Wetting Current for Automotive Applications

ABSOLUTE MAXIMUM RATINGS

VBATP, INT_B Voltage.....	-0.3V to 40V
VDDQ, SCLK, MOSI, MISO, CS_B, RESET Voltage	-0.3V to 6V
SGx, SPx Switch Input Voltage.....	-24V to 40V
CAP_PRE Voltage.....	-0.3V to 5.5V
CAP_A Voltage.....	-0.3V to 5.5V
CAP_D Voltage.....	-0.3V to 2V
Package Thermal Resistance	
TSSOP-38 (Exposed Pad), θ_{JA}	25.9°C/W
TSSOP-38 (Exposed Pad), θ_{JB}	7.9°C/W
TSSOP-38 (Exposed Pad), θ_{JC_TOP}	18.7°C/W
TSSOP-38 (Exposed Pad), θ_{JC_BOT}	0.8°C/W
Junction Temperature.....	+150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 10s).....	+260°C
ISO-10605 Contact Discharge	
Unpowered, SPx/SGx Pins ^{(1) (2)}	±8000V
Powered, SPx/SGx Pins ^{(1) (3)}	±8000V
ESD Susceptibility ^{(4) (5)}	
HBM, SGMCD1024AQ All Pins.....	±2000V
HBM, SGMCD1024AQ SPx/SGx Pins ⁽⁶⁾	±4000V
HBM, SGMCD1024DQ	±4000V
CDM, SGMCD1024AQ	±1000V
CDM, SGMCD1024DQ	±1000V

NOTES:

1. External component requirements at system level: reverse blocking diode from battery to VBATP ($0.6V < V_F < 1V$). See Figure 33.
2. External components: $2 \times 100nF$ capacitors and a 100Ω resistor. ESD generator: $150pF$ storage capacitance and 330Ω or 2000Ω discharge resistance.
3. External components: $2 \times 100nF$ capacitors and a 100Ω resistor. ESD generator: $330pF$ storage capacitance and 330Ω or 2000Ω discharge resistance.
4. For human body model (HBM), all pins comply with AEC-Q100-002 specification.
5. For charged device model (CDM), all pins comply with AEC-Q100-011 specification.
6. $\pm 4000V$ rating on the SPx/SGx pins is stressed with respect to GND (with AGND, DGND, and EP tied together).

RECOMMENDED OPERATING CONDITIONS

Power Supply Voltage, VBATP	4.5V to 35V
Logic Supply Voltage, VDDQ	3V to 5.5V
INT_B Pin Voltage, VINT_B.....	0V to 35V
SGx, SPx Switch Input Voltage	0V to 35V
RESET Pin Voltage, VRESET.....	0V to 5.5V
SPI Input/Output Logic Level, VSPI_IO.....	0V to VDDQ
SPI Communication Frequency, fSPI.....	20Hz to 4MHz
Operating Ambient Temperature Range	-40°C to +125°C

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

24-Channel Multiple Switch Detection Interface with SGMCD1024xQ Adjustable Wetting Current for Automotive Applications

PIN DESCRIPTION

PIN	NAME	TYPE	FUNCTION
1 ~ 8, 10 ~ 12, 34 ~ 36	SG3 ~ SG10, SG11 ~ SG13, SG0 ~ SG2	I	Switch-to-Ground Input Pins.
9	AGND	G	Ground for Analog.
13, 14, 25 ~ 27, 29 ~ 33	SP0, SP1, SP2 ~ SP4, SP5 ~ SP9	I	Programmable Switch Inputs Pins. All of the 10 inputs can be programmed to either SB or SG.
15	CS_B	I	Chip Select Input Pin.
16	SCLK	I	Clock Input Pin.
17	MOSI	I	Master Output and Slave Input Pin. Control data of MCU input pin to SGMCD1024xQ.
18	MISO	O	Slave Output and Master Input Pin. Digital data of SGMCD1024xQ out pin to MCU.
19	VDDQ	P	3.3V/5.0V Supply Input Pin. Set SPI communication level.
20	CAP_A	O	External Capacitor Connection for the Analog LDO. A 100nF ceramic capacitor is recommended.
21	RESET	I	RESET Event Input Pin. This pin is logic low during normal mode and can be pulled high for some time to issue a hardware reset event. Note that a 1.1MΩ pull-down resistor is internally connected from RESET pin to GND. This pin should be connected to GND when not used.
22	CAP_PRE	O	External Capacitor Connection for the Pre-Regulator. A 1μF ceramic capacitor is recommended.
23	CAP_D	O	External Capacitor Connection for the Digital LDO. A 100nF ceramic capacitor is recommended.
24	INT_B	O	Open-Drain Output. Used as an indication when the change of switch status or any interrupt occurs.
28	DGND	G	Ground for Digital.
37, 38	VBATP	P	Battery Supply Input Pin. This pin requires an external reverse protection circuit.
Exposed Pad	EP	G	Exposed Pad. It is not electrically connected to AGND or DGND. Connect EP to the board ground to ensure efficient thermal dissipation and robust ESD protection.

NOTE: I: Input, O: Output, G: Ground, P: Power.

24-Channel Multiple Switch Detection Interface with SGMCD1024xQ Adjustable Wetting Current for Automotive Applications

ELECTRICAL CHARACTERISTICS SGMCD1024AQ

($V_{BATP} = 4.5V$ to $35V$, $V_{DDQ} = 3V$ to $5.5V$, $T_A = -40^\circ C$ to $+125^\circ C$, typical values are at $V_{BATP} = 12V$, $V_{DDQ} = 5V$ and $T_A = +25^\circ C$, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
VBATP Continuous Mode Power Supply Current	I _{BATP_CONT}	Continuous mode, I _{WET} = 5mA, all switches open, no unserviced interrupt			3.8	6	mA
VBATP Polling Mode Power Supply Average Current ⁽¹⁾	I _{BATP_POLL_COMP_25}	t _{POLL} = 64ms, t _{POLL_ACT} = 128μs, all 24 channels active, all switches open,	T _A = +25°C		110	200	μA
	I _{BATP_POLL_COMP_85}		T _A = -40°C to +85°C		110	200	
	I _{BATP_POLL_COMP}	I _{WET} = 5mA, no unserviced interrupt	T _A = -40°C to +125°C		110	200	
VBATP Reset Mode Power Supply Current	I _{BATP_RESET}	Reset mode, V _{RESET} = V _{DDQ} , V _{BATP} = 12V, all switches open, T _A = +25°C			13	21	μA
VBATP Power Supply Average Current in Idle State	I _{BATP_IDLE_25}	TRIGGER bit in CONFIG register = logic 0, T _A = +25°C, no unserviced interrupt			93	125	μA
	I _{BATP_IDLE_85}	TRIGGER bit in CONFIG register = logic 0, T _A = -40°C to +85°C, no unserviced interrupt			93	140	
	I _{BATP_IDLE}	TRIGGER bit in CONFIG register = logic 0, T _A = -40°C to +125°C, no unserviced interrupt			93	191	
Logic Supply Current from V _{DDQ}	I _{DDQ}	SCLK = MOSI = 0V, CS_B = INT_B = V _{DDQ} , no SPI communication			4.6	10	μA
Power-on Reset (POR) Voltage for VBATP	V _{POR_R}	Threshold for rising V _{BATP} from device off condition resulting in INT_B pin assertion and a flagged POR bit in the INT_STAT register		3.85		4.5	V
	V _{POR_F}	Threshold for falling V _{BATP} from device normal operation to reset mode and loss of SPI communication		1.95		2.8	V
Over-Voltage (OV) Condition for VBATP	V _{OV_R}	Threshold for rising V _{BATP} from device normal operation resulting in INT_B pin assertion and a flagged OV bit in the INT_STAT register		35		40	V
Over-Voltage (OV) Condition Hysteresis for VBATP	V _{OV_HYST}			1		3.5	V
Under-Voltage (UV) Condition for VBATP	V _{UV_R}	Threshold for rising V _{BATP} from under-voltage condition resulting in INT_B pin assertion and a flagged UV bit in the INT_STAT register		3.85		4.5	V
	V _{UV_F}	Threshold for falling V _{BATP} from under-voltage condition resulting in INT_B pin assertion and a flagged UV bit in the INT_STAT register		3.7		4.4	V
Under-Voltage (UV) Condition Hysteresis for VBATP	V _{UV_HYST}			75		275	mV
Threshold for Falling V _{DDQ} (Resulting in Loss of SPI Communication)	V _{DDQ_F}			2.4		2.7	V
Valid VDDQ Voltage Hysteresis	V _{DDQ_HYST}			50		150	mV
Wetting Current Accuracy (Digital Switches, Maximum Resistance Value with Switch Closed ≤ 100Ω , Minimum Resistance Value with Switch Open ≥ 5000Ω)							
Wetting Current Accuracy for Current Source (CSO), Switch Closed	I _{WET_CSO}	1mA setting	V _{BATP} = 4.5V to 35V	0.84	1	1.2	mA
		2mA setting		1.76	2	2.3	
		5mA setting	V _{BATP} = 4.5V to 5V	4.4		5.5	
			V _{BATP} = 5V to 35V	4.4	5	5.5	
Wetting Current Accuracy for Current Sink (CSI), Switch Closed	I _{WET_CSI}	1mA setting	V _{BATP} = 4.5V to 35V	0.8	1	1.2	mA
		2mA setting		1.7	2	2.3	
		5mA setting		4.4	5	5.6	
Voltage Drop from SPx Programmed as SB (Switch Closed)	V _{SB_DROP_CLOSED}	2mA setting, I _{WET} = 1mA				1.4	V
		5mA setting, I _{WET} = 1mA or 2mA				1.6	

NOTE: 1. Guaranteed by design.

24-Channel Multiple Switch Detection Interface with SGMCD1024xQ Adjustable Wetting Current for Automotive Applications

ELECTRICAL CHARACTERISTICS (continued)

SGMCD1024AQ

(V_{BATP} = 4.5V to 35V, V_{DDQ} = 3V to 5.5V, and T_A = -40°C to +125°C, typical values are at V_{BATP} = 12V, V_{DDQ} = 5V and T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Wetting Current Accuracy (Analog Switches)							
Wetting Current Accuracy (SPx and SGx Programmed as SG)	I _{WET}	1mA setting	V _{BATP} = 4.5V to 35V,	0.8	1	1.12	mA
		2mA setting	V _{BATP} - V _{SPx/SGx} ≥ 2.5V	1.75	2	2.25	
		5mA setting	V _{BATP} = 5.5V to 35V,	3.9	4.9	5.9	
			V _{BATP} - V _{SPx/SGx} ≥ 2.5V V _{BATP} = 5.5V to 35V, V _{BATP} - V _{SPx/SGx} ≥ 3V	4.3	5	5.6	
Leakage Currents							
Leakage Current at Input SPx/SGx when Channel is Disabled	I _{SPx/SGx_LEAK_OFF}	V _{SPx/SGx} = 0V to V _{BATP} , channel disabled (EN_SPx/SGx register bit = logic 0)		-2		2	μA
	I _{SPx/SGx_LEAK_OFF_25}	V _{SPx/SGx} = 0V to V _{BATP} , channel disabled (EN_SPx/SGx register bit = logic 0), T _A = +25°C		-1		1	
Leakage Current at Input SPx/SGx when Wetting Current is 0mA	I _{SPx/SGx_LEAK_0mA}	V _{SPx/SGx} = 0V to 6V, V _{BATP} = 6V to 35V, I _{WET} = 0mA		-5		50	μA
Leakage Current at Input SPx/SGx under Loss of GND Condition	I _{SPx/SGx_LEAK_GND}	V _{BATP} = 24V, V _{SPx/SGx} = 0V to 24V, all grounds (AGND, DGND, and EP) = 24V, VDDQ shorted to the grounds		-2			μA
Leakage Current at Input SPx/SGx under Loss of VBATP Condition	I _{SPx/SGx_LEAK_VBATP}	V _{SPx/SGx} = 0V to 24V, V _{BATP} shorted to the grounds = 0V, VDDQ = 0V				2	μA
Logic Levels							
INT_B Output Low Voltage	V _{INT_B_L}	I _{INT_B} = 2mA				0.35	V
		I _{INT_B} = 4mA				0.6	
MISO Output Low Voltage	V _{MISO_L}	I _{MISO} = 2mA				0.2× V _{DDQ}	V
MISO Output High Voltage	V _{MISO_H}	I _{MISO} = -2mA		0.8 × V _{DDQ}			V
MOSI, SCLK, and CS_B Input Low Voltage	V _{IN_L}					0.25× V _{DDQ}	V
MOSI, SCLK, and CS_B Input High Voltage	V _{IN_H}			0.7 × V _{DDQ}			V
RESET Input Low Voltage	V _{RESET_L}					0.8	V
RESET Input High Voltage	V _{RESET_H}			1.6			V
RESET Pin Internal Pull-Down Resistor	R _{RESET_25}	V _{RESET} = 0V to 5.5V, T _A = +25°C		0.7	1.1	1.7	MΩ
	R _{RESET}	V _{RESET} = 0V to 5.5V, T _A = -40°C to +125°C		0.2		2.1	
Comparator Threshold for 2V	V _{TH_COMP_2V}	THRES_COMP = 2V		1.9		2.2	V
Comparator Threshold for 2.7V	V _{TH_COMP_2.7V}	THRES_COMP = 2.7V		2.6		2.9	V
Comparator Threshold for 3V	V _{TH_COMP_3V}	THRES_COMP = 3V		2.9		3.3	V
Comparator Threshold for 4V	V _{TH_COMP_4V}	THRES_COMP = 4V		3.9		4.3	V
Comparator Equivalent Input Resistance	R _{IN_COMP}	SPx/SGx ≤ 6V, THRES_COMP = 2V/2.7V/3V/4V		200	500	1100	kΩ
Temperature Monitoring ⁽¹⁾							
Temperature Warning Trigger Temperature	T _{TW}			130	141	152	°C
Temperature Shutdown Trigger Temperature	T _{TSD}			148	159	170	°C
Temperature Hysteresis for T _{TW} and T _{TSD}	T _{HYS}				16		°C

NOTE: 1. Guaranteed by design.

24-Channel Multiple Switch Detection Interface with SGMCD1024xQ Adjustable Wetting Current for Automotive Applications

ELECTRICAL CHARACTERISTICS (continued)

SGMCD1024DQ

($V_{BATP} = 4.5V$ to $35V$, $V_{DDQ} = 3V$ to $5.5V$, and $T_A = -40^{\circ}C$ to $+125^{\circ}C$, typical values are at $V_{BATP} = 12V$, $V_{DDQ} = 5V$ and $T_A = +25^{\circ}C$, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
VBATP Continuous Mode Power Supply Current	I_{BATP_CONT}	Continuous mode, $I_{WET} = 10mA$, all switches open, no active ADC conversion or comparator comparison, no unserviced interrupt		6.4	7.2	mA
VBATP Polling Mode Power Supply Average Current in Comparator Mode ⁽¹⁾	$I_{BATP_POLL_COMP_25}$	$t_{POLL} = 64ms$, $t_{POLL_ACT} = 128\mu s$, all 24 channels active and configured to comparator mode, all switches open, $I_{WET} = 10mA$, no unserviced interrupt	$T_A = +25^{\circ}C$	120	200	μA
	$I_{BATP_POLL_COMP_85}$		$T_A = -40^{\circ}C$ to $+85^{\circ}C$	120	200	
	$I_{BATP_POLL_COMP}$		$T_A = -40^{\circ}C$ to $+125^{\circ}C$	120	200	
VBATP Polling Mode Power Supply Average Current in ADC Mode ⁽¹⁾	$I_{BATP_POLL_ADC_25}$	$t_{POLL} = 64ms$, $t_{POLL_ACT} = 128\mu s$, all 24 channels active and configured to ADC mode, all switches open, $I_{WET} = 10mA$, no unserviced interrupt	$T_A = +25^{\circ}C$	128	200	μA
	$I_{BATP_POLL_ADC_85}$		$T_A = -40^{\circ}C$ to $+85^{\circ}C$	128	200	
	$I_{BATP_POLL_ADC}$		$T_A = -40^{\circ}C$ to $+125^{\circ}C$	128	200	
VBATP Reset Mode Power Supply Current	I_{BATP_RESET}	Reset mode, $V_{RESET} = V_{DDQ}$, $V_{BATP} = 12V$, all switches open, $T_A = +25^{\circ}C$		15	21	μA
VBATP Power Supply Average Current in Idle State	$I_{BATP_IDLE_25}$	TRIGGER bit in CONFIG register = logic 0, $T_A = +25^{\circ}C$, no unserviced interrupt		64	90	μA
	$I_{BATP_IDLE_85}$	TRIGGER bit in CONFIG register = logic 0, $T_A = -40^{\circ}C$ to $+85^{\circ}C$, no unserviced interrupt		64	120	
	I_{BATP_IDLE}	TRIGGER bit in CONFIG register = logic 0, $T_A = -40^{\circ}C$ to $+125^{\circ}C$, no unserviced interrupt		64	160	
Logic Supply Current from V_{DDQ}	I_{DDQ}	SCLK = MOSI = 0V, CS_B = INT_B = V_{DDQ} , no SPI communication		5.2	11	μA
Power-on Reset (POR) Voltage for VBATP	V_{POR_R}	Threshold for rising V_{BATP} from device off condition resulting in INT_B pin assertion and a flagged POR bit in the INT_STAT register	3.85		4.5	V
	V_{POR_F}	Threshold for falling V_{BATP} from device normal operation to reset mode and loss of SPI communication	1.95		2.8	V
Over-Voltage (OV) Condition for VBATP	V_{OV_R}	Threshold for rising V_{BATP} from device normal operation resulting in INT_B pin assertion and a flagged OV bit in the INT_STAT register	35		40	V
Over-Voltage (OV) Condition Hysteresis for VBATP	V_{OV_HYST}		1		3.5	V
Under-Voltage (UV) Condition for VBATP	V_{UV_R}	Threshold for rising V_{BATP} from under-voltage condition resulting in INT_B pin assertion and a flagged UV bit in the INT_STAT register	3.85		4.5	V
	V_{UV_F}	Threshold for falling V_{BATP} from under-voltage condition resulting in INT_B pin assertion and a flagged UV bit in the INT_STAT register	3.7		4.4	V
Under-Voltage (UV) Condition Hysteresis for VBATP ⁽¹⁾	V_{UV_HYST}		75		275	mV
Threshold for Falling V_{DDQ} (Resulting in Loss of SPI Communication)	V_{DDQ_F}		2.4		2.7	V
Valid VDDQ Voltage Hysteresis	V_{DDQ_HYST}		50		150	mV

NOTE: 1. Guaranteed by design.

24-Channel Multiple Switch Detection Interface with SGMCD1024xQ Adjustable Wetting Current for Automotive Applications

ELECTRICAL CHARACTERISTICS (continued) SGMCD1024DQ

($V_{BATP} = 4.5V$ to $35V$, $V_{DDQ} = 3V$ to $5.5V$, and $T_A = -40^{\circ}C$ to $+125^{\circ}C$, typical values are at $V_{BATP} = 12V$, $V_{DDQ} = 5V$ and $T_A = +25^{\circ}C$, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Wetting Current Accuracy (Digital Switches, Maximum Resistance Value with Switch Closed ≤ 100Ω , Minimum Resistance Value with Switch Open ≥ 5000Ω)							
Wetting Current Accuracy for Current Source (CSO), Switch Closed	I _{WET_CSO}	1mA setting	V _{BATP} = 4.5V to 35V	0.83	1	1.16	mA
		2mA setting		1.7	2	2.25	
		5mA setting	V _{BATP} = 4.5V to 5V	4.4		5.5	
			V _{BATP} = 5V to 35V	4.4	5	5.5	
		10mA setting	V _{BATP} = 4.5V to 6V	8.9		11.1	
			V _{BATP} = 6V to 35V	8.9	10	11.1	
		15mA setting	V _{BATP} = 4.5V to 6.5V	9.5		16	
			V _{BATP} = 6.5V to 35V	13	15	16.5	
Wetting Current Accuracy for Current Sink (CSI), Switch Closed	I _{WET_CSI}	1mA setting	V _{BATP} = 4.5V to 35V	0.75	1	1.5	mA
		2mA setting		1.6	2	2.5	
		5mA setting		4.3	5	6	
		10mA setting		8.6	10	11.5	
		15mA setting	V _{BATP} = 4.5V to 6V	13.1	14.9	16.8	
			V _{BATP} = 6V to 35V	13.1	14.9	16.8	
Voltage Drop from SPx Programmed as SB (Switch Open)	V _{SB_DROP_OPEN}	10mA setting, R _{SW} = 5kΩ				1.7	V
		15mA setting, R _{SW} = 5kΩ				1.7	
Voltage Drop from SPx Programmed as SB (Switch Closed)	V _{SB_DROP_CLOSED}	2mA setting, I _{WET} = 1mA				1.3	V
		5mA setting, I _{WET} = 1mA or 2mA				1.4	
		10mA setting, I _{WET} = 1mA, 2mA, or 5mA				1.6	
		15mA setting, I _{WET} = 1mA, 2mA, 5mA, or 10mA				2.25	
Wetting Current Accuracy (Analog Switches)							
Wetting Current Accuracy (SPx and SGx Programmed as SG)	I _{WET}	1mA setting	V _{BATP} = 4.5V to 35V, V _{BATP} - V _{SPx/SGx} ≥ 2.5V	0.79	0.94	1.1	mA
		2mA setting		1.67	1.92	2.15	
		5mA setting	V _{BATP} = 5.5V to 35V, V _{BATP} - V _{SPx/SGx} ≥ 2.5V	4.41	5	5.48	
			V _{BATP} = 5.5V to 35V, V _{BATP} - V _{SPx/SGx} ≥ 3V	4.41	5	5.48	
			10mA setting	V _{BATP} = 6V to 35V, V _{BATP} - V _{SPx/SGx} ≥ 4V	9	10	
		15mA setting	V _{BATP} = 6.5V to 35V, V _{BATP} - V _{SPx/SGx} ≥ 5V	13.3	15	16.8	
Leakage Currents							
Leakage Current at Input SPx/SGx when Channel is Disabled	I _{SPx/SGx_LEAK_OFF}	V _{SPx/SGx} = 0V to V _{BATP} , channel disabled (EN_SPx/SGx register bit = logic 0)		-1.5		1.5	μA
	I _{SPx/SGx_LEAK_OFF_25}	V _{SPx/SGx} = 0V to V _{BATP} , channel disabled (EN_SPx/SGx register bit = logic 0), T _A = +25°C		-1		1	
Leakage Current at Input SPx/SGx when Wetting Current is 0mA	I _{SPx/SGx_LEAK_0mA}	V _{SPx/SGx} = 0V to 6V, V _{BATP} = 6V to 35V, I _{WET} = 0mA		-5		50	μA
Leakage Current at Input SPx/SGx under Loss of GND Condition	I _{SPx/SGx_LEAK_GND}	V _{BATP} = 24V, V _{SPx/SGx} = 0V to 24V, all grounds (AGND, DGND, and EP) = 24V, VDDQ shorted to the grounds		-2			μA
Leakage Current at Input SPx/SGx under Loss of VBATP Condition	I _{SPx/SGx_LEAK_VBATP}	V _{SPx/SGx} = 0V to 24V, V _{BATP} shorted to the grounds = 0V, VDDQ = 0V				2	μA

NOTE: 1. Guaranteed by design.

24-Channel Multiple Switch Detection Interface with SGMCD1024xQ Adjustable Wetting Current for Automotive Applications

ELECTRICAL CHARACTERISTICS (continued) SGMCD1024DQ

($V_{BATP} = 4.5V$ to $35V$, $V_{DDQ} = 3V$ to $5.5V$, and $T_A = -40^\circ C$ to $+125^\circ C$, typical values are at $V_{BATP} = 12V$, $V_{DDQ} = 5V$ and $T_A = +25^\circ C$, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNIT S
Logic Levels							
INT_B Output Low Voltage	V _{INT_B_L}	I _{INT_B} = 2mA				0.35	V
		I _{INT_B} = 4mA				0.6	
MISO Output Low Voltage	V _{MISO_L}	I _{MISO} = 2mA				0.2 × V _{DDQ}	V
MISO Output High Voltage	V _{MISO_H}	I _{MISO} = -2mA		0.8 × V _{DDQ}			V
MOSI, SCLK, and CS_B Input Low Voltage	V _{IN_L}					0.25 × V _{DDQ}	V
MOSI, SCLK, and CS_B Input High Voltage	V _{IN_H}			0.7 × V _{DDQ}			V
RESET Input Low Voltage	V _{RESET_L}					0.8	V
RESET Input High Voltage	V _{RESET_H}			1.6			V
RESET Pin Internal Pull-Down Resistor	R _{RESET_25}	V _{RESET} = 0V to 5.5V, T _A = +25°C		0.7	1.1	1.7	MΩ
	R _{RESET}	V _{RESET} = 0V to 5.5V, T _A = -40°C to +125°C		0.2		2.1	
Switch Input and V _{BATP} Measurement Conversion Parameters							
Resolution	RES			10			Bits
ADC Offset Error ⁽¹⁾	V _{OFFSET}	0mA setting, SPx/SGx measurements		-9	1.5	9	LSB
ADC Full-Scale Error	V _{FSE}	0mA setting, SPx/SGx measurements		-16	0	16	LSB
Switch Input Conversion Output	OUT _{SW}	1mA setting, V _{BATP} = 4.5V to 35V	100Ω resistance to ground at SPx/SGx	8	18	30	LSB
			300Ω resistance to ground at SPx/SGx	37	51	64	
			600Ω resistance to ground at SPx/SGx	82	100	120	
		2mA setting, V _{BATP} = 4.5V to 35V	100Ω resistance to ground at SPx/SGx	23	35	46	LSB
			300Ω resistance to ground at SPx/SGx	83	101	119	
			600Ω resistance to ground at SPx/SGx	172	201	229	
		5mA setting, V _{BATP} = 5V to 35V	100Ω resistance to ground at SPx/SGx	71	86	101	LSB
			300Ω resistance to ground at SPx/SGx	220	255	285	
			600Ω resistance to ground at SPx/SGx	448	509	557	
		10mA setting, V _{BATP} = 6V to 35V	100Ω resistance to ground at SPx/SGx	146	172	199	LSB
			250Ω resistance to ground at SPx/SGx	374	429	481	
			400Ω resistance to ground at SPx/SGx	601	686	769	
		15mA setting, V _{BATP} = 6.5V to 35V	100Ω resistance to ground at SPx/SGx	215	257	295	LSB
			200Ω resistance to ground at SPx/SGx	443	511	572	
			300Ω resistance to ground at SPx/SGx	680	768	865	
V _{BATP} Measurement Output Tolerance to Full-Scale Range	OUT _{VBATP}	V _{BATP} measurements (V _{BATP} ≥ 4.5V), VBATP_RATIO= 0 in register CONFIG				±7	%
		V _{BATP} measurements (V _{BATP} ≥ 4.5V), VBATP_RATIO= 1 in register CONFIG				±7	

NOTE: 1. Guaranteed by design.

24-Channel Multiple Switch Detection Interface with SGMCD1024xQ Adjustable Wetting Current for Automotive Applications

ELECTRICAL CHARACTERISTICS (continued) SGMCD1024DQ

(V_{BATP} = 4.5V to 35V, V_{DDQ} = 3V to 5.5V, and T_A = -40°C to +125°C, typical values are at V_{BATP} = 12V, V_{DDQ} = 5V and T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Full-Scale Range	V _{FSR}	SPx/SGx measurements		6		V
		V _{BATP} measurements (V _{BATP} ≥ 4.5V), VBATP_RATIO = 0 in register CONFIG		9		
		V _{BATP} measurements (V _{BATP} ≥ 4.5V), VBATP_RATIO = 1 in register CONFIG		30		
ADC Equivalent Input Resistance	R _{IN, ADC}	SPx/SGx measurements, SPx/SGx ≤ 6V	290	440	760	kΩ
Input Voltage Divider Factor ⁽¹⁾	R _{RATIO}	SPx/SGx measurements		2		
		VBATP measurements (V _{BATP} ≥ 4.5V), VBATP_RATIO = 0 in register CONFIG		3		
		VBATP measurements (V _{BATP} ≥ 4.5V), VBATP_RATIO = 1 in register CONFIG		10		
Comparator Parameters						
Comparator Threshold for 2V	V _{TH_COMP_2V}	THRES_COMP = 2V	1.9		2.15	V
Comparator Threshold for 2.7V	V _{TH_COMP_2.7V}	THRES_COMP = 2.7V	2.6		2.9	V
Comparator Threshold for 3V	V _{TH_COMP_3V}	THRES_COMP = 3V	2.9		3.2	V
Comparator Threshold for 4V	V _{TH_COMP_4V}	THRES_COMP = 4V	3.85		4.25	V
Comparator Equivalent Input Resistance	R _{IN, COMP}	SPx/SGx ≤ 6V, THRES_COMP = 2V/2.7V/3V/4V	290	440	760	kΩ
Temperature Monitoring ⁽¹⁾						
Temperature Warning Trigger Temperature	T _{TW}		130	141	152	°C
Temperature Shutdown Trigger Temperature	T _{TSD}		148	159	170	°C
Temperature Hysteresis for T _{TW} and T _{TSD}	T _{HYS}			16		°C

NOTE: 1. Guaranteed by design.

24-Channel Multiple Switch Detection Interface with SGMCD1024xQ Adjustable Wetting Current for Automotive Applications

TIMING REQUIREMENTS

(V_{BATP} = 4.5V to 35V, V_{DDQ} = 3V to 5.5V, and 10pF capacitive load on MISO, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Switch Monitoring, Interrupt, Startup and Reset						
Polling Active Time Accuracy	t _{POLL_ACT}	Polling mode	-15%		15%	
Polling Active Time Accuracy for Matrix Inputs	t _{POLL_ACTM}	Polling mode with matrix enabled	-15%		15%	
Polling Time Accuracy	t _{POLL}	Polling mode	-15%		15%	
Comparator Detection Time	t _{COMP}			12		μs
ADC Conversion Time (SGMCD1024DQ Only)	t _{ADC}	Sample and hold time included		24		μs
Transition Time Last Input Sampling and Start of Clean Current	t _{CCP_TRAN}			20		μs
Clean Current Active Time	t _{CCP_ACT}		-15%		15%	
Polling Startup Time	t _{STARTUP}		200	300	400	μs
Active INT_B Assertion Duration	t _{INTB_ACTIVE}		1.5	2	2.5	ms
INT_B Deassertion Duration during a Pending Interrupt	t _{INTB_INACTIVE}		3	4	5	ms
Interrupt Idle Time	t _{INTB_IDLE}		80	100	120	μs
Time Required to Keep the RESET Pin High to Successfully Reset the Device	t _{RESET}		2			μs
Delay Between a Fault Event (OV, UV, TW, or TSD) to a High to Low Transition on the INT_B Pin	t _{REACT}	See Figure 3 for OV example			28	μs
SPI Interface						
Falling Edge of CS_B to Rising Edge of SCLK Setup Time	t _{LEAD}		100			ns
Falling Edge of SCLK to Rising Edge of CS_B Setup Time	t _{LAG}		100			ns
MOSI to SCLK Falling Edge Setup Time	t _{SU}		30			ns
MOSI Hold Time After Falling Edge of SCLK	t _{HOLD}		20			ns
Time from Rising Edge of SCLK to Valid MISO Data	t _{VALID}				70	ns
Time from Falling Edge of CS_B to MISO Low-Impedance	t _{MISO_EN}				60	ns
Time from Rising Edge of CS_B to MISO High-Impedance	t _{MISO_DIS}	Loading of 1kΩ to GND. See Figure 4			60	ns
MOSI, CS_B, and SCLK Signals Rise Time	t _R			5	30	ns
MOSI, CS_B, and SCLK Signals Fall Time	t _F			5	30	ns
Delay Between two SPI Communication (CS_B Low) Sequences	t _{INTER_FRAME}		1.5			μs
SCLK High Time	t _{CKH}		120			ns
SCLK Low Time	t _{CKL}		120			ns
Delay Between Valid VDDQ Voltage and Initial SPI Communication	t _{INITIATION}		45			μs

24-Channel Multiple Switch Detection Interface with SGMCD1024xQ Adjustable Wetting Current for Automotive Applications

TIMING DIAGRAM

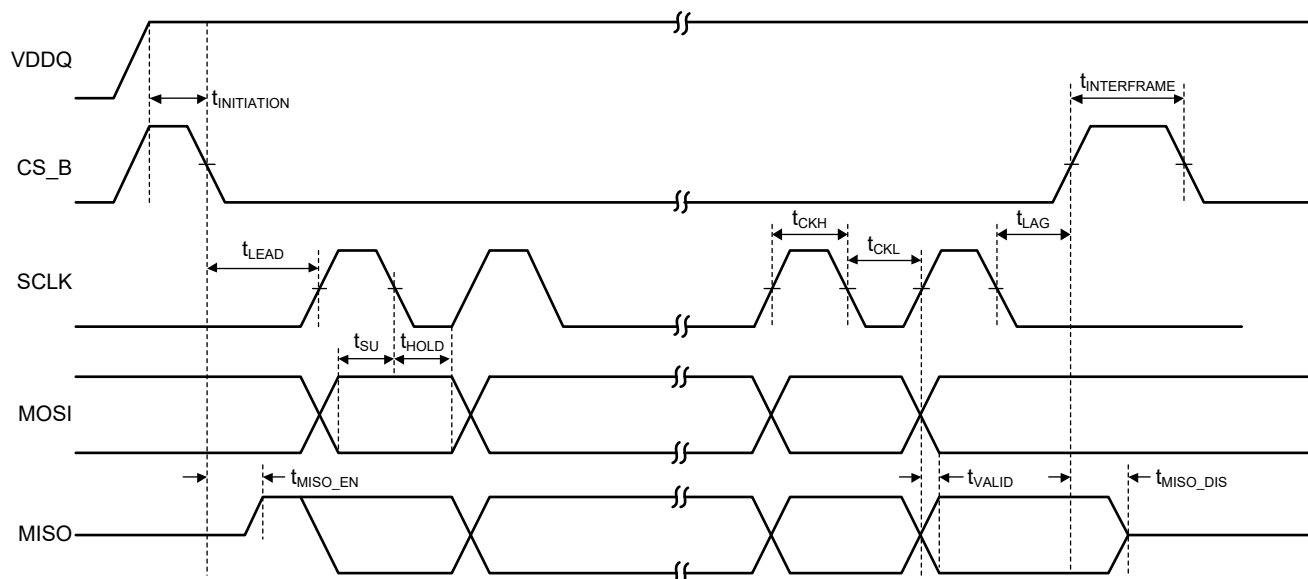


Figure 2. SPI Timing Diagram

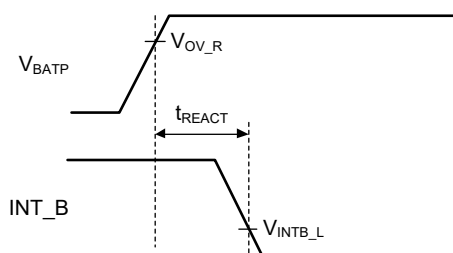


Figure 3. t_{REACT} Timing Diagram

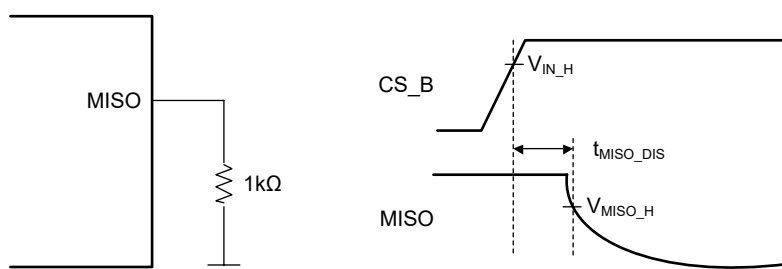


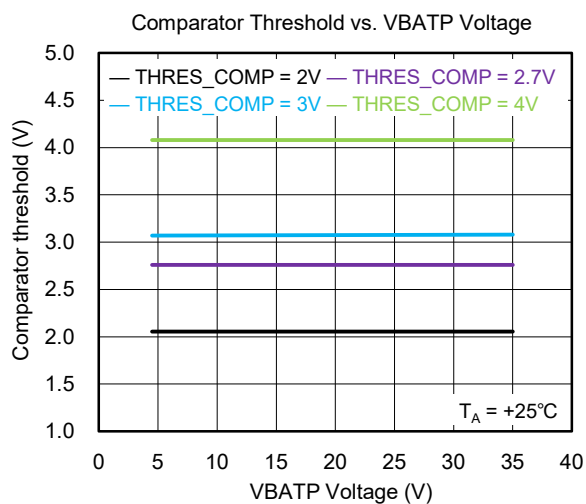
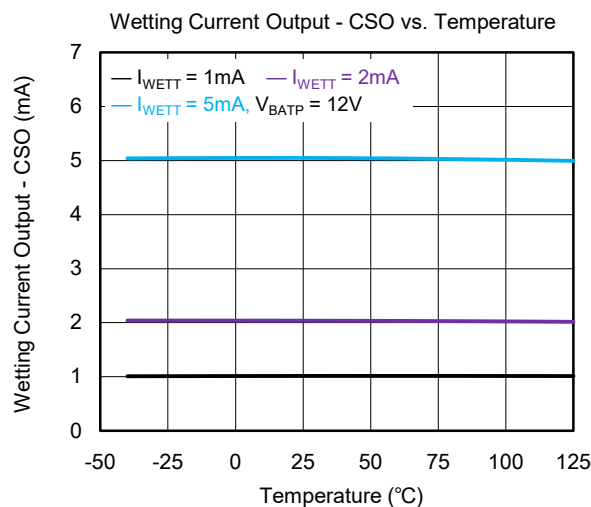
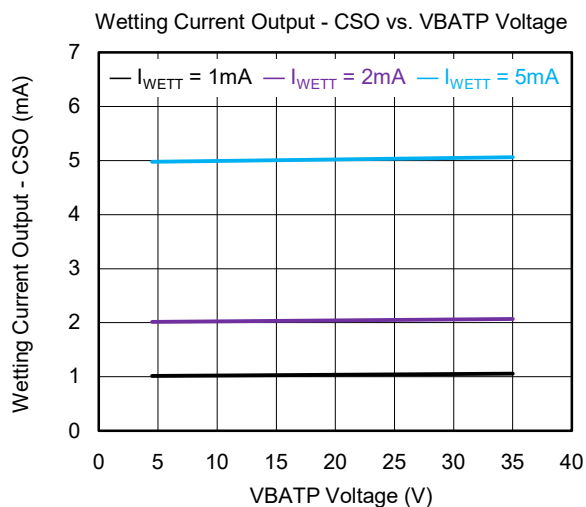
Figure 4. $t_{\text{MISO_DIS}}$ Timing Diagram

24-Channel Multiple Switch Detection Interface with SGMCD1024xQ Adjustable Wetting Current for Automotive Applications

TYPICAL PERFORMANCE CHARACTERISTICS

SGMCD1024AQ

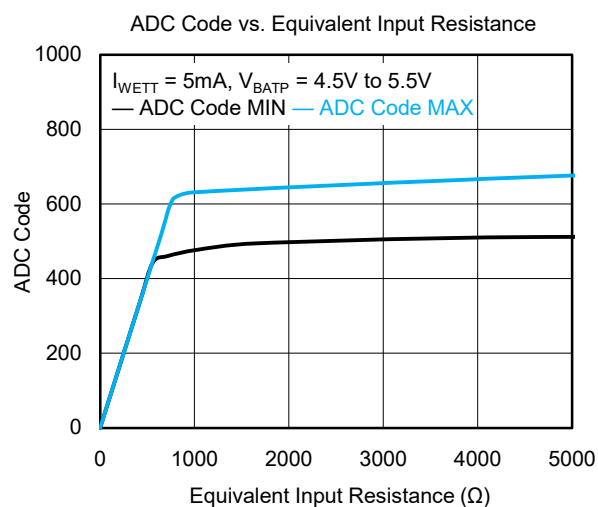
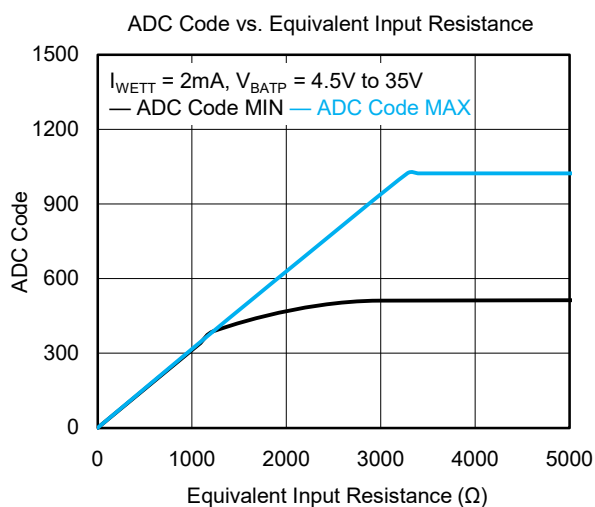
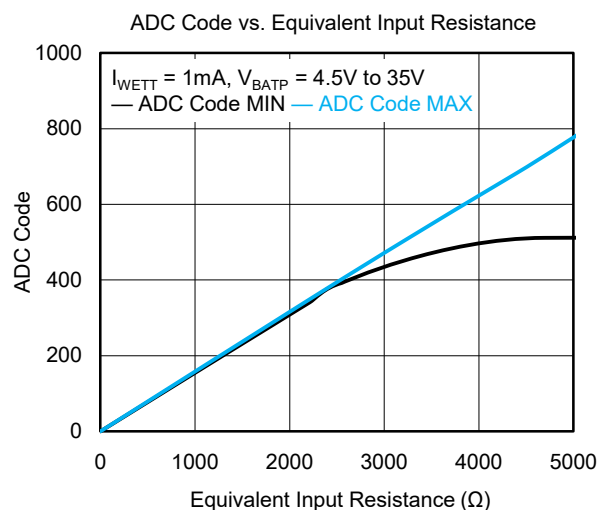
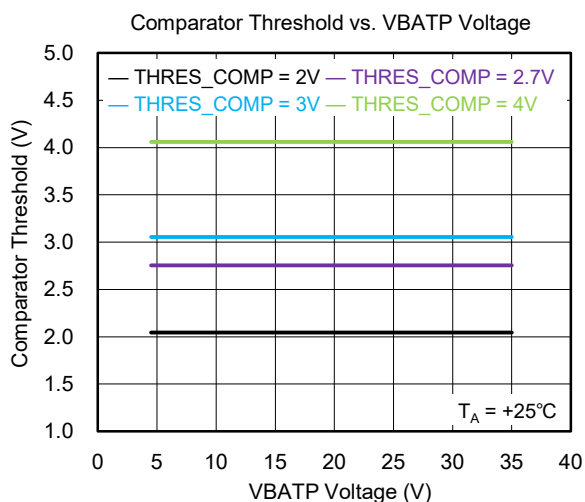
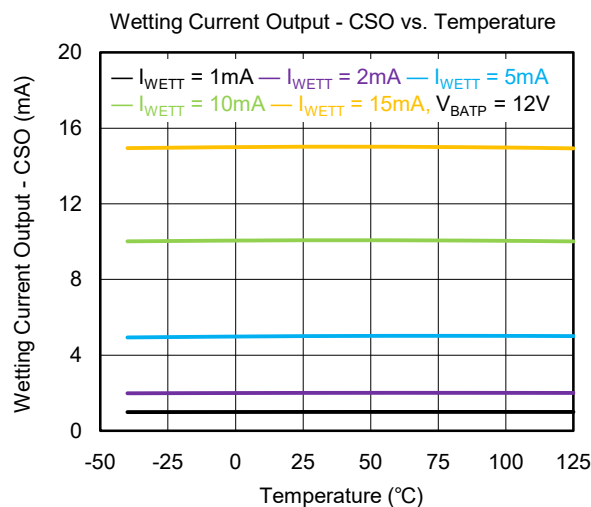
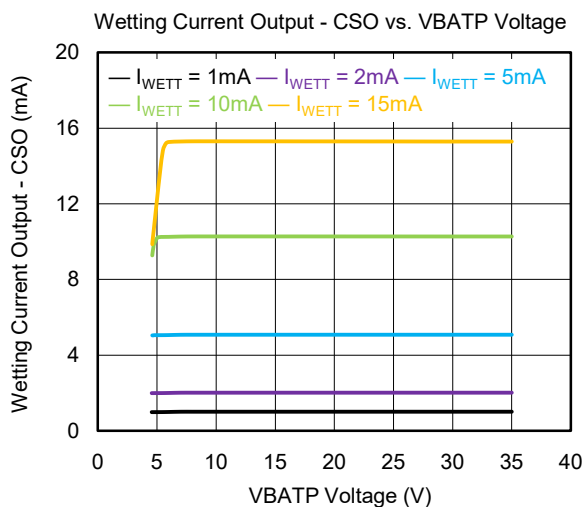
$T_A = +25^\circ\text{C}$, unless otherwise noted.



24-Channel Multiple Switch Detection Interface with SGMCD1024xQ Adjustable Wetting Current for Automotive Applications

TYPICAL PERFORMANCE CHARACTERISTICS (continued) SGMCD1024DQ

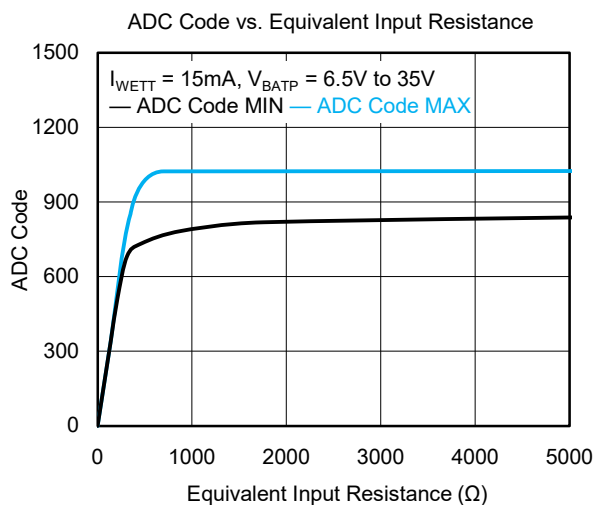
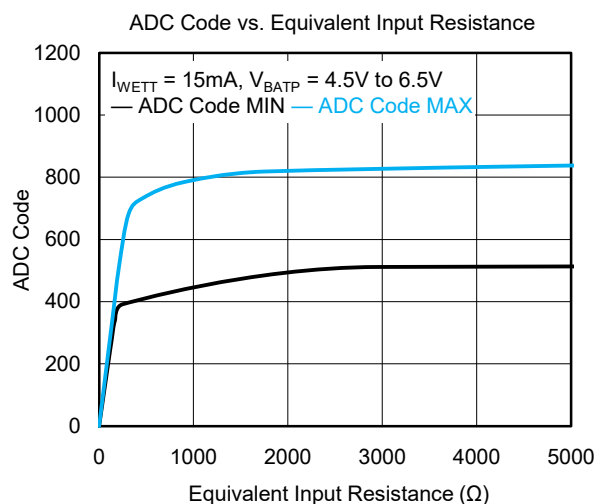
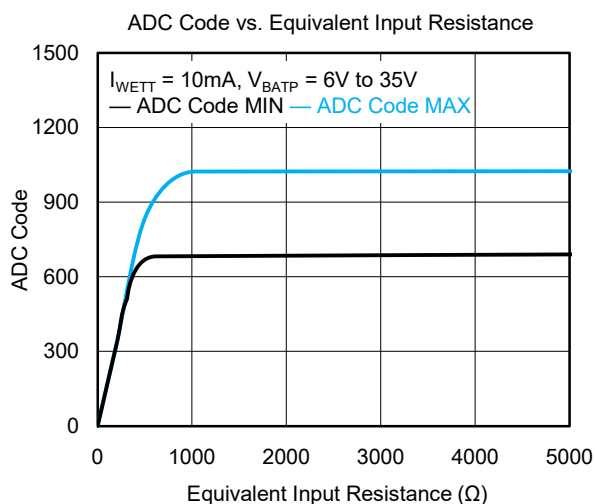
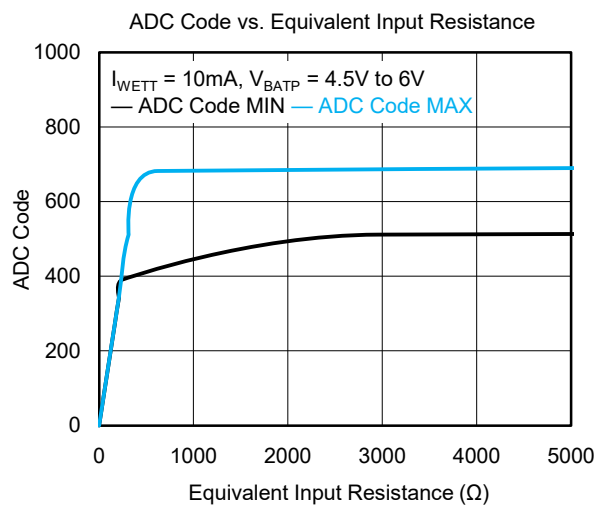
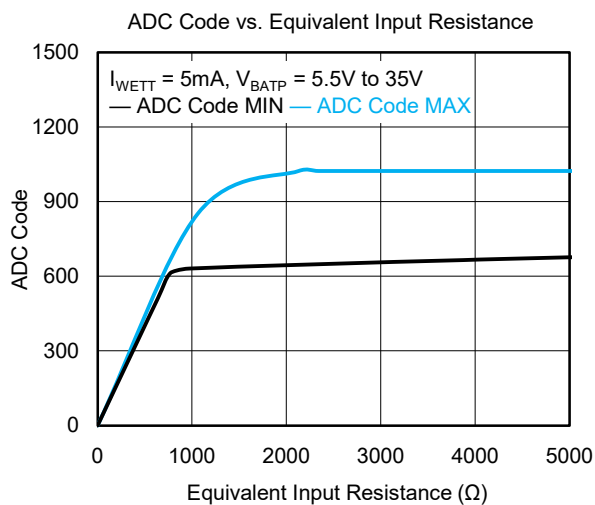
$T_A = +25^\circ\text{C}$, unless otherwise noted.



24-Channel Multiple Switch Detection Interface with SGMCD1024xQ Adjustable Wetting Current for Automotive Applications

TYPICAL PERFORMANCE CHARACTERISTICS (continued) SGMCD1024DQ

$T_A = +25^\circ\text{C}$, unless otherwise noted.



24-Channel Multiple Switch Detection Interface with SGMCD1024xQ Adjustable Wetting Current for Automotive Applications

FUNCTIONAL BLOCK DIAGRAM

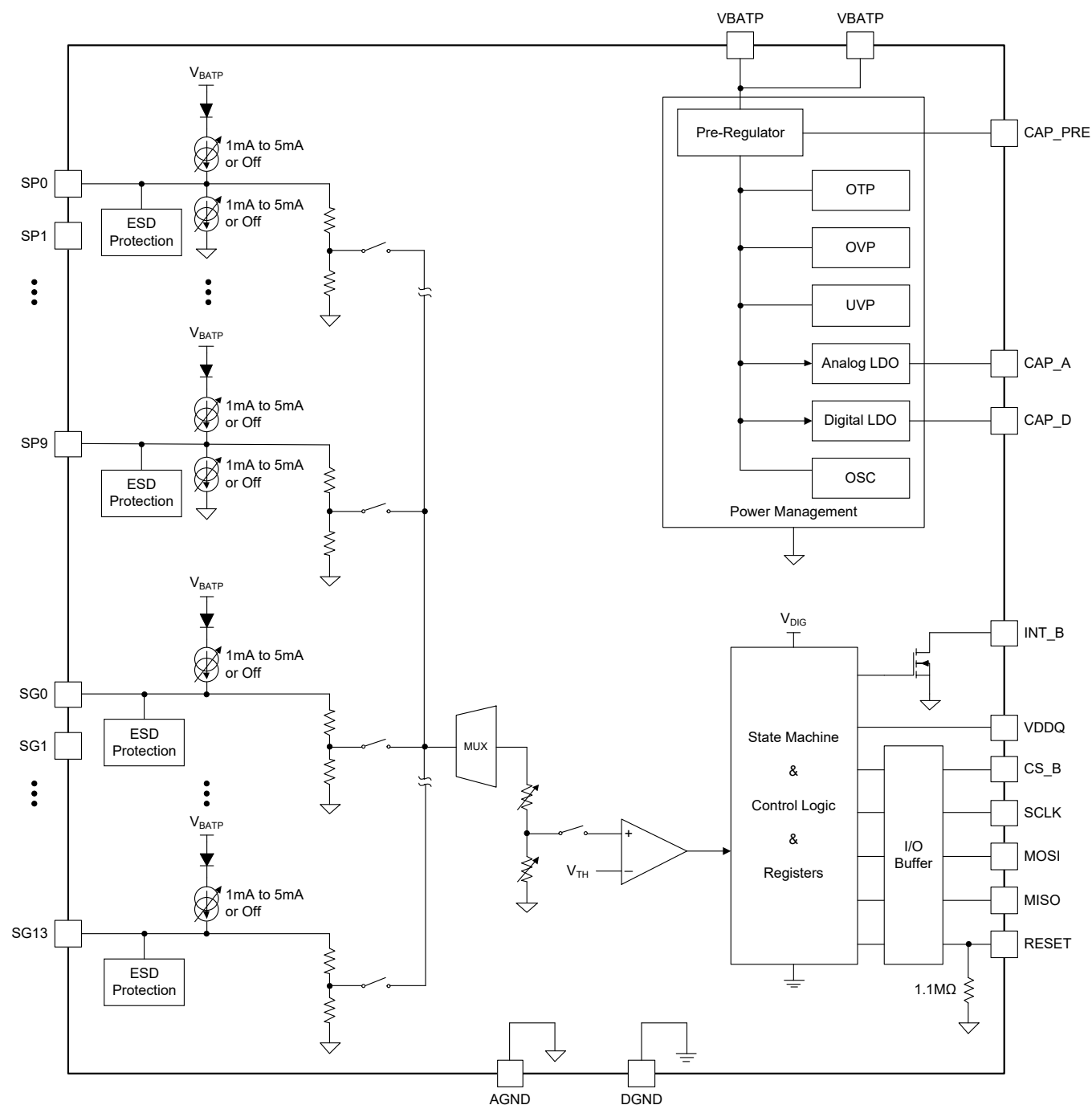


Figure 5. SGMCD1024AQ Block Diagram

24-Channel Multiple Switch Detection Interface with SGMCD1024xQ Adjustable Wetting Current for Automotive Applications

FUNCTIONAL BLOCK DIAGRAM (continued)

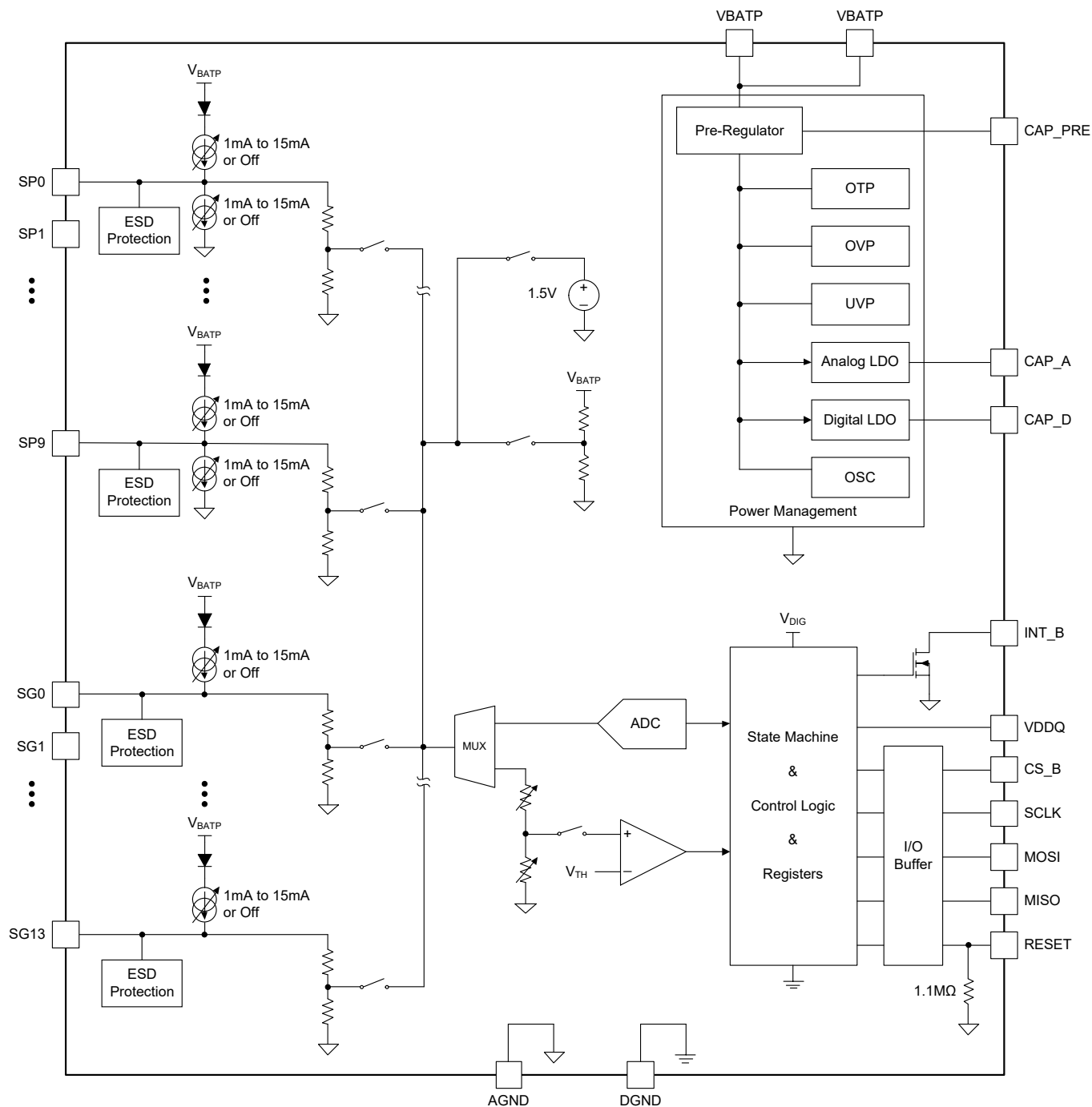


Figure 6. SGMCD1024DQ Block Diagram

24-Channel Multiple Switch Detection Interface with SGMCD1024xQ Adjustable Wetting Current for Automotive Applications

DETAILED DESCRIPTION

Overview

The SGMCD1024xQ device features 24 direct switch inputs, with 10 switch-to-power (SP) inputs, which are configurable to either switch-to-ground (SG) or switch-to-battery (SB), and 14 channels configurable to SG only. Each input supports several distinct programmable wetting current configurations, enabling optimized performance across diverse applications.

To enhance energy efficiency, the system incorporates wake-up functionality for all switches, minimizing the need for sustained MCU activity. This solution integrates advanced protection features including fault detection, ESD protection, and diagnostic capabilities to ensure robust system operation. The device offers dual operational modes — continuous mode and polling mode. Continuous mode provides constant wetting current to detect the switch status. Polling mode employs periodic wetting current activation through a programmable timing interval, drastically reducing power consumption by sampling input statuses at scheduled intervals.

Feature Description

VBATP Pin

The VBATP pin powers the entire chip and generates all internal voltage references. It is intended to connect this pin to the 12V automotive battery via a reverse-polarity blocking diode.

VDDQ Pin

The VDDQ pin sets the SPI logic levels. It furnishes drive current for the MISO output, and defines the pull-up voltage applied to the CS_B pin. Besides VBATP, this supply may act as an alternate external pull-up source for the INT_B pin and may require connection to a logic power rail ranging from 3V to 5.5V. When VDDQ is removed, the SPI operation becomes non-functional while all stored register settings are preserved due to the existing VBATP supply.

Device Initialization

Power-on Reset (POR) describes the scenario when the SGMCD1024xQ powers up, which resets all registers to default values and initializes the internal state machine. The SGMCD1024xQ stays in POR mode until VBATP voltage rises above the V_{POR_R} threshold. After a full initialization, the INT_B pin goes low as an alert signal for the MCU, and the POR status

bit inside the INT_STAT register is set to logic 1. At the same time, the corresponding POR flag is output via the MISO pin of the SPI.

Factory preset values are written into the device throughout the initialization phase to support precise functional behavior. Once these parameters have been loaded, the device runs an internal self-check procedure to confirm successful configuration loading. If the self-check fails, both the CHK_FAIL bit and POR bit in INT_STAT register will assert to logic 1. When this fault happens, it is advised that the MCU issues a software reset. This operation restarts the initialization sequence so that valid factory settings can be re-loaded.

Device Trigger

Once the initialization finishes, the SGMCD1024xQ accepts user-defined configuration. The MCU may employ SPI commands to load target parameters into its configuration registers. After all desired configurations have been written, the TRIGGER bit inside the CONFIG register must be asserted to logic 1, or the wetting current is not generated and the external switch monitoring function is not activated.

When switch monitoring has started, most configuration registers become read-only. Notable exceptions are the TRIGGER, CRC_T and RESET bits of CONFIG register, as well as every bit located within the CCP_CFG1 register. Every time the users need to alter device parameters during runtime, the MCU must first de-assert the TRIGGER bit to logic 0. This action disables the wetting current and terminates ongoing switch monitoring. New values can subsequently be programmed into configuration registers. After re-programming finishes, re-asserting TRIGGER to logic 1 restarts the switch monitoring workflow.

It should be noted that the cyclic redundancy check (CRC) function remains usable even with TRIGGER set to logic 1, which gives the MCU the ability to validate device settings on an ongoing basis. Additional descriptions of the CRC mechanism are provided in section Cyclic Redundancy Check (CRC).

Device Reset

The SGMCD1024xQ supports three separate reset mechanisms, each of which initializes every register content to its default state.

24-Channel Multiple Switch Detection Interface with SGMCD1024xQ Adjustable Wetting Current for Automotive Applications

DETAILED DESCRIPTION (continued)

VBATP POR

Once VBATP voltage decreases below the V_{POR_F} threshold, the device powers off and every stored register data gets erased. Restoration of device operation requires VBATP to rise above V_{POR_R} , which is demonstrated in Figure 7. Following this voltage condition, the SGMCD1024xQ runs through the initialization procedure outlined in section Device Initialization.

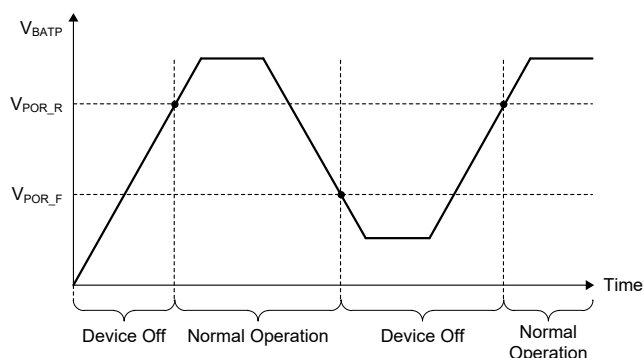


Figure 7. VBATP is Lowered Below the POR Threshold, Then Ramped Back Up to Complete a POR Cycle

Hardware Reset

Hardware reset for the SGMCD1024xQ can be executed by the MCU through toggling the RESET pin. This pin includes an internal 1.1MΩ (TYP) pull-down resistor and must stay low during standard operation. Driving RESET high places the chip into reset condition: most internal modules are disabled, and the device consumes only the low I_{S_RESET} current. In the reset mode, switch monitoring and SPI interfaces halt, and all register data gets cleared. Pulling the RESET pin back low or releasing this pin restores default register settings and restarts the device state machine, reproducing the behavior of a POR event. Once re-initialization finishes, the INT_B pin goes low, and both the POR bit and the POR SPI status flag become logic 1, implying reset completion to the MCU.

Successful reset demands that the RESET pin remains high for no less than t_{RESET} . This pin shall receive defined logic levels (low level below V_{RESET_L} or high above V_{RESET_H}), to guard against undesired reset triggers.

Software Reset

Apart from hardware reset and VBATP POR methods, software reset may be invoked by the MCU using an

SPI command. Writing logic 1 to the RESET bit of the CONFIG register triggers this software reset event, which re-initializes the chip and returns every register to its default configuration. When re-initialization finishes, the INT_B pin is driven low. The POR bit as well as the POR SPI status flag will both become logic 1, informing the MCU that the software reset procedure has concluded.

VBATP Under-Voltage (UV) Condition

In a conventional 12V automotive system operating under normal conditions, the VBATP rail voltage tends to remain stable and well above 11V. Still, temporary voltage sag can happen during certain vehicle operations such as cold cranking. If VBATP decreases below V_{UV_F} , the SGMCD1024xQ enters a UV state because there is inadequate voltage margin to produce accurate wetting currents. The device behaviors under UV condition are listed below:

- ♦ All current source and sink circuits turn off, and switch monitoring stops.
- ♦ An interrupt event is triggered by pulling the INT_B pin low; the UV bit in INT_STAT register is set to logic 1 while the UV_STAT bit inside the IN_STAT_MISC register becomes logic 1. The OI SPI flag is asserted throughout any SPI transaction. The INT_B pin is released and INT_STAT register is cleared on the rising edge of CS_B, on the condition that the INT_STAT register has been read.
- ♦ The SPI communication keeps operating, and all register values are preserved with no reset unless the VBATP voltage drops below V_{POR_F} . Historical switch information can still be retrieved without interruption when needed.

The device continues monitoring VBATP voltage. The UV state persists as long as VBATP voltage stays below V_{UV_R} , and no further interrupt events will be generated once the existing interrupt has been cleared.

When VBATP voltage rises above V_{UV_R} , the INT_B pin goes low to inform the MCU of UV condition recovery. The UV bit of the INT_STAT register is set to logic 1 and the UV_STAT bit of the IN_STAT_MISC register is cleared to logic 0 to signal UV exit. The chip resumes operation based on the current register settings irrespective of INT_B and SPI status; polling restarts from the first enabled channel.

24-Channel Multiple Switch Detection Interface with SGMCD1024xQ Adjustable Wetting Current for Automotive Applications

DETAILED DESCRIPTION (continued)

A Switch State Change (SSC) interrupt occurs at the end of the first polling cycle, and the measured switch state establishes the baseline status used for subsequent polling cycles. After the MCU completes reading the INT_STAT register, the register content is cleared and the INT_B pin deasserts.

Figure 8 depicts how the SGMCD1024xQ behaves across a range of VBATP voltages. For Case 1 where V_{BATP} stays above V_{UV_F} , the chip operates normally. In Case 2, V_{BATP} drops beneath V_{UV_F} but remains higher than V_{POR_F} , causing the device to enter UV condition. Case 3 occurs when V_{BATP} falls below V_{POR_F} ; the device undergoes a full reset and all register settings are cleared. Once V_{BATP} returns to a valid level, the MCU must rewrite all configuration registers before normal operation can be resumed.

VBATP Over-Voltage (OV) Condition

The SGMCD1024xQ activates an over-voltage (OV) protection state once the VBATP voltage exceeds V_{OV_R} . This mechanism safeguards the internal structures of the device, as well as the VBATP and SPx pins used for battery-connected switches against electrical damage. The device operates with the following behaviors during OV events:

- All current source and sink functions are disabled, and the switch monitoring function stops completely.
- An interrupt event is triggered with the INT_B pin going to a low level. Meanwhile, the OV bit of the INT_STAT register and the OV_STAT bit of the IN_STAT_MISC register are set to logic 1, and the OI SPI flag is asserted throughout any ongoing SPI communication. The INT_B pin is de-asserted and the INT_STAT register is cleared at the CS_B rising edge, on the premise that the MCU reads the INT_STAT register during the current SPI transaction.

- The SPI interface maintains normal operation, and all register parameters are preserved without any reset. Previously recorded switch status can be acquired continuously without interruption.
- The device keeps real-time monitoring of VBATP voltage. The OV state remains valid if V_{BATP} stays higher than $V_{OV_R} - V_{OV_HYST}$, and no new interrupts will be issued after the initial interrupt flag is cleared.

Once V_{BATP} drops below $V_{OV_R} - V_{OV_HYST}$, the INT_B pin is pulled low to inform the MCU that the OV condition has been eliminated. The OV bit of the INT_STAT register is set to logic 1 and the OV_STAT bit of the IN_STAT_MISC register is cleared to logic 0 to mark OV state recovery. The device resumes operation with all current register configurations, regardless of INT_B and SPI operating status, and restarts polling starting from the first enabled channel. After the first polling cycle finishes, a SSC interrupt is generated, and the newly detected switch status acts as the baseline for subsequent polling operations. After the MCU reads the INT_STAT register, the register data is cleared and the INT_B pin returns to the default state.

Switch Inputs Settings

SPx/SGx are input pins wired to external mechanical switches, detecting the switch condition of open or closed and storing this information within the status registers. Table 1 below details the different configurable options available for each input channel. It should be noted that several configuration parameters apply to a group of multiple inputs. As outlined in the Device Trigger section, any configuration modification requires stopping device operation first by clearing the TRIGGER bit inside the CONFIG register.

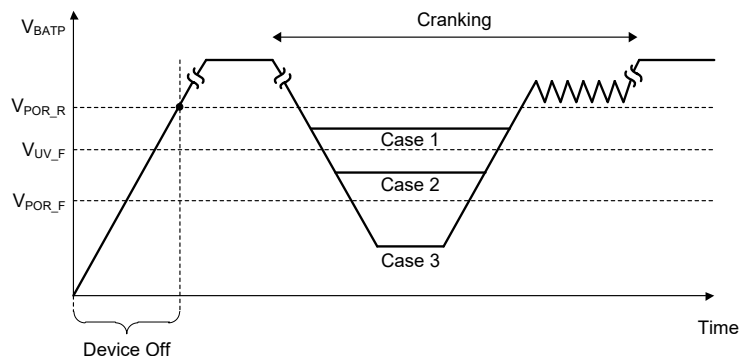


Figure 8. SGMCD1024xQ Operation at Various VBATP Voltage Levels

24-Channel Multiple Switch Detection Interface with SGMCD1024xQ Adjustable Wetting Current for Automotive Applications

DETAILED DESCRIPTION (continued)

Table 1. SGMCD1024xQ Wetting Current and Threshold Setting Details

Input	Threshold		Wetting Current	Current Source (CSO) /Current Sink (CSI)	Supported Switch Type
	Comparator Input Mode	ADC Input Mode			
SP0	THRES_COMP_SP0_SP3	THRES0 to THRES7	WC_SP0_SP1	CSO CSI	Switch to GND Switch to VBATP
SP1		THRES0 to THRES7		CSO CSI	Switch to GND Switch to VBATP
SP2		THRES0 to THRES7	WC_SP2_SP3	CSO CSI	Switch to GND Switch to VBATP
SP3		THRES0 to THRES7		CSO CSI	Switch to GND Switch to VBATP
SP4	THRES_COMP_SP4_SP7	THRES0 to THRES7	WC_SP4	CSO CSI	Switch to GND Switch to VBATP
SP5		THRES0 to THRES7	WC_SP5	CSO CSI	Switch to GND Switch to VBATP
SP6		THRES0 to THRES7	WC_SP6_SP7	CSO CSI	Switch to GND Switch to VBATP
SP7		THRES0 to THRES7		CSO CSI	Switch to GND Switch to VBATP
SP8	THRES_COMP_SP8_SG1	THRES0 to THRES7	WC_SP8_SP9	CSO CSI	Switch to GND Switch to VBATP
SP9		THRES0 to THRES7		CSO CSI	Switch to GND Switch to VBATP
SG0		THRES0 to THRES7	WC_SG0	CSO	Switch to GND
SG1		THRES0 to THRES7	WC_SG1	CSO	Switch to GND
SG2	THRES_COMP_SG2_SG5	THRES2A, THRES2B	WC_SG2_3	CSO	Switch to GND
SG3		THRES2A, THRES2B		CSO	Switch to GND
SG4		THRES2A, THRES2B	WC_SG4_5	CSO	Switch to GND
SG5		THRES2A, THRES2B		CSO	Switch to GND
SG6	THRES_COMP_SG6_SG9	THRES2A, THRES2B	WC_SG6_7	CSO	Switch to GND
SG7		THRES2A, THRES2B		CSO	Switch to GND
SG8		THRES3A, THRES3B, THRES3C	WC_SG8_9	CSO	Switch to GND
SG9		THRES3A, THRES3B, THRES3C		CSO	Switch to GND
SG10	THRES_COMP_SG10_SG13	THRES3A, THRES3B, THRES3C	WC_SG10_11	CSO	Switch to GND
SG11		THRES3A, THRES3B, THRES3C		CSO	Switch to GND
SG12		THRES3A, THRES3B, THRES3C	WC_SG12	CSO	Switch to GND
SG13		THRES3A, THRES3B, THRES3C, THRES8, THRES9	WC_SG13	CSO	Switch to GND

Input Current Source and Sink Selection

The SGMCD1024xQ is a multiple switch detection interface (MSDI) which can detect the switch status change of 14 switch-to-ground (SG) inputs and 10 switch-to-power (SP) inputs. The SP input can be configured as switch-to-battery (SB) input or SG input through the CS_SELECT register. From the aspect of wetting current, the SB input is equal to current sink (CSI) while the SG input is equal to current source (CSO). Following a POR event, SP0 to SP9 are preset to monitor SG switches with current sources enabled.

Input Mode Selection

The SGMCD1024xQ incorporates an internal ADC and comparator to support the monitoring of resistor-coded switches or digital switches. Digital switch signals possess merely open and closed states, and these two states can be reliably sensed by the comparator. Resistor-coded switches have several distinct positions to identify, making the ADC suitable for capturing these varied states.

24-Channel Multiple Switch Detection Interface with SGMCD1024xQ Adjustable Wetting Current for Automotive Applications

DETAILED DESCRIPTION (continued)

Depending on the external switch wiring setup, each input of the SGMCD1024xQ may be separately assigned to comparator mode or ADC mode by configuring the corresponding bits in the MODE register. Compared with the ADC mode, the comparator mode delivers faster polling for digital switches; this reduces polling duration and helps cut overall power consumption when the chip runs in low-power polling mode.

All enabled inputs default to comparator mode after device reset.

Input Enable Selection

The SGMCD1024xQ supports switch state monitoring on up to 24 input channels, yet some applications do not require continuous monitoring of every available input. The MCU can turn the monitoring function of selected inputs on or off through the configuration of the IN_EN register. Clearing the corresponding bit to logic 0 disables the wetting current source and sink, and halts switch status monitoring for that input. Turning off unused input monitoring helps reduce the total operating current.

Upon device reset, all inputs are disabled by default.

Thresholds Adjustment

For inputs operating in comparator mode, users can define the interrupt generation threshold through the THRES_COMP register from one of 2V, 2.7V, 3V, and 4V. Threshold parameters are set on a group basis, with every group containing four input channels.

When an input is configured as ADC mode, the interrupt threshold can be adjusted to any of 1024 levels spanning the range from 0 to 1023 by writing to the THRES_CFG1 and THRES_CFG2 registers. Separate threshold values may be assigned to each input within SP0 to SG1. Besides individual thresholds, a shared common threshold applicable to all SP0 ~ SG1 channels can be configured via the THRES_COM bits in the MATRIX register, and this common threshold works separately from THRES0 to THRES7. SG2 to SG7 rely on two preset thresholds: THRES2A and THRES2B. SG8 to SG12 use three preset thresholds: THRES3A, THRES3B and THRES3C. SG13 uses five

preset thresholds including THRES3A, THRES3B, THRES3C, THRES8 and THRES9.

When multiple thresholds are deployed for ADC inputs, careful configuration of these threshold levels is required. Adopt the rules listed below (see Table 2) during threshold configuration:

Table 2. Proper Threshold Configuration for ADC Inputs

Input	Proper Threshold Configuration
SG2 to SG7	THRES2B ≥ THRES2A
SG8 to SG12	THRES3C ≥ THRES3B ≥ THRES3A
SG13	THRES9 ≥ THRES8 ≥ THRES3C ≥ THRES3B ≥ THRES3A

Special attention is required for threshold programming when working with battery-side external switches. Current sinks introduce inherent voltage drop, which peaks at $V_{SB_DROP_OPEN}$ for 10mA and 15mA wetting current configurations. This means an open switch does not guarantee a near-zero voltage at the SPx pin; the pin voltage can still rise to $V_{SB_DROP_OPEN}$, requiring designers to set detection thresholds higher than this level.

Leakage on an open switch can also compromise the pull-down performance of low-magnitude wetting current sinks, demonstrated in Figure 9. The example models an open switch with significant leakage using a 5kΩ R_{DIRT} resistor. Under this scenario, activating the 2mA current sink can only reduce the SPx voltage to 4V, even though the switch stays open.

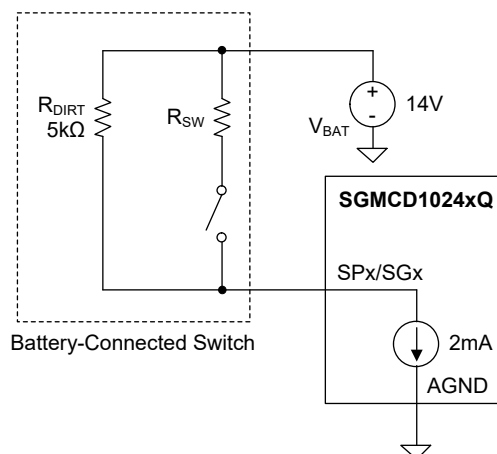


Figure 9. Example Showing the Calculation of the SPx/SGx Pin Voltage for a Leaky Battery-Connected Switch

24-Channel Multiple Switch Detection Interface with SGMCD1024xQ Adjustable Wetting Current for Automotive Applications

DETAILED DESCRIPTION (continued)

Table 3. Recommended Threshold Configuration When Using an ADC Input to Monitor Digital Switches

Input	RECOMMENDED THRESHOLD CONFIGURATION
SP0 to SG1	Configure the desired threshold to one of the settings from THRES0 to THRES7 and map it accordingly.
SG2 to SG7	Configure the desired threshold to THRES2B. Set THRES2A to the same code as THRES2B. Disable interrupt generation for THRES2A by configuring the INT_EN_CFG1 or INT_EN_CFG2 register.
SG8 to SG12	Configure the desired threshold to THRES3C. Set THRES3A and THRES3B to the same code as THRES3C. Disable interrupt generation for THRES3A and THRES3B by configuring the INT_EN_CFG3 or INT_EN_CFG4 register.
SG13	Configure the desired threshold to THRES9. Set THRES3A, THRES3B, THRES3C, and THRES8 to the same code as THRES9. Disable interrupt generation for THRES3A, THRES3B, THRES3C, and THRES8 by configuring the INT_EN_CFG4 register.

Single-threshold digital switches can also be monitored by setting the input to ADC mode instead of the comparator mode. The recommended programming steps for this setup are listed in Table 3 above.

Wetting Current Configuration

Users can select from six wetting current levels of 0mA, 1mA, 2mA, 5mA, 10mA and 15mA for SGMCD1024DQ or four wetting current levels of 0mA, 1mA, 2mA and 5mA for SGMCD1024AQ, programmed via the WC_CFG0 and WC_CFG1 registers, with 0mA as the default state after device reset.

When measuring resistor coded switches, lower wetting currents of 1mA, 2mA or 5mA are usually the better choice. They maintain adequate voltage resolution to tell apart multiple switch positions and ensure the resulting input voltages stay inside the ADC full-scale range. The higher current settings of 10mA and 15mA serve a different purpose: they clear oxide layers that accumulate on exposed open switch contacts. If contact cleaning is needed for resistor-coded switches, users can turn on the clean current polling (CCP) feature. The CCP function injects short high-current cleaning pulses at the end of every polling cycle on a recurring basis.

At low V_{BATP} conditions, V_{BATP} exerts a more pronounced impact on wetting current precision. Reducing V_{BATP} increases the gap between actual wetting current and its nominal value.

Interrupt Generation and INT_B Assertion

Events captured by the SGMCD1024xQ — such as SSC, TW, TSD and OV events — will pull the

open-drain, active-low INT_B pin to a low logic level. A pull-up resistor tied to VDDQ must be added externally to this pin, as shown in Figure 10. For MCU wake-up implementation, you can wire INT_B straight to a 12V vehicle battery.

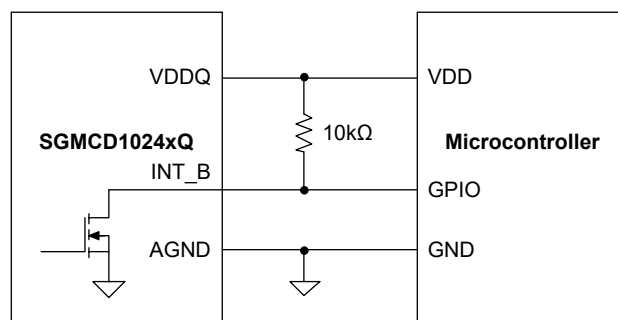


Figure 10. INT_B Connection Example #1

INT_B Pin Assertion Scheme

Designers can pick the behavior between static and dynamic modes for INT_B assertion on the SGMCD1024xQ, with the mode selection handled by the INT_CONFIG bit in the CONFIG register.

In static mode, activated by setting INT_CONFIG to 0, any detected event pulls INT_B to its active low state. Release of the INT_B signal at the CS_B rising edge only takes place if a READ access to INT_STAT happens during the low phase of CS_B. Without such a read operation, INT_B remains latched low. The register values inside INT_STAT are sampled on the first rising SCLK edge after CS_B falls for every SPI transaction, and a READ operation to INT_STAT clears the latched event information, which is visualized in Figure 11.

DETAILED DESCRIPTION (continued)

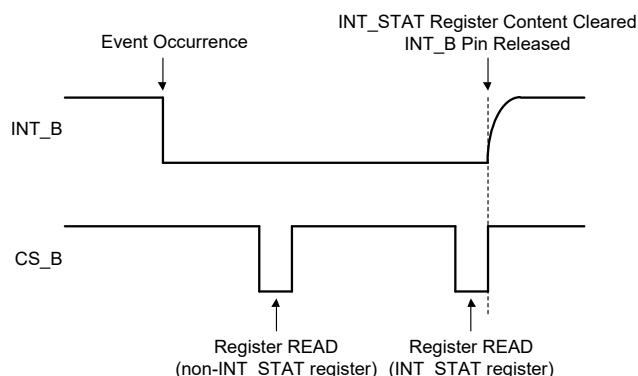


Figure 11. Static INT_B Assertion Scheme

Systems employing edge-triggered MCUs are prone to failing to detect INT_B events under static interrupt configuration, a scenario that occurs frequently during MCU wake-up stages. The SGMCD1024xQ adopts a dynamic INT_B assertion mechanism to solve this problem, effectively eliminating interrupt loss and improving system interrupt stability.

This dynamic mode is activated via the INT_CONFIG bit in the CONFIG register (set to 1). In this mode, INT_B outputs a low-level active signal that lasts for t_{INT_ACTIVE} . The device pulls INT_B high if no INT_STAT register read is completed within the active window, maintains the high state for $t_{INT_INACTIVE}$, and then reactivates the low-level interrupt signal. This cycle repeats continuously until the MCU reads the INT_STAT register to confirm the interrupt.

The device behaves differently based on the INT_B pin state during register reading. Reading the INT_STAT register while INT_B is low clears the register data and deasserts INT_B upon the CS_B rising edge (Figure 12). Reading the INT_STAT register during the INT_B high state also clears the register at the CS_B rising edge, but the device will not re-trigger the INT_B low signal afterwards (Figure 13).

The device defaults to the static INT_B assertion scheme after reset. Engineers can only switch the INT_B assertion mode when the TRIGGER bit of the CONFIG register is configured to logic 0.

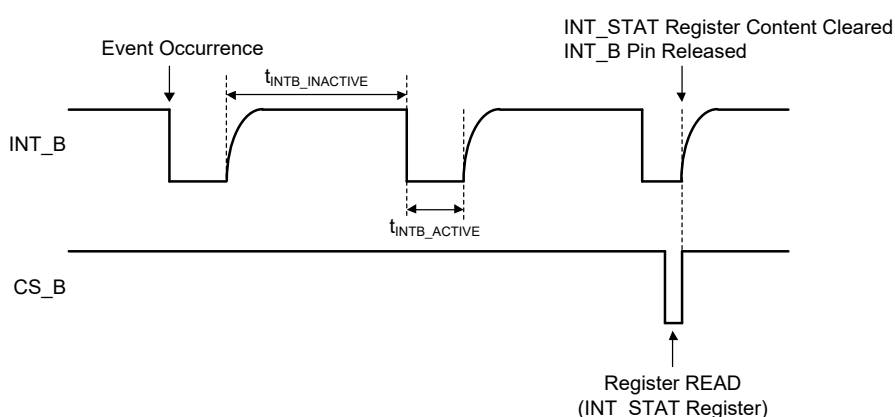


Figure 12. Dynamic INT_B Assertion Scheme with INT_STAT Register Read During t_{INT_ACTIVE}

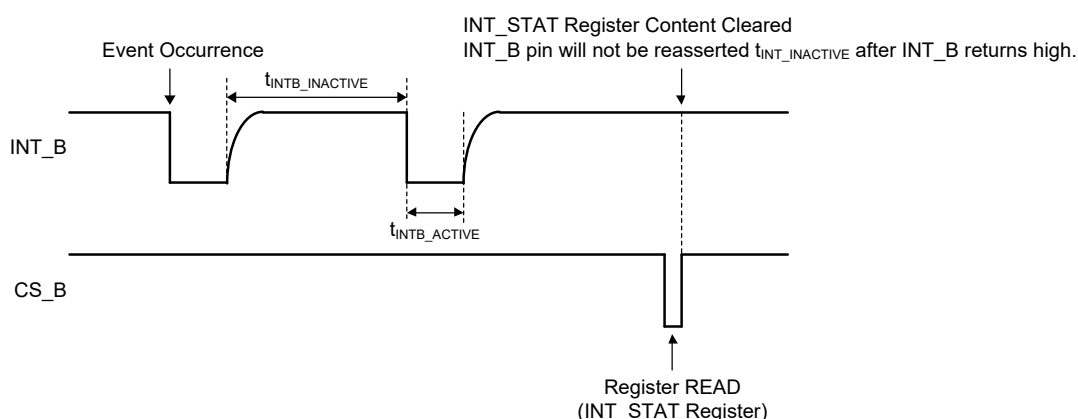


Figure 13. Dynamic INT_B Assertion Scheme with INT_STAT Register Read During $t_{INT_INACTIVE}$

24-Channel Multiple Switch Detection Interface with SGMCD1024xQ Adjustable Wetting Current for Automotive Applications

DETAILED DESCRIPTION (continued)

Interrupt Idle Time (t_{INTB_IDLE}) Time

A timing interval known as t_{INTB_IDLE} is built into the SGMCD1024xQ for interrupt handling. It reserves adequate time for the external pull-up resistor to restore the INT_B pin to the high state. This setup guarantees that edge-triggered MCUs can recognize the next interrupt assertion, while also lowering the likelihood of glitches on INT_B when multiple events take place one after another.

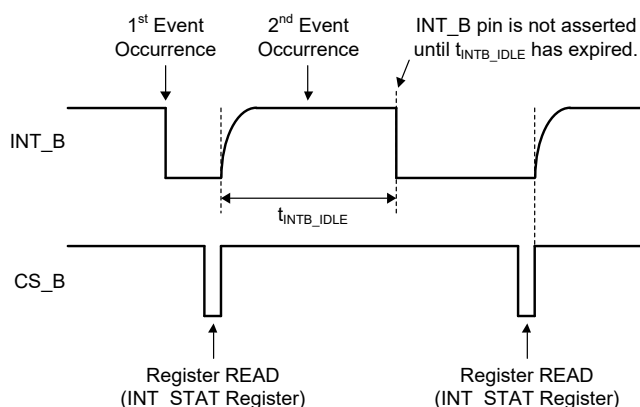


Figure 14. INT_B Assertion Scheme with t_{INTB_IDLE}

For unmasked pending interrupt events, the SGMCD1024xQ starts the t_{INTB_IDLE} count-down procedure once the MCU executes a READ operation on the INT_STAT register. Any new event triggered during this idle window will refresh the INT_STAT

register at once, but the INT_B pin will not drop to the active-low level until t_{INTB_IDLE} finishes. If the MCU sends another READ command targeting INT_STAT while t_{INTB_IDLE} is still running, the register flags get cleared instantly. When the idle period ends, the device will not pull INT_B low again. Figure 14 illustrates how the INT_B pin behaves within the static interrupt assertion scheme.

Microcontroller Wake-Up

Designers can leverage the INT_B pin for wake-up functions with only a handful of external passive and active parts. The INT_B pin activates a voltage regulator via the regulator EN pin. A reference circuit for this topology is provided in Figure 15. This approach excels at waking MCUs and enables large reductions in overall current consumption.

While waiting for a wake trigger, the INT_B pin exhibits high impedance. The MCU maintains sleep state with all GPIO outputs at logic low. This keeps Q_2 turned off because its base is low. A weak pull-up tied to VBATP holds Q_1 base high, which leaves Q_1 off. The resulting low LDO_EN signal shuts down the regulator output V_{OUT} . Without V_{DDQ} (V_{OUT}), neither the SGMCD1024xQ nor the MCU receives this supply rail, and SPI operations cannot run. Importantly, the chip still carries out switch monitoring functions during this time.

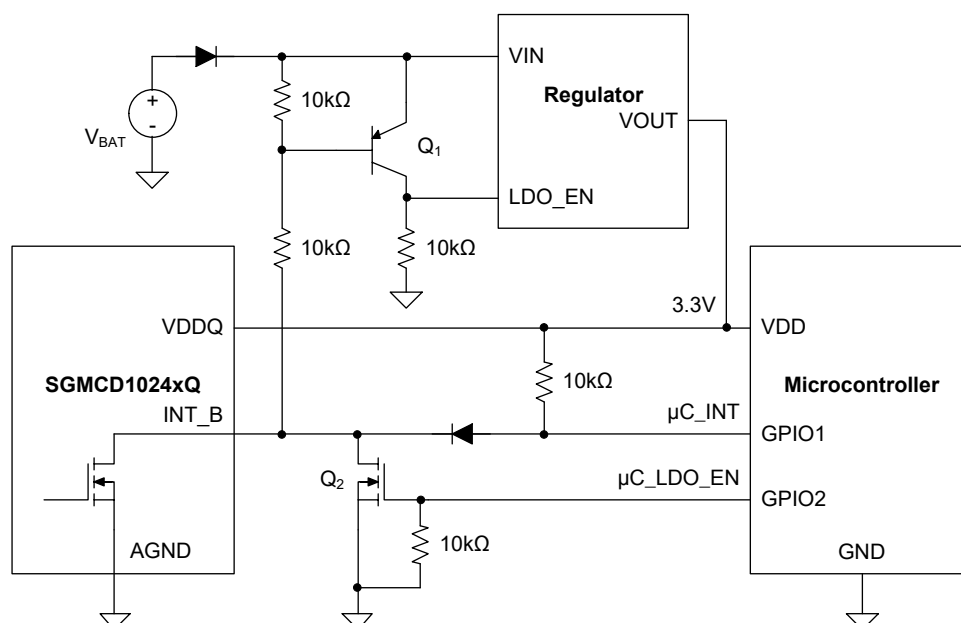


Figure 15. INT_B Connection to Support Microcontroller Wake-Up

24-Channel Multiple Switch Detection Interface with SGMCD1024xQ Adjustable Wetting Current for Automotive Applications

DETAILED DESCRIPTION (continued)

Events like SSC, TW, OT, or OV conditions drive INT_B pin to logic low. The low level switches Q₁ on and powers up the voltage regulator, which brings the MCU out of sleep and restores SPI communications between the MCU and the SGMCD1024xQ. The MCU can then fetch saved event details over the SPI bus.

Designers should keep in mind that reading the INT_STAT register deasserts INT_B pin. After this READ operation, the MCU needs to pull μ C_LDO_EN high manually to maintain the regulator in an enabled state. This preserves the VDDQ supply rail for MCU operation and keeps SPI communication available.

This wake-up topology is only valid when the INT_B is set to static assertion mode.

Interrupt Enable/Disable and Interrupt Generation Conditions

Designers may turn interrupts on or off for each switch input state change by programming dedicated registers. INT_EN_COMP1 and INT_EN_COMP2 control interrupts for comparator inputs, while INT_EN_CFG1 to INT_EN_CFG4 are assigned to ADC inputs. Users can modify the IN_COM_EN bit in the MATRIX register to adjust the THRES_COM interrupt condition for SP0 to SG1.

These registers further support the following interrupt trigger modes:

1. Rising edge: Interrupt occurs if the present sampled input value rises above the threshold, while the preceding sample was below it.
2. Falling edge: Interrupt occurs if the present sampled input value falls below the threshold, while the preceding sample was above it.
3. Both edges: Any bidirectional shift of the input voltage will trigger an interrupt event.

Upon factory reset, all switch-change interrupt functions are disabled by default.

Detection Filter

The detection filter for switch monitoring is set via the DET_FILTER bits in the CONFIG register. It outputs an SSC interrupt only after repeated consecutive samples confirm the same threshold-related input state, effectively removing switch bounce during switching transitions. SSC interrupt can be triggered when the input voltage crosses the threshold and maintains a stable threshold status across no fewer than 0 ~ 3 polling cycles through setting the DET_FILTER bits in the CONFIG register.

Regardless of whether the detection filter (configured through the DET_FILTER bits in the CONFIG register) is activated or not, the SGMCD1024xQ latches the initial switch status internally after the first detection cycle. The example below assumes DET_FILTER bits in the CONFIG register are set to 11. Under this setting, an SSC interrupt fires once the input crosses the threshold and keeps a stable threshold-related state across a minimum of four detection cycles. In this scenario, the switch change is identified in the 3rd detection cycle and holds the same state for the following three cycles.

No matter whether inputs operate in ADC mode or comparator mode, the detection filter will work for every enabled channel. Pulling the DET_FILTER bits in the CONFIG register to logic 0 clears the detection filter counter to zero. The factory-set configuration of the detection filter triggers an SSC interrupt whenever a threshold crossing occurs after device reset.

Note that the common threshold THRES_COM is excluded from detection filter processing.

Table 4. Example of Detection Filter Operation

Detection Cycle	1	2	3	4	5	6
Event	1) Default Switch Status Store 2) INT_B Asserted 3) SSC Flagged	—	Switch Status Change Detected	—	—	1) INT_B Asserted 2) SSC Flagged

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DETAILED DESCRIPTION (continued)

Temperature Monitor

Enabling high wetting current together with multiple closed switch inputs will introduce significant power dissipation and cause the SGMCD1024xQ to heat up. Built-in temperature monitoring and protection logic can switch the device to low-power operation to protect it from overheat damage. There are two integrated thermal protection functions: Temperature Warning (TW) and Temperature Shutdown (TSD). The triggering temperatures and hysteresis are specified in Table 5 below.

Table 5. Temperature Monitoring Characteristics

Parameter	MIN	TYP	MAX	UNIT
Temperature Warning Trigger Temperature (T_{TW})	130	141	152	°C
Temperature Shutdown Trigger Temperature (T_{TSD})	148	159	170	°C
Temperature Hysteresis (T_{HYS}) for T_{TW} and T_{TSD}		16		°C

Temperature Warning (TW)

Once the chip temperature rises past the temperature warning trigger point T_{TW} , the SGMCD1024xQ carries out the following actions:

- An interrupt is issued by pulling INT_B low, and the TW bit of INT_STAT is latched to logic 1. The SPI TEMP flag will be asserted to logic 1 during every SPI access.
- The TW_STAT bit located in IN_STAT_MISC register is set to logic 1.
- When the TW_CUR_DIS_CSO bit in CONFIG register is 0 (default condition), the wetting current for 10mA and 15mA configurations will drop to 2mA for SGMCD1024DQ while the wetting current for 5mA configuration will drop to 2mA for SGMCD1024AQ. Channels programmed with 0mA, 1mA, 2mA or 5mA keep their preset wetting current unchanged for SGMCD1024DQ, while 0mA, 1mA or 2mA keep their preset wetting current unchanged for SGMCD1024AQ.
- This wetting current lower setting persists so long as the junction temperature stays higher than $T_{TW} - T_{HYS}$.

Provided the INT_STAT register is read during the CS_B low phase, INT_B deasserts to logic high and INT_STAT register data gets cleared upon the rising edge of CS_B. The SGMCD1024xQ maintains

temperature monitoring, but it will not generate further interrupts as long as temperature remains higher than $T_{TW} - T_{HYS}$. The TW_STAT bit in the IN_STAT_MISC register remains at logic 1 while the thermal warning condition persists.

Users can turn off the wetting current scaling function by programming the TW_CUR_DIS_CSO bit or TW_CUR_DIS_CSI bit in the CONFIG register to 1. It should be noted that a temperature warning event can still trigger the interrupt even with this setting while wetting current stays unchanged. This option works for both polling and continuous operating modes.

Note that if this function is enabled, switch measurement results may be influenced when the T_{TW} event reduces wetting current from 10mA or 15mA to 2mA for SGMCD1024DQ or from 5mA to 2mA for SGMCD1024AQ.

Once temperature drops below $T_{TW} - T_{HYS}$, INT_B is pulled low again if it has been released, informing the MCU that the thermal warning state has terminated. The TW bit in the INT_STAT register is set to logic 1, and the TW_STAT bit in the IN_STAT_MISC register returns to logic 0. The chip restores operation with its pre-programmed current settings regardless of INT_B and CS_B states.

Temperature Shutdown (TSD)

When the SGMCD1024xQ is already under the TW condition and junction temperature further increases past T_{TSD} , the SGMCD1024xQ activates Temperature Shutdown (TSD) and carries out the following actions:

- All switches are opened to avoid extra heat generation from internal wetting current.
- The device asserts INT_B low (if not already active) to issue an interrupt, and latches the TSD bit in the INT_STAT register to logic 1. The SPI TEMP flag will be set to logic 1 during every SPI access.
- The TSD_STAT bit in the IN_STAT_MISC register is set to logic 1, and the TW_STAT bit retains its logic 1 state.
- The SPI interface continues operation, and no register values are cleared or reset. Prior switch status information remains available for retrieval.
- This state is maintained as long as the junction temperature remains higher than $T_{TSD} - T_{HYS}$.

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DETAILED DESCRIPTION (continued)

If the INT_STAT register is read during the CS_B low interval, INT_B deasserts to logic high and the INT_STAT register is cleared on the rising edge of CS_B. The SGMCD1024xQ keeps tracking junction temperature, yet no additional interrupt events will occur as long as the temperature stays higher than $T_{TSD} - T_{HYS}$. The TSD_STAT bit in the IN_STAT_MISC register latches to logic 1 throughout the TSD state.

After the temperature drops below $T_{TSD} - T_{HYS}$, INT_B is pulled low again if it has been released, alerting the MCU that the thermal shutdown state has ended. The TSD bit in the INT_STAT register is set to logic 1. In the IN_STAT_MISC register, TSD_STAT is deasserted to logic 0, while TW_STAT remains at logic 1. If the temperature is still above $T_{TW} - T_{HYS}$, the chip recovers and operates under the wetting current rules defined in the Temperature Warning section.

Note that channel polling restarts from the first enabled input. An SSC interrupt fires once the first polling cycle finishes. The switch status captured during this first cycle becomes the reference default status for all later polling.

Parity Check and Parity Generation

Parity bit validation is deployed on the SGMCD1024xQ to protect SPI communication and prevent data corruption between the chip and SPI controller.

Odd parity is applied for outgoing MISO data: the parity bit value is chosen to make the sum of logic-1 bits across the entire transmitted word (parity bit included) odd, which satisfies $\text{Bit0} \oplus \text{Bit1} \oplus \dots \oplus \text{Bit30} \oplus \text{Bit31} \oplus \text{Parity} = 1$.

When receiving data from the SPI controller over MOSI pin, the chip runs the same odd parity check. An even count of logic-1 bits (parity bit counted) results in dropping the received data. INT_B pulls low and the PRTY_FAIL bit in the INT_STAT register latches to logic

1 to alert the MCU about this communication error. The PRTY_FAIL flag will also be active throughout the SPI communication.

Cyclic Redundancy Check (CRC)

The SGMCD1024xQ integrates a CRC module for performing redundancy verification of configuration registers to safeguard data integrity. The CRC computation follows the ITU-T X.25 specification, utilizing the polynomial $0x1021$. This algorithm is widely referred to as CRC-16-CCITT, originating from the ITU-T (previously CCITT) committee. The CRC calculation rule is defined in Table 6.

Table 6. CRC Calculation Rule

CRC Rule	Value
CRC Result Width	16 bits
Polynomial	$x^{16} + x^{12} + x^5 + 1$ (1021h)
Initial (Seed) Value, First Time	FFFFh
Initial (Seed) Value	Last CRC Result
Input Data Reflected	No
Result Data Reflected	No
XOR Value	0000h

CRC computation covers all configuration registers from the CONFIG register through the MODE register. Every reserved bit within configuration registers is not included. The CRC operation is initiated by setting the CRC_T bit in the CONFIG register. Upon calculation completion, the CRC_CALC interrupt bit inside the INT_STAT register is asserted to trigger an interrupt. The 16-bit CRC result is stored within the CRC register. This interrupt may be masked by clearing the CRC_CALC_EN bit in the INT_EN_CFG0 register. Writing to configuration registers while CRC computation is in progress shall be avoided to prevent erroneous CRC results.

Figure 16 illustrates the block diagram of the CRC module.

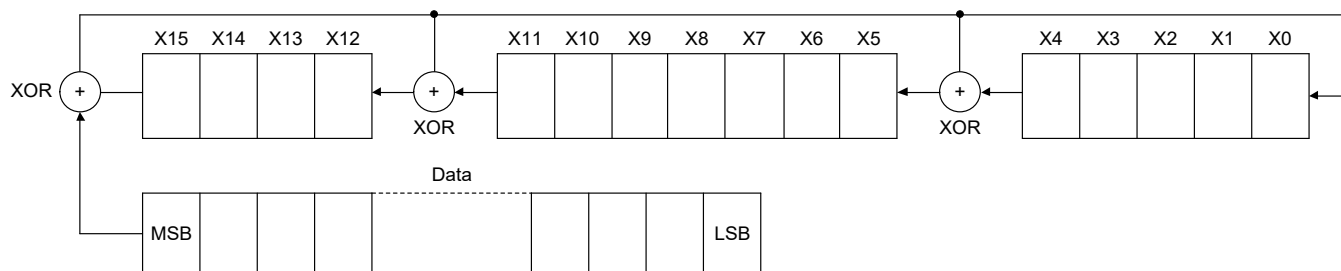


Figure 16. CCITT-16 CRC Module Block Diagram

24-Channel Multiple Switch Detection Interface with SGMCD1024xQ Adjustable Wetting Current for Automotive Applications

DETAILED DESCRIPTION (continued)

This module comprises 16 shift registers and 3 exclusive-OR gates. The shift registers initialize to 1111 1111 1111 1111 (FFFFh). The module executes XOR operations and shifts stored data sequentially until processing the final bit of the register sequence. The value held in the shift registers after the last data bit is processed represents the computed CRC of the dataset, which is saved into the CRC register.

Once the CRC computation finishes, the CRC_T bit will automatically clear. This bit stays at logic 1 for the duration of the CRC calculation process.

Device Functional Modes

Two distinct operating modes are available in the SGMCD1024xQ: continuous mode and polling mode. The following paragraphs provide detailed descriptions of both modes, along with a set of advanced features which can be activated while the device runs normally.

Continuous Mode

When operating in continuous mode, all activated input channels receive constant wetting current, and the device samples channel states in sequence starting at SP0 and ending at SG13. The SGMCD1024xQ keeps tracking enabled channels and triggers an interrupt if a

switch state change is detected and interrupts are turned on. Users can set wetting current separately per channel through WC_CFG0 and WC_CFG1, selecting from 0mA, 1mA, 2mA, 5mA, 10mA and 15mA for SGMCD1024DQ or 0mA, 1mA, 2mA and 5mA for SGMCD1024AQ. Whether a channel takes comparator or ADC for monitoring is defined by the input mode bit in the MODE register.

The timing diagram in Figure 17 demonstrates the detection sequence behavior in continuous mode. When the TRIGGER bit in the CONFIG register is set to logic 1, the device waits for $t_{STARTUP}$ before enabling the wetting current for all enabled inputs. The wetting current stays active continuously, and the device switches each input to the ADC or comparator for sampling one after another. Once conversion and comparison are finished for an input, its switch status (above or below the detection threshold) is written to status registers: IN_STAT_COMP for comparator channels or IN_STAT_ADC0 ~ IN_STAT_ADC1 for ADC channels. This stored status acts as the reference state for later detection cycles. For channels set to ADC input mode, the digital conversion results are stored in ANA_STAT0 ~ ANA_STAT11.

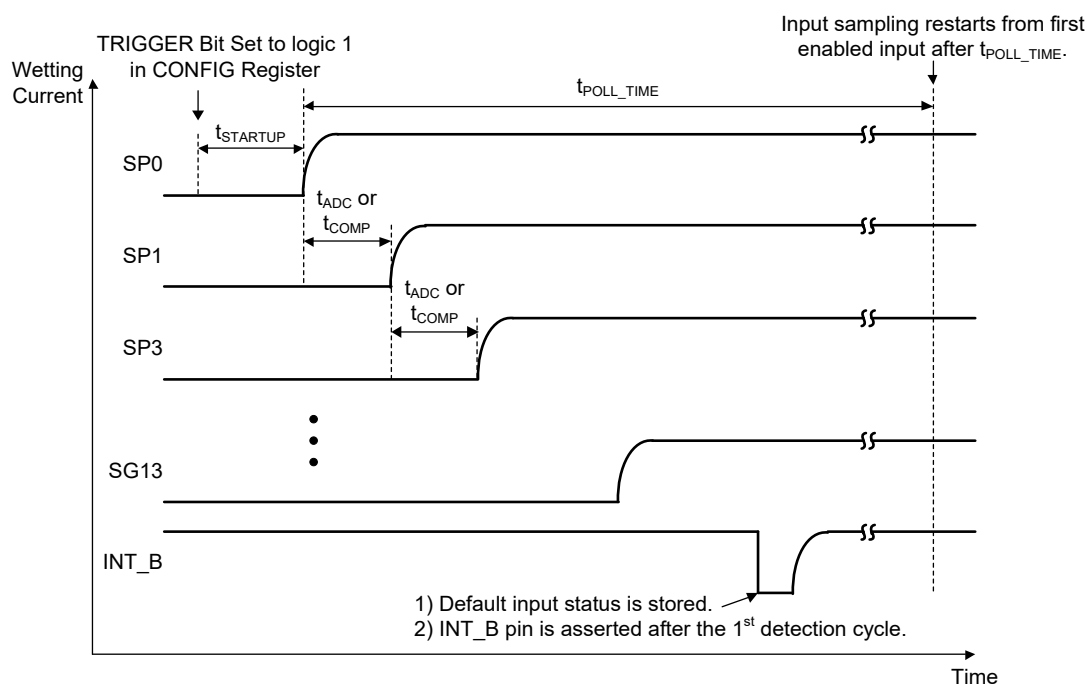


Figure 17. An Example of the Detection Sequence in Continuous Mode

24-Channel Multiple Switch Detection Interface with SGMCD1024xQ Adjustable Wetting Current for Automotive Applications

DETAILED DESCRIPTION (continued)

When the first polling cycle finishes, INT_B pulls low to inform the MCU that default switch status can be read. The SSC bit in the INT_STAT register and the SSC flag in SPI are set to logic 1. The polling cycle time t_{POLL} controls the sampling frequency of each input and can be programmed through the CONFIG register.

Issuing a SPI READ command to the INT_STAT register clears its contents and releases the INT_B pin.

Note that after the TRIGGER bit in the CONFIG register is set to logic 1, an interrupt is guaranteed at the completion of the first detection cycle. In all following cycles, interrupts are only produced when a switch state transition is captured.

Channels programmed to 0mA have the wetting current disabled. A bias current specified as $I_{\text{IN_LEAK_0mA}}$ can still flow in either direction on the input pin. The chip continues threshold crossing monitoring for these inputs with available threshold settings. The 0mA mode enables the on-chip ADC or comparator to sample the input voltage without distortion introduced by wetting current.

Polling Mode

Users can enable the provided polling mode to reduce current draw when ignition is off and retain battery energy. Differing from continuous mode, polling mode does not keep current sources or sinks permanently turned on. These circuits are switched on and off sequentially from SP0 to SG13, cycling through each input channel one by one. The MCU can remain in sleep state to minimize total system power. When the SGMCD1024xQ identifies an SSC event for a channel with interrupt enabled, the INT_B pin goes low, and SSC bit in the INT_STAT register plus the SPI SSC flag are latched to logic 1. This INT_B signal can wake the system regulator, which further wakes the MCU as explained in the Microcontroller Wake-Up section. The MCU can then read switch status over the SPI bus.

Setting TRIGGER bit in the CONFIG register to logic 1 activates polling function. The SGMCD1024xQ provides two selectable polling types: standard polling and matrix polling.

Standard Polling

When operating in standard polling mode, the duration for which wetting current is applied to each input is defined by POLL_ACT_TIME bits in the CONFIG register and can be programmed from 64 μ s to 2048 μ s. Once this active period ends, the device samples the input voltage using the comparator or ADC, depending on the selected input mode. Channels are polled sequentially in the order from SP0 to SG13 (if enabled). The overall sampling refresh period ranges from 2ms to 4096ms and is configured by the POLL_TIME bits of the CONFIG register. Since wetting current is activated for closed switches solely during the polling active window, the overall system power consumption can be significantly lowered.

The behavior matches continuous mode in the following aspects. After the initial polling cycle finishes, each input threshold comparison result is stored in IN_STAT_COMP register (for comparator inputs) and IN_STAT_ADC0 ~ IN_STAT_ADC1 registers (for ADC inputs) as the reference state for future cycles. Raw ADC measurement values populate registers ANA_STAT0 through ANA_STAT11. INT_B is pulled low to alert the MCU that baseline switch status can be retrieved, and SSC bit in the INT_STAT register along with the SPI SSC flag are set to logic 1. Reading INT_STAT via SPI clears this register data and releases INT_B to logic high.

Note that setting TRIGGER bit in the CONFIG register to logic 1 guarantees an interrupt at the end of the first polling cycle. All subsequent cycles produce an interrupt only upon detection of switch state transition.

Figure 18 provides a timing diagram example illustrating operation in polling mode.

When the switch position changes in the interval separating two polling active windows, the device will not generate an interrupt, and the status registers IN_STAT_COMP (for comparator channels) and IN_STAT_ADC0 ~ IN_STAT_ADC1 (for ADC channels) cannot reflect this state change. Refer to Figure 19 for an illustrative example.

24-Channel Multiple Switch Detection Interface with SGMCD1024xQ Adjustable Wetting Current for Automotive Applications

DETAILED DESCRIPTION (continued)

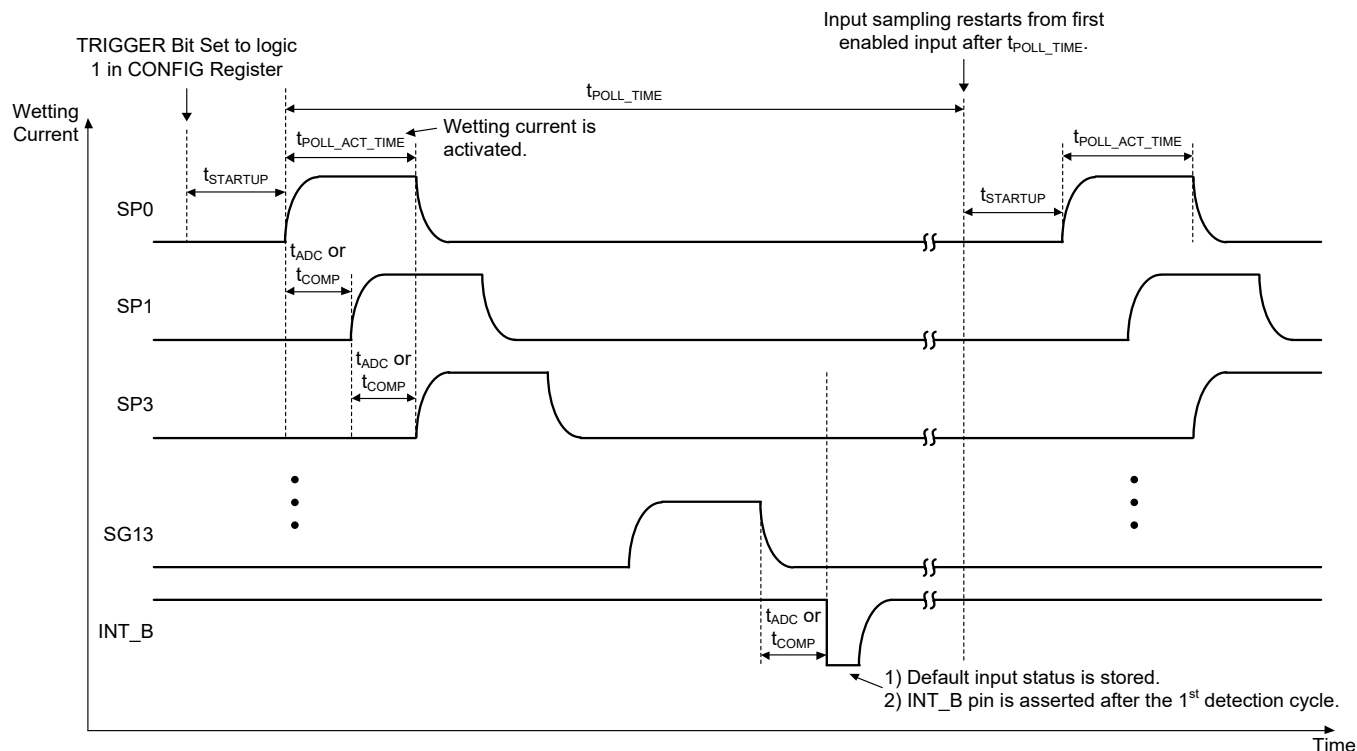


Figure 18. An Example of the Polling Sequence in Standard Polling Mode

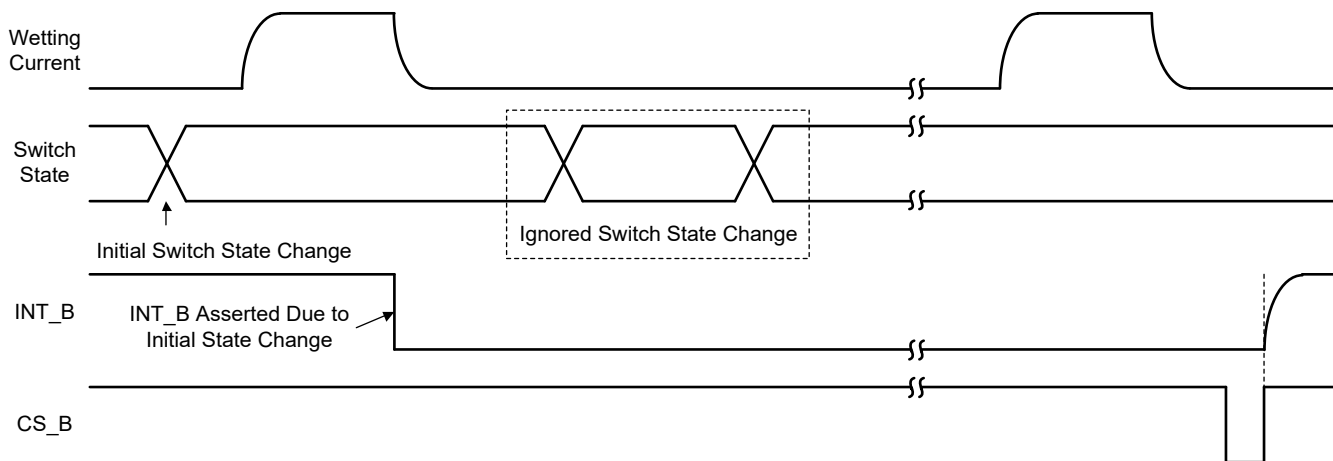


Figure 19. Example for Ignored Switch Position Change between 2 Wetting Current Cycles

24-Channel Multiple Switch Detection Interface with SGMCD1024xQ Adjustable Wetting Current for Automotive Applications

DETAILED DESCRIPTION (continued)

Matrix Polling

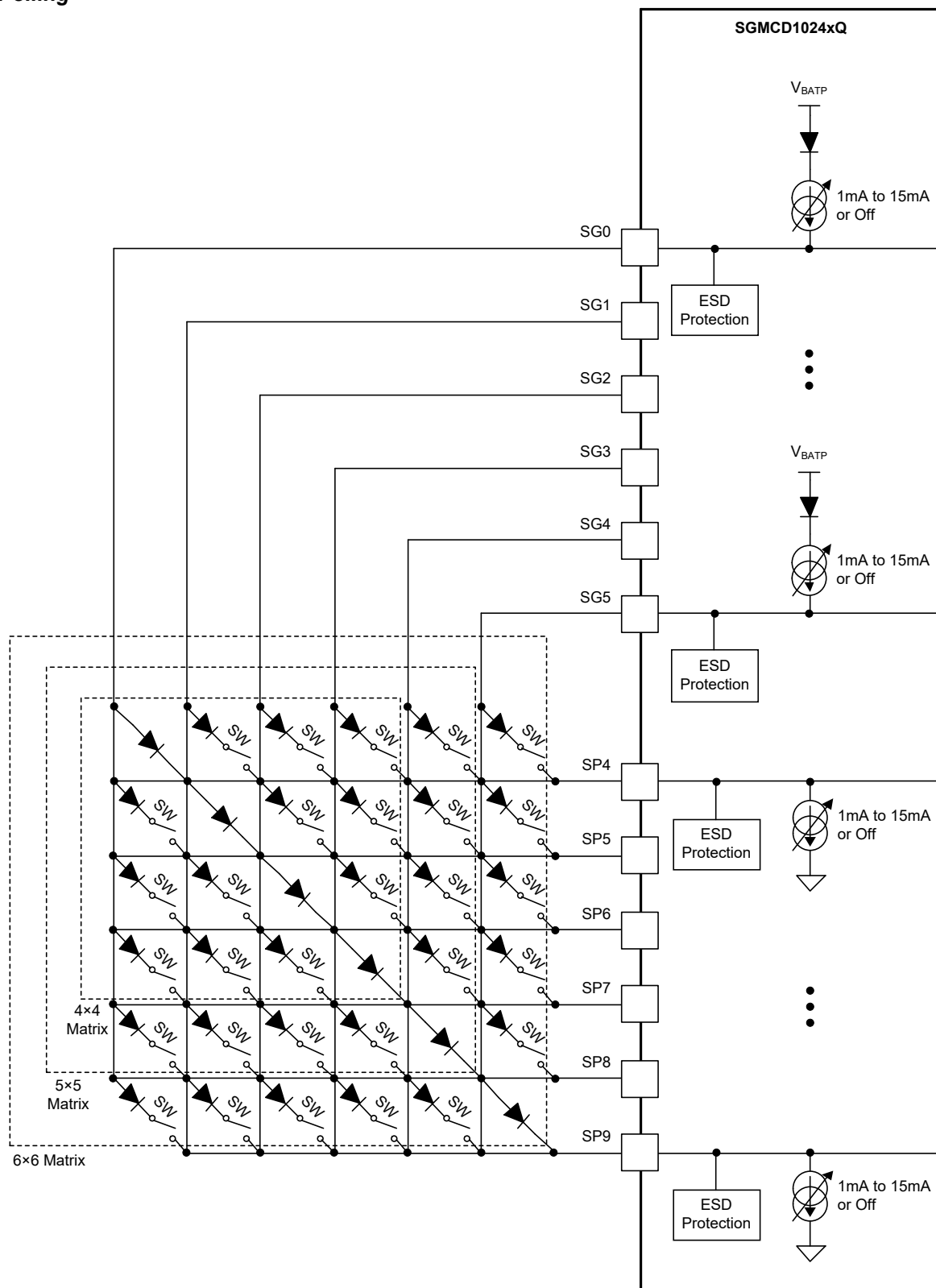


Figure 20. SGMCD1024xQ Matrix Configuration

24-Channel Multiple Switch Detection Interface with SGMCD1024xQ Adjustable Wetting Current for Automotive Applications

DETAILED DESCRIPTION (continued)

Channels SP4 through SG5 support an optional special input switch matrix (shown in Figure 20). It can work together with standard SG or SB switch connections for signal monitoring. This capability implements Matrix Inputs, a special switch input scheme demanded by some OEM customers.

Three matrix modes can be selected through the MATRIX bits of the MATRIX register. If MATRIX bits = 00, all inputs are standard inputs, and their polling active time follows POLL_ACT_TIME bits in the CONFIG register. For all other MATRIX bit values, matrix inputs adopt the polling active time from the POLL_ACT_TIME_M bit from the MATRIX register, while non-matrix channels still use the POLL_ACT_TIME bits. Users must set $t_{\text{POLL_ACT_TIME_M}}$ to a suitable value, so that current sources and sinks have enough time to charge or discharge any capacitors connected to the switch inputs.

Once matrix input configuration is activated, the SGMCD1024xQ adopts an alternate polling workflow. When CONFIG.TRIGGER is set to logic 1 to launch polling, the matrix input group is scanned first, followed by the remaining standard input channels.

After matrix input scanning completes, the threshold comparison result for every input combination is saved to the IN_STAT_MATRIX0 and IN_STAT_MATRIX1 registers. This stored status acts as the reference baseline for future matrix polling cycles. Standard inputs retain the polling characteristics explained in the Standard Polling section.

Once all matrix and standard channels finish their polling sequence, INT_B is pulled low to alert the MCU that baseline switch status can be retrieved. INT_STAT, SSC and the SPI SSC flag are latched to logic 1.

Reading INT_STAT through SPI transaction clears this register and releases INT_B.

Note that after CONFIG.TRIGGER is set to logic 1, an interrupt will always occur at the end of the first complete polling cycle. For all later cycles, interrupt events are only produced when a switch state transition is identified.

Observe the following programming rules when enabling matrix polling.

- Each matrix input for CSO/CSI configuration must be set correctly following Table 7; improper configuration will cause wrong switch state detection.

Table 7. SGMCD1024xQ Matrix Configuration Settings

Input	4 × 4 Matrix		5 × 5 Matrix		6 × 6 Matrix	
	Current Source or Sink	Polling Active Time Setting	Current Source or Sink	Polling Active Time Setting	Current Source or Sink	Polling Active Time Setting
SP4	CSI	POLL_ACT_TIME_M	CSI	POLL_ACT_TIME_M	CSI	POLL_ACT_TIME_M
SP5	CSI		CSI		CSI	
SP6	CSI		CSI		CSI	
SP7	CSI		CSI		CSI	
SP8	Configurable to CSO or CSI	POLL_ACT_TIME	CSI	POLL_ACT_TIME	CSI	
SP9	Configurable to CSO or CSI		Configurable to CSO or CSI		CSI	
SG0	CSO	POLL_ACT_TIME_M	CSO	POLL_ACT_TIME_M	CSO	
SG1	CSO		CSO		CSO	
SG2	CSO		CSO		CSO	
SG3	CSO		CSO		CSO	
SG4	CSO	POLL_ACT_TIME	CSO	POLL_ACT_TIME	CSO	
SG5	CSO		CSO		CSO	

24-Channel Multiple Switch Detection Interface with SGMCD1024xQ Adjustable Wetting Current for Automotive Applications

DETAILED DESCRIPTION (continued)

- CSI channels (SP4 ~ SP9) need a larger wetting current setting than CSO channels (SG0 ~ SG5). The real current passing through external switches is limited to the lower value set by the corresponding CSO channel. Equal current settings on sources and sinks can produce faulty detection outcomes. Therefore, current sources cannot use the 15mA option, and current sinks cannot use the 1mA option. Depending on the matrix switch hardware, particular wetting current values may be necessary for the SGMCD1024xQ to tell open and closed switches apart.
- If TW_CUR_DIS_CSO or TW_CUR_DIS_CSI bit in the CONFIG register equals logic 0, any 10mA or 15mA wetting current will drop to 2mA for SGMCD1024DQ, while any 5mA wetting current will drop to 2mA for SGMCD1024AQ once a TW condition occurs. As matrix polling enforces higher sink current than source current, Table 8 summarizes the valid available configurations for systems expecting TW events.

Table 8. Possible Wetting Current Settings for the Matrix Polling Mode if TW_CUR_DIS = 0 and TW Event is Expected

CSO (SG0-SG5)	CSI (SP4-SP9)	Resulting Wetting Current
1mA	2mA, 5mA, 10mA and 15mA	1mA
2mA	5mA	2mA

When higher wetting current is required and TW events are possible, users must disable the wetting current reduction under TW conditions by programming the TW_CUR_DIS_CSO or TW_CUR_DIS_CSI bit in the CONFIG register.

- Matrix polling operates exclusively with comparator input mode. In other words, the matrix inputs must not be set to ADC mode.
- Since the sink side is tied to ground, threshold comparison is implemented on the source side (SG0 ~ SG5). The interrupt criteria for SG0 through SG5 can be programmed in the INT_EN_COMP1 and INT_EN_COMP2 registers.
- Enabling matrix polling removes certain configuration options, listed as follows:
- For simplified polling logic, individual matrix inputs cannot be disabled. Only three matrix sizes are permitted: 4 × 4, 5 × 5 and 6 × 6. Standard inputs outside the matrix group can still be disabled if needed.
- The detection filter controlled by CONFIG.DET_FILTER works for non-matrix standard inputs only and has no effect on matrix channels.
- If matrix polling is activated, continuous mode is unavailable for any standard inputs outside the matrix group.

24-Channel Multiple Switch Detection Interface with SGMCD1024xQ Adjustable Wetting Current for Automotive Applications

DETAILED DESCRIPTION (continued)

Figure 21 depicts a polling sequence example under the 6 × 6 matrix input configuration.

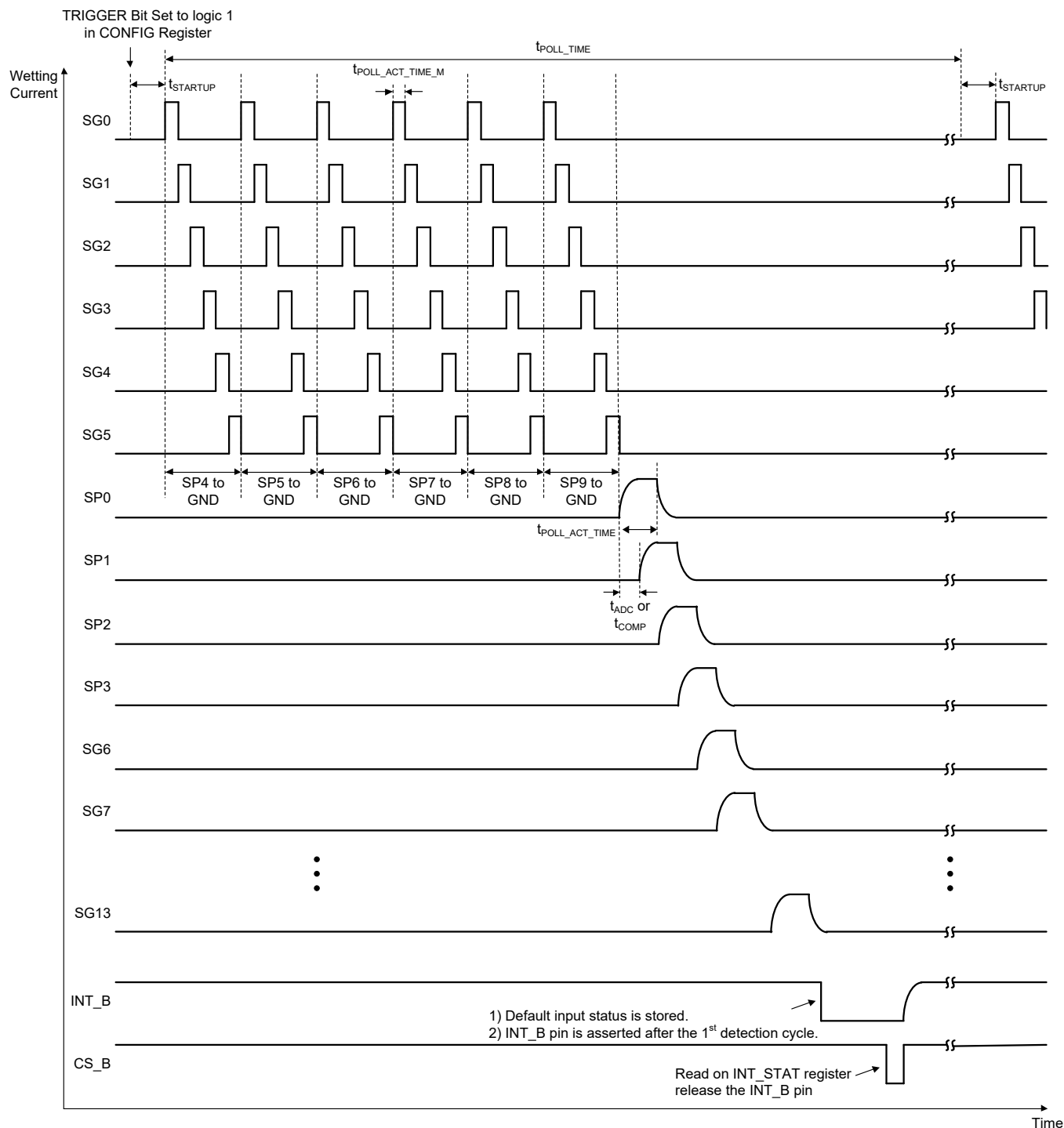


Figure 21. Polling Scheme for 6×6 Matrix Inputs

24-Channel Multiple Switch Detection Interface with SGMCD1024xQ Adjustable Wetting Current for Automotive Applications

DETAILED DESCRIPTION (continued)

Figure 22 depicts a polling sequence example under the 5×5 matrix input configuration. It should be noted that SP9 and SG5 are part of the standard polling sequence.

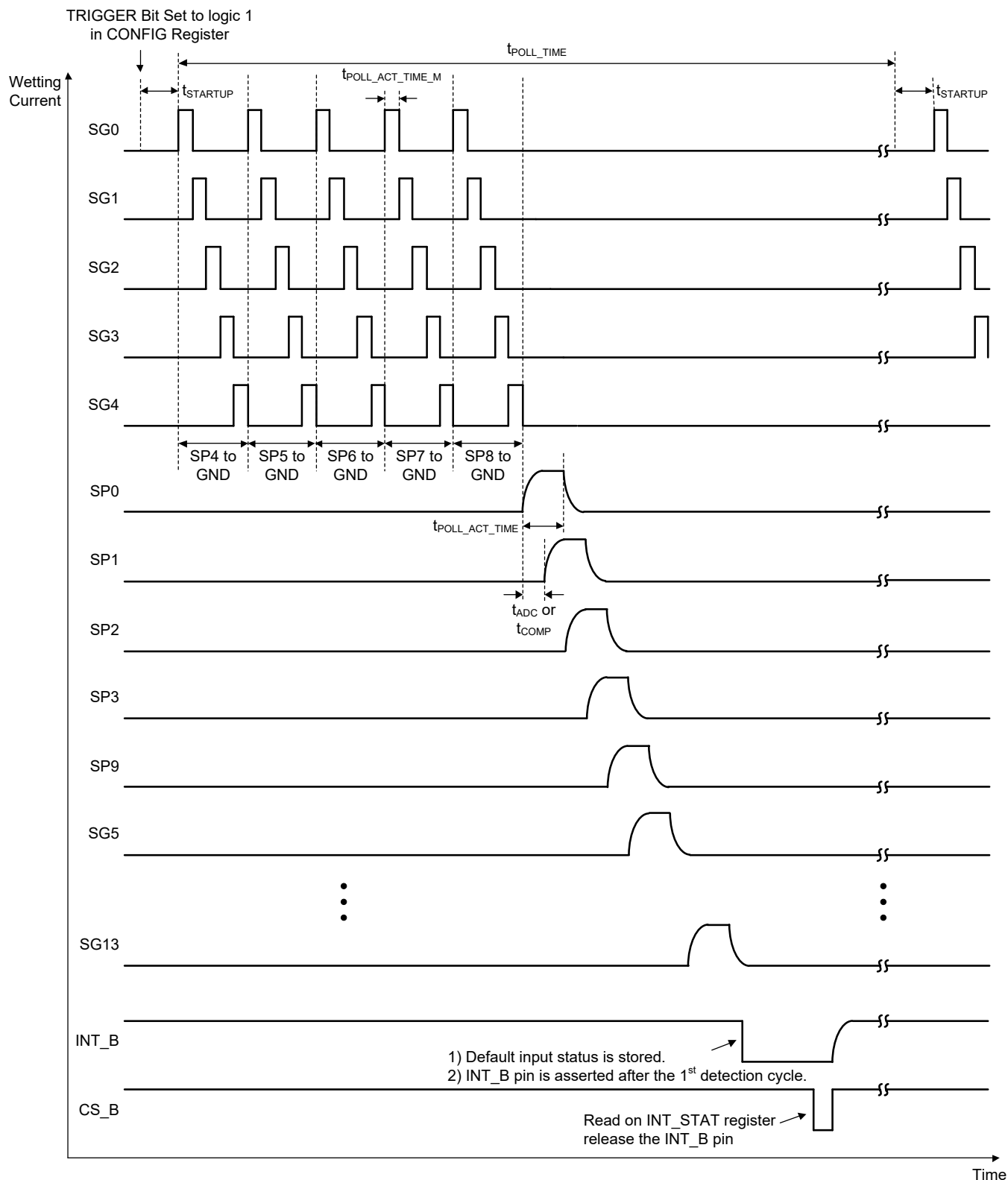


Figure 22. Polling Scheme for 5×5 Matrix Inputs

24-Channel Multiple Switch Detection Interface with SGMCD1024xQ Adjustable Wetting Current for Automotive Applications

DETAILED DESCRIPTION (continued)

Figure 23 depicts a polling sequence example under the 4×4 matrix input configuration. It should be noted that SP8, SP9, SG4 and SG5 are part of the standard polling sequence.

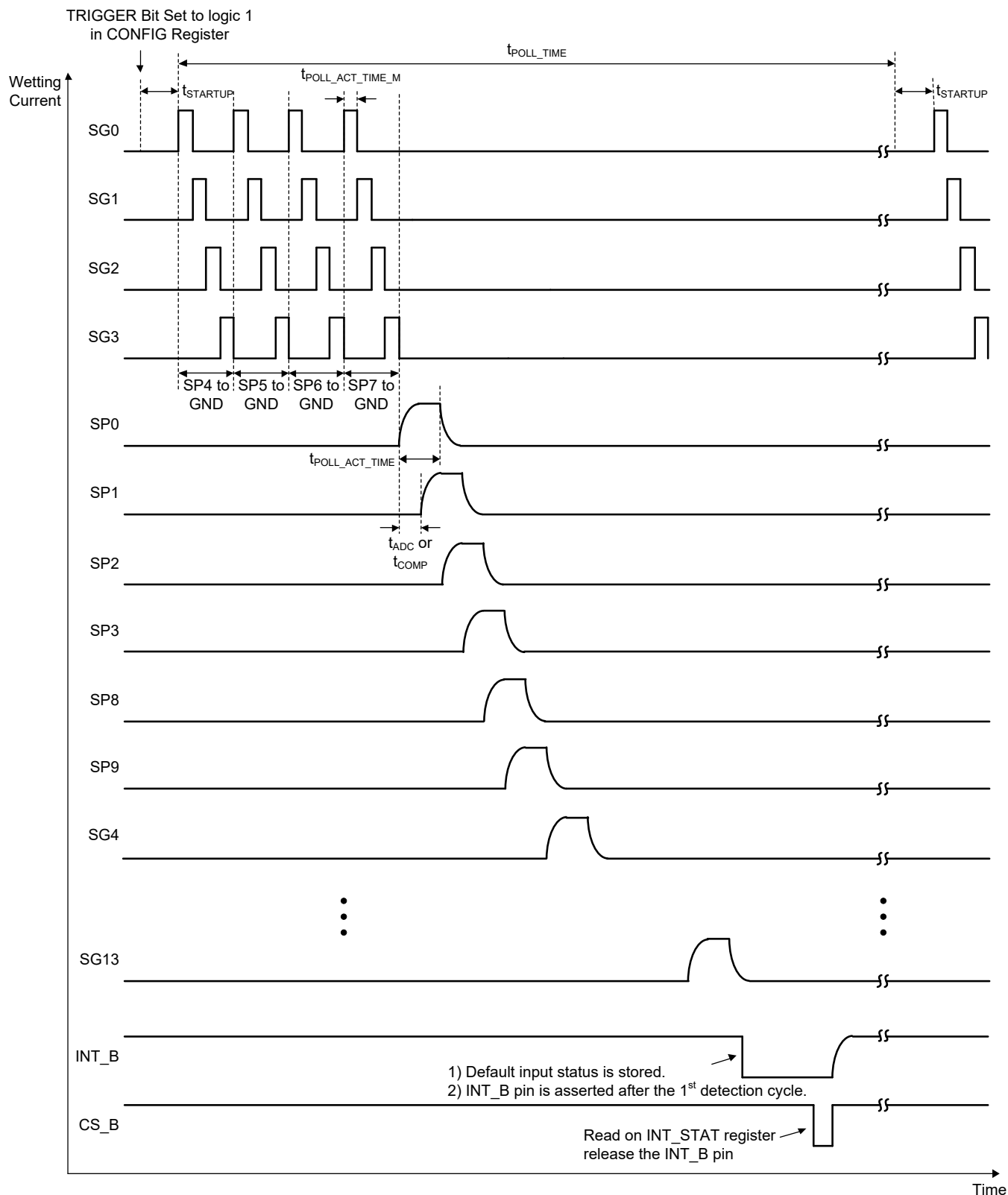


Figure 23. Polling Scheme for 4x4 Matrix Inputs

24-Channel Multiple Switch Detection Interface with SGMCD1024xQ Adjustable Wetting Current for Automotive Applications

DETAILED DESCRIPTION (continued)

Additional Features

A set of supplementary features can be turned on to improve the reliability of device operation and deliver more system status information. Detailed descriptions of these functions are presented in the following paragraphs.

Clean Current Polling (CCP)

Users may select smaller wetting current values to detect resistor-coded switches or cut down total current consumption. Certain systems, however, need 10mA or larger cleaning current to burn off oxide deposits on mechanical switch contacts once the switches close and current passes through them. Clean Current Polling (CCP) is a special polling function intended for this requirement.

With CCP turned on, each polling cycle has two wetting current stages. The first stage uses wetting currents configured by the WC_CFG0 and WC_CFG1 registers, identical to continuous or standard polling operation. The second cleaning stage triggers on all CCP-enabled

inputs at the same time, starting t_{CCP_TRAN} after the end of normal polling for the last active input. These clean current pulses have no influence on interrupt triggering or INT_B behavior.

The CCP_CFG0 register sets the CCP wetting current and its active time. Users can disable the cleaning cycle separately for each input channel through configuration of the CCP_CFG1 register. The CCP function works in both continuous and polling modes. CCP can only be used when at least one standard or matrix input is enabled or the VBATP Measurement feature is enabled.

Note: Even though CCP may be enabled alongside matrix polling, it cannot efficiently clean matrix switch contacts because the CSO output current will be divided among several matrix channels.

Figure 24 shows CCP behavior for the device configured in standard polling mode. And Figure 25 shows CCP behavior for the device configured in continuous mode.

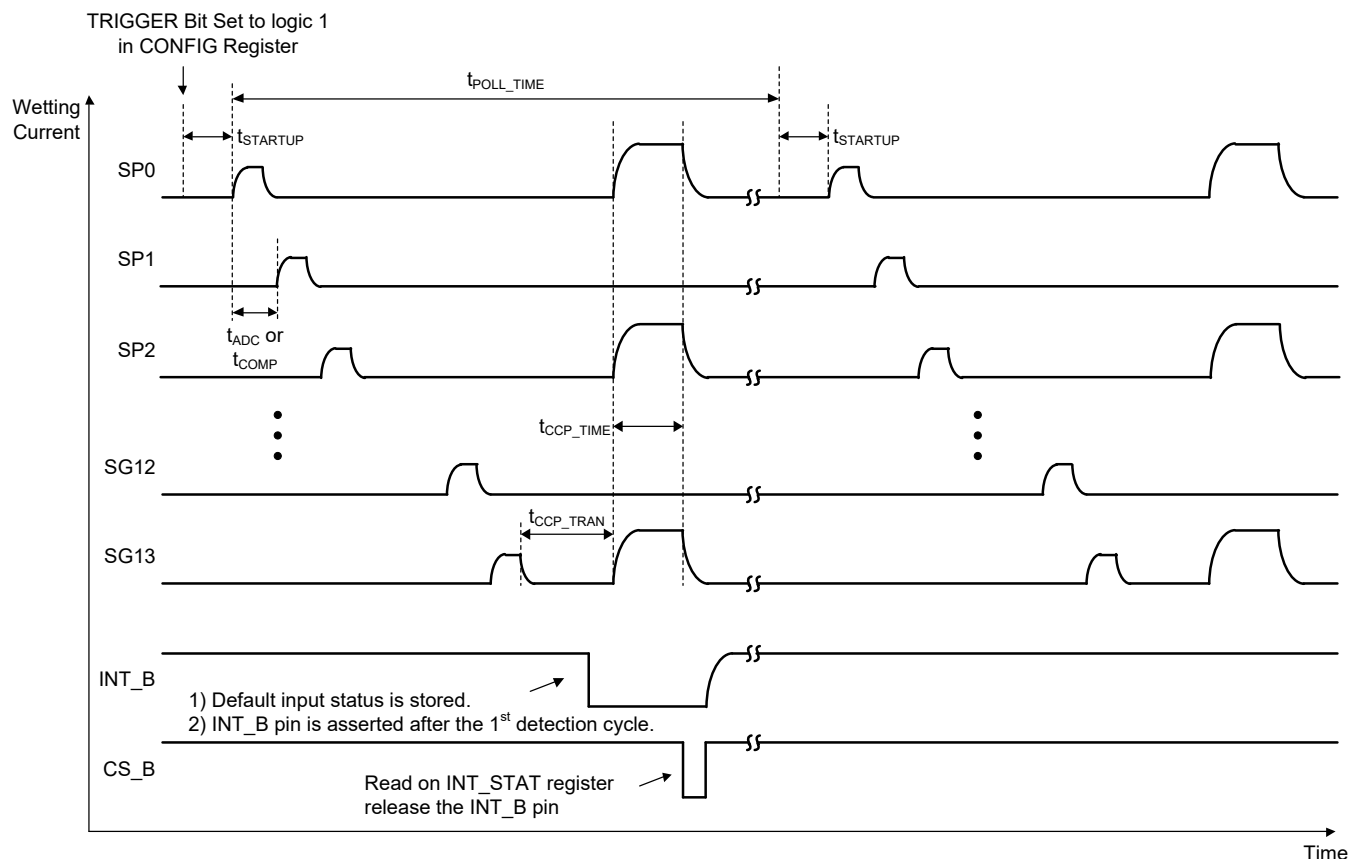


Figure 24. Standard Polling with CCP Enabled

24-Channel Multiple Switch Detection Interface with SGMCD1024xQ Adjustable Wetting Current for Automotive Applications

DETAILED DESCRIPTION (continued)

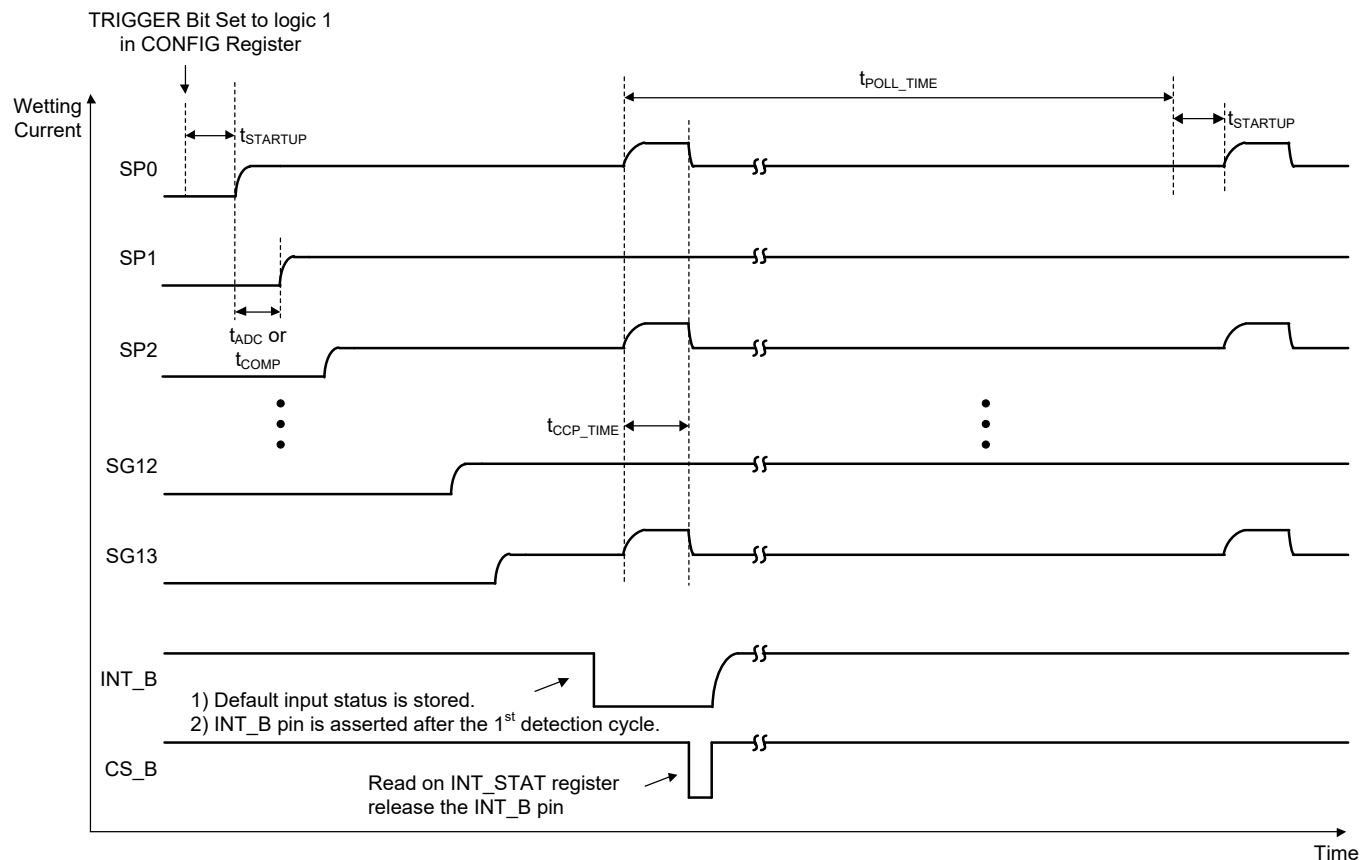


Figure 25. Continue Mode with CCP Enabled

Wetting Current Auto-Scaling

The 10mA and 15mA wetting current options can clear oxide deposits on mechanical switch contacts when a switch closes from an open state. After the switch has closed, keeping high wetting current is not preferred for pure digital switch monitoring. It increases power draw and may rapidly heat the chip if many inputs are active. Thanks to the wetting current auto-scaling capability of SGMCD1024xQ, it is easy to address this problem.

If the AUTO_SCALE_DIS_CSO or AUTO_SCALE_DIS_CSI bit in the WC_CFG1 register is logic 0, the wetting current will drop from 10mA/15mA down to 2mA once switch closure is identified. Comparator mode inputs use the threshold programmed in the THRES_COMP register to judge switch closure. For ADC mode inputs, the corresponding threshold for switch detection differs based on channel index; refer to Table 9 for details.

Table 9. Threshold Used to Determine a Switch Closure for Wetting Current Auto-Scaling for ADC Inputs

Input	Threshold Used to Determine a Switch Closure
SP0 to SG1	Mapped threshold from THRES0 to THRES7
SG2 to SG7	THRES2B
SG8 to SG12	THRES3C
SG13	THRES9

Once the device detects a closed switch on an input channel, the current will be lowered after N detection cycles. The value N is controlled by the DET_FILTER bit in the CONFIG register.

- DET_FILTER = 00: reduce wetting current in next detection cycle upon closed switch detection.
- DET_FILTER = 01: reduce after closed status stable for ≥ 2 consecutive detection cycles.
- DET_FILTER = 10: reduce after closed status stable for ≥ 3 consecutive detection cycles.
- DET_FILTER = 11: reduce after closed status stable for ≥ 4 consecutive detection cycles.

24-Channel Multiple Switch Detection Interface with SGMCD1024xQ Adjustable Wetting Current for Automotive Applications

DETAILED DESCRIPTION (continued)

Likewise, the wetting current restores to the original 10mA or 15mA level for SGMCD1024DQ or 5mA level for SGMCD1024AQ N cycles after an open switch is detected, with N still governed by the DET_FILTER setting. Figure 26 shows the operation of wetting current auto-scaling for SGMCD1024DQ.

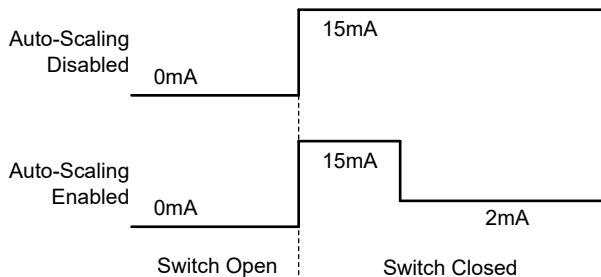


Figure 26. Wetting Current Auto-Scaling Behavior

The wetting current auto-scaling function works only for 10mA and 15mA selections for SGMCD1024DQ or 5mA selections for SGMCD1024AQ and is restricted to continuous mode operation. Setting the AUTO_SCALE_DIS_CSO or AUTO_SCALE_DIS_CSI bit in the WC_CFG1 register to logic 1 keeps the wetting current unchanged even after a closed switch is detected. When auto-scaling is turned off for many input channels, thermal monitoring is essential. High wetting current levels can heat the chip rapidly. With auto-scaling disabled in continuous mode, Equation 1 provides an approximation of total power dissipation.

$$P_{\text{TOTAL}} = V_{\text{BATP}} \times (I_{\text{S_CONT}} + I_{\text{WETT_TOTAL}}) \quad (1)$$

$I_{\text{WETT_TOTAL}}$ is the sum of all wetting currents from all input channels. Junction temperature rise of the device is computed as $P \times R_{\theta\text{JA}}$. The chip will operate correctly only if its junction temperature stays lower than T_{TSD} . Once the junction temperature surpasses T_{TW} or T_{TSD} , an interrupt event is generated. See the Temperature Warning (TW) and Temperature Shutdown (TSD) sections for comprehensive temperature monitoring descriptions.

V_{BATP} Measurement

For resistor-coded switch monitoring applications using the SGMCD1024xQ, VBATP supply voltage is a key parameter. A low V_{BATP} level reduces voltage headroom and prevents the chip from generating accurate wetting currents, which impairs switch state detection accuracy. In this scenario, the MCU needs continual visibility of the VBATP voltage.

The SGMCD1024xQ supports VBATP voltage measurement. This function is activated by programming CONFIG.VBATP_MEAS_EN to logic 1. When enabled, the ADC performs sampling and conversion on the VBATP pin at the conclusion of every polling cycle. The conversion requires an additional t_{ADC} time, and the digital result is saved to the ANA_STAT12 register.

Two VBATP voltage ranges are available for VBATP measurement, and are selected by VBATP_RATIO bit in the CONFIG register. The default setting, VBATP_RATIO = 0 covers 4.5V ~ 9V. Any VBATP voltage higher than 9V will saturate the ADC raw reading at 1023. This mode achieves higher resolution for low VBATP values. Setting VBATP_RATIO = 1 expands the measurement range to 4.5V ~ 30V. V_{BATP} exceeding 30V results in saturated ADC code 1023. This wider range comes with reduced measurement resolution. Users need to modify detection thresholds to match the selected V_{BATP} range.

Four measurement thresholds can be programmed: VS0_THRES2A/B and VS1_THRES2A/B. The threshold magnitudes are set in THRES_CFG0 ~ THRES_CFG3, and threshold mapping is defined by THRESMAP_VS0_THRES2A/B and THRESMAP_VS1_THRES2A/B bits in the THRESMAP_CFG2 register. Refer to Table 10 and comply with its rules when configuring thresholds.

Table 10. Proper Threshold Configuration for V_{BATP} Measurements

V_{BATP} Threshold	Proper Threshold Configuration
VS0	$\text{VS0_THRES2B} \geq \text{VS0_THRES2A}$
VS1	$\text{VS1_THRES2B} \geq \text{VS1_THRES2A}$

When V_{BATP} measurement is enabled for the first time, an interrupt will automatically fire after completion of the first polling cycle. INT_B pulls low and the VS0/VS1 bit in the INT_STAT register is latched high, informing the MCU that the first V_{BATP} reading can be fetched. The VS0_STAT and VS1_STAT bits in the IN_STAT_MISC register show whether V_{BATP} is above or below the configured thresholds. The ANA_STAT12 register contains the ADC conversion result of V_{BATP} , and the SPI VS_TH flag is set to logic 1 for SPI communication. Note that the measured status from the first polling cycle acts as the reference baseline for all later V_{BATP} measurements. Subsequent interrupts are only issued if the voltage crosses a threshold.

24-Channel Multiple Switch Detection Interface with SGMCD1024xQ Adjustable Wetting Current for Automotive Applications

DETAILED DESCRIPTION (continued)

Same as regular inputs, interrupt conditions are configured by INT_EN_CFG4.VS_TH0_EN and VS_TH1_EN bits.

Users can turn off interrupt generation by programming INT_EN_CFG4.VS_TH0_EN or VS_TH1_EN to logic 0. When disabled, V_{BATP} threshold crossings will not set the VS0/VS1 flag in the INT_STAT register and will not pull INT_B low. If only INT_B assertion needs to be suppressed while the INT_STAT register continues to be updated, configure INT_EN_CFG0.VS0_EN and VS1_EN to logic 0.

Note that V_{BATP} measurement is meant to work together with switch detection to verify the switch states output by SGMCD1024xQ. It is not suitable for independent supply monitoring applications such as cranking voltage capture, since the response delay is determined by the polling cycle. The V_{BATP} reading is accurate when $V_{BATP} > 4.5V$.

V_{BATP} measurement is disabled at device reset by default.

Wetting Current Diagnostic

For safety-critical applications about switch monitoring with SGMCD1024xQ, the MCU can monitor the health of wetting current sources and sinks using the built-in wetting current diagnostic function, which applies to

SP0 ~ SP3. SP0 and SP1 are used to test wetting current sources for faults, while SP2 and SP3 are dedicated to current sink diagnostics.

Enable this function by setting the WET_D_SPx_EN bit of the CONFIG register to logic 1 for the target input channels ($x = 0, 1, 2, 3$). After activation, the chip periodically checks the wetting current sources and sinks of selected inputs during polling. If a wetting current malfunction is detected, INT_B is pulled low, INT_STAT.WET_DIAG is set to logic 1, and the SPI OI flag is asserted during SPI communication. The MCU can check IN_STAT_MISC.SP0_D ~ SP3_D bits to locate which wetting current source or sink has failed.

If an input is disabled from polling via IN_EN.IN_EN_x = 0, wetting current diagnostics will be skipped for that channel, even when the diagnostic feature is turned on. To avoid false interrupt events, users must configure current source/sink settings correctly (CSO for SP0/SP1, CSI for SP2/SP3) and set the corresponding inputs to ADC input mode before enabling wetting current diagnostics. This diagnostic runs irrespective of external switch status and works under both continuous and polling modes.

Figure 27 depicts the diagnostic operation inside a standard polling sequence.

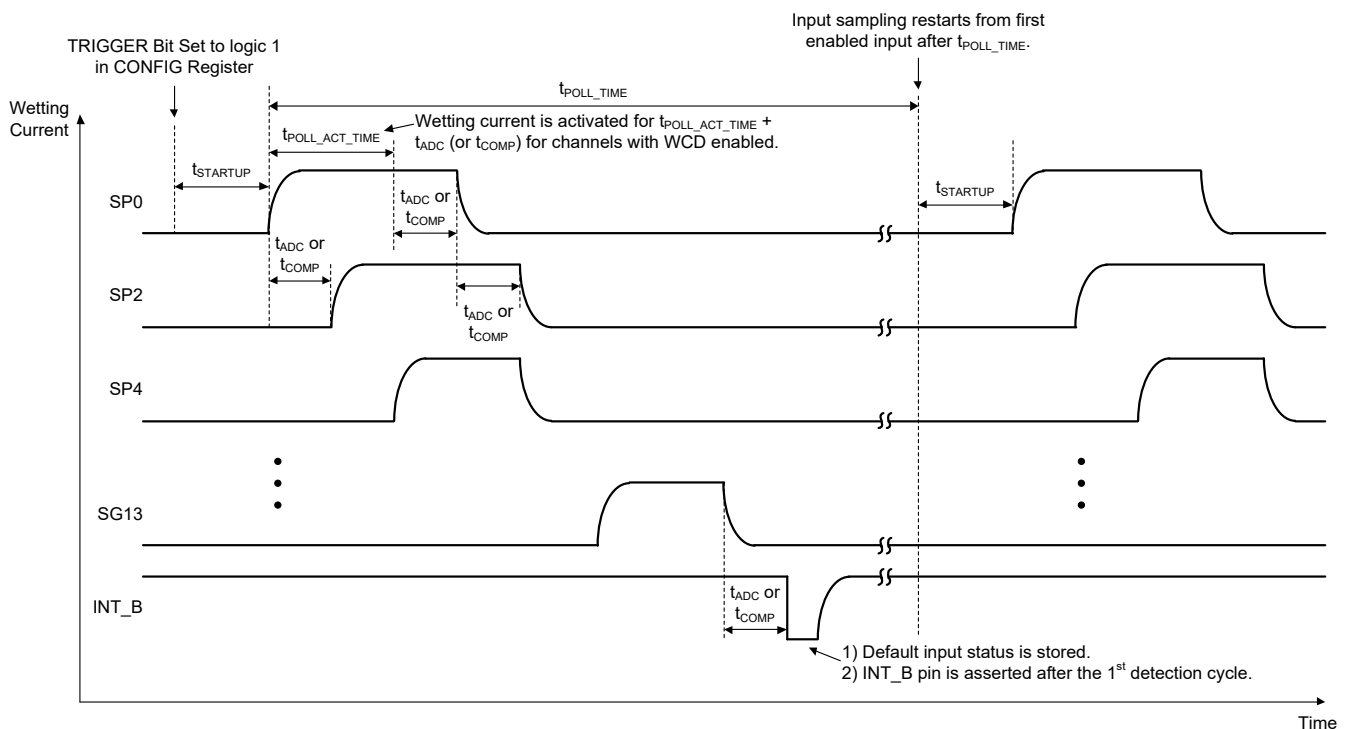


Figure 27. An Example of the Polling Sequence in Standard Polling Mode with Wetting Current Diagnostic Enabled

24-Channel Multiple Switch Detection Interface with SGMCD1024xQ Adjustable Wetting Current for Automotive Applications

DETAILED DESCRIPTION (continued)

In this example, each diagnosed input (SP0 or SP2) has wetting current enabled for $t_{\text{POLL_ACT}} + t_{\text{ADC}}$. Normal polling continues from SP4 onward, with wetting current active for $t_{\text{POLL_ACT}}$ on all subsequent inputs. SP1 and SP3 are disabled in this example and therefore do not undergo diagnostic checks.

ADC Self-Diagnostic

Apart from wetting current diagnostics, the ADC self-diagnostic feature can be turned on to check the internal ADC health. Enable ADC self-diagnostic by programming CONFIG.ADC_DIAG_T to logic 1. Once enabled, the SGMCD1024xQ periodically feeds a test voltage to the ADC. The conversion result is held in ANA_STAT12.ADC_SELF_ANA bits and compared with a predefined code to judge whether the ADC conversion works correctly. When an error is found, INT_B is pulled low, INT_STAT.ADC_DIAG is set to logic 1, and IN_STAT_MISC.ADC_D reflects the self-test result. This ADC self-diagnostic works in both continuous mode and polling mode.

SPI Communication Interface Buses

The SPI interface has four pins, namely CS_B, SCLK, MOSI and MISO. The maximum supported SCLK frequency for the SGMCD1024xQ SPI interface is 4MHz.

Chip Select (CS_B)

The MCU selects the SGMCD1024xQ as a slave unit for communication via the CS_B pin. When CS_B is held at logic low, command words can be transmitted to the SGMCD1024xQ through the MOSI pin, while device status information can be read by the MCU from the MISO pin. The falling edge of CS_B enables the MISO output and latches the data of the INT_STAT interrupt register. The MCU can execute READ commands to access register-stored information.

A rising edge on the CS_B pin triggers the following operations.

- Disables the output driver and sets the MISO pin to a high-impedance state.
- Resets the INT_B pin to logic high if a READ command targeting the INT_STAT register is executed while CS_B is low.

To prevent data corruption, all high-to-low and low-to-high transitions of the CS_B signal must occur

while SCLK is at logic low. A clean CS_B signal is required to avoid transmitting incomplete SPI words to the device. The CS_B pin shall be externally pulled up to VDDQ through a 10kΩ resistor.

System Clock (SCLK)

The SCLK, system clock input, drives the internal shift register of SGMCD1024xQ. MOSI data gets captured into the input shift register at SCLK falling edge. The chip outputs internal information via MISO at the SCLK rising edge, and the MISO data can be sampled by the MCU at SCLK falling edge.

To avoid invalid data caused by false shift register clocking, SCLK must be logic low whenever CS_B transitions. It is suggested to hold SCLK low when there is no device access and CS_B is high. When CS_B = logic high, SCLK and MOSI inputs are disregarded, and MISO stays high-impedance. See Figure 28 and Figure 29 for typical SPI read/write timing diagrams.

Master Output Slave Input (MOSI)

The MOSI pin receives serial command data. The input register captures MOSI data at the falling edge of SCLK. Programming a full word requires sending 32 bits to the SGMCD1024xQ. The SPI hardware counts incoming bits and latches data only after receiving exactly 32 bits. When the bit count does not match the 32-bit requirement, INT_STAT.SPI_FAIL becomes logic 1, INT_B pulls low, and the received data is discarded as invalid. If there is no SCLK clock signal, the SPI_FAIL flag will not be triggered.

Master Input Slave Output (MISO)

MISO outputs data from the internal shift register. MISO stays high-impedance before CS_B falls to logic low. The CS_B falling edge turns on the MISO output driver, which defaults to logic high. On the first SCLK rising edge, status bit 31 appears on MISO. Every subsequent rising SCLK edge sends out the next data bit, and the MCU reads this bit at the SCLK falling edge. MOSI and MISO use FIFO data shifting, and all input and output words are transmitted MSB first.

SPI Sequence

Figure 28 and Figure 29 depict the SPI communication sequence during read and write operations for the SGMCD1024xQ.

24-Channel Multiple Switch Detection Interface with SGMCD1024xQ Adjustable Wetting Current for Automotive Applications

DETAILED DESCRIPTION (continued)

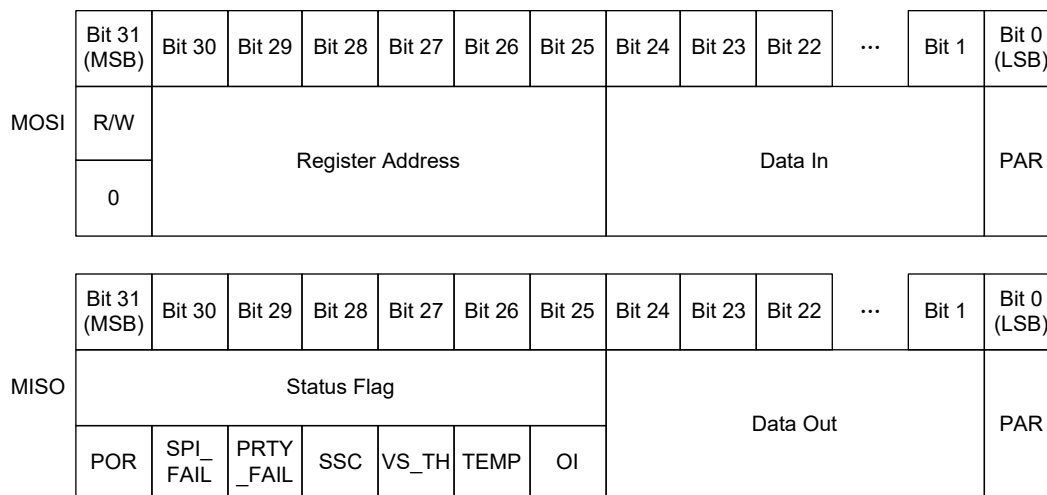


Figure 28. SGMCD1024xQ Read SPI Sequence

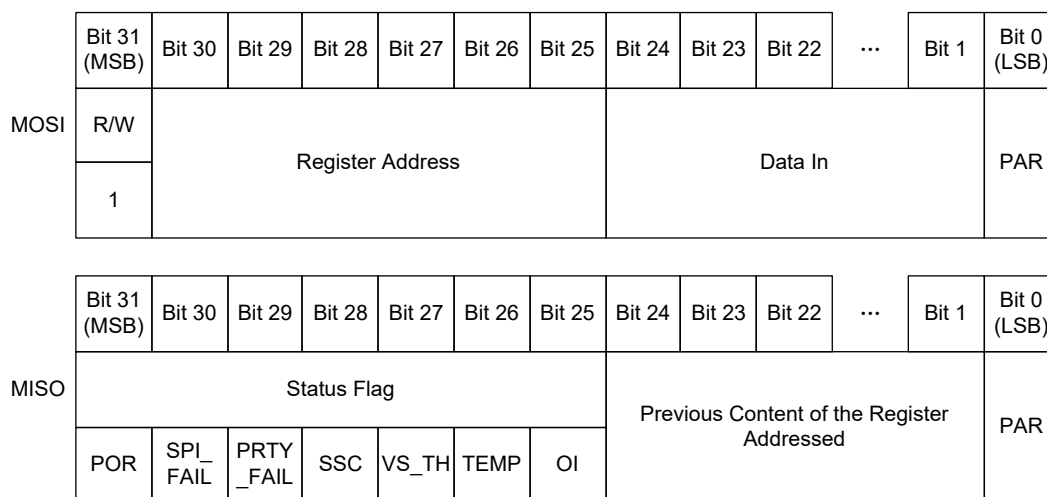


Figure 29. SGMCD1024xQ Write SPI Sequence

Read Operation

For READ operations, the Read/Write bit (bit 31) on MOSI must be logic 0. The 6-bit target register address is then sent over MOSI. Bits 24 to bit 1 carry no valid read command information and will be disregarded. The LSB (bit 0) is a parity bit for checking communication faults.

The SGMCD1024xQ sends status flags out via MISO, then transmits the data of the requested register. Its LSB is also the parity bit used to detect communication errors.

When a READ command accesses an invalid register address, the SGMCD1024xQ outputs all 0s.

Write Operation

For write operations, set the Read/Write bit (bit 31) on MOSI to logic 1. The subsequent 6 bits on MOSI define the address of the register to be programmed. Note that only writable configuration registers accept this command and commands targeting non-writable registers will be discarded. Bits 24 to bit 1 contain the data intended for register programming, and the LSB (bit 0) acts as a parity bit to check communication errors.

Via MISO, the SGMCD1024xQ outputs status flags and then the pre-existing data of the written register. This original register value gets latched after the full address in the MOSI command is decoded upon transmission of bit 25.

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DETAILED DESCRIPTION (continued)

If the MOSI write command is valid with a correct address and no SPI or parity errors, the register will be updated to the new data at the end of SPI transfer flow. Invalid write commands will ignore the incoming data, leaving the register value untouched. The LSB on MISO is used as a parity bit for communication error detection.

When a WRITE command addresses an invalid register location, MISO outputs all-zero bits.

Status Flag

MISO outputs status flags in every SPI READ or WRITE transaction to reflect system operating conditions. These flags are not stored in a standalone physical register, but copied from the INT_STAT register. When the MCU sends a READ command targeting INT_STAT register, both the bits inside INT_STAT register and these mirrored status flags will be cleared. The following table lists the meaning of each SPI status flag.

Table 11. SPI Status Flag Description

SYMBOL	NAME	DESCRIPTION
POR	Power-on Reset	This flag copies the POR bit from the INT_STAT register. A value of logic 1 signals that a reset event has taken place. This bit is set after completion of power-on reset, hardware reset or software reset.
SPI_FAIL	SPI Error	This flag reflects the SPI_FAIL bit inside INT_STAT register. A logic 1 value means the last MOSI SPI transfer received by the chip is invalid. Programming a full word requires sending 32 bits to the device. The SPI hardware counts incoming bits and latches data only after receiving exactly 32 bits. When the bit count does not match the required length, the SPI_FAIL bit in the INT_STAT register is set to logic 1; this mirrored SPI_FAIL status flag is updated accordingly, INT_B is pulled low, and the received data is marked invalid. Once the MCU reads the INT_STAT register, the register content is cleared at the CS_B rising edge, and the SPI_FAIL status flag (copied from INT_STAT register) is also cleared. If there is no SCLK clock signal, the SPI_FAIL flag will not be triggered.
PRTY_FAIL	Parity Fail	This flag copies the PRTY_FAIL bit from INT_STAT register. A logic 1 means the latest MOSI SPI transfer has a parity fault. The chip uses odd parity checking. If the sum of 1s in the received data (including parity bit) is even, the incoming data will be rejected. INT_B is pulled low, the PRTY_FAIL bit in INT_STAT register becomes logic 1, and the mirrored PRTY_FAIL status flag is also set high. When the MCU reads INT_STAT register, the register content clears at the CS_B rising edge, and the mirrored PRTY_FAIL status flag is cleared simultaneously.
SSC	Switch State Change	This flag reflects the SSC bit inside INT_STAT register. Logic 1 means at least one switch input has crossed its threshold. The MCU can check IN_STAT_COMP (comparator mode), IN_STAT_ADC0 ~ IN_STAT_ADC1 (ADC mode), or IN_STAT_MATRIX0 ~ IN_STAT_MATRIX1 (matrix mode) to locate which input triggered the state change. Once INT_STAT register is read, the register data is cleared at the rising edge of CS_B, and the mirrored SSC status flag from the INT_STAT register is also cleared.
VS_TH	VS Threshold Crossing	This flag becomes logic 1 if INT_STAT.VS0 or INT_STAT.VS1 equals logic 1. It signals that the VBATP voltage has crossed at least one threshold set by VS0_THRES2A, VS0_THRES2B, VS1_THRES2A, or VS1_THRES2B. The MCU can check IN_STAT_MISC.VS0_STAT and IN_STAT_MISC.VS1_STAT bits to locate which threshold triggered the event. Once the INT_STAT register is read, the register data is cleared at the CS_B rising edge, and the VS_TH status flag is also cleared.
TEMP	Temperature Event	This flag goes to logic 1 when INT_STAT.TW or INT_STAT.TSD is logic 1, signalling a TW or TSD event. The flag is also asserted when a TW or TSD event terminates. To distinguish which event happened, the SPI controller can read the INT_STAT register, and may also check the IN_STAT_MISC register for the chip temperature status. When the INT_STAT register is read, the register contents are cleared at the CS_B rising edge, and the TEMP status flag is cleared as well.
OI	Other Interrupt	Other interrupt sources cover OV, UV, CRC_CALC, WET_DIAG, ADC_DIAG and CHK_FAIL. This flag becomes logic 1 if any of these corresponding bits mentioned above in the INT_STAT register is asserted. The SPI controller can read the INT_STAT register to find out which event or multiple events have occurred, and read the IN_STAT_MISC register for the latest device status. Once the INT_STAT register is read, its contents are cleared at the CS_B rising edge, and the OI status flag is cleared at the same time.

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REGISTER MAPS

Summary Register Map

OFFSET		TYPE	RESET	ACRONYM	REGISTER NAME
SGMCD1024AQ	SGMCD1024DQ				
1h	—	R	25h	DEVICE_ID	Device ID Register
—	1h	R	24h	DEVICE_ID	Device ID Register
2h	2h	RC	1h	INT_STAT	Interrupt Status Register
3h	3h	R	DBACH	CRC	CRC Result Register
4h	4h	R	0h	IN_STAT_MISC	Miscellaneous Status Register
5h	5h	R	0h	IN_STAT_COMP	Comparator Status Register
6h, 7h	—	—	—	RESERVED	RESERVED
—	6h, 7h	R	0h	IN_STAT_ADC0, IN_STAT_ADC1	ADC Status Register
8h, 9h	8h, 9h	R	0h	IN_STAT_MATRIX0, IN_STAT_MATRIX1	Matrix Status Register
—	Ah ~ 16h	R	0h	ANA_STAT0 ~ ANA_STAT12	ADC Raw Code Register
Ah ~ 19h	17h ~ 19h	—	—	RESERVED	RESERVED
1Ah	1Ah	R/W	0h	CONFIG	Device Global Configuration Register
1Bh	1Bh	R/W	0h	IN_EN	Input Enable Register
1Ch	1Ch	R/W	0h	CS_SELECT	Current Source/Sink Selection Register
1Dh, 1Eh	1Dh, 1Eh	R/W	0h	WC_CFG0, WC_CFG1	Wetting Current Configuration Register
1Fh, 20h	1Fh, 20h	R/W	0h	CCP_CFG0, CCP_CFG1	Clean Current Polling Register
21h	21h	R/W	0h	THRES_COMP	Comparator Threshold Control Register
22h, 23h	22h, 23h	R/W	0h	INT_EN_COMP1, INT_EN_COMP2	Comparator Input Interrupt Generation Control Register
24h	24h	R/W	0h	INT_EN_CFG0	Global Interrupt Generation Control Register
25h ~ 30h	—	—	—	RESERVED	RESERVED
—	25h ~ 28h	R/W	0h	INT_EN_CFG1 ~ INT_EN_CFG4	ADC Input Interrupt Generation Control Register
—	29h ~ 2Dh	R/W	0h	THRES_CFG0 ~ THRES_CFG4	ADC Threshold Control Register
—	2Eh ~ 30h	R/W	0h	THRESMAP_CFG0 ~ THRESMAP_CFG2	ADC Threshold Mapping Register
31h	31h	R/W	0h	Matrix	Matrix Setting Register
32h	—	—	—	RESERVED	RESERVED
—	32h	R/W	0h	Mode	Mode Setting Register
33h	33h	RC	0h	SSC_INT	SSC Interrupt Detection Register
34h, 35h	—	RC	0h	MTX_INT0, MTX_INT1	Matrix Interrupt Detection Register

Bit Types:

R/W: Read/Write bit(s)

R: Read only bit(s)

RC: Bit(s) cleared to 0 by being read

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REGISTER MAPS (continued)

Detailed Register Maps

REG1h: DEVICE_ID Register [Reset = 25h for SGMCD1024AQ and 24h for SGMCD1024DQ]

This register represents the device ID of the SGMCD1024xQ.

BITS	BIT NAME	RESET	TYPE	DESCRIPTION
D[23:11]	RESERVED	0h	R	Reserved.
D[10:4]	MAJOR	2h	R	Major revision ID.
D[3:0]	MINOR	5h	R	SGMCD1024AQ minor revision ID.
		4h	R	SGMCD1024DQ minor revision ID.

REG2h: INT_STAT Register [Reset = 1h]

This register presents event-related information upon the occurrence of external events. Issuing a READ command to this register clears its stored data and returns to the factory-default state. The INT_B pin shall be de-asserted on the rising edge of the CS_B signal subsequent to a READ operation.

BITS	BIT NAME	RESET	TYPE	DESCRIPTION
D[23:14]	RESERVED	0h	R	Reserved.
D[13]	CHK_FAIL	0h	RC	0h = Successful loading of the factory-default initialization setting or clearing of the event-status flag occurs after a READ command to this register. 1h = Error detected upon device initialization. This is a self-check function in the power-up procedure. Once the CHK_FAIL bit is 1, please issue a software reset by the host MCU and reload the factory-default settings.
SGMCD1024DQ				
D[12]	ADC_DIAG	0h	RC	0h = Either no error judging from the ADC self-diagnostic routine is identified, or the ADC self-diagnostic status is cleared upon a READ operation on the INT_STAT register. 1h = An ADC error is self-diagnosed.
D[11]	WET_DIAG	0h	RC	0h = Either no error judging from the wetting current self-diagnostic routine is identified, or the wetting current self-diagnostic status is cleared upon a READ operation on the INT_STAT register. 1h = Wetting current error is detected.
D[10]	VS1	0h	RC	0h = Either no VBATP occurs judging from VS1_THRES2A or VS1_THRES2B, or the VBATP SSC event status is cleared upon a READ operation on the INT_STAT register. 1h = VBATP SSC event occurred with respect to VS1_THRES2A or VS1_THRES2B.
D[9]	VS0	0h	RC	0h = Either no VBATP occurs judging from VS0_THRES2A or VS0_THRES2B, or the VBATP SSC event status is cleared upon a READ operation on the INT_STAT register. 1h = VBATP SSC event occurred with respect to VS0_THRES2A or VS0_THRES2B.
SGMCD1024AQ				
D[12:9]	RESERVED	0h	R	Reserved.
D[8]	CRC_CALC	0h	RC	0h = CRC calculation may be running, unstarted, or the related event shall be acknowledged upon execution of a READ operation on the INT_STAT register. 1h = CRC calculation is finished. To confirm proper programming of register configurations, a CRC calculation can be initiated. After the operation finishes, the CRC_CALC bit is asserted to logic 1 as a completion indicator, and users may read the outcome from the CRC register.
D[7]	UV	0h	RC	0h = Either no under-voltage event (UV) is identified, or the UV status is cleared upon a READ operation on the INT_STAT register. 1h = UV events occurred or cleared on the VBATP pin.
D[6]	OV	0h	RC	0h = Either no over-voltage event (OV) is identified, or the OV status is cleared upon a READ operation on the INT_STAT register. 1h = OV events occurred or cleared on the VBATP pin.
D[5]	TW	0h	RC	0h = Either no temperature warning (TW) is identified, or the TW status is cleared upon a READ operation on the INT_STAT register. 1h = Temperature warning event occurred or cleared.
D[4]	TSD	0h	RC	0h = Either no temperature shutdown (TSD) is identified, or the TSD status is cleared upon a READ operation on the INT_STAT register. 1h = Temperature Shutdown event occurred or cleared.

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REGISTER MAPS (continued)

BITS	BIT NAME	RESET	TYPE	DESCRIPTION
D[3]	SSC	0h	RC	0h = Either no switch status change (SSC) is identified, or the SSC status is cleared upon a READ operation on the INT_STAT register. 1h = Switch state change occurred.
D[2]	PRTY_FAIL	0h	RC	0h = Either no error judging from the parity diagnostic routine is identified, or the MOSI parity check status is cleared upon a READ operation on the INT_STAT register. 1h = Parity error occurred. PRTY_FAIL set to logic 1 indicates a parity error on the MOSI transaction. The device operates with odd parity. Received data is dropped when the total number of 1-bits (parity bit included) is even. This bit is duplicated to the PRTY_FLAG status flag.
D[1]	SPI_FAIL	0h	RC	0h = Either no error judging from the SPI diagnostic routine is identified, or the SPI diagnostic status is cleared upon a READ operation on the INT_STAT register. 1h = SPI error occurred. A logic-high state on the SPI_FAIL bit signifies that the preceding SPI MOSI transfer is invalid. A complete 32-bit word must be supplied to the device for successful programming. Bit-counting circuitry within the SPI peripheral tallies clock-driven bits fed into the IC; data capture is permitted solely when precisely 32 bits have been shifted in. Any word-length deviation above or below the expected bit count causes the SPI_FAIL bit to be set to logic 1, marking incoming data as invalid. The state of this bit is duplicated on the SPI_FLAG status flag.
D[0]	POR	1h	RC	0h = Either no Power-On-Reset (POR) event is identified, or the POR status is cleared upon a READ operation on the INT_STAT register. 1h = Power-On-Reset (POR) event occurred.

REG3h: CRC Register [Reset = DBACh]

The result of the CRC-16-CCITT computation is returned by this register. A comparison between this value and the result calculated on-side by the microcontroller enables validation of properly programmed device register settings.

BITS	BIT NAME	RESET	TYPE	DESCRIPTION
D[23:1]	RESERVED	0h	R	Reserved.
D[15:0]	CRC	DBACh	R	CRC-16-CCITT calculation result: Bit [1] is the LSB, while bit [16] is the MSB.

REG4h: IN_STAT_MISC Register [Reset = 0h]

This register indicates current device status unrelated to switch input monitoring.

BITS	BIT NAME	RESET	TYPE	DESCRIPTION
D[23:13]	RESERVED	0h	R	Reserved.
SGMCD1024DQ				
D[12]	ADC_D	0h	R	0h = No ADC self-diagnostic error. 1h = An error is identified from ADC self-diagnostic.
D[11:10]	SP[3:2]_D	0h	R	Current Sink State on SPx (x = 2, 3). 0h = Operational 1h = Abnormal
D[9:8]	SP[1:0]_D	0h	R	Current Source State on SPx (x = 0, 1). 0h = Operational 1h = Abnormal
D[7:6]	VS1_STAT	0h	R	0h = VBATP voltage is below threshold VS1_THRES2A. 1h = VBATP voltage is below threshold VS1_THRES2B and equal to or above threshold VS1_THRES2A. 2h = VBATP voltage is equal to or above threshold VS1_THRES2B. 3h = N/A.
D[5:4]	VS0_STAT	0h	R	0h = VBATP voltage is below threshold VS0_THRES2A. 1h = VBATP voltage is below threshold VS0_THRES2B and equal to or above threshold VS0_THRES2A. 2h = VBATP voltage is equal to or above threshold VS0_THRES2B. 3h = N/A
SGMCD1024AQ				
D[12:4]	RESERVED	0h	R	Reserved.

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REGISTER MAPS (continued)

BITS	BIT NAME	RESET	TYPE	DESCRIPTION
D[3]	UV_STAT	0h	R	0h = VBATP voltage is above the under-voltage condition threshold. 1h = VBATP voltage is below the under-voltage condition threshold.
D[2]	OV_STAT	0h	R	0h = VBATP voltage is below the over-voltage condition threshold. 1h = VBATP voltage is above the over-voltage condition threshold.
D[1]	TW_STAT	0h	R	0h = T_j is below the temperature warning threshold T_{TW} . 1h = T_j is above the temperature warning threshold T_{TW} .
D[0]	TSD_STAT	0h	R	0h = T_j is below the temperature shutdown threshold T_{TSD} . 1h = T_j is above the temperature shutdown threshold T_{TSD} .

REG5h: IN_STAT_COMP Register [Reset = 0h]

BITS	BIT NAME	RESET	TYPE	DESCRIPTION
D[23:10]	INC[23:10]	R	0h	INC[23:10] bits indicates whether SGx (x = 13 to 0) input is below or above the comparator threshold when it is configured as comparator input mode. 0h = Input SGx is below the comparator threshold. 1h = Input SGx is above the comparator threshold.
D[9:0]	INC[9:0]	R	0h	INC[9:0] bits indicates whether SPx (x = 9 to 0) input is below or above the comparator threshold when it is configured as comparator input mode. 0h = Input SPx is below the comparator threshold. 1h = Input SPx is above the comparator threshold.

REG6h: IN_STAT_ADC0 Register [Reset = 0h] (SGMCD1024DQ Only)

This register shows the switch status comparison results for SP0-SG1 when ADC input mode is selected. SG2-SG7 support two thresholds, with 2 register bits indicating the input is below, above, or in-between both threshold levels.

BITS	BIT NAME	RESET	TYPE	DESCRIPTION
D[23:22]	INA17	0h	R	0h = Input SGx (x = 7 to 2) is below threshold 2A. 1h = Input SGx (x = 7 to 2) is below threshold 2B and equal to or above threshold 2A. 2h = Input SGx (x = 7 to 2) is equal to or above threshold 2B. 3h = N/A
D[21:20]	INA16	0h	R	
D[19:18]	INA15	0h	R	
D[17:16]	INA14	0h	R	
D[15:14]	INA13	0h	R	
D[13:12]	INA12	0h	R	0h = Input SGx (x = 1 to 0) is below configured threshold. 1h = Input SGx (x = 1 to 0) is above configured threshold.
D[11:10]	INA[11:10]	0h	R	
D[9:0]	INA[9:0]	0h	R	0h = Input SPx (x = 9 to 0) is below configured threshold. 1h = Input SPx (x = 9 to 0) is above configured threshold.

REG7h: IN_STAT_ADC1 Register [Reset = 0h] (SGMCD1024DQ Only)

This register shows SG8-SG13 switch status comparison results when ADC input mode is selected.

BITS	BIT NAME	RESET	TYPE	DESCRIPTION
D[23:13]	RESERVED	0h	R	Reserved.
D[12:10]	INA_23	0h	R	0h = Input SGx (x = 13 to 8) is below threshold 3A. 1h = Input SG x (x = 13 to 8) is below threshold 3B and equal to or above threshold 3A. 2h = Input SG x (x = 13 to 8) is below threshold 3C and equal to or above threshold 3B. 3h = Input SG13 is below threshold THRES8 or SGx (x = 12 to 8) equal to or above threshold 3C. 4h = Input SG13 is below threshold THRES9 and equal to or above threshold THRES8. 5h = Input SG13 is equal to or above threshold THRES9.
D[9:8]	INA_22	0h	R	
D[7:6]	INA_21	0h	R	
D[5:4]	INA_20	0h	R	
D[3:2]	INA_19	0h	R	
D[1:0]	INA_18	0h	R	

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REGISTER MAPS (continued)

REG8h: IN_STAT_MATRIX0 Register [Reset = 0h]

BITS	BIT NAME	RESET	TYPE	DESCRIPTION
D[23:18]	INMAT_13_SP[9:4]	0h	R	0h = Input SG3 is below threshold while SPx (x = 9 to 4) pulled to GND. 1h = Input SG3 is above threshold while SPx (x = 9 to 4) pulled to GND.
D[17:12]	INMAT_12_SP[9:4]	0h	R	0h = Input SG2 is below threshold while SPx (x = 9 to 4) pulled to GND. 1h = Input SG2 is above threshold while SPx (x = 9 to 4) pulled to GND.
D[11:6]	INMAT_11_SP[9:4]	0h	R	0h = Input SG1 is below threshold while SPx (x = 9 to 4) pulled to GND. 1h = Input SG1 is above threshold while SPx (x = 9 to 4) pulled to GND.
D[5:0]	INMAT_10_SP[9:4]	0h	R	0h = Input SG0 is below threshold while SPx (x = 9 to 4) pulled to GND. 1h = Input SG0 is above threshold while SPx (x = 9 to 4) pulled to GND.

REG9h: IN_STAT_MATRIX1 Register [Reset = 0h]

BITS	BIT NAME	RESET	TYPE	DESCRIPTION
D[23:22]	SG[1:0]_COM	0h	R	0h = Input SGx (x = 1 to 0) below threshold THRES_COM. 1h = Input SGx (x = 1 to 0) equal to or above threshold THRES_COM.
D[21:12]	SP[9:0]_COM	0h	R	0h = Input SPx (x = 9 to 0) below threshold THRES_COM. 1h = Input SPx (x = 9 to 0) equal to or above threshold THRES_COM.
D[11:6]	INMAT_15_SP[9:4]	0h	R	0h = Input SG5 below threshold while SPx (x = 9 to 4) pulled to GND. 1h = Input SG5 above threshold while SPx (x = 9 to 4) pulled to GND.
D[5:0]	INMAT_14_SP[9:4]	0h	R	0h = Input SG4 below threshold while SPx (x = 9 to 4) pulled to GND. 1h = Input SG4 above threshold while SPx (x = 9 to 4) pulled to GND.

REGAh: ANA_STAT0 Register [Reset = 0h] (SGMCD1024DQ Only)

BITS	BIT NAME	RESET	TYPE	DESCRIPTION
D[23:20]	RESERVED	0h	R	Reserved.
D[19:10]	SP1_ANA	0h	R	10-bits value of SP1. Bit 10: LSB Bit 19: MSB
D[9:0]	SP0_ANA	0h	R	10-bits value of SP0. Bit 0: LSB Bit 9: MSB

REGBh: ANA_STAT1 Register [Reset = 0h] (SGMCD1024DQ Only)

BITS	BIT NAME	RESET	TYPE	DESCRIPTION
D[23:20]	RESERVED	0h	R	Reserved.
D[19:10]	SP3_ANA	0h	R	10-bits value of SP3. Bit 10: LSB Bit 19: MSB
D[9:0]	SP2_ANA	0h	R	10-bits value of SP2. Bit 0: LSB Bit 9: MSB

REGCh: ANA_STAT2 Register [Reset = 0h] (SGMCD1024DQ Only)

BITS	BIT NAME	RESET	TYPE	DESCRIPTION
D[23:20]	RESERVED	0h	R	Reserved.
D[19:10]	SP5_ANA	0h	R	10-bits value of SP5. Bit 10: LSB Bit 19: MSB
D[9:0]	SP4_ANA	0h	R	10-bits value of SP4. Bit 0: LSB Bit 9: MSB

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REGISTER MAPS (continued)

REGDh: ANA_STAT3 Register [Reset = 0h] (SGMCD1024DQ Only)

BITS	BIT NAME	RESET	TYPE	DESCRIPTION
D[23:20]	RESERVED	0h	R	Reserved.
D[19:10]	SP7_ANA	0h	R	10-bits value of SP7. Bit 10: LSB Bit 19: MSB
D[9:0]	SP6_ANA	0h	R	10-bits value of SP6. Bit 0: LSB Bit 9: MSB

REGEh: ANA_STAT4 Register [Reset = 0h] (SGMCD1024DQ Only)

BITS	BIT NAME	RESET	TYPE	DESCRIPTION
D[23:20]	RESERVED	0h	R	Reserved.
D[19:10]	SP9_ANA	0h	R	10-bits value of SP9. Bit 10: LSB Bit 19: MSB
D[9:0]	SP8_ANA	0h	R	10-bits value of SP8. Bit 0: LSB Bit 9: MSB

REGFh: ANA_STAT5 Register [Reset = 0h] (SGMCD1024DQ Only)

BITS	BIT NAME	RESET	TYPE	DESCRIPTION
D[23:20]	RESERVED	0h	R	Reserved.
D[19:10]	SG1_ANA	0h	R	10-bits value of SG1. Bit 10: LSB Bit 19: MSB
D[9:0]	SG0_ANA	0h	R	10-bits value of SG0. Bit 0: LSB Bit 9: MSB

REG10h: ANA_STAT6 Register [reset = 0h] (SGMCD1024DQ Only)

BITS	BIT NAME	RESET	TYPE	DESCRIPTION
D[23:20]	RESERVED	0h	R	Reserved.
D[19:10]	SG3_ANA	0h	R	10-bits value of SG3. Bit 10: LSB Bit 19: MSB
D[9:0]	SG2_ANA	0h	R	10-bits value of SG2. Bit 0: LSB Bit 9: MSB

REG11h: ANA_STAT7 Register [Reset = 0h] (SGMCD1024DQ Only)

BITS	BIT NAME	RESET	TYPE	DESCRIPTION
D[23:20]	RESERVED	0h	R	Reserved.
D[19:10]	SG5_ANA	0h	R	10-bits value of SG5. Bit 10: LSB Bit 19: MSB
D[9:0]	SG4_ANA	0h	R	10-bits value of SG4. Bit 0: LSB Bit 9: MSB

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REGISTER MAPS (continued)

REG12h: ANA_STAT8 Register [Reset = 0h] (SGMCD1024DQ Only)

BITS	BIT NAME	RESET	TYPE	DESCRIPTION
D[23:20]	RESERVED	0h	R	Reserved.
D[19:10]	SG7_ANA	0h	R	10-bits value of SG7. Bit 10: LSB Bit 19: MSB
D[9:0]	SG6_ANA	0h	R	10-bits value of SG6. Bit 0: LSB Bit 9: MSB

REG13h: ANA_STAT9 Register [Reset = 0h] (SGMCD1024DQ Only)

BITS	BIT NAME	RESET	TYPE	DESCRIPTION
D[23:20]	RESERVED	0h	R	Reserved.
D[19:10]	SG9_ANA	0h	R	10-bits value of SG9. Bit 10: LSB Bit 19: MSB
D[9:0]	SG8_ANA	0h	R	10-bits value of SG8. Bit 0: LSB Bit 9: MSB

REG14h: ANA_STAT10 Register [Reset = 0h] (SGMCD1024DQ Only)

BITS	BIT NAME	RESET	TYPE	DESCRIPTION
D[23:20]	RESERVED	0h	R	Reserved.
D[19:10]	SG11_ANA	0h	R	10-bits value of SG11. Bit 10: LSB Bit 19: MSB
D[9:0]	SG10_ANA	0h	R	10-bits value of SG10. Bit 0: LSB Bit 9: MSB

REG15h: ANA_STAT11 Register [Reset = 0h] (SGMCD1024DQ Only)

BITS	BIT NAME	RESET	TYPE	DESCRIPTION
D[23:20]	RESERVED	0h	R	Reserved.
D[19:10]	SG13_ANA	0h	R	10-bits value of SG13. Bit 10: LSB Bit 19: MSB
D[9:0]	SG12_ANA	0h	R	10-bits value of SG12. Bit 0: LSB Bit 9: MSB

REG16h: ANA_STAT12 Register [Reset = 0h] (SGMCD1024DQ Only)

BITS	BIT NAME	RESET	TYPE	DESCRIPTION
D[23:20]	RESERVED	0h	R	Reserved.
D[19:10]	ADC_SELF_ANA	0h	R	10-bits value of the ADC self-diagnosis. Bit 10: LSB Bit 19: MSB
D[9:0]	VBATP_ANA	0h	R	10-bits value of V_{BATP} measurement. Bit 0: LSB Bit 9: MSB

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REGISTER MAPS (continued)

REG1Ah: CONFIG Register [Reset = 0h]

BITS	BIT NAME	RESET	TYPE	DESCRIPTION
SGMCD1024DQ				
D[23]	VBATP_RATIO	0h	R/W	0h = Use voltage divider factor of 3 for the V_{BATP} measurement. 1h = Use voltage divider factor of 10 for the V_{BATP} measurement.
D[22]	ADC_DIAG_T	0h	R/W	0h = Disable ADC self-diagnostic feature. 1h = Enable ADC self-diagnostic feature.
D[21:18]	WET_D_SP[3:0]_EN	0h	R/W	0h = Disable wetting current diagnostic for input SPx (x = 3 to 0). 1h = Enable wetting current diagnostic for input SPx (x = 3 to 0).
D[17]	VBATP_MEAS_EN	0h	R/W	0h = Disable V_{BATP} measurement at the end of every polling cycle. 1h = Enable V_{BATP} measurement at the end of every polling cycle.
SGMCD1024AQ				
D[23:17]	RESERVED	0h	R	Reserved.
D[16]	TW_CUR_DIS_CSI	0h	R/W	0h = Wetting current of 5mA is reduced to 2mA for SGMCD1024AQ, while wetting current of 10mA and 15mA is reduced to 2mA for SGMCD1024DQ upon TW event for all active SP inputs. 1h = No wetting current reduction upon TW event for all active SP inputs.
D[15:14]	DET_FILTER	0h	R/W	0h = Every sample is valid and taken for threshold evaluation. 1h = 2 consecutive and equal samples required to be valid data. 2h = 3 consecutive and equal samples required to be valid data. 3h = 4 consecutive and equal samples required to be valid data.
D[13]	TW_CUR_DIS_CSO	0h	R/W	0h = Wetting current of 5mA is reduced to 2mA for SGMCD1024AQ, while wetting current of 10mA and 15mA is reduced to 2mA for SGMCD1024DQ upon TW event for all active SP inputs. 1h = No wetting current reduction upon TW event for all active SG inputs.
D[12]	INT_CONFIG	0h	R/W	0h = Static 1h = Dynamic
D[11]	TRIGGER	0h	R/W	Setting TRIGGER = 1 starts normal device operation like wetting-current activation and polling, while clearing this bit to 0 stops operation and enters idle state. To modify settings after operation has begun, the MCU shall first set TRIGGER to 0. Reset TRIGGER to 1 after reconfiguration to restart operation. Dynamic configuration changes while the device is running may trigger false switch readings and unwanted interrupts. The following register bits are the exception and can be configured when TRIGGER bit is set to logic 1: • TRIGGER (bit 11 of the CONFIG register) • CRC_T (bit 9 of the CONFIG register) • RESET (bit 0 of the CONFIG register) • The CCP_CFG1 register 0h = Stop SGMCD1024xQ from normal operation. 1h = Trigger SGMCD1024xQ from normal operation.
D[10]	POLL_EN	0h	R/W	0h = Polling disabled. Device operates in continuous mode. 1h = Polling enabled and the device operates in one of the polling modes.
D[9]	CRC_T	0h	R/W	Writing this bit to 1 starts a CRC check across all configuration registers. After trigger, avoid modifying configuration registers via SPI before CRC finishes to prevent invalid CRC results. SGMCD1024xQ raises the CRC_CALC interrupt flag and pulls INT_B pin low once CRC completes; the result is accessible from the CRC register. This bit self-resets to 0 following CRC execution. 0h = no CRC calculation triggered. 1h = trigger CRC calculation.
D[8:5]	POLL_ACT_TIME	0h	R/W	0h = 64μs 1h = 128μs 2h = 192μs 3h = 256μs 4h = 320μs 5h = 384μs 6h = 448μs 7h = 512μs 8h = 640μs 9h = 768μs Ah = 896μs Bh = 1024μs Ch = 2048μs Dh ~ Fh = 512μs (most frequently-used setting)

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REGISTER MAPS (continued)

BITS	BIT NAME	RESET	TYPE	DESCRIPTION
D[4:1]	POLL_TIME	0h	R/W	0h = 2ms 1h = 4ms 2h = 8ms 3h = 16ms 4h = 32ms 5h = 48ms 6h = 64ms 7h = 128ms 8h = 256ms 9h = 512ms Ah = 1024ms Bh = 2048ms Ch = 4096ms Dh ~ Fh = 8ms (most frequently-used setting)
D[0]	RESET	0h	R/W	0h = No reset. 1h = Trigger software reset of the device.

REG1Bh: IN_EN Register [Reset = 0h]

BITS	BIT NAME	RESET	TYPE	DESCRIPTION
D[23:10]	IN_EN_SG[13:0]	0h	R/W	0h = Input channel SGx (x = 13 to 0) disabled. Polling sequence skips this channel 1h = Input channel SGx (x = 13 to 0) enabled.
D[9:0]	IN_EN_SP[9:0]	0h	R/W	0h = Input channel SPx (x = 9 to 0) disabled. Polling sequence skips this channel 1h = Input channel SPx (x = 9 to 0) enabled.

REG1Ch: CS_SELECT Register [Reset = 0h]

BITS	BIT NAME	RESET	TYPE	DESCRIPTION
D[23:10]	RESERVED	0h	R/W	Reserved.
D[9:0]	CS_SP[9:0]	0h	R/W	0h = Current Source (CSO) in default. CSO is equal to SG. 1h = Current Sink (CSI) selected.

REG1Dh: WC_CFG0 Register [Reset = 0h]

BITS	BIT NAME	RESET	TYPE	DESCRIPTION
SGMCD1024AQ				
D[23:21]	WC_SG1	0h	R/W	0h = No wetting current 1h = 1mA (TYP) wetting current 2h = 2mA (TYP) wetting current 3h = 5mA (TYP) wetting current 4h ~ 7h = Reserved
D[20:18]	WC_SG0	0h	R/W	
D[17:15]	WC_SP8_SP9	0h	R/W	
D[14:12]	WC_SP6_SP7	0h	R/W	
D[11:9]	WC_SP5	0h	R/W	
D[8:6]	WC_SP4	0h	R/W	
D[5:3]	WC_SP2_SP3	0h	R/W	
D[2:0]	WC_SP0_SP1	0h	R/W	
SGMCD1024DQ				
D[23:21]	WC_SG1	0h	R/W	0h = No wetting current 1h = 1mA (TYP) wetting current 2h = 2mA (TYP) wetting current 3h = 5mA (TYP) wetting current 4h = 10mA (TYP) wetting current 5h ~ 7h = 15mA (TYP) wetting current
D[20:18]	WC_SG0	0h	R/W	
D[17:15]	WC_SP8_SP9	0h	R/W	
D[14:12]	WC_SP6_SP7	0h	R/W	
D[11:9]	WC_SP5	0h	R/W	
D[8:6]	WC_SP4	0h	R/W	
D[5:3]	WC_SP2_SP3	0h	R/W	
D[2:0]	WC_SP0_SP1	0h	R/W	

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REGISTER MAPS (continued)

REG1Eh: WC_CFG1 Register [Reset = 0h]

BITS	BIT NAME	RESET	TYPE	DESCRIPTION
D[23]	RESERVED	0h	R	Reserved.
SGMCD1024AQ				
D[22]	AUTO_SCALE_DIS_CSI	0h	R/W	0h = Wetting current of 5mA is reduced to 2mA upon switch closure event for all active SP inputs. 1h = No wetting current reduction upon switch closure event for all active SP inputs.
D[21]	AUTO_SCALE_DIS_CSO	0h	R/W	0h = Wetting current of 5mA is reduced to 2mA upon switch closure event for all active SG inputs. 1h = No wetting current reduction upon switch closure event for all active SG inputs.
D[20:18]	WC_SG13	0h	R/W	0h = No wetting current 1h = 1mA (TYP) wetting current 2h = 2mA (TYP) wetting current 3h = 5mA (TYP) wetting current 4h ~ 7h = Reserved
D[17:15]	WC_SG12	0h	R/W	
D[14:12]	WC_SG10_SG11	0h	R/W	
D[11:9]	WC_SG8_SG9	0h	R/W	
D[8:6]	WC_SG6_SG7	0h	R/W	
D[5:3]	WC_SG4_SG5	0h	R/W	
D[2:0]	WC_SG2_SG3	0h	R/W	
SGMCD1024DQ				
D[22]	AUTO_SCALE_DIS_CSI	0h	R/W	0h = Wetting current of 10mA and 15mA is reduced to 2mA upon switch closure event for all active SP inputs. 1h = No wetting current reduction upon switch closure event for all active SP inputs.
D[21]	AUTO_SCALE_DIS_CSO	0h	R/W	0h = Wetting current of 10mA and 15mA is reduced to 2mA upon switch closure event for all active SG inputs. 1h = No wetting current reduction upon switch closure event for all active SG inputs.
D[20:18]	WC_SG13	0h	R/W	0h = No wetting current 1h = 1mA (TYP) wetting current 2h = 2mA (TYP) wetting current 3h = 5mA (TYP) wetting current 4h = 10mA (TYP) wetting current 5h ~ 7h = 15mA (TYP) wetting current
D[17:15]	WC_SG12	0h	R/W	
D[14:12]	WC_SG10_SG11	0h	R/W	
D[11:9]	WC_SG8_SG9	0h	R/W	
D[8:6]	WC_SG6_SG7	0h	R/W	
D[5:3]	WC_SG4_SG5	0h	R/W	
D[2:0]	WC_SG2_SG3	0h	R/W	

REG1Fh: CCP_CFG0 Register [Reset = 0h]

BITS	BIT NAME	RESET	TYPE	DESCRIPTION
D[23:7]	RESERVED	0h	R	Reserved.
D[6:4]	CCP_TIME	0h	R/W	Wetting current activation time in CCP mode. 0h = 64µs 1h = 128µs 2h = 192µs 3h = 256µs 4h = 320µs 5h = 384µs 6h = 448µs 7h = 512µs
SGMCD1024DQ				
D[3]	WC_CCP3	0h	R/W	Wetting current setting for SG8 to SG13 in CCP mode. 0h = 10mA (TYP) 1h = 15mA (TYP)
D[2]	WC_CCP2	0h	R/W	Wetting current setting for SG2 to SG7 in CCP mode. 0h = 10mA (TYP) 1h = 15mA (TYP)

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REGISTER MAPS (continued)

BITS	BIT NAME	RESET	TYPE	DESCRIPTION
D[1]	WC_CCP1	0h	R/W	Wetting current setting for SP6 to SG1 in CCP mode. 0h = 10mA (TYP) 1h = 15mA (TYP)
D[0]	WC_CCP0	0h	R/W	Wetting current setting for SP0 to SP5 in CCP mode. 0h = 10mA (TYP) 1h = 15mA (TYP)
SGMCD1024AQ				
D[3:0]	RESERVED	0h	R	Reserved.

REG20h: CCP_CFG1 Register [Reset = 0h]

BITS	BIT NAME	RESET	TYPE	DESCRIPTION
D[23:10]	CCP_SG[13:0]	0h	R/W	0h = No CCP wetting current 1h = CCP wetting current activated
D[9:0]	CCP_SP[9:0]	0h	R/W	0h = No CCP wetting current 1h = CCP wetting current activated

REG21h: THRES_COMP Register [Reset = 0h]

BITS	BIT NAME	RESET	TYPE	DESCRIPTION
D[23:12]	RESERVED	0h	R	Reserved.
D[11:10]	THRES_COMP_SG10_SG13	0h	R/W	Comparator thresholds setting for SG10 to SG13 channels. 0h = 2V 1h = 2.7V 2h = 3V 3h = 4V
D[9:8]	THRES_COMP_SG6_SG9	0h	R/W	Comparator thresholds setting for SG6 to SG9 channels. 0h = 2V 1h = 2.7V 2h = 3V 3h = 4V
D[7:6]	THRES_COMP_SG2_SG5	0h	R/W	Comparator thresholds setting for SG2 to SG5 channels. 0h = 2V 1h = 2.7V 2h = 3V 3h = 4V
D[5:4]	THRES_COMP_SP8_SG1	0h	R/W	Comparator thresholds setting for SP8 to SG1 channels. 0h = 2V 1h = 2.7V 2h = 3V 3h = 4V
D[3:2]	THRES_COMP_SP4_SP7	0h	R/W	Comparator thresholds setting for SP4 to SP7 channels. 0h = 2V 1h = 2.7V 2h = 3V 3h = 4V
D[1:0]	THRES_COMP_SP0_SP3	0h	R/W	Comparator thresholds setting for SP0 to SP3 channels. 0h = 2V 1h = 2.7V 2h = 3V 3h = 4V

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REGISTER MAPS (continued)

REG22h: INT_EN_COMP1 Register [Reset = 0h]

BITS	BIT NAME	RESET	TYPE	DESCRIPTION
D[23:22]	INC_EN_11	0h	R/W	Interrupt Generation Conditions of SG1. 0h = No interrupt generation. 1h = Interrupt generation on rising edge above THRES_COMP_SP8_SG1. 2h = Interrupt generation on falling edge below THRES_COMP_SP8_SG1. 3h = Interrupt generation on falling and rising edge of THRES_COMP_SP8_SG1.
D[21:20]	INC_EN_10	0h	R/W	Interrupt Generation Conditions of SG0. 0h = No interrupt generation. 1h = Interrupt generation on rising edge above THRES_COMP_SP8_SG1. 2h = Interrupt generation on falling edge below THRES_COMP_SP8_SG1. 3h = Interrupt generation on falling and rising edge of THRES_COMP_SP8_SG1.
D[19:18]	INC_EN_9	0h	R/W	Interrupt Generation Conditions of SP9. 0h = No interrupt generation. 1h = Interrupt generation on rising edge above THRES_COMP_SP8_SG1. 2h = Interrupt generation on falling edge below THRES_COMP_SP8_SG1. 3h = Interrupt generation on falling and rising edge of THRES_COMP_SP8_SG1.
D[17:16]	INC_EN_8	0h	R/W	Interrupt Generation Conditions of SP8. 0h = No interrupt generation. 1h = Interrupt generation on rising edge above THRES_COMP_SP8_SG1. 2h = Interrupt generation on falling edge below THRES_COMP_SP8_SG1. 3h = Interrupt generation on falling and rising edge of THRES_COMP_SP8_SG1.
D[15:14]	INC_EN_7	0h	R/W	Interrupt Generation Conditions of SP7. 0h = No interrupt generation. 1h = Interrupt generation on rising edge above THRES_COMP_SP4_SP7. 2h = Interrupt generation on falling edge below THRES_COMP_SP4_SP7. 3h = Interrupt generation on falling and rising edge of THRES_COMP_SP4_SP7.
D[13:12]	INC_EN_6	0h	R/W	Interrupt Generation Conditions of SP6. 0h = No interrupt generation. 1h = Interrupt generation on rising edge above THRES_COMP_SP4_SP7. 2h = Interrupt generation on falling edge below THRES_COMP_SP4_SP7. 3h = Interrupt generation on falling and rising edge of THRES_COMP_SP4_SP7.
D[11:10]	INC_EN_5	0h	R/W	Interrupt Generation Conditions of SP5. 0h = No interrupt generation. 1h = Interrupt generation on rising edge above THRES_COMP_SP4_SP7. 2h = Interrupt generation on falling edge below THRES_COMP_SP4_SP7. 3h = Interrupt generation on falling and rising edge of THRES_COMP_SP4_SP7.
D[9:8]	INC_EN_4	0h	R/W	Interrupt Generation Conditions of SP4. 0h = No interrupt generation. 1h = Interrupt generation on rising edge above THRES_COMP_SP4_SP7. 2h = Interrupt generation on falling edge below THRES_COMP_SP4_SP7. 3h = Interrupt generation on falling and rising edge of THRES_COMP_SP4_SP7.
D[7:6]	INC_EN_3	0h	R/W	Interrupt Generation Conditions of SP3. 0h = No interrupt generation. 1h = Interrupt generation on rising edge above THRES_COMP_SP0_SP3. 2h = Interrupt generation on falling edge below THRES_COMP_SP0_SP3. 3h = Interrupt generation on falling and rising edge of THRES_COMP_SP0_SP3.
D[5:4]	INC_EN_2	0h	R/W	Interrupt Generation Conditions of SP2. 0h = no interrupt generation. 1h = Interrupt generation on rising edge above THRES_COMP_SP0_SP3. 2h = Interrupt generation on falling edge below THRES_COMP_SP0_SP3. 3h = Interrupt generation on falling and rising edge of THRES_COMP_SP0_SP3.
D[3:2]	INC_EN_1	0h	R/W	Interrupt Generation Conditions of SP1. 0h = no interrupt generation. 1h = Interrupt generation on rising edge above THRES_COMP_SP0_SP3. 2h = Interrupt generation on falling edge below THRES_COMP_SP0_SP3. 3h = Interrupt generation on falling and rising edge of THRES_COMP_SP0_SP3.
D[1:0]	INC_EN_0	0h	R/W	Interrupt Generation Conditions of SP0. 0h = No interrupt generation. 1h = Interrupt generation on rising edge above THRES_COMP_SP0_SP3. 2h = Interrupt generation on falling edge below THRES_COMP_SP0_SP3. 3h = Interrupt generation on falling and rising edge of THRES_COMP_SP0_SP3.

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REGISTER MAPS (continued)

REG23h: INT_EN_COMP2 Register [Reset = 0h]

BITS	BIT NAME	RESET	TYPE	DESCRIPTION
D[23:22]	INC_EN_23	0h	R/W	Interrupt Generation Conditions of SG13. 0h = No interrupt generation. 1h = Interrupt generation on rising edge above THRES_COMP_SG10_SG13. 2h = Interrupt generation on falling edge below THRES_COMP_SG10_SG13. 3h = Interrupt generation on falling and rising edge of THRES_COMP_SG10_SG13.
D[21:20]	INC_EN_22	0h	R/W	Interrupt Generation Conditions of SG12. 0h = No interrupt generation. 1h = Interrupt generation on rising edge above THRES_COMP_SG10_SG13. 2h = Interrupt generation on falling edge below THRES_COMP_SG10_SG13. 3h = Interrupt generation on falling and rising edge of THRES_COMP_SG10_SG13.
D[19:18]	INC_EN_21	0h	R/W	Interrupt Generation Conditions of SG11. 0h = No interrupt generation. 1h = Interrupt generation on rising edge above THRES_COMP_SG10_SG13. 2h = Interrupt generation on falling edge below THRES_COMP_SG10_SG13. 3h = Interrupt generation on falling and rising edge of THRES_COMP_SG10_SG13.
D[17:16]	INC_EN_20	0h	R/W	Interrupt Generation Conditions of SG10. 0h = no interrupt generation. 1h = Interrupt generation on rising edge above THRES_COMP_SG10_SG13. 2h = Interrupt generation on falling edge below THRES_COMP_SG10_SG13. 3h = Interrupt generation on falling and rising edge of THRES_COMP_SG10_SG13.
D[15:14]	INC_EN_19	0h	R/W	Interrupt Generation Conditions of SG9. 0h = no interrupt generation. 1h = Interrupt generation on rising edge above THRES_COMP_SG6_SG9. 2h = Interrupt generation on falling edge below THRES_COMP_SG6_SG9. 3h = Interrupt generation on falling and rising edge of THRES_COMP_SG6_SG9.
D[13:12]	INC_EN_18	0h	R/W	Interrupt Generation Conditions of SG8. 0h = no interrupt generation. 1h = Interrupt generation on rising edge above THRES_COMP_SG6_SG9. 2h = Interrupt generation on falling edge below THRES_COMP_SG6_SG9. 3h = Interrupt generation on falling and rising edge of THRES_COMP_SG6_SG9.
D[11:10]	INC_EN_17	0h	R/W	Interrupt Generation Conditions of SG7. 0h = no interrupt generation. 1h = Interrupt generation on rising edge above THRES_COMP_SG6_SG9. 2h = Interrupt generation on falling edge below THRES_COMP_SG6_SG9. 3h = Interrupt generation on falling and rising edge of THRES_COMP_SG6_SG9.
D[9:8]	INC_EN_16	0h	R/W	Interrupt Generation Conditions of SG6. 0h = No interrupt generation. 1h = Interrupt generation on rising edge above THRES_COMP_SG6_SG9. 2h = Interrupt generation on falling edge below THRES_COMP_SG6_SG9. 3h = Interrupt generation on falling and rising edge of THRES_COMP_SG6_SG9.
D[7:6]	INC_EN_15	0h	R/W	Interrupt Generation Conditions of SG5. 0h = No interrupt generation. 1h = Interrupt generation on rising edge above THRES_COMP_SG2_SG5. 2h = Interrupt generation on falling edge below THRES_COMP_SG2_SG5. 3h = Interrupt generation on falling and rising edge of THRES_COMP_SG2_SG5.
D[5:4]	INC_EN_14	0h	R/W	Interrupt Generation Conditions of SG4. 0h = no interrupt generation. 1h = Interrupt generation on rising edge above THRES_COMP_SG2_SG5. 2h = Interrupt generation on falling edge below THRES_COMP_SG2_SG5. 3h = Interrupt generation on falling and rising edge of THRES_COMP_SG2_SG5.
D[3:2]	INC_EN_13	0h	R/W	Interrupt Generation Conditions of SG3. 0h = No interrupt generation. 1h = Interrupt generation on rising edge above THRES_COMP_SG2_SG5. 2h = Interrupt generation on falling edge below THRES_COMP_SG2_SG5. 3h = Interrupt generation on falling and rising edge of THRES_COMP_SG2_SG5.
D[1:0]	INC_EN_12	0h	R/W	Interrupt Generation Conditions of SG2. 0h = No interrupt generation. 1h = Interrupt generation on rising edge above THRES_COMP_SG2_SG5. 2h = Interrupt generation on falling edge below THRES_COMP_SG2_SG5. 3h = Interrupt generation on falling and rising edge of THRES_COMP_SG2_SG5.

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REGISTER MAPS (continued)

REG24h: INT_EN_CFG0 Register [Reset = 0h]

BITS	BIT NAME	RESET	TYPE	DESCRIPTION
SGMCD1024DQ				
D[23:12]	RESERVED	0h	R/W	Reserved.
D[11]	ADC_DIAG_EN	0h	R/W	INT_B Pin Assertion Conditions. 0h = ADC error disabled. 1h = ADC error enabled.
D[10]	WET_DIAG_EN	0h	R/W	INT_B Pin Assertion Conditions. 0h = wetting current error disabled. 1h = wetting current error enabled.
D[9]	VS1_EN	0h	R/W	INT_B Pin Assertion Conditions. 0h = VS1 threshold crossing disabled. 1h = VS1 threshold crossing enabled.
D[8]	VS0_EN	0h	R/W	INT_B Pin Assertion Conditions. 0h = VS0 threshold crossing disabled. 1h = VS0 threshold crossing enabled.
SGMCD1024AQ				
D[23:8]	RESERVED	0h	R/W	Reserved.
D[7]	CRC_CALC_EN	0h	R/W	INT_B Pin Assertion Conditions. 0h = CRC calculation completion disabled. 1h = CRC calculation completion enabled.
D[6]	UV_EN	0h	R/W	INT_B Pin Assertion Conditions. 0h = UV event disabled. 1h = UV event enabled.
D[5]	OV_EN	0h	R/W	INT_B Pin Assertion Conditions. 0h = OV event disabled. 1h = OV event enabled.
D[4]	TW_EN	0h	R/W	INT_B Pin Assertion Conditions. 0h = TW event disabled. 1h = TW event enabled.
D[3]	TSD_EN	0h	R/W	INT_B Pin Assertion Conditions. 0h = TSD event disabled. 1h = TSD event enabled.
D[2]	SSC_EN	0h	R/W	INT_B Pin Assertion Conditions. 0h = SSC event disabled. 1h = SSC event enabled.
D[1]	PRTY_FAIL_EN	0h	R/W	INT_B Pin Assertion Conditions. 0h = parity fail event disabled. 1h = parity fail event enabled.
D[0]	SPI_FAIL_EN	0h	R/W	INT_B Pin Assertion Conditions. 0h = SPI fail event disabled. 1h = SPI fail event enabled.

REG25h: INT_EN_CFG1 Register [Reset = 0h] (SGMCD1024DQ Only)

BITS	BIT NAME	RESET	TYPE	DESCRIPTION
D[23:22]	SG1_EN	0h	R/W	0h = No interrupt generation for SGx (x = 1 to 0). 1h = Interrupt generation on rising edge above THRESx for SGx (x = 1 to 0). 2h = Interrupt generation on falling edge below THRESx for SGx (x = 1 to 0). 3h = Interrupt generation on falling and rising edge of THRESx for SGx (x = 1 to 0).
D[21:20]	SG0_EN	0h	R/W	
D[19:18]	SP9_EN	0h	R/W	
D[17:16]	SP8_EN	0h	R/W	0h = No interrupt generation for SPx (x = 9 to 0). 1h = Interrupt generation on rising edge above THRESx for SPx (x = 9 to 0). 2h = Interrupt generation on falling edge below THRESx for SPx (x = 9 to 0). 3h = Interrupt generation on falling and rising edge of THRESx for SPx (x = 9 to 0).
D[15:14]	SP7_EN	0h	R/W	
D[13:12]	SP6_EN	0h	R/W	
D[11:10]	SP5_EN	0h	R/W	
D[9:8]	SP4_EN	0h	R/W	
D[7:6]	SP3_EN	0h	R/W	
D[5:4]	SP2_EN	0h	R/W	
D[3:2]	SP1_EN	0h	R/W	
D[1:0]	SP0_EN	0h	R/W	

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REGISTER MAPS (continued)

REG26h: INT_EN_CFG2 Register [Reset = 0h] (SGMCD1024DQ Only)

BITS	BIT NAME	RESET	TYPE	DESCRIPTION
D[23:20]	SG7_EN	0h	R/W	xx00 = No interrupt generation for SGx (x = 7 to 2) w.r.t. THRES2A. xx01 = Interrupt generation on rising edge above THRES2A for SGx (x = 7 to 2). xx10 = Interrupt generation on falling edge below THRES2A for SGx (x = 7 to 2). xx11 = Interrupt generation on falling and rising edge of THRES2A for SGx (x = 7 to 2). 00xx = No interrupt generation for SGx (x = 7 to 2) w.r.t. THRES2B. 01xx = Interrupt generation on rising edge above THRES2B for SGx (x = 7 to 2). 10xx = Interrupt generation on falling edge below THRES2B for SGx (x = 7 to 2). 11xx = Interrupt generation on falling and rising edge of THRES2B for SGx (x = 7 to 2).
D[19:16]	SG6_EN	0h	R/W	
D[15:12]	SG5_EN	0h	R/W	
D[11:8]	SG4_EN	0h	R/W	
D[7:4]	SG3_EN	0h	R/W	
D[3:0]	SG2_EN	0h	R/W	

REG27h: INT_EN_CFG3 Register [Reset = 0h] (SGMCD1024DQ Only)

BITS	BIT NAME	RESET	TYPE	DESCRIPTION
D[23:18]	SG11_EN	0h	R/W	xxxxx00 = No interrupt generation for SGx (x = 11 to 8) w.r.t. THRES3A. xxxxx01 = Interrupt generation on rising edge above THRES3A for SGx (x = 11 to 8) xxxxx10 = Interrupt generation on falling edge below THRES3A for SGx (x = 11 to 8) xxxxx11 = Interrupt generation on falling and rising edge of THRES3A for SGx (x = 11 to 8)
D[17:12]	SG10_EN	0h	R/W	
D[11:6]	SG9_EN	0h	R/W	xx00xx = No interrupt generation for SGx (x = 11 to 8) w.r.t. THRES3B. xx01xx = Interrupt generation on rising edge above THRES3B for SGx (x = 11 to 8) xx10xx = Interrupt generation on falling edge below THRES3B for SGx (x = 11 to 8) xx11xx = Interrupt generation on falling and rising edge of THRES3B for SGx (x = 11 to 8)
D[5:0]	SG8_EN	0h	R/W	

REG28h: INT_EN_CFG4 Register [Reset = 0h] (SGMCD1024DQ Only)

BITS	BIT NAME	RESET	TYPE	DESCRIPTION
D[23:20]	VS_TH1_EN	0h	R/W	xx00 = No interrupt generation for VBATP w.r.t. VS1_THRES2A. xx01 = Interrupt generation on rising edge above VS1_THRES2A for VBATP. xx10 = Interrupt generation on falling edge below VS1_THRES2A for VBATP. xx11 = Interrupt generation on falling and rising edge of VS1_THRES2A for VBATP. 00xx = no interrupt generation for VBATP w.r.t. VS1_THRES2B. 01xx = Interrupt generation on rising edge above VS1_THRES2B for VBATP. 10xx = Interrupt generation on falling edge below VS1_THRES2B for VBATP. 11xx = Interrupt generation on falling and rising edge of VS1_THRES2B for VBATP.
D[19:16]	VS_TH0_EN	0h	R/W	xx00 = No interrupt generation for VBATP w.r.t. VS0_THRES2A. xx01 = Interrupt generation on rising edge above VS0_THRES2A for VBATP. xx10 = Interrupt generation on falling edge below VS0_THRES2A for VBATP. xx11 = Interrupt generation on falling and rising edge of VS0_THRES2A for VBATP. 00xx = No interrupt generation for VBATP w.r.t. VS0_THRES2B. 01xx = Interrupt generation on rising edge above VS0_THRES2B for VBATP. 10xx = Interrupt generation on falling edge below VS0_THRES2B for VBATP. 11xx = Interrupt generation on falling and rising edge of VS0_THRES2B for VBATP.
D[15:6]	SG13_EN	0h	R/W	xxxxxxxx00 = No interrupt generation for SG13 w.r.t. THRES3A. xxxxxxxx01 = Interrupt generation on rising edge above THRES3A for SG13. xxxxxxxx10 = Interrupt generation on falling edge below THRES3A for SG13. xxxxxxxx11 = Interrupt generation on falling and rising edge of THRES3A for SG13. xxxxxx00xx = No interrupt generation for SG13 w.r.t. THRES3B. xxxxxx01xx = Interrupt generation on rising edge above THRES3B for SG13. xxxxxx10xx = Interrupt generation on falling edge below THRES3B for SG13. xxxxxx11xx = Interrupt generation on falling and rising edge of THRES3B for SG13. xxxxx00xxxx = No interrupt generation for SG13 w.r.t. THRES3C. xxxxx01xxxx = Interrupt generation on rising edge above THRES3C for SG13. xxxxx10xxxx = Interrupt generation on falling edge below THRES3C for SG13. xxxxx11xxxx = Interrupt generation on falling and rising edge of THRES3C for SG13. xx00xxxxxx = No interrupt generation for SG13 w.r.t. THRES8. xx01xxxxxx = Interrupt generation on rising edge above THRES8 for SG13. xx10xxxxxx = Interrupt generation on falling edge below THRES8 for SG13. xx11xxxxxx = Interrupt generation on falling and rising edge of THRES8 for SG13. 00xxxxxxx = No interrupt generation for SG13 w.r.t. THRES9. 01xxxxxxx = Interrupt generation on rising edge above THRES9 for SG13. 10xxxxxxx = Interrupt generation on falling edge below THRES9 for SG13. 11xxxxxxx = Interrupt generation on falling and rising edge of THRES9 for SG13.

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REGISTER MAPS (continued)

BITS	BIT NAME	RESET	TYPE	DESCRIPTION
D[5:0]	SG12_EN	0h	R/W	xxxx00 = No interrupt generation for SG12 w.r.t. THRES3A. xxxx01 = Interrupt generation on rising edge above THRES3A for SG12. xxxx10 = Interrupt generation on falling edge below THRES3A for SG12. xxxx11 = Interrupt generation on falling and rising edge of THRES3A for SG12. xx00xx = No interrupt generation for SG12 w.r.t. THRES3B. xx01xx = Interrupt generation on rising edge above THRES3B for SG12. xx10xx = Interrupt generation on falling edge below THRES3B for SG12. xx11xx = Interrupt generation on falling and rising edge of THRES3B for SG12. 00xxxx = No interrupt generation for SG12 w.r.t. THRES3C. 01xxxx = Interrupt generation on rising edge above THRES3C for SG12. 10xxxx = Interrupt generation on falling edge below THRES3C for SG12. 11xxxx = Interrupt generation on falling and rising edge of THRES3C for SG12.

REG29h: THRES_CFG0 Register [Reset = 0h] (SGMCD1024DQ Only)

BITS	BIT NAME	RESET	TYPE	DESCRIPTION
D[23:20]	RESERVED	0h	R	Reserved.
D[19:10]	THRES1	0h	R/W	10-bits value of threshold 1. Bit10: LSB Bit19: MSB
D[9:0]	THRES0	0h	R/W	10-bits value of threshold 0. Bit0: LSB Bit9: MSB

REG2Ah: THRES_CFG1 Register [Reset = 0h] (SGMCD1024DQ Only)

BITS	BIT NAME	RESET	TYPE	DESCRIPTION
D[23:20]	RESERVED	0h	R	Reserved.
D[19:10]	THRES3	0h	R/W	10-bits value of threshold 3. Bit10: LSB Bit19: MSB
D[9:0]	THRES2	0h	R/W	10-bits value of threshold 2. Bit0: LSB Bit9: MSB

REG2Bh: THRES_CFG2 Register [Reset = 0h] (SGMCD1024DQ Only)

BITS	BIT NAME	RESET	TYPE	DESCRIPTION
D[23:20]	RESERVED	0h	R	Reserved.
D[19:10]	THRES5	0h	R/W	10-bits value of threshold 5. Bit10: LSB Bit19: MSB
D[9:0]	THRES4	0h	R/W	10-bits value of threshold 4. Bit0: LSB Bit9: MSB

REG2Ch: THRES_CFG3 Register [Reset = 0h] (SGMCD1024DQ Only)

BITS	BIT NAME	RESET	TYPE	DESCRIPTION
D[23:20]	RESERVED	0h	R	Reserved.
D[19:10]	THRES7	0h	R/W	10-bits value of threshold 7. Bit10: LSB Bit19: MSB
D[9:0]	THRES6	0h	R/W	10-bits value of threshold 6. Bit0: LSB Bit9: MSB

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REGISTER MAPS (continued)

REG2Dh: THRES_CFG4 Register [Reset = 0h] (SGMCD1024DQ Only)

BITS	BIT NAME	RESET	TYPE	DESCRIPTION
D[23:20]	RESERVED	0h	R	Reserved.
D[19:10]	THRES9	0h	R/W	10-bits value of threshold 9. Bit10: LSB Bit19: MSB
D[9:0]	THRES8	0h	R/W	10-bits value of threshold 8. Bit0: LSB Bit9: MSB

REG2Eh: THRESMAP_CFG0 Register [Reset = 0h] (SGMCD1024DQ Only)

BITS	BIT NAME	RESET	TYPE	DESCRIPTION
D[23:21]	THRESMAP_SP7	0h	R/W	0h = THRES0 1h = THRES1 2h = THRES2 3h = THRES3 4h = THRES4 5h = THRES5 6h = THRES6 7h = THRES7
D[20:18]	THRESMAP_SP6	0h	R/W	
D[17:15]	THRESMAP_SP5	0h	R/W	
D[14:12]	THRESMAP_SP4	0h	R/W	
D[11:9]	THRESMAP_SP3	0h	R/W	
D[8:6]	THRESMAP_SP2	0h	R/W	
D[5:3]	THRESMAP_SP1	0h	R/W	
D[2:0]	THRESMAP_SP0	0h	R/W	

REG2Fh: THRESMAP_CFG1 Register [Reset = 0h] (SGMCD1024DQ Only)

BITS	BIT NAME	RESET	TYPE	DESCRIPTION
D[23:18]	RESERVED	0h	R	Reserved.
D[17:15]	THRESMAP_SG2_SG7_THRES2B	0h	R/W	0h = THRES0 1h = THRES1 2h = THRES2 3h = THRES3 4h = THRES4 5h = THRES5 6h = THRES6 7h = THRES7
D[14:12]	THRESMAP_SG2_SG7_THRES2A	0h	R/W	
D[11:9]	THRESMAP_SG1	0h	R/W	
D[8:6]	THRESMAP_SG0	0h	R/W	
D[5:3]	THRESMAP_SP9	0h	R/W	
D[2:0]	THRESMAP_SP8	0h	R/W	

REG30h: THRESMAP_CFG2 Register [Reset = 0h] (SGMCD1024DQ Only)

BITS	BIT NAME	RESET	TYPE	DESCRIPTION
D[23:21]	RESERVED	0h	R	Reserved.
D[20:18]	THRESMAP_VS1_THRES2B	0h	R/W	0h = THRES0 1h = THRES1 2h = THRES2 3h = THRES3 4h = THRES4 5h = THRES5 6h = THRES6 7h = THRES7
D[17:15]	THRESMAP_VS1_THRES2A	0h	R/W	
D[14:12]	THRESMAP_VS0_THRES2B	0h	R/W	
D[11:9]	THRESMAP_VS0_THRES2A	0h	R/W	
D[8:6]	THRESMAP_SG8_SG13_THRES3C	0h	R/W	
D[5:3]	THRESMAP_SG8_SG13_THRES3B	0h	R/W	
D[2:0]	THRESMAP_SG8_SG13_THRES3A	0h	R/W	

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REGISTER MAPS (continued)

REG31h: Matrix Register [Reset = 0h]

BITS	BIT NAME	RESET	TYPE	DESCRIPTION
D[23:17]	RESERVED	0h	R	Reserved.
SGMCD1024DQ				
D[16:15]	IN_COM_EN	0h	R/W	0h = No interrupt generation for w.r.t. threshold THRES_COM 1h = Interrupt generation on rising edge above threshold THRES_COM 2h = Interrupt generation on falling edge below threshold THRES_COM 3h = Interrupt generation on falling and rising edge of threshold THRES_COM
D[14:5]	THRES_COM	0h	R/W	10-bits value of threshold THRES_COM. Bit5: LSB Bit14: MSB
SGMCD1024AQ				
D[16:5]	RESERVED	0h	R/W	Reserved.
D[4:3]	MATRIX	0h	R/W	0h = No matrix, regular inputs only 1h = 4×4 matrix 2h = 5×5 matrix 3h = 6×6 matrix
D[2:0]	POLL_ACT_TIME_M	0h	R/W	Polling active time setting for the matrix inputs. 0h = 64μs 1h = 128μs 2h = 256μs 3h = 384μs 4h = 512μs 5h = 768μs 6h = 1024μs 7h = 1360μs

REG32h: Mode Register [Reset = 0h] (SGMCD1024DQ Only)

BITS	BIT NAME	RESET	TYPE	DESCRIPTION
D[23:10]	M_SG[13:0]	0h	R/W	0h = Comparator mode for SGx (x = 13 to 0) 1h = ADC mode for SGx (x = 13 to 0)
D[9:0]	M_SP[9:0]	0h	R/W	0h = Comparator mode for SPx (x = 9 to 0) 1h = ADC mode for SPx (x = 9 to 0)

REG33h: SSC_INT Register [Reset = 0h]

This register records the information of the switch status change (SSC) events as they occur on all channels. A READ command executed on this register clears its content and resets the register to its default value.

BITS	BIT NAME	RESET	TYPE	DESCRIPTION
D[23:0]	SSC_SGx[13:0]	0h	RC	0h = No SSC events occurred 1h = SSC events occurred
D[9:0]	SSC_SPx[9:0]	0h	RC	0h = No SSC events occurred 1h = SSC events occurred

REG34h: MTX_INT0 Register [Reset = 0h] (SGMCD1024AQ Only)

This register records the information of the switch status change (SSC) events as they occur on SG0-SG3 under matrix polling mode while SPx (x = 9 to 4) pulled to GND. A READ command executed on this register clears its content and resets the register to its default value.

BITS	BIT NAME	RESET	TYPE	DESCRIPTION
D[23:18]	INMAT_13_SP[9:4]	0h	RC	0h = No SSC events occurred at SG3 while SPx (x = 9 to 4) pulled to GND. 1h = SSC events occurred at SG3 while SPx (x = 9 to 4) pulled to GND.
D[17:12]	INMAT_12_SP[9:4]	0h	RC	0h = No SSC events occurred at SG2 while SPx (x = 9 to 4) pulled to GND. 1h = SSC events occurred at SG2 while SPx (x = 9 to 4) pulled to GND.
D[11:6]	INMAT_11_SP[9:4]	0h	RC	0h = No SSC events occurred at SG1 while SPx (x = 9 to 4) pulled to GND. 1h = SSC events occurred at SG1 while SPx (x = 9 to 4) pulled to GND.
D[5:0]	INMAT_10_SP[9:4]	0h	RC	0h = No SSC events occurred at SG0 while SPx (x = 9 to 4) pulled to GND. 1h = SSC events occurred at SG0 while SPx (x = 9 to 4) pulled to GND.

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REGISTER MAPS (continued)

REG35h: MTX_INT1 Register [Reset = 0h] (SGMCD1024AQ Only)

This register records the information of the switch status change (SSC) events as they occur on SG4-SG5 under matrix polling mode while SPx (x = 9 to 4) pulled to GND. A READ command executed on this register clears its content and resets the register to its default value.

BITS	BIT NAME	RESET	TYPE	DESCRIPTION
D[23:12]	RESERVED	0h	R	Reserved
D[11:6]	INMAT_15_SP[9:4]	0h	RC	0h = No SSC events occurred at SG5 while SPx (x = 9 to 4) pulled to GND. 1h = SSC events occurred at SG5 while SPx (x = 9 to 4) pulled to GND.
D[5:0]	INMAT_14_SP[9:4]	0h	RC	0h = No SSC events occurred at SG4 while SPx (x = 9 to 4) pulled to GND. 1h = SSC events occurred at SG4 while SPx (x = 9 to 4) pulled to GND.

Programming Guidelines

To ensure correct operation of the SGMCD1024xQ during configuration, follow the programming guidelines summarized in Table 12.

Table 12. SGMCD1024xQ Programming Guidelines

Category	Programming requirement
Threshold Setup: • Continuous Mode • Regular Polling Mode • Matrix Mode (Non-Matrix Inputs)	THRES2B ≥ THRES2A (for SG2 to SG7) THRES3C ≥ THRES3B ≥ THRES3A (for SG8 to SG12) THRES9 ≥ THRES8 ≥ THRES3C ≥ THRES3B ≥ THRES3A (for IN23)
Threshold Setup: V _{BATP} Measurement	VS0_THRES2B ≥ VS0_THRES2A VS1_THRES2B ≥ VS1_THRES2A
4×4 Matrix Mode (MATRIX[4:3] = 01)	POLL_EN = 1 IN_EN[7:4] = 1111; IN_EN[13:10] = 1111 MODE[7:4] = 0000; MODE[13:10] = 0000 CS_SELECT[7:4] = 1111; CS_SELECT[13:10] = 0000 I _{WETT(CSI)} > I _{WETT(CSO)} : • WC_CFG0[20:18] < WC_CFG0[8:6] • WC_CFG0[23:21] < WC_CFG0[11:9] • WC_CFG1[2:0] > WC_CFG0[14:12] If TW event is expected, CSO can only be set to 1mA or 2mA: • If WC_CFG0[8:6] = 001: WC_CFG0[20:18] = 010, 011, 100, 101, 110, or 111; If WC_CFG0[8:6] = 010: WC_CFG0[20:18] = 011 • If WC_CFG0[11:9] = 001: WC_CFG0[23:21] = 010, 011, 100, 101, 110, or 111; If WC_CFG0[11:9] = 010: WC_CFG0[23:21] = 011 • If WC_CFG1[2:0] = 001: WC_CFG0[14:12] = 010, 011, 100, 101, 110, or 111; If WC_CFG1[2:0] = 010: WC_CFG0[14:12] = 011
5×5 Matrix Mode (MATRIX[4:3] = 10)	POLL_EN = 1 IN_EN[8:4] = 1111; IN_EN[14:10] = 1111 MODE[8:4] = 0000; MODE[14:10] = 0000 CS_SELECT[8:4] = 1111; CS_SELECT[14:10] = 0000 I _{WETT(CSI)} > I _{WETT(CSO)} : • WC_CFG0[20:18] < WC_CFG0[8:6] • WC_CFG0[23:21] < WC_CFG0[11:9] • WC_CFG1[2:0] > WC_CFG0[14:12] • WC_CFG1[5:3] > WC_CFG0[17:15] If TW event is expected, CSO can only be set to 1mA or 2mA: • If WC_CFG0[8:6] = 001: WC_CFG0[20:18] = 010, 011, 100, 101, 110, or 111; If WC_CFG0[8:6] = 010: WC_CFG0[20:18] = 011 • If WC_CFG0[11:9] = 001: WC_CFG0[23:21] = 010, 011, 100, 101, 110, or 111; If WC_CFG0[11:9] = 010: WC_CFG0[23:21] = 011 • If WC_CFG1[2:0] = 001: WC_CFG0[14:12] = 010, 011, 100, 101, 110, or 111; If WC_CFG1[2:0] = 010: WC_CFG0[14:12] = 011 • If WC_CFG1[5:3] = 001: WC_CFG0[17:15] = 010, 011, 100, 101, 110, or 111; If WC_CFG1[5:3] = 010: WC_CFG0[17:15] = 011

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REGISTER MAPS (continued)

Category	Programming requirement
6×6 Matrix Mode (MATRIX[4:3] = 11)	POLL_EN = 1 IN_EN[9:4] = 111111; IN_EN[15:10] = 111111 MODE[9:4] = 000000; MODE[15:10] = 000000 CS_SELECT[9:4] = 111111; CS_SELECT[15:10] = 000000 $I_{WETT(CSI)} > I_{WETT(CSO)}$: - WC_CFG0[20:18] < WC_CFG0[8:6] - WC_CFG0[23:21] < WC_CFG0[11:9] - WC_CFG1[2:0] > WC_CFG0[14:12] - WC_CFG1[5:3] > WC_CFG0[17:15] If TW event is expected, CSO can only be set to 1mA or 2mA: - If WC_CFG0[8:6] = 001: WC_CFG0[20:18] = 010, 011, 100, 101, 110, or 111; If WC_CFG0[8:6] = 010: WC_CFG0[20:18] = 011 - If WC_CFG0[11:9] = 001: WC_CFG0[23:21] = 010, 011, 100, 101, 110, or 111; If WC_CFG0[11:9] = 010: WC_CFG0[23:21] = 011 - If WC_CFG1[2:0] = 001: WC_CFG0[14:12] = 010, 011, 100, 101, 110, or 111; If WC_CFG1[2:0] = 010: WC_CFG0[14:12] = 011 - If WC_CFG1[5:3] = 001: WC_CFG0[17:15] = 010, 011, 100, 101, 110, or 111; If WC_CFG1[5:3] = 010: WC_CFG0[17:15] = 011
Clean Current Polling (if CCP_SPx = 1 in the CCP_CFG1 register)	At least one input (standard or matrix) or the V_{BATP} measurement has to be enabled: IN_EN_x = 1 in the IN_EN register or CONFIG [17] = 1. ⁽¹⁾
Wetting Current Auto-Scaling (if WC_CFG1[22:21] != 11)	The wetting current auto-scaling feature is only activated in the continuous mode: POLL_EN = 0 ⁽²⁾ The wetting current auto-scaling only applies to 10mA or 15mA wetting currents: WC_INx bits = 100, 101, 110, or 111 in the WC_CFG0 and WC_CFG1 registers. ⁽²⁾
Wetting Current Diagnostic (If CONFIG[21:18] != 0000)	At least one channel has to be enabled from SP0 to SP3 (IN_EN[3:0] != 4b'0000) and corresponding channel wetting current has to be enabled from CS_SELECT[3:0] != 4b'0000 Inputs SP0 to SP3 need to be configured to ADC input mode: MODE[3:0] = 1111 Inputs SP0 and SP1 need to be configured to CSO: CS_SELECT [1:0] = 00 Inputs SP2 and SP3 need to be configured to CSI: CS_SELECT [3:2] = 11
Continuous Mode Standard Polling Mode	t_{POLL_TIME} and $t_{POLL_ACT_TIME}$ settings have to meet the below requirement: $t_{POLL_TIME} \geq 1.3 \times [t_{POLL_ACT_TIME} + n \times 24\mu s + 10\mu s]$ ^{(3) (4)} - n: the number of enabled channels configured in register IN_EN t_{POLL_TIME}: timing setting configured in CONFIG[4:1] $t_{POLL_ACT_TIME}$: timing setting configured in CONFIG[8:5]
Matrix Polling Mode	t_{POLL_TIME}, $t_{POLL_ACT_TIME}$ and $t_{POLL_ACT_TIME_M}$ settings have to meet the below requirement: $t_{POLL_TIME} > 1.3 \times [m \times t_{POLL_ACT_TIME_M} + t_{POLL_ACT_TIME} + n \times 24\mu s + 10\mu s]$ ^{(3) (4)} n: the number of enabled channels configured in register IN_EN - m: 16 for 4 × 4 matrix; 25 for 5 × 5 matrix; 36 for 6 × 6 matrix t_{POLL_TIME}: timing setting configured in CONFIG[4:1] $t_{POLL_ACT_TIME_M}$: timing setting configured in MATRIX[2:0] $t_{POLL_ACT_TIME}$: timing setting configured in CONFIG[8:5]

NOTES:

1. This is a soft requirement for the clean current polling feature. The feature is inactive if this requirement is not met.
2. These are soft requirements for the wetting current auto-scaling feature. The feature is inactive if these requirements are not met.
3. If Wetting Current Diagnostic (WCD) is enabled, add additional 96μs.
4. If CCP is enabled, add $t_{CCP_TRAN} + t_{CCP_TIME}$, where t_{CCP_TIME} is the timing setting configured in CCP_CFG0[6:4].

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APPLICATION INFORMATION

As a high-performance 24-channel Multiple Switch Detection Interface (MSDI), the SGMCD1024xQ serves as the bridge between external mechanical switches and a low-voltage MCU within 12V automotive applications. Its rich proprietary functions enable substitution for discrete hardware solutions, resulting in reduced board footprint and lower bill of materials (BOM) cost. Configurable low-power polling mode further delivers considerable system power-saving benefits.

Resistor-Coded Switches Detection in Automotive Body Control Module

The Body Control Module (BCM) is an ECU that oversees monitoring and control of a wide range of vehicle body electronic accessories. A major responsibility of the BCM is reading the states of vehicle mechanical switches. Apart from standard digital on-off switches, an automotive BCM can adopt resistor-coded switches with higher complexity.

Resistor-coded switches can represent more than two separate states and are widely used in wiper, light and turn signal control stalks. Each position of this switch

generates a unique voltage potential and an ADC (usually built into the MCU) measures these voltages to resolve switch positions. The SGMCD1024DQ integrates a 10-bit ADC and configurable thresholds, enabling direct monitoring of resistor-coded switches. The application diagram below shows how the SGMCD1024xQ is deployed in a BCM to detect external mechanical resistor-coded switches, with detailed design examples covered in later sections.

Design Requirements

Figure 31 illustrates a 3-state resistor-coded switch application scenario, and Table 13 lists its comprehensive technical parameters. This design scheme relies on the built-in ADC module of the SGMCD1024xQ to identify and differentiate three working states of the switch:

1. State 1: SW1 and SW2 are both in the open state.
2. State 2: SW1 is open while SW2 is closed.
3. State 3: SW1 is closed while SW2 is open.

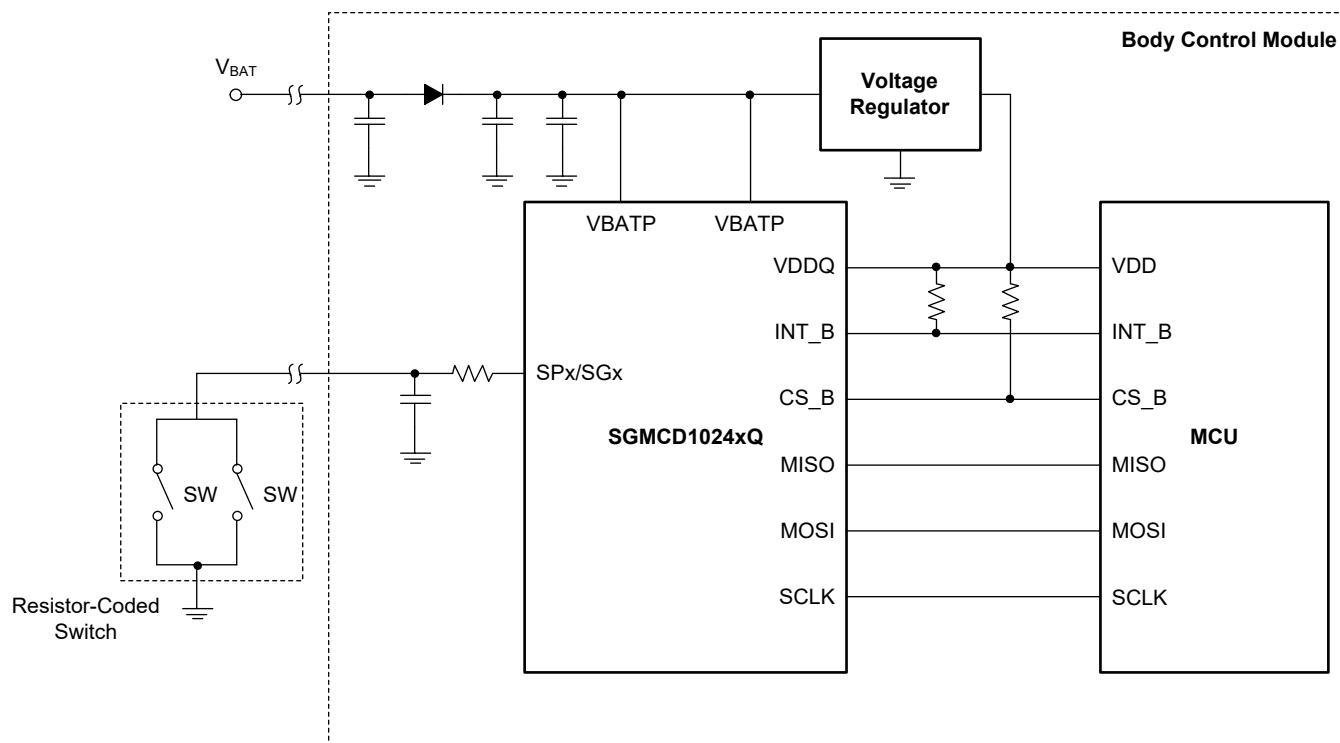


Figure 30. Using SGMCD1024xQ to Monitor a Resistor-Coded Switch in Body Control Module Application

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APPLICATION INFORMATION (continued)

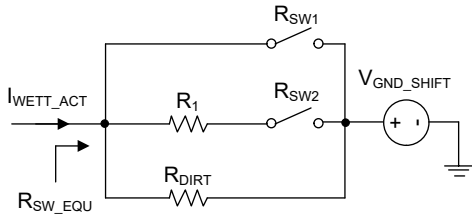


Figure 31. Example 3-State Resistor-Coded Switch

In order to replicate the actual operating environment of automotive systems, the battery voltage fluctuates in the range of 9V to 16V. The R_{DIRT} component is used to simulate the subtle leakage current of switches under open-circuit conditions. Meanwhile, the system supports a $\pm 1V$ ground offset, namely a potential deviation of up to $\pm 1V$ may exist between the switch reference point and the device ground reference. Whenever the switch position changes and the working state switches, the SGMCD1024xQ can effectively detect the state transition and output an INT_B interrupt signal to inform or wake up the MCU. The device stores switch state data in status registers for MCU query and acquisition.

Table 13. Example Resistor-Coded Switch Specification

SYMBOL	SPECIFICATION	MIN	MAX
V_{BAT}	$9V \leq V_{BAT} \leq 16V$	9V	16V
R_1	$680\Omega \pm 1\%$	673.2Ω	686.8Ω
R_{SW1}	50 Ω Max when closed	0 Ω	50 Ω
R_{SW2}	50 Ω Max when closed	0 Ω	50 Ω
R_{DIRT}	5000 Ω Min	5000 Ω	∞
V_{GND_SHIFT}	$\pm 1V$	-1V	+1V

Detailed Design Procedure

Follow the steps below to compute the threshold values that will be programmed into the SGMCD1024xQ to ensure correct switch detection.

Table 14. Detailed Design Procedure

	STEP 1		STEP 2		STEP 3		STEP 4		STEP 5
	Equivalent Resistance Value (Ω)		$V_{SPX/SGX}$ (V)		$V_{SPX/SGX} + V_{GND_SHIFT}$ (V)		ADC Code Spread		Threshold
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
State 1: Both SW1 and SW2 Open	5000	∞	> 6V	—	> 6V	—	1023	—	
State 2: SW1 Open and SW2 Closed	593.32	763.79	2.61	4.05	1.61	5.05	274	861	942
State 3: SW1 Closed and SW2 Open	0	50	0	0.275	0	1.275	0	217	246

1. Compute the equivalent resistance for each switch state, including the effects of R_{DIRT} and 1% resistor variation.

2. Calculate the voltage generated by wetting current across the switch with the equation $V_{SPX/SGX} = R_{SW_EQU} \times I_{WETT_ACT}$. R_{SW_EQU} is the equivalent switch resistance and I_{WETT_ACT} is the real wetting current through the switch. This design selects 5mA wetting current to make optimal use of the ADC input range from 0V to 6V. Wetting current changes with manufacturing process deviation and temperature, and these factors cannot be ignored. According to the SGMCD1024xQ electrical table and with adequate operating headroom for the CSO current source, the 5mA setting outputs current from 4.4mA to 5.5mA under the condition $V_{BATP} - V_{SPX/SGX} \geq 3V$. This value can be used to find the input pin voltage $V_{SPX/SGX}$ of the SGMCD1024xQ.

3. Include ground shift error in the calculation. As described in the Design Requirements section, ground shift can be $\pm 1V$. This means the voltage sampled by the SGMCD1024xQ may shift up to $\pm 1V$.

4. Convert $V_{SPX/SGX}$ into ADC raw codes. The integrated 10-bit ADC has a full scale of 0V to 6V, where 6V corresponds to the maximum code 1023. Based on this relation, calculate the ADC code interval for each of the three switch states.

5. After finishing the ADC code range calculation for all switch states, place each detection threshold at the midpoint between the upper code boundary of one state and the lower code boundary of the neighboring state to achieve the best detection margin.

24-Channel Multiple Switch Detection Interface with SGMCD1024xQ Adjustable Wetting Current for Automotive Applications

APPLICATION INFORMATION (continued)

Power Supply Recommendations

Two power-supply inputs, VBATP and VDDQ, are available on the SGMCD1024xQ. All core device functions rely on VBATP, which should connect to a 12V car battery (16V, MAX) through a reverse-protection diode. The VDDQ rail sets SPI interface logic levels, delivers drive current to the MISO driver, and provides pull-up voltage for CS_B. As an alternative to VBATP, VDDQ can supply external pull-up for the INT_B pin and requires a 3V-to-5.5V source. If the VDDQ power is removed, the SPI functionality becomes inactive, but the device continues its regular operational behavior with register data stored.

Proper PCB decoupling capacitors are advised to stabilize both supply inputs. Figure 32 presents a typical board-level power supply decoupling example. A large-value C_{BUFF} capacitor decouples VBATP on the Electronic Control Unit (ECU) board, and a diode safeguards internal circuits from reverse battery damage. To achieve superior decoupling, C_{VBATP} should be placed physically near the SGMCD1024xQ. A voltage regulator delivers regulated power for the device digital circuits and the nearby MCU, with its output filtered by $C_{DECOUPLE}$. Table 15 enumerates the recommended capacitance values corresponding to each capacitor in the system diagram.

Table 15. Decoupling Capacitor Recommendations

CRC Rule	Value
C_{BUFF}	100 μ F, 50V rated, $\pm 20\%$
C_{VBAT}	100nF, 50V rated, $\pm 10\%$; X7R
C_{VBATP}	100nF, 50V rated
$C_{DECOUPLE}$	100nF ~ 1 μ F

Layout

Layout Guidelines

The main layout design considerations of the SGMCD1024xQ are listed below.

1. Apply decoupling capacitors to the VBATP and VDDQ pins. Select capacitor values according to the Power Supply Recommendations section, and mount each capacitor in close physical proximity to its associated pin. The voltage rating of every capacitor must be sufficient to withstand the operating voltage present on the VBATP and VDDQ supply rails.
2. Keep the input lines as short as possible.
3. Implement a solid ground plane layer. This aids heat spreading and reduces susceptibility to electromagnetic interference (EMI) noise.
4. Sensitive analog traces shall not be routed in parallel with digital traces. Minimize intersections between analog and digital signal paths. If trace crossing cannot be avoided, route traces perpendicularly to one another.
5. The exposed thermal pad under the component shall be soldered onto the board and filled with thermal vias tied to the ground planes to obtain satisfactory thermal performance. On basic double-sided PCBs lacking internal layers, heat can be dissipated via surface layers. Multilayer PCBs leverage internal ground planes to evacuate heat.
6. Keep the parasitic inductance as low as possible for the path connecting the SPx/SGx input capacitors to the thermal pad ground return.

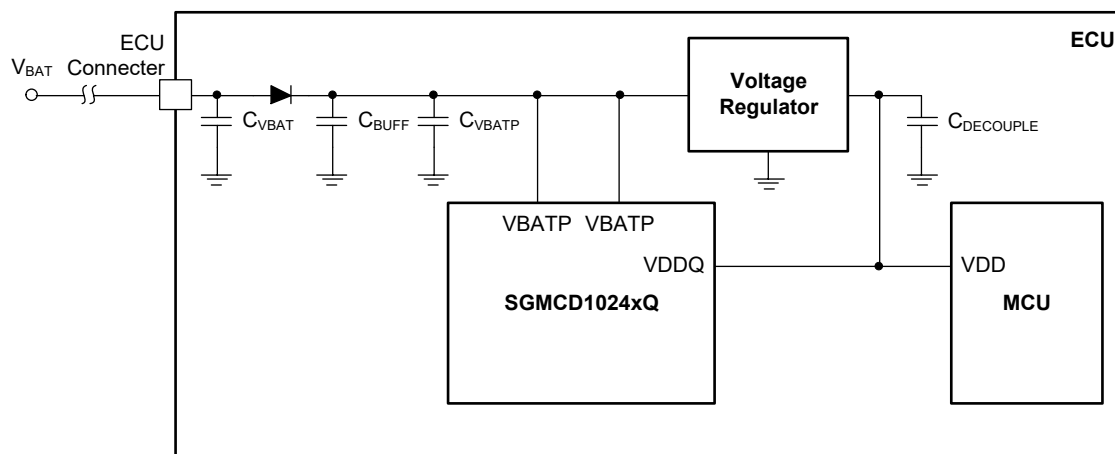


Figure 32. Recommended Power Supply Decoupling

APPLICATION INFORMATION (continued)

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24-Channel Multiple Switch Detection Interface with SGMCD1024xQ Adjustable Wetting Current for Automotive Applications

APPLICATION INFORMATION (continued)

Bill of Materials

Table 16. Bill of Materials

Item	Quantity	Reference	Value	Description
1	2	C ₁ , C ₃	100nF	CAP CER 100nF 100V 10% X7R 0603
2	1	C ₂	100μF	CAP CER 100μF 50V 20% 0603
3	27	C ₄ , C ₅ ~ C ₂₈ , C ₅₇ , C ₅₈	0.1μF	CAP CER 0.1μF 100V 10% X7R 0603
4	24	C ₂₉ ~ C ₅₂	0.1μF	CAP CER 0.1μF 100V 10% X7R 0603 (optional)
5	4	C ₅₃ ~ C ₅₆	10pF	CAP CER 10pF 100V 10% X7R 0603
6	1	C ₅₉	1μF	CAP CER 1μF 50V 10% X7R 0603
7	1	D ₁	—	DIODE RECT 3.0A 50V AEC-Q101 SMB
8	1	R ₁	10kΩ	RES MF 10kΩ 0.1W 5% 0603 (optional)
9	24	R ₂ ~ R ₂₅	100Ω	RES MF 100Ω 0.5W 1% 0805
10	3	R ₂₆ , R ₂₉ , R ₃₀	100Ω	RES MF 100Ω 0.1W 1% 0603
11	1	R ₂₇	100Ω	RES MF 100Ω 0.1W 1% 0603 (optional)
12	1	R ₂₈	10kΩ	RES MF 10kΩ 0.1W 5% 0603
13	1	U ₁	SGMCD1024xQ	IC Multiple Detection Switch Interface, TSSOP-38 (Exposed Pad)

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

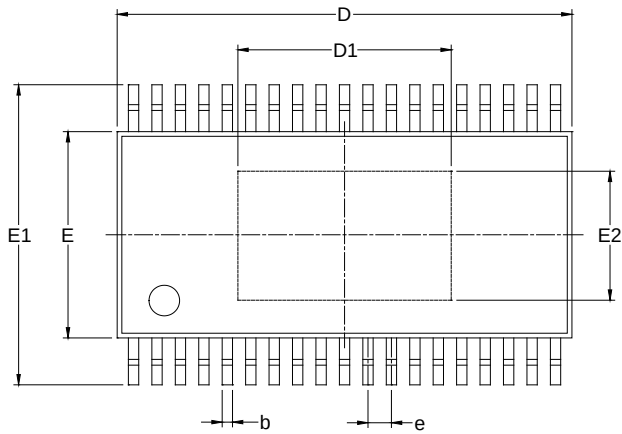
Changes from Original to REV.A (SEPTEMBER 2026)

Page

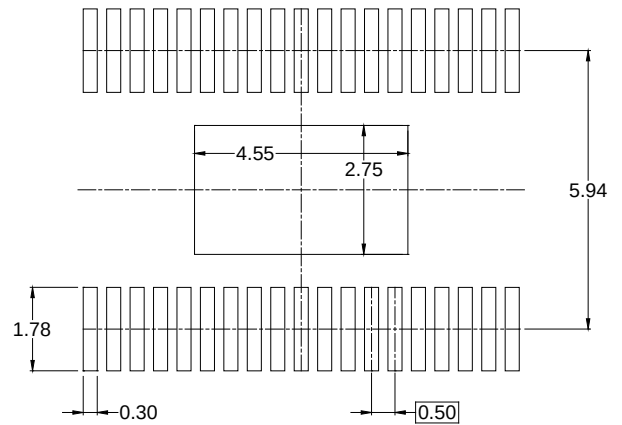
Changed from product preview to production data.....All

PACKAGE OUTLINE DIMENSIONS

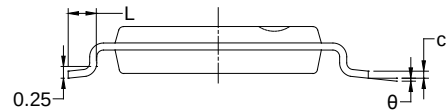
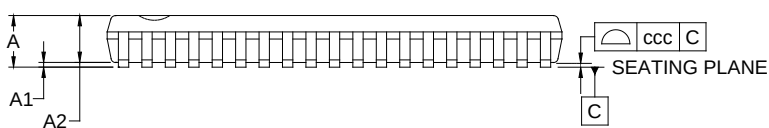
TSSOP-38 (Exposed Pad)



TOP VIEW



RECOMMENDED LAND PATTERN (Unit: mm)



Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	-	-	1.200
A1	0.000	-	0.150
A2	0.800	-	1.050
b	0.170	-	0.270
c	0.090	-	0.200
D	9.600	-	9.800
D1	4.350	-	4.750
E	4.300	-	4.500
E1	6.200	-	6.600
E2	2.550	-	2.950
e	0.500 BSC		
L	0.450	-	0.750
θ	0°	-	8°
ccc	0.100		

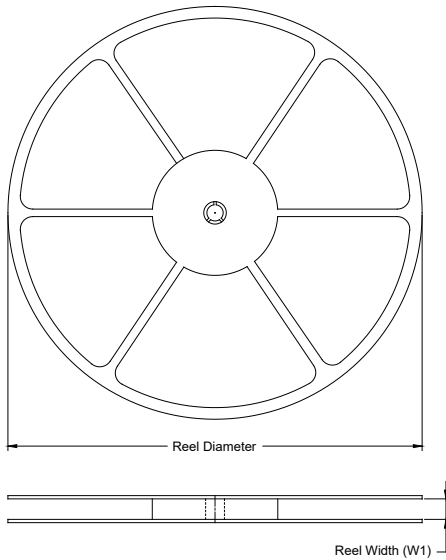
NOTES:

1. This drawing is subject to change without notice.
2. The dimensions do not include mold flashes, protrusions, or gate burrs.
3. Reference JEDEC MO-153.

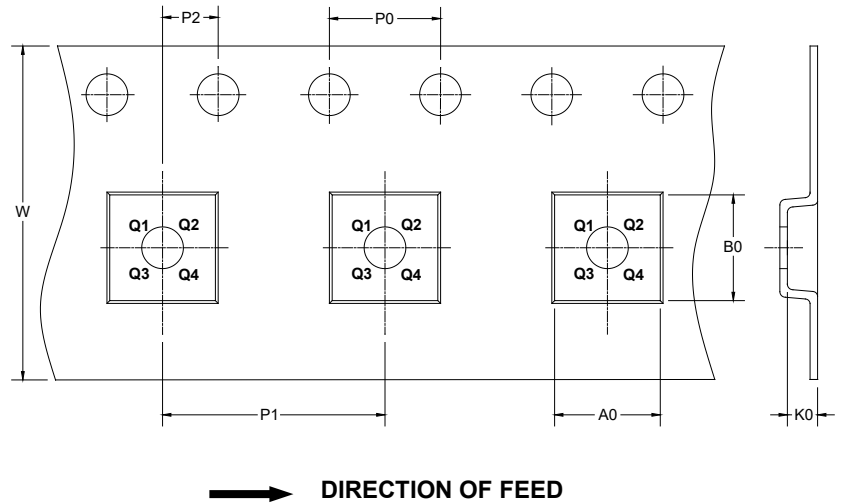
PACKAGE INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

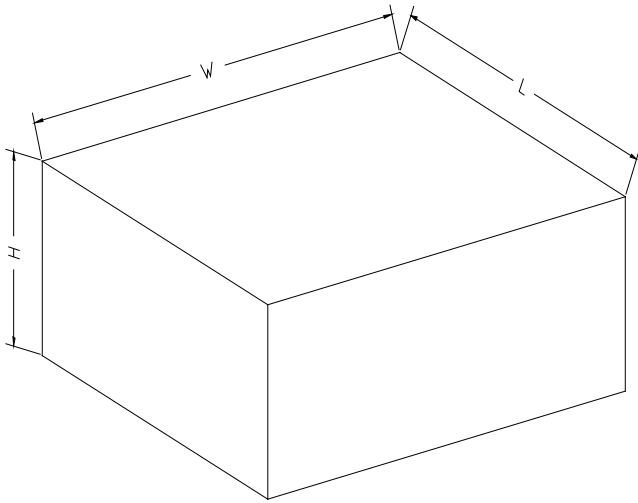
KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TSSOP-38 (Exposed Pad)	13"	16.4	6.80	10.25	1.60	4.0	8.0	2.0	16.0	Q1

DD00001

PACKAGE INFORMATION

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13"	386	280	370	5

DD0002