SGM7302C
6.8GHz, 2:1 (SPDT) 10-Channel MIPI Switch with 1.2V Logic Support

GENERAL DESCRIPTION

The SGM7302C is an optimized differential 5-channel (single-ended 10-channel) single-pole, double-throw (SPDT) dual directional high-speed switch. The product attribute determines that it is suitable for multiple MIPI compliant devices to connect to a single CSI/DSI, C-PHY/D-PHY module. The device also supports SATA, SAS, MIPI DSI/CSI, LVDS, RGMII, DDR and Ethernet interfaces.

The main features of product are 6.8GHz bandwidth, low skew between channels with little signal degradation, and great layout loss compensation. Its low current consumption meets the needs of low power applications, including mobile phones and other personal electronics.

The SGM7302C is available in a Green FOCSP-2.43×2.43-36B package.

FEATURES

- **Supply Voltage Range: 1.5V to 5.5V**
- **Low R_{ON}: 5.2Ω (TYP)**
- **High Bandwidth: 6.8GHz**
- **Ultra Low Crosstalk: -55dB**
- **Low Power Disable Mode**
- **1.2V Logic Compatible**
- **Bidirectional Signal Path**
- **Available in a Green FOCSP-2.43×2.43-36B Package**

APPLICATIONS

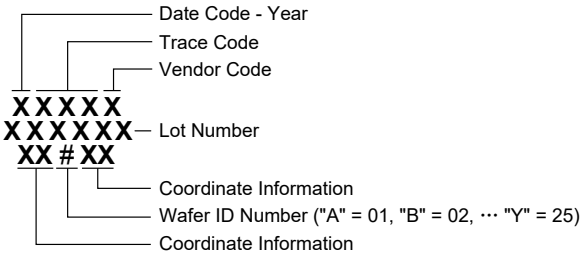
Smart Phone
Tablet PC
Notebook PC
AI Equipment
Medical Equipment

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM7302C	FOCSP-2.43×2.43-36B	-40℃ to +85℃	SGM7302CYG/TR	2C5 XXXXX XXXXXX XX#XX	Tape and Reel, 3000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code. XXXXXX = Lot Number. XX#XX = Coordinate Information and Wafer ID Number.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage Range, V_{DD} ..... -0.5V to 5.8V
Switch Signal Voltage (Differential Input/Output), V_{SW} .....
..... -0.5V to 3.3V
V_{SEL}, V_{nOE} ..... -0.5V to 5.8V
Junction Temperature .....+150℃
Storage Temperature Range .....-65℃ to +150℃
Lead Temperature (Soldering, 10s) .....+260℃
ESD Susceptibility (1) (2)
HBM.....±2500V
CDM .....±2000V

NOTES:

1. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.

2. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

RECOMMENDED OPERATING CONDITIONS

Operating Temperature Range, T_A.....-40℃ to +85℃
Supply Voltage Range, V_{DD} .....1.5V to 5.5V
Switch Signal Voltage (Differential Input/Output), V_{SW} .....
.....0V to 1.3V
V_{SEL}, V_{nOE}.....0V to 5.5V

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

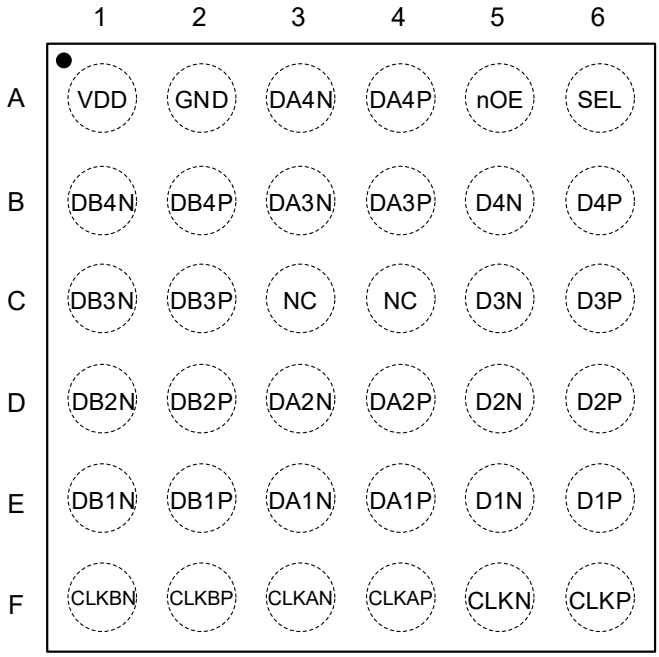
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

(TOP VIEW)



FOCSP-2.43×2.43-36B

PIN DESCRIPTION

PIN	NAME	I/O	FUNCTION	PIN	NAME	I/O	FUNCTION
F3	CLKAN	I/O	Differential Input/Output.	B3	DA3N	I/O	Differential Input/Output.
F4	CLKAP	I/O	Differential Input/Output.	B4	DA3P	I/O	Differential Input/Output.
F1	CLKBN	I/O	Differential Input/Output.	A3	DA4N	I/O	Differential Input/Output.
F2	CLKBP	I/O	Differential Input/Output.	A4	DA4P	I/O	Differential Input/Output.
F5	CLKN	I/O	Differential Input/Output.	E1	DB1N	I/O	Differential Input/Output.
F6	CLKP	I/O	Differential Input/Output.	E2	DB1P	I/O	Differential Input/Output.
E5	D1N	I/O	Differential Input/Output.	D1	DB2N	I/O	Differential Input/Output.
E6	D1P	I/O	Differential Input/Output.	D2	DB2P	I/O	Differential Input/Output.
D5	D2N	I/O	Differential Input/Output.	C1	DB3N	I/O	Differential Input/Output.
D6	D2P	I/O	Differential Input/Output.	C2	DB3P	I/O	Differential Input/Output.
C5	D3N	I/O	Differential Input/Output.	B1	DB4N	I/O	Differential Input/Output.
C6	D3P	I/O	Differential Input/Output.	B2	DB4P	I/O	Differential Input/Output.
B5	D4N	I/O	Differential Input/Output.	A2	GND	G	Ground.
B6	D4P	I/O	Differential Input/Output.	C3, C4	NC	-	No Connection.
E3	DA1N	I/O	Differential Input/Output.	A5	nOE	I	Output Enable (Active Low), Has Internal Pull-Down Resistor.
E4	DA1P	I/O	Differential Input/Output.	A6	SEL	I	Channel Select.
D3	DA2N	I/O	Differential Input/Output.	A1	VDD	P	Power Supply Voltage.
D4	DA2P	I/O	Differential Input/Output.				

NOTE: I = input, O = output, G = ground, P = power.

FUNCTIONAL BLOCK DIAGRAM

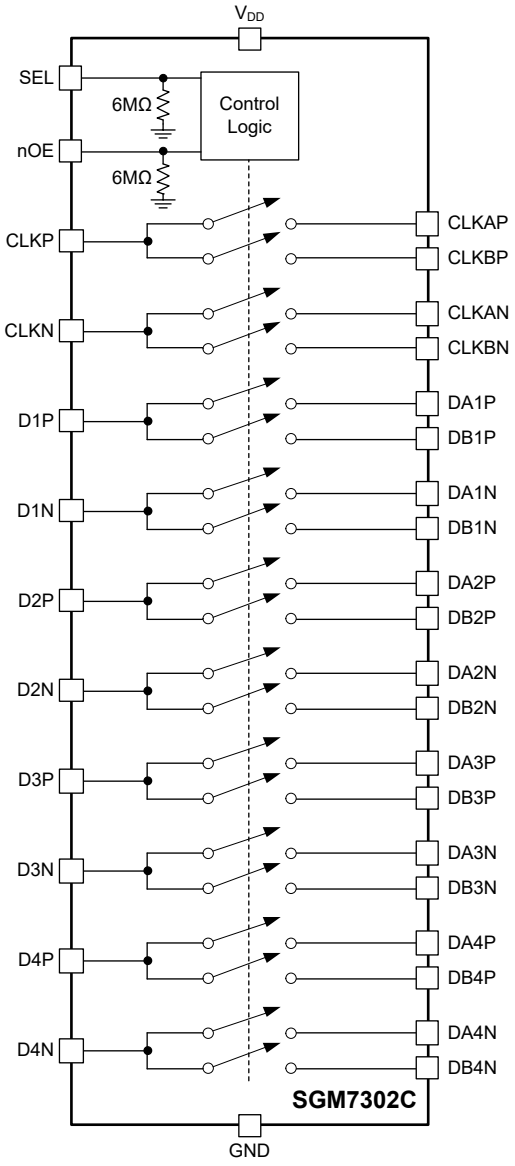


Figure 1. Block Diagram

FUNCTION TABLE

nOE	SEL	FUNCTION
H	X	Input/Output Pins High-Impedance
L	L	Differential Input CLKX = Differential Output CLKAX
		Differential Input DXX = Differential Output DAXX
L	H	Differential Input CLKX = Differential Output CLKBX
		Differential Input DXX = Differential Output DBXX

NOTE: X = Don’t care.

ELECTRICAL CHARACTERISTICS

(T_A = +25℃, V_{DD} = 1.5V to 5.5V, typical values are at V_{DD} = 1.8V, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Device Parameters							
Input Voltage (High)	V_{IH}	SEL, nOE		1		5.5	V
Input Voltage (Low)	V_{IL}	SEL, nOE		0		0.4	V
Input Leakage Current (High)	I_{LK_H}	SEL, nOE		-1		5	μA
Input Leakage Current (Low)	I_{LK_L}	SEL, nOE		-1		5	μA
Pull-Down Resistance	R_{PD}	SEL, nOE			6		MΩ
Digital Input Capacitance	C_I	V_{SEL} = 0V, 1.8V or V_{DD}, f = 1MHz			5		pF
Power Supply							
Supply Current (Normal)	I_{VDD}	V_{DD} = 1.5V to 5.5V, V_{nOE} = 0V, V_{SEL} = 0V or 5.5V Differential port input = 0V			50	85	μA
Supply Current (Power-Down)	I_{DD_PD}	V_{DD} = 1.5V to 5.5V, V_{nOE} = V_{DD}, V_{SEL} = 0V or 5.5V Differential port input = 0V				3	μA
DC Characteristics							
Resistance-On (High Speed)	R_{ON}	V_{nOE} = 0V, V_{SEL} = 0V or V_{DD} Differential port input = 0.2V Differential port output = -8mA, Test Circuit 1	V_{DD} = 1.8V to 5.5V		3.5	5.2	Ω
			V_{DD} = 1.5V		3.8	5.5	
Resistance-On (Low Power)	R_{ON}	V_{nOE} = 0V, V_{SEL} = 0V or V_{DD} Differential port input = 1.3V Differential port output = -8mA, Test Circuit 1	V_{DD} = 1.8V to 5.5V		4.2	6.2	Ω
			V_{DD} = 1.5V		5.2	7.5	
Resistance-On Flatness (High Speed)	R_{FLAT_ON}	V_{nOE} = 0V, V_{SEL} = 0V or V_{DD} Differential port input = 0V to 0.2V Differential port output = -8mA, Test Circuit 1	V_{DD} = 1.8V to 5.5V		0.1		Ω
			V_{DD} = 1.5V		0.2		
Resistance-On Flatness (Low Power)	R_{FLAT_ON}	V_{nOE} = 0V, V_{SEL} = 0V or V_{DD} Differential port input = 0V to 1.3V Differential port output = -8mA, Test Circuit 1	V_{DD} = 1.8V to 5.5V		0.8		Ω
			V_{DD} = 1.5V		1.6		
Resistance-On Match between Pairs of the Same Channel (High Speed)	ΔR_{ON}	V_{DD} = 1.5V to 5.5V, V_{nOE} = 0V, V_{SEL} = 0V or V_{DD} Differential port input = 0.2V, Differential port output = -8mA, Test Circuit 1			0.1		Ω
Resistance-On Match between Pairs of the Same Channel (Low Power)	ΔR_{ON}	V_{DD} = 1.5V to 5.5V, V_{nOE} = 0V, V_{SEL} = 0V or V_{DD} Differential port input = 1.3V, Differential port output = -8mA, Test Circuit 1			0.1		Ω
Leakage Current (Switch Off)	I_{OFF}	V_{DD} = 0V to 5.5V, V_{nOE} and V_{SEL} = 0V or 5.5V Differential port input = 0V to 3.0V Differential port output = 0V to 3.0V, Test Circuit 2		-1		1	μA
Leakage Current (Switch On)	I_{ON}	V_{DD} = 1.5V to 5.5V, V_{nOE} = 0V, V_{SEL} = 0V or 5.5V Differential port input = 0V to 3.0V Differential port output = NC, Test Circuit 3		-2		2	μA

ELECTRICAL CHARACTERISTICS (continued)

(T_A = +25℃, V_{DD} = 1.5V to 5.5V, typical values are at V_{DD} = 1.8V, unless otherwise noted.)

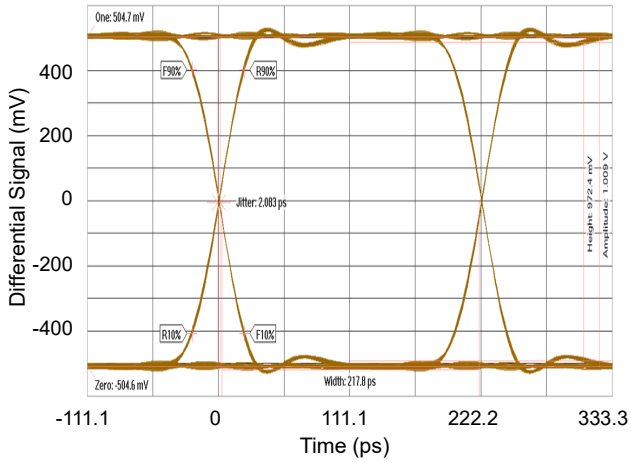
PARAMETER	SYMBOL	CONDITIONS	MIN (1)	TYP	MAX (1)	UNITS
Dynamic Characteristics						
Switching Time (SEL to Output)	t_{SW}	V_{DD} = 1.5V to 5.5V, V_{nOE} = 0V Differential port input = 1.2V Differential port output: R_L = 50Ω, C_L = 15pF, Test Circuit 4			1.5	μs
Turn-On Time (nOE to Output)	t_{ON_nOE}	V_{DD} = 1.5V to 5.5V Differential port input = 1.2V Differential port output: R_L = 50Ω, C_L = 15pF, Test Circuit 5			20	μs
Turn-Off Time (nOE to Output)	t_{OFF_nOE}	V_{DD} = 1.5V to 5.5V Differential port input = 1.2V Differential port output: R_L = 50Ω, C_L = 15pF, Test Circuit 5			1	μs
Maximum Toggling Frequency (SEL Line)	f_{SEL_MAX}	V_{DD} = 1.5V to 5.5V Differential port input = 1.2V Differential port output: R_L = 50Ω, C_L = 2pF			100	kHz
Turn-On Time (VDD to Output)	t_{ON_VDD}	V_{DD} from 0V to 5.5V, V_{DD} ramp rate = 2μs Differential port input = 1.2V Differential port output: R_L = 50Ω, C_L = 15pF			20	μs
Turn-Off Time (VDD to Output)	t_{OFF_VDD}	V_{DD} from 5.5V to 0V Differential port input = 1.2V Differential port output: R_L = 50Ω, C_L = 15pF			4.5	ms
Minimum Pulse Width (nOE)	t_{MIN_nOE}	V_{DD} = 1.5V to 5.5V Differential port input = 1.2V Differential port output: R_L = 50Ω, C_L = 2pF	500			ns
Break-Before-Make Time Delay	t_{BBM}	V_{DD} = 1.5V to 5.5V, V_{nOE} = 0V Differential port: R_L = 50Ω, C_L = 15pF, V_{SW} = 0.6V, Test Circuit 6	50			ns
Intra-Pair Output Skew (Bit to Bit)	t_{SKEW_INTRA}	V_{DD} = 1.5V to 5.5V, V_{nOE} = 0V Differential port input = 0.3V Differential port output: R_L = 50Ω, C_L = 5pF, Test Circuit 7, Test Circuit 8		1 (1)		ps
Inter-Pair Output Skew (CH to CH)	t_{SKEW_INTER}	V_{DD} = 1.5V to 5.5V, V_{nOE} = 0V Differential port input = 0.3V Differential port output: R_L = 50Ω, C_L = 5pF, Test Circuit 7, Test Circuit 9		4 (1)		ps
Switch Propagation Delay	t_{PD}	V_{DD} = 1.5V to 5.5V, V_{nOE} = 0V Differential port input = 1.2V Differential port output: R_L = 50Ω, C_L = 5pF, t_{RISE} = 100ps, Test Circuit 7, Test Circuit 10		40 (1)		ps
Differential Isolation	ISO	V_{DD} = 1.5V to 5.5V, V_{nOE} and V_{SEL} = 0V or V_{DD} Differential port: R_S = 50Ω, R_L = 50Ω, C_L = 5pF V_{SW} = 200mVpp (differential), f = 1250MHz, Test Circuit 11		-35		dB
Differential Crosstalk (CH to CH)	X_{TALK}	V_{DD} = 1.5V to 5.5V, V_{nOE} and V_{SEL} = 0V or V_{DD} Differential port: R_S = 50Ω, R_L = 50Ω, C_L = 5pF V_{SW} = 200mVpp (differential), f = 1250MHz, Test Circuit 12		-55		dB
Differential Bandwidth	BW	V_{DD} = 1.5V to 5.5V, V_{nOE} = 0V, V_{SEL} = 0V or V_{DD} Differential port: V_{SW} = 200mVpp (differential), Test Circuit 13		6.8		GHz
Insertion Loss	IL	V_{DD} = 1.5V to 5.5V, V_{nOE} = 0V, V_{SEL} = 0V or V_{DD} Differential port: R_S = 50Ω, R_L = 50Ω, C_L = 5pF V_{SW} = 200mVpp (differential), f = 100MHz		-0.35		dB
Capacitance-Off	C_{OFF}	V_{DD} = 1.5V to 5.5V, V_{nOE} and V_{SEL} = 0V or V_{DD} Differential port: 0V, 0.2V, f = 1250MHz		1.5		pF
Capacitance-On	C_{ON}	V_{DD} = 1.5V to 5.5V, V_{nOE} = 0V, V_{SEL} = 0V or V_{DD} Differential port: 0V, 0.2V, f = 1250MHz		1.5		pF

NOTE:

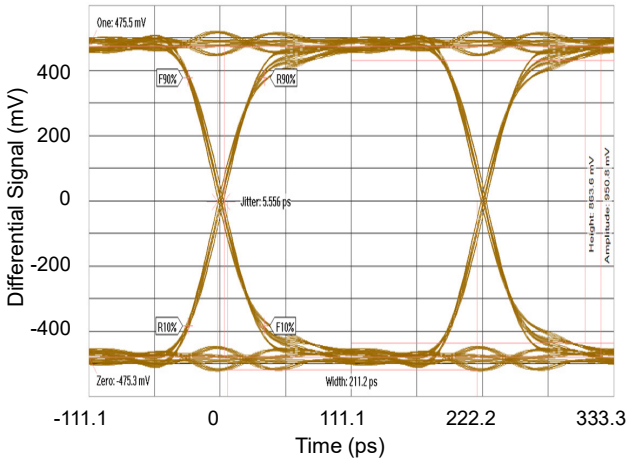
1. Guaranteed by design, not tested in production.

TYPICAL PERFORMANCE CHARACTERISTICS

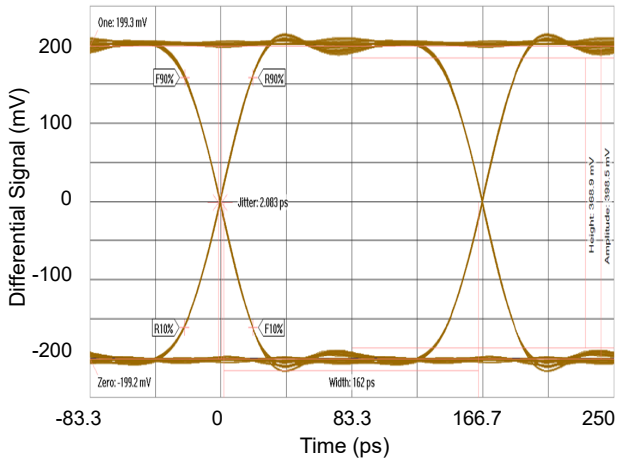
4.5Gbps ($500mV_{PP}$), Before Switch



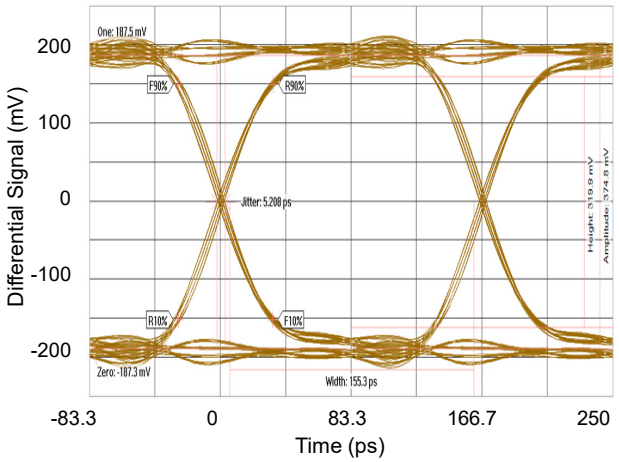
4.5Gbps ($500mV_{PP}$), After Switch



6Gbps ($200mV_{PP}$), Before Switch

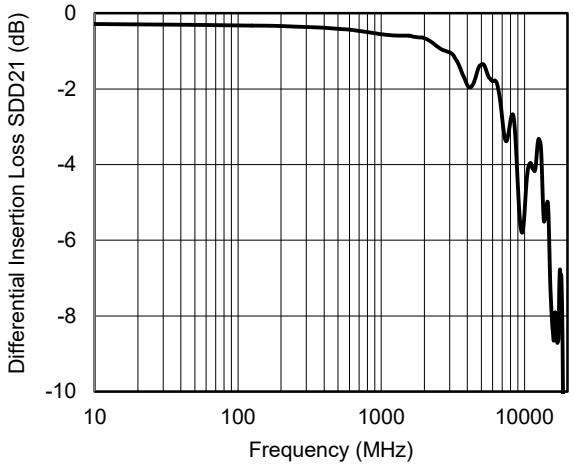


6Gbps ($200mV_{PP}$), After Switch

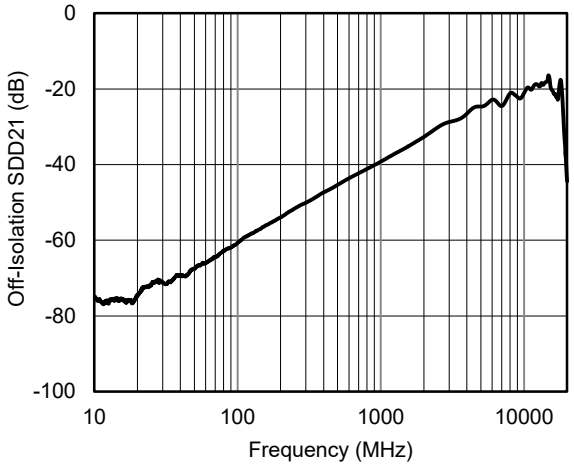


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

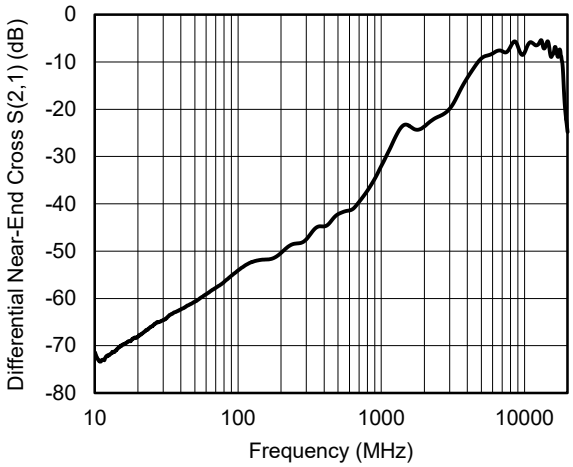
Differential Insertion Loss



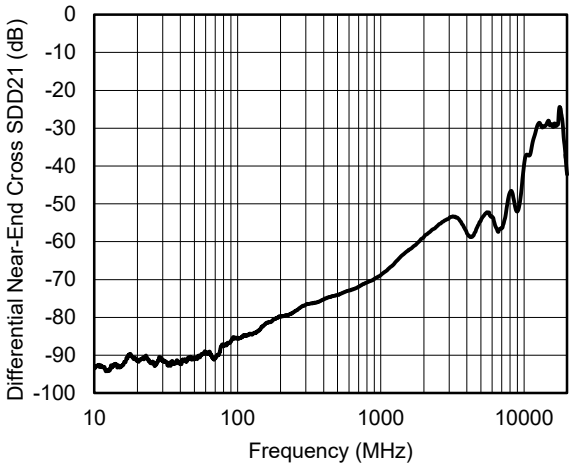
Off-Isolation



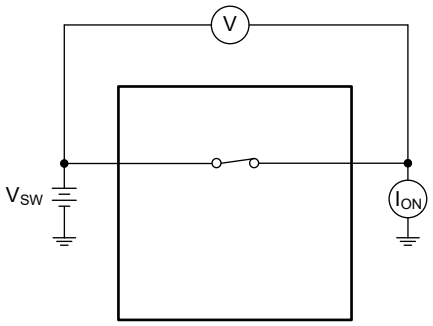
Intra-Pair Crosstalk



Inter-Pair Crosstalk

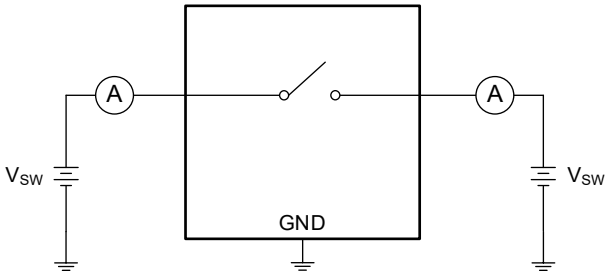


TEST CIRCUITS

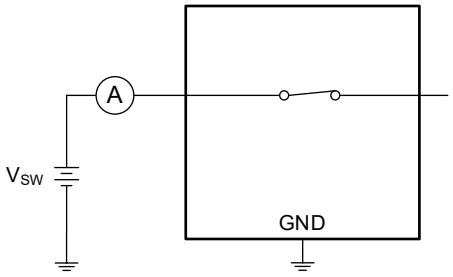


$R_{ON} = V1/I_{ON}$

Test Circuit 1. On-Resistance

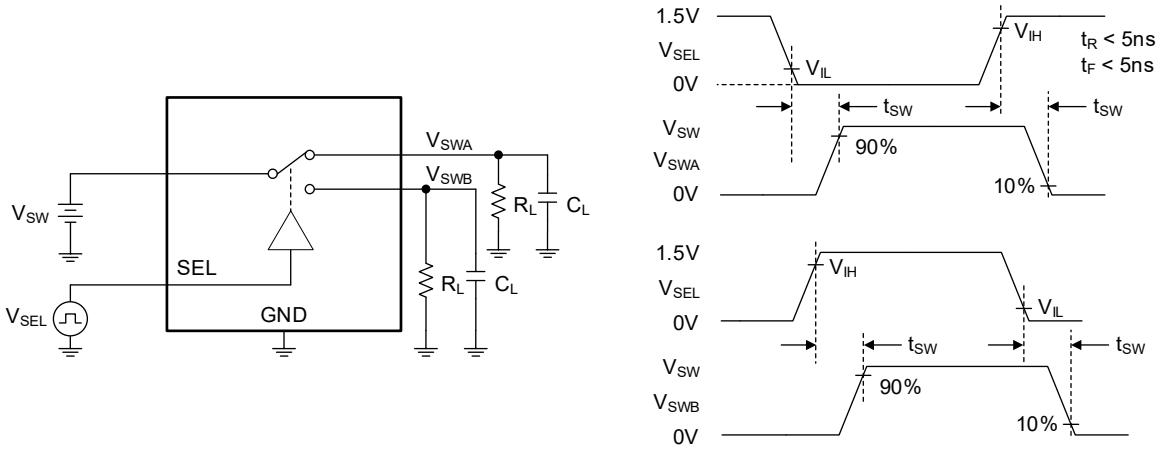


Test Circuit 2. Off Leakage

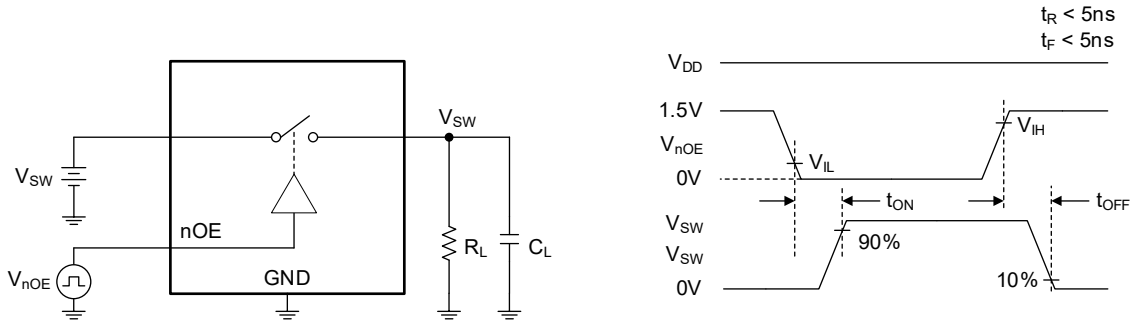


Test Circuit 3. On Leakage

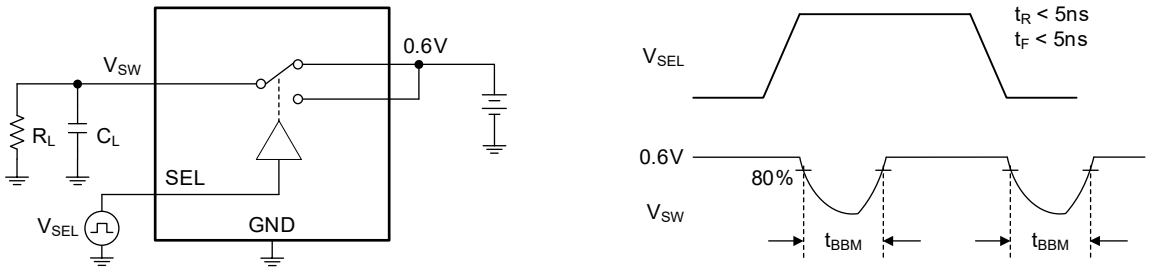
TEST CIRCUITS (continued)



Test Circuit 4. t_{SW} Timing

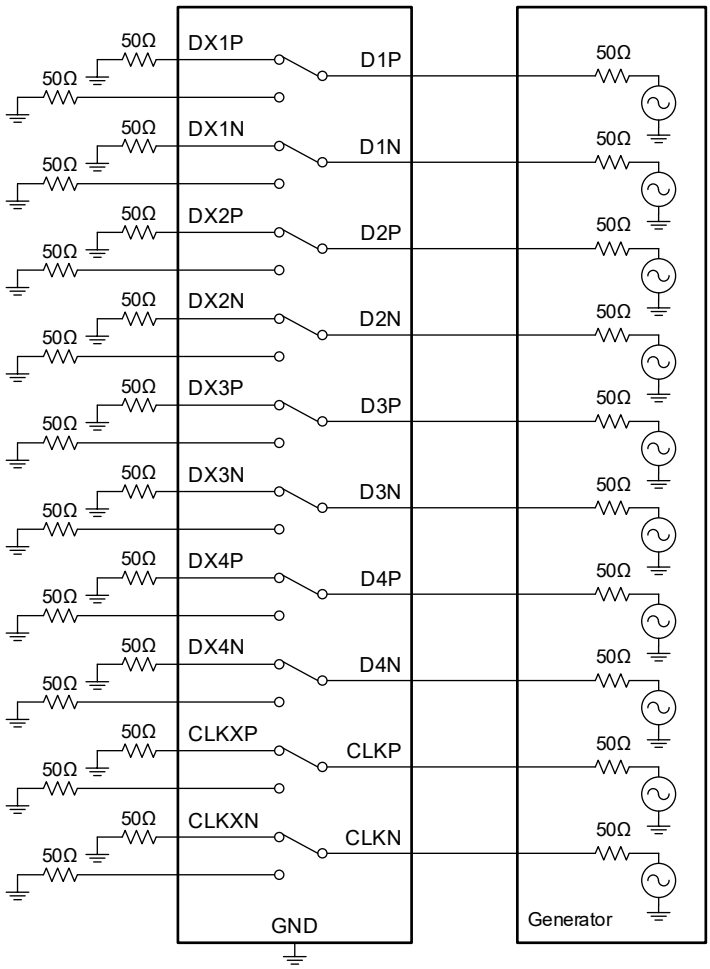


Test Circuit 5. Switching Times (t_{ON}, t_{OFF})



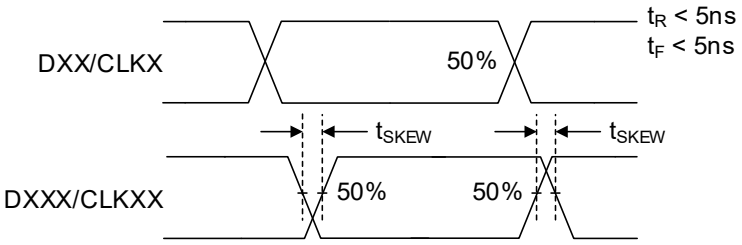
Test Circuit 6. Break-Before-Make Time Delay (t_{BBM})

TEST CIRCUITS (continued)

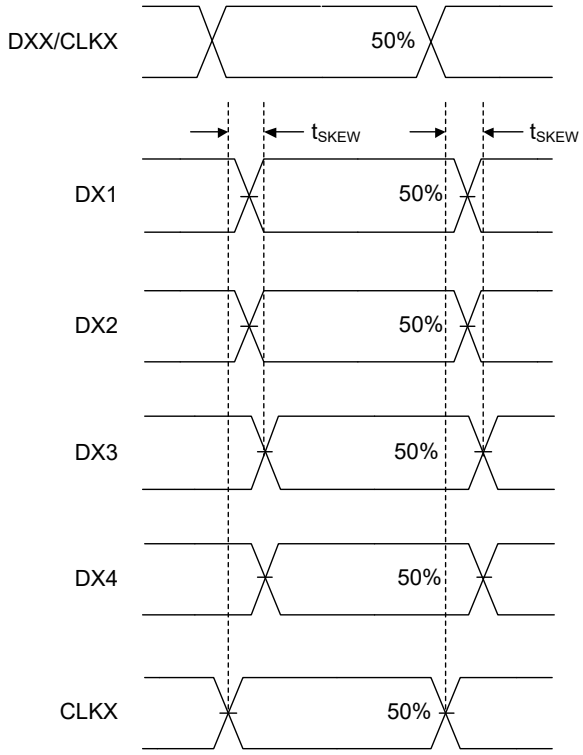


Test Circuit 7. t_{PD}, t_{SKEW_INTRA} and t_{SKEW_INTER} Setup

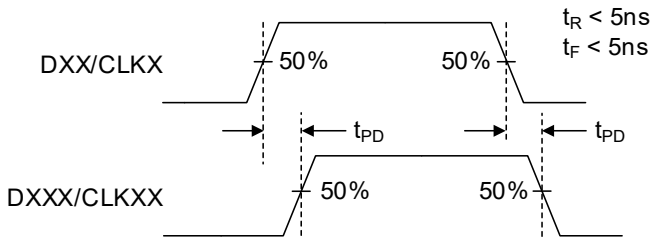
TEST CIRCUITS (continued)



Test Circuit 8. Opposite Transitions of Same Output (t_{SKEW_INTRA})

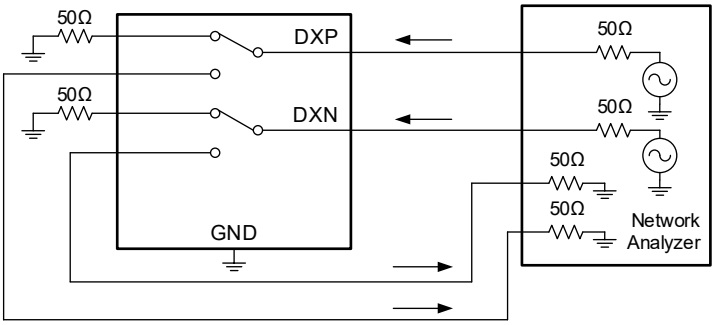


Test Circuit 9. Channel-to-Channel Skew (t_{SKEW_INTER})

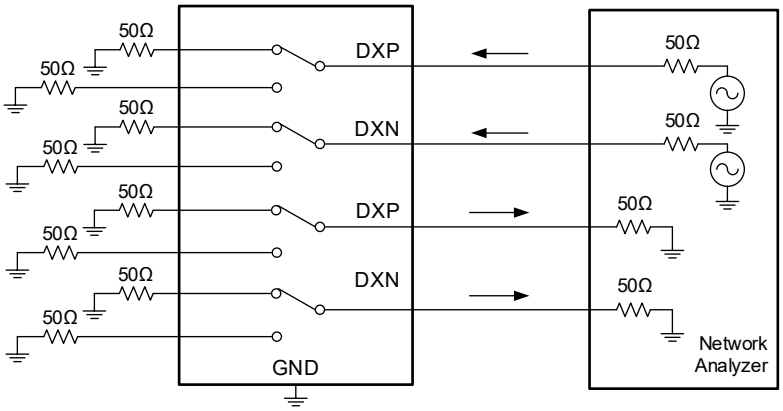


Test Circuit 10. Propagation Delay Time (t_{PD})

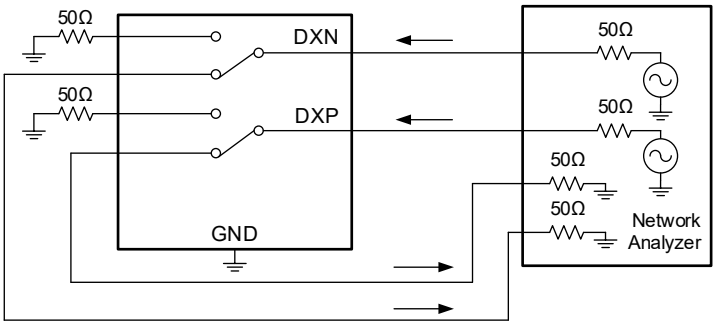
TEST CIRCUITS (continued)



Test Circuit 11. Off-Isolation



Test Circuit 12. Channel-to-Channel Crosstalk



Test Circuit 13. -3dB Bandwidth and Insertion Loss

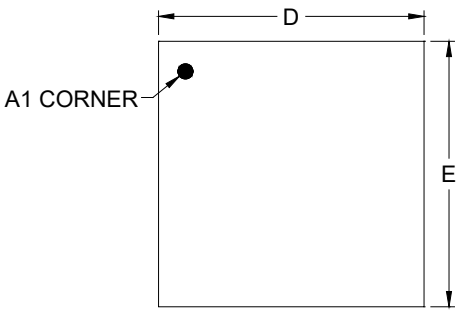
REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

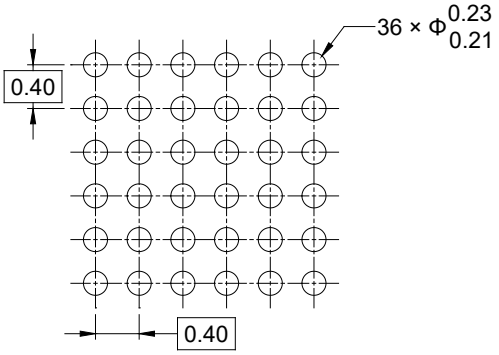
Changes from Original to REV.A (FEBRUARY 2026)	Page
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

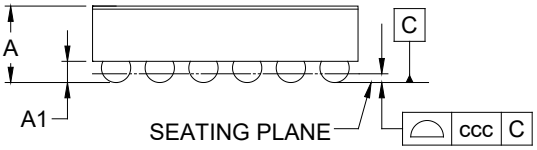
FOCSP-2.43×2.43-36B



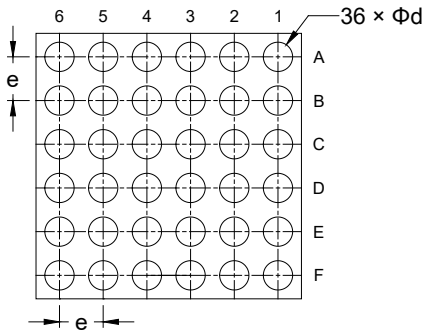
TOP VIEW



RECOMMENDED LAND PATTERN (Unit: mm)



SIDE VIEW



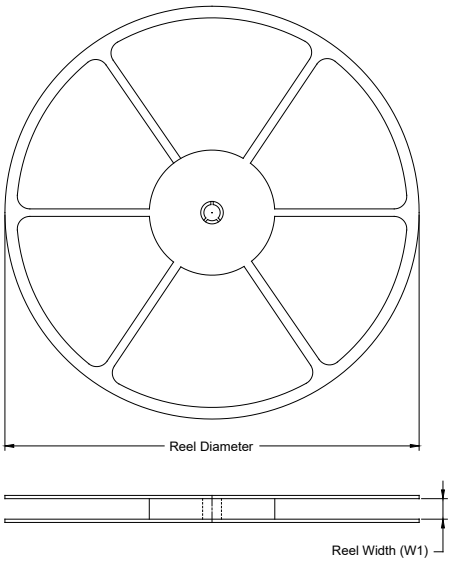
BOTTOM VIEW

Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	-	-	0.700
A1	0.169	-	0.219
D	2.400	-	2.460
E	2.400	-	2.460
d	0.238	-	0.298
e	0.400 BSC		
ccc	0.050		

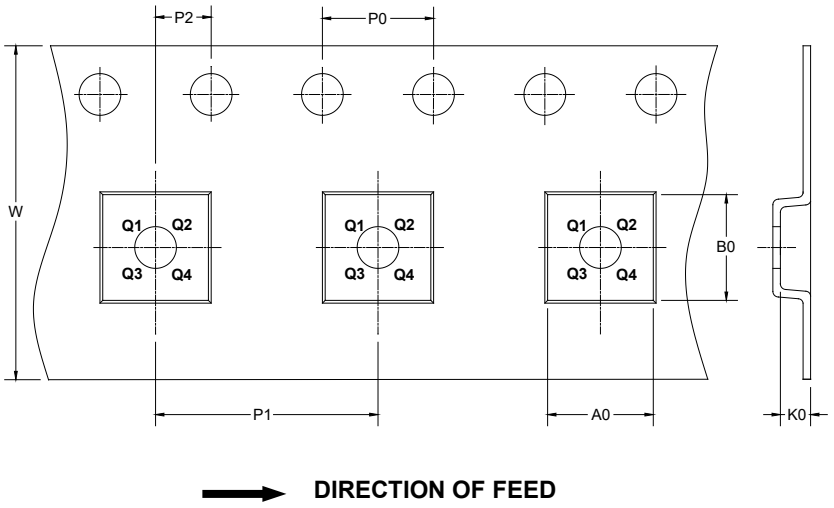
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



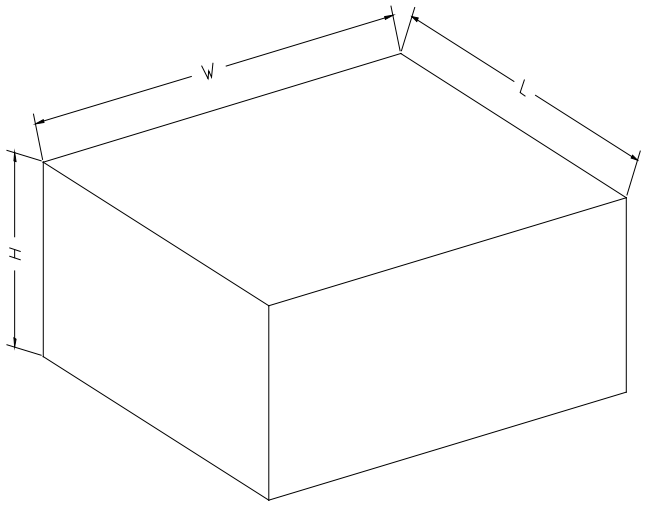
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
FOCSP-2.43×2.43-36B	7"	9.5	2.75	2.75	0.81	4.0	4.0	2.0	8.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18

DD0002