SGM2545
2.7V to 23V, 5.5A, 29mΩ eFuse with True Reverse Current Blocking and Supporting Input Reverse Polarity Protection

GENERAL DESCRIPTION

The SGM2545 is a compact electronic fuse (eFuse) with a full suite of protection functions. With very few external components, the SGM2545 can provide multiple protection modes. To encounter overloads, short-circuit, voltage surges, high inrush current and reverse polarity, the device is suitable as a robust defense. Due to the back-to-back FETs packaged inside the chip, SGM2545 prohibits reverse current flow from output to input, which is ideal for power MUX/ORing applications and systems requiring load side energy hold up storage when input power supply fails. The SGM2545 has almost zero DC reverse current by adopting a linear ORing based scheme, mimicking ideal diode behavior with minimum power dissipation and forward voltage drop.

The V_{OUT} rise time can be programmed by setting an additional capacitor to the SS pin, which can minimize inrush current. Programmable over-voltage protection is used to turn off the device or clamp the output to a fixed voltage (pin-selectable) if the IN rises over a threshold value. In case of output overload, the device actively limits the current or disconnects the circuit. The output current limit threshold and the transient over-current blanking timer can be adjusted by the user. The ILIM pin is also used for load current monitoring.

The SGM2545 is available in a Green TQFN-2×2-10L package.

SIMPLIFIED SCHEMATIC

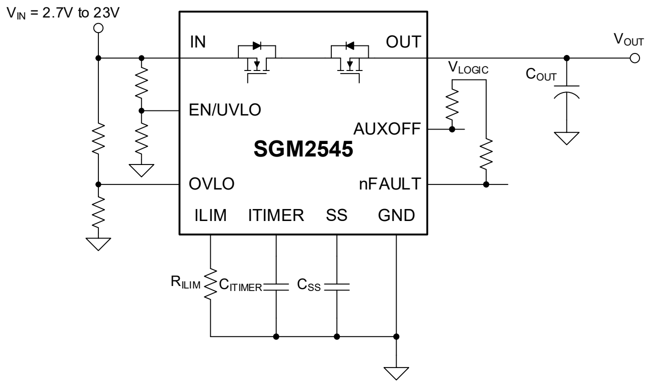

Figure 1. Simplified Schematic

FEATURES

- **Input Voltage: 2.7V to 23V, Surge up to 28V**
  - **Up to -15V Withstands Negative Voltage**
- **Low On-Resistance: 29mΩ (TYP)**
- **Ideal Diode Operation with True Reverse Current Blocking**
- **Fast Over-Voltage Protection**
  - **Pin-Selectable Threshold (3.91V, 5.82V, 13.99V), Over-Voltage Clamp and 5μs Response Time (TYP)**
  - **Adjustable Over-Voltage Lockout and 1.2μs Response Time (TYP)**
- **Over-Current Protection (OCP) with Load Current Monitor Output (ILIM)**
  - **Current Limit or Circuit-Breaker Option**
  - **Programmable Current Limit: 0.5A to 6A ±8% Accuracy for I_{LIM} > 1A**
  - **Programmable Transient Blanking Timer (ITIMER) Allowing Up to 2 × I_{LIM} Peak Currents**
  - **Load Current Monitor Accuracy: ±4.5% (I_{OUT} ≥ 1A)**
- **Fast-Trip Response for Short-Circuit Protection**
  - **Response Time: 500ns (TYP)**
  - **Programmable (2 × I_{LIM}) and Fixed Thresholds**
- **Programmable Output Ramp Time (SS)**
- **Over-Temperature Protection**
- **Digital Outputs**
  - **Priority Power MUX Control Pin (AUXOFF) and Fault Indication (nFAULT)**
  - **Power Good Indication (PG) with Adjustable Threshold (PGTH)**
- **Available in a Green TQFN-2×2-10L Package**

APPLICATIONS

Power MUX/ORing
Protection for Adapter Input
USB PD Protection for PC, Notebook and Monitors
Server, PC Motherboard and Add-On Cards
Patient Monitors
Enterprise Storage for RAID/HBA/SAN/eSSD

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM2545AR	TQFN-2×2-10L	-40℃ to +125℃	SGM2545ARXTSP10G/TR	1IK XXXX	Tape and Reel, 3000
SGM2545AL	TQFN-2×2-10L	-40℃ to +125℃	SGM2545ALXTSP10G/TR	2BW XXXX	Tape and Reel, 3000
SGM2545BR	TQFN-2×2-10L	-40℃ to +125℃	SGM2545BRXTSP10G/TR	1IL XXXX	Tape and Reel, 3000
SGM2545BL	TQFN-2×2-10L	-40℃ to +125℃	SGM2545BLXTSP10G/TR	2AI XXXX	Tape and Reel, 3000
SGM2545CR	TQFN-2×2-10L	-40℃ to +125℃	SGM2545CRXTSP10G/TR	2BX XXXX	Tape and Reel, 3000
SGM2545CL	TQFN-2×2-10L	-40℃ to +125℃	SGM2545CLXTSP10G/TR	2BY XXXX	Tape and Reel, 3000

MARKING INFORMATION

NOTE: XXXX = Date Code, Trace Code and Vendor Code.

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Y Y Y — Serial Number
X X X X
│ │  └── Vendor Code
│ └──── Trace Code
└────── Date Code - Year
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Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

SELECTABLE MODEL

Model	Over-Voltage Response	Over-Current Response	AUXOFF/PG	nFAULT/PGTH	Response to Fault
SGM2545AR	Adjustable OVLO	Active Current Limit	AUXOFF	nFAULT	Auto-Retry
SGM2545AL					Latch-Off
SGM2545BR	Pin-Selectable OVC (3.91V/5.82V/13.99V)		PG	PGTH	Auto-Retry
SGM2545BL					Latch-Off
SGM2545CR	Adjustable OVLO	Circuit Breaker			Auto-Retry
SGM2545CL					Latch-Off

ABSOLUTE MAXIMUM RATINGS

Input Voltage Range, V_{IN}
-40℃ to +125℃.................. MAX(-15V, V_{OUT} - 21V) to 28V
-10℃ to +125℃.................. MAX(-15V, V_{OUT} - 22V) to 28V
Output Voltage Range, V_{OUT}
-40℃ to +125℃.................... -0.3V to MIN(28V, V_{IN} + 21V)
-10℃ to +125℃.................... -0.3V to MIN(28V, V_{IN} + 22V)
Output Voltage Pulse (< 1μs), V_{OUT_PLS} ....> -0.8V
Enable Voltage Range, $V_{EN/UVLO}$ (1)................... -0.3V to 6.5V
OVLO Voltage Range (SGM2545Ax/Cx), V_{OVLO} (1)................ -0.3V to 6.5V
OVCSEL Voltage Range (SGM2545Bx), V_{OVCSEL}................. Internally Limited
SS Voltage Range, V_{SS}............................... Internally Limited
ITIMER Voltage Range, V_{ITIMER} .... Internally Limited
PGTH Voltage Range (SGM2545Bx/Cx), V_{PGTH} (1)................ -0.3V to 6.5V
AUXOFF Voltage Range (SGM2545Ax), V_{AUXOFF}.................. -0.3V to 6.5V
PG Voltage Range (SGM2545Bx/Cx), V_{PG}............................ -0.3V to 6.5V
nFAULT Voltage Range (SGM2545Ax), V_{nFAULT} (1)................ -0.3V to 6.5V
ILIM Voltage Range, V_{ILIM}........................... Internally Limited
Continuous Switch Current, I_{MAX}................. Internally Limited
Package Thermal Resistance
TQFN-2×2-10L, θ_{JA}... 66.7℃/W
TQFN-2×2-10L, θ_{JB}... 3.8℃/W
TQFN-2×2-10L, θ_{JC}... 50.6℃/W
Junction Temperature...+150℃
Storage Temperature Range........................-65℃ to +150℃
Lead Temperature (Soldering, 10s)............................+260℃
ESD Susceptibility (2) (3)
HBM (NC OUT)..±4000V
HBM (OUT Only to GND)...±2000V
CDM ....±1000V

NOTES:

1. If this pin is pulled up to V_{IN}, a 350kΩ or higher pull-up resistance is recommended which is to limit the current when input voltage is negative.
2. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.
3. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

RECOMMENDED OPERATING CONDITIONS

Input Voltage Range, V_{IN} ....2.7V to 23V (1)
Output Voltage Range, V_{OUT}.......MIN(23V, V_{IN} + 20V) (MAX)
Enable Voltage Range, $V_{EN/UVLO}$....................................5V (2)
OVLO Voltage Range (SGM2545Ax/Cx)............0.5V to 1.5V
SS Capacitor Voltage Rating, V_{SS}...............V_{IN} + 5V (3) (MIN)
nFAULT Voltage Range, V_{nFAULT}.................................. 5V (4)
PGTH Voltage Range (SGM2545Bx/Cx), V_{PGTH}..................... 5V (4)
AUXOFF Voltage Range (SGM2545Ax), V_{AUXOFF}.................. 5V (4)
PG Voltage Range (SGM2545Bx/Cx), V_{PG}............................ 5V (4)
ITIMER Capacitor Voltage Rating, V_{ITIMER}...................... > 4V
ILIM Pin Resistance to GND, R_{ILIM} .... 549Ω to 6650Ω
Continuous Switch Current (T_J ≤ +125℃), I_{MAX}.............. 5.5A
Operating Junction Temperature Range..... -40℃ to +125℃

NOTES:

1. When using SGM2545Bx variants, ensure that the input operating voltage is restricted to the chosen output voltage clamp threshold as specified in the electrical characteristics section.
2. When supply voltages are below 5V, connecting the EN/UVLO pin directly to IN is acceptable. For voltages exceeding 5V or systems prone to reverse polarity on the input supply, it's advised to employ a pull-up resistor with a minimum value of 350kΩ.
3. In PowerMUX/ORing setups with unequal supplies, select the SS capacitor rating for each device based on the higher of the two rails.
4. For systems at risk of reverse polarity on the input supply, if referencing this pin to the input supply, using a pull-up resistor with a minimum value of 350kΩ is recommended to limit current through the pin.

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

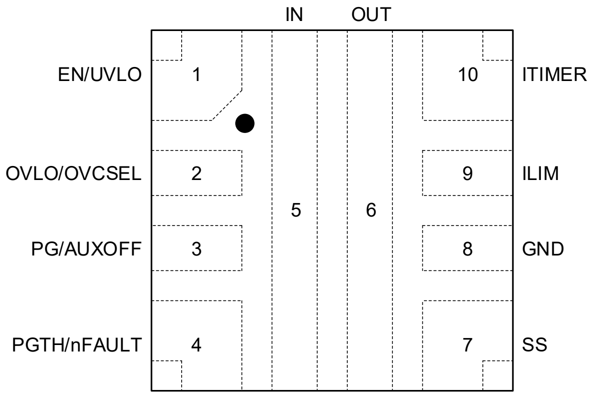
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

(TOP VIEW)



TQFN-2×2-10L

PIN DESCRIPTION

PIN	NAME	TYPE	FUNCTION
1	EN/UVLO	AI	Enable and Under-Voltage Lockout Input. Asserting EN/UVLO pin high enables the device. As a UVLO pin, the UVLO threshold is programmed by an external resistor divider. This pin cannot be left floating.
2	OVLO	AI	(SGM2545Ax/Cx Only) Over-Voltage Lockout Pin. The over-voltage lockout threshold is programmed by the resistor divider from the power supply to the OVLO terminal to GND. The device is enabled when this pin is tied to low level. This pin cannot be left floating.
	OVCSEL	AI	(SGM2545Bx Only) Output Clamp Voltage Selection Pin.
3	PG	DO	Power Good Indication (SGM2545Bx/Cx Only). This is an open-drain pin, when the internal channels of the chip are all turned on and the PGTH signal value is higher than the set value, the pin is set to high level.
	AUXOFF	DO	(SGM2545Ax Only) Auxiliary Channel Control Pin. This is an open-drain pin, if V_{IN} > V_{UVP} and the internal channels of the chip are all turned on, the pin is set to high level. This can be utilized to enable/disable the auxiliary supply eFuse, aiding in seamless switchover in a priority power MUXing configuration.
4	nFAULT	DO	Fault Event Indicator (SGM2545Ax Only). The nFAULT is an open-drain output, and when a fault occurs, it will be low.
	PGTH	AI	Power Good Threshold. (SGM2545Bx/Cx Only)
5	IN	P	Input Supply Voltage.
6	OUT	P	Output of the Device.
7	SS	AO	Soft-Start Pin. The capacitor between SS and GND pins will set the slew rate according to the application requirements. When this pin is left floating, the device will start up at the fastest rate.
8	GND	G	GND.
j9	ILIM	AO	Current Limit Programming Pin. Use this dual function pin for limiting and monitoring the output current. Connecting this pin to GND can set the output current limit. It is also possible to monitor the load current with this pin voltage. Do not float this pin.
10	ITIMER	AO	Place a capacitor between this pin and GND can set the over-current blanking time, at this stage, the output current value can temporarily exceed the internally set current limit value (but not exceed the fast-trip threshold). After this time, the device will take action if it is still in over-current state. Leaving this pin open will provide the fastest response to an over-current event.

NOTE: AI = analog input, AO = analog output, DO = digital output, P = power, G = ground.

ELECTRICAL CHARACTERISTICS

(T_J = -40℃ to +125℃, V_{IN} = 12V, OUT pin floating, $V_{EN/UVLO}$ = 2V, V_{OVLO} = 0V for SGM2545Ax/Cx, OVCSEL = 390kΩ to GND for SGM2545Bx, R_{ILIM} = 549Ω, SS, ITIMER, AUXOFF and nFAULT pins floating for SGM2545Ax, PGTH and PG pins floating for SGM2545Bx/Cx, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Supply (IN)						
Under-Voltage Protection Threshold	V_{UVP_R}	Rising	2.46	2.55	2.64	V
	V_{UVP_F}	Falling	2.23	2.31	2.39	
Supply Quiescent Current	I_{Q_ON}	SGM2545Ax only		200	300	μA
		SGM2545Bx only		210	320	
		SGM2545Cx only		200	300	
		During RCB, V_{OUT} = V_{IN} + 1V, SGM2545Ax/Cx only		180		
		During RCB, V_{OUT} = V_{IN} + 1V, SGM2545Bx only		190		
		During OVC, SGM2545Bx only		225	330	
Supply Disabled State Current	I_{Q_OFF}	V_{SD_F} < V_{EN} < V_{UVLO_F}		67	115	μA
Supply Shutdown Current	I_{SD}	V_{EN} < V_{SD_F}		8.0	21.0	μA
IN Supply Off Current	I_{Q_OVLO}	OVLO condition, V_{OUT} = V_{IN} + 1V		170	260	μA
IN Supply Leakage Current	I_{INLKG_IRPP}	V_{IN} = -14V, V_{OUT} = 0V		-13.0		μA
OUT Leakage Current	I_{OUTLKG_OVLO}	OVLO condition, V_{OUT} > V_{IN}, SGM2545Ax/Bx only		340	500	μA
		OVLO condition, V_{OUT} > V_{IN}, SGM2545Cx only		1880	2700	
On-Resistance (IN - OUT)						
On-Resistance	R_{DSON}	V_{IN} = 12V, I_{OUT} = 3A, T_J = +25℃		29		mΩ
		V_{IN} = 2.7V to 23V, I_{OUT} = 3A, T_J = -40℃ to +125℃			48	
Enable/Under-Voltage Lockout (EN/UVLO)						
EN/UVLO Rising Threshold	V_{UVLO_R}		1.185	1.210	1.235	V
EN/UVLO Falling Threshold	V_{UVLO_F}		1.065	1.090	1.115	V
EN/UVLO Falling Threshold for Lowest Shutdown Current	V_{SD_F}		0.30	0.73		V
EN/UVLO Leakage Current	I_{ENLKG}		-0.7		0.7	μA
Over-Voltage Lockout (OVLO) SGM2545Ax/Cx						
OVLO Rising Threshold	V_{OV_R}		1.185	1.210	1.235	V
OVLO Falling Threshold	V_{OV_F}		1.065	1.090	1.115	V
OVLO Pin Leakage Current	I_{OVLKG}	0.5V < V_{OVLO} < 1.5V	-0.9		0.9	μA
Output Voltage Clamp (OUT) SGM2545Bx						
Over-Voltage Clamp Threshold	V_{OVC}	OVCSEL = shorted to GND	3.71	3.91	4.11	V
		OVCSEL = open	5.50	5.82	6.14	
		OVCSEL = 390kΩ to GND	13.39	13.99	14.59	
Output Voltage during Clamping	V_{CLAMP}	I_{OUT} = 10mA, OVCSEL = shorted to GND	3.63	3.83	4.03	V
		I_{OUT} = 10mA, OVCSEL = open	5.40	5.72	6.04	
		I_{OUT} = 10mA, OVCSEL = 390kΩ to GND	13.26	13.86	14.46	

ELECTRICAL CHARACTERISTICS (continued)

(T_J = -40℃ to +125℃, V_{IN} = 12V, OUT pin floating, $V_{EN/UVLO}$ = 2V, V_{OVLO} = 0V for SGM2545Ax/Cx, OVCSEL = 390kΩ to GND for SGM2545Bx, R_{ILIM} = 549Ω, SS, ITIMER, AUXOFF and nFAULT pins floating for SGM2545Ax, PGTH and PG pins floating for SGM2545Bx/Cx, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Over-Current Protection (OUT)						
Over-Current Threshold	I_{LIM}	R_{ILIM} = 6.65kΩ	0.415	0.490	0.565	A
		R_{ILIM} = 3.32kΩ	0.870	0.980	1.090	
		R_{ILIM} = 1.65kΩ	1.870	2.040	2.210	
		R_{ILIM} = 750Ω	4.120	4.500	4.880	
		R_{ILIM} = 549Ω	5.550	6.120	6.690	
Circuit-Breaker Threshold	I_{FAULT}	ILIM pin open		0.1		A
		ILIM pin shorted to GND		1.1	1.7	
Scalable Fast-Trip Threshold (I_{SC}): I_{LIM} Ratio	I_{SCGain}			190		%
Fixed Fast-Trip Current Threshold	I_{FT}			22.0		A
V_{OUT} Threshold to Exit Current Limit Foldback	V_{FB}			1.9		V
Over-Current Fault Timer (ITIMER)						
ITIMER Internal Discharge Current	I_{ITIMER}	$I_{OUT} > I_{LIM}$	1.2	1.8	2.4	μA
ITIMER Internal Pull-Up Resistance	R_{ITIMER}			17		kΩ
ITIMER Internal Pull-Up Voltage	V_{INT}		2.53	2.68	2.83	V
ITIMER Discharge Differential Voltage Threshold	ΔV_{ITIMER}		1.39	1.52	1.65	V
Output Load Current Monitor (ILIM)						
Analog Load Current Monitor Gain (I_{MON} : I_{OUT})	G_{IMON}	I_{OUT} = 0.5A to 1A, $I_{OUT} < I_{LIM}$	170	190	215	μA/A
		I_{OUT} = 1A to 5.5A, $I_{OUT} < I_{LIM}$	165	182	200	
Reverse Current Blocking (IN - OUT)						
V_{IN} - V_{OUT} Forward Regulation Voltage	V_{FWD}	I_{OUT} = 10mA	5.0	18.0		mV
V_{IN} - V_{OUT} Threshold for Fast BFET Turn-Off	V_{REVTH}	Enter reverse current blocking	-42.0	-26.0	-10.0	mV
	V_{FWDTH}	Exit reverse current blocking	40.0	110.0	170.0	
OUT Leakage Current during Unpowered Condition	I_{REVLKG_OFF}	V_{OUT} = 12V, V_{IN} = 0V		4.3		μA
Reverse Leakage Current to GND	I_{REVLKG_GND}	V_{OUT} - V_{IN} = 21.5V		5.5		μA
Reverse Leakage Current to VIN	I_{REVLKG_VIN}	V_{OUT} - V_{IN} = 21.5V, T_J = +85℃			6 (1)	μA
OUT Leakage Current during On-State with RCB	I_{OUTLKG_RCB}	V_{OUT} = V_{IN} + 1V		60		μA
Power Good (PG) Indication - SGM2545Bx/Cx or Auxiliary Channel Control (AUXOFF) - SGM2545Ax						
PG/AUXOFF Voltage while De-Asserted	V_{PGD}	$V_{IN} < V_{UVP\_F}$, $V_{EN} < V_{SD\_F}$, weak pull-up (I_{PG} = 26μA)		0.51	0.71	V
		$V_{IN} < V_{UVP\_F}$, $V_{EN} < V_{SD\_F}$, strong pull-up (I_{PG} = 242μA)		0.64	0.84	
		$V_{IN} > V_{UVP\_R}$		0.0		
PG/AUXOFF Leakage Current	I_{PGLKG}	PG/AUXOFF asserted		0.9	2.0	μA

ELECTRICAL CHARACTERISTICS (continued)

(T_J = -40℃ to +125℃, V_{IN} = 12V, OUT pin floating, $V_{EN/UVLO}$ = 2V, V_{OVLO} = 0V for SGM2545Ax/Cx, OVCSEL = 390kΩ to GND for SGM2545Bx, R_{ILIM} = 549Ω, SS, ITIMER, AUXOFF and nFAULT pins floating for SGM2545Ax, PGTH and PG pins floating for SGM2545Bx/Cx, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Power Good Threshold (PGTH) - SGM2545Bx/Cx						
PGTH Threshold	V_{PGTH_R}	Rising	1.175	1.210	1.245	V
	V_{PGTH_F}	Falling	1.055	1.090	1.125	V
PGTH Leakage Current	$I_{PGTHLKG}$		-1.5		1.5	μA
Fault Indication (nFAULT) - SGM2545Ax						
nFAULT Leakage Current	$I_{FAULTLKG}$		-1.0		1.0	μA
nFAULT Internal Pull-Down Resistance	R_{nFAULT}			14.0		Ω
Over-Temperature Protection (OTP)						
Thermal Shutdown Rising Threshold	T_{SD}			150		℃
Thermal Shutdown Hysteresis	T_{HYS}			10		℃
SS						
SS Pin Charging Current	I_{SS}		0.90	2.20	3.50	μA

NOTE:

1. Guaranteed by design, not tested in production.

TIMING REQUIREMENTS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Over-Voltage Lockout Response Time	t_{OVLO}	SGM2545Ax/Cx, V_{OVLO} > V_{OV_R} to V_{OUT}↓		1.2		μs
Over-Voltage Clamp Response Time	t_{OVC}	SGM2545Bx, V_{IN} > V_{OVC} to V_{OUT}↓		5		μs
Circuit-Breaker Response Time	t_{CB}	SGM2545Cx, I_{OUT} > 1.2 × I_{LIM} and ITIMER expired to I_{OUT}↓		2		μs
Current Limit Response Time	t_{LIM}	SGM2545Ax/Bx, I_{OUT} > 1.2 × I_{LIM} and ITIMER expired to I_{OUT} settling to within 5% of I_{LIM}		400		μs
Scalable Fast-Trip Response Time	t_{SC}	I_{OUT} > 3 × I_{LIM} to I_{OUT}↓		500		ns
Fixed Fast-Trip Response Time	t_{FT}	I_{OUT} > I_{FT} to I_{OUT}↓		500		ns
Auto-Retry Interval after Fault	t_{RST}	SGM2545xR		110		ms
OVLO Fast Recovery Response Time	t_{SWOV}	V_{OVLO} < V_{OV_F} to V_{OUT}↑		90		μs
Reverse Current Blocking Recovery Time	t_{SWRCB}	V_{IN} - V_{OUT} > V_{FWDTH} to V_{OUT}↑		50		μs
Reverse Current Blocking Comparator Response Time	t_{RCB}	V_{IN} - V_{OUT} > 1.3 × V_{REVTH} to BFET OFF		1		μs
PG Assertion De-Glitch Time	t_{PGA}	SGM2545Bx/Cx		12		μs
PG De-Assertion De-Glitch Time	t_{PGD}	SGM2545Bx/Cx		12		μs

SWITCHING CHARACTERISTICS

In the entire normal voltage range, the output voltage rise rate is set by the internal circuit and remains unchanged to ensure that the load state does not affect the start-up sequence. Adding capacitance between the SS pin and GND can change the OUT rising slope. Increasing capacitor C_{SS} will reduce the rate of rise (SR) of the output voltage. For a detailed description, please refer to the relevant sections on inrush current suppression (SS) and slew rate. However, the time that V_{OUT} falls when the device is turned off is determined by the RC time constants of the load resistor (R_L) and load capacitor (C_{OUT}). The control of the switch only affects the power-on sequence when the chip is turned on.

(R_L = 100Ω, C_{OUT} = 1μF, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	V_{IN}	C_{SS} = Open	C_{SS} = 1800pF	C_{SS} = 3300pF	UNITS
Output Rising Slew Rate	SR_{ON}	2.7V	11.85	1.10	0.62	V/ms
		12V	31.87	1.21	0.66	
		23V	50.83	1.23	0.67	
Turn-On Delay	t_{D_ON}	2.7V	0.26	1.06	1.75	ms
		12V	0.33	1.85	3.40	
		23V	0.34	2.78	4.84	
Rise Time	t_R	2.7V	0.18	1.98	3.49	ms
		12V	0.30	7.91	14.29	
		23V	0.36	14.95	27.46	
Turn-On Time	t_{ON}	2.7V	0.44	3.04	5.24	ms
		12V	0.69	9.76	17.69	
		23V	0.70	17.73	32.30	
Turn-Off Delay	t_{D_OFF}	2.7V	10.95	10.16	10.21	μs
		12V	6.67	6.66	6.73	
		23V	4.90	4.89	4.91	

SWITCHING CHARACTERISTICS (continued)

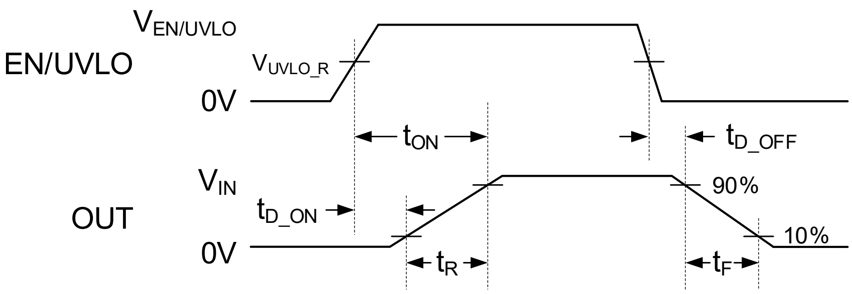
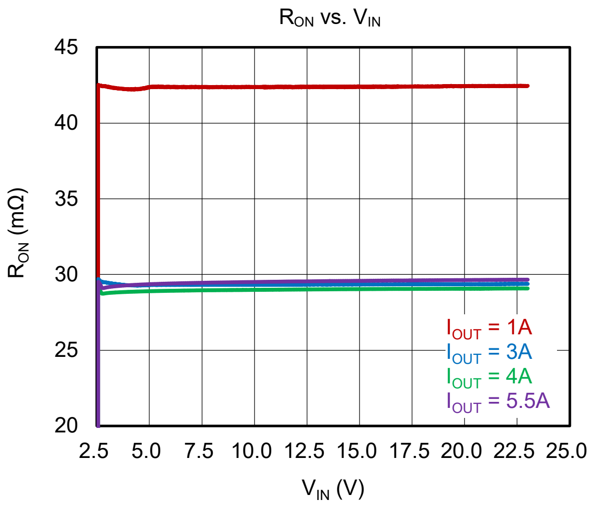
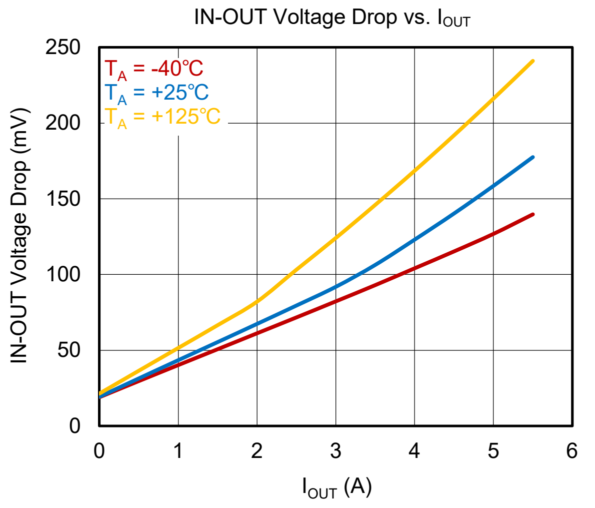


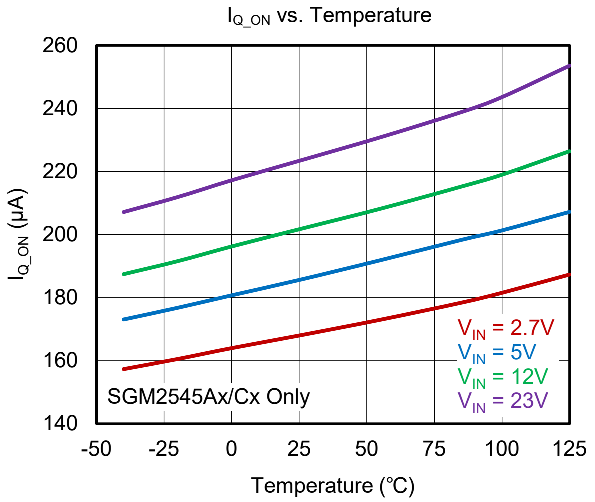
Figure 2. SGM2545 Switching Times

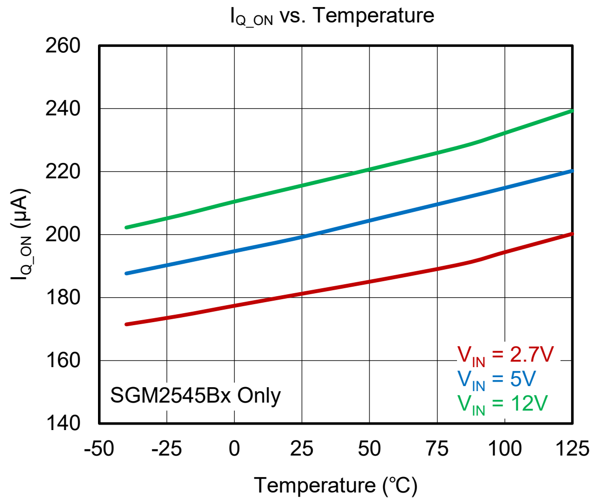
TYPICAL PERFORMANCE CHARACTERISTICS

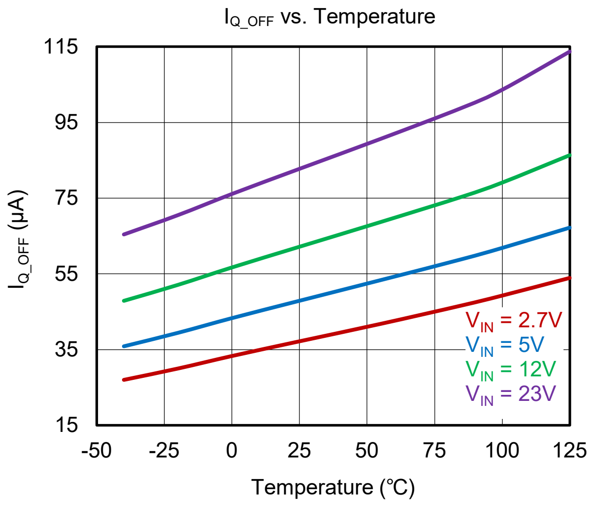
V_{IN} = 12V, T_A = +25℃, unless otherwise noted.

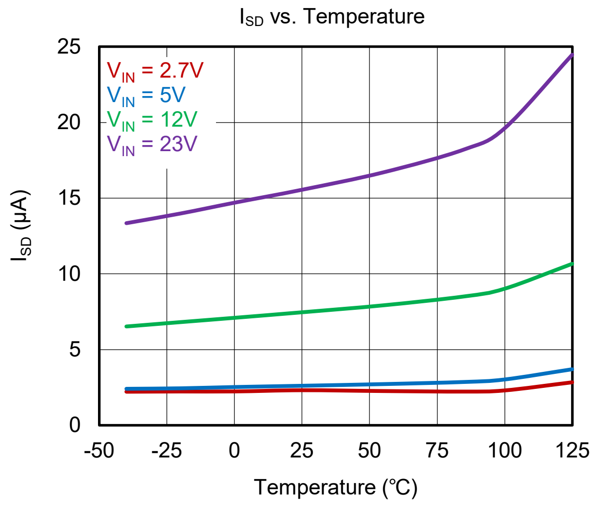






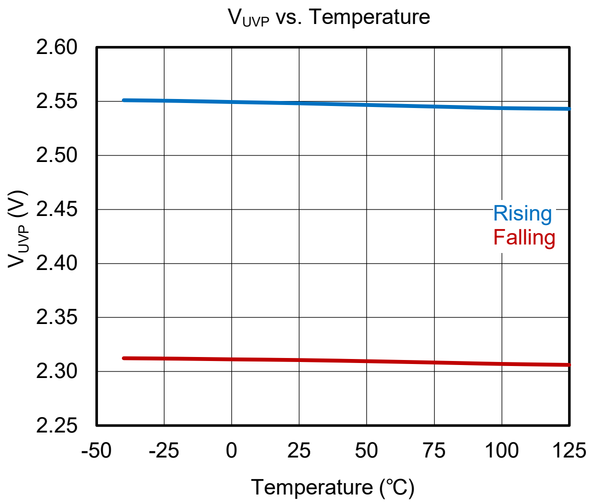


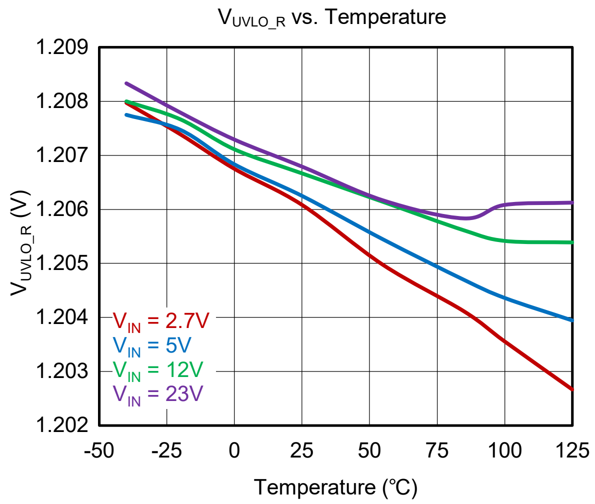


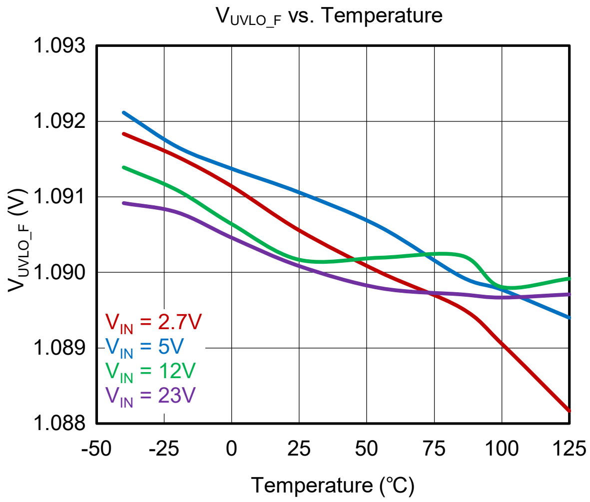


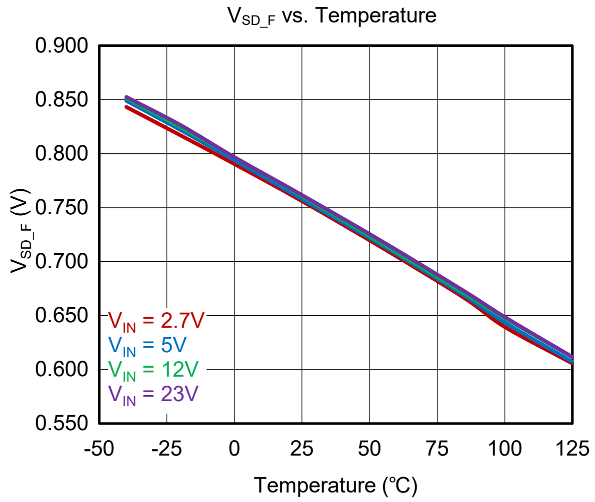
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

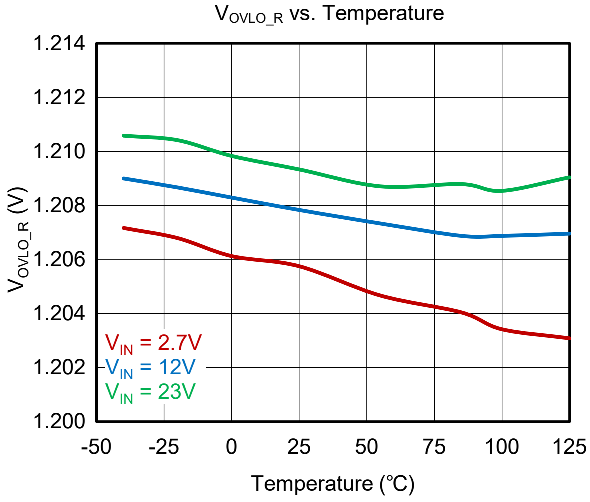
V_{IN} = 12V, T_A = +25℃, unless otherwise noted.

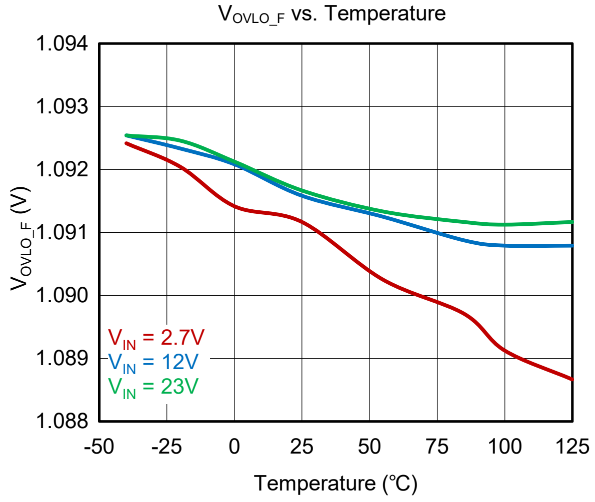








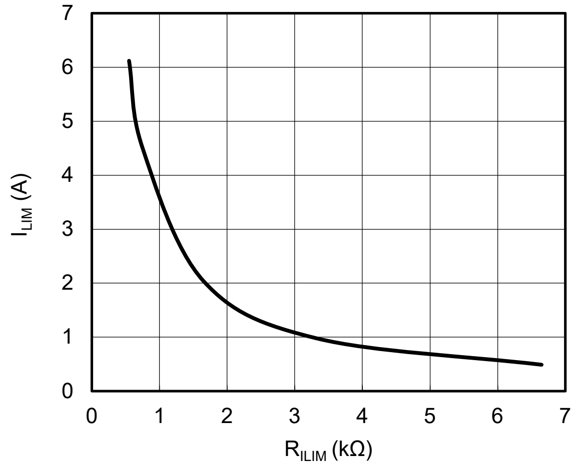




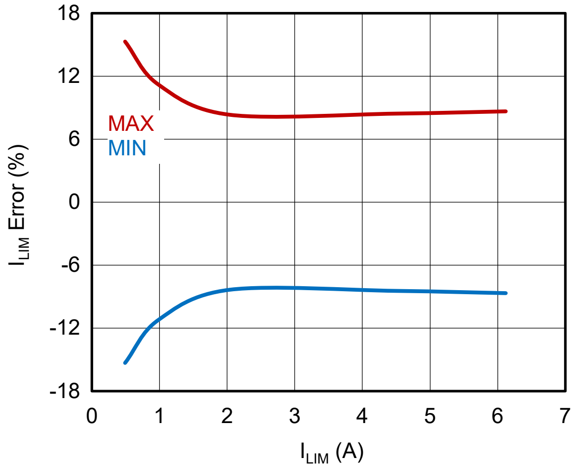
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

V_{IN} = 12V, T_A = +25℃, unless otherwise noted.

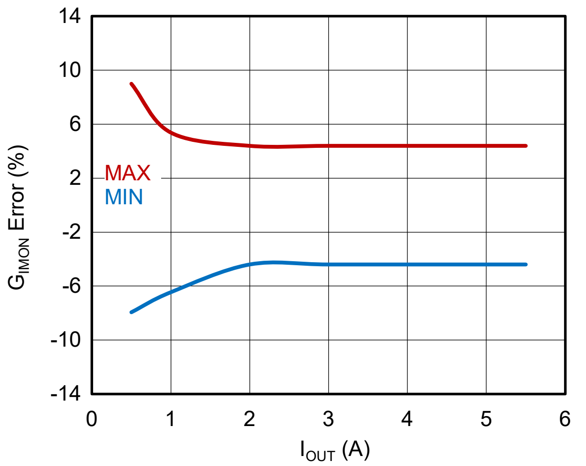
I_{LIM} vs. R_{LIM}



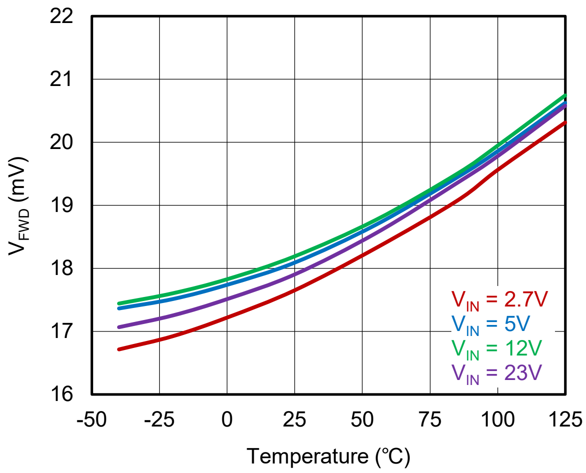
I_{LIM} Error vs. I_{LIM}



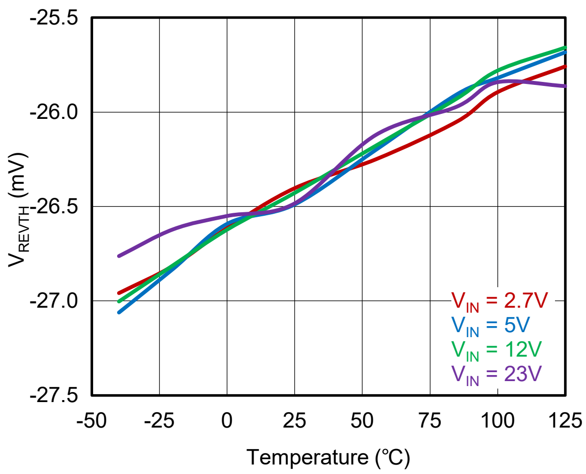
G_{IMON} Error vs. I_{OUT}



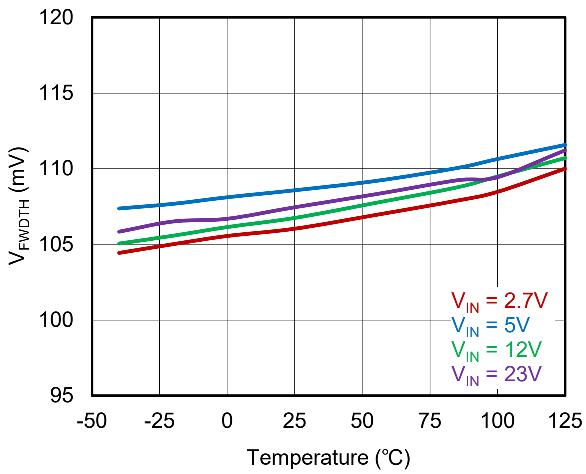
V_{FWD} vs. Temperature



V_{REVTH} vs. Temperature



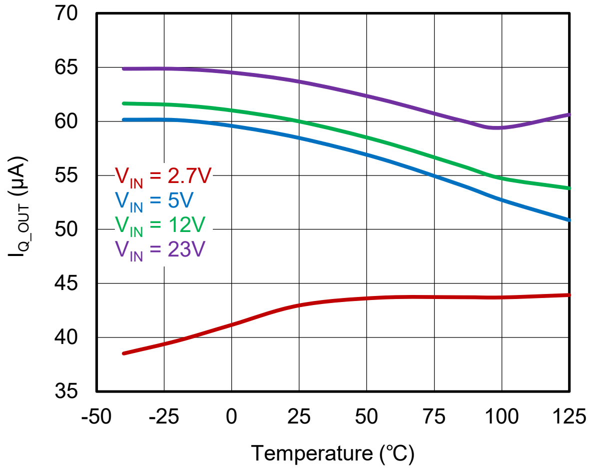
V_{FWDTH} vs. Temperature



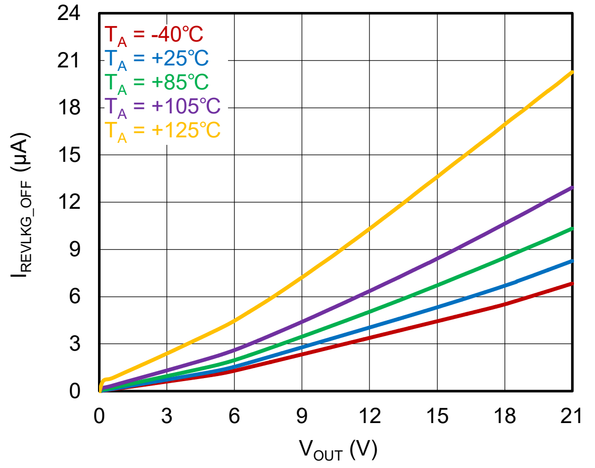
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

V_{IN} = 12V, T_A = +25℃, unless otherwise noted.

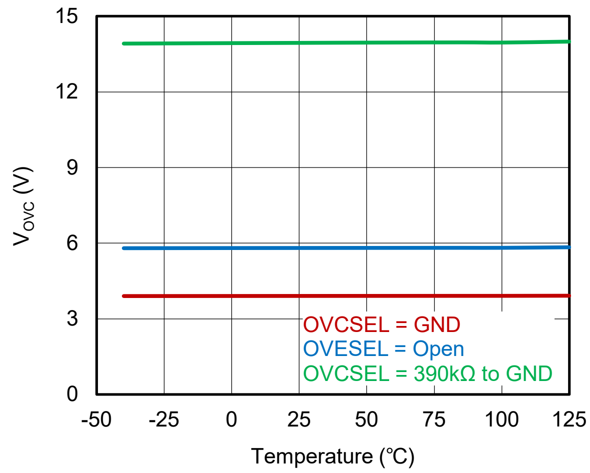
I_{Q_OUT} vs. Temperature



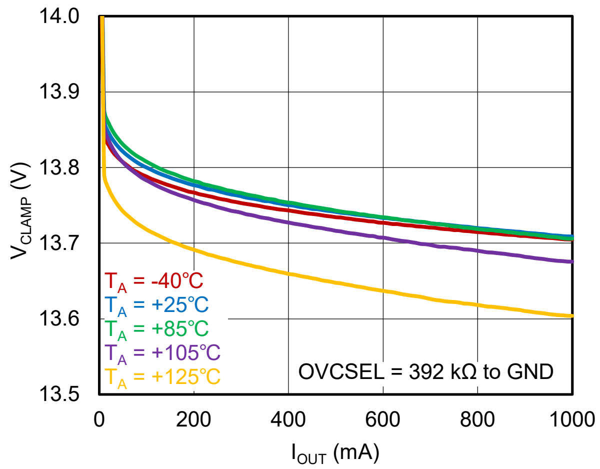
I_{REVLKG_OFF} vs. V_{OUT}



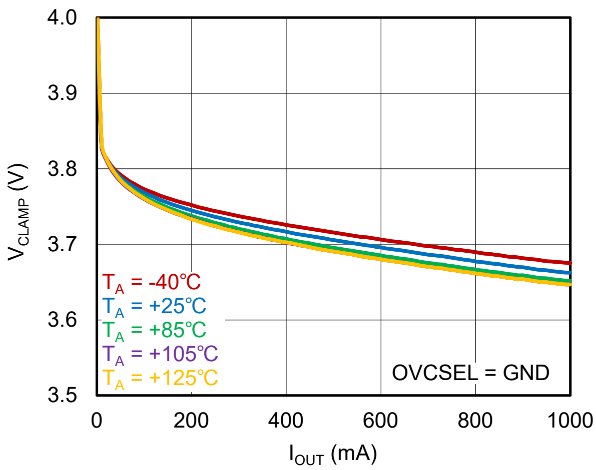
V_{OVC} vs. Temperature



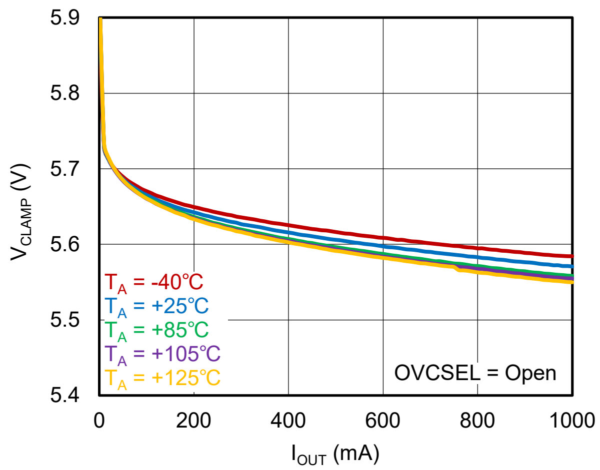
V_{CLAMP} vs. I_{OUT}



V_{CLAMP} vs. I_{OUT}

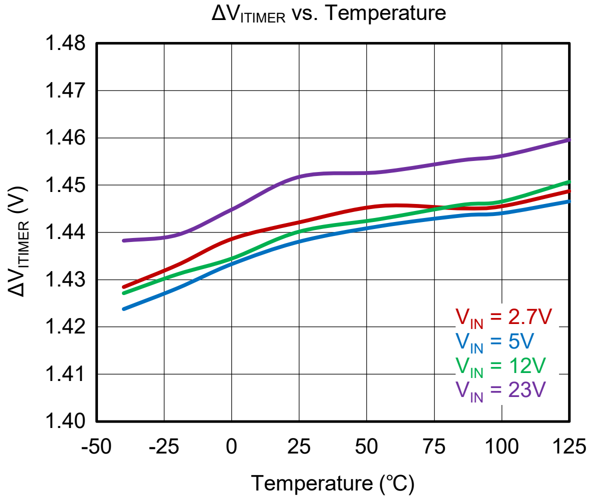


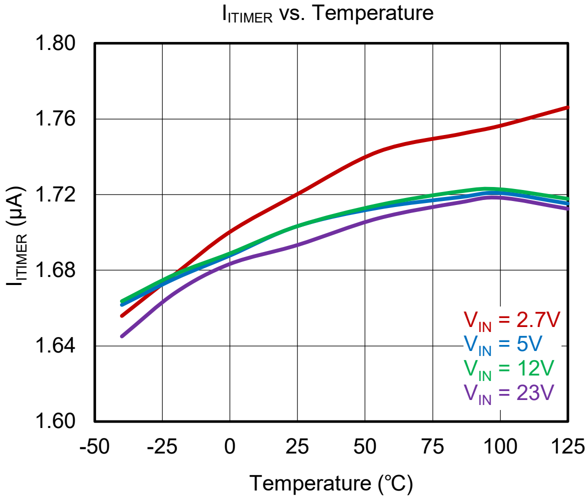
V_{CLAMP} vs. I_{OUT}

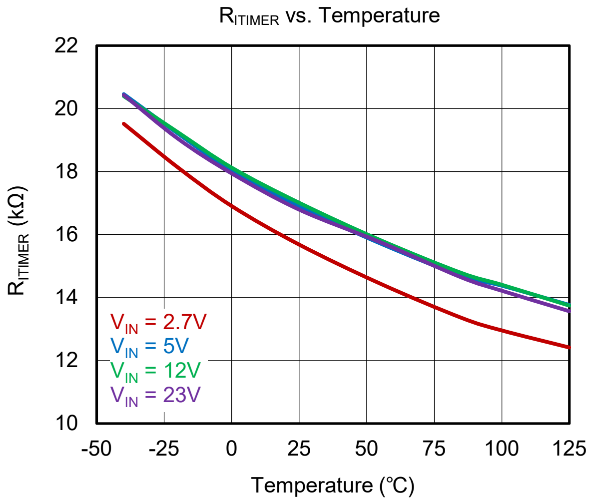


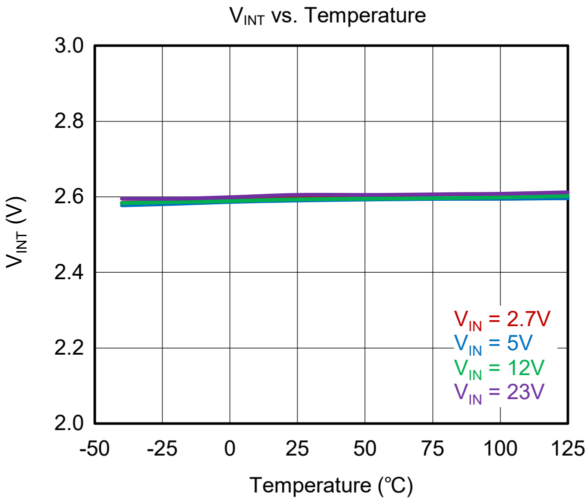
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

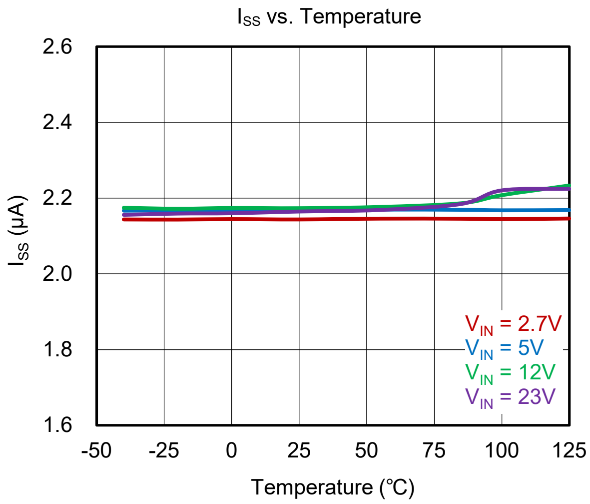
V_{IN} = 12V, T_A = +25℃, unless otherwise noted.

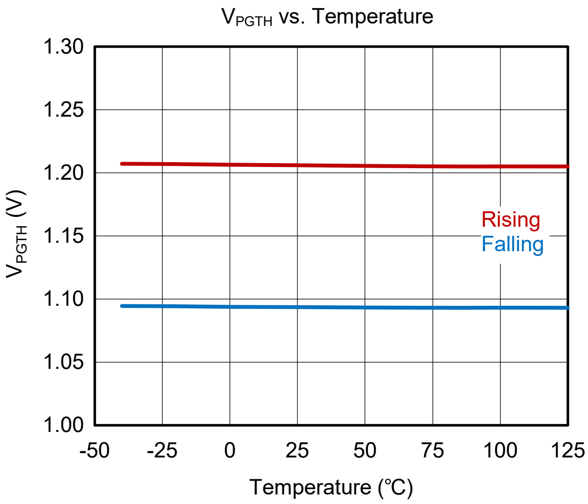






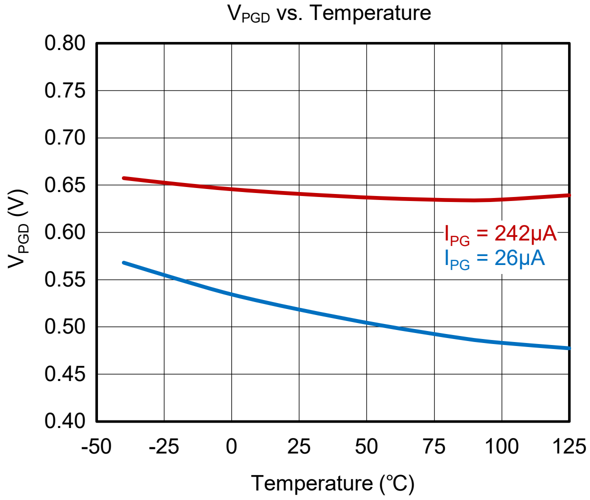


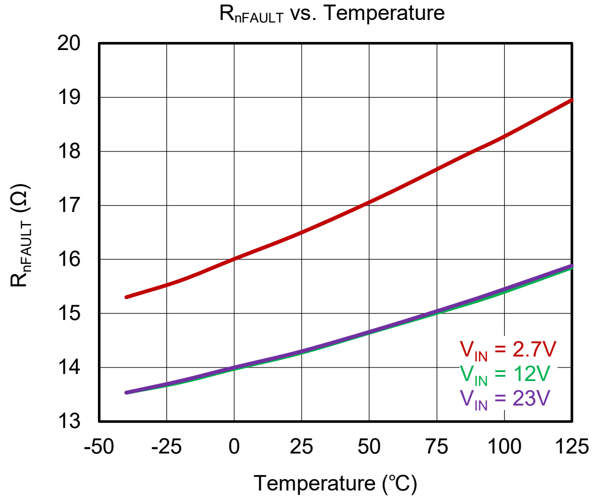


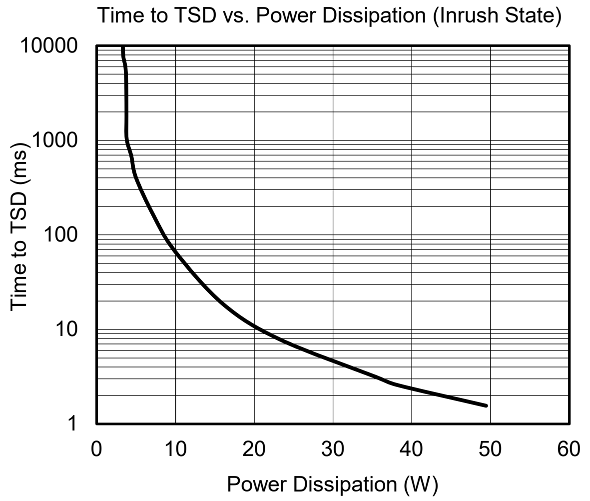


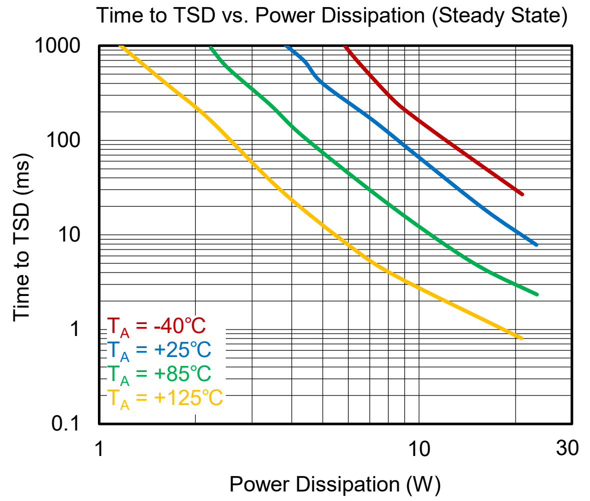
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

V_{IN} = 12V, T_A = +25℃, unless otherwise noted.





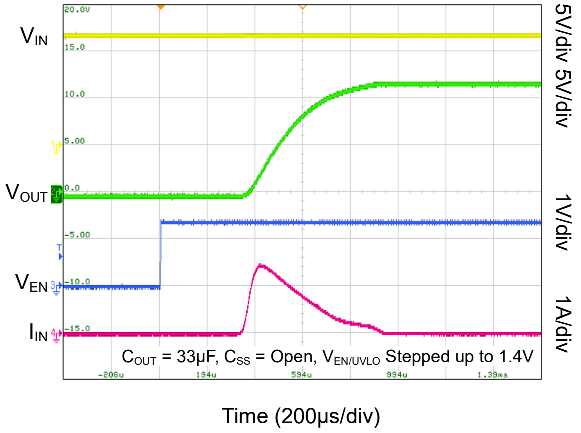




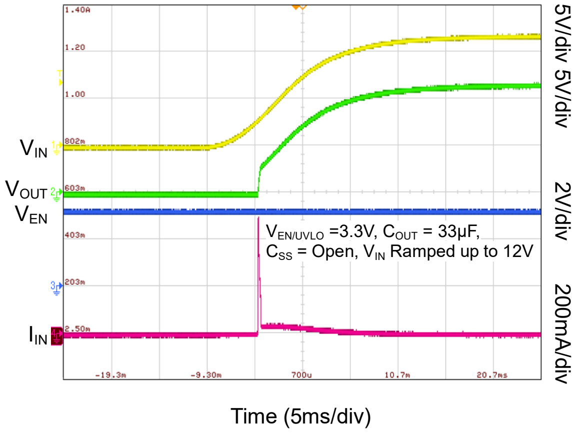
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

V_{IN} = 12V, T_A = +25℃, unless otherwise noted.

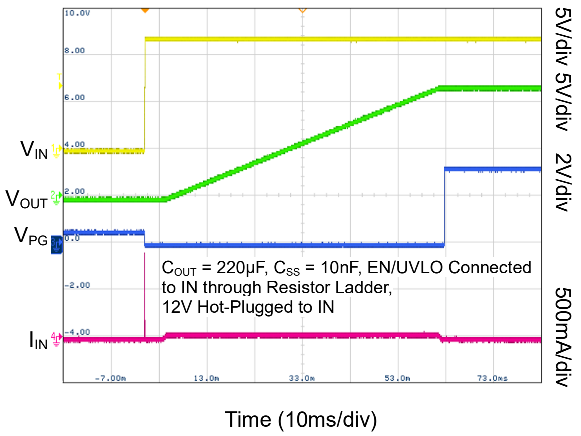
Start-Up with Enable



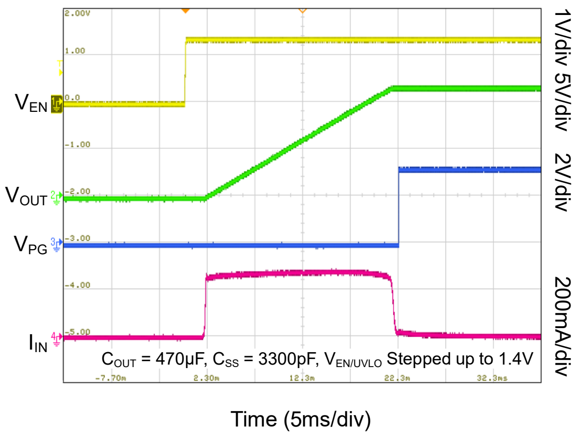
Start-Up with Supply



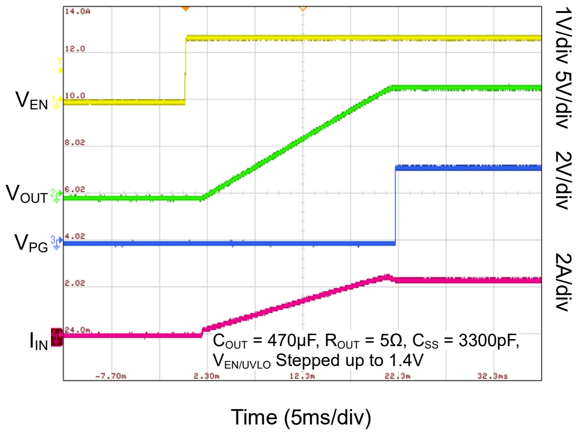
Input Hot-Plug



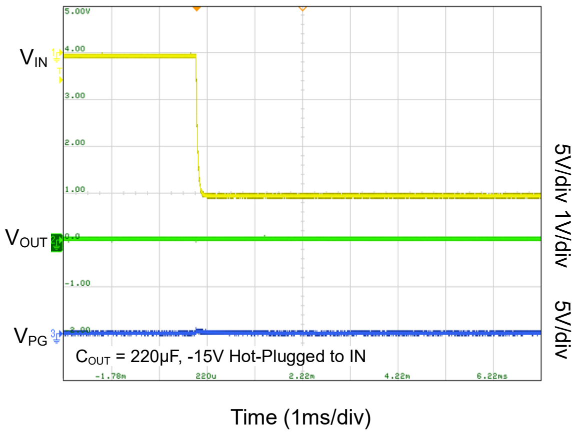
Inrush Current with Capacitive Load



Inrush Current with Resistive and Capacitive Load



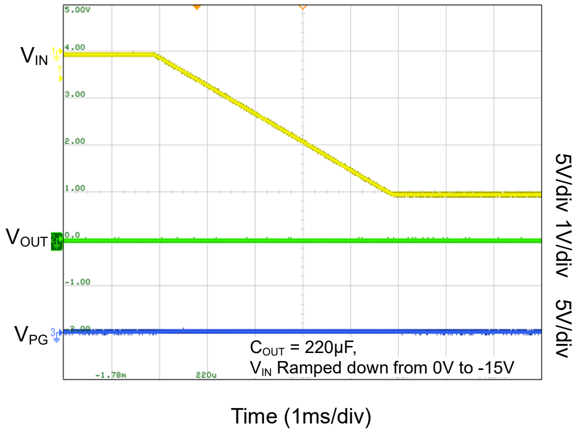
Input Reverse Polarity Protection - Fast Ramp



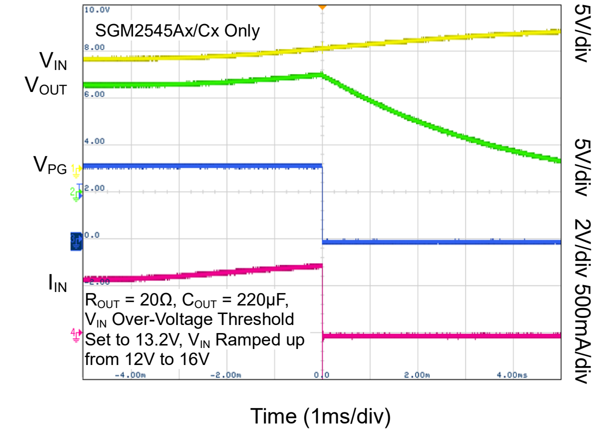
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, unless otherwise noted.

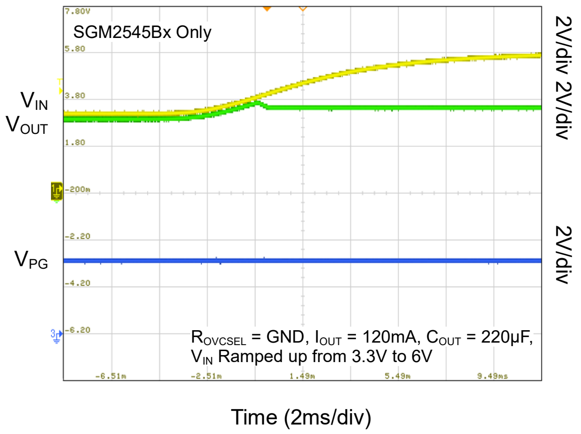
Input Reverse Polarity Protection - Slow Ramp



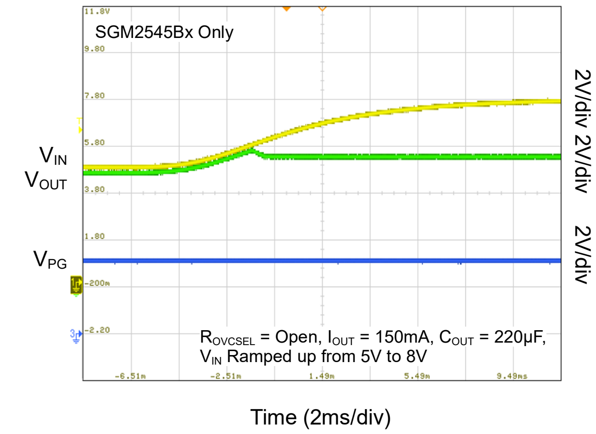
Over-Voltage Lockout Response



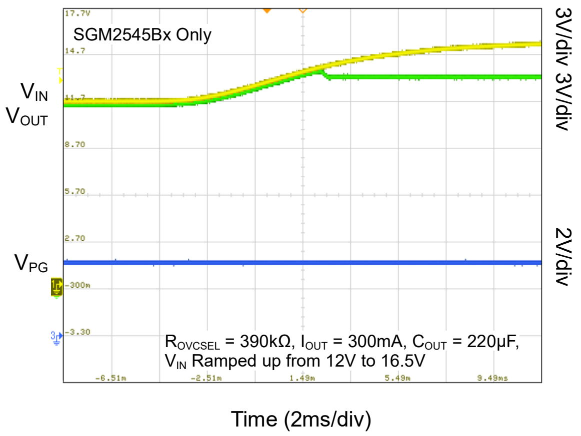
Over-Voltage Clamp Response



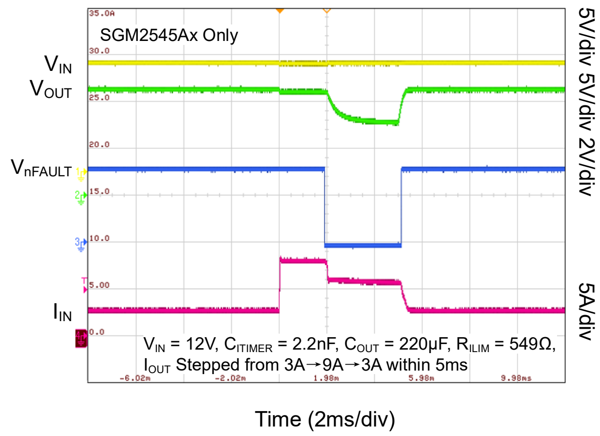
Over-Voltage Clamp Response



Over-Voltage Clamp Response



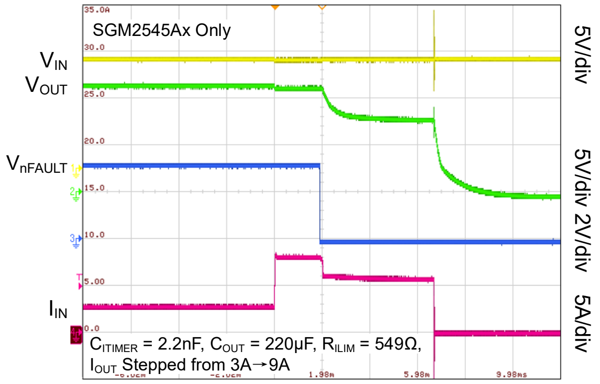
Active Current Limit Response



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

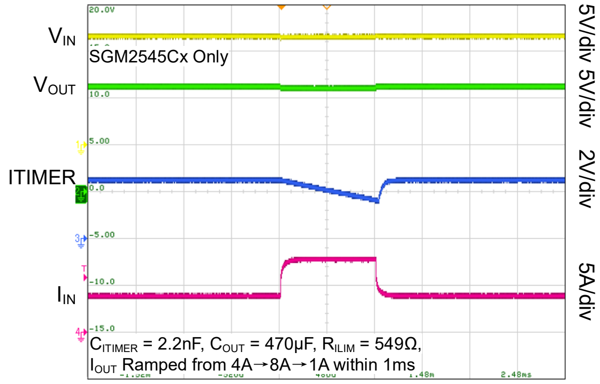
V_{IN} = 12V, T_A = +25℃, unless otherwise noted.

Active Current Limit Response Followed by TSD



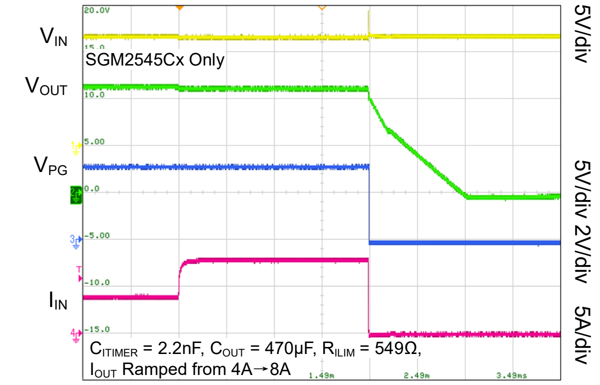
Time (2ms/div)

Transient Over-Current Blanking Timer Response



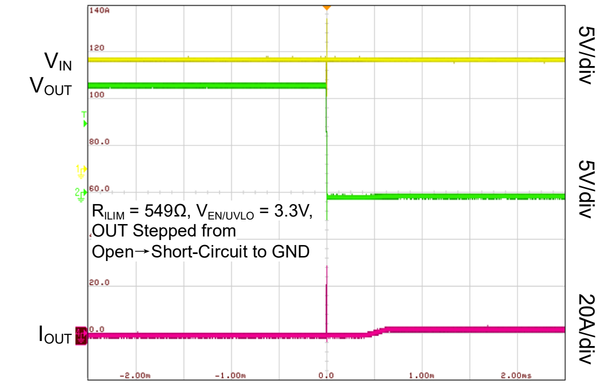
Time (500μs/div)

Circuit Breaker Response



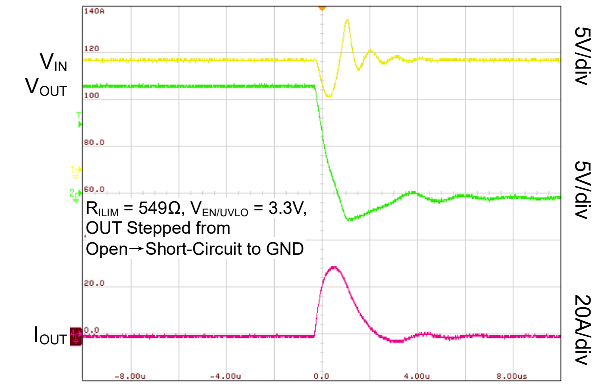
Time (500μs/div)

Output Short-Circuit During Steady State



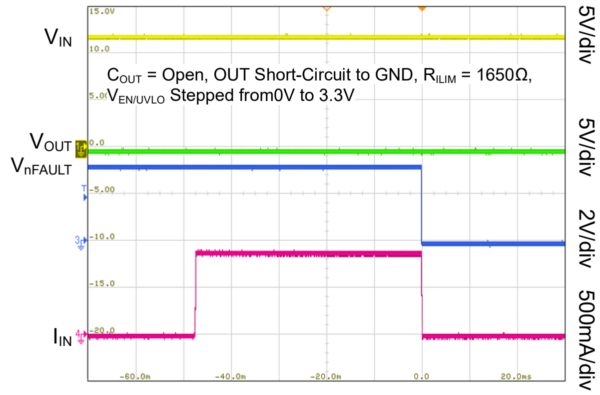
Time (500μs/div)

Output Short-Circuit During Steady State (Zoomed In)



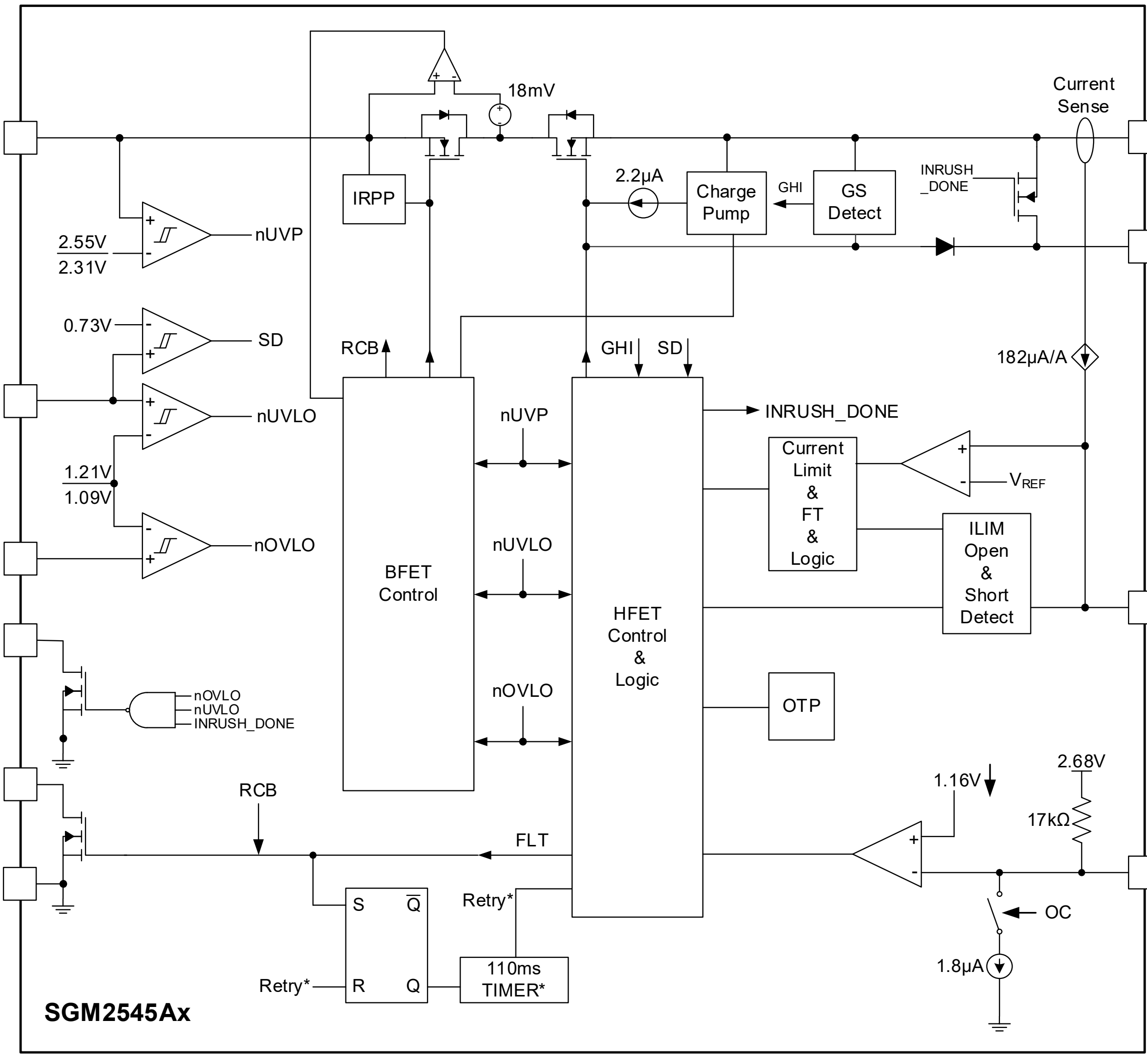
Time (2μs/div)

Power Up into Short-Circuit



Time (10ms/div)

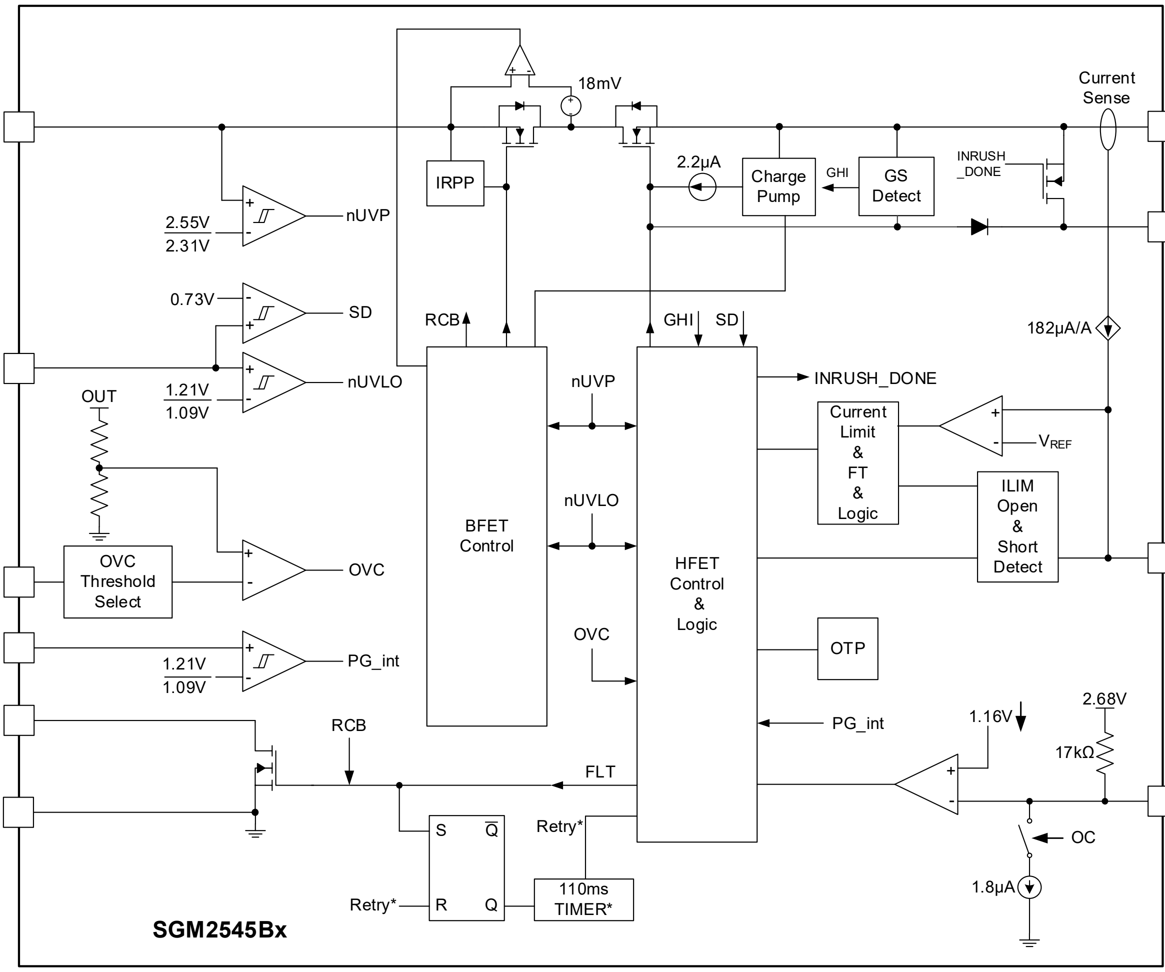
BLOCK DIAGRAMS



*: Not applied to SGM2545AL

Figure 3. SGM2545Ax Block Diagram

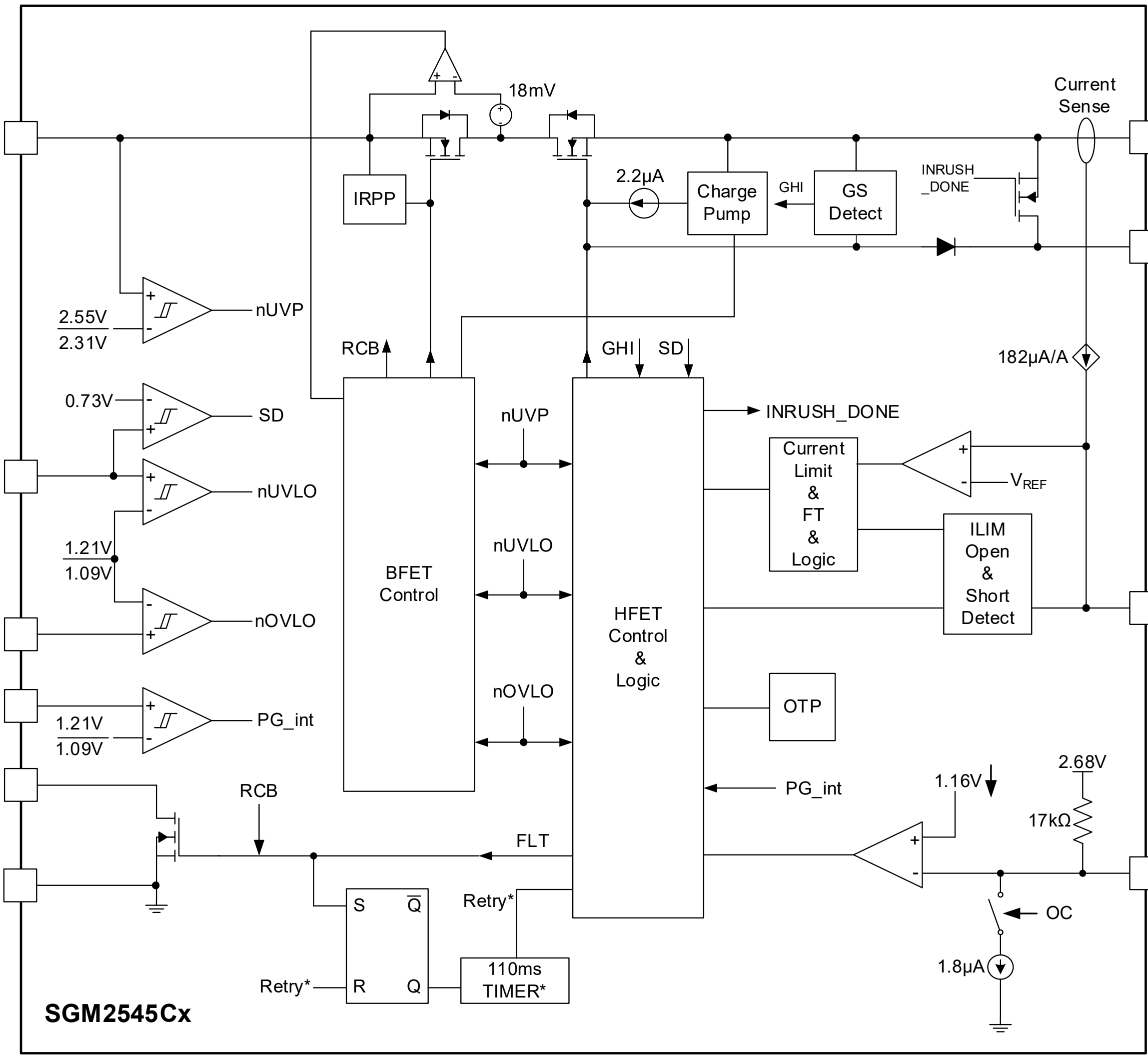
BLOCK DIAGRAMS (continued)



*: Not applied to SGM2545BL

Figure 4. SGM2545Bx Block Diagram

BLOCK DIAGRAMS (continued)



*: Not applied to SGM2545CL

Figure 5. SGM2545Cx Block Diagram

DETAILED DESCRIPTION

The SGM2545xx is an eFuse with internal integration of FET. It ensures the safety of the power delivery system due to its rich features. When the V_{IN} is greater than V_{UVP_R}, the device starts to sample the voltage of the EN/UVLO pin ($V_{EN/UVLO}$). If $V_{EN/UVLO}$ exceeds V_{UVLO_R}, the internal FET starts conducting and the current can flow from IN to OUT. When the V_{IN} is less than V_{UVP_F} or $V_{EN/UVLO}$ < V_{UVLO_F}, the internal FET is turned off. Protection against reverse input voltage is maintained by keeping the power path in the OFF state.

After device start-up, the SGM2545xx will monitor the VIN and forward current (from IN to OUT). By controlling the internal HFET, the load current is limited to the set current limit threshold (I_{LIM}). During over-voltage event, the output voltage will be clamped to the chosen threshold (V_{OVC}) or be cut-off if it exceeds the user-adjustable over-voltage lockout threshold (V_{OVLO}). The fast-trip response of the device can provide rapid protection against serious over-current during short-circuit of OUT pin, so as to prevent the system from being damaged by harmful voltage and current. In addition, the device also provides a user-adjustable over-current blanking timer to allow short-time over-current in the power path without tripping the device frequently. Therefore, SGM2545xx not only provides complete protection functions, but also ensures the maximum system uptime during transient events.

The device integrates a reverse-current-blocking FET (BFET) that functions as an ideal diode. During forward conduction, the BFET is linearly regulated to maintain a constant low forward voltage drop (V_{FWD}). If V_{OUT} exceeds V_{IN}, the BFET shuts off completely to block reverse current.

The device incorporates an integrated thermal shutdown circuit. When the junction temperature (T_J) exceeds specified operational limits, this protection circuitry automatically disables the device to prevent thermal damage.

Designed for robust system protection, the compact SGM2545xx integrates fault detection, protective responses, and status indication capabilities to safeguard power delivery during abnormal operating conditions.

Input Reverse Polarity Protection

The SGM2545 features integrated reverse-polarity protection at its input supply pin. It blocks negative voltages (down to -15V or V_{OUT} - 21V, whichever is higher) from reaching the output, safeguarding downstream circuits. No reverse current flows from output to input during such events. For signal pins connected to V_{IN} (EN/UVLO, OVLO, PGTH), use sufficiently large pull-up resistors to limit fault current. Refer to Absolute Maximum Ratings for details.

Under-Voltage Lockout (UVLO and UVP)

The SGM2545 implements under-voltage protection at IN pin to prevent IN voltage from being too low for normal operation of system and equipment. A fixed locking threshold voltage (V_{UVP}) is provided inside the device for under-voltage protection. In addition, the comparator on the EN/UVLO terminal can be used to set the user-adjustable under-voltage protection threshold through the external resistor divider. Figure 6 and Equation 1 show how to set the specific value of under-voltage protection threshold using an external resistor divider.

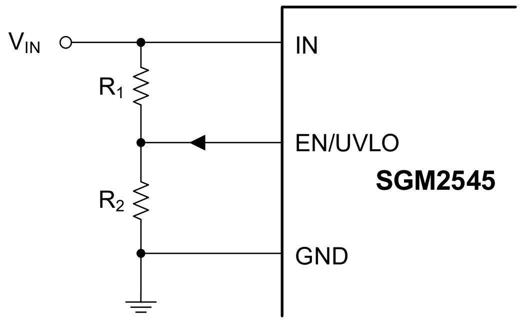


Figure 6. Adjustable Under-Voltage Protection

$$V_{IN\_UV} = \frac{V_{UVLO} \times (R_1 + R_2)}{R_2} \quad (1)$$

DETAILED DESCRIPTION (continued)

Over-Voltage Lockout (OVLO)

The SGM2545Ax/Cx implements over-voltage lockout at OVLO pin to prevent IN voltage from being too high for normal operation of system and equipment. The comparator on the OVLO pin is used to set the user-adjustable over-voltage protection threshold through the external resistor divider. If the voltage of OVLO pin exceeds the V_{OV_R}, the device will shut down the power path. When the voltage of OVLO pin is lower than the V_{OV_F}, the power path will be reopened with inrush control. There is a hysteresis between the rising threshold and falling threshold of OVLO. The Equation 2 and Figure 7 show how to set the specific value of over-voltage protection threshold using an external resistor divider.

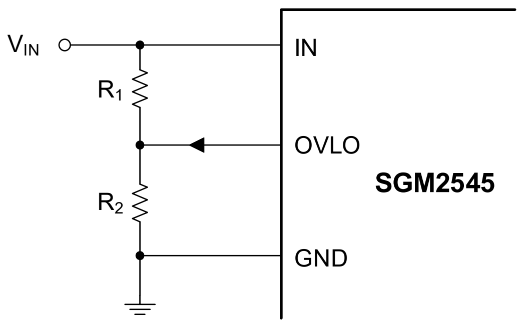


Figure 7. Adjustable Over-Voltage Protection

$$V_{IN\_OV} = \frac{V_{OV} \times (R_1 + R_2)}{R_2} \tag{2}$$

During OVLO recovery, SGM2545Ax variants accelerate restart by bypassing soft-start (SS) control. Instead, they initiate current-limited startup to minimize input voltage droop while achieving faster power-up.

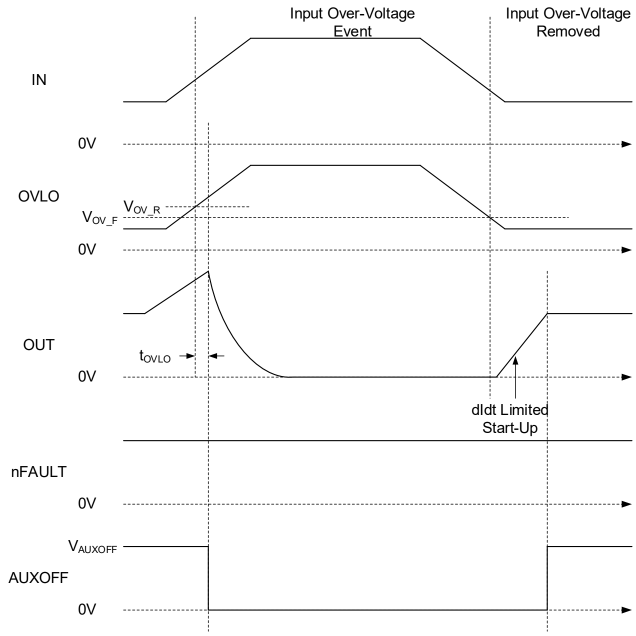


Figure 8. SGM2545Ax Over-Voltage Lockout and Recovery

While recovering from an OVLO event, the SGM2545Cx variants start up with inrush control (SS).

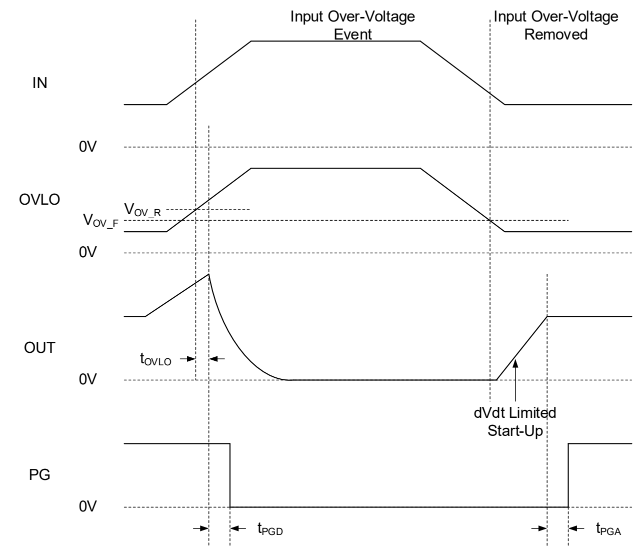


Figure 9. SGM2545Cx Over-Voltage Lockout and Recovery

Over-Voltage Clamp (OVC)

The SGM2545BR performs an output voltage clamp under input over-voltage event. When the input voltage exceeds the over-voltage clamp threshold (V_{OVC}), the device acts quickly within t_{OVC} and clamps the output voltage. During persistent input over-voltage conditions, the device linearly controls the HFET to clamp the output at or below V_{CLAMP}.

DETAILED DESCRIPTION (continued)

If the device stays in clamp state driving certain load for a long time, considerable power will be dissipated on the device, which could cause over-temperature and thermal shutdown (TSD). After thermal shutdown, SGM2545BL would stay latched off and SGM2545BR would restart automatically after a fixed delay. Device behavior during thermal shutdown is detailed in the Over-Temperature Protection (OTP) specifications.

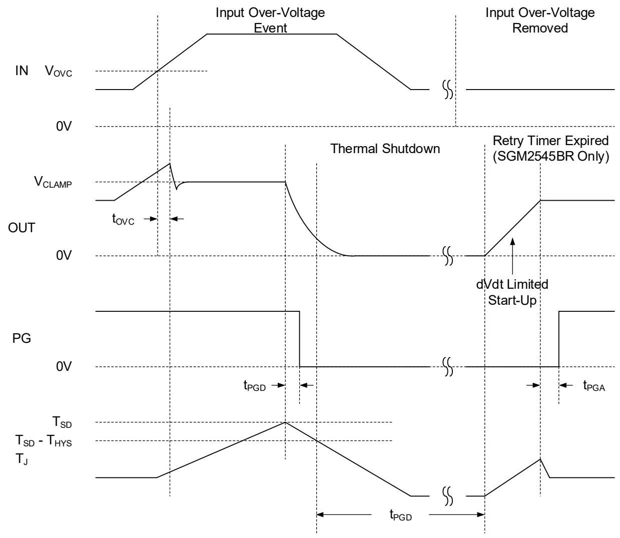


Figure 10. SGM2545Bx Over-Voltage Response (Auto-Retry)

There are 3 available over-voltage clamp threshold options which can be configured using the OVCSEL pin.

Table 1. SGM2545Bx Over-Voltage Clamp Threshold Selection

OVCSEL Pin Connection	Over-Voltage Clamp Threshold
Shorted to GND	3.91V
Open	5.82V
Connected to GND through a 390kΩ resistor	13.99V

Inrush Current, Over-Current, and Short Circuit Protection

SGM2545 adopts four levels of forward over-current protection function:

1. Programmable slew rate (SR) for inrush current protection.
2. Programmable current limit threshold (I_{LIM}) for over-current in steady state or start-up.
3. Programmable threshold (I_{SC}) for severe over-current in steady state or start-up.
4. Fixed I_{FT} for fast-trip function when short-circuit of OUT occurs.

Slew Rate (SS) and Inrush Current Control

When hot-plug or system charging large capacitive load occurs, a large inrush current is generated in the equipment power path. The input connector may be damaged or the input power rail voltage may drop, which affects the normal operation and even restarts other equipment in the system. The inrush current during turn on is directly proportional to the load capacitance and rising slew rate. For a given C_{OUT}, the relationship between the slew rate (SR) and inrush current (I_{INRUSH}) is shown in Equation 3:

$$SR(V/ms) = \frac{I_{INRUSH}(mA)}{C_{OUT}(\mu F)} \quad (3)$$

The slew rate can be controlled by connecting a capacitor at the SS pin to reduce inrush current. For a given slew rate, the corresponding C_{SS} can be calculated by Equation 4.

$$C_{SS}(pF) = \frac{2200}{SR(V/ms)} \quad (4)$$

When the SS pin is left floating, the fastest output slew rate can be obtained.

DETAILED DESCRIPTION (continued)

Circuit-Breaker

For output over-current events, the SGM2545Cx initiates output shutdown following an adjustable transient blanking period. When the load current exceeds the over-current threshold I_{LIM} (set by the resistor at ILIM pin) but lower than the fast-trip threshold (2 × I_{LIM}), the capacitor at I_{TIMER} pin CITIMER starts discharging through the internal 1.8μA pulldown current. If the load current falls below I_{LIM} before the C_{ITIMER} discharges by ΔV_{ITIMER}, the ITIMER pin is reset by re-charging C_{ITIMER} to the internal pull-up voltage V_{INT}, and the circuit-breaker action will not be activated. This action allows short load transient pulses to pass through the device without tripping the circuit. If the over-current event persists, once C_{ITIMER} discharges by ΔV_{ITIMER}, the circuit-breaker action turns off the HFET immediately. Meanwhile, C_{ITIMER} is re-charged to V_{INT} for the next over-current condition. This design ensures full blanking time is provided for every over-current fault. Equation 5 can be used to calculate the R_{ILIM} value for a desired over-current threshold.

$$R_{ILIM}(\Omega) = \frac{3338}{I_{LIM}(A)} \quad (5)$$

1. Leave the ILIM pin floating to set the over-current threshold near zero, and the device can hardly be loaded.

2. When the ILIM is short to the GND under normal operations, it will be detected as a fault case and the device shuts down. The load current should reach a minimum threshold I_{FAULT} for the device to detect LIM short pin.

The blanking time can be adjusted by changing the capacitance connected to the ITIMER pin. Over-current blanking time can be calculated by Equation 6.

$$t_{ITIMER}(ms) = \frac{\Delta V_{ITIMER}(V) \times C_{ITIMER}(nF)}{I_{ITIMER}(\mu A)} \quad (6)$$

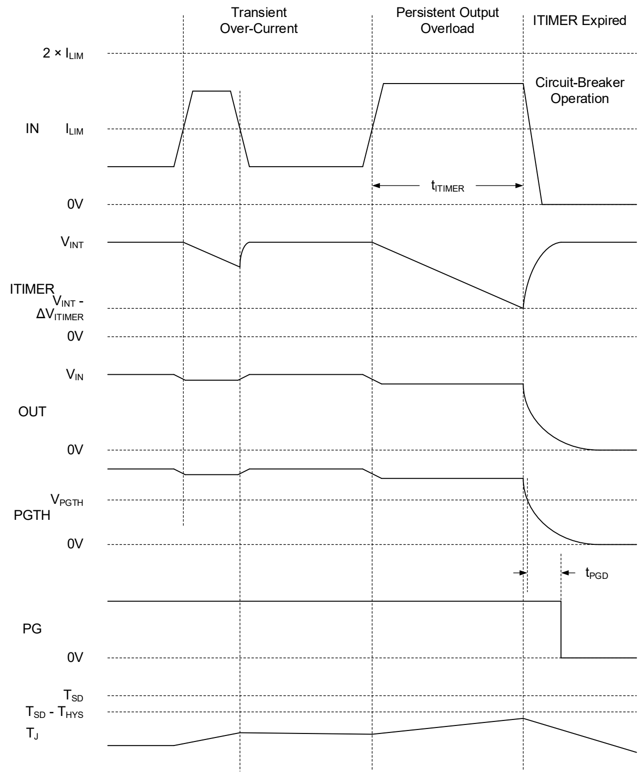


Figure 11. SGM2545Cx Over-Current Response

1. Leaving the ITIMER pin open would make the device to break the circuit with the minimum possible delay.

2. Leaving the ITIMER pin short to GND sets the minimum over-current blanking time. But it is not recommended to leave ITIMER pin short to GND, because it increases the current consumption of the device

3. Increasing C_{ITIMER} can increase the over-current blanking time, but it also increases the time for C_{ITIMER} to charge to V_{INT}. If the next over-current case occurs before the C_{ITIMER} is fully charged to the VINT, the current blanking time of this event will be shorter than intended.

After the part shuts down due to a circuit-breaker fault, the device will either be restarted automatically after a certain time interval (SGM2545CR variants) or stay latched off (SGM2545CL variants).

DETAILED DESCRIPTION (continued)

Active Current Limiting

The SGM2545Ax and SGM2545Bx implement an over-current limiting response under over-current condition. The device actively regulates the current at the current-limit threshold (I_{LIM}) after the user-programmable over-current blanking time. When the load current exceeds the over-current threshold ILIM (set by the resistor at ILIM pin) but lower than the fast-trip threshold (2 × I_{LIM}), the capacitor at ITIMER pin CITIMER starts discharging through the internal 1.8μA pulldown current. If the load current falls below I_{LIM} before the C_{ITIMER} discharges by ΔV_{ITIMER}, the ITIMER pin is reset by re-charging C_{ITIMER} to the internal pull-up voltage V_{INT}, and the current limit will not be activated. During this event, transient load spikes propagate through the device unimpeded by current limiting. If the over-current event persists, once C_{ITIMER} discharges by ΔV_{ITIMER}, the device actively limits the current at I_{LIM}. Meanwhile, C_{ITIMER} is re-charged to V_{INT} for the next over-current condition. This design ensures full blanking time is provided for every over-current fault. Use Equation 7 to calculate the R_{ILIM} value for a desired over-current threshold.

$$R_{ILIM}(\Omega) = \frac{3338}{I_{LIM}(A)} \tag{7}$$

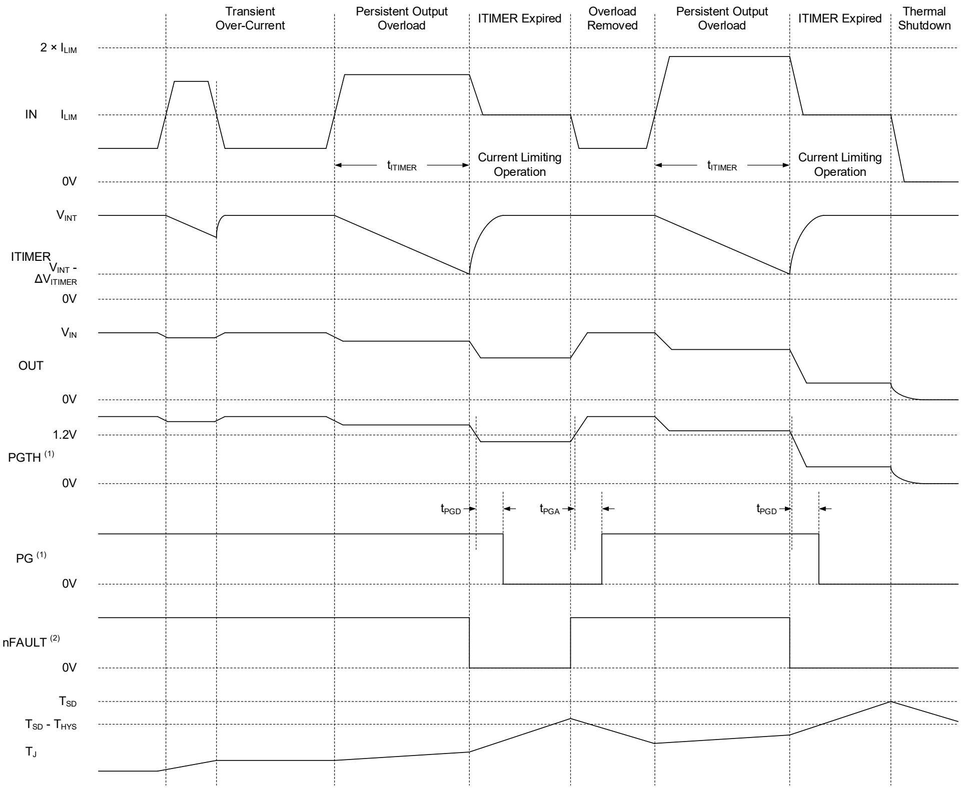
1. Leave the ILIM pin floating to set the over-current threshold near zero, and the device can hardly be loaded.

2. The current limit circuit implements the fold-back mechanism. In the fold-back region (0V < V_{OUT} < V_{FB}), the current limit threshold is smaller than the current limit threshold (I_{LIM}) under steady state.

3. When the ILIM is short to the GND under normal operations, it will be detected as a fault case and the device shuts down. The load current should reach a minimum threshold I_{FAULT} for the device to detect LIM short pin.

The blanking time can be adjusted by changing the capacitance connected to the ITIMER pin. Over-current blanking time can be calculated by Equation 8.

$$t_{ITIMER}(ms) = \frac{\Delta V_{ITIMER}(V) \times C_{ITIMER}(nF)}{I_{ITIMER}(\mu A)} \tag{8}$$



NOTES:

1. Applicable only to SGM2545Bx and SGM2545Cx variants
2. Applicable only to SGM2545Ax variants

Figure 12. SGM2545Ax and SGM2545Bx Active Current Limit Response

DETAILED DESCRIPTION (continued)

1. Leaving the ITIMER pin open would make the device to limit the circuit with the minimum possible delay.

2. Leaving the ITIMER pin short to GND sets the minimum over-current blanking time. But it is not recommended to leave ITIMER pin short to GND, because it increases the current consumption of the device

3. The active current limit set by R_{ILIM} is still valid for SGM2545Ax and SGM2545Bx (active current limit) and SGM2545Cx (circuit-breaker) during start-up, which ensures that the load current does not exceed ILIM during start-up. However, there is no over-current blanking time in the start-up process.

4. For the SGM2545Bx, during over-voltage clamp condition, if an over-current event occurs, the current limit is activated immediately without the ITIMER delay.

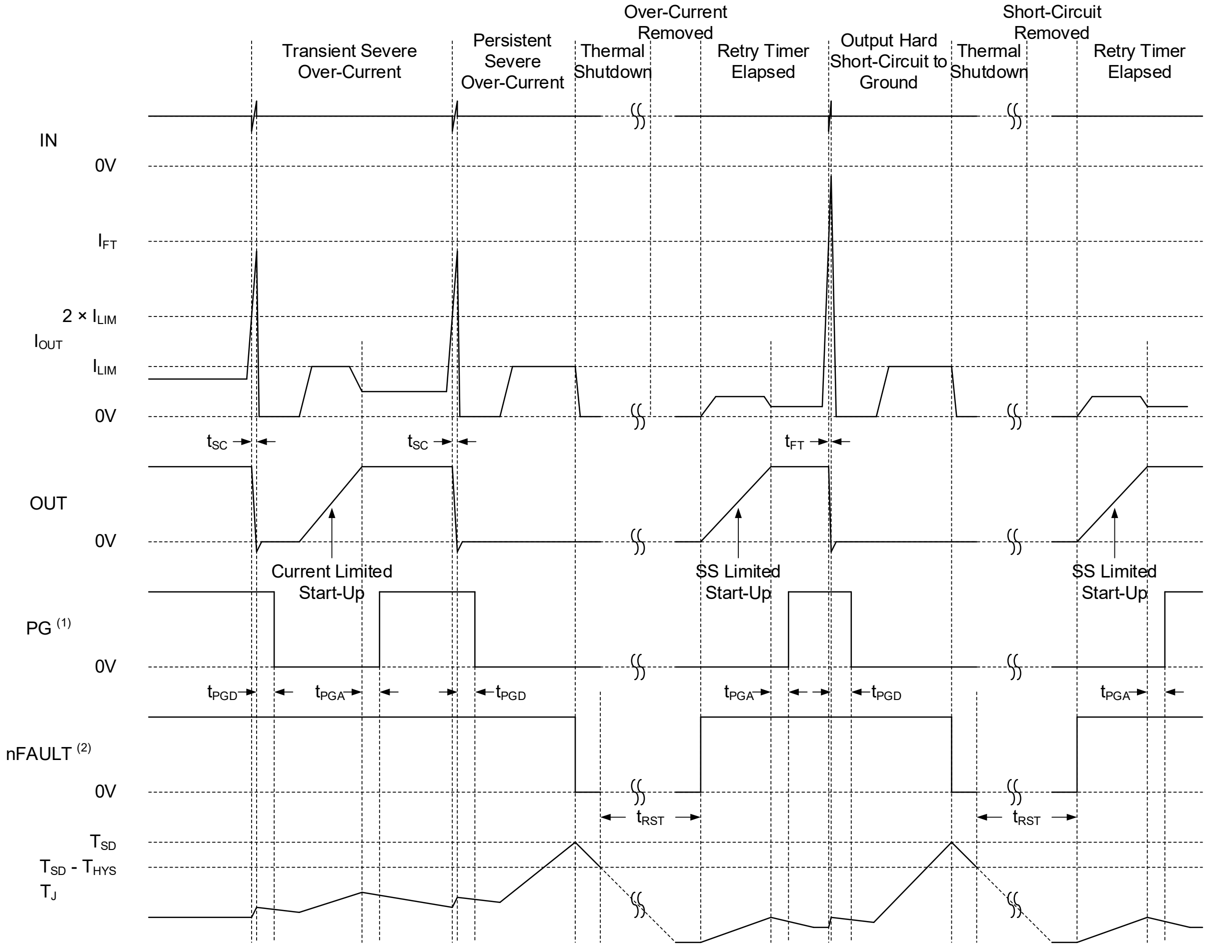
5. Increasing C_{ITIMER} can increase the over-current blanking time, but it also increases the time for C_{ITIMER} to charge to V_{INT}. If the next over-current case occurs before the C_{ITIMER} is fully charged to the V_{INT}, the current blanking time of this event will be shorter than intended.

During the active current limit, there is more power dissipation on the internal HFET because the output voltage drops. If the internal temperature of the device exceeds the TSD, the internal HFET will be turned off, and the device will either be restarted automatically after a certain time interval (SGM2545xR variants) or stay latched off (SGM2545xL variants). Device behavior during thermal shutdown is detailed in the Over-Temperature Protection (OTP) specifications.

Short-Circuit Protection

When a serious over-current event similar to a short-circuit event occurs, the SGM2545 triggers a fast-trip response to prevent the system from being damaged by excessive current flowing through the device. A fast-trip comparator with scalable threshold (I_{SC} = 2 × I_{LIM}) is adopted inside the device, which allows users to program the fast-trip threshold in low current system. A fixed fast-trip threshold is also set inside the device for fast protection against hard short-circuit events in steady state. The fixed fast-trip threshold is higher than the maximum fast-trip threshold configured by user within the recommended operating range. The internal HFET will be completely turned off within t_{FT} if the current exceeds I_{FT} or I_{SC}. Then the device will turn on the internal FET again after a short of deglitch time (30μs) in a current limit mode instead of a SS limited manner. In this way, the rapid recovery of internal HFET can be realized after a transient severe over-current event, and the drop of OUT voltage can be minimized. Device behavior during thermal shutdown is detailed in the Over-Temperature Protection (OTP) specifications.

DETAILED DESCRIPTION (continued)



NOTES:

1. Applicable only to SGM2545Bx and SGM2545Cx variants
2. Applicable only to SGM2545Ax variants
3. Applicable only to SGM2545xR variants

Figure 13. SGM2545xx Short-Circuit Response

Analog Load Current Monitor

The device provides an analog current sensing output proportional to the load current at the ILIM pin, which enables the device to monitor the load current (from IN to OUT). The user can calculate the load current through the voltage of the ILIM pin connected to the R_{ILIM}. The relationship between V_{ILIM} and I_{OUT} is shown in Equation 9.

$$I_{OUT}(A) = \frac{V_{ILIM}(\mu V)}{R_{ILIM}(\Omega) \times G_{IMON}(\mu A / A)} \quad (9)$$

The waveform below shows the analog load current monitor response to a load step at the output.

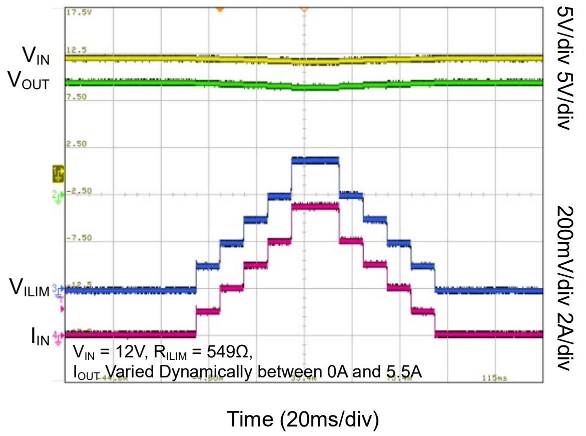


Figure 14. Analog Load Current Monitor Response

ILIM pin is sensitive to capacitive loads. In order to ensure the normal operation of the device, the parasitic capacitance of the ILIM pin needs to be less than 50pF.

DETAILED DESCRIPTION (continued)

Reverse Current Protection

The device operates as an ideal diode, preventing any reverse current from flowing from the OUT to IN terminal under all operating conditions. It incorporates integrated back-to-back MOSFETs arranged in a shared drain configuration. The voltage drop across the IN and OUT pins is continuously monitored, and the gate drive of the blocking FET (BFET) is dynamically adjusted to maintain the forward voltage drop at a set level, V_{FWD}. This closed-loop regulation method, known as linear ORing control, allows for smooth MOSFET turn-off during reverse current situations and guarantees the absence of DC reverse current conduction.

The device further incorporates a traditional comparator-based reverse current suppression system (V_{REVTH}) to enable accelerated reaction (t_{RCB}) against transient reverse currents. Upon activating reverse current protection, the system delays recovery until the forward voltage differential (V_{IN} minus V_{OUT}) surpasses the V_{FWDTH} threshold, subsequently executing rapid restoration to full operational conductivity. This mechanism introduces a robust hysteresis effect to eliminate interference from power supply fluctuations or electrical noise on the protective response. The reactivation process from reverse current blocking exhibits exceptional speed (t_{SWRCB}), effectively mitigating voltage sag in critical implementations including supply MUXing/ORing and USB Fast Role Swap (FRS).

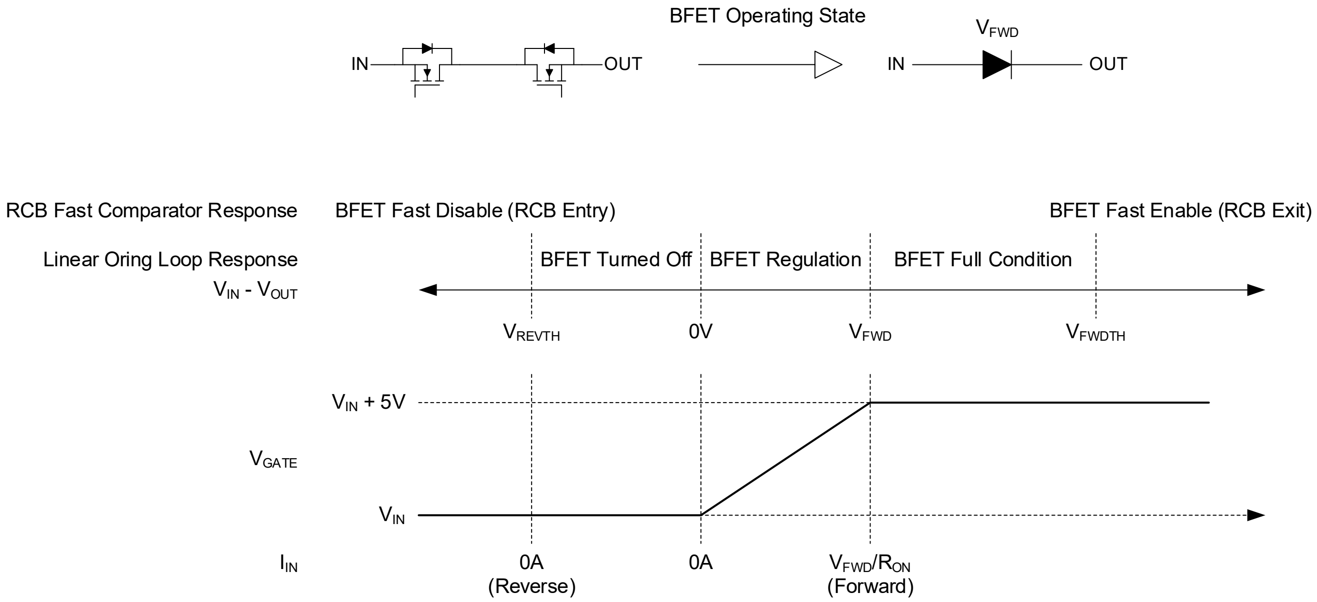


Figure 15. Reverse Current Blocking Response

The waveforms below demonstrate the reverse current blocking performance across different operating conditions.

When encountering rapid output voltage transients (such as hot-plug events), the rapid-response comparator-driven protection system maintains input stability by preventing significant voltage spikes or transient disturbances.

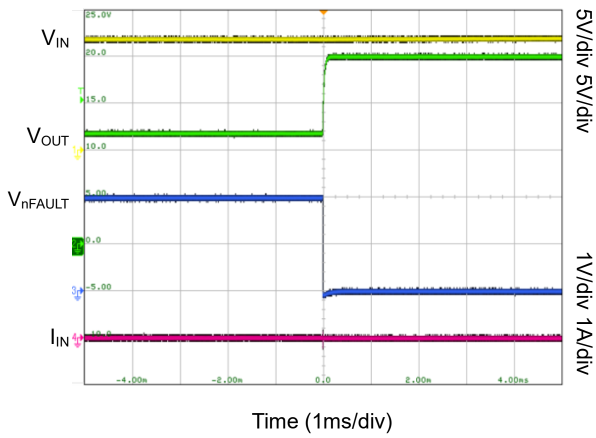


Figure 16. Reverse Current Blocking Performance during Fast Voltage Step at Output

DETAILED DESCRIPTION (continued)

When output voltages increase gradually, the linear ORing control architecture prevents DC reverse current conduction and maintains isolation between input and output terminals, effectively preventing input rail from getting slowly charged up by output voltage.

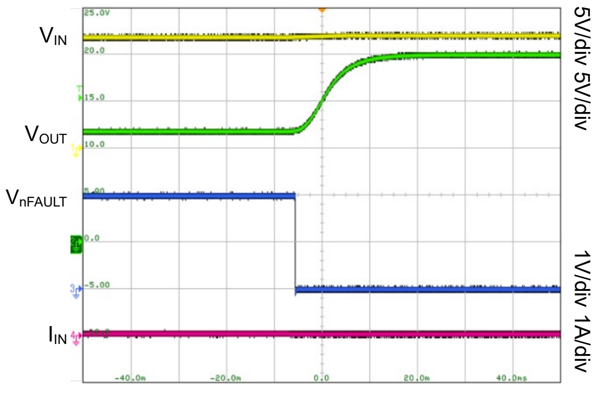


Figure 17. Reverse Current Blocking Performance during Slow Voltage Ramp at Output

The linear ORing configuration effectively suppresses reverse discharge pathways when input power becomes unavailable while energy storage components at output (such as bulk capacitors or super capacitors) remain at full charge potential. This operational principle optimizes energy preservation in reserve power systems by significantly reducing backward current transmission from output to input ports, thereby extending discharge latency periods for critical energy storage elements in during emergencies or power failures.

This feature also stops false power connection alerts in systems that sense input voltage to confirm whether an energy source remains properly connected.

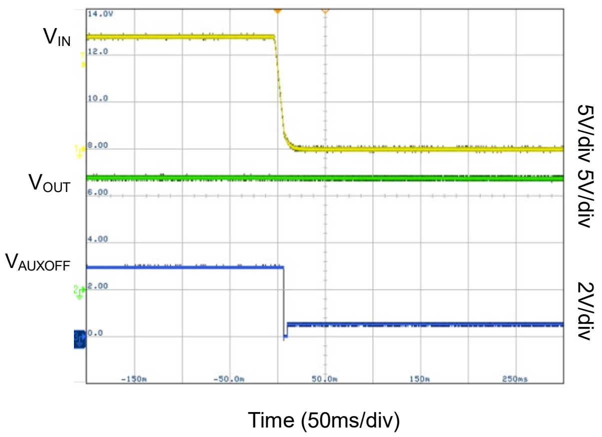


Figure 18. Reverse Current Blocking Performance during Input Supply Failure

Over-Temperature Protection (OTP)

The SGM2545 continuously monitors the temperature (T_J) of the internal die. Once the internal temperature exceeds the T_{SD}, the device shuts down immediately. The SGM2545 will not turn on until the internal temperature is lower than a safe threshold (T_{SD} - T_{HYS}).

When SGM2545xL (latch-off variant) triggers the thermal shutdown, it shuts down and remains latched-off until V_{IN} power cycle or external reset. When SGM2545xR (auto-retry variant) triggers the thermal shutdown, it remains in the shutdown state until the internal temperature of the equipment drops by T_{HYS}. After that, it will retry to turn on automatically after a t_{RST} delay time if the device is still enabled.

Table 2. Thermal Shutdown

DEVICE	ENTER TSD	EXIT TSD
SGM2545xL (Latch-Off)	$T_J \geq T_{SD}$	$T_J < T_{SD} - T_{HYS}$ V_{IN} cycled to 0V and then above V_{UVP_R} OR EN/UVLO toggled below V_{SD_F}
SGM2545xR (Auto-Retry)	$T_J \geq T_{SD}$	$T_J < T_{SD} - T_{HYS}$ V_{IN} cycled to 0V and then above V_{UVP_R} or EN/UVLO toggled below V_{SD_F} or t_{RST} timer expired

Fault Response and Indication (nFAULT)

Table 3 shows the protection response of equipment under different fault conditions. The SGM2545Ax provides an active-low external fault flag pin.

DETAILED DESCRIPTION (continued)

Table 3. Fault Summary

EVENT	PROTECTION RESPONSE	FAULT LATCHED INTERNALLY	nFAULT PIN STATUS (1)	nFAULT ASSERTION DELAY (1)
Over-Temperature	Shutdown	Y	L	
Under-Voltage (UVP or UVLO)	Shutdown	N	H	
Input Reverse Polarity	Shutdown	N	H	
Input Over-Voltage	Shutdown (1)(2)	N	H	
	Voltage Clamp (2)	N	N/A	
Transient Over-Current (I_{LIM} < I_{OUT} < 2 × I_{LIM})	None	N	N	
Persistent Over-Current	Circuit-Breaker (3)	Y	N/A	
Persistent Over-Current	Current Limit (4)	N	L	t_{ITIMER}
Output Short-Circuit to GND	Circuit-Breaker followed by Current Limit	N	H	
ILIM Pin Open (During Steady State)	Shutdown	N	L	
ILIM Pin Shorted to GND	Shutdown	Y	L	
Reverse Current (V_{OUT} - V_{IN} > V_{REVTH})	Reverse Current Blocking	N	L	

NOTES:

1. Applicable to SGM2545Ax variants only.
2. Applicable to SGM2545Bx variants only.
3. Applicable to SGM2545Cx variants only.
4. Applicable to SGM2545Ax and SGM2545Bx variants only.

An internally latched fault can be cleared by power cycling (pulling V_{IN} to 0V) or re-enable (pulling EN/UVLO pin below V_{SD}). This will reset the nFAULT pin for the SGM2545Ax and the t_{RST} timer for the SGM2545xR (auto-retry).

During a latched fault, pulling the EN/UVLO just below the UVLO threshold cannot clear the latched fault. This applies equally to both SGM2545xL (latch-off) and SGM2545xR (auto-retry).

After the retry delay t_{RST}, the SGM2545xR (auto-retry) restarts automatically and the nFAULT pin is released (SGM2545AR).

Auxiliary Channel Control (AUXOFF)

The SGM2545Ax features an active-high AUXOFF signal. This output asserts when:

- Priority input voltage is within UVLO-to-OVLO range
- Inrush current sequencing is complete

The AUXOFF with open-drain output requires an external pull-up resistor to an external voltage rail

At the initial stage of power-on, AUXOFF is pulled down. Then the device enters the start-up sequence, in which the internal HFET has been controlled and not fully conductive. When the gate voltage of the internal HFET reaches overdrive, it is fully conductive and the start-up sequence is completed, the AUXOFF pin is asserted high. AUXOFF de-assertion occurs **exclusively** when the input supply becomes invalid (V_{IN} < UVLO or V_{IN} > OVLO). Load-side conditions **do not influence** this de-assertion.

This pin serves to manage the auxiliary channel when two SGM2545Ax devices are configured in a priority-based power multiplexer setup. Additionally, it can function as an indicator of supply validity for the downstream load or system controller.

DETAILED DESCRIPTION (continued)

Table 4. SGM2545Ax AUXOFF Indication Summary

Event	AUXOFF Pin
Under-Voltage (UVP or UVLO)	L
Input Reverse Polarity	L
Over-Voltage (OVLO)	L
Inrush	L
Steady State	H
Over-Current	H
Short-Circuit	H
ILIM Pin Open	H
ILIM Pin Shorted to GND	H
Reverse Current (V_{OUT} - V_{IN} > V_{REVTH})	H
Over-Temperature	H

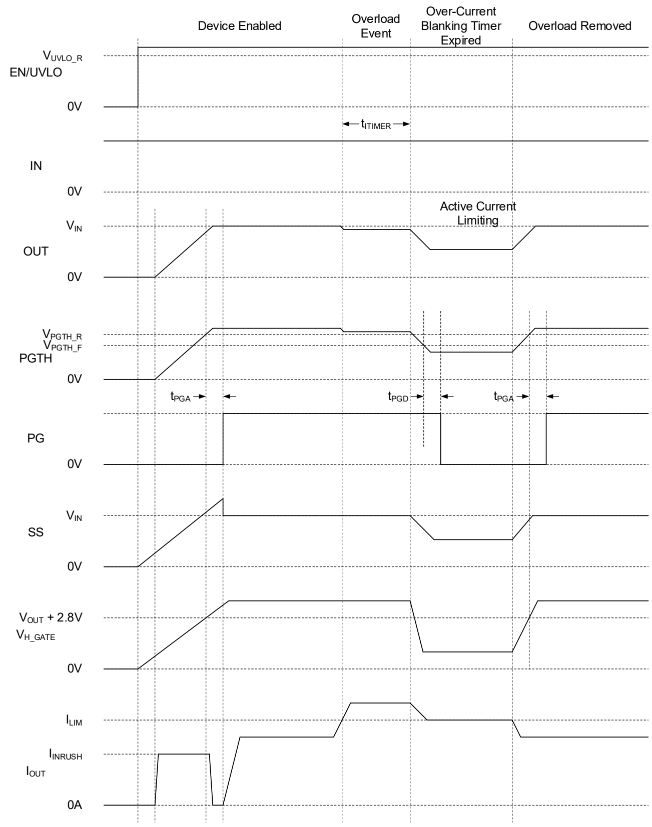
When the device is not powered, the AUXOFF pin should be low. However, there is no effective power supply to drive the AUXOFF pin down to GND in this case. If the AUXOFF is pulled up by an independent power supply and the device is not powered, there may be a small voltage on the AUXOFF caused by sink current, which is a function of the pull-up supply and pull-up resistance connected to the AUXOFF. In order to avoid the small voltage on the AUXOFF pin being detected as logic high by the external related circuit, the sink current of the pin should be minimized. This also ensures that in the priority power multiplexing configuration, the auxiliary channel will not be accidentally shut down.

Power-Good Indication (PG)

The SGM2545Bx and SGM2545Cx provide an active-high open-drain output (PG) as the indication pin of power good. It is asserted as high according to the PGTH pin voltage and the device working state. PG pin needs to be pulled up to an external power supply.

At the initial stage of power-on, PG is pulled down. Then the device enters the start-up sequence, in which the internal HFET has been controlled and not fully conductive. When the gate voltage of the internal HFET reaches overdrive, it is fully conductive and the start-up sequence is completed, V_{PGTH} is higher than V_{PGTH_R}, and PG is asserted high after a deglitch time (t_{PGA}).

The PG will be de-asserted when the PGTH voltage falls below V_{PGTH_F} or when the system has some faults. The deglitch time is t_{PGD}, when PG is de-asserted.



NOTES:

1. Applicable to SGM2545Bx only.

Figure 19. SGM2545Bx/Cx PG Timing Diagram

DETAILED DESCRIPTION (continued)

Table 5. SGM2545Bx and SGM2545Cx PG Indication Summary

EVENT	DEVICE STATUS	PG PIN STATUS	PG PIN TOGGLE DELAY
Under-Voltage UVP or UVLO)	Shutdown	L	
Input Reverse Polarity	Shutdown	L	
Over-Voltage (OVC) (SGM2545Bx only)	Clamp	H (If PGTH pin voltage > V_{PGTH_R}) L (If PGTH pin voltage < V_{PGTH_F})	t_{PGA} t_{PGD}
Over-Voltage (OVLO) (SGM2545Cx only)	Shutdown	L	t_{PGD}
Steady State	N/A	H (If PGTH pin voltage > V_{PGTH_R}) L (If PGTH pin voltage < V_{PGTH_F})	t_{PGA} t_{PGD}
Transient Over-Current	N/A	H (If PGTH pin voltage > V_{PGTH_R}) L (If PGTH pin voltage < V_{PGTH_F})	t_{PGA} t_{PGD}
Persistent Overload (SGM2545Bx Only)	Current Limiting	H (If PGTH pin voltage > V_{PGTH_R}) L (If PGTH pin voltage < V_{PGTH_F})	t_{PGA} t_{PGD}
Persistent Overload (SGM2545Cx Only)	Shutdown	L	t_{PGD}
Output Short-Circuit to GND	Fast-Trip Followed by Current Limit	H (If PGTH pin voltage > V_{PGTH_R}) L (If PGTH pin voltage < V_{PGTH_F})	t_{PGA} t_{PGD}
ILIM Pin Open	Shutdown	H (If PGTH pin voltage > V_{PGTH_R}) L (If PGTH pin voltage < V_{PGTH_F})	t_{PGA} t_{PGD}
ILIM Pin Shorted to GND & I_{OUT} > 1.1A	Shutdown	H (If PGTH pin voltage > V_{PGTH_R}) L (If PGTH pin voltage < V_{PGTH_F})	t_{PGA} t_{PGD}
Reverse Current (V_{OUT} - V_{IN} > V_{REVTH})	Reverse Current Blocking	L	t_{PGD}
Over-Temperature	Shutdown	L	t_{PGD}

When the device is not powered, the PG pin should be low. However, there is no effective power supply to drive the PG pin down to GND in this case. If the PG is pulled up by an independent power supply and the device is not powered, there may be a small voltage on the PG caused by sink current, which is a function of the pull-up supply and pull-up resistance connected to the PG. In order to avoid the small voltage on the PG pin being detected as logic high by the external related circuit, the sink current of the pin should be minimized.

Device Functional Modes

The SGM2545Ax and SGM2545Cx have only one functional mode within the recommended operating conditions.

The SGM2545Bx have three different functional modes depending on the OVCSEL pin connection.

Table 6. SGM2545Bx Over-Voltage Clamp Threshold Selection

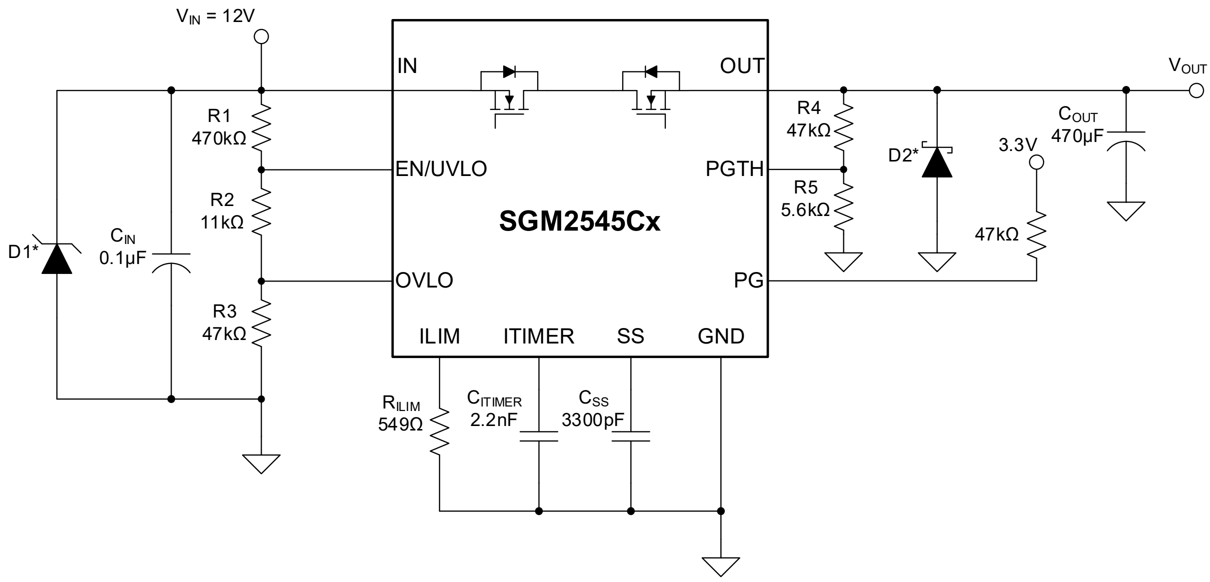
OVCSEL Pin Connection	Over-Voltage Clamp Threshold
Shorted to GND	3.91V
Open	5.82V
Connected to GND through a 390kΩ Resistor	13.99V

APPLICATION INFORMATION

The information in the following application section is not within the scope of SGMICRO's device specifications. SGMICRO does not guarantee the accuracy and completeness of this information. The customers of SGMICRO are responsible for determining whether the devices are suitable for their applications. The client should verify and test their design to ensure the functionality of the system.

Typical Application

The SGM2545 is suitable for implementing input power protection in PCIe card applications. A standard ×16 graphics card may consume up to 5.5A from a +12V supply (66W power draw), while a typical PCIe slot supports currents of up to 6A. Under load-side overcurrent or short-circuit conditions, the SGM2545Cx rapidly reacts by disabling the output, thereby safeguarding connected components and preventing voltage sag at the input. Its ITIMER functionality permits brief current spikes to pass without activating overcurrent protection, complying with the transient load requirements of modern graphics processors.



* Supplementary circuit elements for transient protection may be required, with their necessity determined by the specific input and output inductance values. Detailed guidelines are provided in the Transient Protection section.

Figure 20. PCIe Card Input Power Protection

Design Requirements

Table 7. Design Parameters

PARAMETER	VALUE
Input Supply Voltage (V_{IN})	12V
Under-Voltage Threshold (V_{IN_UV})	10.8V
Over-Voltage Threshold (V_{IN_OV})	13.2V
Output Power-Good Threshold (V_{PG})	11.4V
Max Continuous Current	5.5A
Load Transient Blanking Interval (t_{ITIMER})	2ms
Output Capacitance (C_{OUT})	470µF
Output Rise Time (t_R)	20ms
Over-Current Threshold (I_{LIM})	6A
Over-Current Response	Circuit-Breaker
Fault Response	Latch-Off

Detailed Design Procedure

Device Selection

This application requires circuit-breaker response to over-current with latch-off response after a fault, so the SGM2545CL variant was selected in accordance with the SELECTABLE MODEL guidelines.

Setting Under-Voltage and Over-Voltage Thresholds

Resistors R1, R2, and R3 determine the supply's under-voltage and over-voltage thresholds, with their values derived from Equation 10 and Equation 11:

$$V_{IN\_UV} = \frac{V_{UVLO\_R} \times (R1 + R2 + R3)}{R2 + R3} \quad (10)$$

$$V_{IN\_OV} = \frac{V_{OV\_R} \times (R1 + R2 + R3)}{R3} \quad (11)$$

APPLICATION INFORMATION (continued)

Resistors R1, R2, and R3 establish both the under-voltage (UVLO_R) and over-voltage (OVLO_R) rising thresholds. Since these resistors draw current from the input supply (V_{IN}), their selection must account for permissible leakage current. The combined current through these resistors is calculated as $I_{R123} = V_{IN}$ / (R1 + R2 + R3). Note that leakage currents from external active components connected to this resistor network may introduce inaccuracies in these calculations. Therefore, the current through the resistor string (I_{R123}) should be designed to exceed the anticipated leakage current at the EN/UVLO and OVLO pins by a factor of 20.

Based on the device's technical specifications, the maximum leakage current for both the EN/UVLO and OVLO pins is 0.9μA (MAX), while the rising thresholds for OVLO and UVLO are both 1.21V. Per the design requirements, the over-voltage input (V_{IN_OV}) is set to 13.2V and the under-voltage input (V_{IN_UV}) to 10.8V. To determine the resistor values, start by assigning R1 as 470kΩ, then utilize the provided equations to calculate R2 as 10.7kΩ and R3 as 48.5kΩ.

Using the closest standard 1% resistor values, we get R1 = 470kΩ, R2 = 11kΩ, and R3 = 47kΩ.

Setting Output Voltage Rise Time (t_R)

To achieve a reliable design, the junction temperature of the device must remain under the absolute maximum specified limit during both transient (startup) and steady-state operation. Dynamic power dissipation during startup is typically an order of magnitude higher than under static conditions, making it critical to calculate the optimal startup time and inrush current limit relative to the system capacitance to prevent thermal shutdown during initialization.

The required slew rate (SR) to obtain the target output rise time is determined by the formula:

$$SR(V/ms) = \frac{V_{IN}(V)}{t_R(ms)} = \frac{12V}{20ms} = 0.6V/ms \quad (12)$$

The value of C_{SS} required to attain the specified slew rate is derived from the following formula:

$$C_{SS}(pF) = \frac{2200}{SR(V/ms)} = \frac{2200}{0.6} = 3666pF \quad (13)$$

Choose the nearest standard capacitor value as 3600pF.

Based on the specified slew rate, the corresponding inrush current can be determined using the formula:

$$I_{INRUSH}(mA) = SR(V/ms) \times C_{OUT}(\mu F) = 0.6 \times 470 = 282mA \quad (14)$$

The average power dissipated within the component during inrush conditions is determined by the following equation:

$$PD_{INRUSH}(W) = \frac{I_{INRUSH}(A) \times V_{IN}(V)}{2} = \frac{0.282 \times 12}{2} = 1.69W \quad (15)$$

To ensure reliable startup, the thermal shutdown time of the device must surpass the ramp-up time t_R under the specified power dissipation conditions. According to *Time to T_{SD} vs. Power Dissipation (Inrush State)*, which outlines the thermal shutdown limit, the shutdown time exceeds 10 seconds for a power of 1.69W, significantly longer than the t_R value of 20ms. Consequently, a startup time of 20ms is considered safe for this application.

Setting Power-Good Assertion Threshold

The resistors R4 and R5 connected to the PGTH pin determine the Power-Good assertion threshold, with their values derived from the formula:

$$V_{PG} = \frac{V_{PGTH\_R} \times (R4 + R5)}{R5} \quad (16)$$

To minimize leakage current from the output rail VOUT, resistors R4 and R5 must be carefully selected, as they draw current from the supply. The current through these resistors is defined as $I_{R45} = V_{OUT}$ / (R4 + R5). Note that external active components attached to this network may introduce additional leakage, potentially affecting calculation accuracy. Therefore, to ensure precision, the current through the resistor string (I_{R45}) should be set to a value at least 20 times larger than the anticipated leakage current at the PGTH pin.

APPLICATION INFORMATION (continued)

Based on the device specs, the PGTH leakage current is 1.5μA (max), with a rising threshold voltage (V_{PGTH_R}) of 1.21V. The design requires V_{PG} = 11.4V. To compute the values, begin by setting R4 to 47kΩ, which yields R5 = 5.58kΩ. The nearest 1% standard value is R5 = 5.6kΩ.

Setting Over-Current Threshold (I_{LIM})

The over-current protection threshold (Circuit-Breaker) is programmed through the R_{ILIM} resistor value, determined by the following equation:

$$R_{ILIM}(\Omega) = \frac{3338}{I_{LIM}(A)} = \frac{3338}{6A} = 555.3\Omega \quad (17)$$

Choose nearest 1% standard resistor value as 549Ω.

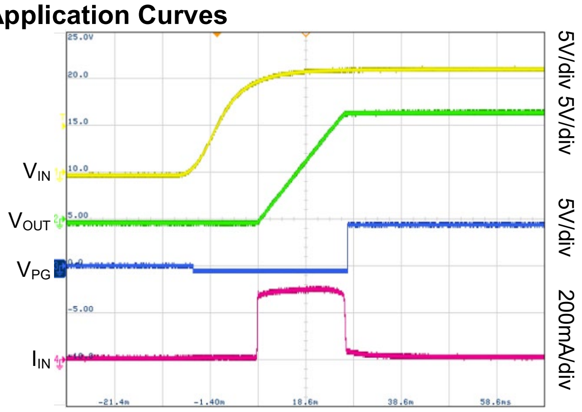
Setting Over-Current Blanking Interval (t_{ITIMER})

The C_{ITIMER} capacitor value determines the over-current blanking time interval, calculated as follows:

$$C_{ITIMER}(nF) = \frac{t_{ITIMER}(ms) \times I_{ITIMER}(\mu A)}{\Delta V_{ITIMER}(V)} = \frac{2 \times 1.8}{1.52} = 2.37nF \quad (18)$$

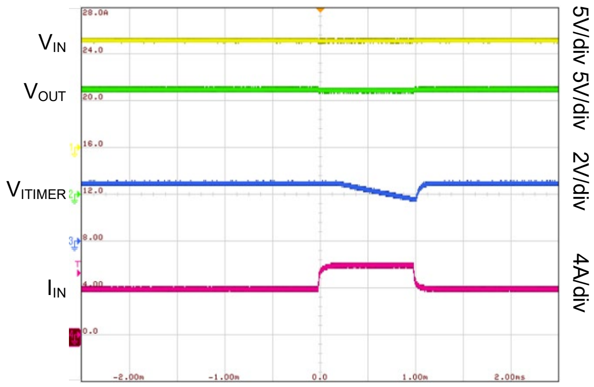
Choose nearest standard capacitor value as 2.2nF.

Application Curves



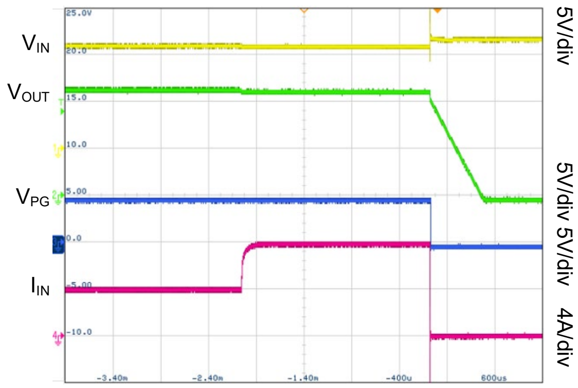
Time (10ms/div)

Figure 21. Power Up



Time (500μs/div)

Figure 22. Transient Overload



Time (500μs/div)

Figure 23. Circuit-Breaker Response

Active ORing

Figure 24 illustrates a common setup for a redundant power supply. Schottky ORing diodes have traditionally been used to connect power supplies in parallel, such as combining a wall adapter with a battery or a backup storage capacitor. However, a major drawback of ORing diodes is the significant voltage drop and resulting power dissipation. The SGM2545Ax/Cx series, which integrates low-resistance, back-to-back FETs, offers a more efficient and streamlined alternative. As depicted in Figure 24, an active ORing configuration can be implemented using SGM2545Cx devices.

APPLICATION INFORMATION (continued)

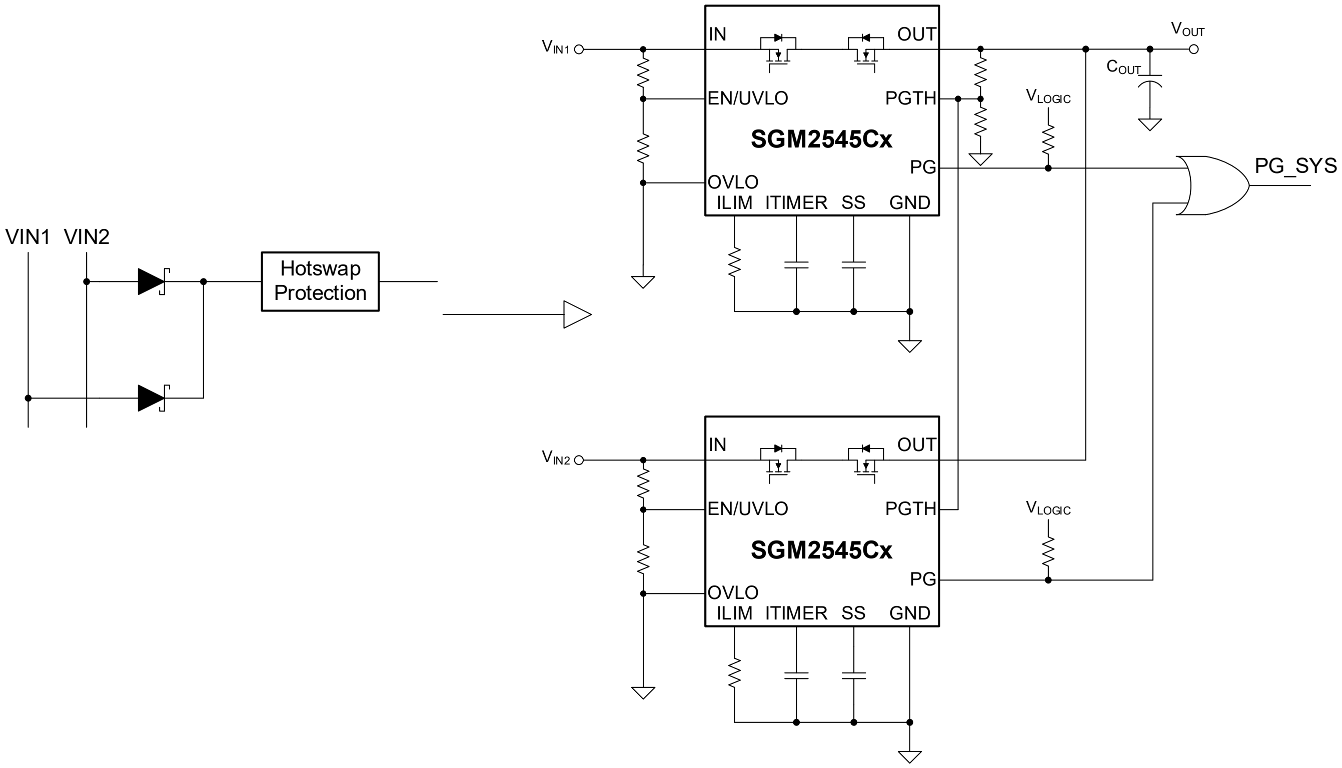


Figure 24. Two Devices, Active ORing Configuration

The linear ORing functionality in the SGM2545xx prevents reverse current from transferring between power sources, regardless of whether the supply voltage ramps up quickly or slowly.

The subsequent waveform demonstrates the operation of active ORing during the sequential voltage increase of the supply rails.

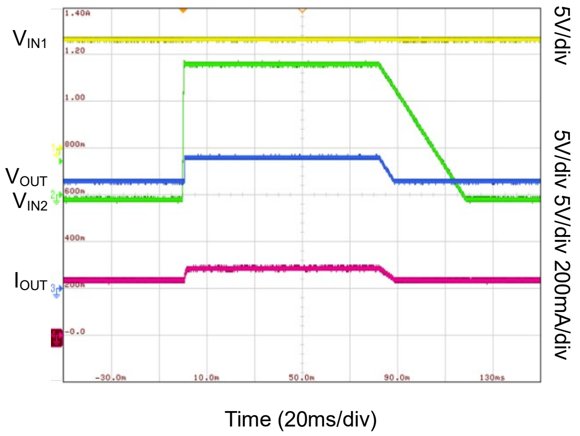


Figure 25. Active ORing Response

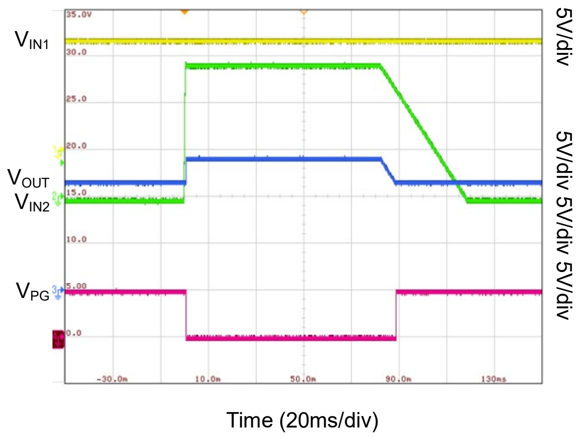


Figure 26. Active ORing Response

When the bus voltages (IN1 and IN2) are equal, the components in each pathway become forward-biased and conduct, supplying current to the load. Current distribution between the rails during this operation is proportional to the voltage differential present across each respective component.

Beyond performing supply ORing functions, these components continuously safeguard the system against overvoltage conditions, high inrush currents, overload situations, and short-circuit failures under all operating conditions.

APPLICATION INFORMATION (continued)

Power Supply Recommendations

The operational input voltage range for the SGM2545xx devices is specified between 2.7V and 23V. A ceramic input bypass capacitor with a value exceeding 0.1μF is recommended if the supply is positioned more than a few inches away. The power supply must be specified to deliver currents beyond the set current limit to avoid droops under overcurrent or short-circuit events.

The device's input must not exceed a minimum negative voltage of -15V or V_{OUT} - 21V, whichever is greater. For low-voltage signals derived from the input supply (such as EN/UVLO, OVLO, and PGTH), a sufficiently large pull-up resistor must be used to ensure that the current through these pins remains below 10μA under reverse polarity conditions. For further information, please consult the Absolute Maximum Ratings table.

Transient Protection

During a short-circuit or overload current interruption event, the input inductance produces a positive voltage spike at the input, while the output inductance creates a negative voltage spike at the output. The magnitude of these voltage transients is determined by the amount of inductance in series with the device's input or output. Without adequate mitigation, such transients may exceed the absolute maximum ratings of the device. Common methods used to suppress these transients include:

- Keep all lead lengths into and out of the device as short as possible to minimize inductance.
- Implement an extensive ground plane on the PCB.
- Attach a Schottky diode between the OUT pin and ground to suppress negative voltage transients.
- Place a low-ESR capacitor with a value greater than 1μF adjacent to the OUT pin.
- Utilize a ceramic input capacitor (C_{IN} = 1μF) with low equivalent series resistance to absorb energy and dampen transients. Ensure its voltage rating is at least twice the input supply voltage to endure positive voltage overshoot during inductive ringing.

The required input capacitance can be approximated using Equation 19

$$V_{SPIKE\_ABS} = V_{IN} + I_{LOAD} \times \sqrt{\frac{L_{IN}}{C_{IN}}} \quad (19)$$

where

V_{IN} is the nominal supply voltage.

I_{LOAD} is the load current.

L_{IN} equals the effective inductance seen looking into the source.

C_{IN} is the capacitance present at the input

- In certain applications, adding a Transient Voltage Suppressor (TVS) may be necessary to keep voltage transients within the device's absolute maximum ratings. Even when transient amplitudes remain below these limits, a TVS can help absorb excess energy, preventing very fast transient voltages from developing at the IC's supply input. Such transients could otherwise couple into internal control circuitry and lead to erratic operation.

NOTE: If reverse polarity conditions may occur at the input, it suggests employing either a bidirectional TVS or a unidirectional TVS paired with a series reverse-blocking diode for enhanced protection.

- In systems such as USB-C where a powered cable connects to the device output, overvoltage stress from OUT to IN may surpass the absolute maximum rating of the device. It recommends placing a TVS diode across OUT and IN to clamp the transient voltage within a safe operating range.

The circuit implementation with optional protection components is shown in Figure 27.

APPLICATION INFORMATION (continued)

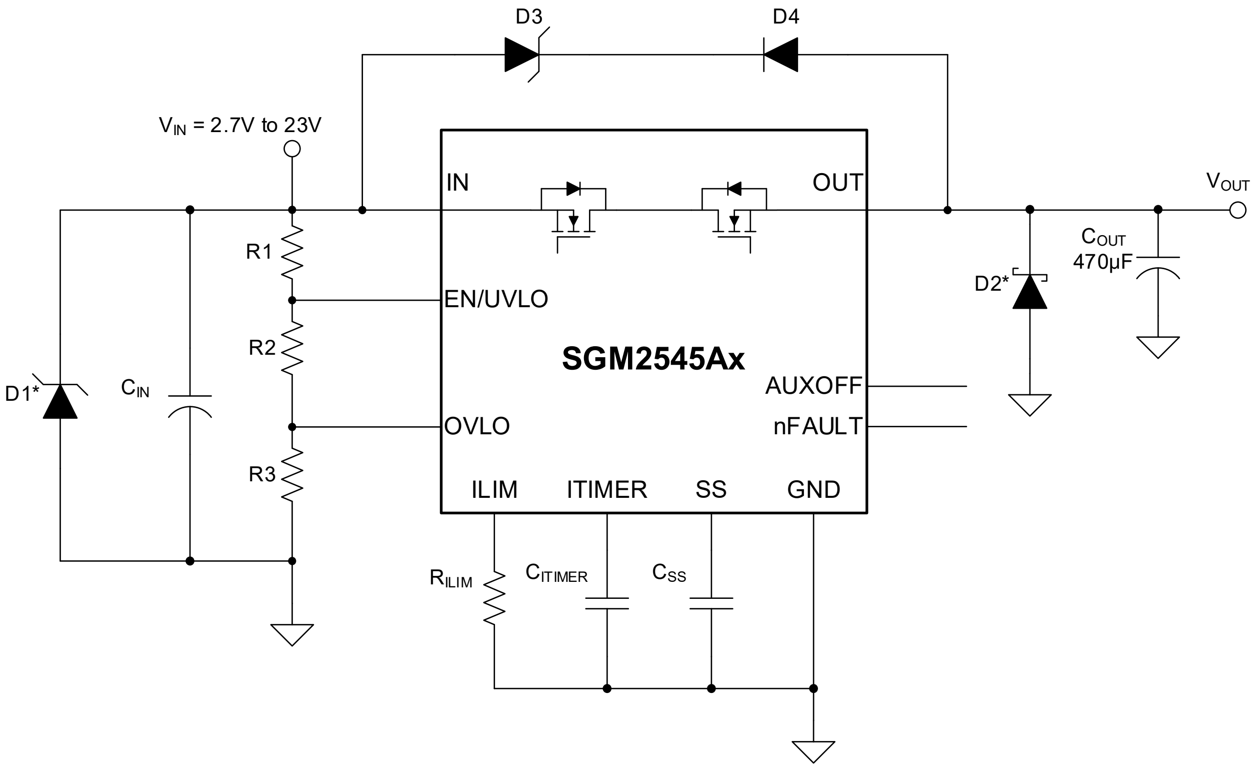


Figure 27. Circuit Implementation with Optional Protection Components

Output Short-Circuit Measurements

Achieving consistent and reproducible short-circuit test results can be challenging due to multiple factors introducing variability. Key contributors to result discrepancies include:

- Source bypassing
- Input leads
- Circuit layout
- Component selection
- Output shorting method
- Relative location of the short
- Instrumentation

The physical shorting process itself involves inherent randomness—microscopic bouncing and arcing effects occur during contact. It is important to employ a well-defined configuration and methodology to achieve representative results. Note that actual waveforms are likely to differ from those shown in this datasheet, as each test setup varies.

APPLICATION INFORMATION (continued)

Layout Guidelines

- To ensure stable operation in all designs, SGMICRO advises placing a ceramic decoupling capacitor with a capacitance of at least 0.1μF between the input (IN) and ground (GND) terminals.
- The decoupling capacitor should be positioned as near as possible to the IN and GND pins of the device. Critical attention is required to reduce the loop area generated by the bypass capacitor's trace connections, the input (IN) terminal, and the ground (GND) node of the device.
- For power transmission lines handling significant currents, conductor lengths should be minimized to reduce resistance, with their cross-sectional dimensions engineered to safely accommodate currents exceeding twice the system's maximum operational load capacity.
- The GND terminal must be connected to the PCB ground plane of the IC's terminals via the shortest possible trace adjacent. The PCB ground layer should be constructed as a continuous copper plane or an isolated island on the board. SGMICRO strongly advises implementing a dedicated ground plane for the eFuse, which is designed exclusively as a low-current pathway to serve as a noise-free reference potential for all critical analog signals of the device. This isolated ground plane must be interfaced with the system's power ground layer using a star-configured single-point interconnection to eliminate ground loops and ensure signal integrity.
- The IN and OUT pins are used for heat dissipation. Connect as much copper area as possible to the top and bottom layers of the PCB, using thermal vias for connection. The vias below the device also help to reduce the voltage gradient between the IN and OUT pins and ensure that the current flows uniformly through the device, which is crucial for achieving the best conduction resistance and current detection accuracy.
- Place the following components as close as possible to their connection pins:
  1. R_{ILIM}
  2. C_{SS}
  3. C_{ITIMER}
  4. Resistors for the EN/UVLO, OVLO/OVCSEL, and PGTH pins
- Use the shortest trace to connect the other end of the above component to the GND pin of IC. In order to minimize the parasitic effects on the current limit, over-current blanking interval and soft start timing, the trace from the R_{ILIM}, C_{ITIMER} and C_{SS} components to the IC must be as short as possible. To maintain stable system performance, the parasitic capacitance at the ILIM pin should not exceed 50pF. Additionally, ensure these traces are fully isolated from any switching signals on the PCB to avoid unintended coupling or noise interference.
- The ILIM pin's bias current dictates the device's over-current protection (OCP) threshold. To ensure reliable OCP operation, its PCB traces must be rigorously isolated from switching noise sources (e.g., power switching) to prevent false triggering due to coupled interference.
- Place TVS diodes, snubbers, bypass capacitors, and protective diodes adjacent to the device they protect. Route connections with short, wide traces to minimize parasitic inductance. For example, it recommends to use a protection Schottky diode for suppressing negative voltage transients from inductive load switching. It also recommends to install a ≥ 1μF ceramic capacitor directly between the OUT pin and GND. These components must be physically close to the OUT pins. Optimize the layout of the Schottky diode → OUT pin → GND path to form the smallest possible loop.

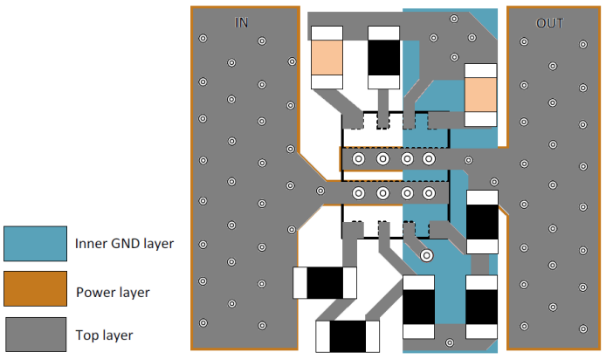


Figure 28. Layout Example

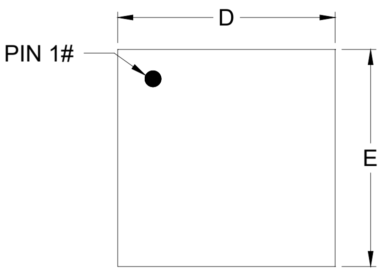
REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

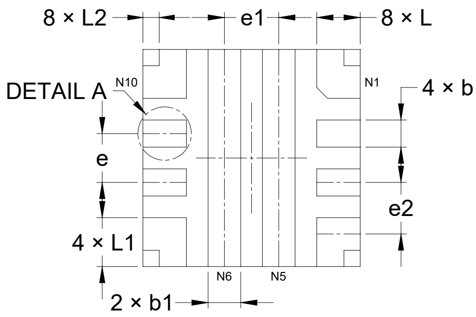
Changes from Original to REV.A (MAY 2026)	**Page**
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

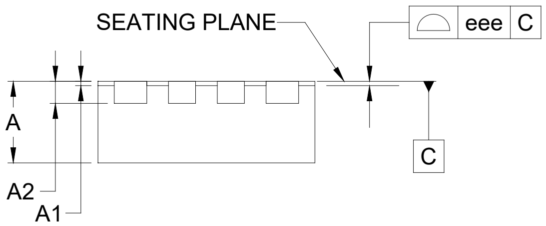
TQFN-2×2-10L



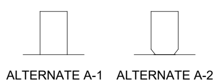
TOP VIEW



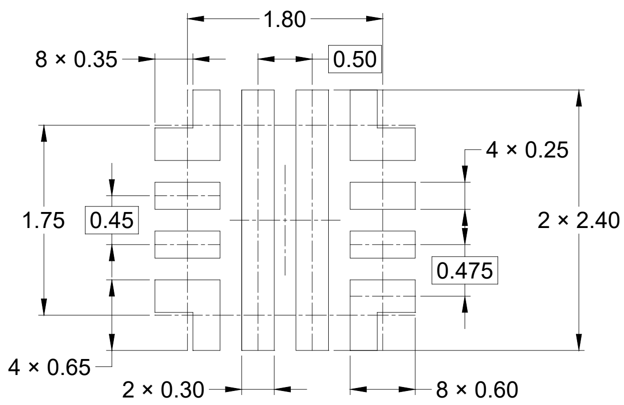
BOTTOM VIEW



SIDE VIEW



DETAIL A
ALTERNATE TERMINAL CONSTRUCTION



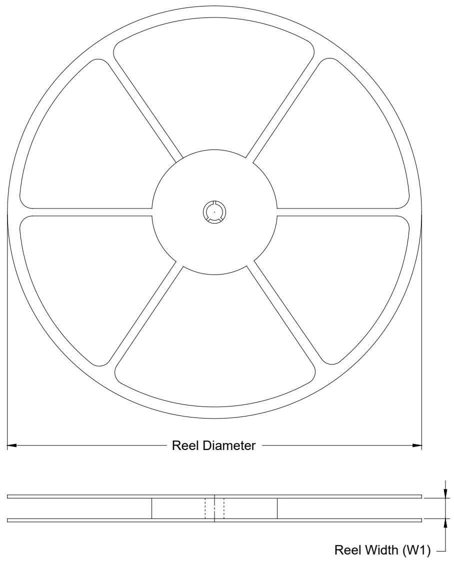
RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	0.700	-	0.800
A1	0.000	-	0.050
A2	0.203 REF		
b	0.200	-	0.300
b1	0.250	-	0.350
D	1.900	-	2.100
E	1.900	-	2.100
e	0.450 BSC		
e1	0.500 BSC		
e2	0.475 BSC		
L	0.300	-	0.500
L1	0.350	-	0.550
L2	0.150 REF		
eee	0.080		

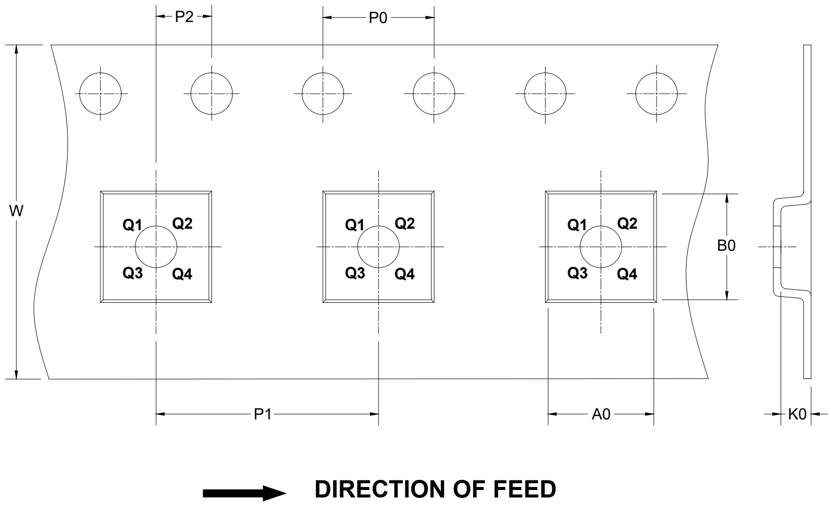
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



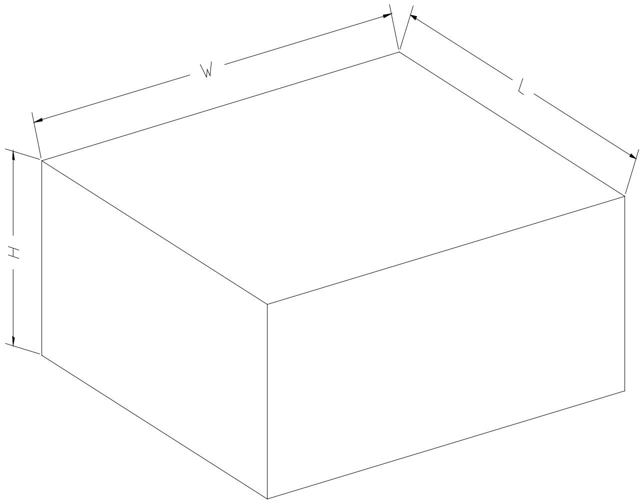
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TQFN-2×2-10L	7"	9.5	2.30	2.30	1.10	4.0	4.0	2.0	8.0	Q2

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18

DD0002