SGM64A00Q
100V Synchronous Buck DC/DC Controller with Wide Duty Cycle Range for Automotive Applications

FEATURES

- AEC-Q100 Qualified for Automotive Applications
  Device Temperature Grade 1
  T_A = -40℃ to +125℃
- Functional Safety: Available Documentation in the Design of Functional Safety Systems
- Range of Application:
  - Input Voltage Range: 6.5V to 100V
  - Output Voltage Range: 0.8V to 60V
  - Reference Voltage: 0.8V (±1% Accuracy)
  - Fixed Switching Frequency: Adjustable, 100kHz to 1MHz
- Drive Timing Characteristics:
  - High-side Minimum On-Time: 40ns
  - Low-side Minimum On-Time: 150ns
  - HO Turn-On Dead Time: 16ns
  - LO Turn-On Dead Time: 18ns
- Drive Capability:
  - Gate Drive Voltage: 7.5V
  - Current Capability: 3A Sink, 2A Source
- Control Architecture: Voltage-Mode Control with Feed-Forward Compensation
- Power Management and Protection:
  - EN: Configurable Power-On/Off Thresholds
  - VIN UVLO: Hysteretic Under-Voltage Lockout for Input Voltage
  - VCC UVLO: Hysteretic Under-Voltage Lockout for Gate Drive Supply
- Adjustable Soft-Start: Programmable Startup Time
- Conduction Mode Configuration: Selectable DCM or CCM Operation
- PGOOD: Power-Good Indicator
- Synchronization: Support Parallel or Cascaded Operation for Phase Management
- Current Sensing and Protection:
  - Low-side MOSFET R_{DSON} or External Sense Resistor Current Sensing
  - Hiccup Mode Over-Current Protection
- Over-Temperature Protection: +175°C Thermal Shutdown with Hysteresis
- Available in a Green TQFN-3.5×4.5-20BL Package

APPLICATIONS

Automotive Motor Drives
ADAS (Advanced Driver Assistance Systems)
High-Power Automotive DC/DC Regulator
HEV/EV Powertrain Systems
Body Electronics and Lighting
Infotainment and Cluster

SIMPLIFIED SCHEMATIC

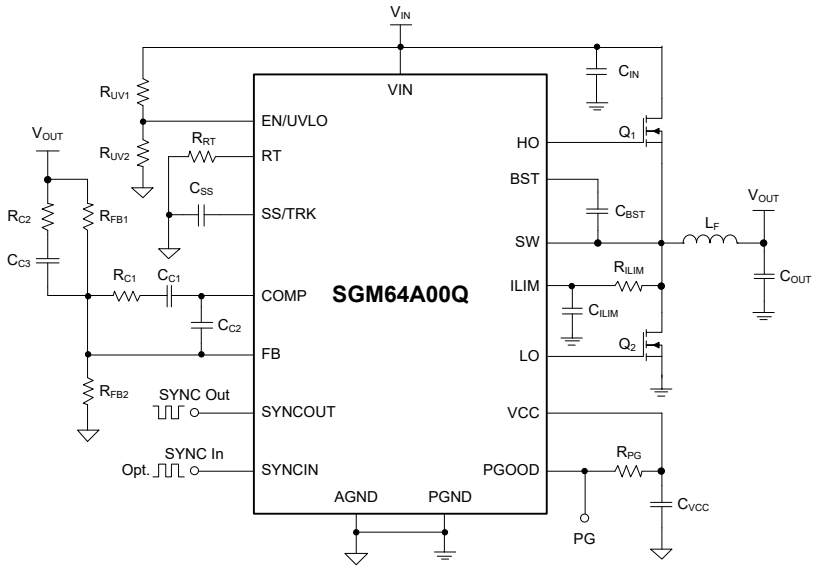


Figure 1. Simplified Schematic

GENERAL DESCRIPTION

The SGM64A00Q is a wide input voltage range synchronous Buck controller, supporting an input voltage range of 6.5V to 100V. The minimum high-side MOSFET on-time of 40ns effectively supports low duty cycle applications. The device can be directly applied to industrial-standard 48V high-voltage DC power supply systems, enabling step-down conversion to low-voltage power rails (e.g., 5V/12V). The SGM64A00Q is suitable for applications with stringent requirements on input voltage fluctuations, such as ADAS and HEV/EV systems.

The SGM64A00Q is feed-forward voltage-mode control architecture, which dynamically adjusts the ramp signal by sampling the input voltage (V_{IN}) in real-time and generating a proportional ramp signal ($V_{RAMP} = V_{IN}/k_{FF}$). This control architecture improves the transient response of the system to input voltage variations, simplifies the compensation network design, and delivers good dynamic performance and stability across a wide input voltage range.

Fixed frequency pulse width modulation (FPWM) control architecture with programmable switching frequency capability spanning 100kHz to 1MHz. It incorporates an optional discontinuous conduction mode (DCM) featuring integrated valley current detection, enabling low-side MOSFET turn-off control to minimize switching losses and reverse recovery losses during light-load operation.

The gate drive voltage is 7.5V, supporting a sink capability of 3A and a source current of 2A. An external supply can be applied to VCC to achieve higher drive voltages, supporting up to 14V for enhanced drive voltage.

The SGM64A00Q features synchronization capability, allowing the gate drive signal to synchronize with the SYNCIN clock signal, while the SYNCOUT pin outputs a clock signal with a 180° phase shift relative to the HO drive signal. This function effectively reduces input voltage ripple and minimizes EMI filter size in multi-channel or cascaded power supply applications.

This device is AEC-Q100 qualified (Automotive Electronics Council Standard Q100 Grade 1) and the use of this device is suitable for automotive applications.

The SGM64A00Q also integrates the following features: programmable soft-start, a power detection module with a power-good (PG) indicator, output voltage tracking (ensuring monotonic startup with pre-biased loads), hiccup mode over-current protection, and recoverable over-temperature protection.

The SGM64A00Q is available in a Green TQFN-3.5×4.5-20BL package and specified over a junction temperature range of -40℃ to +150℃.

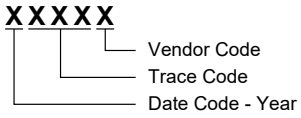
PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM64A00Q	TQFN-3.5×4.5-20BL	-40℃ to +125℃	SGM64A00QTVM20G/TR	249 XXXXX	Tape and Reel, 4000

Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



ABSOLUTE MAXIMUM RATINGS

Input Voltage
- VIN ..... -0.3V to 100V
- SW ..... -0.6V to 100V
- SW (20ns Transient) ..... -5V to 100V
- ILIM ..... -0.3V to 100V
- EN/UVLO ..... -0.3V to 100V
- VCC ..... -0.3V to 14V
- FB, COMP, SS/TRK, RT ..... -0.3V to 6V
- SYNCIN ..... -0.3V to 14V

Output Voltage
- BST ..... -0.3V to 110V
- BST to VCC ..... 100V (MAX)
- BST to SW ..... -0.3V to 14V
- LO (7ns Transient) ..... -3V (MIN)
- PGOOD ..... -0.3V to 14V
- SYNCOUT ..... -0.3V to 6V

Package Thermal Resistance
- TQFN-3.5×4.5-20BL, θ_{JA} ..... 31.4℃/W
- TQFN-3.5×4.5-20BL, θ_{JB} ..... 10.1℃/W
- TQFN-3.5×4.5-20BL, $\theta_{JC\ (TOP)}$ ..... 23.5℃/W
- TQFN-3.5×4.5-20BL, $\theta_{JC\ (BOT)}$ ..... 2.1℃/W

Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility (1) (2)
HBM ..... ±2000V
CDM ..... ±1000V

NOTES:

1. For human body model (HBM), all pins comply with AEC-Q100-002 specification.

2. For charged device model (CDM), all pins comply with AEC-Q100-011 specification.

RECOMMENDED OPERATING CONDITIONS

Input Voltage
- VIN ..... 6.5V to 100V
- SW ..... -0.6V to 100V
- ILIM ..... -0.3V to 100V
- External VCC Bias Rail ..... 8V to 13V
- EN/UVLO ..... -0.3V to 100V

Output Voltage
- BST ..... -0.3V to 110V
- BST to VCC ..... 100V (MAX)
- BST to SW ..... 5V to 13V
- PGOOD ..... 13V (MAX)

Sink/Source Current SYNCOUT, I_{SINK}/I_{SRC} ..... -1mA to 1mA
Sink/Source Current PGOOD, I_{SINK}/I_{SRC} ..... 2mA (MAX)
Operating Junction Temperature, T_J ..... -40℃ to +150℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

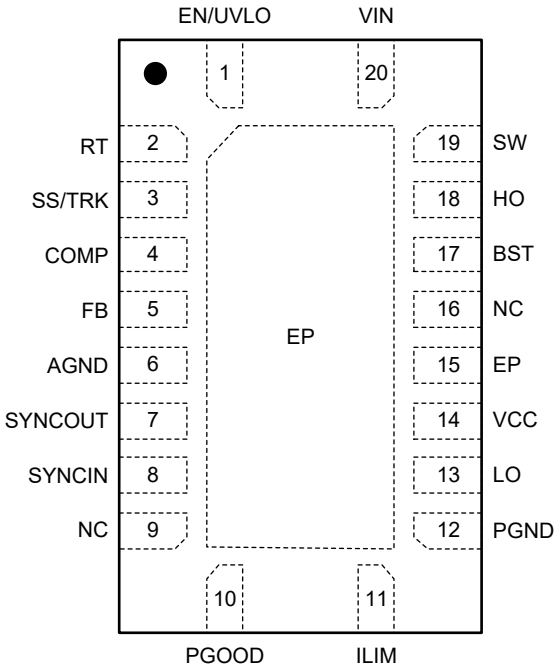
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

(TOP VIEW)



TQFN-3.5×4.5-20BL

PIN DESCRIPTION

PIN	NAME	TYPE	FUNCTION
1	EN/UVLO	I	Power Enable and Adjustable Under-Voltage Lockout Pin. Based on the EN/UVLO voltage, the SGM64A00Q operates in three distinct states: shutdown mode, pre-operational mode, and operational mode. When EN/UVLO is below 0.41V, the device enters shutdown mode, disabling all internal modules. When EN/UVLO is between 0.41V and 1.2V, the device enters pre-operational mode, where the VCC LDO is active while SS/TRK is pulled to ground, and no drive signals are output on HO or LO. When EN/UVLO exceeds 1.2V, the device enters operational mode, enabling the system to function: the voltage on SS/TRK begins to ramp up, and the control loop starts regulating the pulse width of the HO and LO drive signals. Additionally, a 10μA current source is enabled on EN/UVLO, injecting current into an external resistor network, allowing a programmable UVLO threshold to be achieved by configuring the external resistor values and voltage divider ratio.
2	RT	I	Frequency Adjustment Pin. The system clock can be configured via an external resistor between RT and AGND, with an adjustable range of 100kHz to 1MHz. Note: the RT external resistor is essential for initial startup configuration, even when an external clock is used to SYNCIN.
3	SS/TRK	I	Soft-Start and Output Voltage Tracking Pin. When the SS/TRK voltage is below 0.8V, the SS/TRK pin voltage serves as the reference, and the pin is connected to the non-inverting input of the error amplifier. When SS/TRK exceeds 0.8V, it switches to the internal 0.8V reference source as the input. SS/TRK clamps the voltage to FB + 115mV, supporting monotonic startup with pre-biased loads and ensuring controlled recovery with unexpected V_{OUT} drops. In operational mode, the SS/TRK pin sources a 10μA current to charge an external capacitor, with the capacitor value determining the soft-start time. In pre-operational mode or fault conditions (e.g. SCP), the SS/TRK discharges through an internal 11Ω pull-down resistor. Note: for system stability, a minimum 2.2nF capacitor must be connected from SS/TRK to AGND.

PIN DESCRIPTION (continued)

PIN	NAME	TYPE	FUNCTION
4	COMP	O	Error Amplifier Output Pin. Connect it to the external compensation network between COMP and FB pins.
5	FB	I	Output Voltage Feedback Pin. Connect it to V_{OUT} through a resistor divider network. Under stable conditions, the FB pin voltage is regulated to approximately 0.8V.
6	AGND	P	Analog Ground. As the ground reference for the internal 0.8V reference and other analog modules, AGND requires a single-point connection to power ground (PGND).
7	SYNCOUT	O	Synchronous Clock Output Pin. It outputs a clock signal with a 180° phase shift relative to the HO drive signal. The SYNCOUT can be connected to the SYNCIN pin of another SGM64A00Q, enabling two devices to operate at the same frequency with a 180° phase shift. Note: When an external clock is applied to SYNCIN, the HO and LO frequencies will synchronize with SYNCIN. The delay time for SYNCOUT to output high (relative to the HO rising edge) is still determined by the RT configuration, while the delay time for SYNCOUT to output low (relative to the SYNCIN rising edge) is 100ns. As a result, the high duration of SYNCOUT differs between synchronized and non-synchronized modes. If the SYNCIN frequency deviates significantly from the RT configuration, SYNCOUT will stop outputting.
8	SYNCIN	I	Synchronous Clock Input and Conduction Mode Configuration pin. When SYNCIN is used as a synchronous clock input or a high logic level, the SGM64A00Q disables low-side current zero-crossing detection and operates in CCM mode. When SYNCIN is at a low logic level, low-side current zero-crossing detection is enabled. Upon detecting zero current, the LO driver is disabled to prevent reverse inductor current, optimizing light-load efficiency. Note: Irrespective of the SYNCIN configuration, the SGM64A00Q always starts up in DCM during soft-start. If SYNCIN is configured for CCM operation, the system gradually adjusts the zero-crossing detection threshold after startup to achieve a smooth transition from DCM to CCM.
9, 16	NC	—	No Connection.
10	PGOOD	O	Power-Good Indicator Pin. The open-drain output structure requires an external pull-up resistor. A high level indicates that the FB feedback voltage is within the specified window range, signaling normal power conditions.
11	ILIM	I	Over-Current Threshold Configuration and Detection Pin. It supports two over-current detection methods, low-side MOSFET R_{DSON} sensing or external current-sense resistor sampling. During startup, the SGM64A00Q automatically identifies the sampling method and sets the ILIM current source output to 200μA (for R_{DSON} sensing) or 100μA (for external current-sense resistor sampling) accordingly. In application, the ILIM pin is connected an external resistor to the drain of the low-side MOSFET (for R_{DSON} sensing) or to the source the low-side MOSFET (for external current-sense resistor sampling) to enable current sensing.
12	PGND	P	Power Ground. The ground reference for the Buck power stage, carrying high frequency switching currents. It requires low-impedance, short-path connections to the power loop to minimize noise and parasitic inductance effects.
13	LO	P	Low-side Gate Driver Output Pin. Connect it to the gate of the low-side MOSFET in the Buck converter. It requires minimized trace length to reduce parasitic inductance, ensuring signal integrity and optimal switching performance.
14	VCC	O	7.5V LDO Output or External Supply Input Pin. A decoupling capacitor must be placed close to the VCC pin and PGND. Note: The LDO does not include reverse current protection. When using an external supply, ensure the external supply voltage does not exceed V_{IN} and the safe operating limits of VCC pin.
15	EP	—	Exposed Pad. Connect it to the ground plane to optimize thermal conduction paths, reduce thermal resistance, and enhance heat dissipation performance.

PIN DESCRIPTION (continued)

PIN	NAME	TYPE	FUNCTION
17	BST	O	Bootstrap Power Pin. It integrates a bootstrap diode from VCC to BST. A bootstrap capacitor must be connected between BST and SW to supply the high-side gate driver, with the capacitor placed close to the controller for optimal performance.
18	HO	P	High-side Gate Driver Output Pin. Connect it to the gate of the high-side MOSFET in the Buck converter. It requires minimized trace length to reduce parasitic inductance, ensuring signal integrity and optimal switching performance.
19	SW	P	Switching Node of the Buck Controller. Connect it to the bootstrap capacitor, the source of high-side MOSFET, and the drain of the low-side MOSFET. Due to rapid voltage transitions, minimize trace length to reduce parasitic inductance and noise.
20	VIN	P	Power Supply Input Pin. It supplies input power to the internal VCC LDO. Ensure the input voltage remains within the specified safe operating range of the device.
—	EP	—	Exposed pad. Connected to the ground plane to optimize thermal conduction paths, reduce thermal resistance, and enhance heat dissipation performance.

NOTE: P = Power, G = Ground, I = Input, O = Output.

ELECTRICAL CHARACTERISTICS

(V_{IN} = 48V, $V_{EN/UVLO}$ = 1.5V, R_{RT} = 24.9kΩ, T_J = -40℃ to +150℃, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Supply						
Operating Input Voltage Range	V_{IN}		6.5		100	V
Operating Input Current, Not Switching	I_{Q-RUN}	$V_{EN/UVLO}$ = 1.5V, $V_{SS/TRK}$ = 0V, V_{IN} = 6.5V to 100V		1.25	2.1	mA
Standby Input Current	I_{Q-STBY}	$V_{EN/UVLO}$ = 1V, V_{IN} = 6.5V to 100V		0.6	1	mA
Shutdown Input Current	I_{Q-SHDN}	V_{IN} = 6.5V to 100V		11	40	μA
VCC Regulator						
VCC Regulation Voltage	V_{VCC}	$V_{SS/TRK}$ = 0V, V_{IN} = 9V to 100V, I_{VCC} = 0mA to 20mA	7.28	7.55	7.72	V
VIN to VCC Dropout Voltage	$V_{VCC-LDO}$	V_{IN} = 6V, $V_{SS/TRK}$ = 0V, I_{VCC} = 20mA		0.3	0.72	V
VCC Short-Circuit Current	I_{SC-LDO}	$V_{SS/TRK}$ = 0V, V_{VCC} = 0V, V_{IN} = 6.5V to 100V	40	55	70	mA
VCC Under-Voltage Threshold	V_{VCC-UV}	V_{VCC} rising	6	6.17	6.4	V
VCC Under-Voltage Hysteresis	$V_{VCC-UVH}$	Rising threshold - falling threshold		0.34		V
Minimum External Bias Voltage	$V_{VCC-EXT}$	Voltage required to disable VCC regulator	8			V
External VCC Input Current, Not Switching	I_{VCC}	$V_{SS/TRK}$ = 0V, V_{VCC} = 13V			0.9	mA
ENABLE and Input UVLO						
Shutdown to Standby Threshold	V_{SHDN}	$V_{EN/UVLO}$ rising		0.41		V
Shutdown Threshold Hysteresis	$V_{SHDN-HYS}$	EN/UVLO rising threshold - falling threshold		50		mV
Standby to Operating Threshold	V_{EN}	$V_{EN/UVLO}$ rising, V_{IN} = 6.5V to 100V	1.164	1.2	1.236	V
Standby to Operating Hysteresis Current	I_{EN-HYS}	$V_{EN/UVLO}$ = 1.5V	8.8	10	11	μA
Error Amplifier						
FB Reference Voltage	V_{REF}	FB connected to COMP	792	800	808	mV
FB Input Bias Current	$I_{FB-BIAS1}$	V_{FB} = 0.8V, T_J = -40℃ to +125℃	-0.1		0.1	μA
FB Input Bias Current	$I_{FB-BIAS2}$	V_{FB} = 0.8V, T_J = -40℃ to +150℃	-0.2		0.2	μA
COMP Output High Voltage	$V_{COMP-OH}$	V_{FB} = 0V, COMP sourcing 1mA		5		V
COMP Output Low Voltage	$V_{COMP-OL}$	COMP sinking 1mA			0.3	V
DC Gain (1)	A_{VOL}			100		dB
Unity Gain Bandwidth (1)	G_{BW}			5		MHz
Soft-Start and Voltage Tracking						
SS/TRK Capacitor Charging Current	I_{SS}	$V_{SS/TRK}$ = 0V	8.5	10	12	μA
SS/TRK Discharge FET Resistance	R_{SS}	$V_{EN/UVLO}$ = 1V, $V_{SS/TRK}$ = 0.1V		11		Ω
SS/TRK to FB Offset	V_{SS-FB}		-15		15	mV
SS/TRK Clamp Voltage	$V_{SS-CLAMP}$	$V_{SS/TRK}$ - V_{FB}, V_{FB} = 0.8V		115		mV
Power-Good Indicator						
FB Upper Threshold for PGOOD High to Low	PG_{UTH}	% of V_{REF}, V_{FB} rising	105.5	108	110	%
FB Lower Threshold for PGOOD High to Low	PG_{LTH}	% of V_{REF}, V_{FB} falling	90	92	94	%
PGOOD Upper Threshold Hysteresis	PG_{HYS_U}	% of V_{REF}		3.5		%
PGOOD Lower Threshold Hysteresis	PG_{HYS_L}	% of V_{REF}		2.5		%
PGOOD Rising Filter	$t_{PG-RISE}$	FB to PGOOD rising edge		25		μs
PGOOD Falling Filter	$t_{PG-FALL}$	FB to PGOOD falling edge		25		μs
PGOOD Low State Output Voltage	V_{PG-OL}	V_{FB} = 0.9V, I_{PGOOD} = 2mA			150	mV
PGOOD High State Leakage Current	I_{PG-OH}	V_{FB} = 0.8V, V_{PGOOD} = 13V			400	nA

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 48V, $V_{EN/UVLO}$ = 1.5V, R_{RT} = 24.9kΩ, T_J = -40℃ to +150℃, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Oscillator						
Oscillator Frequency 1	f_{SW1}	R_{RT} = 100kΩ		100		kHz
Oscillator Frequency 2	f_{SW2}	R_{RT} = 24.9kΩ	380	400	420	kHz
Oscillator Frequency 3	f_{SW3}	R_{RT} = 12.4kΩ		780		kHz
Synchronization Input and Output						
SYNCIN External Clock Frequency Range	f_{SYNC}	% of nominal frequency set by R_{RT}	-20		50	%
SYNCIN Input Logic High	$V_{SYNC-IH}$	V_{IN} = 6.5V to 100V	2			V
SYNCIN Input Logic Low	$V_{SYNC-IL}$	V_{IN} = 6.5V to 100V			0.8	V
SYNCIN Input Resistance	$R_{SYNC-IN}$	V_{SYNCIN} = 3V		20		kΩ
SYNCIN Input Minimum Pulse Width	$t_{SYNCI-PW}$	Minimum high state or low state duration	50			ns
SYNCOUT High-State Output Voltage	$V_{SYNCO-OH}$	$I_{SYNCOUT}$ = -1mA (sourcing current)	3			V
SYNCOUT Low-State Output Voltage	$V_{SYNCO-OL}$	$I_{SYNCOUT}$ = 1mA (sinking current)			0.4	V
Delay from HO Rising to SYNCOUT Leading Edge	$t_{SYNCOUT}$	V_{SYNCIN} = 0V, $t_S = 1/f_{SW}$, f_{SW} set by R_{RT}		t_S/2 - 320		ns
Delay from SYNCIN Rising to HO Leading Edge	t_{SYNCIN}	50% to 50%		320		ns
Gate Drivers						
HO High State Resistance, HO to BST	R_{HO-UP}	V_{BST} - V_{SW} = 7V, I_{HO} = -100mA		2.1		Ω
HO Low State Resistance, HO to SW	$R_{HO-DOWN}$	V_{BST} - V_{SW} = 7V, I_{HO} = 100mA		0.9		Ω
LO High State Resistance, LO to VCC	R_{LO-UP}	V_{BST} - V_{SW} = 7V, I_{LO} = -100mA		2.1		Ω
LO Low State Resistance, LO to PGND	$R_{LO-DOWN}$	V_{BST} - V_{SW} = 7V, I_{LO} = 100mA		0.9		Ω
HO, LO Source Current	I_{HOH}, I_{LOH}	V_{BST} = V_{SW} = 7V, HO = SW, LO = AGND		2		A
HO, LO Sink Current	I_{HOL}, I_{LOL}	V_{BST} = V_{SW} = 7V, HO = BST, LO = VCC		3		A
Bootstrap Diode and Under-Voltage Threshold						
Diode Forward Voltage, VCC to BST	$V_{BST-FWD}$	VCC to BST, BST pin sourcing 20mA		0.67	0.9	V
BST to SW Quiescent Current, Not Switching	I_{Q-BST}	$V_{SS/TRK}$ = 0V, V_{SW} = 48V, V_{BST} = 54V		70		μA
BST to SW Under-Voltage Detection	V_{BST-UV}	V_{BST} - V_{SW} falling		4		V
BST to SW Under-Voltage Hysteresis	$V_{BST-HYS}$	V_{BST} - V_{SW} rising		0.42		V
PWM Control						
Minimum Controllable On-Time	t_{ON_MIN}	V_{BST} - V_{SW} = 7V, HO 50% to 50%		40	60	ns
Minimum Off-Time	t_{OFF_MIN}	V_{BST} - V_{SW} = 7V, HO 50% to 50%		150	200	ns
Maximum Duty Cycle	DC_{100kHz}	f_{SW} = 100kHz, V_{IN} = 6.5V to 100V	98	98.5		%
	DC_{400kHz}	f_{SW} = 400kHz, V_{IN} = 6.5V to 100V	90	94		%
RAMP Valley Voltage (COMP at 0% Duty Cycle)	V_{RAMP_MIN}			300		mV
PWM Feed-Forward Gain (V_{IN}/V_{RAMP})	k_{FF}	V_{IN} = 9V to 100V		15		V/V
Over-Current Protect (OCP) – Valley Current Limiting						
ILIM Source Current, R_{SENSE} Mode	I_{RS}	Low voltage detected at ILIM	90	100	110	μA
ILIM Source Current, R_{DSON} Mode	I_{RDSON}	SW voltage detected at ILIM, T_J = +25℃	180	200	220	μA
ILIM Current Tempco	$I_{RDSONTC}$	R_{DSON} mode		4500		ppm/℃
ILIM Current Tempco	I_{RSTC}	R_{SENSE} mode		0		ppm/℃
ILIM Comparator Threshold at ILIM	$V_{ILIM-TH}$		-11.5	-2	7	mV

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 48V, $V_{EN/UVLO}$ = 1.5V, R_{RT} = 24.9kΩ, T_J = -40℃ to +150℃, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Short Circuit Protection (SCP) – Duty Cycle Clamp						
Clamp Offset Voltage (No Current Limiting)	$V_{CLAMP-OS}$	COMP to duty cycle clamp voltage		0.2 + V_{IN}/75		V
Hiccup Mode Fault Protection						
Hiccup Mode Activation Delay	$C_{HICC-DEL}$	Clock cycles with current limiting before off-time activated		128		cycles
Hiccup Mode Off-Time after Activation	C_{HICCUP}	Clock cycles with no switching followed by SS/TRK release		8192		cycles
Diode Emulation/DCM Operation						
Zero-Cross Detect (ZCD) Soft-Start Ramp	V_{ZCD-SS}	ZCD threshold measured at SW pin 50 cycles after first HO pulse		0		mV
Zero-Cross Detect Disable Threshold	$V_{ZCD-DIS}$	ZCD threshold measured at SW pin 1000 cycles after first HO pulse		200		mV
Diode Emulation Zero-Cross Threshold	V_{DEM-TH}	Measured at SW with V_{SW} rising	-14	-2	8	mV
Thermal Shutdown						
Thermal Shutdown Threshold	T_{SD}	T_J rising		175		℃
Thermal Shutdown Hysteresis	T_{SD-HYS}			22		℃

NOTE:

1. Guaranteed by design.

SWITCHING CHARACTERISTICS

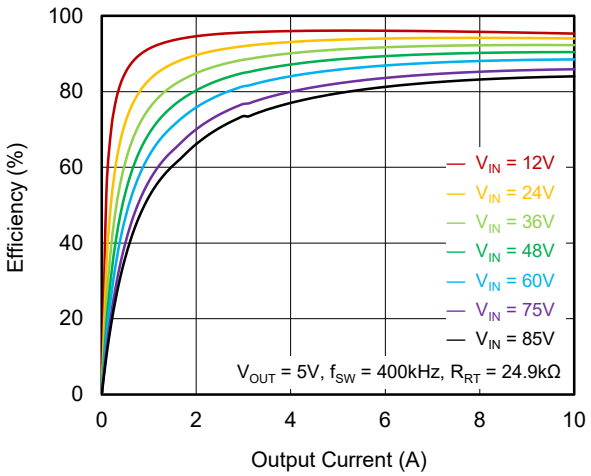
(Typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
HO, LO Rise Times	t_{HTR}, t_{LTR}	V_{BST} - V_{SW} = 7V, C_{LOAD} = 1nF, 20% to 80%		7		ns
HO, LO Fall Times	t_{HO-TF}, t_{LO-TF}	V_{BST} - V_{SW} = 7V, C_{LOAD} = 1nF, 80% to 20%		4		ns
HO Turn-On Dead Time	t_{HO-DT}	V_{BST} - V_{SW} = 7V, LO off to HO on, 50% to 50%		16		ns
LO Turn-On Dead Time	t_{LO-DT}	V_{BST} - V_{SW} = 7V, HO off to LO on, 50% to 50%		18		ns

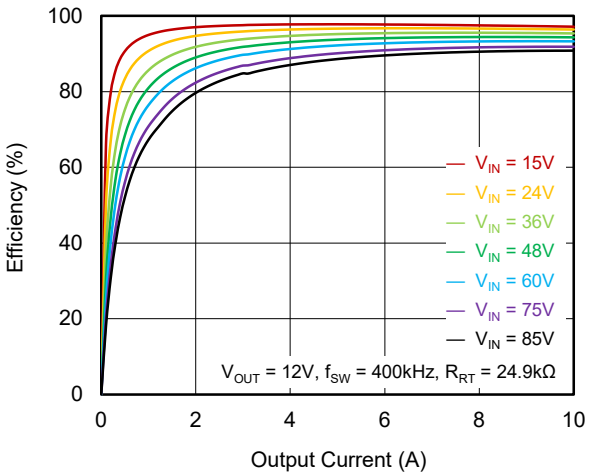
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 48V, R_{RT} = 24.9kΩ, SYNCIN tied to VCC, EN/UVLO tied to VIN, unless otherwise noted.

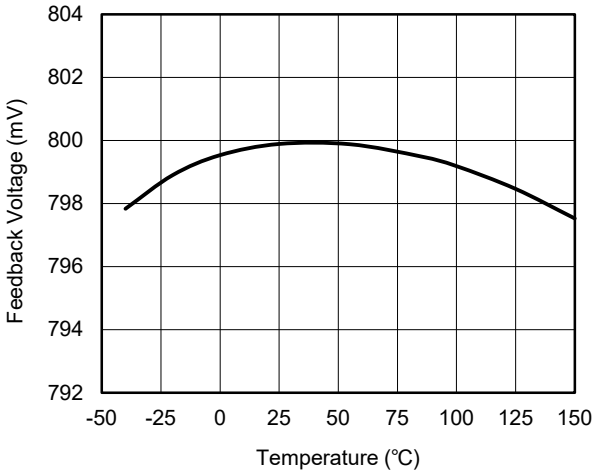
Efficiency vs. Load, CCM



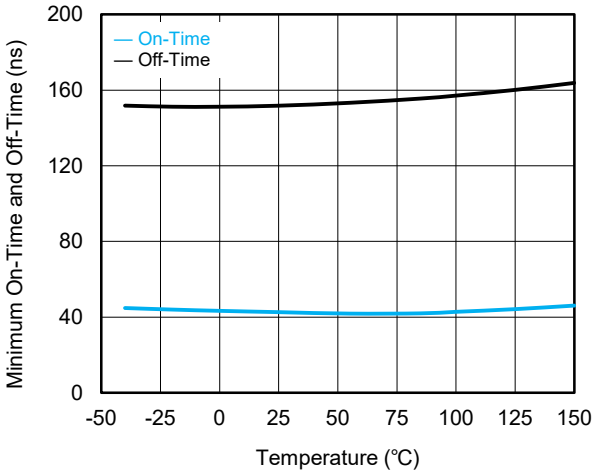
Efficiency vs. Load, CCM



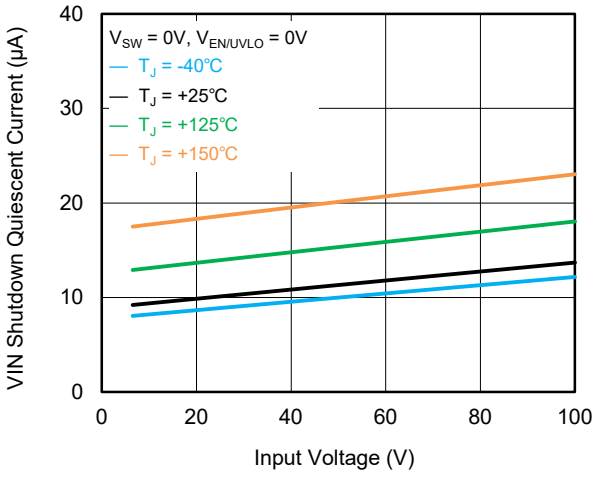
Feedback Voltage vs. Temperature



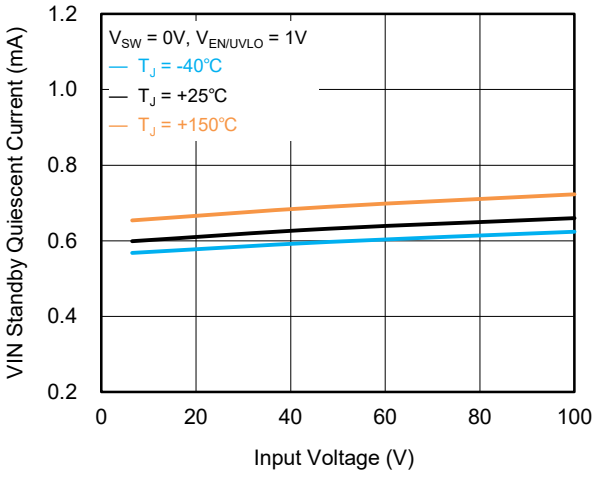
Minimum On-Time and Off-Time vs. Temperature



VIN Shutdown Quiescent Current vs. Input Voltage



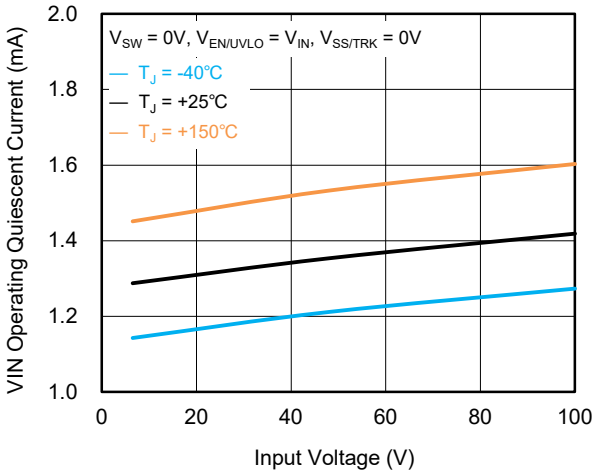
VIN Standby Quiescent Current vs. Input Voltage



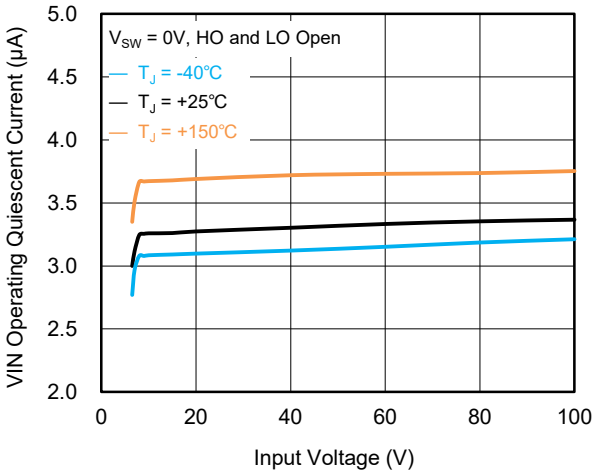
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

V_{IN} = 48V, R_{RT} = 24.9kΩ, SYNCIN tied to VCC, EN/UVLO tied to VIN, unless otherwise noted.

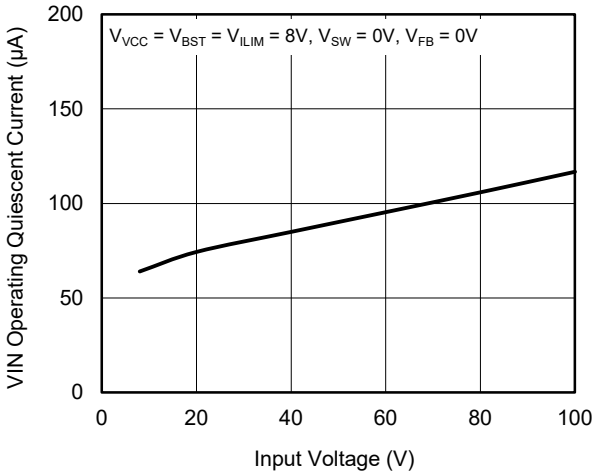
VIN Operating Quiescent Current (Non-Switching) vs. Input Voltage



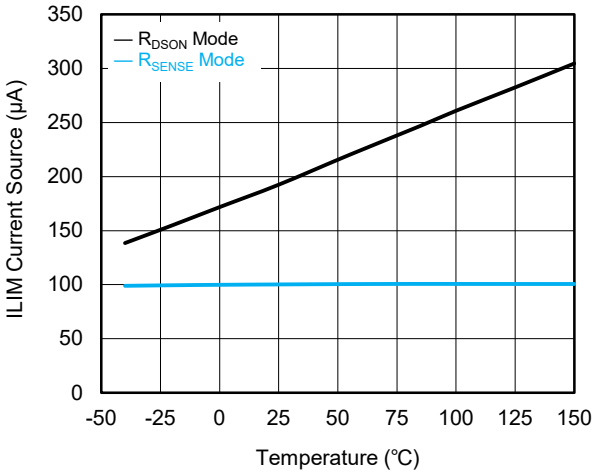
VIN Operating Quiescent Current (Switching) vs. Input Voltage



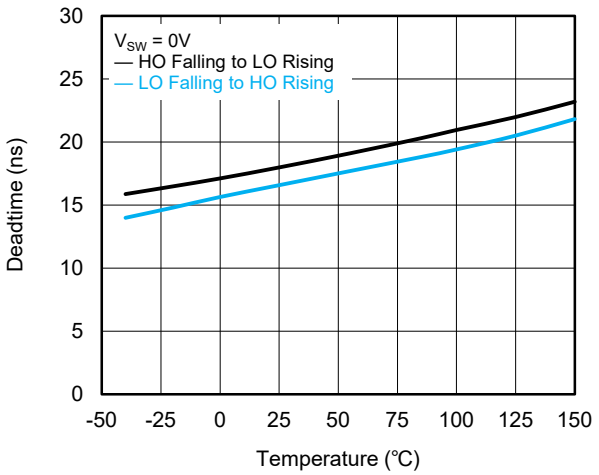
VIN Operating Quiescent Current with External VCC Applied



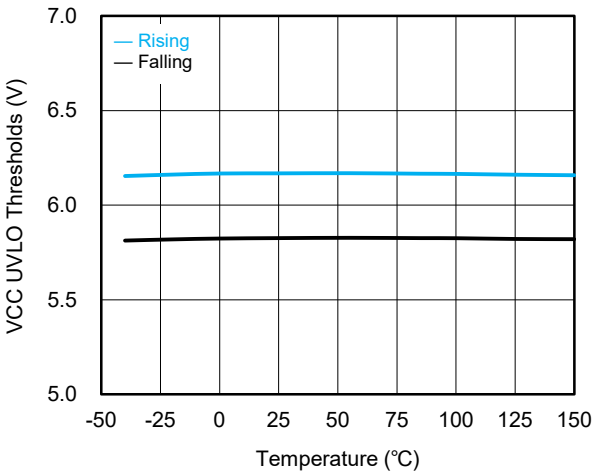
ILIM Current Source vs. Temperature



Deadtime vs. Temperature



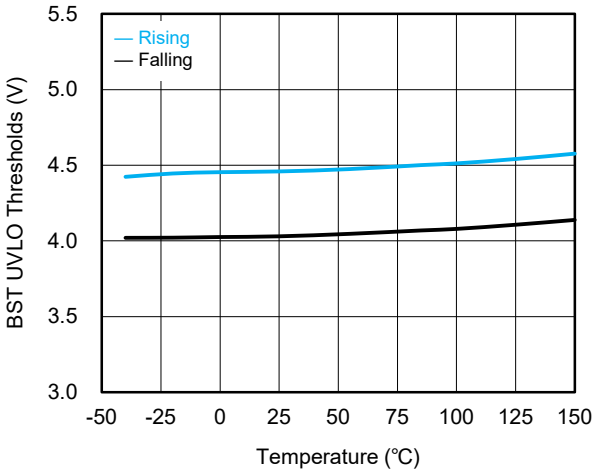
VCC UVLO Thresholds vs. Temperature



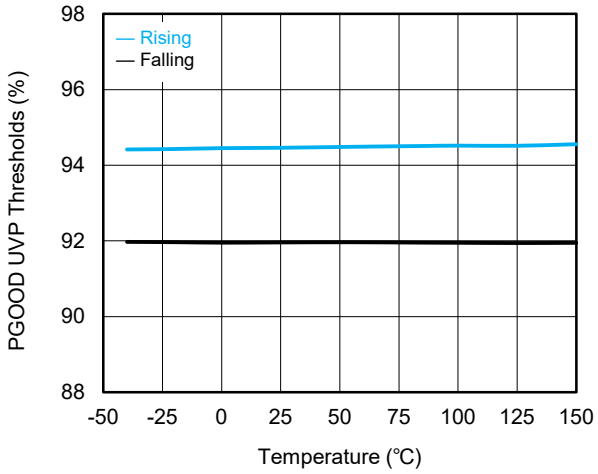
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

V_{IN} = 48V, R_{RT} = 24.9kΩ, SYNCIN tied to VCC, EN/UVLO tied to VIN, unless otherwise noted.

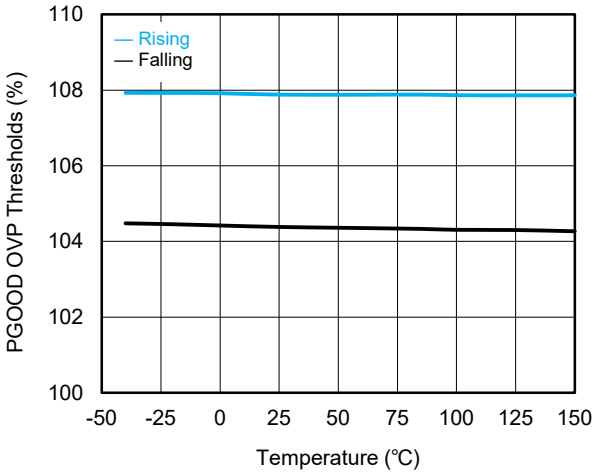
BST UVLO Thresholds vs. Temperature



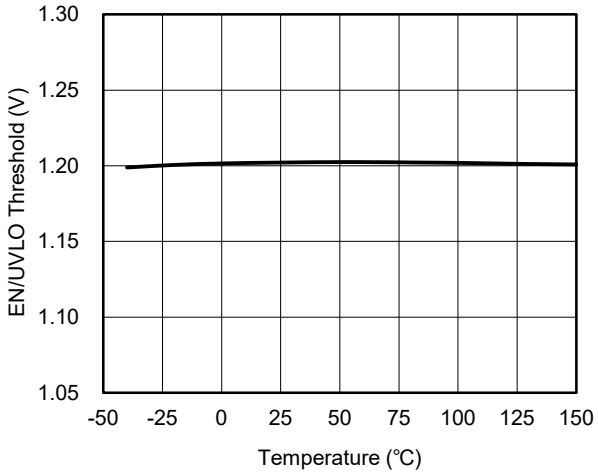
PGOOD UVP Thresholds vs. Temperature



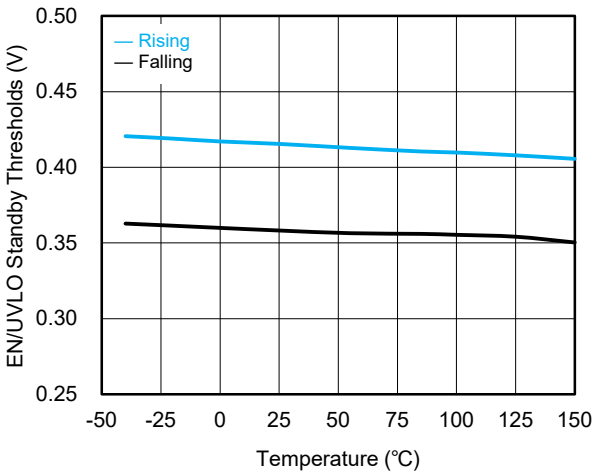
PGOOD OVP Thresholds vs. Temperature



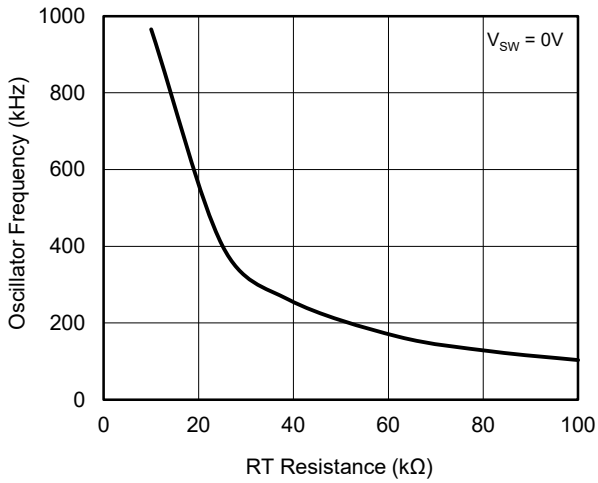
EN/UVLO Threshold vs. Temperature



EN/UVLO Standby Thresholds vs. Temperature



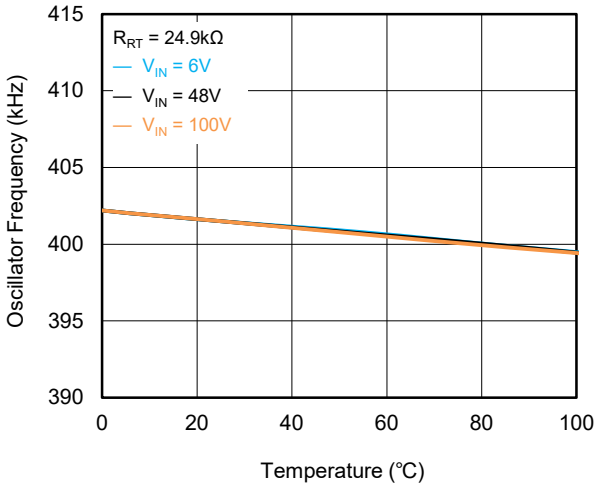
Oscillator Frequency vs. RT Resistance



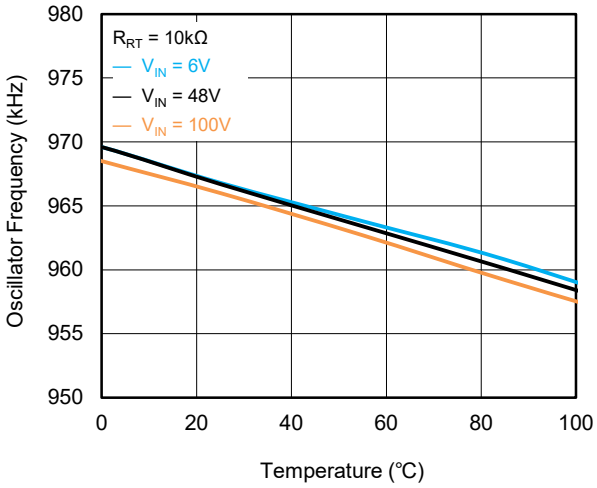
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

V_{IN} = 48V, R_{RT} = 24.9kΩ, SYNCIN tied to VCC, EN/UVLO tied to VIN, unless otherwise noted.

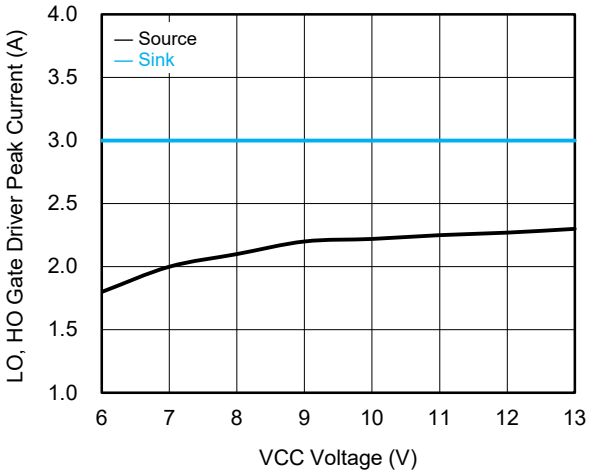
Oscillator Frequency vs. Temperature



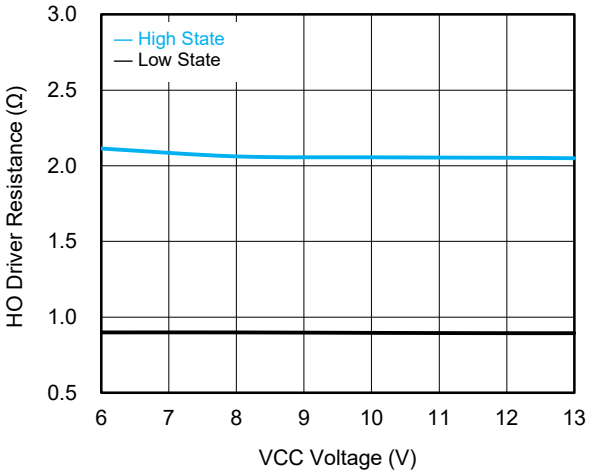
Oscillator Frequency vs. Temperature



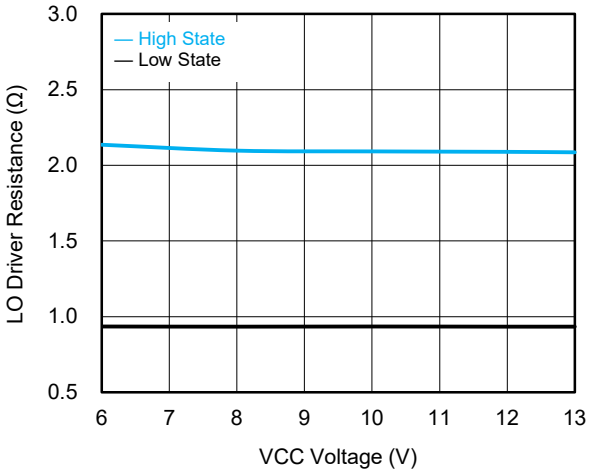
LO, HO Gate Driver Peak Current vs. VCC Voltage



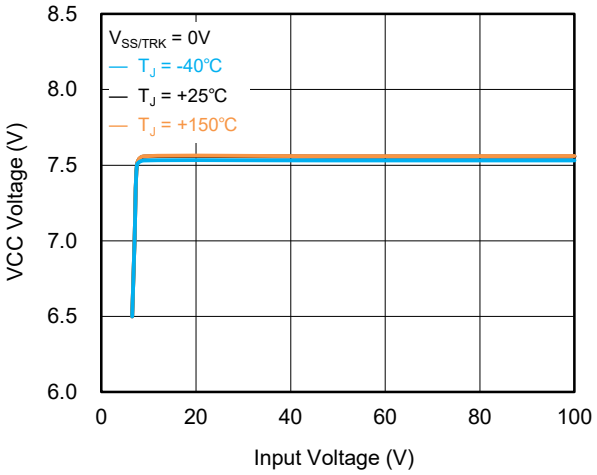
HO Driver Resistance vs. VCC Voltage



LO Driver Resistance vs. VCC Voltage



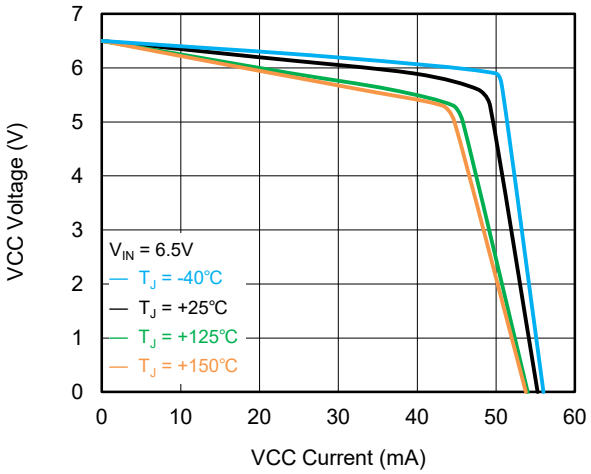
VCC Voltage vs. Input Voltage



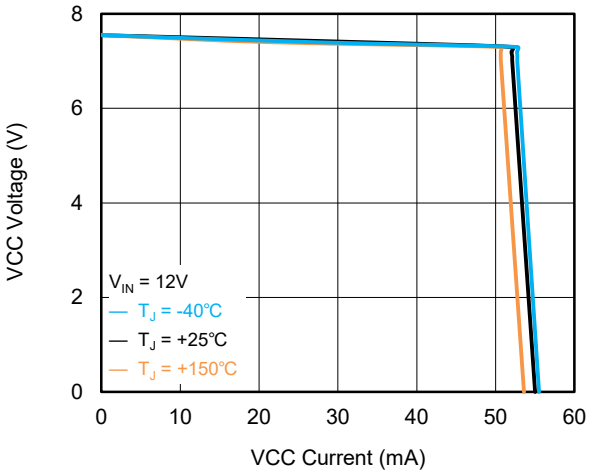
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

V_{IN} = 48V, R_{RT} = 24.9kΩ, SYNCIN tied to VCC, EN/UVLO tied to VIN, unless otherwise noted.

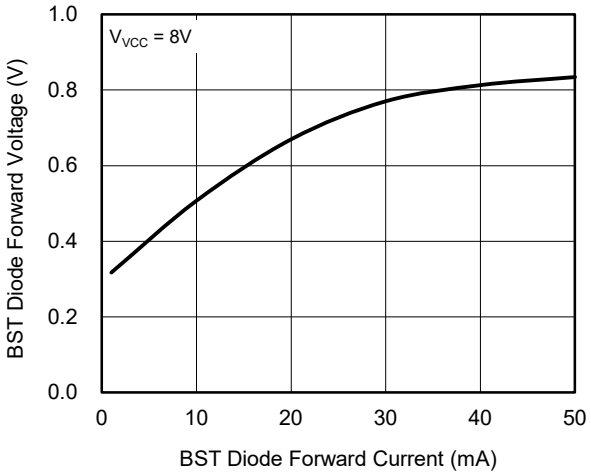
VCC Voltage vs. VCC Current



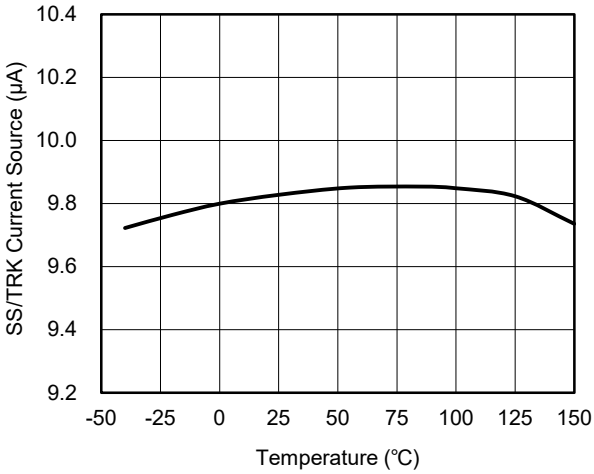
VCC Voltage vs. VCC Current



BST Diode Forward Voltage vs. Current



SS/TRK Current Source vs Temperature



FUNCTIONAL BLOCK DIAGRAM

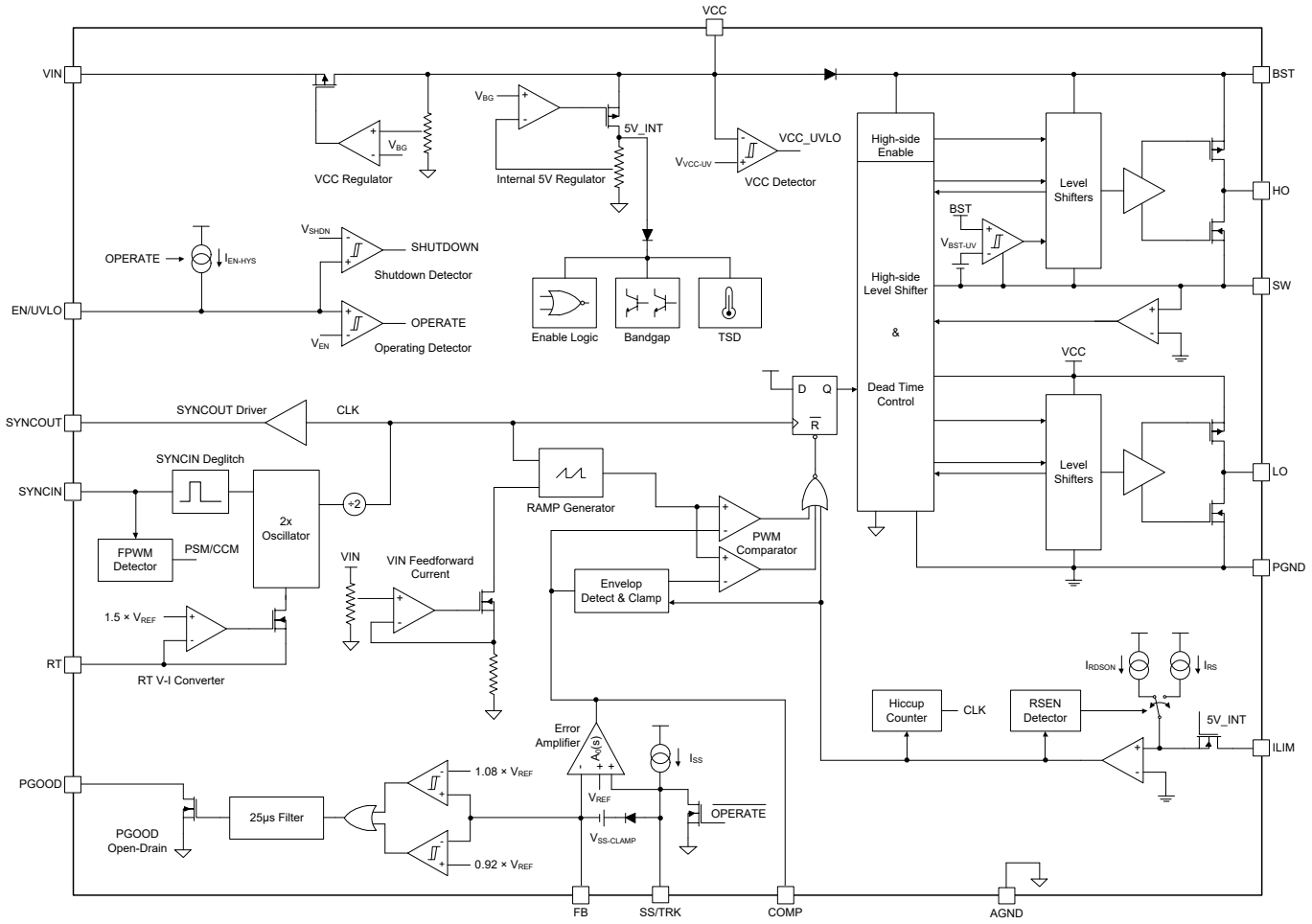


Figure 2. Block Diagram

DETAILED DESCRIPTION

Overview

The SGM64A00Q is a 100V synchronous Buck controller featuring the voltage-mode control architecture with input feed-forward. This design achieves exceptional line transient response across wide input voltage variations while supporting extended duty cycle operation, making it optimized for high conversion ratio and low dropout applications. The SGM64A00Q features programmable switching frequency from 100kHz to 1MHz and implements cycle-by-cycle current limiting through either low-side FET R_{DSON} detection or an external current sense resistor. It integrates a 7.5V gate driver compatible with standard-threshold MOSFETs and supports an external bias supply to improve efficiency in high-voltage applications. For system optimization, a configurable diode emulation mode (DCM) is available to improve light-load efficiency. And the SYNC function supports multi-chip parallel operation with 180° phase-shifted SW signals, which smooths input current, minimizes input voltage ripple and system EMI.

Feature Description

Input Voltage

The SGM64A00Q operates with an input voltage range from 6.5V to 100V, making it suitable for use with 12V, 24V, 48V, 60V, and 72V unregulated, semi-regulated or fully regulated power bus systems. An integrated internal LDO regulator generates a 7.5V VCC bias supply for the gate driver and control circuitry. In high-voltage applications, ensure the voltage at the VIN pin within the absolute maximum rating to prevent permanent damage to the SGM64A00Q. It is recommended to place high-quality ceramic capacitors or an RC network near the VIN pin to suppress voltage ringing.

Output Voltage and Accuracy

The FB pin features a 0.8V reference voltage (V_{REF}), maintaining ±1% feedback system accuracy across the entire -40℃ to +150℃ junction temperature range. The SGM64A00Q supports output voltage configuration from 0.8V up to 60V. The DC output voltage level during normal operation is set by the R_{FB1} and R_{FB2} feedback resistor network connected to the output.

Internal High-Voltage VCC LDO Regulator

The SGM64A00Q integrates an internal high-voltage LDO regulator to generate the VCC rail, which supplies power to the PWM controller and gate drivers for the external MOSFETs.

This VCC regulator is set to 7.5V, its output tracks the VIN voltage with a minimal dropout when the input falls below the VCC target level. It is recommended to place ceramic decoupling capacitor between 1μF and 5μF between VCC and AGND to ensure stability.

During power-up, once the EN/UVLO voltage exceeds 0.41V, the regulator charges the capacitor on the VCC pin. Once the VCC voltage exceeds its rising UVLO threshold of 6.17V and the EN/UVLO pin voltage is above 1.2V, the PWM controller is enabled and an output soft-start begins. The controller remains active until the VCC voltage drops below the falling UVLO threshold of 5.83V or the EN/UVLO voltage below 1.2V.

The VCC regulator exhibits an inherent dropout voltage with a supported output current limit of 40mA. Designs must carefully evaluate the power MOSFET's gate charge (Q_g) and switching frequency (f_{SW}) when using the internal VCC regulator for gate drive. Excessive gate drive loss can lead to VCC dropout, which may trigger the VCC UVLO protection and disable the PWM controller.

Enable and Adjustable Under-Voltage Lockout

The EN/UVLO supports adjustable input under-voltage lockout (UVLO) functionality. It integrates an internal 1.2V bandgap reference and a 10μA current source, enabling the hysteresis thresholds for turn-on and turn-off to be set by external resistors to meet specific system-sequencing requirements. The SGM64A00Q operates in three distinct modes depending on the EN/UVLO voltage: shutdown mode, pre-operational mode, and operational mode.

Shutdown Mode: When the EN/UVLO voltage is below 0.36V, the SGM64A00Q enters shutdown mode. Both the internal VCC regulator and the PWM driver are turned off. Under this condition, the input current of the typically drops to 11μA at V_{IN} = 48V.

Pre-Operational Mode: With the EN/UVLO voltage between 0.41V and 1.2V, the device enters pre-operational mode. In this state, the internal VCC regulator becomes operational and generates the VCC supply, the PWM driver remaining disabled.

DETAILED DESCRIPTION (continued)

Operational Mode: When the EN/UVLO voltage exceeds 1.2V and the VCC voltage rises above VCC under-voltage threshold, the device enters operational mode. The internal 10μA current source is active at the EN/UVLO pin, sourcing current to external circuit. And the PWM driver is activated, a soft-start sequence begins at output.

Most applications can implement a UVLO threshold using the resistor-divider network (R_{UV1} and R_{UV2}) shown in Figure 3. The relationship between the configured VIN turn-on/turn-off voltages and the resistor values can be calculated with the following formulas:

$$R_{UV1} = \frac{V_{IN\_ON} - V_{IN\_OFF}}{I_{HYS}} \quad (1)$$

$$R_{UV2} = R_{UV1} \times \frac{V_{EN}}{V_{IN\_ON} - V_{EN}} \quad (2)$$

where,

I_{HYS} is the 10μA standby to operating hysteresis current.

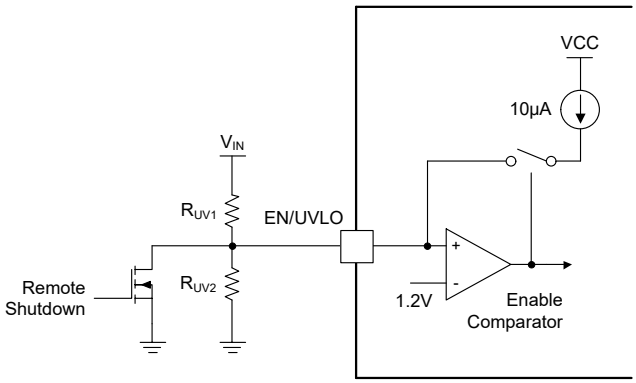


Figure 3. Application Circuit for Programmable Input UVLO

Power-Good Function

The SGM64A00Q features an open-drain power-good (PGOOD) output. When EN > V_{SHDN} (0.41V, TYP), PGOOD is pulled low if the output voltage falls outside its regulation window. When EN < V_{SHDN} (0.41V, TYP), PGOOD is in a high-impedance state. It must be connected through a resistor to a voltage source not exceeding 13V, with a typical resistance between 10kΩ and 100kΩ. The PGOOD window thresholds are defined by comparing the FB voltage with the internal reference voltage (V_{REF}).

Normal Window: The PGOOD pin is pulled high by the external resistor when the FB voltage is between 94% and 108% of V_{REF}.

Under-Voltage Indication: If the FB voltage falls below 92% of V_{REF}, the internal switch turns on, pulling PGOOD low.

Over-Voltage Indication: If the FB voltage rises above 108% of V_{REF}, the internal switch also turns on, forcing PGOOD low.

Recovery: After an under-voltage event, the FB voltage must rise above 94% of V_{REF} for PGOOD to return high. After an over-voltage event, it must fall below 105% of V_{REF}.

All state transitions incorporate a built-in 25μs deglitch delay to prevent false triggering.

Programmable Switching Frequency

The SGM64A00Q offers two methods for setting the switching frequency (f_{SW}): using a resistor (R_{RT}) between the RT pin and AGND, or synchronizing to an external clock signal through the SYNCIN pin. This section describes the method of setting the free-running frequency through the R_{RT} resistor. External clock synchronization is detailed in the Synchronization section.

The free-running switching frequency can be set from 100kHz to 1MHz through the R_{RT} resistor. The value of R_{RT} for a given free-running switching frequency can be calculated by Equation 3.

$$R_{RT}(k\Omega) = \frac{10^4}{f_{SW}(kHz)} \quad (3)$$

Table 1 provides E96 standard resistor values for setting common switching frequencies.

Table 1. Frequency vs. Resistors

Frequency (kHz)	Resistor (kΩ)
100	100
200	49.9
250	40.2
300	33.2
400	24.9
500	20
750	13.3
1000	10

DETAILED DESCRIPTION (continued)

Synchronization and Selectable DCM Mode

The SGM64A00Q integrates external clock synchronization and selectable DCM mode into the SYNCIN pin. The dual-function SYNCIN pin accepts two types of input: a DC logic level signal for selectable DCM mode control or an active clock signal for synchronization.

Selectable DCM Mode: A low logic level enables low-side zero-crossing detection comparator. This comparator senses the SW node voltage to detect reverse current flow and switches off the low-side MOSFET once reverse current is detected. In DCM, the high-side MOSFET remains off as long as the COMP output voltage is below 300mV. The benefit of this configuration is reduced power loss under no-load and light-load conditions, while the impact is a slower transient response at light loads.

A high level disables low-side zero-crossing detection, forcing the system in CCM operation, with its switching frequency set by the free-running frequency determined by the R_{RT} resistor.

Synchronization: When SYNCIN is used as a synchronous clock input, the external clock signal must meet the following specifications: a frequency range of 100kHz to 1MHz, a tolerance within -20% to +50% of the free-running frequency set by R_{RT}, a maximum amplitude of 13V, and a minimum pulse width of 50ns.

The delay from the rising edge of SYNCIN to the rising edge of the SW voltage is approximately 320ns. The delay from the rising edge of SW to the rising edge of SYNCOUT equals $T_{SW}/2$ - 320ns. Figure 5 shows the application circuit with two SGM64A00Q devices cascaded through the SYNCIN and SYNCOUT connection. By connecting the SYNCOUT of one SGM64A00Q to the SYNCIN of another, the two devices achieve 180° out-of-phase SW signals, which minimizes input voltage ripple and system EMI by interleaving the input current pulses, thus reducing the peak current demand and smoothing the total input current waveform.

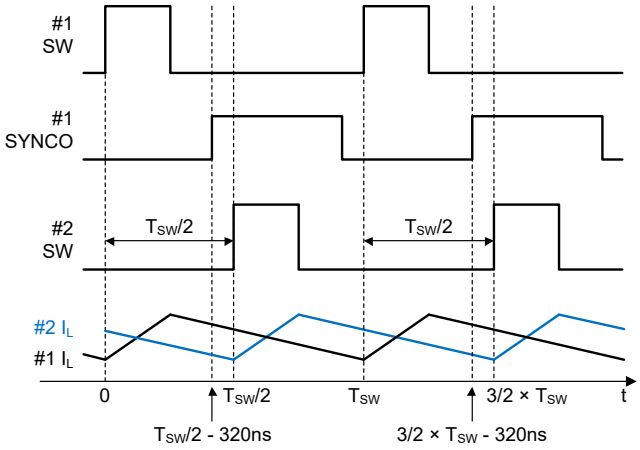


Figure 4. Timing Diagram of Figure 5

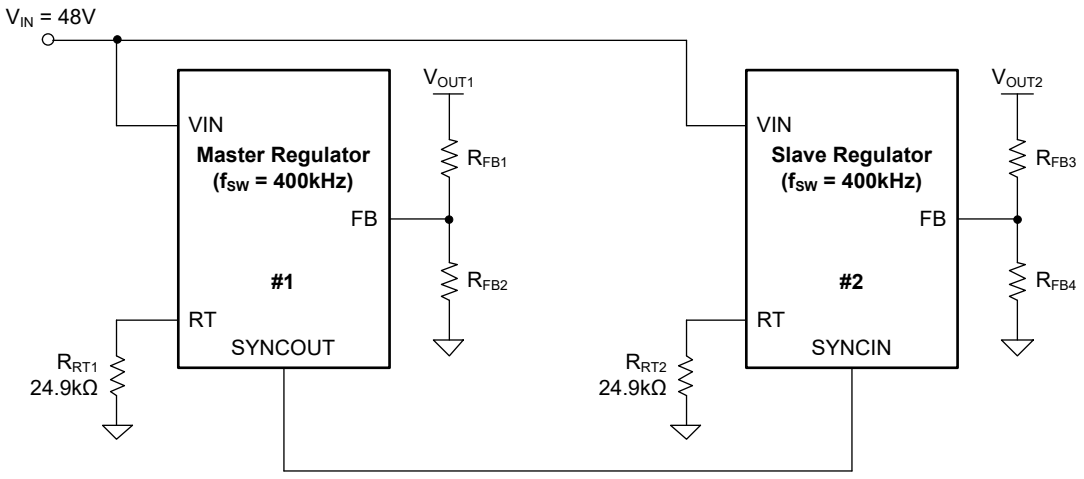


Figure 5. Synchronized Application Circuit Diagram

DETAILED DESCRIPTION (continued)

Configurable Soft-Start and Tracking

The SGM64A00Q can be configured with external components at the SS/TRK pin to implement either soft-start function or output tracking of a target voltage.

Soft-Start: The soft-start function prevents the converter output voltage from overshooting during startup while also reducing stress on the input supply rail. When the EN/UVLO voltage exceeds 1.2V and VCC rises above VCC under-voltage threshold, the SGM64A00Q initiates startup. A 10μA current source charges the external soft-start capacitor connected between the SS/TRK pin and GND, generating a soft-start voltage (V_{SS}) that ramps from 0V to 0.8V. When V_{SS} is lower than the internal V_{REF}, V_{SS} overrides V_{REF} and becomes the reference for the error amplifier. Once V_{SS} exceeds V_{REF}, control reverts to V_{REF}.

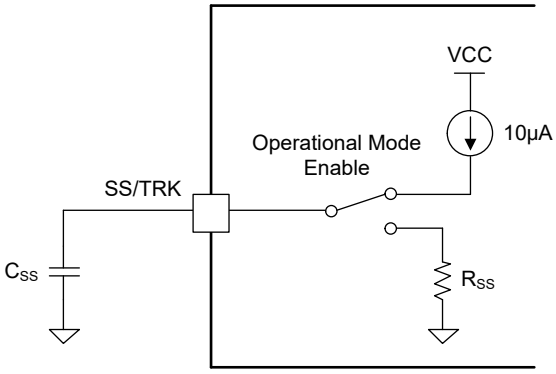


Figure 6. Soft-Start Application Circuit Diagram

An internal clamp circuit at the SS/TRK pin limits V_{SS} to no more than V_{FB} + 115mV, allowing soft-start recovery after an overload event. For circuit stability, a soft-start capacitance of at least 2nF is required, while the clamp circuit features an approximate current limit of 2mA.

The soft-start time (t_{SS}) is set by the external SS capacitor (C_{SS}) and can be calculated using Equation 4.

$$t_{SS} = \frac{C_{SS} \times V_{REF}}{I_{SS}} \quad (4)$$

where,

C_{SS} is the soft-start capacitance.

V_{REF} is the 0.8V FB reference voltage.

I_{SS} is the 10μA capacitor charging current sourced from the SS/TRK pin.

Tracking: Leveraging the characteristic that the SS/TRK voltage serves as the reference when below 0.8V, the SS/TRK pin can also serve as a tracking input for master-slave voltage tracking. This is achieved by dividing down the master output voltage with a resistor network, supporting three tracking modes: coincident, ratiometric, and offset. Figure 7 illustrates two practical tracking configurations.

The design can be configured to enable either soft-start or voltage-tracking functionality as required. In all cases, the output voltage ramp rate must be managed to prevent current limit during startup, and the steady-state SS/TRK voltage should be kept at least 100mV above FB to ensure regulation by the internal V_{REF} for accuracy.

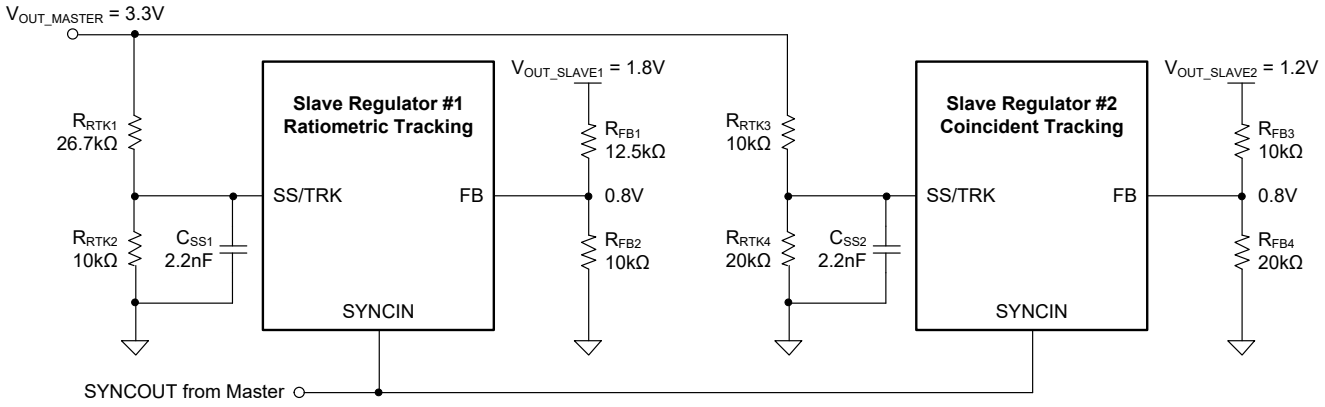


Figure 7. Coincident and Ratiometric Tracking Mode Application Circuit Diagram

DETAILED DESCRIPTION (continued)

Gate Drivers

Operating at V_{VCC} = 7.5V, the gate drivers provide 2.1Ω pull-up and 0.9Ω pull-down impedance for both high-side and low-side switches, with peak drive capabilities of 2A source and 3A sink. The controller employs fixed dead times of 25ns (turn-on) and 20ns (turn-off). This driver performance translates into fast switching transitions, lower switching loss, and higher system efficiency.

Note that the controller uses fixed dead-time control. Any externally added gate resistance must be carefully evaluated against the SW node rise/fall rates to prevent cross-conduction.

Voltage-Mode Control

The SGM64A00Q features a voltage-mode control architecture with integrated input voltage feed-forward. The controller generates the PWM signal by comparing the error-amplifier output (V_{COMP}) with a ramp voltage, which drives the external MOSFETs to regulate the output voltage. The added feed-forward structure adjusts the ramp amplitude in real time according to the input voltage V_{IN}, with a feed-forward gain k_{FF} of 15, satisfying the relationship V_{IN}/V_{RAMP} = 15. The feed-forward loop ensures system stability across the entire input voltage range by providing a constant gain, which also significantly simplifies loop compensation design.

Current Sensing

The SGM64A00Q implements cycle-by-cycle over-current protection by sampling the inductor current during the low-side MOSFET on-time. It supports two current sense schemes: by sensing the voltage across the low-side MOSFET's on-resistance (R_{DSON}), or by measuring the voltage across a low-side shunt resistor (R_{SENSE}). The circuit diagrams for these two current sense modes are shown in Figure 8 and Figure 9, respectively.

To set the current-limit threshold, an external resistor R_{ILIM} must be connected in series with the ILIM pin. In R_{DSON} mode, the opposite end of R_{ILIM} is tied to the drain of the low-side MOSFET to use the MOSFET's on-resistance as the sense element. In R_{SENSE} mode, it is connected to the junction between the low-side MOSFET source and the shunt resistor, using an external sense resistor for detection.

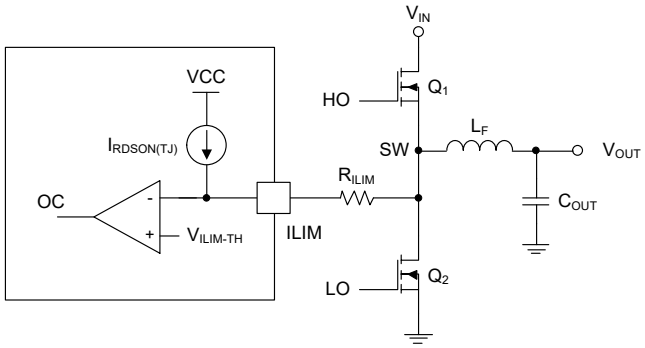


Figure 8. R_{DSON} Mode Current Sensing

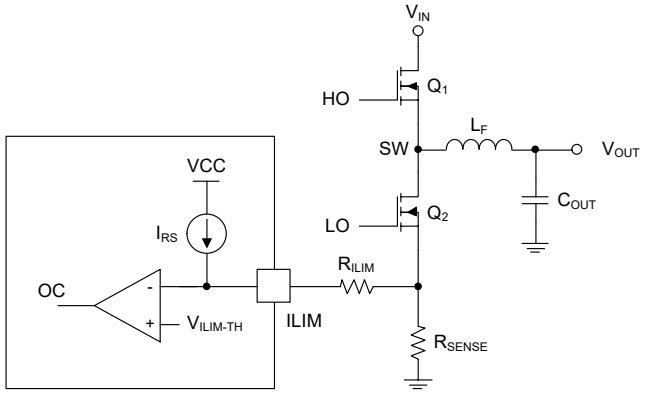


Figure 9. R_{SENSE} Mode Current Sensing

After power-up, the SGM64A00Q automatically detects the circuit configuration and adjusts the constant reference current sourced from the ILIM pin accordingly: 200μA for R_{DSON} mode and 100μA for R_{SENSE} mode. To compensate for the temperature variation of the low-side MOSFET's on-resistance, the ILIM current in R_{DSON} mode features a temperature coefficient of +4500 ppm/℃. The sum of the voltage across R_{ILIM} and the inductor current sense voltage (across R_{DSON} or R_{SENSE}) is compared to the internal current limit reference. If an over-current condition is detected, the controller suspends switching and holds the low-side MOSFET on until the over-current state clears.

DETAILED DESCRIPTION (continued)

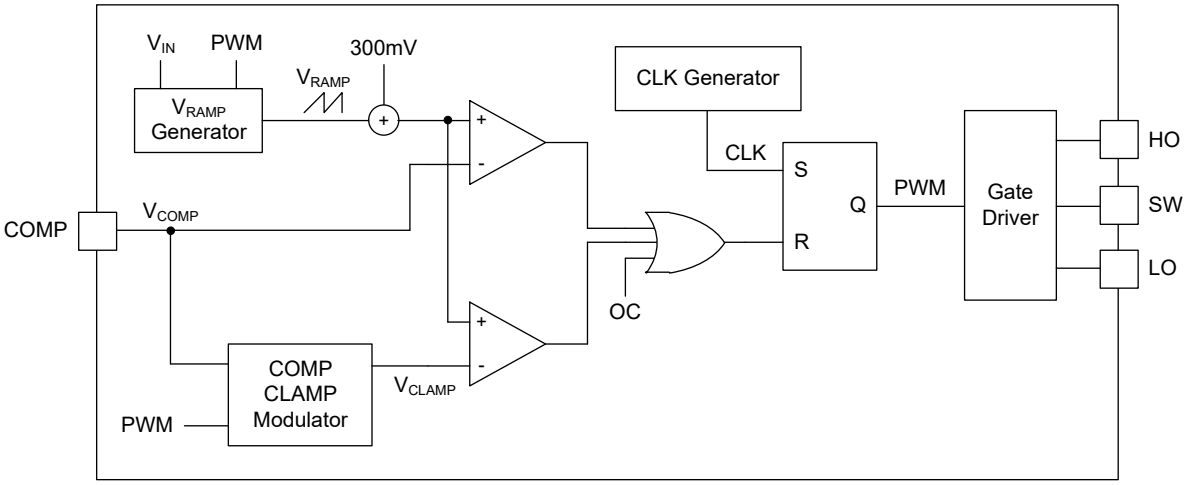


Figure 10. OCP and COMP CLAMP Duty Cycle Control Circuit Diagram

The value of R_{ILIM} can be calculated using Equation 5, based on the selected sensing mode.

$$R_{ILIM} = \begin{cases} \dfrac{I_{OUT} - \Delta I_L / 2}{I_{RDSON}} \times R_{DSON}, & R_{DSON}\ \text{Mode} \\ \dfrac{I_{OUT} - \Delta I_L / 2}{I_{RS}} \times R_{SENSE}, & R_{SENSE}\ \text{Mode} \end{cases} \quad (5)$$

Where,

ΔI_L is the peak-to-peak inductor ripple current.

R_{DSON} is the on-resistance of the low-side MOSFET.

I_{RDSON} is the 200μA ILIM pin current in R_{DSON} mode.

R_{SENSE} is the resistance of the current-sensing shunt element.

I_{RS} is the 100μA ILIM pin current in R_{SENSE} mode.

Designers should note the following for current-limit circuit design.

In R_{DSON} sensing mode, due to the large voltage swing at the ILIM pin, a capacitor C_{ILIM} must be connected between ILIM and PGND to ensure proper operation of the current limit circuit, and the time constant should meet $R_{ILIM} \times C_{ILIM} \approx 6ns$. Because of the physical separation between the MOSFET and the controller on the PCB, the internal temperature sampling cannot fully track the actual MOSFET junction temperature; moreover, the R_{DSON} of the MOSFET varies non-linearly with temperature. As a result, the over-current protection threshold based on R_{DSON} will exhibit some deviation over-temperature.

If the R_{SENSE} sensing mode is used, the external shunt resistor can improve protection accuracy across the full temperature range. However, it introduces additional conduction loss and increases layout complexity and cost. Therefore, this scheme is generally not recommended for high-current applications unless precise current limit accuracy over the operating temperature range is a critical system requirement.

Over-Current Protection and COMP Clamp

To protect the high-side switch while using low-side current sensing, the SGM64A00Q integrates an internal duty-cycle limiter that prevents the high-side MOSFET from being damaged by severe over-current. The V_{COMP} includes an internal voltage clamp (V_{CLAMP}). When the V_{COMP} voltage exceeds V_{CLAMP} as shown in Figure 10, the internal comparator automatically switches to use V_{CLAMP} for PWM generation, which limits duty cycle and provides current limiting protection.

During normal operation, the V_{CLAMP} is regulated above the V_{COMP} to ensure sufficient headroom for load-step transient response. Once the over-current is detected, the V_{CLAMP} is regulated to a lower level, decreasing the duty-cycle. If the over-current condition persists for 128 consecutive clock cycles, the system pulling the SS/TRK pin low for 8192 clock cycles and then automatically reinitiating the soft-start sequence. The complete over-current protection flow is illustrated in Figure 11.

DETAILED DESCRIPTION (continued)

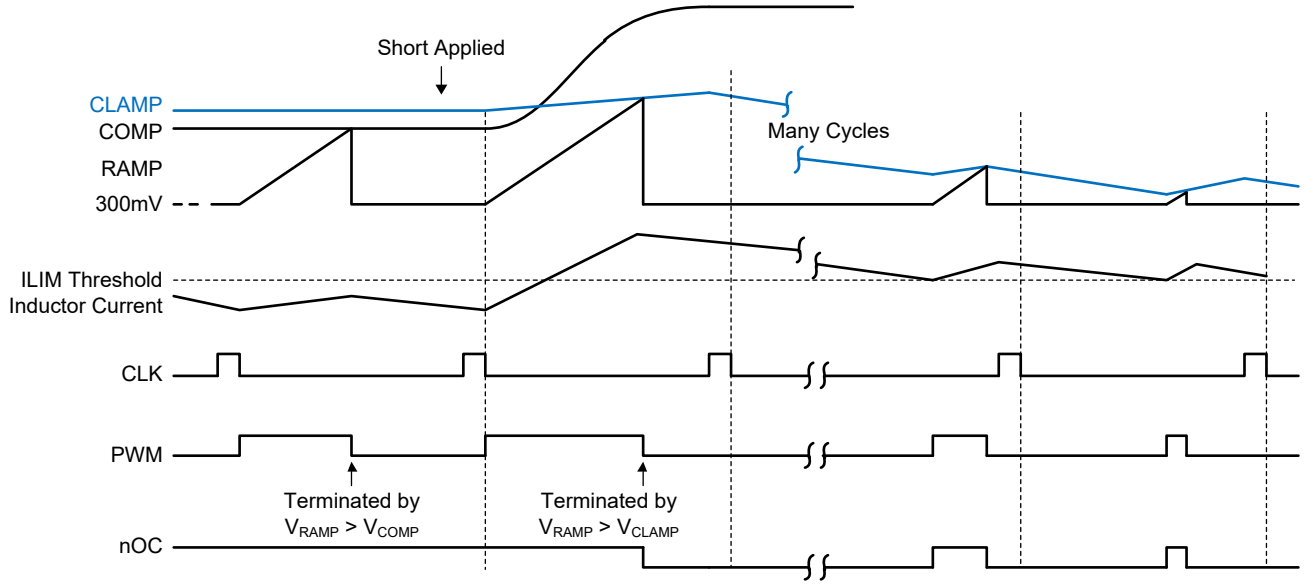


Figure 11. OCP Duty Cycle Limiting Waveforms

Over-Temperature Protection

The SGM64A00Q integrates an over-temperature protection (OTP) circuit. The primary protection function is thermal shutdown, which activates when the junction temperature exceeds +175℃. Upon entering this state, the device performs the following sequence: it turns off both the high-side and low-side MOSFETs, pulls the SS/TRK and PGOOD pins low, and disables the VCC regulator. The device recovers from thermal shutdown once the junction temperature decreases by 20 ℃, and a soft-start sequence is automatically reinitiated.

APPLICATION INFORMATION

Power Train Components

Inductor

When selecting an inductor, a larger inductance generally provides lower ripple current and reduced output ripple voltage (ΔV_{IN}), but it also leads to larger physical size, larger series resistance, and lower saturation current. Therefore, most applications require a balanced consideration of these factors. Typically, it is recommended to choose an inductor with a DC current rating at least 25% above the maximum load current and to design the inductor ripple current to be between 30% and 40% of the maximum load current. The inductance can be calculated with Equation 6, and maximum inductor peak current can be calculated with Equation 7:

$$L_F = \frac{V_{OUT}}{V_{IN}} \times \left(\frac{V_{IN} - V_{OUT}}{\Delta I_L \times f_{SW}} \right) \quad (6)$$

$$I_{L\_PEAK} = I_{OUT} + \frac{\Delta I_L}{2} \quad (7)$$

where,

I_{L_PEAK} is the maximum inductor peak current.

I_{OUT} is the load current.

ΔI_L is the peak-to-peak inductor ripple current.

Output Capacitors

The regulator requires the output capacitors to maintain voltage stability and to meet ripple specifications under both steady state and dynamic conditions. The electrical and physical characteristics of capacitors differ significantly by technology. To achieve balanced performance, ceramic capacitors are often combined with tantalum or electrolytic types. The ceramics capacitors deliver extremely low ESR, reducing output voltage ripple and noise spikes, while the tantalum or electrolytic capacitors supply large capacitance in a compact footprint to handle load transients.

Selection capacitance is based on the following two calculations.

Static Ripple Specification: For a given peak-to-peak output voltage ripple (ΔV_{OUT}), the output capacitance must exceed the value calculated from Equation 8.

$$C_{OUT} \geq \frac{\Delta I_L}{8 \times f_{SW} \times \sqrt{\Delta V_{OUT}^2 - \left(R_{ESR} \times \Delta I_L\right)^2}} \quad (8)$$

Dynamic Overshoot Specification: For a load-step-down transient overshoot ($\Delta V_{OVERSHOOT}$, corresponding to an output current step reduction of ΔI_{OUT}), the output capacitance must exceed the value given by the corresponding equation.

$$C_{OUT} \geq \frac{L_F \times \Delta_{IOUT}^2}{\left(V_{OUT} + \Delta V_{OVERSHOOT}\right)^2 - V_{OUT}^2} \quad (9)$$

Use Equation 8 to get the minimum ceramic capacitance and the Equation 9 to decide whether electrolytic or tantalum capacitors need to be added. Both calculations should be evaluated to determine the final output capacitance value and the composite capacitor arrangement.

Input Capacitors

To maintain stable input voltage for the regulator, the input capacitors need to effectively suppress the input ripple caused by switching currents. In theory, the DC component of the input current is supplied by the upstream source, and the AC component is provided by the input filter capacitors. Neglecting inductor ripple, the RMS current of the input capacitor can be calculated using Equation 10. The worst case condition occurs at $V_{IN} = 2 \times V_{OUT}$, where $I_{RMS} = I_{OUT}/2$. Therefore, the selected input capacitor must be rated to handle this RMS current. If a specific input ripple voltage (ΔV_{IN}) is defined, the minimum required input capacitance can be determined from Equation 11.

$$I_{CIN\_RMS} = \sqrt{D \times \left(I_{OUT}^2 \times (1-D) + \frac{\Delta I_L^2}{12} \right)} \quad (10)$$

$$C_{IN} \geq \frac{D \times (1-D) \times I_{OUT}}{f_{SW} \times \left(\Delta V_{IN} - R_{ESR} \times I_{OUT}\right)} \quad (11)$$

where,

R_{ESR} is equivalent series resistance of input capacitors.

In applications, ceramic capacitors are often placed in parallel with electrolytic capacitors to optimize input filtering. The capacitor selection should be based on its rated ripple current and operating temperature. Furthermore, to minimize parasitic inductance in the switching loop, the input capacitors should be placed as close as possible to the drain of the high-side MOSFET and the source of the low-side MOSFET.

APPLICATION INFORMATION (continued)

Power MOSFETs

Power MOSFET selection determines the efficiency of a DC/DC regulator. MOSFETs with low on-state resistance (R_{DSON}) reduce conduction loss, while low parasitic capacitance enables faster switching and minimizes crossover loss. For a semiconductor technology, the figure of merit (FOM) of product, FOM = $R_{DSON} \times Q_g$, is widely adopted as a key to evaluate this balance. A lower R_{DSON} is invariably accompanied by higher gate charge (Q_g) and output charge (Q_{OSS}), and vice versa. Selecting a MOSFET requires balancing this trade-off by carefully matching the device characteristics to the application's operational demands.

Key parameters to consider during selection include:

On-resistance: R_{DSON} at V_{GS} = 7.5V.

Voltage rating: Drain-source breakdown voltage (BV_{DSS}), which must exceed the maximum input voltage.

Charge parameters: Q_g at V_{GS} = 7.5V and Q_{OSS} at the relevant input voltage.

Body-diode characteristics: Reverse-recovery charge (Q_{RR}).

Turn-on threshold: Gate-threshold voltage (V_{GS-TH}).

The relevant power-loss equations are summarized in Table 2, covering the major switching and drive losses and can be used for initial estimation.

In high step-down ratio applications, the low-side MOSFET conducts for a larger portion of the cycle, resulting in higher conduction loss. Therefore, selecting a MOSFET with low R_{DSON} is essential for achieving high system efficiency. If the conduction loss of a single MOSFET is too high or the target R_{DSON} cannot be met with one device, two low-side MOSFETs can be connected in parallel to share the current and reduce the total effective on-resistance.

Control Loop Compensation

In the design of a voltage-mode controlled Buck regulator, the LC output filter of the power stage introduces a double pole. This causes the system's open-loop gain to roll off at a rate of -40dB/dec at its resonant frequency and generates a phase lag approaching 180°, severely limiting the system bandwidth and compromising loop stability. To counteract this issue, a Type-III compensation network (characterized by two zeros and three poles) is commonly used to stabilize the loop. It introduces two zeros to counteract the LC double pole. Of its three poles, one is fixed at the origin to ensure high DC gain, one is placed to cancel the output capacitor's ESR zero, and the third is set at half the switching frequency to attenuate high-frequency noise. Table 3 summarizes the small-signal models and the corresponding pole-zero formulations for the voltage-mode Buck regulator.

Table 2. Buck Regulator MOSFET Power Losses

Power Loss Mode	High-Side MOSFET	Low-Side MOSFET
MOSFET Conduction	$P_{COND1} = D \times \left({I_{OUT}}^2 + \frac{\Delta {I_L}^2}{12} \right) \times R_{DSON1}$	$P_{COND2} = D' \times \left({I_{OUT}}^2 + \frac{\Delta {I_L}^2}{12} \right) \times R_{DSON2}$
MOSFET Switching	$P_{SW1} = \frac{V_{IN} \times f_{SW}}{2} \times \left[\left(I_{OUT} - \frac{\Delta I_L}{2} \right) \times t_R + \left(I_{OUT} + \frac{\Delta I_L}{2} \right) \times t_F \right]$	Negligible
MOSFET Gate Drive	$P_{GATE1} = V_{CC} \times f_{SW} \times Q_{G1}$	$P_{GATE2} = V_{CC} \times f_{SW} \times Q_{G2}$
MOSFET Output Charge	$P_{C\_OSS} = f_{SW} \times \left(V_{IN} \times Q_{OSS2} + E_{OSS1} - E_{OSS2} \right)$	
Body Diode Conduction	N/A	$P_{COND\_BD} = V_F \times f_{SW} \times \left[\left(I_{OUT} + \frac{\Delta I_L}{2} \right) \times t_{DT1} + \left(I_{OUT} - \frac{\Delta I_L}{2} \right) \times t_{DT2} \right]$
Body Diode Reverse Recovery	$P_{RR} = V_{IN} \times f_{SW} \times Q_{RR2}$	

APPLICATION INFORMATION (continued)

Table 3. Voltage Mode Buck Regulator Small-Signal Analysis

Transfer Function	Expression
Open-Loop Transfer Function	$T_V(s)=\frac{\hat{V}_{COMP}(s)}{\hat{V}_O(s)}\times\frac{\hat{V}_O(s)}{\hat{d}(s)}\times\frac{\hat{d}(s)}{\hat{V}_{COMP}(s)}=G_C(s)\times G_{VD}(s)\times F_M$
Duty-Cycle-to-Output Transfer Function	$G_{VD}(s)=\frac{\hat{V}_O(s)}{\hat{d}(s)}=V_{IN}\times\frac{1+\frac{s}{\omega_{ESR}}}{1+\frac{s}{Q_O\times\omega_O}+\frac{s^2}{\omega_O^2}}$, $\omega_{ESR}=\frac{1}{R_{ESR}\times C_{OUT}}$, $\omega_O\approx\frac{1}{\sqrt{C_{OUT}\times L_F}}$, $Q_O\approx R_L\times\sqrt{\frac{C_{OUT}}{L_F}}$
Compensator Transfer Function	$G_C(s)=\frac{\hat{V}_{COMP}(s)}{\hat{V}_O(s)}=\frac{\left(1+\frac{s}{\omega_{Z1}}\right)\times\left(1+\frac{s}{\omega_{Z2}}\right)}{\frac{s}{\omega_{P0}}\times\left(1+\frac{s}{\omega_{P1}}\right)\times\left(1+\frac{s}{\omega_{P2}}\right)}$, $\omega_{Z1}=\frac{1}{R_{C1}\times C_{C1}}$, $\omega_{Z2}=\frac{1}{(R_{FB1}+R_{C2})\times C_{C3}}$, $\omega_{P0}\approx\frac{1}{R_{FB1}\times C_{C1}}$, $\omega_{P1}\approx\frac{1}{R_{C1}\times C_{C1}}$, $\omega_{P2}=\frac{1}{R_{C2}\times C_{C3}}$
Modulator Transfer Function	$F_M=\frac{\hat{d}(s)}{\hat{V}_{COMP}(s)}=\frac{1}{V_{RAMP}}$

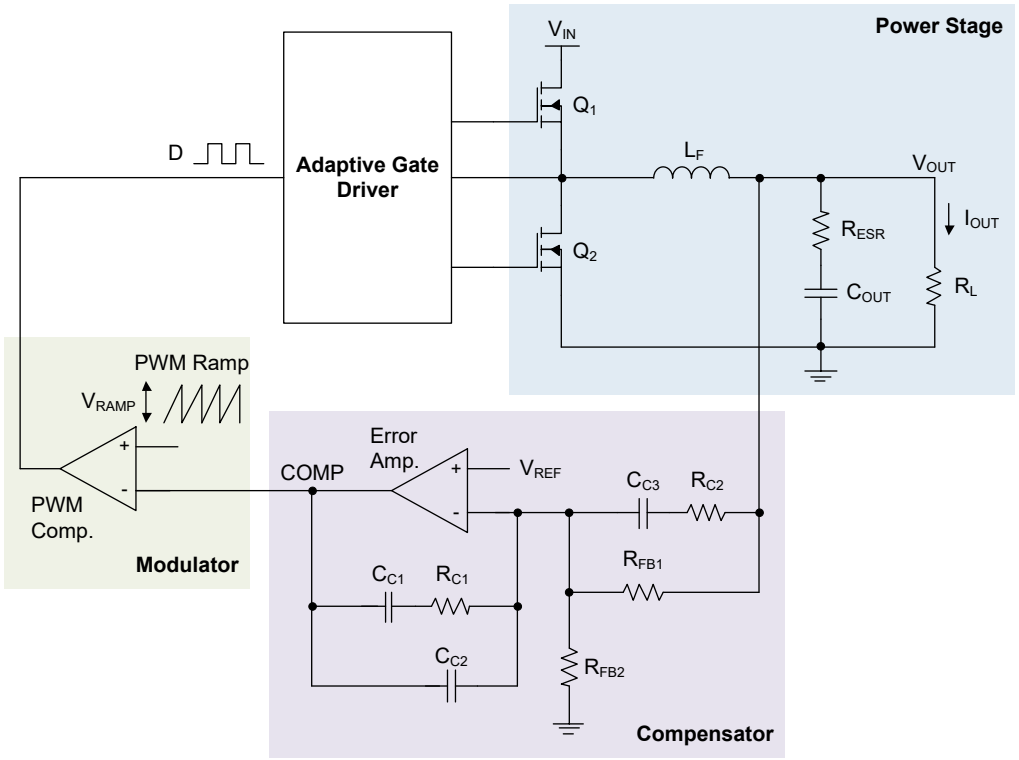


Figure 12. Feed-Forward Compensated Voltage-Mode Control Loop Analysis Diagram

APPLICATION INFORMATION (continued)

The compensation design for a voltage-mode Buck regulator follows a systematic procedure.

Initially, the feedback voltage divider network (R_{FB1}, R_{FB2}) must be defined based on the target output voltage and the reference voltage (V_{REF}). This step is foundational as the feedback factor directly participates in the compensator gain computation. Following this, the core performance objectives need to be established. The loop bandwidth is defined by setting the target crossover frequency ($f_C = \omega_C/2\pi$), typically within a range of one-tenth to one-fifth of the switching frequency, to balance dynamic response speed against noise rejection. And the target phase margin is set within 50° to 70° to ensure stability and good transient response.

Next, the inherent characteristic parameters of the power stage, such as the LC resonant frequency and the ESR zero frequency of the output capacitor, are determined. With these parameters defined, the zeros and poles of the Type-III compensator are configured according to the standard guidelines: $\omega_{z1} = 0.5 \times \omega_O$, $\omega_{z2} = \omega_O$, $\omega_{P1} = \omega_{SW}/2$, $\omega_{P2} = \omega_{ESR}$. Using the design formulas provided in Table 4, the specific parameter values for the compensation network resistors R_{C1}, R_{C2} and capacitors C_{C1}, C_{C2}, C_{C3} are calculated, thereby completing the compensation design for the entire loop.

Table 4. Compensation Component Calculation

Resistors	Capacitors
$R_{FB2} = \frac{R_{FB1}}{(V_{OUT}/V_{REF})-1}$	$C_{C1} = \frac{1}{\omega_{Z1} \times R_{C1}}$
$R_{C1} = \frac{\omega_C}{\omega_O} \times \frac{1}{k_{FF}} \times R_{FB1}$	$C_{C2} = \frac{1}{\omega_{P1} \times R_{C1}}$
$R_{C2} = \frac{1}{\omega_{P2} \times C_{C3}}$	$C_{C3} = \frac{1}{\omega_{Z2} \times R_{FB1}}$

The design results can be verified using a Bode plot (as shown in Figure 13). Compensation should exhibit a gain curve crossing the 0dB line with a slope of approximately -20dB/dec and possess sufficient phase margin at the crossover frequency. This ensures the system achieves the desired bandwidth while maintaining stable and reliable dynamic performance.

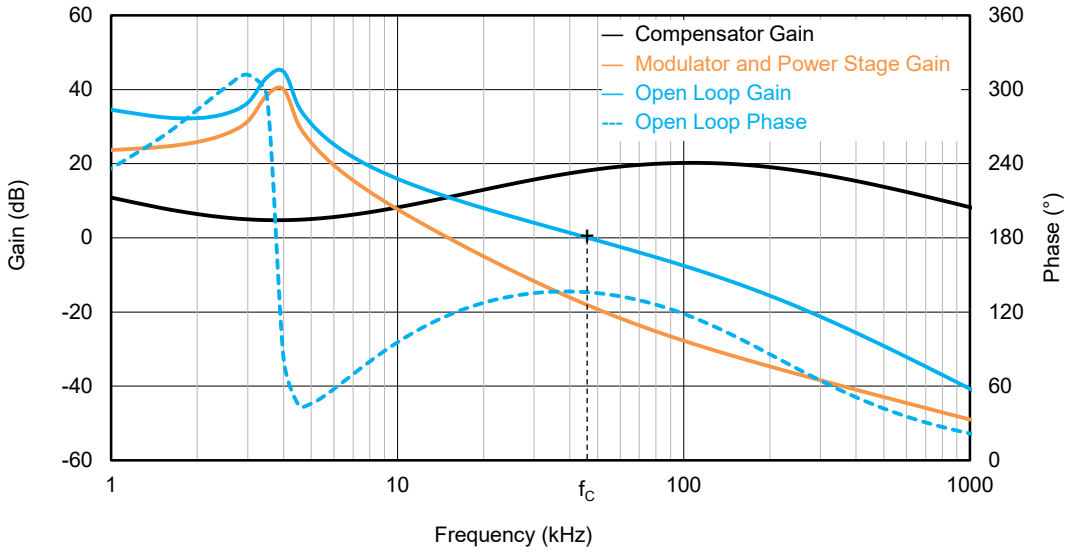


Figure 13. Voltage-Mode Controlled Buck Regulator: Bode Plot of Loop Gain – Module Decomposition and Synthesis

APPLICATION INFORMATION (continued)

Typical Applications Circuits

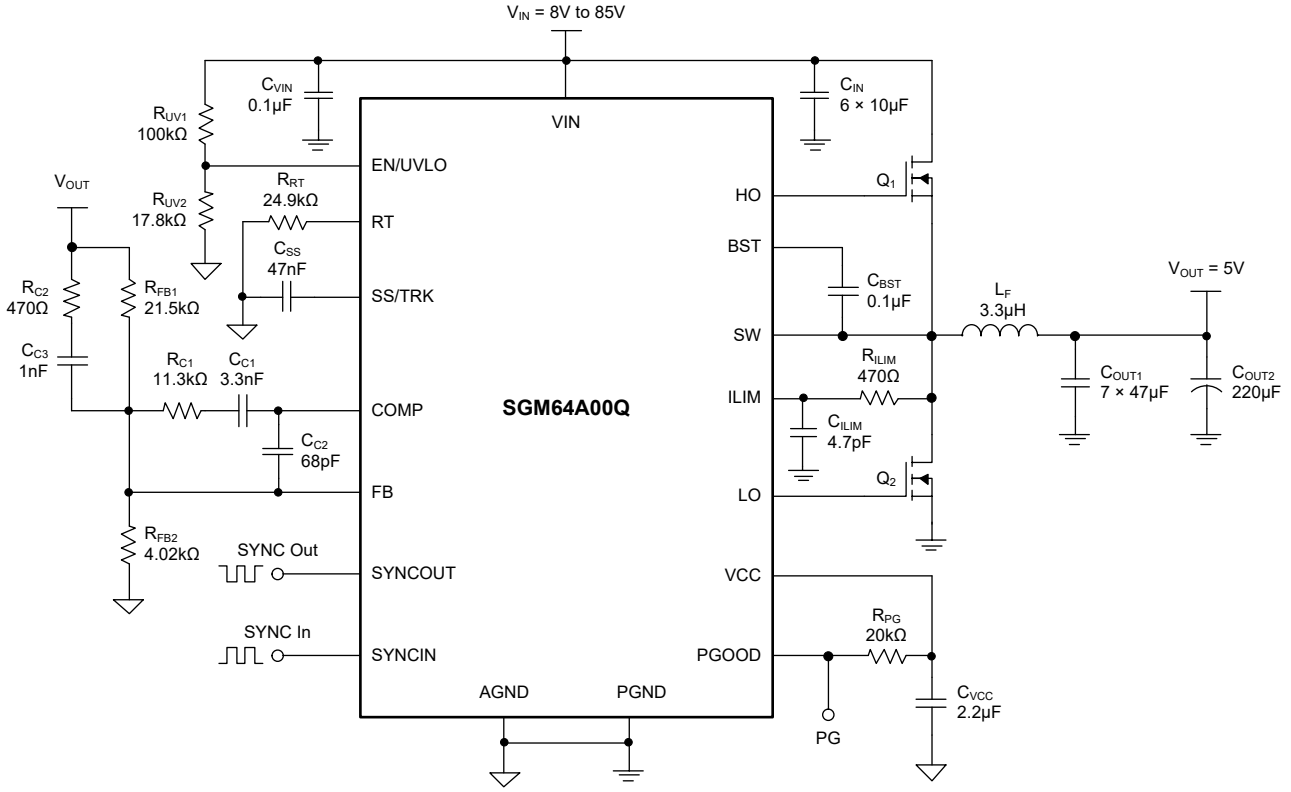


Figure 14. R_{DSON} Application Circuit with SGM64A00Q 48V to 5V, 10A Buck Regulator at 400kHz

Table 5. List of Materials

Reference Designator	Qty	Specification	Manufacturer	Part Number
C_{IN}	6	10μF, 100V, X7S, 1210, ceramic	Murata	GRM32EC72A106KE05L
C_{OUT1}	7	47μF, 10V, X7R, 1210, ceramic	Murata	GRM32ER71A476KE15L
C_{OUT2}	1	220μF, 25V, -40℃ to +125℃, D 8mm × L 10mm, electrolytic	NCC	EMVH250ARA221MHA0G
L_F	1	3.3μH, 5.8mΩ, 28.6A, 10.5mm × 10.0mm × 6.5mm	TDK	SPM10065VTT-3R3M-D
		3.3μH, 6.8mΩ, 35A, 12.9mm × 12.9mm × 6.7mm	VISHAY	IHLP5050FDER3R3M01
Q_1	1	100V, 7mΩ, MOSFET, TDSON-8 (5 × 6)	Infineon	BSC0805LS
Q_2	1	100V, 7mΩ, MOSFET, TDSON-8 (5 × 6)	Infineon	BSC0805LS
U_1	1	Wide V_{IN} synchronous Buck controller	SGMICRO	SGM64A00Q

APPLICATION INFORMATION (continued)

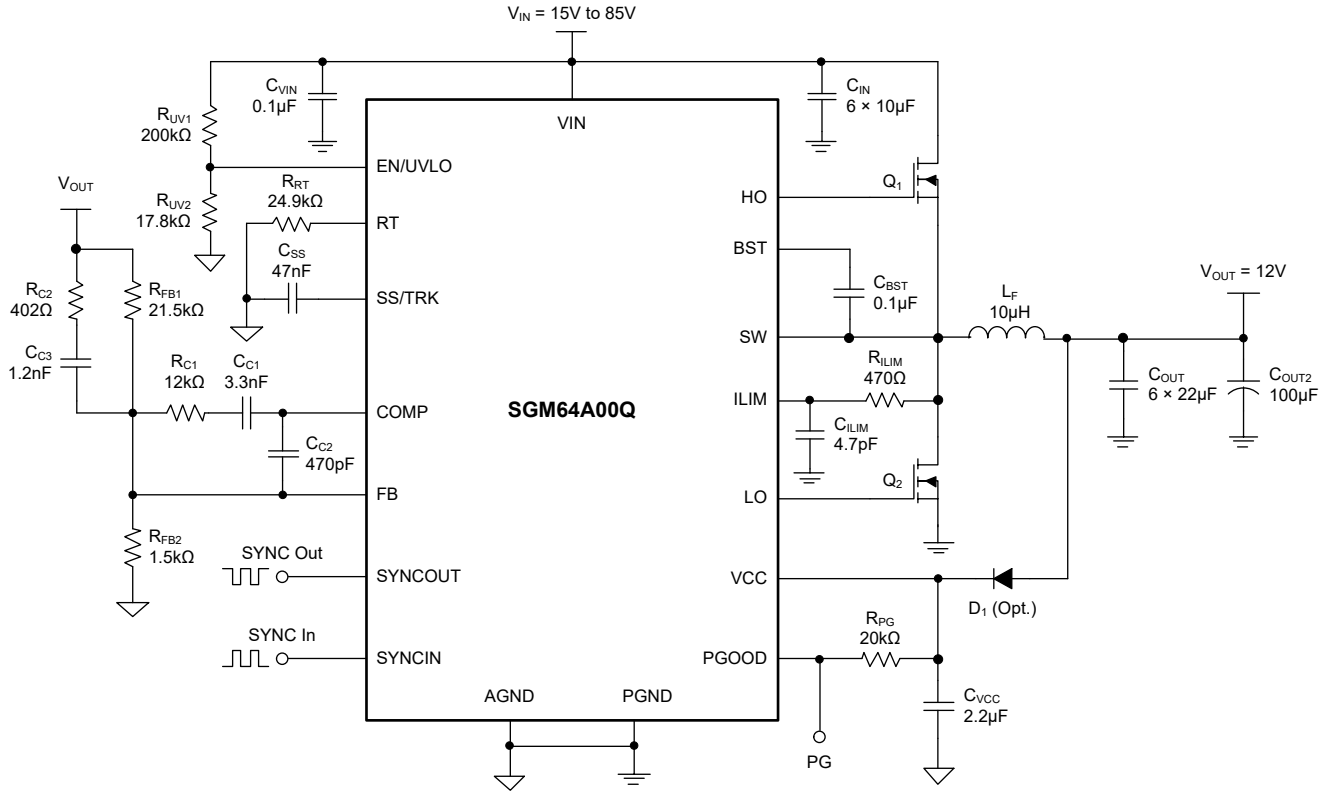


Figure 15. R_{SENSE} Application Circuit with SGM64A00Q 48V to 12V, 10A Buck Regulator at 400kHz

Table 6. List of Materials

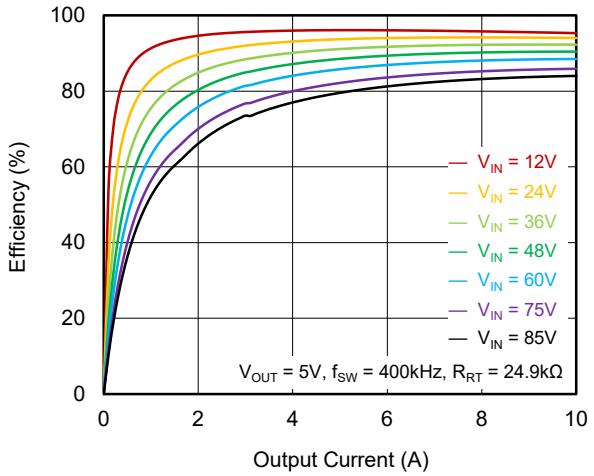
Reference Designator	Qty	Specification	Manufacturer	Part Number
C_{IN}	6	10μF, 100V, X7S, 1210, ceramic	Murata	GRM32EC72A106KE05L
C_{OUT1}	6	22μF, 25V, X7R, 1210, ceramic	Murata	GCM32EC71226KE36L
C_{OUT2}	1	100μF, 63V, -40℃ to +125℃, D 8mm × L 10mm, electrolytic	PANASONIC	EEETG1J101UP
L_F	1	10μH, 11mΩ, 20.3A, 11.6 × 10.5 × 9.1mm	Wurth	78439369100
		10μH, 16.4mΩ, 15.5A, 13.2 × 12.9 × 6.7mm	VISHAY	IHLP5050FDER100M01
Q_1	1	100V, 7mΩ, MOSFET, TDSON-8 (5 × 6)	Infineon	BSC0805LS
Q_2	1	100V, 7mΩ, MOSFET, TDSON-8 (5 × 6)	Infineon	BSC0805LS
U_1	1	Wide V_{IN} synchronous Buck controller	SGMICRO	SGM64A00Q

APPLICATION INFORMATION (continued)

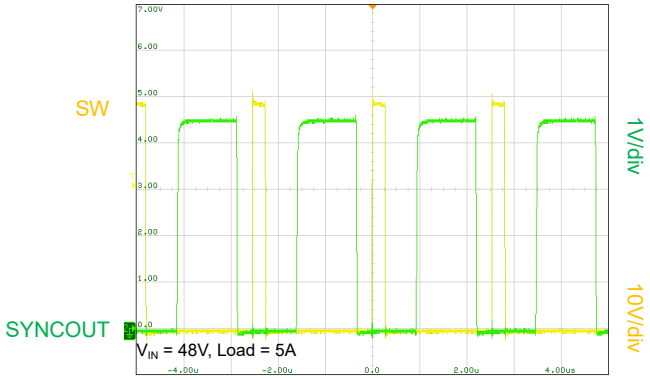
Typical Performance Characteristics

V_{OUT} = 5V, f_{SW} = 400kHz, unless otherwise noted.

Efficiency and Power Loss vs. I_{OUT} and V_{IN}

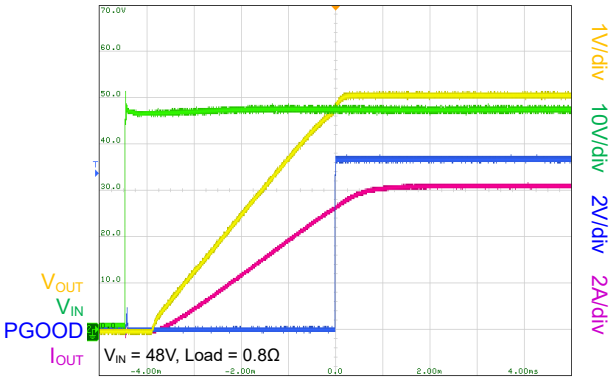


SYNCOUT and SW Node Voltages



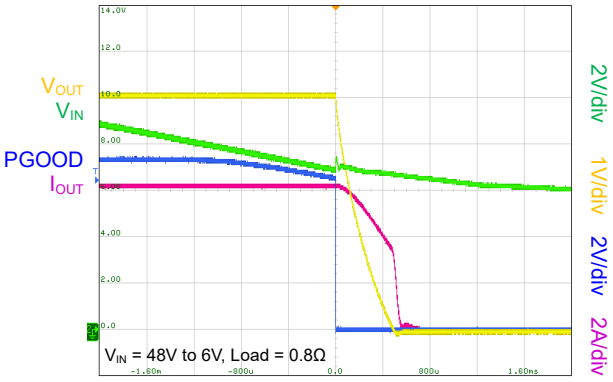
Time (1μs/div)

Startup, Resistive Load



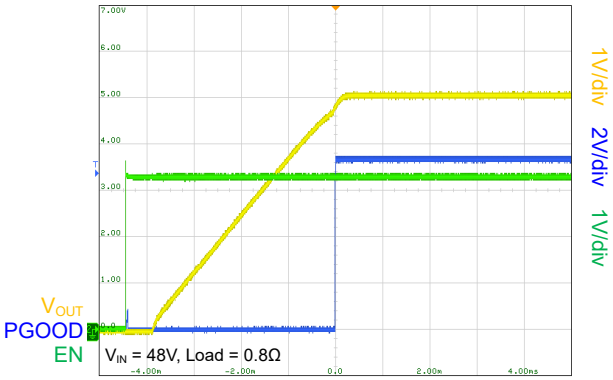
Time (1ms/div)

Shutdown Through UVLO



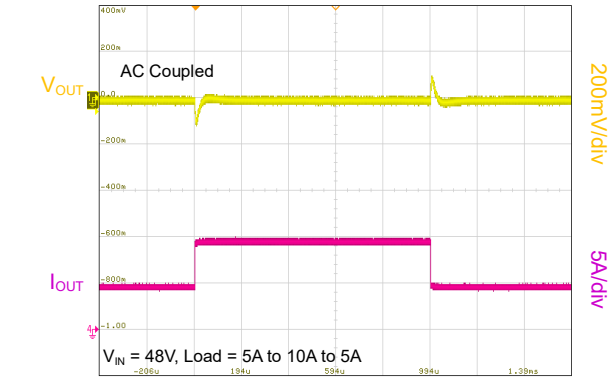
Time (400μs/div)

ENABLE On, Resistive Load



Time (1ms/div)

Load Transient Response

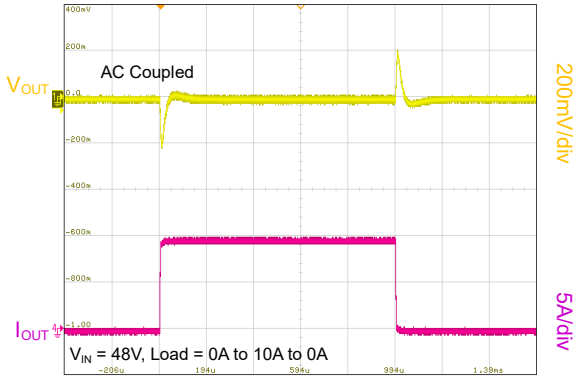


Time (200μs/div)

APPLICATION INFORMATION (continued)

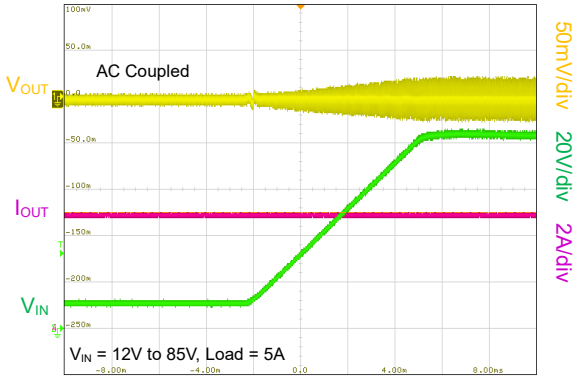
V_{OUT} = 5V, f_{SW} = 400kHz, unless otherwise noted.

Load Transient Response



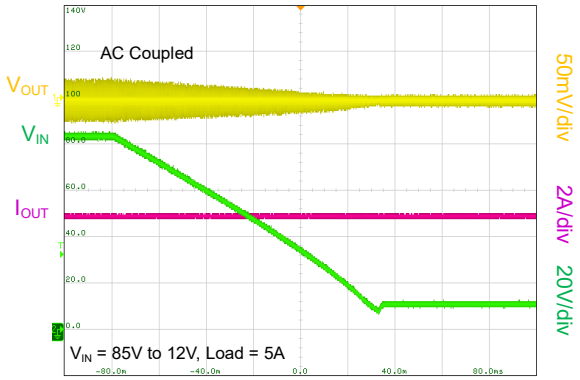
Time (200μs/div)

Line Transient Response, 12V to 85V



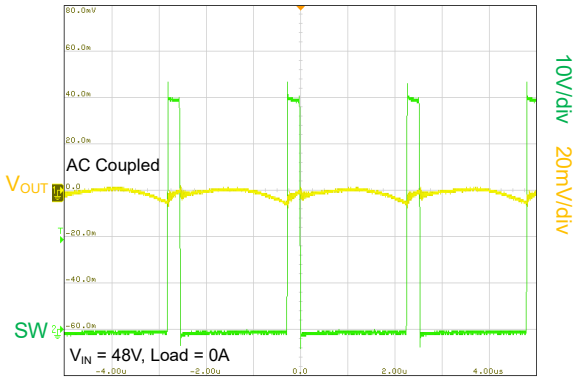
Time (2ms/div)

Line Transient Response, 85V to 12V



Time (20ms/div)

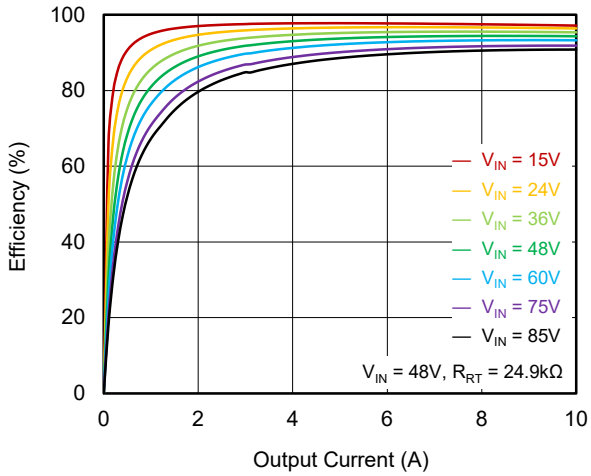
SW Node and Output Ripple Voltages



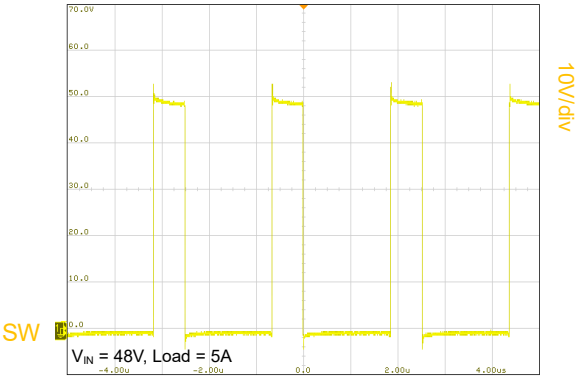
Time (1μs/div)

V_{OUT} = 12V, f_{SW} = 400kHz, unless otherwise noted.

Efficiency and Power Loss vs. I_{OUT} and V_{IN}



SW Node Voltages

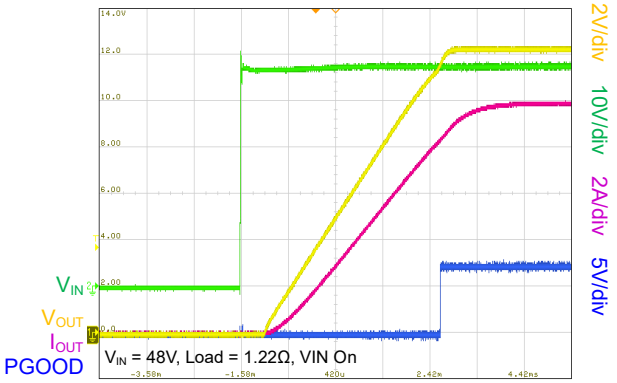


Time (1μs/div)

APPLICATION INFORMATION (continued)

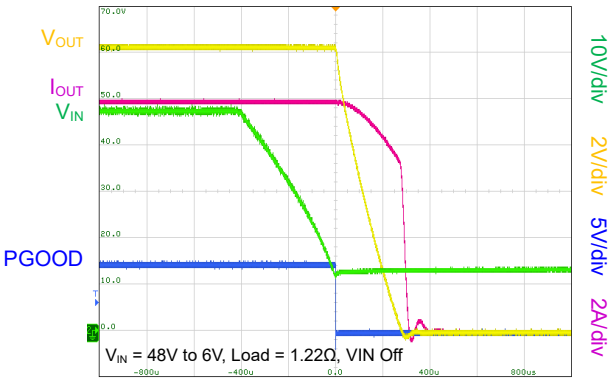
V_{OUT} = 12V, f_{SW} = 400kHz, unless otherwise noted.

Startup, 10A Resistive Load



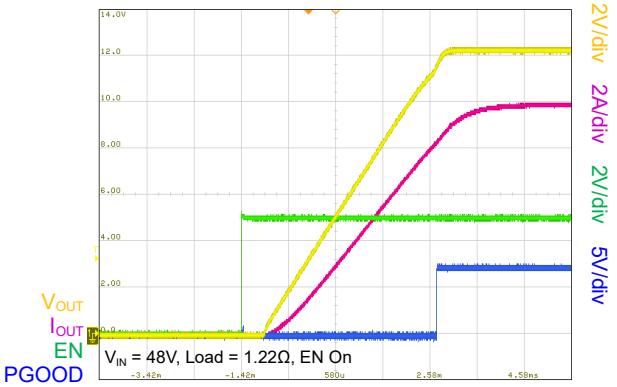
Time (1ms/div)

Shutdown by Input UVLO, 10A Resistive Load



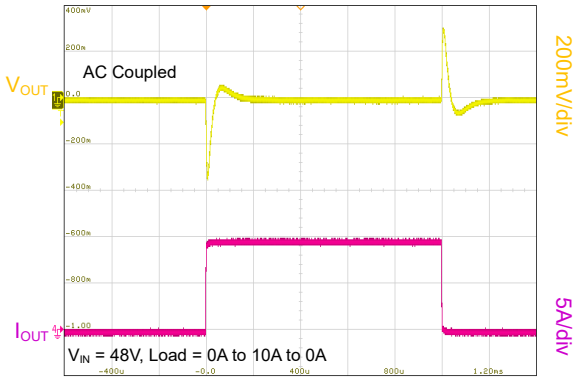
Time (200μs/div)

ENABLE On, 10A Resistive Load



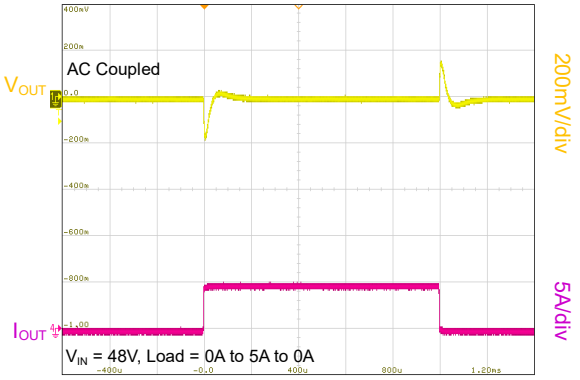
Time (1ms/div)

Load Transient Response



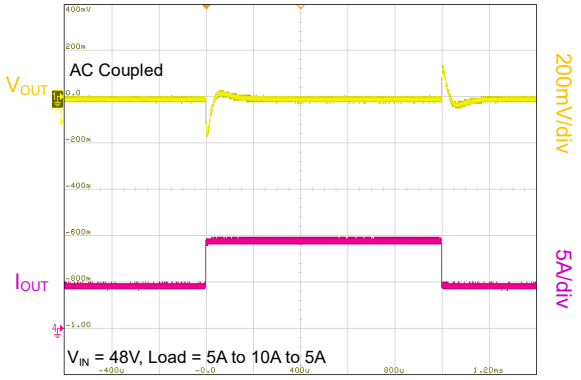
Time (200μs/div)

Load Transient Response



Time (200μs/div)

Load Transient Response

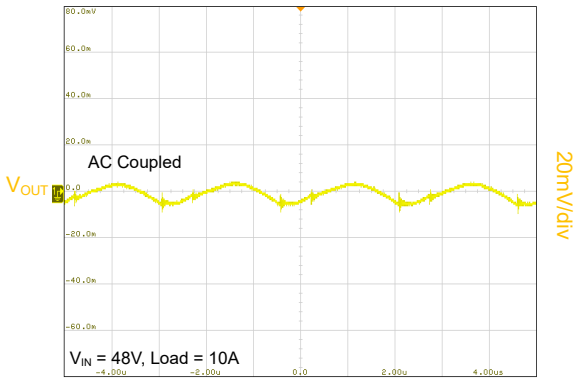


Time (200μs/div)

APPLICATION INFORMATION (continued)

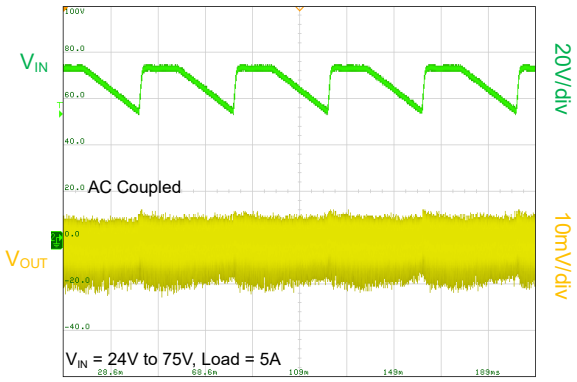
V_{OUT} = 12V, f_{SW} = 400kHz, unless otherwise noted.

Output Voltage Ripple



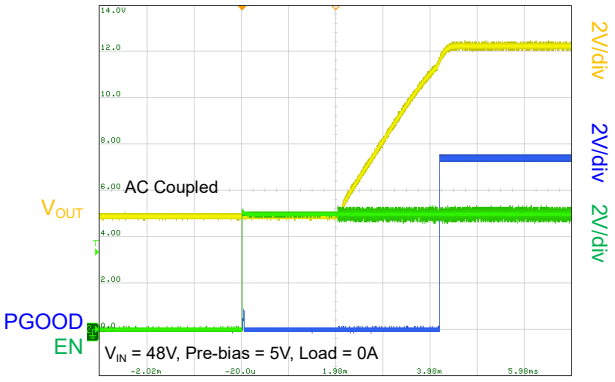
Time (1μs/div)

Repetitive Line Transients, 24V to 75V



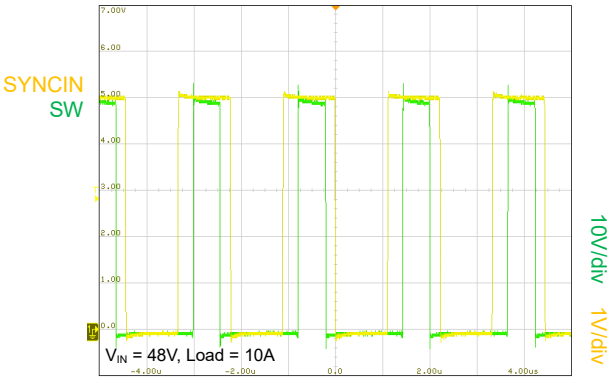
Time (20ms/div)

Pre-Biased Startup



Time (1ms/div)

SW Node and SYNCIN Voltages



Time (1μs/div)

LAYOUT

Layout Guidelines

For the controller, a well-designed PCB layout is critical as it effectively reduces system electromagnetic interference (EMI), minimizes losses, and enhances system stability. The following are specific layout recommendations:

Power Stage Layout

Ensure that all power components (input capacitors, output capacitors, inductors, and power MOSFETs) are placed on the same layer of the PCB. Focus on optimizing two key high-current paths: the first is the main power loop from the input capacitor through the high-side and low-side MOSFETs and back to the capacitor via ground; the second is the synchronous rectification loop from the low-side MOSFET through the inductor and output capacitor and back. Minimizing the physical area of these two loops is essential for reducing parasitic inductance and suppressing switching noise.

Switch Node Layout

The switch node is a source of noise due to rapid voltage transitions. The SW trace should be short and sufficiently wide to carry the current with low loss, but its geometry must be kept compact to minimize the radiating antenna area for EMI control. It is recommended to reserve layout space for an RC snubber near the SW node. This provision enables the snubber to be populated during debugging to suppress potential high-frequency ringing.

Gate Drive Layout

The length of the gate drive loop directly affects switching speed and reliability. The traces from the controller’s driver pins to the MOSFET gates should be as short and direct as possible, with a recommended width of no less than 0.65mm to handle high peak currents. Minimize or avoid vias in high-speed gate loops. If vias are absolutely essential, use vias with a strict minimum diameter of 0.5mm to reduce parasitic inductance.

Drive Power and Input Decoupling Layout

Providing clean power to the driver and the controller itself is fundamental for stable operation. The VCC capacitor should be placed close to the VCC pin, while the bootstrap capacitor should be placed close to the BST and SW pins. At the same time, the input voltage decoupling capacitor must also be placed close to the VIN pin to minimize the loop area formed with GND.

Signal Integrity and Grounding Strategy

It is recommended to use an internal PCB layer to establish a solid, continuous ground plane, which provides shielding for sensitive signals and a quiet reference potential. During layout, it is essential to physically isolate small-signal analog traces and components (e.g., COMP, FB, RT, ILIM, SS/TRK) from high-voltage, high-current switching nodes (e.g., SW, HO, LO, BST). It is advisable to separate the power ground (PGND) from the analog ground (AGND) and connect them at a single point. The feedback network's divider resistors should be placed close to the FB pin, and the ILIM setting resistor should be placed close to the ILIM pin, with its trace routed away from high-voltage networks to ensure accurate sensing and avoid interference.

Thermal Design Considerations

For applications with continuous heavy loads, the PCB itself becomes an important heat dissipation path. In addition to optimizing the layout of power components, consider increasing the copper thickness of power layers and placing a large number of thermal vias beneath the chip's thermal pad and around power devices to effectively reduce thermal resistance and enhance long-term system reliability.

LAYOUT (continued)

Layout Example

Figure 16 to Figure 19 show an example PCB layout.

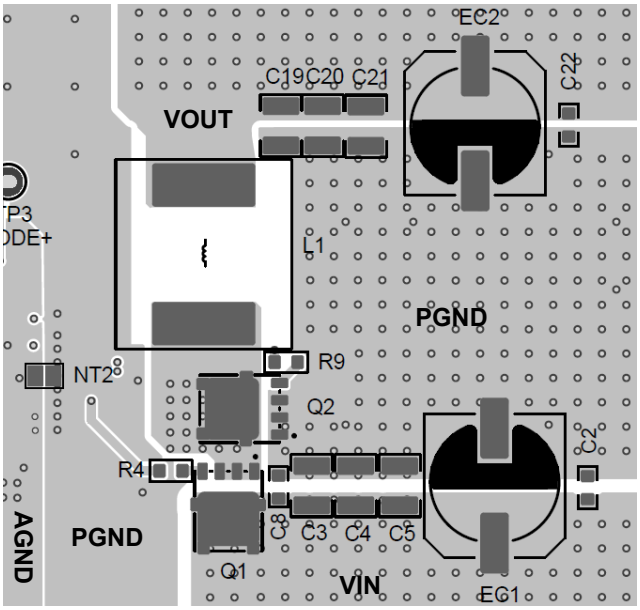


Figure 16. Layout Example (Top View)

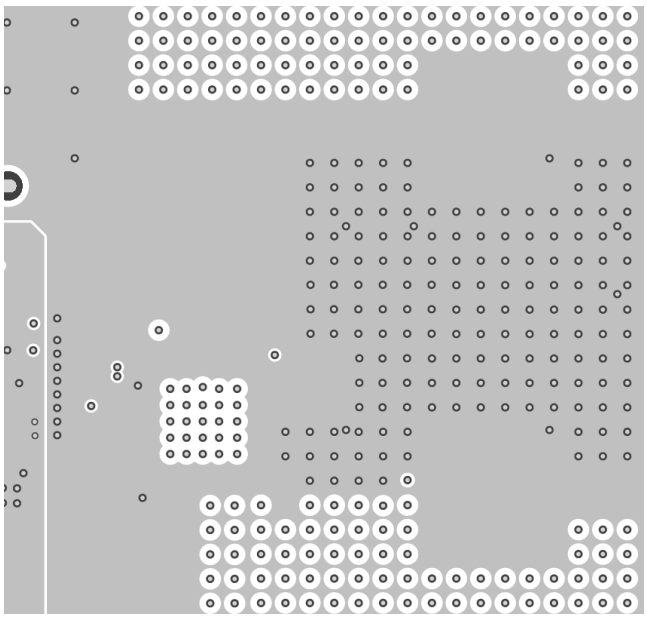


Figure 17. Layout Example (Middle Layer 1 View)

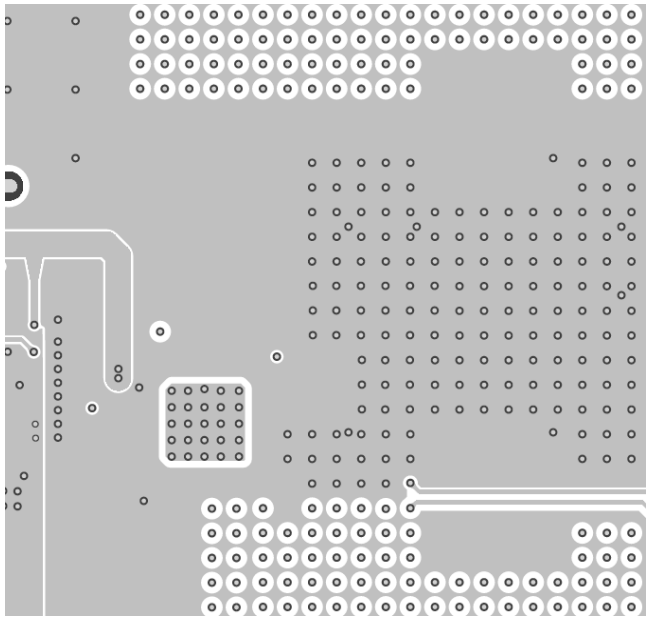


Figure 18. Layout Example (Middle Layer 2 View)

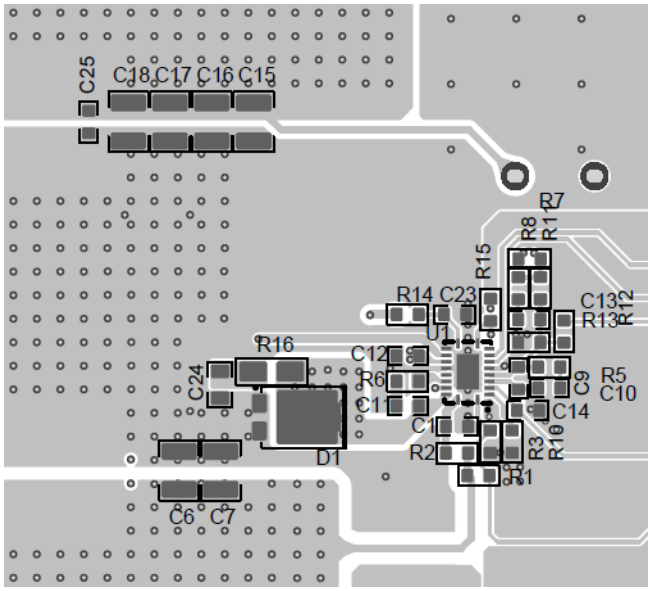


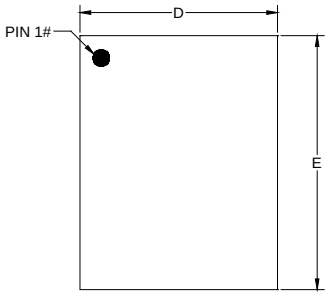
Figure 19. Layout Example (Bottom View)

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

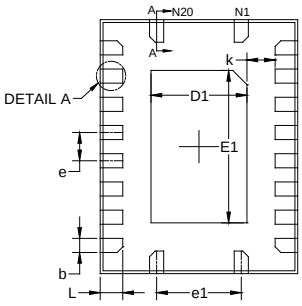
Changes from Original to REV.A (DECEMBER 2025)	Page
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

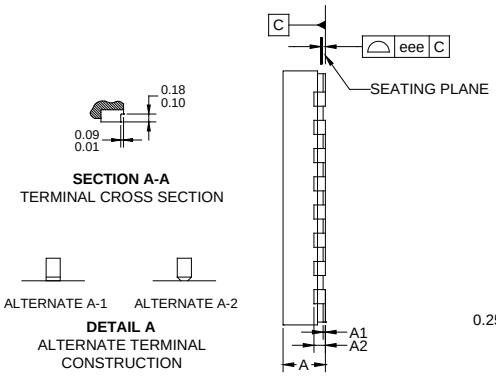
TQFN-3.5×4.5-20BL



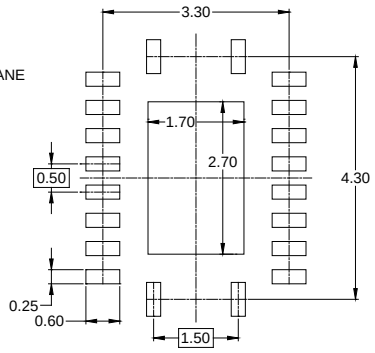
TOP VIEW



BOTTOM VIEW



SIDE VIEW



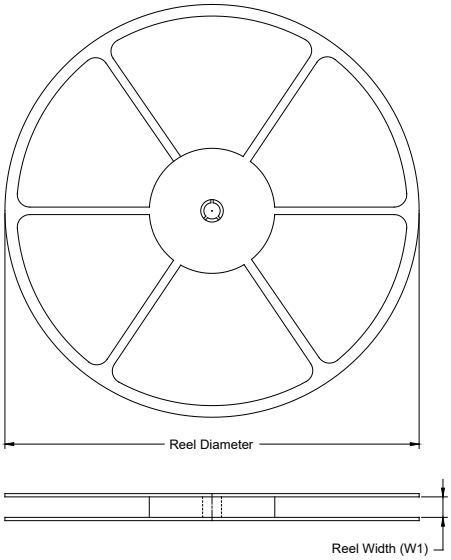
RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	0.700	-	0.800
A1	0.000	-	0.050
A2	0.203 REF		
b	0.200	-	0.300
D	3.400	-	3.600
D1	1.600	-	1.800
E	4.400	-	4.600
E1	2.600	-	2.800
e	0.500 BSC		
e1	1.500 BSC		
L	0.300	-	0.500
k	0.500 REF		
eee	0.080		

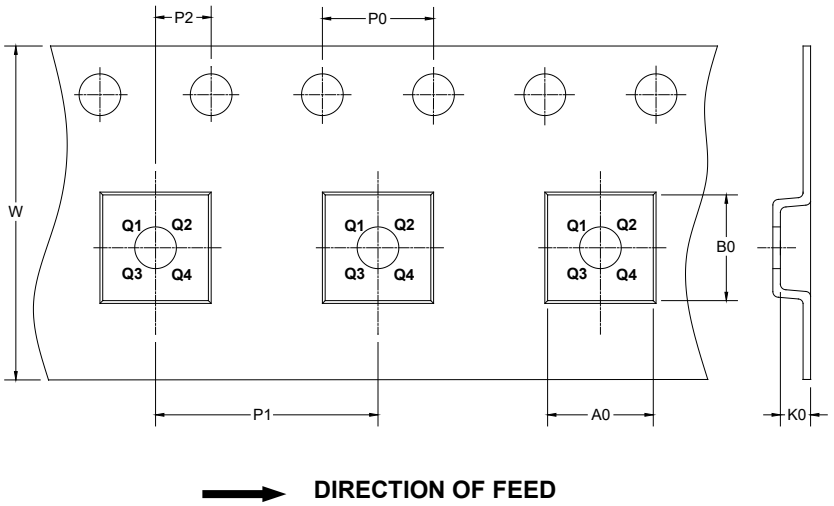
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



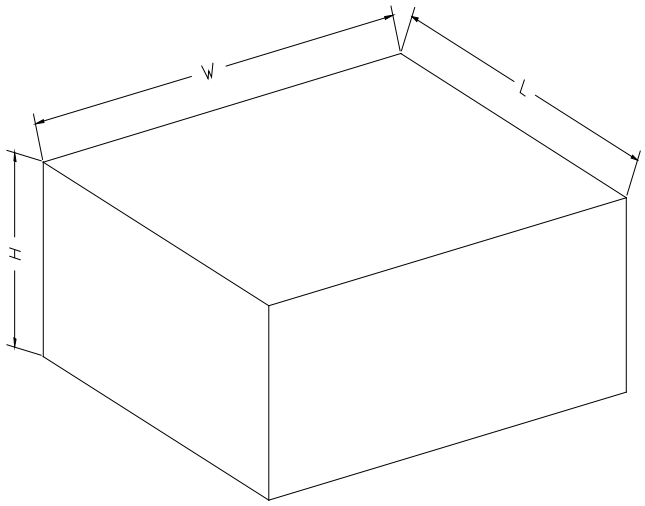
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TQFN-3.5×4.5-20BL	13"	12.4	3.80	4.80	1.10	4.0	8.0	2.0	12.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002