SGMGQ58410
100V, TLGA Package, GaN E-Mode Power Transistor

FEATURES

- **GaN-on-Silicon E-Mode HEMT Technology**
- **Industry Application**
- **Very Low Gate Charge**
- **Ultra-Low On-Resistance**
- **Very Small Footprint**
- **RoHS Compliant and Halogen Free**

APPLICATIONS

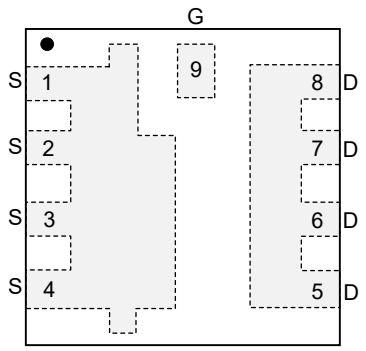
High Frequency DC/DC Converter
High Density DC/DC Power Module
Synchronous Rectification
Motor Driver
Solar System MPPT & Solar Power Optimizer

PRODUCT SUMMARY

R_{DSON} (TYP) V_{GS} = 5V	R_{DSON} (MAX) V_{GS} = 5V	I_D (MAX) T_C = +25℃
5.8mΩ	7mΩ	93A

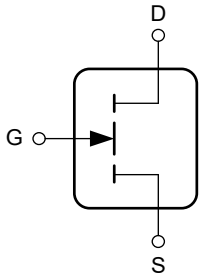
PIN CONFIGURATION

(TOP VIEW)



TLGA-3.3×3.3-9AL

EQUIVALENT CIRCUIT



ABSOLUTE MAXIMUM RATINGS

PARAMETER		SYMBOL	VALUE	UNITS
Drain-to-Source Voltage		V_{DS}	100	V
Drain-to-Source Voltage (1) (V_{GS} = 0V, 1h total time, T_A = T_{JMAX})		V_{DS_TR}	120	V
Gate-to-Source Voltage		V_{GS}	6	V
			-4	
Gate-to-Source Voltage (1) (V_{DS} = 0V, 168h total time, T_A = T_{JMAX})		V_{GS_TR}	6.5	V
Drain Current	T_C = +25℃	I_D	93	A
	T_A = +25℃		13	
Drain Current (Pulse) (2)		I_{DM}	175	A
Total Dissipation	T_C = +25℃	P_D	112	W
	T_A = +25℃		2.2	
Junction Temperature		T_J	-40 to +150	℃
Storage Temperature Range		T_{STG}	-55 to +150	℃
Lead Temperature (Soldering, 10s)			+260	℃

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

NOTES:

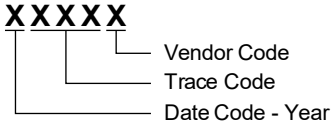
1. Provided as measure of robustness under abnormal operating conditions and not recommended for normal operation.
2. V_{GS} = 5V, T_J = +25℃, t_{PULSE} = 100μs.

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGMGQ58410	TLGA-3.3×3.3-9AL	-40℃ to +150℃	SGMGQ58410TTLBH9G/TR	58410 XXXXX	Tape and Reel, 2500

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

THERMAL RESISTANCE

PARAMETER	SYMBOL	TYP	UNITS
Junction-to-Ambient Thermal Resistance (1)	$R_{\theta JA}$	52.7	℃/W
Junction-to-Board Thermal Resistance	$R_{\theta JB}$	9.7	℃/W
Junction-to-Case Thermal Resistance	$R_{\theta JC}$	1	℃/W

NOTE: 1. $R_{\theta JA}$ is determined with the device on FR4 PCB (2s2p with thermal vias) defined in accordance with JEDEC standards. PCB is mounted in horizontal position without air stream cooling.

ELECTRICAL CHARACTERISTICS

(T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Static Characteristics							
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0V, V_{DS} = 100V	T_J = +25℃		0.5	43	μA
			T_J = +125℃		100		
Gate-to-Source Leakage Current	I_{GSS}	V_{GS} = 6V			0.2	43	μA
		V_{GS} = 6V, T_J = +125℃			20		
		V_{GS} = -4V			0.1	43	
Gate-to-Source Threshold Voltage	V_{GS_TH}	V_{GS} = V_{DS}, I_D = 3.2mA		0.8	1.1	2.1	V
Drain-to-Source On-State Resistance	R_{DSON}	V_{GS} = 5V, I_D = 2.5A			5.8	7	mΩ
Gate Resistance	R_G	f = 5MHz, open drain			1.1		Ω
Source-to-Drain Forward Voltage	V_{SD}	V_{GS} = 0V, I_S = 16A			2.3		V
Dynamic Characteristics							
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 50V			407		pF
Output Capacitance	C_{OSS}				175		
Reverse Transfer Capacitance	C_{RSS}				2.6		
Effective Output Capacitance, Energy Related	C_{O_ER}	V_{GS} = 0V, V_{DS} = 0V to 50V			242		
Effective Output Capacitance, Time Related	C_{O_TR}				346		
Total Gate Charge	Q_G	V_{GS} = 5V, V_{DS} = 0V to 50V, I_D = 16A			3.4		nC
Gate-to-Source Charge	Q_{GS}				0.8		
Gate-to-Drain Charge	Q_{GD}				0.5		
Gate Plateau Voltage	V_{PLAT}	V_{GS} = 0V to 5V, V_{DS} = 50V, I_D = 16A			2		V
Gate Charge at Threshold	Q_{G_TH}	V_{GS} = 5V, V_{DS} = 0V to 50V, I_D = 16A			0.5		nC
Output Charge	Q_{OSS}	V_{GS} = 0V, V_{DS} = 0V to 50V			17.3		
Reverse Recovery Charge	Q_{RR}	V_{DS} = 50V, I_S = 16A			0		

TYPICAL PERFORMANCE CHARACTERISTICS

Fig. 1 Typ. Output Characteristics (T_J = 25 °C)

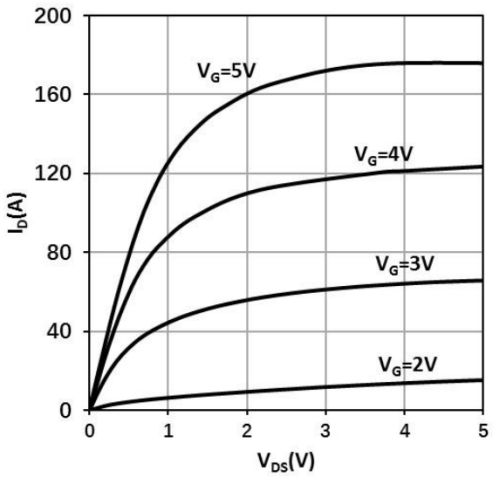


Fig. 2 Typ. Output Characteristics (T_J = 125 °C)

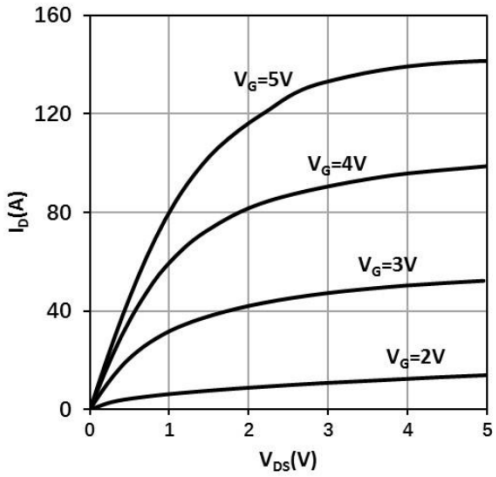


Fig. 3 Typ. Drain On-state Resistance (T_J = 25 °C)

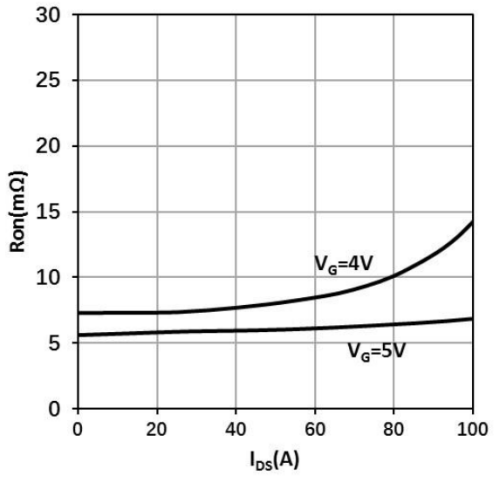
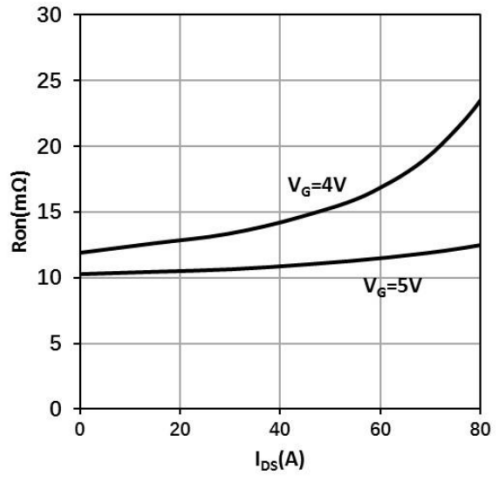


Fig. 4 Typ. Drain On-state Resistance (T_J = 125 °C)



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Fig. 5 Normalized On-State Resistance vs. Temp.

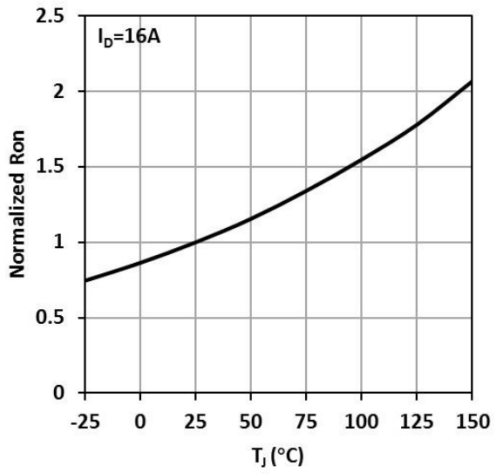


Fig. 6 Typ. Transfer Characteristics

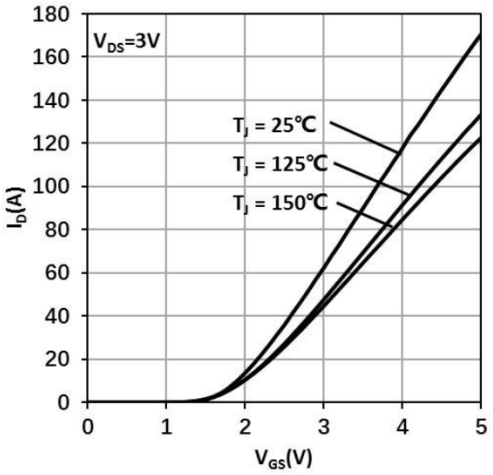


Fig. 7 Typ. Reverse Drain-Source Characteristics (V_{GS} ≤ 0, T_J = 25 °C)

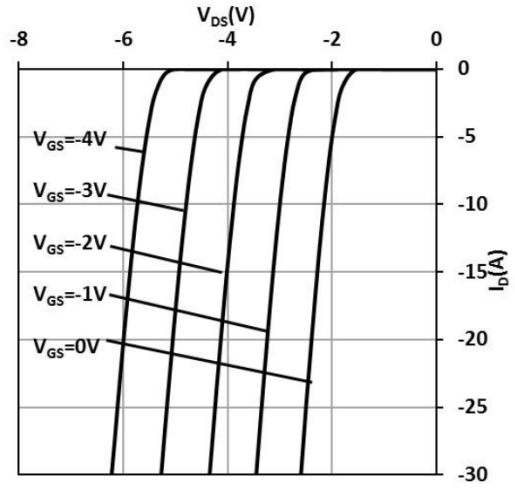
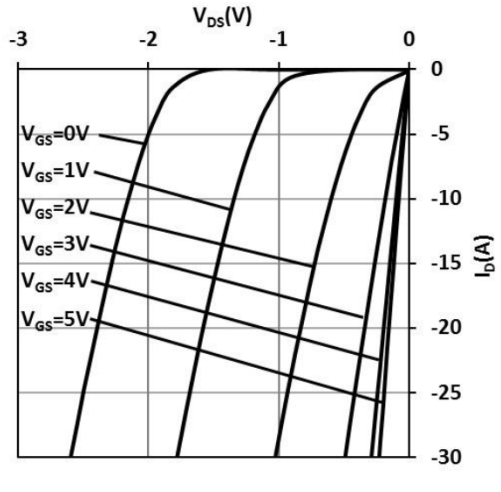


Fig. 8 Typ. Reverse Drain-Source Characteristics (V_{GS} ≥ 0, T_J = 25 °C)



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Fig. 9 Typ. Reverse Drain-Source Characteristics ($V_{GS} \leq 0$, T_J = 125 °C)

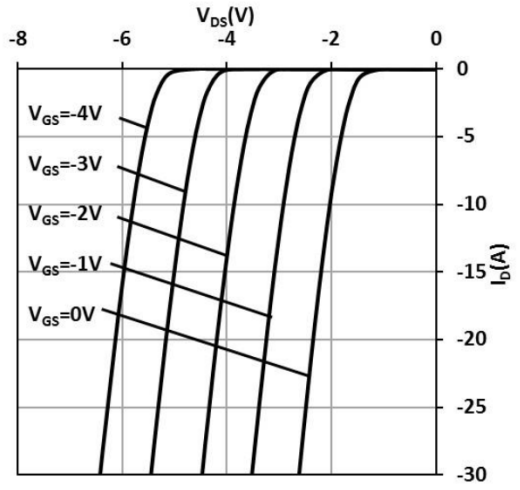


Fig. 10 Typ. Reverse Drain-Source Characteristics ($V_{GS} \geq 0$, T_J = 125 °C)

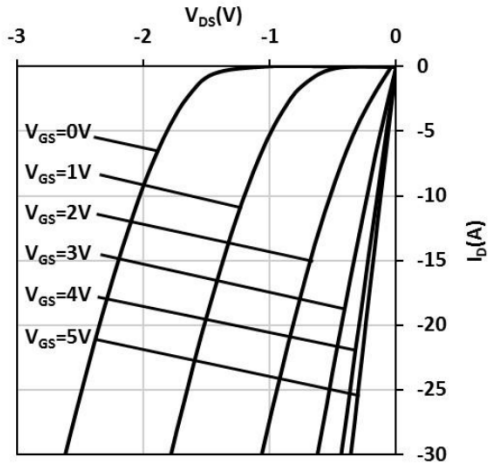


Fig. 11 Typ. Capacitances Characteristics

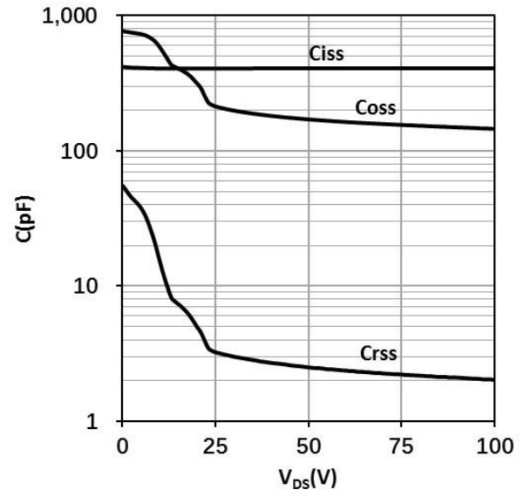
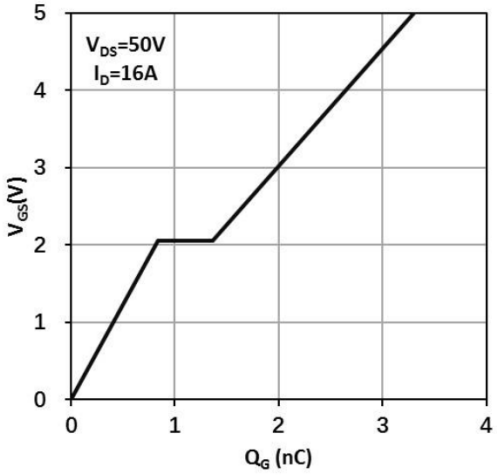


Fig. 12 Typ. Gate Charge



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Fig. 13 Normalized Threshold Voltage vs. Temp.

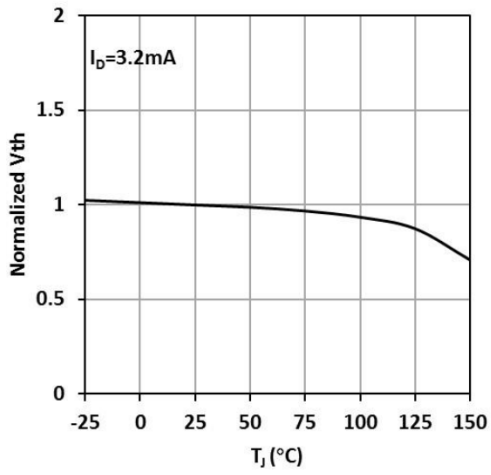


Fig. 14 Typ. Output Charge

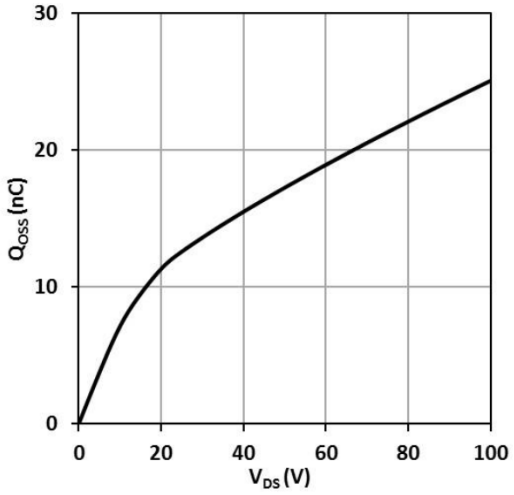


Fig. 15 Typ. Output Capacitance Stored Energy

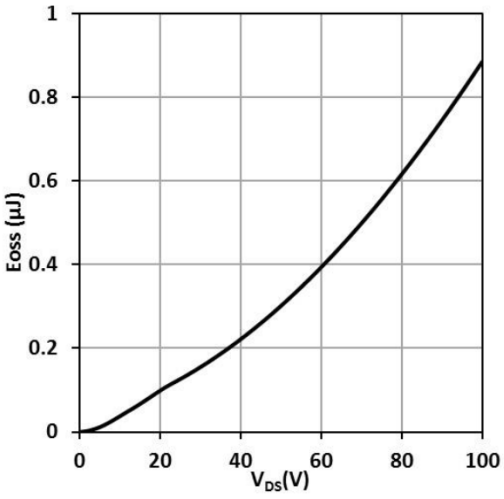
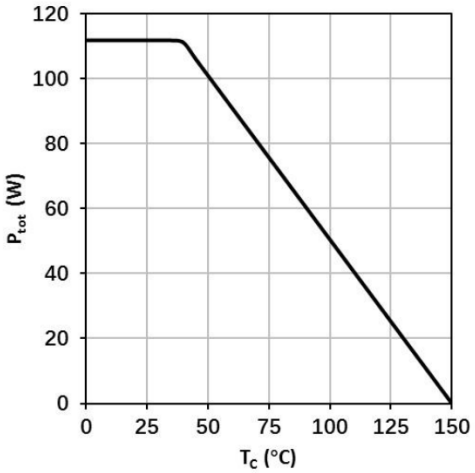


Fig. 16 Power Dissipation P_{tot} = f(T_C), $R_{\theta JC}$ = 1.0 ˚C/W



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Fig. 17 Power Dissipation P_{tot} = f(T_A), $R_{\theta JA}$ = 52.7 ˚C/W

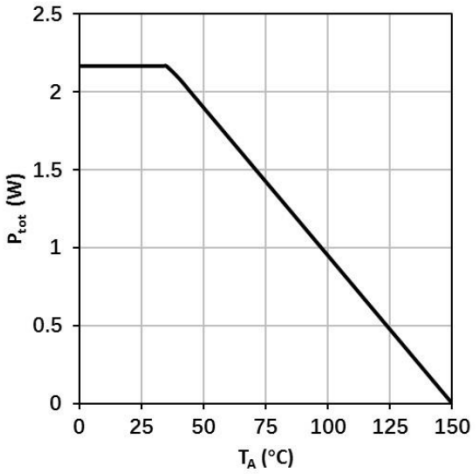


Fig. 18 Typ. Gate-to-Source Leakage Characteristics
I_G = f(V_{GS}); Drain Open

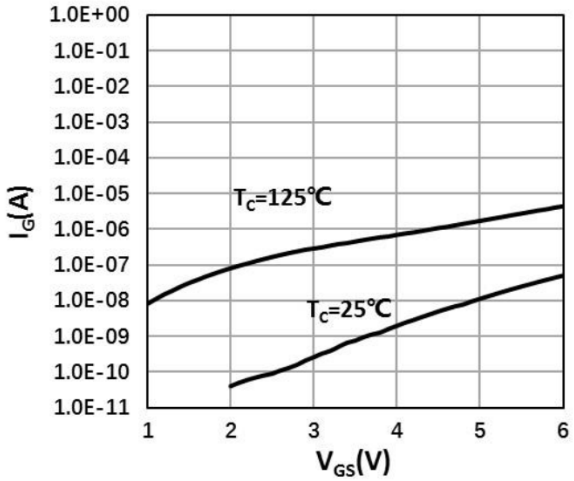


Fig. 19 Typ. Drain-source Leakage Characteristics
I_{DSS} = f(V_{DS}); V_{GS} = 0 V

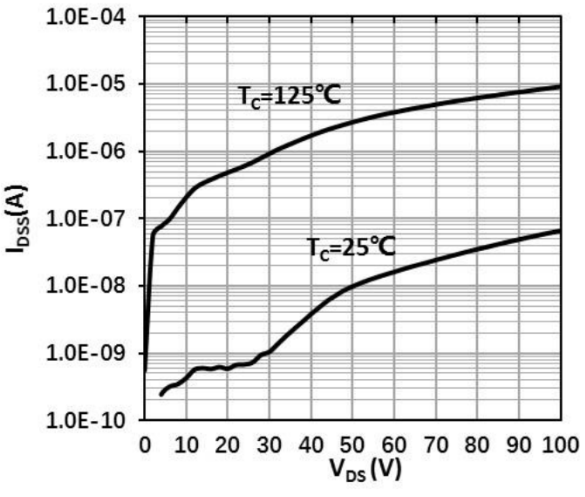
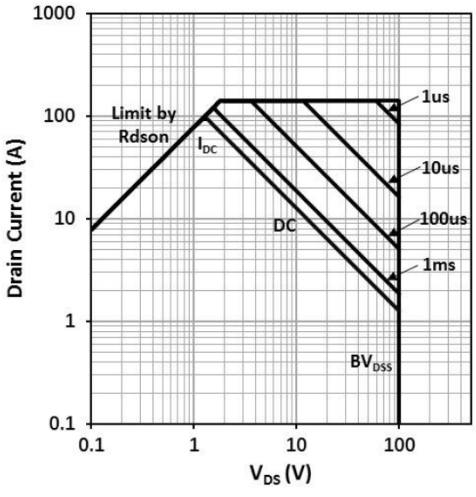


Fig. 20 Safe Operating Area
I_D = f(V_{DS}); Tc = 25 °C; single pulse; parameter: t_p



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Fig. 21 Safe Operating Area
$I_D = f(V_{DS})$; Tc = 125 °C; single pulse; parameter: t_p

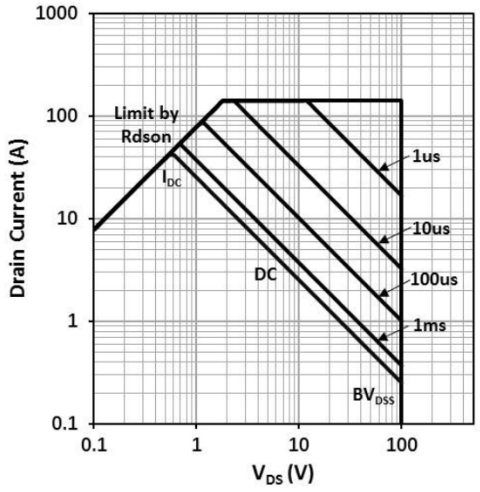
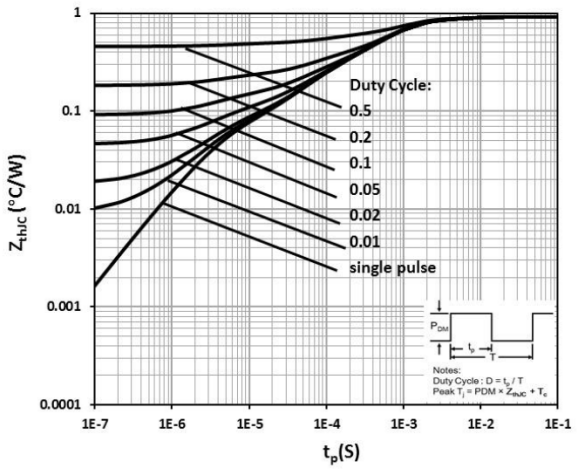


Fig. 22 Max. Transient Thermal Impedance
$Z_{thJC} = f(t_p)$; parameter: $D=t_p/T$



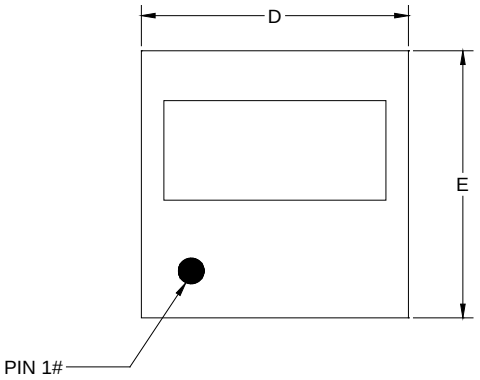
REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

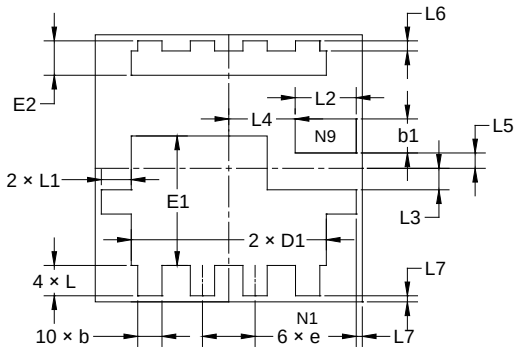
Changes from Original to REV.A (JUNE 2026)	Page
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

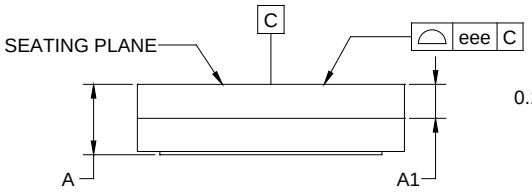
TLGA-3.3×3.3-9AL



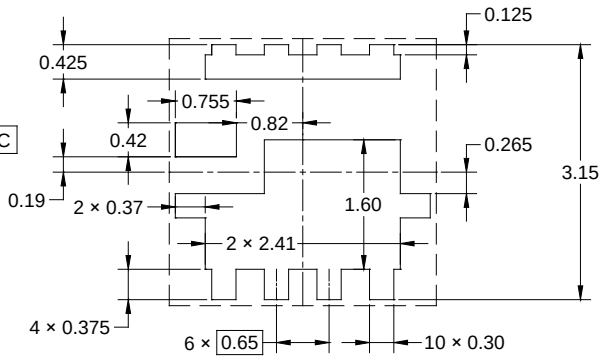
TOP VIEW



BOTTOM VIEW



SIDE VIEW



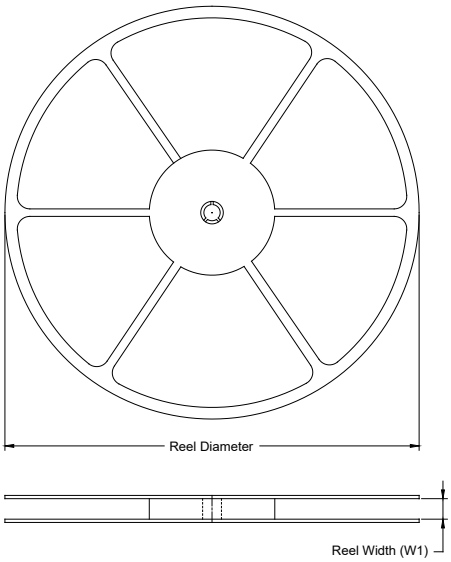
RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	0.770	-	0.970
A1		0.420 REF	
b	0.250	-	0.350
b1	0.370	-	0.470
D	3.200	-	3.400
D1	2.310	-	2.510
E	3.200	-	3.400
E1	1.500	-	1.700
E2	0.325	-	0.525
e		0.650 BSC	
L	0.325	-	0.425
L1	0.320	-	0.420
L2	0.705	-	0.805
L3		0.265 REF	
L4		0.820 REF	
L5		0.190 REF	
L6		0.125 REF	
L7		0.075 REF	
eee		0.100	

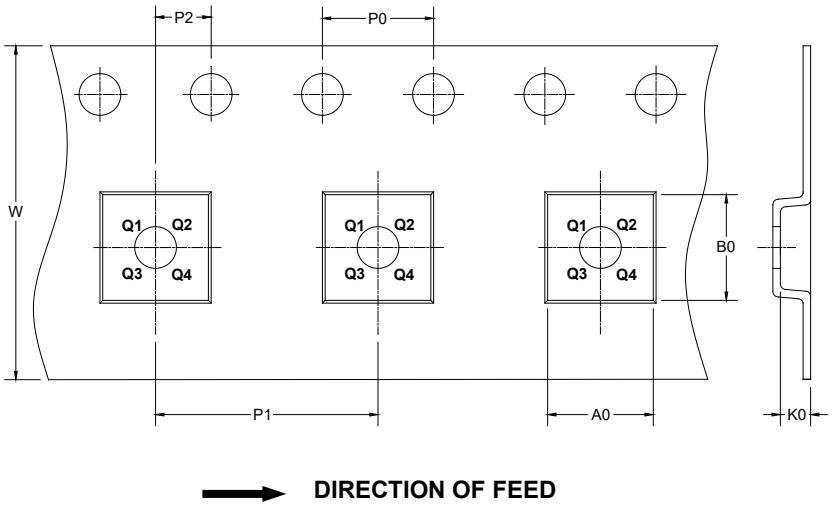
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



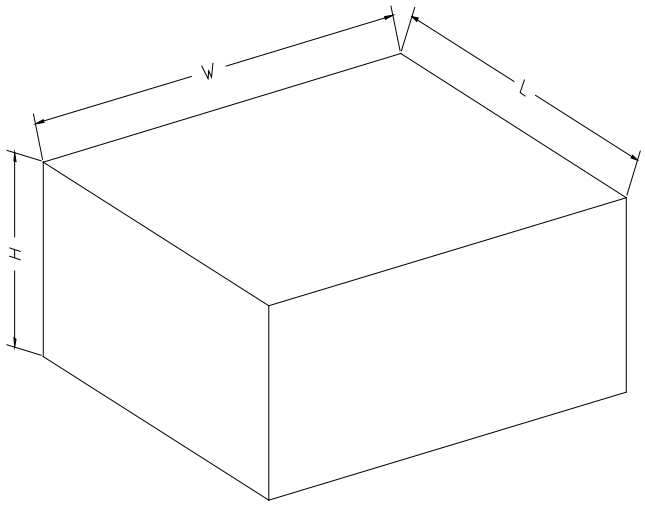
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TLGA-3.3×3.3-9AL	13"	12.4	3.55	3.55	1.20	4.0	8.0	2.0	12.0	Q2

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002