

### GENERAL DESCRIPTION

The SGM70411 is a low dropout linear regulator with 5V fixed output and low quiescent current. This device adopts user-programmable reset delay, watchdog timer, automatic wake-up function and enable function. It also has over-temperature protection and over-current protection. Additionally, it can suppress transient voltages with maximum magnitude within 45V.

The SGM70411 is available in a Green SOIC-8 (Exposed Pad) package. It operates over the ambient temperature range of -40°C to +125°C.

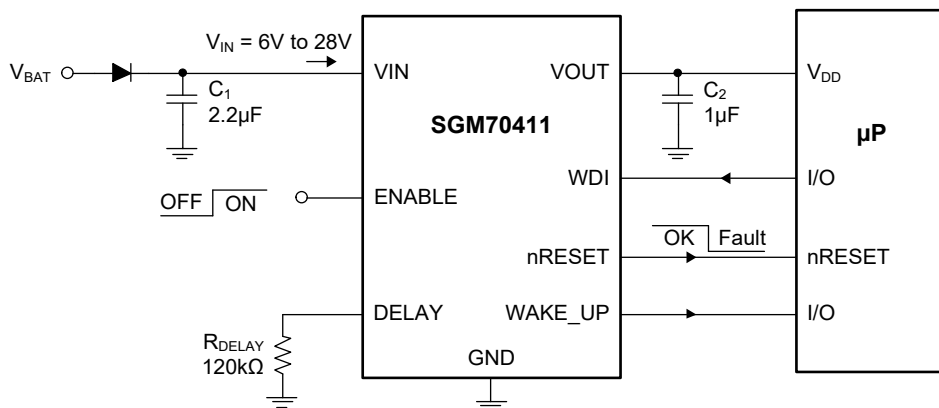
### FEATURES

- Output Voltage of 5.0V
- High Accuracy Output Voltage Tolerance
- Up to 250mA Output Current
- Suitable for Micropower Control Applications: Enable, Watchdog, nRESET and Wake-Up
- Low Dropout Voltage
- Low Quiescent Current: 85μA (TYP)
- Low Sleep Mode Current: Typically Less than 1μA
- Thermal Shutdown and Short-Circuit Protection
- Available in a Green SOIC-8 (Exposed Pad) Package

### APPLICATIONS

Tire Pressure Monitor  
Battery-Powered Consumer Electronics  
Applications Requiring Site and Change Control

### TYPICAL APPLICATION



NOTE:  $C_1$  is recommended if the regulator is located away from the power filter. If extremely fast input voltage transients are required to be suppressed, an input filter with several capacitors in parallel can be used.

Figure 1. Typical Application Circuit

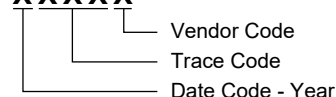
## PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM70411	SOIC-8 (Exposed Pad)	-40°C to +125°C	SGM70411XPS8G/TR	SGM 70411XPS8 XXXXX	Tape and Reel, 4000

## MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.

XXXXX



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

## ABSOLUTE MAXIMUM RATINGS

Input Voltage, $V_{IN}$	-0.3V to 45V
ENABLE Voltage, $V_{EN}$	-0.3V to 45V
Output Voltage, $V_{OUT}$	-0.3V to 7V
nRESET Voltage, $V_{nRESET}$	0V to $V_{OUT}$
nRESET Current <sup>(1)</sup> , $I_{nRESET}$	Internally Limited
Reset, WDI, Wake-Up, Delay Inputs/Outputs	-0.3V to 7V
Package Thermal Resistance	
SOIC-8 (Exposed Pad), $\theta_{JA}$	44.8°C/W
SOIC-8 (Exposed Pad), $\theta_{JB}$	19.7°C/W
SOIC-8 (Exposed Pad), $\theta_{JC (TOP)}$	58.7°C/W
SOIC-8 (Exposed Pad), $\theta_{JC (BOT)}$	8.5°C/W
Junction Temperature	+150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 10s)	+260°C
ESD Susceptibility <sup>(2) (3)</sup>	
HBM	±4000V
CDM	±1000V

## NOTES:

1. nRESET may be incidentally shorted either to VOUT or to GND without damage.

1. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.

2. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

## RECOMMENDED OPERATING CONDITIONS

Supply Voltage, $V_{IN}$	6V to 28V
Operating Ambient Temperature	-40°C to +125°C
Operating Junction Temperature Range	-40°C to +150°C

## OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

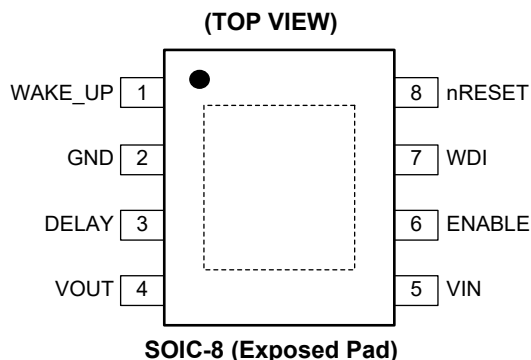
## ESD SENSITIVITY CAUTION

This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

## DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

## PIN CONFIGURATION



## PIN DESCRIPTION

PIN	NAME	FUNCTION
1	WAKE_UP	Frequently wake up the microprocessor from the sleeping mode.
2	GND	Ground.
3	DELAY	Precise Voltage Reference Pin. It is used to provide reference current for the timing circuit with $R_{DELAY}$ resistor.
4	VOUT	Regulated Output Voltage.
5	VIN	Power Supply Voltage.
6	ENABLE	Positive Logic Enable Control of the IC.
7	WDI	Watchdog Input Pin. Falling edge effective.
8	nRESET	Reset Output Pin. If $V_{OUT}$ drops by more than 7% from nominal, or the WDI pin fails to accept an effective falling edge within a wake-up period, the nRESET will become low.
Exposed Pad	—	Exposed Pad.

## ELECTRICAL CHARACTERISTICS

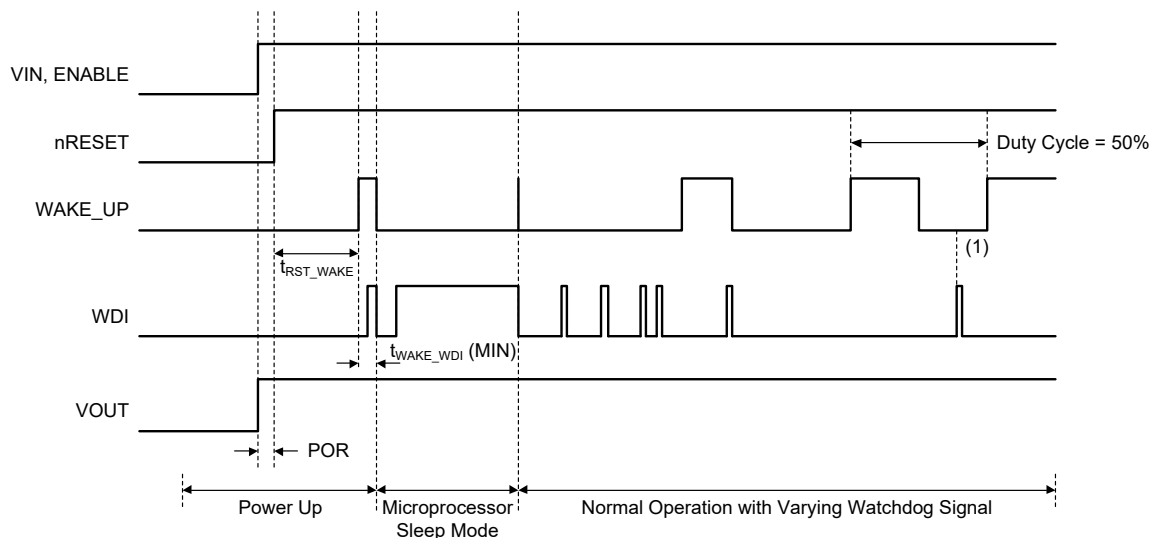
( $V_{IN} = 6.0V$  to  $28V$ ,  $I_{OUT} = 100\mu A$  to  $150mA$ ,  $C_2 = 1.0\mu F$ ,  $R_{DELAY} = 120k\Omega$ ,  $T_A = -40^\circ C$  to  $+125^\circ C$ , typical values are measured at  $T_A = +25^\circ C$ , unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>Output</b>						
Output Voltage	$V_{OUT}$		4.93	5	5.07	V
			-1.4		1.4	%
Dropout Voltage <sup>(1)</sup> ( $V_{IN} - V_{OUT}$ )	$V_{DO}$	$I_{OUT} = 150mA$		260	450	mV
Load Regulation	$REG_{LOAD}$	$V_{IN} = 13.5V$ , $I_{OUT} = 100\mu A$ to $150mA$	-10		10	mV
Line Regulation	$REG_{LINE}$	$I_{OUT} = 5.0mA$ , $V_{IN} = 6.0V$ to $28V$	-10		10	mV
Current Limit	$I_{LIM}$		270	480		mA
Thermal Shutdown <sup>(2)</sup>	$T_{J\_MAX}$		160	173	186	$^\circ C$
Quiescent Current	$I_Q$	$V_{IN} = 13.5V$ , $I_{OUT} = 100\mu A$ , $ENABLE = 2.0V$		85	130	$\mu A$
Shutdown Current	$I_{SD}$	$ENABLE = 0V$ , $T_A = +125^\circ C$			1.5	$\mu A$
<b>nRESET</b>						
Threshold Voltage			4.58	4.65	4.72	V
Output Low		$R_{nRESET} = 10k\Omega$ to $V_{OUT}$ , $V_{OUT} = 1.0V$		0.015	0.2	V
Output High		$R_{nRESET} = 10k\Omega$ to GND	$V_{OUT} - 0.2$	$V_{OUT} - 0.01$		V
Power-On Reset Delay Time	$t_D$	$V_{IN} = 13.5V$ , $R_{DELAY} = 60k\Omega$ , $I_{OUT} = 5.0mA$		3.22		ms
		$V_{IN} = 13.5V$ , $R_{DELAY} = 120k\Omega$ , $I_{OUT} = 5.0mA$	5.25	6.25	7.25	
		$V_{IN} = 13.5V$ , $R_{DELAY} = 500k\Omega$ , $I_{OUT} = 5.0mA$		25.4		
Reset Reaction Time	$t_{RR}$			6		$\mu s$
<b>Watchdog Input (WDI)</b>						
Threshold	$WDI_{HIGH}$		30	50	70	$V_{OUT}\%$
Hysteresis	$WDI_{HYS}$		25	100		mV
Input Current		$WDI = 6.0V$		1.2	2	$\mu A$
Wake-Up Rising Edge to WDI Falling Edge Delay	$t_{WAKE\_WDI}$		5			$\mu s$
<b>ENABLE</b>						
Logic Low Input Threshold	$V_{TH\_ENL}$				0.8	V
Logic High Input Threshold	$V_{TH\_ENH}$		2			V
Input Current		$ENABLE = 2.0V$		3	10	$\mu A$
<b>WAKE_UP Output (<math>V_{IN} = 13.5V</math>, <math>I_{OUT} = 5.0mA</math>)</b>						
Wake-Up Period		$R_{DELAY} = 60k\Omega$		26		ms
		$R_{DELAY} = 120k\Omega$		50		
		$R_{DELAY} = 500k\Omega$		203		
Wake-Up Duty Cycle Nominal				50		%
nRESET High to Wake-Up Rising Delay Time (50% nRESET rising edge to 50% wake-up edge)	$t_{RST\_WAKE}$	$R_{DELAY} = 60k\Omega$		12.9		ms
		$R_{DELAY} = 120k\Omega$	21	25	29	
		$R_{DELAY} = 500k\Omega$		102		
Wake-Up Response to Watchdog Input (50% WDI falling edge to 50% wake-up falling edge)				0.2	5	$\mu s$
Output Low		$R_{WAKE\_UP} = 10k\Omega$ to $V_{OUT}$ , $V_{OUT} = 1V$		0.01	0.2	V
Output High		$R_{WAKE\_UP} = 10k\Omega$ to GND	$V_{OUT} - 0.2$	$V_{OUT} - 0.015$		V
<b>DELAY</b>						
Output Voltage		$R_{DELAY} = 60k\Omega$ , $120k\Omega$ , $500k\Omega$		0.48		V

## NOTES:

- These values are taken when the output voltage decreases by 2% from its nominal value.
- Guaranteed by design.
- Input or enable slew rates in excess of  $3V/\mu s$  may cause nRESET to change state.

## TIMING DIAGRAM



NOTE: 1. If the WDI pulse occurs with the WAKE\_UP signal low, the wake-up duty cycle will be 50%.

Figure 2. Power-Up, Sleep Mode and Normal Operation

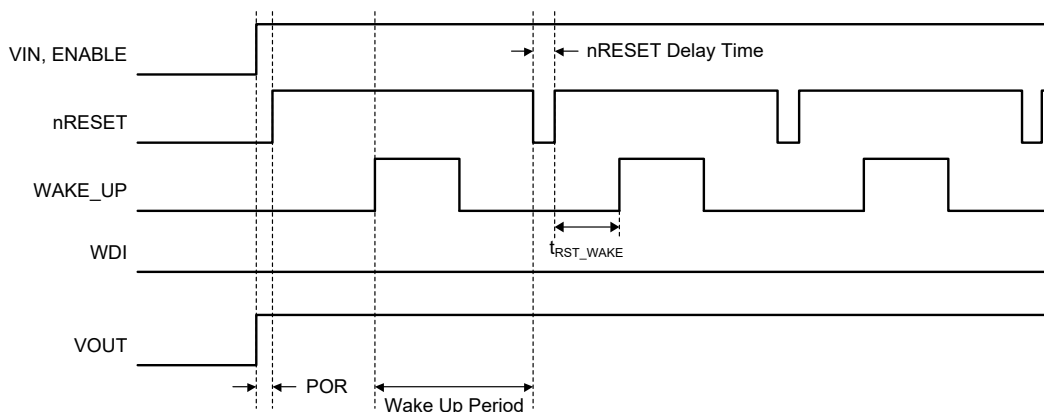


Figure 3. Error State: WDI Stays Low & an nRESET Signal is Triggered

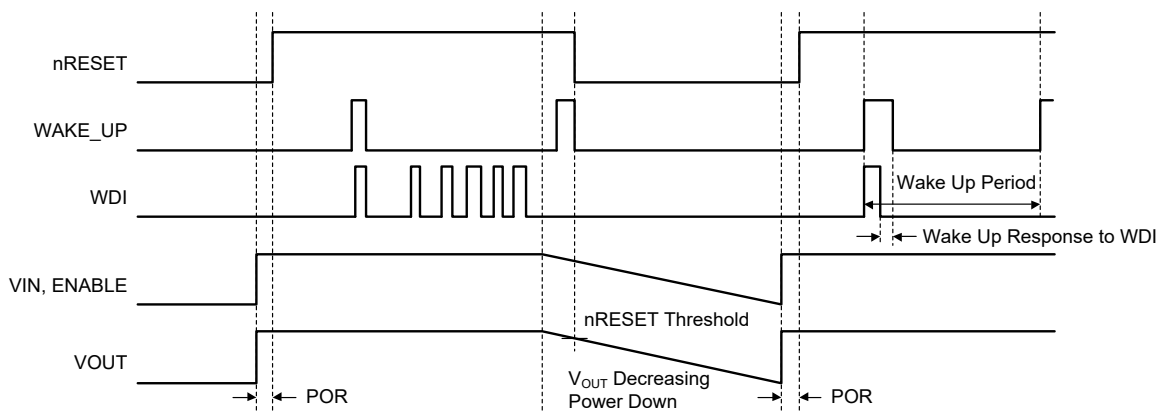
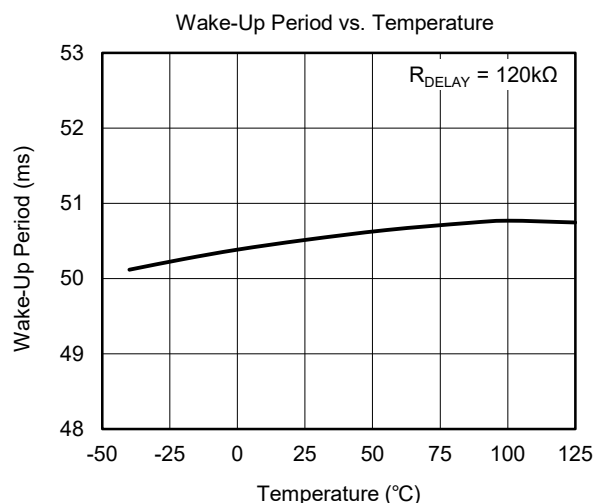
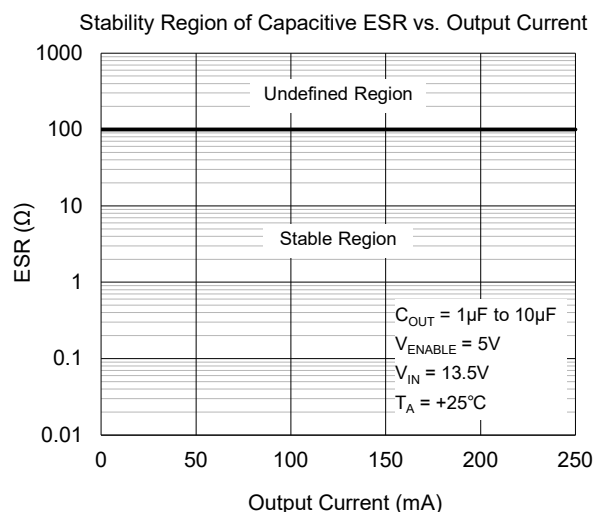
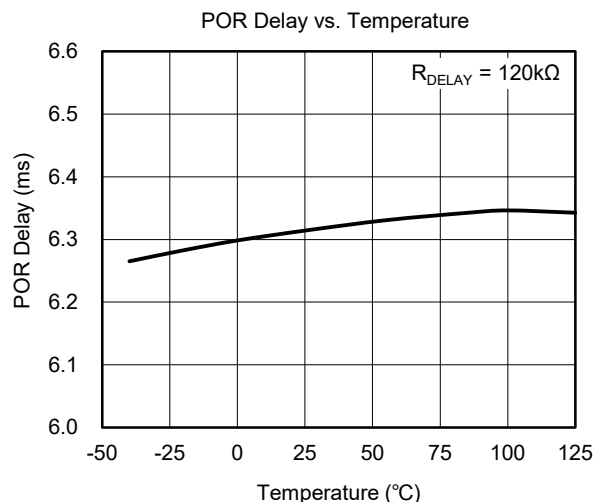
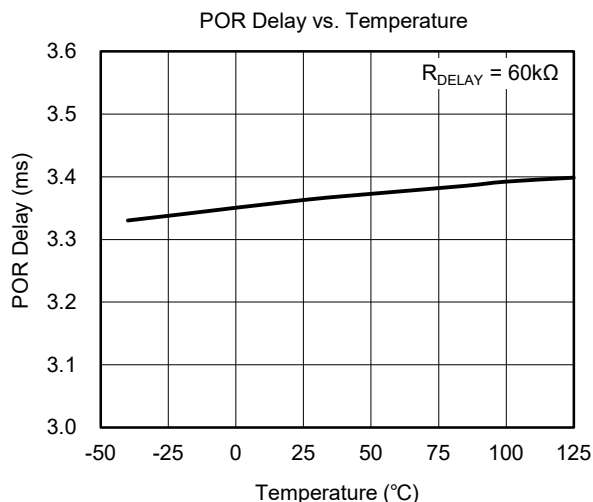
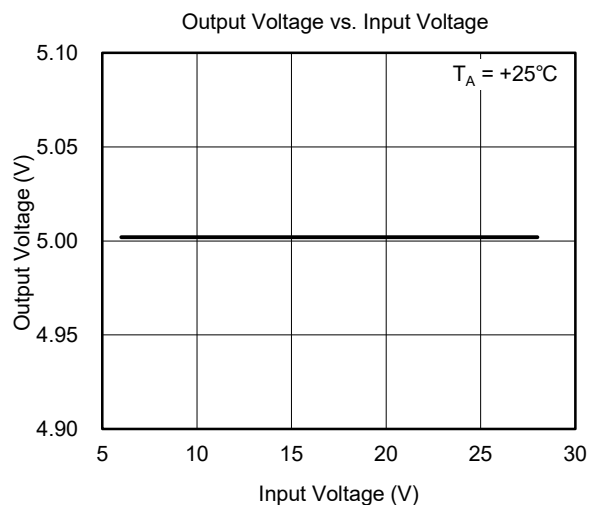
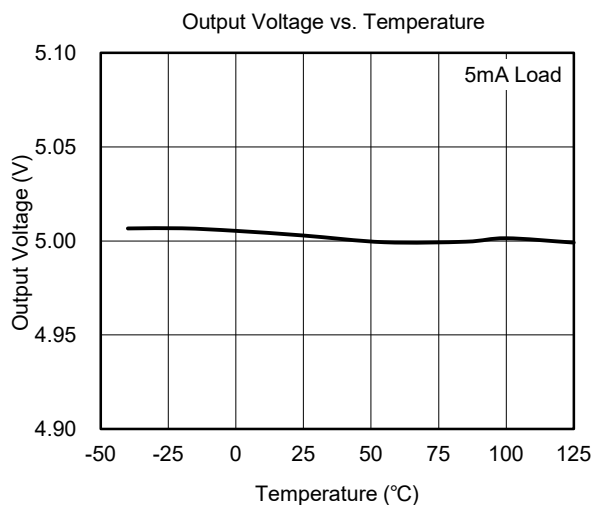
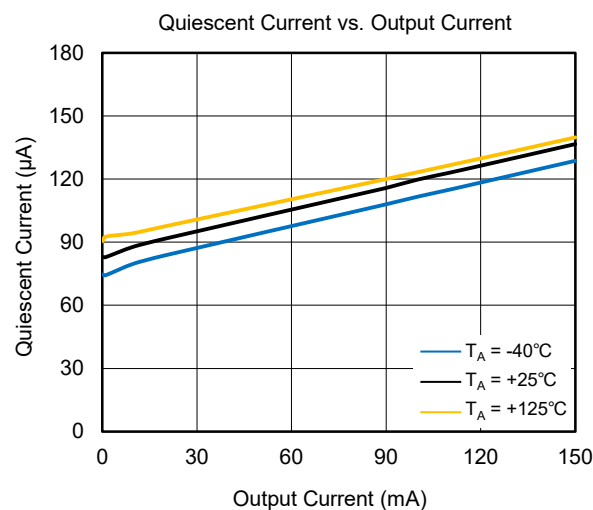
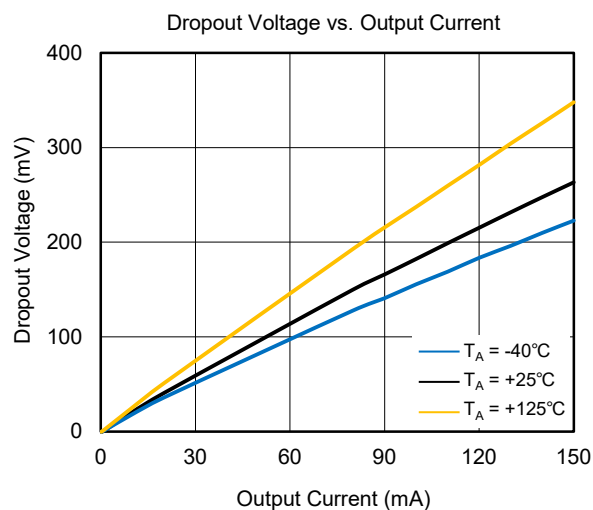
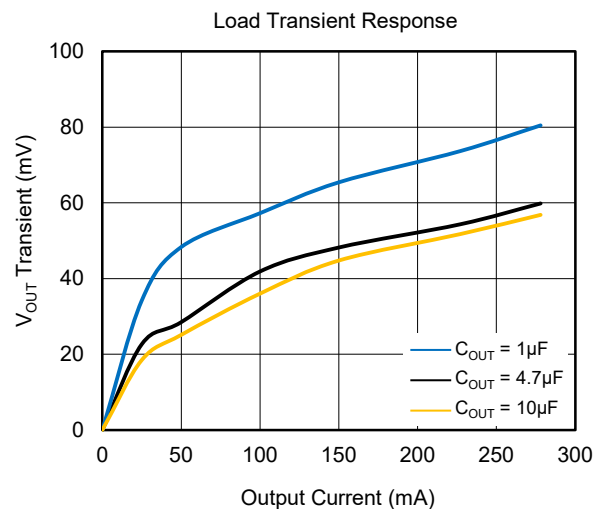
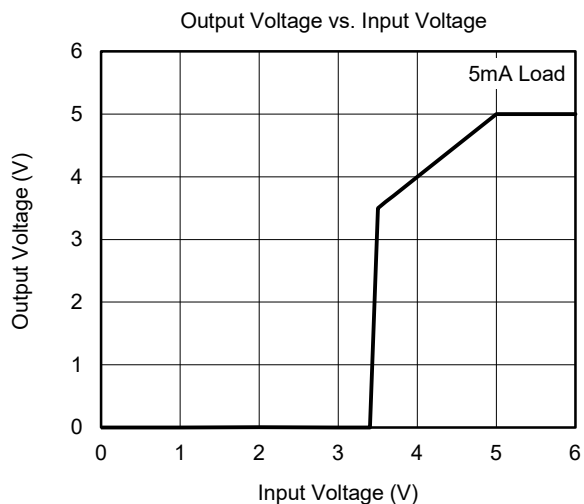
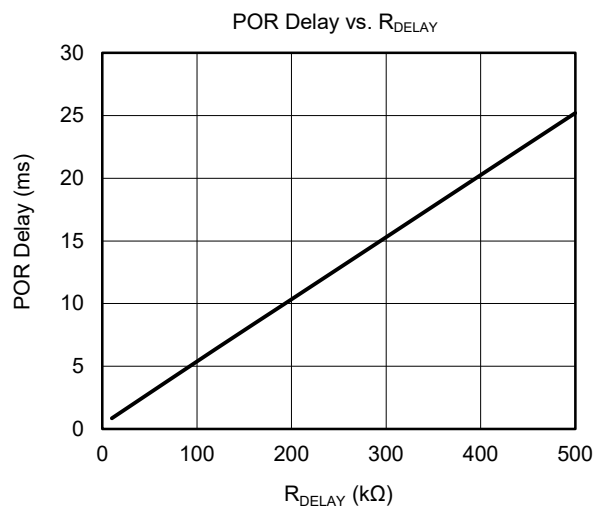
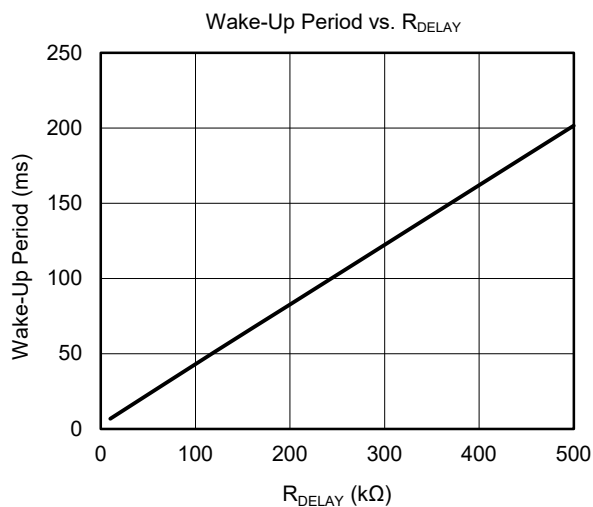


Figure 4. Power-Down, Restart Sequence, and Wake-Up Response to WDI

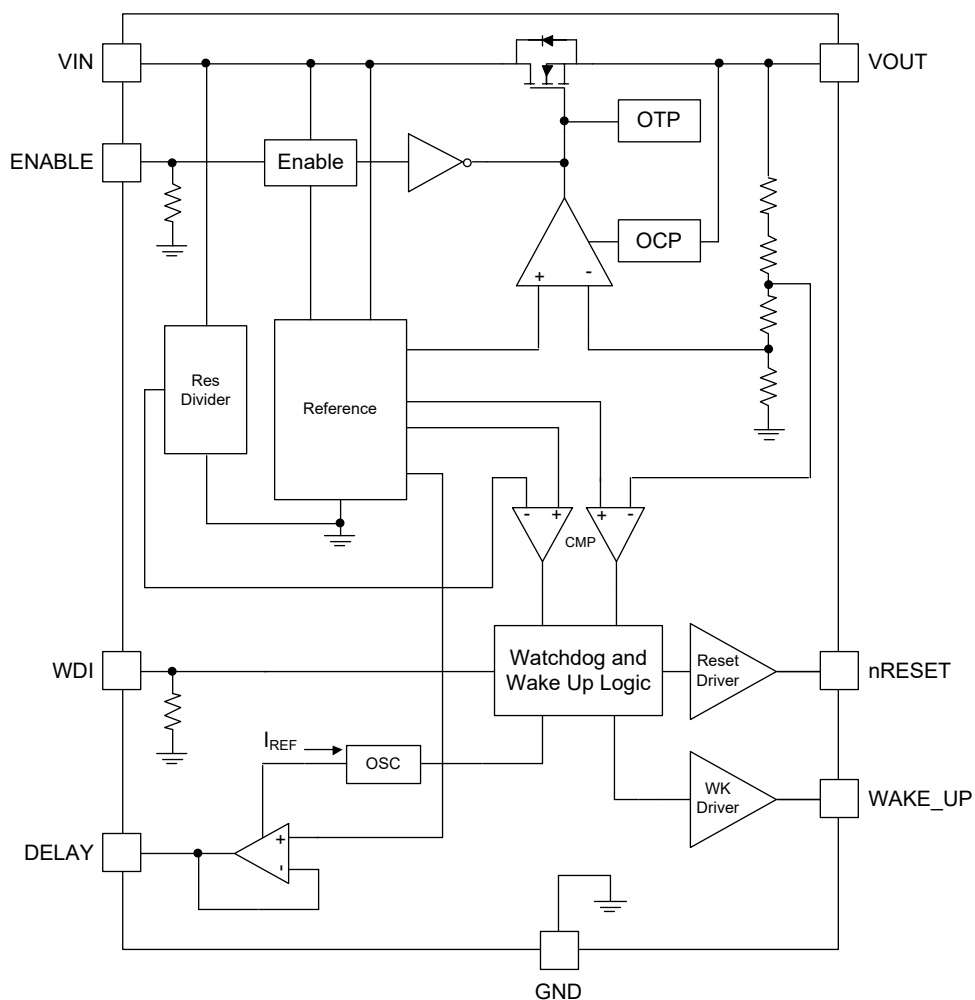
## TYPICAL PERFORMANCE CHARACTERISTICS



## TYPICAL PERFORMANCE CHARACTERISTICS (continued)



## FUNCTIONAL BLOCK DIAGRAM



### Figure 5. Block Diagram



## DETAILED DESCRIPTION

### General

The SGM70411 is a high precision linear low dropout regulator with enable, watchdog, wake-up and reset functions. It has low supply current of 85μA (TYP) at 100μA load and low dropout voltage of 260mV (TYP) at 150mA load. With the two advantages mentioned above, this device is very suitable for battery powered consumer electronics.

The SGM70411 has built-in short-circuit protection and thermal shutdown function without any external elements. It can still work properly under extremely high transient voltage up to 45V.

### Wake Up and Watchdog

To reduce the power loss of the battery when no code is executing, the micro-processor usually goes into the sleeping mode in order to consume very low supply current. The SGM70411 periodically provides wake-up signal that tries to break the sleeping mode. At the rising edge of the wake up signal, a WDI signal is sent out by the micro-processor and checked to determine whether the SGM70411 stays in the sleeping mode or wakes up to the normal mode. Typically, the wake-up signal is a 5V square wave with a duty cycle of 50% generated by  $V_{OUT}$ . The frequency of the wake-up signal is decided by the external resistor placed between the DELAY pin and GND.

The falling edge of the WDI signal is effective for the SGM70411. When an effective WDI pulse is recognized, the WAKE UP pin is pulled low and other pulses from WDI are aborted in this wake-up period. Note that the watchdog module continues to receive and monitor the WDI signal. Once no WDI falling edge is detected during a wake-up period, the nRESET pin will be pulled low at the end of the wake-up cycle (see Figure 3).

### nRESET

When  $V_{OUT}$  drops and the nRESET pin goes low, the nRESET keeps low until  $V_{OUT} < 1V$ . The nRESET goes low for any of four conditions:

1. The nRESET pin maintains low until  $V_{OUT}$  is higher than the nRESET positive-going threshold in the power-on process.

2. When  $V_{OUT}$  is in regulation, the nRESET goes low as  $V_{OUT}$  falls under the nRESET negative-going threshold. The nRESET will not turn high unless the following two conditions are simultaneously met:

1).  $V_{OUT}$  is higher than the nRESET positive-going threshold.

2). The new reset delay POR is finished.

3. No effective WDI falling edge is detected in a wake-up period.

4. The VIN voltage is too low, and the internal circuits cannot work properly. This voltage value of VIN is related to temperature. For example, it is about 4.5V at +25°C.

The WAKE\_UP pin goes low when nRESET is asserted. After the nRESET returns high, the wake-up timer starts to count again (see Figure 3).

The wake-up period, nRESET delay time and nRESET high to wake-up delay time are determined by  $R_{DELAY}$ , described as below:

$$\text{Wake-up period(s)} = (4.18 \times 10^{-7}) \times R_{DELAY}(\Omega) \quad (1)$$

$$\text{nRESET delay time(s)} = (5.21 \times 10^{-8}) \times R_{DELAY}(\Omega) \quad (2)$$

$$\begin{aligned} \text{nRESET high to wake-up delay time(s)} \\ = (2.08 \times 10^{-7}) \times R_{DELAY}(\Omega) \end{aligned} \quad (3)$$

The DELAY pin voltage is generated from the bandgap and is intended to be used as a voltage reference.

### Enable

The ENABLE pin is used to turn on or turn off the SGM70411 and can be applied with TTL or CMOS logic level. Logic high means the device is enabled and turned on while logic low means the device is disabled and turned off. When in disabled status, the overall supply current decreases to no more than 1.5μA.

## REVISION HISTORY

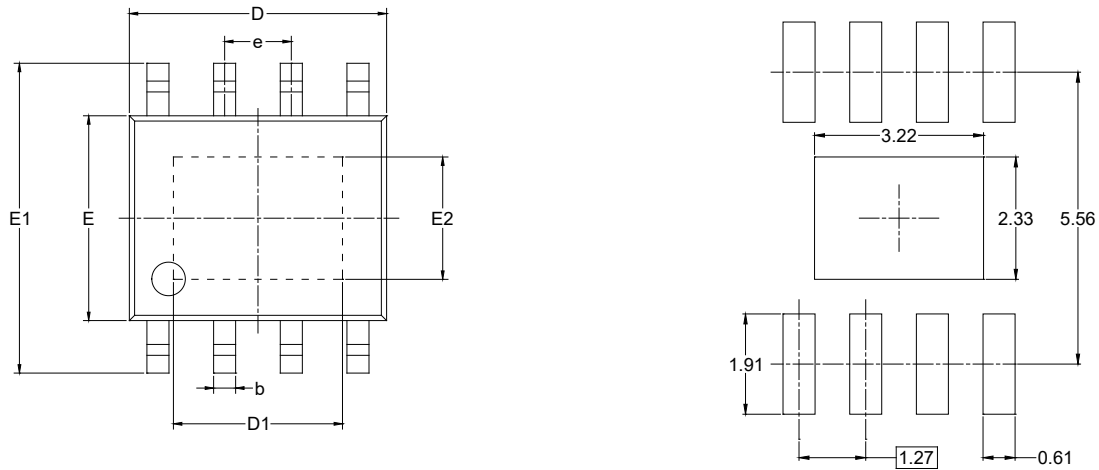
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

### Changes from Original to REV.A (JUNE 2025)

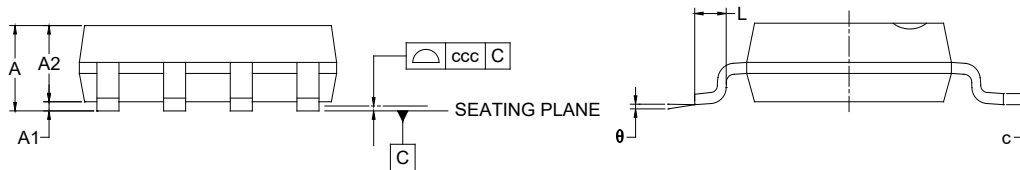
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## PACKAGE OUTLINE DIMENSIONS

### SOIC-8 (Exposed Pad)



RECOMMENDED LAND PATTERN (Unit: mm)



Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A			1.700
A1	0.000	-	0.150
A2	1.250	-	1.650
b	0.330	-	0.510
c	0.170	-	0.250
D	4.700	-	5.100
D1	3.020	-	3.420
E	3.800	-	4.000
E1	5.800	-	6.200
E2	2.130	-	2.530
e	1.27 BSC		
L	0.400	-	1.270
θ	0°	-	8°
ccc	0.100		

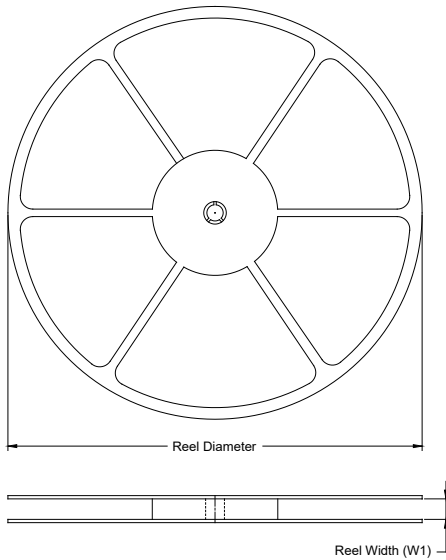
#### NOTES:

1. This drawing is subject to change without notice.
2. The dimensions do not include mold flashes, protrusions or gate burrs.
3. Reference JEDEC MS-012.

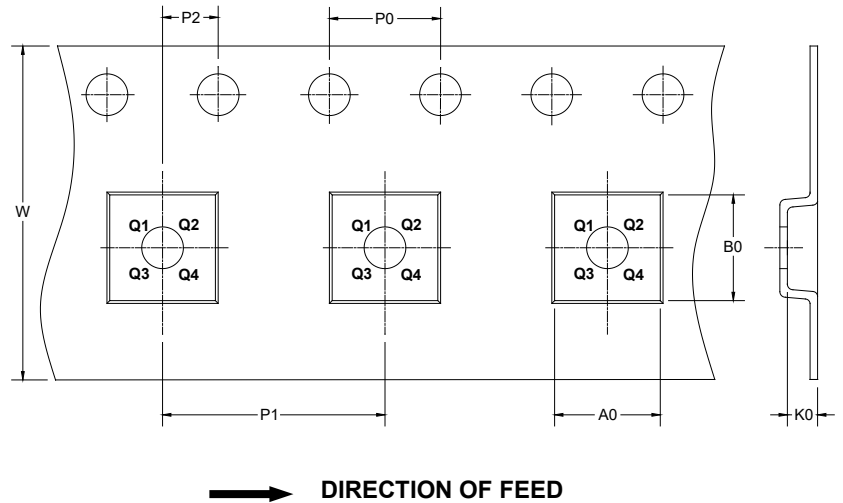
# PACKAGE INFORMATION

## TAPE AND REEL INFORMATION

### REEL DIMENSIONS



### TAPE DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

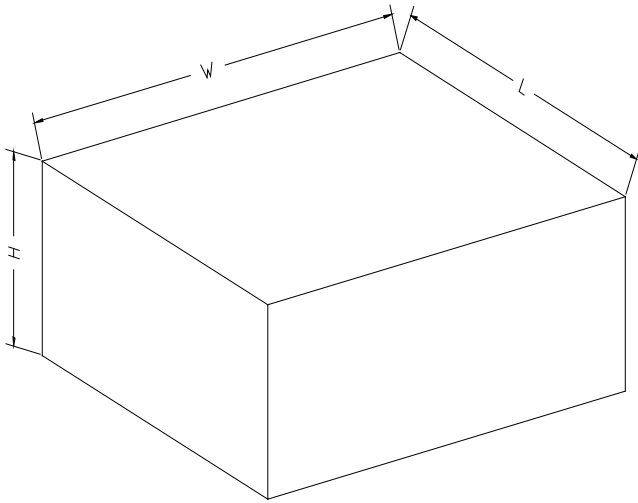
### KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
SOIC-8 (Exposed Pad)	13"	12.4	6.40	5.40	2.10	4.0	8.0	2.0	12.0	Q1

DD00001

## PACKAGE INFORMATION

### CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

### KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13"	386	280	370	5

DD0002