SGM62138
36V Input and Output, Bi-Directional Buck-Boost Controller

GENERAL DESCRIPTION

The SGM62138 is a wide input and output bi-directional 4-switch Buck-Boost controller. The device is capable to operate at 36V input and output, and withstands up to an absolute maximum of 40V. The device integrates four 2A drivers which is suitable for most common catalog MOSFETs. The boot diode is also integrated to reduce design complexity.

The bi-directional control of the SGM62138 enables easy implementation of battery charging and reverse OTG operations. While supporting charging Li-ion batteries up to 8 cells, the SGM62138 is also capable to program both input and output as constant voltage ports with dedicated constant current loop.

The SGM62138 integrates I^2C bus to support communication between host processor and the DC/DC. Features such as output voltage slew rate, charging profile, constant current loop threshold, and direction control are adjustable via I^2C.

Power path control is also available on SGM62138. Multi-input source control and VIN sinking device detections are implemented to reduce system design complexity.

The SGM62138 also integrates various protection features such as over-voltage protection, over-current protection, input under-voltage lockout, short-circuit protection and over-temperature protection.

The SGM62138 is available in a Green TQFN-4×4-32L package.

FEATURES

- **3V to 36V Input Voltage Range (40V ABS)**
- **3V to 36V Output Voltage Range (40V ABS)**
- **USB PD3.2 V_{IN} from 5V to 36V Supported**
- **USB PD V_{IN} Input Current Limit Setting**
- **Multi Input-Source Power Path Control**
- **150kHz to 450kHz Programmable Switching Frequency**
- **Integrated Boot Diode and 2A MOSFET Drivers**
- **Low Quiescent Current: 25μA (TYP)**
- **Bi-Directional CC/CV Loop**
- **Adaptive Soft-Start**
- **I^2C Interface for Device Status Report and Setting Configuration**
- **Bi-Directional Power Path Direction Control**
- **Programmable Light Load PFM Mode or FPWM Mode**
- **Short-Circuit and Over-Voltage Protection**
- **Thermal Shutdown Protection**
- **Available in a Green TQFN-4×4-32L Package**

APPLICATIONS

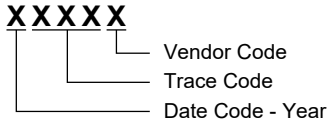
Battery Backup
Power Tool
USB PD

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM62138	TQFN-4×4-32L	-40℃ to +125℃	SGM62138XTQU32G/TR	SGM62138 XTQU32 XXXXX	Tape and Reel, 3000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

VIN, VOUT, ISNS+, ISNS-, CC+, CC-, SW1, SW2, nEN, USBDET1, USBDET2, USBDV1, USBDV2/DITHER, FB, VOS ..... -0.3V to 40V
BOOT1, BOOT2, HG1, HG2 ..... -0.3V to 46V
VIN to ISNS+, ISNS- ..... -0.3V to 11V
VOUT to CC+, CC- ..... -0.3V to 11V
ISNS+ to ISNS- ..... -10V to 10V
CC+ to CC- ..... -10V to 10V
BOOT1, HG1 with Respect to SW1 ..... -0.3V to 6V
BOOT2, HG2 with Respect to SW2 ..... -0.3V to 6V
SDA, SCL, COMP, ADC, INT, BIAS, VCC, PSTOP .....
..... -0.3V to 6V
Package Thermal Resistance
TQFN-4×4-32L, θ_{JA} ..... 33.8℃/W
TQFN-4×4-32L, θ_{JB} ..... 10.7℃/W
TQFN-4×4-32L, $\theta_{JC\ (TOP)}$ ..... 24.1℃/W
TQFN-4×4-32L, $\theta_{JC\ (BOT)}$ ..... 1.5℃/W
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility (1) (2)
HBM ..... ±2000V
CDM ..... ±1000V

NOTES:

1. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.

2. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

RECOMMENDED OPERATING CONDITIONS

Input Voltage Range ..... 3V to 36V
Output Voltage Range ..... 3V to 36V
Operating Junction Temperature Range ..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

SIMPLIFIED SCHEMATIC

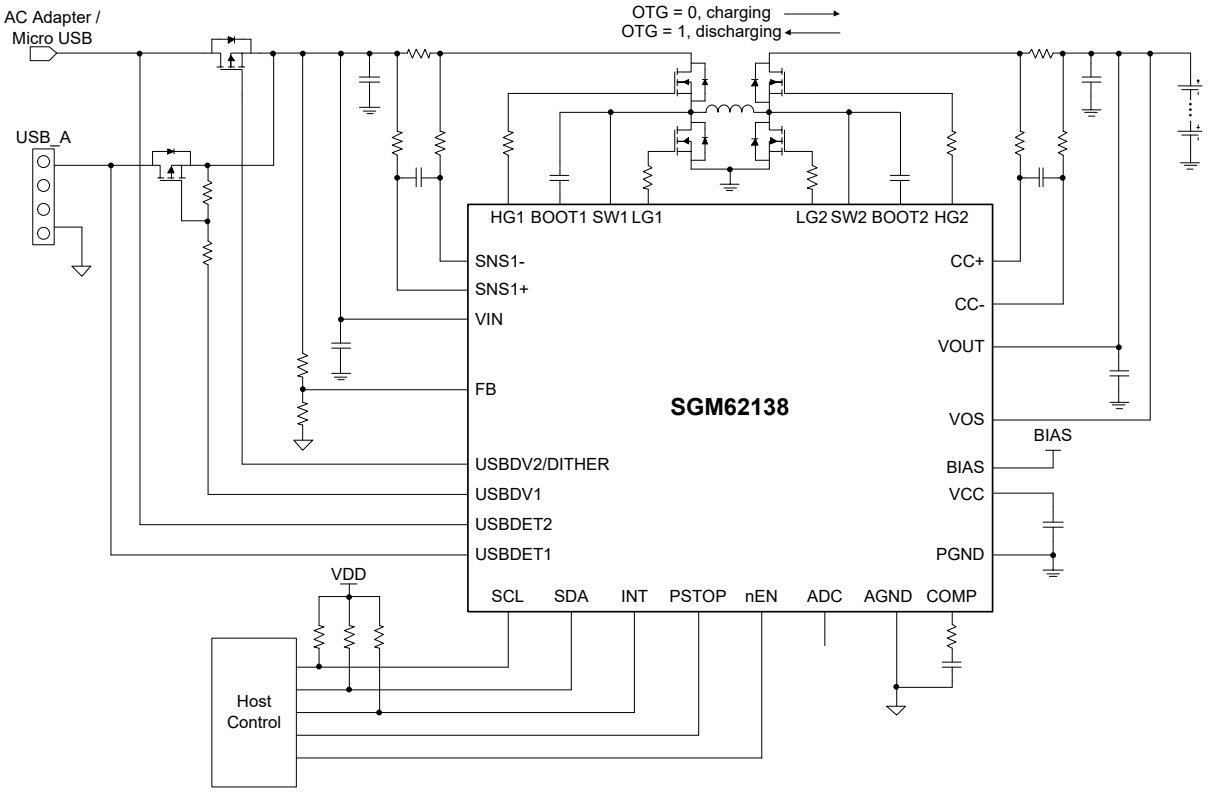
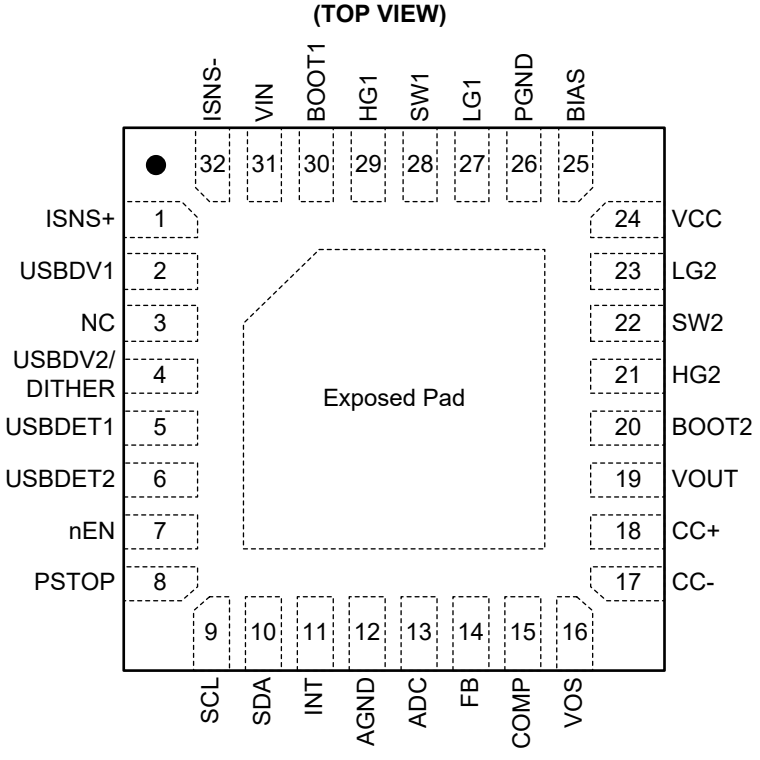


Figure 1. Simplified Schematic

PIN CONFIGURATION

(TOP VIEW)



TQFN-4×4-32L

PIN DESCRIPTION

PIN	NAME	TYPE	FUNCTION
1	ISNS+	P	Positive Input of the Current Sense Amplifier. Connect this pin to one pad of the current sense resistor (typically 10mΩ) on the power path to sense current flowing into or out of the VIN. It is recommended to add a filter (2.2Ω + 22nF + 2.2Ω) between the ISNS+ and ISNS- pins, and place the filter as close to the chip as possible. In Buck mode applications with high input voltage and low output current (especially at 50% duty cycle), the external filter resistor can be increased (e.g., 20Ω) to improve negative current sensing.
2	USBDV1	DO	General-Purpose Open-Drain Output Controlled by the EN_USBDV1 Bit. It can drive an external PMOS with a pull-up resistor and is recommended for discharging phase.
3	NC	—	This pin is not electrically connected internally. It can be kept open/floating, connected to GND or any other signal.
4	USBDV2/DITHER	AI/AO	The PMOS gate driver is controlled by the USBDV2 bit and is used to regulate the external PMOS on the power path. This pin supports configuration for the switching frequency dithering function via I^2C. When enabling the frequency dithering function (set EN_DITHER bit to 1), connect a ceramic capacitor (typically 100nF) from this pin to ground.
5	USBDET1	AI	Connect this pin to a USB-A port to detect load insertion events. If an insertion event is detected, the IC sets the USBDET1 bit and outputs an interrupt (INT) pulse to notify the MCU.
6	USBDET2	AI	Connect this pin to the AC adapter input node or the micro-USB port to detect AC adapter insertion events. If an insertion event is detected, the IC sets the AC_OK bit and outputs an interrupt (INT) pulse to notify the MCU.
7	nEN	DI	Active-Low Logic. If this pin is pulled high, both the power switch and the I^2C interface are disabled. This pin has an internal pull-down resistor.
8	PSTOP	DI	Active-Low Logic. Pull this pin to logic high, the chip enters standby mode, the power blocks are disabled, only the AC adapter, load insertion detection, and I^2C circuits remain active. This pin has an internal pull-down resistor.
9	SCL	DI	I^2C Interface Clock (SCL). Connect SCL to the logic high rail via a pull-up resistor (typically 10kΩ). The IC operates as a slave device, with the I^2C address set to 0x74.
10	SDA	DI/DO	I^2C Interface Data (SDA). Connect SDA to the logic high rail via a pull-up resistor (typically 10kΩ).
11	INT	DO	Open-Drain Output for Interrupt Signal. When an interrupt event occurs, the IC outputs a low logic pulse on the INT pin to notify the host.
12	AGND	GND	Analog Ground (AGND). Connect AGND and PGND together to the thermal pad on the underside of the IC.
13	ADC	AI	ADC Input Pin. Apply an analog signal (≤ 2.048V) to this pin. The internal 10-bit ADC converts the analog signal to a digital value and stores the result in a register.
14	FB	AI	Feedback Node for VIN Voltage. Connect a resistor divider between VIN pin and FB pin to set the VIN voltage via an external network in OTG mode. The FB reference voltage can also be programmed via the I^2C interface.
15	COMP	AI	Connect a series RC compensation network from this pin to AGND to compensate the control loop.
16	VOS	AI	Sense Node for VOUT Voltage. Connect to the VOUT rail when the internal feedback is selected for VOUT charging termination voltage setting. Connect a resistor divider from VOUT when the external feedback is selected.
17	CC-	P	Negative Input of the Current Sense Amplifier. Connect this pin to one pad of the current sense resistor (typically 10mΩ) on the power path to sense current flowing into or out of the battery. It is recommended to add a filter (2.2Ω + 22nF + 2.2Ω) between the CC+ and CC- pins, and place the filter as close to the chip as possible. In Buck mode applications with high input voltage and low output current (especially at 50% duty cycle), the external filter resistor can be increased (e.g., 20Ω) to improve negative current sensing.

PIN DESCRIPTION (continued)

PIN	NAME	TYPE	FUNCTION
18	CC+	P	Positive Input of the Current Sense Amplifier. Connect this pin to one pad of the current sense resistor (typically 10mΩ) on the power path to sense current flowing into or out of the battery. It is recommended to add a filter (2.2Ω + 22nF + 2.2Ω) between the CC+ and CC- pins, and place the filter as close to the chip as possible. In Buck mode applications with high input voltage and low output current (especially at 50% duty cycle), the external filter resistor can be increased (e.g., 20Ω) to improve negative current sensing.
19	VOUT	P	Power Supply Pin. Connect it to the battery positive node. A 1μF ceramic capacitor is recommended between this pin and PGND as close to the chip as possible.
20	BOOT2	P	Boost Mode High-side N-Channel MOSFET (Q4) Driver Power Supply. Place a 100nF capacitor between SW2 and BOOT2. It is internally connected to the Boost-strap diode cathode.
21	HG2	AO	Boost Mode High-side N-Channel MOSFET (Q4) Driver. Connect it to the gate of Q4.
22	SW2	P	Boost Mode Switching Node. Connect it to the source of the Boost mode high-side N-channel MOSFET (Q4).
23	LG2	AO	Boost Mode Low-side N-Channel MOSFET (Q3) Driver. Connect it to the gate of Q3.
24	VCC	P	5V LDO Output. It is supplied by VIN or VOUT. A 1μF ceramic capacitor is recommended between this pin and PGND as close to the chip as possible.
25	BIAS	P	Gate Driver Supply Input. Place a less than 10Ω resistor from VCC to this pin, and place a 1μF ceramic capacitor from this pin to ground.
26	PGND	GND	Power Ground.
27	LG1	AO	Buck Mode Low-side N-Channel MOSFET (Q2) Driver. Connect it to the gate of Q2.
28	SW1	P	Buck Mode Switching Node. Connect it to the source of the Buck mode high-side N-channel MOSFET (Q1).
29	HG1	AO	Buck Mode High-side N-Channel MOSFET (Q1) Driver. Connect it to the gate of Q1.
30	BOOT1	P	Buck Mode High-side N-Channel MOSFET (Q1) Driver Power Supply. Place a 100nF capacitor between SW1 and BOOT1. It is internally connected to the boost-strap diode cathode.
31	VIN	P	Power Supply Pin. A 1μF ceramic capacitor is recommended between this pin and PGND as close to the chip as possible.
32	ISNS-	I	Negative Input of the Current Sense Amplifier. Connect this pin to one pad of the current sense resistor (typically 10mΩ) on the power path to sense current flowing into or out of the VIN. It is recommended to add a filter (2.2Ω + 22nF + 2.2Ω) between the ISNS+ and ISNS- pins, and place the filter as close to the chip as possible. In Buck mode applications with high input voltage and low output current (especially at 50% duty cycle), the external filter resistor can be increased (e.g., 20Ω) to improve negative current sensing.
—	Exposed Pad	—	Thermal Pad. It is the thermal pad to conduct heat from the device. Tie it externally to the PCB power ground plane. Thermal vias under the pad are needed to conduct the heat to the PCB power ground planes.

NOTE: AI = Analog input, AO = Analog output, AI/AO = Analog input/output, DI = Digital input, DO =Digital output, DI/DO = Digital input/output, P = Power.

ELECTRICAL CHARACTERISTICS

(V_{IN} = 5V, V_{OUT} = 10.8V, T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage						
VIN Under-Voltage Lockout Threshold (1)	V_{UVLO_VIN}	Rising edge	2.8	2.9	3	V
		Hysteresis		380		mV
VOUT Under-Voltage Lockout Threshold (1)	V_{UVLO_VOUT}	Rising edge	2.8	2.9	3	V
		Hysteresis		380		mV
Quiescent Current into VOUT	I_{Q_VOUT}	V_{IN} = 5V, PSTOP = L, non-switching		2.1	3	mA
		V_{IN} = 5V, PSTOP = L, after charging termination		1.5	2.5	
Quiescent Current into VIN	I_{Q_VIN}	PSTOP = L, non-switching		25	40	μA
Standby Current into VOUT	I_{SB_VOUT}	VIN open, PSTOP = H, AD_START = 0		8	20	μA
		VIN open, PSTOP = H, AD_START = 1		0.9	1.2	mA
Standby Current into VIN	I_{SB_VIN}	PSTOP = H, AD_START = 0		3.5	8	μA
Shutdown Current into VOUT	I_{SD_VOUT}	nEN = H, VIN open		5	10	μA
VCC, Driver and Power Switch						
VCC Regulation Voltage (1)	V_{CC}	PSTOP = L, V_{IN} = 9V		5	5.3	V
		PSTOP = L, V_{IN} = 5V		4.97	5	
		PSTOP = H, V_{OUT} = 3.6V			3	
VCC Current Limit (1)	I_{VCC_LIM}	PSTOP = L, V_{IN} = 5V, V_{CC} = 4.5V	23	31	36	mA
		PSTOP = L, V_{IN} = 9V, V_{CC} = 4.5V		160		
		PSTOP = H			2	
High/Low-side MOS Driver Pull-up Resistor	R_{HS/LS_PU}			4		Ω
High/Low-side MOS Driver Pull-down Resistor	R_{HS/LS_PD}			1		Ω
Reference Voltage in Charging Mode						
VOS Reference Voltage for External Setting (1)	V_{OS_EXT}	VOUT_SEL = 1	1.195	1.2	1.205	V
VOS Accuracy for Internal Setting, over VOS Target (1)	V_{OS_INT}	VOUT_SEL = 0, CSEL[1:0] = 00, VCELL_SET[2:0] + VCELL_SET2 = 0000 ~ 1111	-0.6		0.6	%
Trickle Charge Threshold Voltage for Internal Setting (1)	$V_{TRICKLE\_INT}$	VOUT_SEL = 0, cell number = N, VCELL_SET[2:0] + VCELL_SET2 = 0000 ~ 1111, TRICKLE_SET = 0	2.73 × N	2.94 × N	3.15 × N	V
		VOUT_SEL = 0, cell number = N, VCELL_SET[2:0] + VCELL_SET2 = 0000 ~ 1111, TRICKLE_SET = 1	2.31 × N	2.52 × N	2.73 × N	
Trickle Charge Threshold for External Setting, over VOUT Target (1)	$V_{TRICKLE\_EXT}$	VOUT_SEL = 1, TRICKLE_SET = 0	65	70	75	%
		VOUT_SEL = 1, TRICKLE_SET = 1	55	60	65	
EOC Voltage Threshold, over VOUT Target (1)	V_{EOC}	VOUT_SEL = 0/1	97.4	98.4	99.4	%
Recharge Threshold Voltage, over VOUT Target (1)	V_{RECH}	VOUT_SEL = 0/1	95.4	96.4	97.4	%
V_{INREG} Reference Voltage (1)	V_{INREG}	4.5V target, VINREG_SET = 0x2C, VINREG_RATIO = 0	4.3	4.5	4.7	V
		15V target, VINREG_SET = 0x95, VINREG_RATIO = 0	14.6	15	15.3	
		4.48V target, VINREG_SET = 0x6F, VINREG_RATIO = 1	4.4	4.48	4.6	
		10V target, VINREG_SET = 0xF9, VINREG_RATIO = 1	9.8	10	10.2	
VOUT OVP Threshold, over VOUT Target (1)	V_{OUT_OVP}	VOUT_SEL = 0/1	107.5	110	112.5	%

NOTE: 1. These parameters are initial accuracy values.

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 5V, V_{OUT} = 10.8V, T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Hysteresis	V_{OUT_OVP}	VOUT_SEL = 0/1		3		%
Clamp Voltage	V_{CLAMP}			125		mV
Reference Voltage in Discharging Mode						
FB Reference Voltage for External Setting (1)	V_{FB}	FB_SEL = 1, V_{INREF_E} target from 0.5V to 2.048V	-2		2	%
VIN Reference Voltage Accuracy for Internal Setting (1)	V_{IN}	FB_SEL = 0 VIN_RATIO = 1 (5×), V_{IN} = 3.6V to 10.24V	-2		2	%
		FB_SEL = 0 VIN_RATIO = 0 (12.5×), V_{IN} = 9V to 24V	-2		2	%
VIN OVP Threshold, Rising Edge (1)	V_{IN_OVP}	VINREF_I_SET = 1V, VINREF_E_SET = 1V	107.3	110	113	%
Hysteresis	V_{IN_OVP}	VINREF_I_SET = 1V, VINREF_E_SET = 1V		3		%
VOUT OVP Threshold, Rising Edge	V_{OUT_OVP}	VINREF_I_SET = 1V, VINREF_E_SET = 1V		105		%
Current Limit						
I_{IN} Current Limit Accuracy (1)	I_{IN_LIM}	Charging mode, 6A target IIN_RATIO = 01 (6×), IIN_LIM = 0xFF	-6		6	%
		Charging mode, 3A target IIN_RATIO = 10 (3×), IIN_LIM = 0xFF	-6		6	
		Discharging mode, 6A target IIN_RATIO = 01 (6×), IIN_LIM = 0xFF	-6		6	
		Discharging mode, 3A target, IIN_RATIO = 10 (3×), IIN_LIM = 0xFF	-6		6	
I_{OUT} Current Limit Accuracy (1)	I_{OUT_LIM}	Charging mode, 6A target, IOUT_RATIO = 0 (6×), IOUT_LIM = 0xFF	-6		6	%
		Charging mode,12A target, IOUT_RATIO = 1 (12×), IOUT_LIM = 0xFF	-6		6	
		Discharging mode, 6A target, IOUT_RATIO = 0 (6×), IOUT_LIM = 0xFF	-6		6	
		Discharging mode, 12A target, IOUT_RATIO = 1 (12×), IOUT_LIM = 0xFF	-6		6	
Trickle Charge Current, over IOUT_LIM Setting	$I_{TRICKLE}$			10		%
Trickle Charge Current, over IIN_LIM Setting	$I_{TRICKLE}$			20		%
EOC Current Threshold, over IIN_LIM/IOUT_LIM Setting	I_{EOC}	EOC_SET = 0		4		%
		EOC_SET = 1		10		
Error Amplifier						
Error Amplifier Gm	Gm_{EA}		0.13	0.16	0.19	mS
COMP Sink Current	I_{SINK_COMP}			32		μA
COMP Source Current	I_{SRC_COMP}			24		μA
FB Pin Input Bias Current	I_{BIAS_FB}	FB_SEL = 1, FB in regulation			50	nA
Switching						
Switching Frequency (1)	f_{SW}	FREQ_SET[1:0] = 00 (150kHz)	130	150	180	kHz
		FREQ_SET[1:0] = 01 (300kHz)	265	300	335	kHz
		FREQ_SET[1:0] = 11 (450kHz)	400	450	500	kHz
Power Path Management						
USBDV2 Pin Pull-up Resistor	R_{PU_USBDV2}	EN_USBDV2 = 0		20		kΩ
USBDV2 Pin Pull-down Resistor	R_{PD_USBDV2}	EN_USBDV2 = 1		6		kΩ
Clamp Voltage from VIN to USBDV2 Pin	V_{CLAMP}	EN_USBDV2 = 1	7.1	7.4	7.7	V
USBDV1 Pin Pull-down Resistor	R_{PD_USBDV1}	EN_USBDV1 = 1		6		kΩ

NOTE: 1. These parameters are initial accuracy values.

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 5V, V_{OUT} = 10.8V, T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Detection						
AC Detection Threshold	V_{AC_DET}		2.9	3.2	3.5	V
Short-Circuit Detection Threshold	V_{SHORT}		0.95	1	1.05	V
I^2C and Logic Control						
PSTOP Pin Internal Pull-down Resistor	R_{PD}		0.8	1.05	1.3	MΩ
PSTOP, SCL, SDA Input Low Voltage	V_{IL}				0.4	V
PSTOP, SCL, SDA Input High Voltage	V_{IH}		1.2			V
INT Pin Sink Current	I_{SINK_INT}	V_{INT} = 0.4V	0.35	0.4	0.45	mA
SDA Pin Sink Current	I_{SINK_SDA}	V_{SDA} = 0.4V		50		mA
Interrupt Pulse Width (Logic Low)	t_{PULSE}		0.6	1	1.6	ms
Soft-Start						
Deglitch Time for Charging	$t_{DEGLITCH}$	PSTOP = L, EN_OTG = 0, V_{IN} = 5V, from PSTOP low to IC starting charging		220		ms
Internal Soft-Start Time	t_{SS}	V_{IN} from 0V to 5V in discharging mode, VIN_RATIO = 1 (5×)		16		ms
Thermal Shutdown						
Thermal Shutdown Temperature	T_{SD}			165		℃
Hysteresis	T_{SD_HYS}			15		℃

FUNCTIONAL BLOCK DIAGRAM

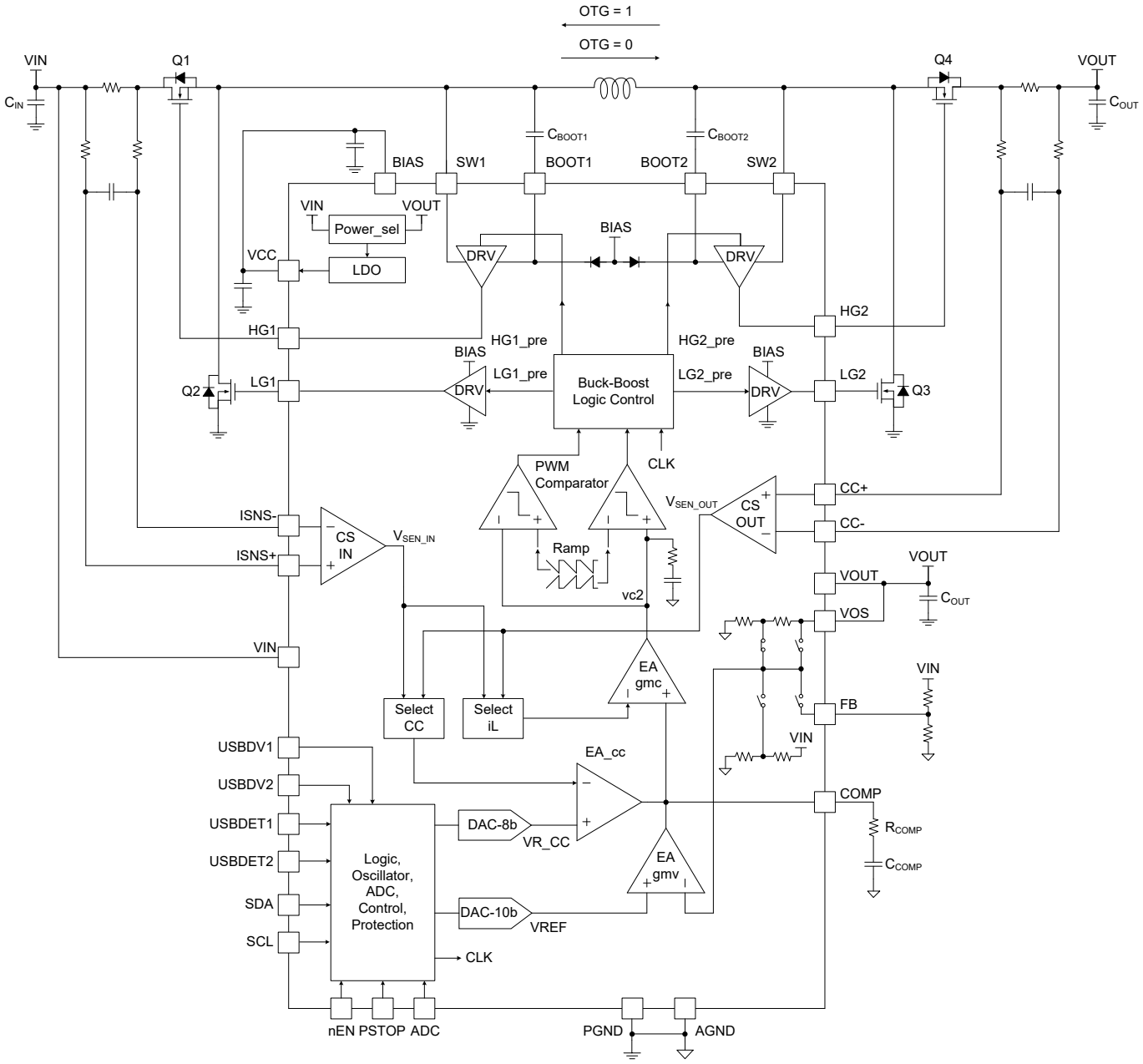


Figure 2. Block Diagram

DETAILED DESCRIPTION

Charging Mode

Users can select between charging and discharging modes via the EN_OTG bit.

When the EN_OTG bit is set to 0, the chip operates in charging mode, with current flowing from VIN to VOUT to charge the battery cells. The battery charging profile for this mode is shown in Figure 3.

If the battery cell voltage is below the trickle charge voltage threshold, the chip enters the trickle charge phase, supplying a small trickle charge current to the cells.

Once the battery cell voltage exceeds the trickle charge voltage threshold, the chip switches to the constant current charging mode. In this phase, the battery cells are charged at a constant current set by either the I_{IN} limit or I_{OUT} limit.

When the battery cell voltage reaches the target termination voltage, the chip enters the constant voltage charging phase. During this phase, the charging current gradually decreases until it falls below the termination current threshold.

When the chip satisfies the termination charging conditions for current and voltage, it enters the End of Charge (EOC) phase. During this phase, the chip can either stop charging entirely or keep charging the battery cells.

Trickle Charge

Users can set the trickle charge voltage threshold to either 60% or 70% of the single battery cell voltage (4.2V) via the TRICKLE_SET bit. During the trickle charging phase, the charging current can be reduced to a low level by setting the ICHAR_SEL bit to 1 or 0:

When ICHAR_SEL bit is 0, I_{IN} equals 20% of the IIN_LIM setting.

When ICHAR_SEL bit is 1, I_{OUT} equals 10% of the IOUT_LIM setting.

The trickle charging phase can be disabled by setting the DIS_TRICKLE bit to 1 when not required.

CC Charge (Constant Current Charge)

When the battery cell voltage exceeds the trickle charge voltage threshold, the chip enters the constant current charging mode. The battery cells are then charged at a constant current (either IIN_LIM or IOUT_LIM), which can be set via the IIN_LIM_SET and IOUT_LIM_SET registers respectively. The current limit value is related to the current sense resistor and ratio bits, and can also be adjusted dynamically. Refer to the REGISTER MAP section for details.

In CC charging mode, the chip regulates charging current at either IIN_LIM or IOUT_LIM whichever hits its limit first. For example, if the I_{IN} current limit is set to 3A and the I_{OUT} limit to 10A, the chip will limit I_{IN} to 3A once it reaches that level, even if I_{OUT} is only 6A (well below its 10A limit).

Note that none of the current limits should be set to 0A. A minimum current limit above 0.3A must be maintained.

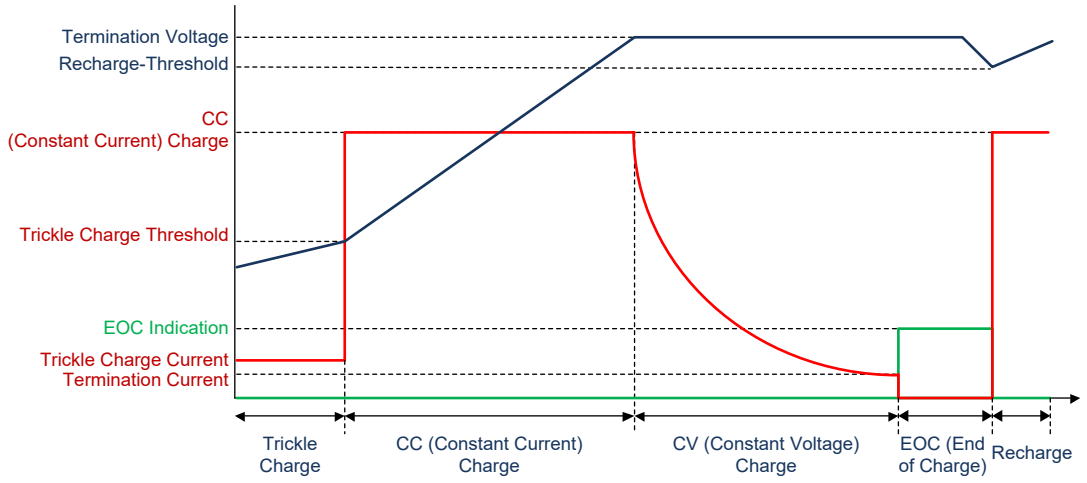


Figure 3. Battery Charging Profile

DETAILED DESCRIPTION (continued)

CV Charge (Constant Voltage Charge)

Users can select either internal or external feedback via the VOUT_SEL bit.

When the VOUT_SEL bit is set to 0, the internal feedback is enabled.

When the VOUT_SEL bit is set to 1, the external feedback is enabled.

Internal Feedback

The VOS pin must be connected to the VOUT terminal to sense the battery cell voltage.

Users can set the target battery cell voltage via the CSEL[1:0], CSEL2 bits and the VCELL_SET[2:0], VCELL_SET2 bits. The CSEL[1:0] and CSEL2 bits configured the number of series-connected battery cells, while the VCELL_SET[2:0] and VCELL_SET2 bits set the voltage rating per battery cell.

Table 1. Battery Cell Selection

0x20 D[7], 0x00 D[4:3]	N Cell
0 00	1S
0 01	2S
0 10	3S
0 11	4S
1 00	5S
1 01	6S
1 10	7S
1 11	8S

Table 2. Battery Cell Voltage Selection

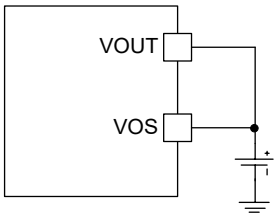
0x00 D[2:0], 0x20 D[4]	Battery Cell Voltage (V)	0x00 D[2:0], 0x20 D[4]	Battery Cell Voltage (V)
000 0	4.1	000 1	3.65
001 0	4.2	001 1	4.05
010 0	4.25	010 1	4.175
011 0	4.3	011 1	4.225
100 0	4.35	100 1	4.325
101 0	4.4	101 1	4.375
110 0	4.45	110 1	4.425
111 0	4.5	111 1	4.55

External Feedback

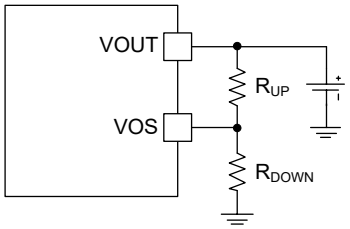
The feedback resistor divider is used at the VOS pin to set the target voltage.

The reference voltage of V_{OS} is 1.2V, and the calculation is as follows:

$$V_{OUT} = V_{OS} \times \left(1 + \frac{R_{UP}}{R_{DOWN}}\right) \quad (1)$$



(a) VOUT_SEL = 0



(b) VOUT_SEL = 1

Figure 4. Battery Voltage Setting

Once the battery cell voltage reaches 98.4% of the target voltage, the chip enters the constant voltage charging phase. During this phase, the charging current gradually decreases until it falls below the termination current threshold, while the VOUT voltage is regulated to the target value.

EOC (End of Charge)

When the chip enters the End of Charge (EOC) phase, the EOC interrupt bit will send an interrupt signal to inform the MCU. The voltage and current conditions for entering the EOC phase are as follows.

The battery cell voltage exceeds 98.4% of target value.

The I_{IN} or I_{OUT} current (determined by the ICHAR_SEL bit) falls below either 1/10 or 1/25 of its current limit value (selected via the EOC_SET bit).

In the EOC phase, users can configure the DIS_TERM bit to either terminate charging or continue charging. If the chip continues charging, it will regulate the battery cell voltage to the set value.

DETAILED DESCRIPTION (continued)

Recharge

When an End of Charge (EOC) event occurs and the chip terminates charging, the battery voltage may decrease gradually due to leakage current or the self-discharge current of the battery. Once the VOUT voltage falls below 96.4% of the set voltage, the EOC bit clears, and the chip re-enters constant current (CC) charging phase to recharge the battery.

Self-Adaptive Charging Current (V_{INREG})

The chip incorporates dynamic power management functionality. The minimum allowable VIN operating voltage is defined by the V_{INREG} threshold, which can be dynamically configured via the VINREG_SET register and VINREG_RATIO bit. During charging, if the I_{IN} charging current exceeds the maximum current capacity of the adapter, the adapter enters an overload state and the VIN voltage decreases. Once the VIN voltage falls to the V_{INREG} threshold, the chip automatically reduces the charging current and regulates the VIN voltage at this threshold.

Battery Impedance Compensation

The chip offers battery impedance compensation functionality. User can set the compensation impedance via the IRCOMP[1:0] bits, which adjusts the target VOUT voltage during the CV phase as follows:

$$V_{OUT\_COMP} = V_{OUT\_SET} + MIN[I_{OUT} \times I_{RCOMP}, V_{CLAMP}] \quad (2)$$

Where,

V_{OUT_COMP} = Compensated target battery voltage.

V_{OUT_SET} = Originally set battery termination voltage.

I_{OUT} = Charging current at the battery side.

I_{RCOMP} = Resistance compensation value set via the IRCOMP[1:0] bits.

V_{CLAMP} = Maximum allowable compensation value (fixed at 125mV).

Users must carefully evaluate the actual battery impedance. If the I_{RCOMP} setting exceeds the actual battery impedance, over-charging may occur.

Discharging Mode

When the EN_OTG bit is set to 1, the chip enters discharging mode (with current flows from VOUT to VIN). In discharging mode, users can select either internal or external feedback via the FB_SEL bit.

When the FB_SEL bit is set to 0, the internal feedback is enabled.

When the FB_SEL bit is set to 1, the external feedback is enabled.

Internal Feedback

The VIN output voltage can be configured via the VINREF_I_SET, VINREF_I_SET2 registers and the VIN_RATIO bit. The recommended VIN voltage range is 3V to 36V.

When VIN voltage is below 10.24V, it is recommended to set VIN_RATIO to 5x, resulting in a minimum adjustment step of 10mV/step.

For VIN voltages range from 10.24V to 25.6V, setting VIN_RATIO to 12.5x, with a minimum adjustment step of 25mV/step.

When VIN voltage exceeds 25.6V, VIN_RATIO must be set to 18.75x, which provides a minimum adjustment step of 37.5mV/step.

External Feedback

The feedback resistor divider is used at the FB pin to set the target voltage, with the calculation as follows:

$$V_{IN} = V_{INREF\_E} \times \left(1 + \frac{R_{UP}}{R_{DOWN}}\right) \quad (3)$$

R_{UP}/R_{DOWN} is recommended to be less than 25. When using external feedback, users can also dynamically adjust the VIN voltage by changing the reference voltage (V_{INREF_E}) via the VINREF_E_SET and VINREF_E_SET2 registers.

The recommended range voltage for V_{INREF_E} is 0.5V to 2.048V (1V default).

The I_{IN} and I_{OUT} current limits are still functional during discharging mode and support dynamic adjustment.

Note that none of the current limits should be set to 0A. A minimum current limit above 0.3A must be maintained.

DETAILED DESCRIPTION (continued)

Soft-Start

The chip integrates a soft-start control function for discharging mode. The I_{IN} current limit fold back to 20% of I_{IN} set value, and the I_{OUT} current limit fold back to 10% of I_{OUT} set value when V_{IN} is below V_{SHORT} (1V, TYP). Meanwhile, the internal reference voltage of the chip ramps up gradually (~ 10ms) to limit inrush current.

If the chip starts up with a load applied to VIN, the VIN voltage may fail to rise above V_{SHORT} due to 10% of the I_{OUT} current limit and 20% of the I_{IN} current limit. For applications requiring startup under load, the current limit fold-back function can be disabled by setting the DIS_ShortFoldBack bit to 1. To maintain short-circuit protection following startup, the DIS_ShortFoldBack bit can be reset to 0 to re-enable the function. Refer to the VIN Short Protection section for detailed specifications.

Slew Rate Setting

When users dynamically adjust the VIN voltage via the internal reference voltage configuration registers (VINREF_I_SET/VINREF_I_SET2 or VINREF_E_SET /VINREF_E_SET2), the slew rate of the internal reference voltage can be precisely controlled using the SLEW_SET bits.

For example, if the internal V_{IN} ratio of the chip is set to 5x. An initial measured value of V_{INREF_I} = 1V corresponds to an actual V_{IN} of 5V. When users adjust V_{INREF_I} to 1.6V, the output voltage is updated to 8V. With a rising slew rate of 2mV/μs, the V_{IN} will ramp up to 8V in 300μs, calculated as: 600mV ÷ 2mV/μs.

PFM Operation

Users can select the PFM mode operation in discharging mode by setting the EN_PFM bit to 1.

If the chip operates in PWM mode, it will always operate at a constant switching frequency throughout the load range. Although the output voltage can achieve the best performance, the higher switching loss will result in lower efficiency under light load conditions.

If the PFM mode is selected, the chip will operate at a pulse frequency modulation during light load conditions. In this mode, the switching loss can be reduced and the efficiency will be improved under light load conditions, while the output voltage ripple will be a little larger compared with PWM operation. A heavy load forces the chip to operate at a constant switching frequency. The output voltage behavior of the PFM mode is shown in the Figure 5.

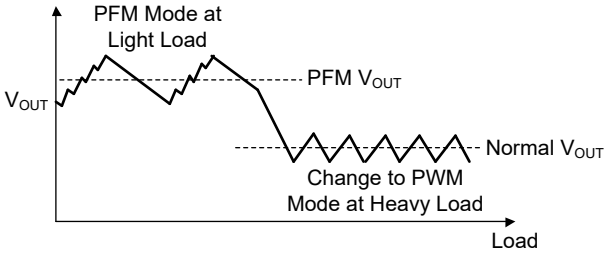


Figure 5. PFM/PWM Mode Behavior

ADC for Voltage and Current Monitor

The chip supports an analog input: ADC pin for 10-bit ADC sampling. Its maximum voltage that can sample at ADC pin is 2.048V, with a sampling resolution of 2mV/step. Whether in charging or discharging mode, this internally integrated 10-bit ADC can monitor the V_{IN}, V_{OUT}, I_{IN} and I_{OUT}. Users can enable the ADC function by setting the AD_START bit to 1. If the ADC is enabled in standby mode, the chip will draw an operating current of 0.5mA to 1mA. Refer to Register Map section for details.

Power Path Management

The IC provides power path management by its USBDV2 and USBDV1 pins.

The USBDV2 pin can drive the PMOS connected to the VIN terminal. When the EN_USBDV2 bit is set to 1, the USBDV2 pin features an internal 6kΩ pull-down resistor, with the maximum voltage between VIN pin and USBDV2 pin clamped at 7.4V. When the EN_USBDV2 bit is set to 0, the USBDV2 pin internally connects to the VIN rail through a 20kΩ pull-up resistor.

The USBDV1 pin is an open-drain output requiring an external pull-up resistor. With the EN_USBDV1 bit set to 0, USBDV1 exhibits high impedance. When the EN_USBDV1 bit is set to 1, the USBDV1 pin is pulled low internally through a 6kΩ resistor.

As shown in the Simplified Schematic, the USBDV2 pin is recommended for the charging port and the USBDV1 pin for the discharging port. However, since these control bits are managed by the MCU or system controller via an I^2C interface – which introduces communication latency – PMOS switching may not be instantaneous. For applications requiring rapid control of the isolation PMOS, the MCU I/O pins are recommended to use for direct control.

DETAILED DESCRIPTION (continued)

Phone Insert Detection

As shown in Simplified Schematic, the chip can detect the phone detection when the USBDET1 pin is connected to USB-A port.

When the chip detects that a phone has been inserted, it will set the USBDET1 interrupt bit to inform MCU, and the USBDET1 bit is cleared after it is read by MCU.

Adapter Attachment/Detachment Detection

As shown in Simplified Schematic, the chip can detect the attachment/detachment of the adapter when the USBDET2 pin is connected to Micro-USB port.

When the voltage at USBDET2 pin exceeds 3.2V, which means the adapter has been inserted, the chip sets the AC_OK interrupt bit to inform MCU about the attachment. When the voltage at USBDET2 pin is lower than 3.2V, which means the adapter has been removed, the chip clears AC_OK bit to inform the MCU about the detachment.

Switching and Frequency Dithering

The chip operates at a fixed switching frequency which can be adjusted via the FREQ_SET[1:0] bits. The switching dead time can also be set by the DT_SET bits. Refer to REGISTER MAP section for details.

The chip also supports frequency dithering function which can be enabled by setting the EN_DITHER bit to 1. If this function is enabled, the switching frequency varies within ±5% range. For example, when the switching frequency is set to 300kHz (FREQ_SET[1:0] = 01), it will change from 285kHz to 315kHz gradually and then back to 285kHz back and forth. The time it varies from the lowest to the highest frequency or from highest to lowest frequency can be controlled by a capacitor connected at USBDV2/DITHER pin as shown in the equation. For example, when a 100nF capacitor is used, the time is 1.2ms.

$$t_{DITHER} = \frac{120mV \times C}{10\mu A} \quad (4)$$

Note that if the EN_DITHER bit is set to 1, the USBDV2/DITHER pin only operates for dithering function (the USBDV2 driver function is disabled).

VCC Regulator and Driver Supply

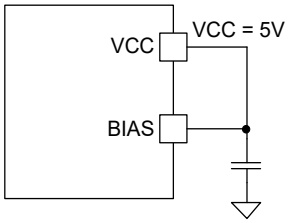
The chip integrates an LDO powered by either VIN or VOUT. This LDO generates 5V at the VCC pin with a driving capability of 40mA. In standby mode, the VCC voltage is not recommended for use, as it is unregulated and has very limited current capability. The current limit of VCC can be set by the VCC_I_LIM_SET bit.

When the VCC_I_LIM_SET bit is set to 0, the VCC current limit is 160mA (TYP).

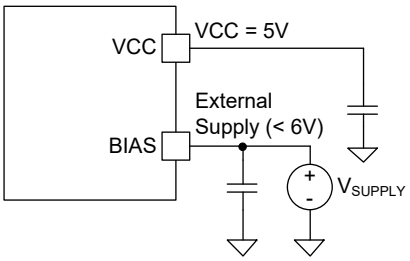
When the VCC_I_LIM_SET bit is set to 1, the VCC current limit reduces from 160mA if V_{IN} or V_{OUT} is higher than 13V.

If users need to connect external loads to the VCC pin, it is recommended that the load current be less than 50mA for safety considerations.

A power supply must be provided at the BIAS pin, which powers the internal driving circuit. There are two options: connect the VCC pin to the BIAS pin or connect an external power supply to the BIAS pin.



(a) Connect VCC to BIAS (highly recommended)



(b) Use External Supply

Figure 6. Supply for BIAS

Standby Mode

The chip enters the standby mode when the PSTOP signal is pulled high and the nEN signal is low. In this mode, the power switch turns off to minimize quiescent current, while the chip can still be controlled by the MCU through I^2C. Furthermore, the quiescent current will increase to 0.5mA ~ 1mA when the ADC function is enabled in standby mode.

DETAILED DESCRIPTION (continued)

Shutdown Mode

The chip enters shutdown mode when the nEN signal is pulled high. In this mode, both the power switch and I^2C interface are disabled. Pulling the nEN signal low will return the chip to either active mode or standby mode. The chip features an internal pull-down resistor, which can pull down the nEN signal.

Over-Voltage Protection (OVP)

The OVP function can be enabled/disabled via the DIS_OVP bit. In discharging mode, the OVP threshold at VIN pin is 110% of the target voltage. And in charging mode, the OVP threshold at VOUT pin is 110% of the target voltage. If the voltage exceeds 110% of the target voltage, the chip will shut down when the OVP function is enabled.

In discharge mode, the power switch of the chip shuts off when the voltage at the VOUT pin exceeds 105% of the battery voltage.

In charging mode, the chip also supports input over-voltage protection (IVP) function at the VIN pin, which can be set via the EN_IVP bit, and the 40V or 30V (with a 2V hysteresis) options can be selected via the IVP_SEL bit.

VIN Short Protection

If the VIN pin is shorted to GND in discharging mode, when the VIN voltage falls below V_{SHORT} (1V, TYP), the current limit of the chip will be reduced to 10% of I_{OUT} current limit and 20% of I_{IN} current limit, and an interrupt bit of VIN_SHORT will be sent to inform the MCU. If the DIS_ShortFoldBack bit is set to 1, the current limits will not be reduced.

If the VIN pin is shorted to GND in discharging mode, the chip will soft-start again when the VIN drops from above 1V to below 1V, provided that the SCP_RESTART bit is set to 0. Users can disable this function via setting the SCP_RESTART bit to 1.

Peak Current Limit

The chip supports inductor peak current limiting, which can be configured via the PEAK_OCP_SET bit and PEAK_OCP_SEL bit. Users can enable this function by setting the PEAK_OCP_SET bit to 0 (1 to disable). A threshold of 18A is selected by setting the PEAK_OCP_SEL bit to 0 (1 selects 22 A). If the inductor peak current triggers the over-current limit, the chip will soft-start again.

Over-Temperature Protection

The chip integrates an over-temperature protection (OTP) function to prevent damage caused by overheating. If junction temperature exceeds +165℃, the power switch of the chip will turn off. When OTP is triggered, an interrupt bit is set by the chip to notify the MCU. Once the temperature decreases by 15℃, the power switch will turn on automatically.

I^2C and Interrupt

I^2C Interface

Standard I^2C interface is used to program SGM62138 parameter and get the device status. I^2C is a widely used, 2-wire, bi-directional serial communication interface. The 2 bus lines are named serial clock (SCL) and serial data (SDA). The SCL and SDA should be pulled high by a current source or the pull-up resistors. When the bus lines are free, they are both at the high voltage. The SDA and SCL pins are open-drain.

All devices connected to the bus have their own addresses (7-bit) and each device may act as a master or a slave during a data transfer. The master is usually a processor or another host that initiates a data transfer and generates the clock signals to allow transmission of the data bit. All the slaves get the unique address for identification. When SGM62138 acts as a slave, the 7-bit I^2C address is 0x74. The I^2C interface of SGM62138 supports standard mode (100kbps) and fast mode (400kbps, with 5kΩ pull-up resistor at SCL pin and SDA pin) communication speeds.

Data Validity

All the data (high or low) must be remain stable on the SDA during the clock high period. The state of SDA only can change when SCL is low. For each data bit transmission, one clock pulse is generated by the master. Bit transferring procedure is shown in Figure 7.

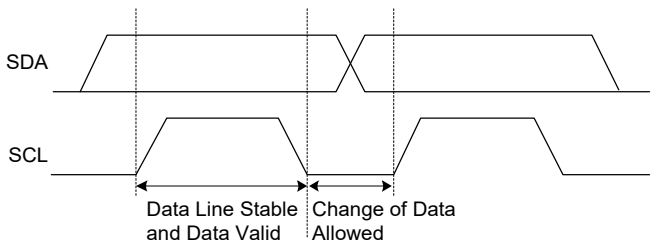


Figure 7. Bit Transfer on the I^2C Interface

DETAILED DESCRIPTION (continued)

START and STOP Conditions

If the bus is free, a transaction can be started by master. When the data transfer is completed, the transaction is terminated by releasing the bus, as shown in Figure 8. All transactions are started by the master, which applies a START (S) condition on the bus to take over the bus and exchange data. Finally, the master terminates the transaction by applying one (or more) STOP (P) conditions.

The START conditions are generated by the master converting the SDA from high to low when SCL is high. And the STOP conditions are generated by the master converting the SDA from low to high when SCL is high. The START and STOP conditions are always generated by a master. After a START and before a STOP, the bus is considered busy.

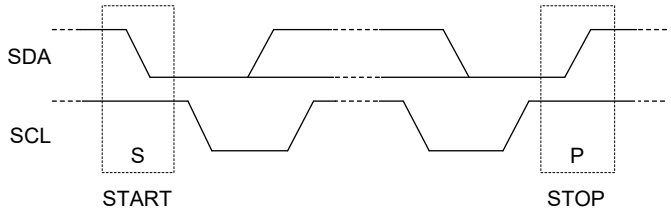


Figure 8. START and STOP Conditions

Byte Format

Data is transmitted in 8-bit packets (one byte at a time). There is no limit to the number of bytes in a transaction. In each packet, the eight bits are transferred first with the most significant bit (MSB). After 8 data bits, there must be an acknowledge (or not-acknowledge) bit.

Acknowledge (ACK) and Not Acknowledge (NCK)

After the transmitter sends each byte, the receiver replies with an acknowledgement bit, the ninth bit. With this acknowledgement bit, the receiver informs the transmitter that the byte is received, and another byte is expected or can be sent (ACK), or that another byte is not expected to be sent (NCK = not ACK). The clock (SCL) is always generated by the master, including the acknowledge clock pulse, regardless of the transmitter or receiver. And the receiver can pull the SDA line low as ACK (reply a 0 bit) or let it be high as NCK during the SCL high pulse.

The master can choose a STOP to end the transaction, or send a new START condition to start a new transmission (known as a repeated start). For example, when the master wants to read a register on a slave, one START is required to send the slave address and the register address, and then, without a STOP condition, the master sends another START to initiate a receive transaction on the slave. The master then sends a STOP condition and releases the bus.

The Slave Address and R/W Bit

After sending a START condition, the master sends the slave address (7 bits) with the 8th data-direction bit (R/W) to notify the slave whether the following data byte should be received by the slave (WRITE) or whether the slave should return a byte of data to the master (READ). After receiving the ACK from the addressed slave, the master continues to send more clock pulses for future reads or writes. Typically, the second byte is also a WRITE containing the address of the register that the master wants to access in the slave.

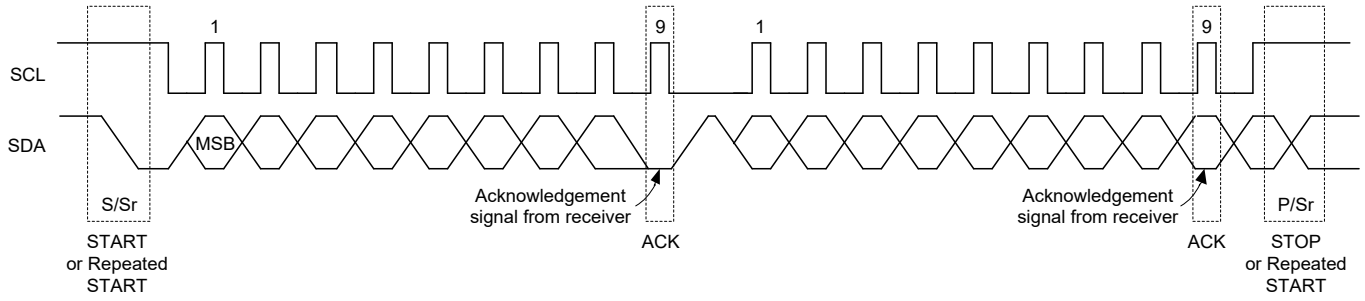


Figure 9. Data Transfer on the I^{2}C Bus

DETAILED DESCRIPTION (continued)

WRITE: If the sequence is a single write and the master wants to perform a write operation in the slave's addressing register, the third byte will be the contents of the addressing register, as shown in Figure 12 for a single write data transfer.

READ: If the sequence is single read and the master wants to read the contents of the addressing register in the slave, the master first sends a new START (repeat START) before the third byte because the read/write direction needs to be changed from write to read. Therefore, the third byte is still from the address (7 bits) and the 8th data direction bit will be R/W = 1. The slave will send an ACK bit followed by the contents of the register as the fourth byte. The master can reply with either an ACK or NCK and then issue a STOP condition. Data read from an unlisted register address will be 00h.

The device register contents are updated on the falling edge of the acknowledge signal after the last byte.

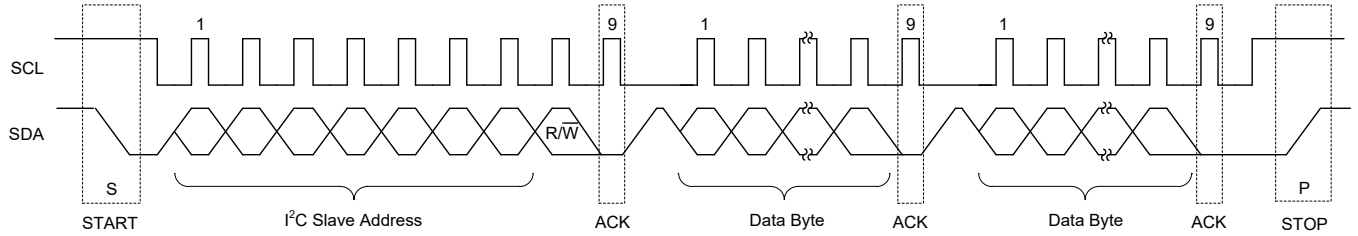


Figure 10. A Complete Data Transfer

Figure 11. The First Byte after the START Procedure

Single Read and Write

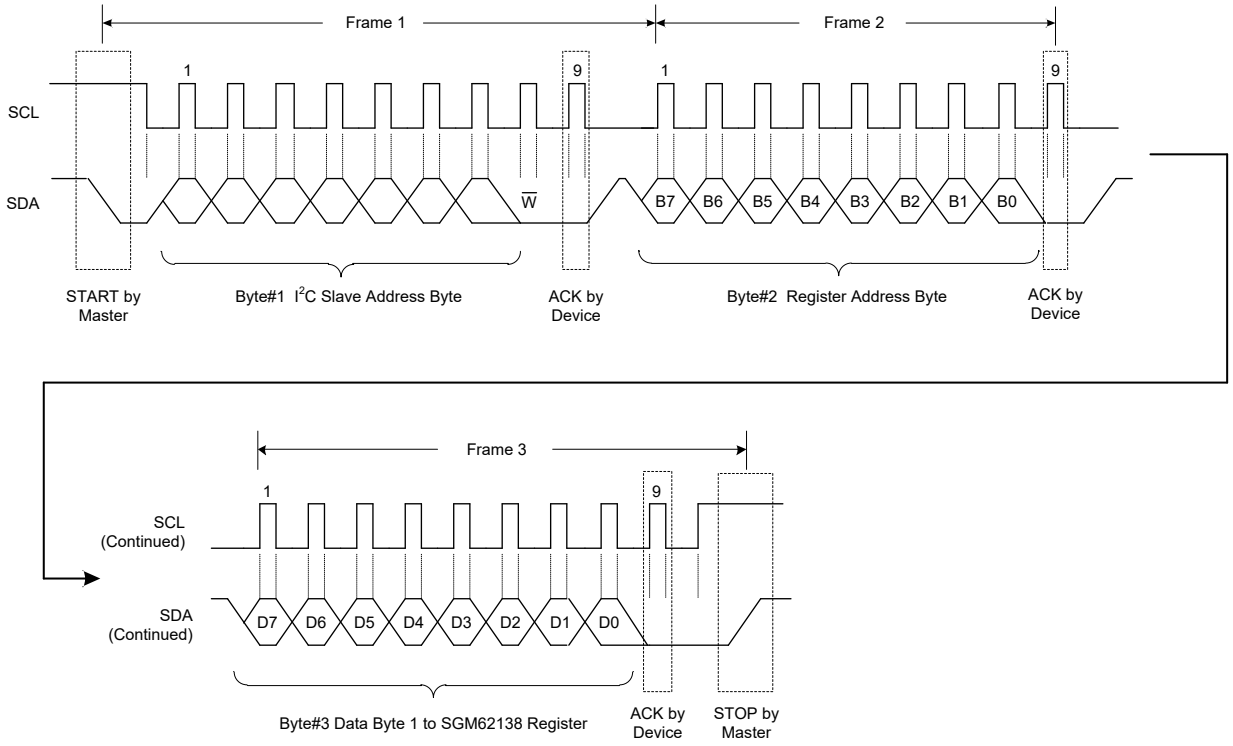


Figure 12. A Single Write Transaction

DETAILED DESCRIPTION (continued)

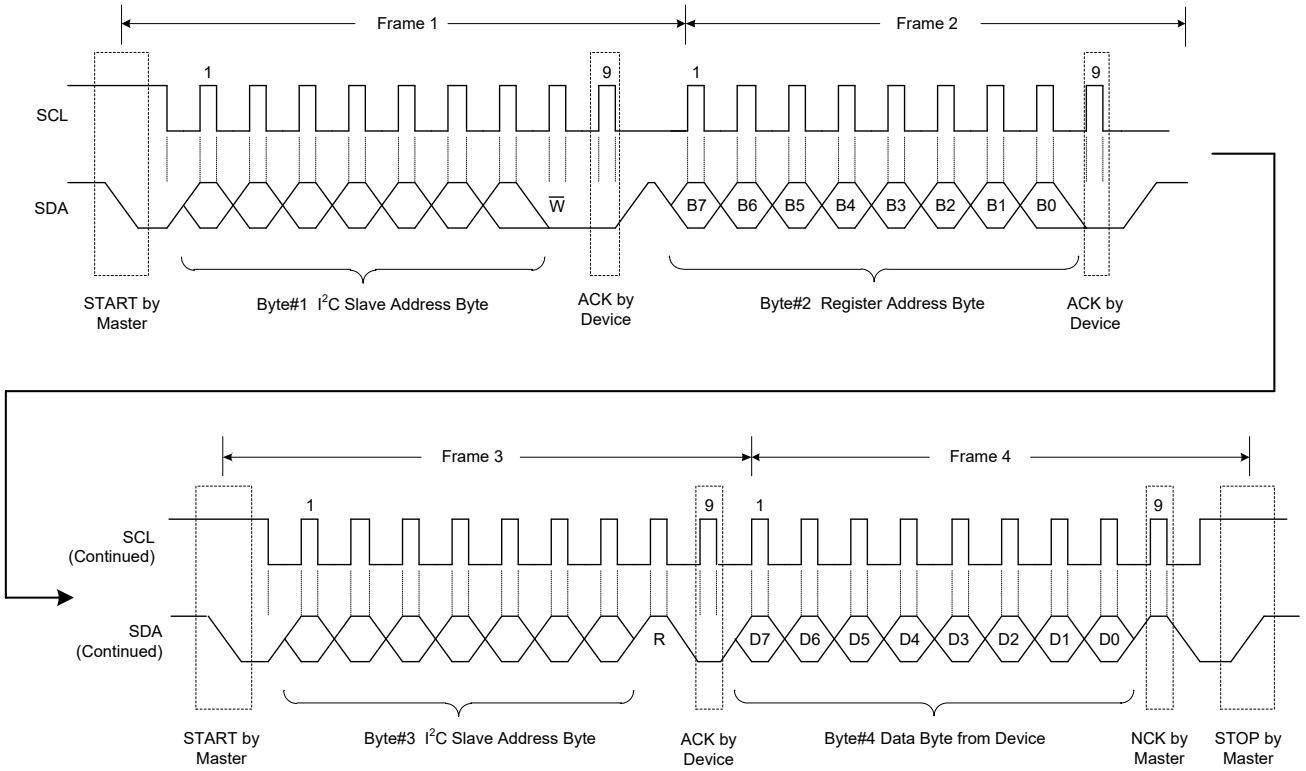


Figure 13. A Single Read Transaction

Multi-Read and Multi-Write

SGM62138 supports multi-read and multi-write. In the multi-write, every new data byte sent by master is written to the next register of the device as shown in Figure 14. A STOP is sent whenever master is done with writing into device registers.

In a multi-read transaction, after receiving the first register data (its address is written to the slave), the master responds with an ACK requesting the slave to send the next register data. The master can continue to do this as long as necessary. After receiving the last byte, the master returns an NCK and issues a STOP condition.

DETAILED DESCRIPTION (continued)

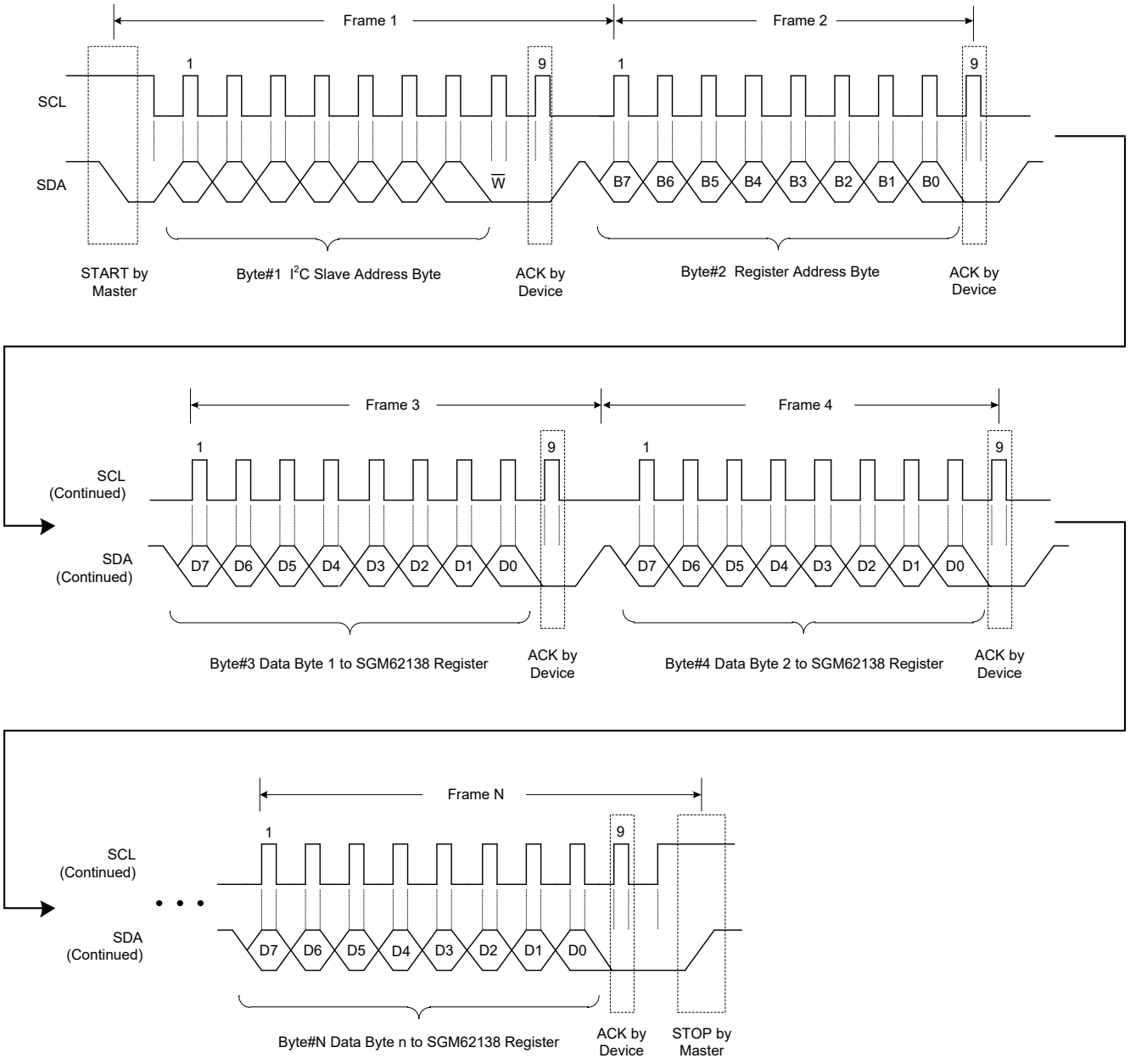


Figure 14. Multi-Write Transaction

DETAILED DESCRIPTION (continued)

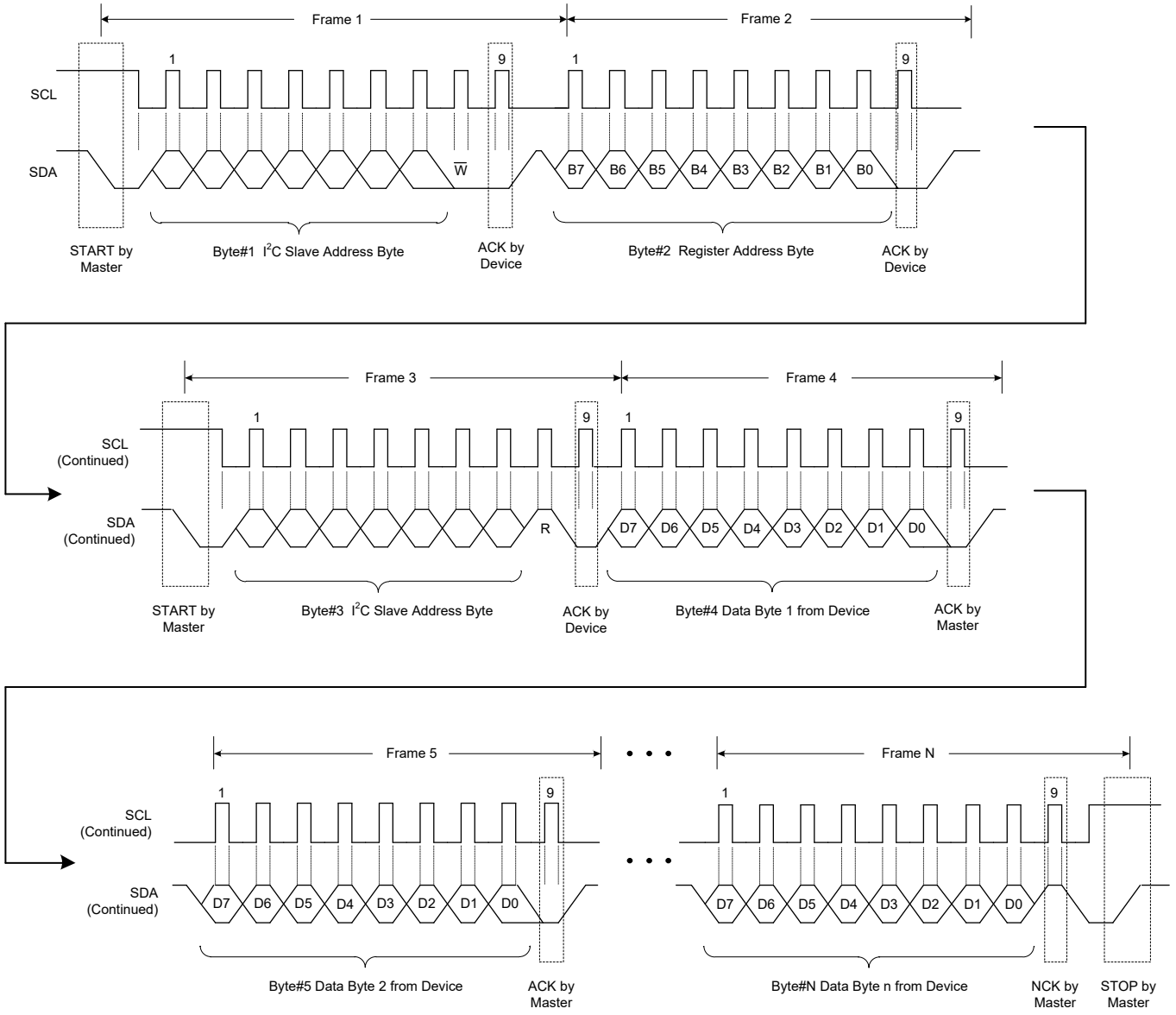


Figure 15. Multi-read

DETAILED DESCRIPTION (continued)

Interrupt

In some unexpected condition, when the monitored event like AC_OK, VIN_SHORT, OTP or EOC is set to 1, or is cleared to 0, the chip sends an interrupt pulse at INT pin to inform MCU. However, if USBDET1 is only set to 1, the chip will send an interrupt pulse. The summary table is shown below.

Table 3. Interrupt Trigger

Status Signal	Interrupt Triggering Mechanism
RESERVED	
AC_OK	Rising/Falling edge triggers INT pulse of 1ms.
USBDET1	Only rising edge triggers INT pulse of 1ms.
RESERVED	
VIN_SHORT	Logic high triggers continuous INT.
OTP	Rising/Falling edge triggers INT pulse of 1ms.
EOC	Rising/Falling edge triggers INT pulse of 1ms.
RESERVED	

Figure 16 shows the interrupt pulse at INT pin.

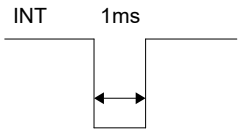


Figure 16. Interrupt Pulse at INT Pin

The USBDET1 bit is read and clear type. Users need to read this bit, and then it will clear to default. In addition to USBDET1, the other bits in the STATUS register represent the real time status. User can be informed of the fault status through the INT pin.

The Mask register is used to mask the interrupt output if it isn't necessary. When the mask register is set, though the corresponding event happens, the chip doesn't send the interrupt at INT pin.

REGISTER MAP

7-bit I^{2}C slave device address: 0b1110 100 + R/W.

I^{2}C Register Address Map

Addr	Register	Type	Default Value @POR	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x00	VOUT_SET	R/W	0b0000 0001	IRCOMP[1:0]		VOUT_SEL	CSEL[1:0]		VCELL_SET[2:0]		
0x01	VINREF_I_SET	R/W	0b0011 0001	VINREF_I_SET[7:0]							
0x02	VINREF_I_SET2	R/W	0b1100 0000	VINREF_I_SET2[1:0]		RESERVED					
0x03	VINREF_E_SET	R/W	0b0111 1100	VINREF_E_SET[7:0]							
0x04	VINREF_E_SET2	R/W	0b1100 0000	VINREF_E_SET2[1:0]		RESERVED					
0x05	IIN_LIM_SET	R/W	0b1111 1111	IIN_LIM_SET[7:0]							
0x06	IOUT_LIM_SET	R/W	0b1111 1111	IOUT_LIM_SET[7:0]							
0x07	VINREG_SET	R/W	0b0010 1100	VINREG _SET[7:0]							
0x08	RATIO	R/W	0b0011 1000	PEAK_OCP_SEL	RESERVED		IOUT_RATIO	IIN_RATIO[1:0]		VOUT_RATIO	VIN_RATIO
0x09	CTRL0_SET	R/W	0b0000 0100	EN_OTG	RESERVED	SCP_RESTART	VINREG_RATIO	FREQ_SET[1:0]		DT_SET	
0x0A	CTRL1_SET	R/W	0b0000 0001	ICHAR_SEL	DIS_TRICKLE	DIS_TERM	FB_SEL	TRICKLE_SET	DIS_OVP	RESERVED	
0x0B	CTRL2_SET	R/W	0b0000 0001	RESERVED	VCC_I_LIM_SET	RESERVED		FACTORY	EN_DITHER	SLEW_SET	
0x0C	CTRL3_SET	R/W	0b0000 0010	EN_USBDV2	EN_USBDV1	AD_START	ILIM_BW_SEL	LOOP_SET	DIS_ShortFoldBack	EOC_SET	EN_PFM
0x0D	VIN_FB_VALUE	R	0b0000 0000	VIN_FB_VALUE[7:0]							
0x0E	VIN_FB_VALUE2	R	0b0000 0000	VIN_FB_VALUE2[1:0]		RESERVED					
0x0F	VOUT_FB_VALUE	R	0b0000 0000	VOUT_FB_VALUE[7:0]							
0x10	VOUT_FB_VALUE2	R	0b0000 0000	VOUT_FB_VALUE2[1:0]		RESERVED					
0x11	IIN_VALUE	R	0b0000 0000	IIN_VALUE[7:0]							
0x12	IIN_VALUE2	R	0b0000 0000	IIN_VALUE2[1:0]		RESERVED					
0x13	IOUT_VALUE	R	0b0000 0000	IOUT_VALUE[7:0]							
0x14	IOUT_VALUE2	R	0b0000 0000	IOUT_VALUE2[1:0]		RESERVED					
0x15	ADC_VALUE	R	0b0000 0000	ADC_VALUE[7:0]							
0x16	ADC_VALUE2	R	0b0000 0000	ADC_VALUE2[1:0]		RESERVED					
0x17	STATUS	RC	0b0000 0000	RESERVED	AC_OK	USBDET1	RESERVED	VIN_SHORT	OTP	EOC	RESERVED
0x18	RESERVED	R	0b0000 0000	RESERVED							
0x19	MASK	R/W	0b0000 0000	RESERVED	AC_OK_Mask	USBDET1_ Mask	RESERVED	VIN_SHORT_ Mask	OTP_Mask	EOC_Mask	RESERVED
0x1A	RESERVED	R/W	0b0000 0000	RESERVED							
0x1B	RESERVED	R/W	0b0000 0000	RESERVED							
0x20	RATIO_SET	R/W	0b0000 0000	CSEL2	VOUT_RATIO2	VIN_RATIO2	VCELL_SET2	VINREG_RATIO2	PEAK_OCP_SET	IVP_SEL	EN_IVP

REGISTER MAP (continued)

REG0x00: VOUT_SET Register Address [reset = 0x01]

BITS	BIT NAME	TYPE	DEFAULT	DESCRIPTION	RESET BY
D[7:6]	IRCOMP[1:0]	R/W	00	Battery I_R Compensation Setting. 00 = 0mΩ (default) 01 = 20mΩ 10 = 40mΩ 11 = 80mΩ Set these bits during PSTOP pin is high.	POR-Reset
D[5]	VOUT_SEL	R/W	0	VOUT Voltage Setting Selection. 0 = internal setting (default) 1 = external setting Set this bit during PSTOP pin is high.	POR-Reset
D[4:3]	CSEL[1:0]	R/W	00	Battery Cell Selection. Only valid for internal VOUT voltage setting. 00 = 1S battery (default) 01 = 2S battery 10 = 3S battery 11 = 4S battery Set these bits during PSTOP pin is high.	POR-Reset
D[2:0]	VCELL_SET[2:0]	R/W	001	Battery Voltage Setting per Cell. Only valid for internal VOUT voltage setting. 000 = 4.1V 001 = 4.2V (default) 010 = 4.25V 011 = 4.3V 100 = 4.35V 101 = 4.4V 110 = 4.45V 111 = 4.5V Set these bits during PSTOP pin is high.	POR-Reset

REG0x01: VINREF_I_SET Register Address [reset = 0x31]

BITS	BIT NAME	TYPE	DEFAULT	DESCRIPTION	RESET BY
D[7:0]	VINREF_I_SET[7:0]	R/W	00110001	Internal VIN Voltage Setting at FB_SEL = 0. Set the high 8-bit of the reference voltage for VIN (total 10-bit programming). The internal reference VIN voltage is calculated as: V_{INREF_I} = (4 × VINREF_I_SET[7:0] + VINREF_I_SET2[1:0] + 1) × 2mV The VIN output voltage is calculated as: V_{IN} = V_{INREF_I} × VIN_RATIO VINREF_I_SET[7:0] range: 0 to 255 00000000 = 0 00000001 = 1 00000010 = 2 …… 00110001 = 49 (default) …… 11111111 = 255 The default reference voltage is (4 × 49 + 3 + 1) × 2mV = 400mV; the default VIN output voltage with FB_SEL = 0 is 400mV × 12.5 = 5V	POR-Reset

REG0x02: VINREF_I_SET2 Register Address [reset = 0xC0]

BITS	BIT NAME	TYPE	DEFAULT	DESCRIPTION	RESET BY
D[7:6]	VINREF_I_SET2[1:0]	R/W	11	Internal VIN Voltage Setting at FB_SEL = 0. Set the low 2-bit of the reference voltage for VIN (total 10-bit programming). The internal reference VIN voltage is calculated as: V_{INREF_I} = (4 × VINREF_I_SET[7:0] + VINREF_I_SET2[1:0] + 1) × 2mV The VIN output voltage is calculated as: V_{IN} = V_{INREF_I} × VIN_RATIO VINREF_I_SET2[1:0] range: 0 to 3 00 = 0 01 = 1 10 = 2 11 = 3 (default)	POR-Reset
D[5:0]	RESERVED	R/W	000000	Internal use. Don't overwrite this bit.	

REGISTER MAP (continued)

REG0x03: VINREF_E_SET Register Address [reset = 0x7C]

BITS	BIT NAME	TYPE	DEFAULT	DESCRIPTION	RESET BY
D[7:0]	VINREF_E_SET[7:0]	R/W	01111100	External VIN Voltage Setting at FB_SEL = 1. Set the high 8-bit of the reference voltage for VIN (total 10-bit programming). The external reference VIN voltage is calculated as: V_{INREF_E} = (4 × VINREF_E_SET[7:0] + VINREF_E_SET2[1:0] + 1) × 2mV The VIN output voltage is calculated as: $V_{IN} = V_{INREF\_E} \times (1+ R_{UP}/R_{DOWN})$ VINREF_E_SET[7:0] range: 0 to 255 00000000 = 0 00000001 = 1 00000010 = 2 …… 01111100 = 124 (default) …… 11111111 = 255 The default reference voltage is (4 × 124 + 3 + 1) × 2mV = 1V	POR-Reset

REG0x04: VINREF_E_SET2 Register Address [reset = 0xC0]

BITS	BIT NAME	TYPE	DEFAULT	DESCRIPTION	RESET BY
D[7:6]	VINREF_E_SET2[1:0]	R/W	11	External VIN Voltage Setting at FB_SEL = 1. Set the low 2-bit of the reference voltage for VIN (total 10-bit programming). The external reference VIN voltage is calculated as: V_{INREF_E} = (4 × VINREF_E_SET[7:0] + VINREF_E_SET2[1:0] + 1) × 2mV The VIN output voltage is calculated as: $V_{IN} = V_{INREF\_E} \times (1+ R_{UP}/R_{DOWN})$ VINREF_E_SET2[1:0] range: 0 to 3 00 = 0 01 = 1 10 = 2 11 = 3 (default)	POR-Reset
D[5:0]	RESERVED	R/W	000000	Internal use. Don't overwrite this bit.	

REG0x05: IIN_LIM_SET Register Address [reset = 0xFF]

BITS	BIT NAME	TYPE	DEFAULT	DESCRIPTION	RESET BY
D[7:0]	IIN_LIM_SET[7:0]	R/W	11111111	I_{IN} Current Limit. Valid in both charging and discharging modes. I_{IN_LIM} (A) = (IIN_LIM_SET[7:0] + 1)/256 × IIN_RATIO × 10mΩ/R_{S1} R_{S1} is the current sense resistor at VIN side. IIN_LIM_SET[7:0] range: 0 to 255 00000000 = 0 00000001 = 1 00000010 = 2 …… 11111111 = 255 (default) E.g., if R_{S1} = 10mΩ, the default I_{IN} current limit is: (255 + 1)/256 × 3 × 10mΩ/10mΩ = 3A, IIN_LIM_SET must be ≥ 300mA	POR-Reset

REG0x06: IOUT_LIM_SET Register Address [reset = 0xFF]

BITS	BIT NAME	TYPE	DEFAULT	DESCRIPTION	RESET BY
D[7:0]	IOUT_LIM_SET[7:0]	R/W	11111111	I_{OUT} Current Limit. Valid in both charging and discharging modes. I_{OUT_LIM} (A) = (IOUT_LIM_SET[7:0] + 1)/256 × IOUT_RATIO × 10mΩ/R_{S2} R_{S2} is the current sense resistor at VOUT side. IOUT_LIM_SET[7:0] range: 0 to 255 00000000 = 0 00000001 = 1 00000010 = 2 …… 11111111 = 255 (default) E.g., if R_{S2} = 10mΩ, the default I_{OUT} current limit is: (255 + 1)/256 × 12 × 10mΩ/10mΩ = 12A, IOUT_LIM_SET must be ≥ 300mA	POR-Reset

REGISTER MAP (continued)

REG0x07: VINREG_SET Register Address [reset = 0x2C]

BITS	BIT NAME	TYPE	DEFAULT	DESCRIPTION	RESET BY
D[7:0]	VINREG_SET[7:0]	R/W	00101100	Set V_{INREG} reference voltage for charging mode. V_{INREG} = (VINREG_SET[7:0] + 1) × VINREG_RATIO (mV) VINREG_SET[7:0] range: 0 to 255 00000000 = 0 00000001 = 1 …… 00101100 = 44 (default) …… 11111111 = 255 Default V_{INREG} voltage is 1.8V, and the valid maximum V_{INREG} voltage is 10.24V when VINREG_RATIO = 1 (40×). Default V_{INREG} voltage is 4.5V, and the valid maximum V_{INREG} voltage is 25.6V when VINREG_RATIO = 1 (100×). Default V_{INREG} voltage is 6.75V, and the valid maximum V_{INREG} voltage is 38.4V when VINREG_RATIO = 1 (150×).	POR-Reset

REG0x08: RATIO Register Address [reset = 0x38]

BITS	BIT NAME	TYPE	DEFAULT	DESCRIPTION	RESET BY
D[7]	PEAK_OCP_SEL	R/W	0	Peak Current Limit Value Setting. 0 = 18A (default) 1 = 22A Set this bit during PSTOP pin is high.	POR-Reset
D[6:5]	RESERVED	R/W	01	Internal use. Don't overwrite this bit.	
D[4]	IOUT_RATIO	R/W	1	I_{OUT_LIM} Setting Ratio. 0 = 6× 1 = 12× (default) Set this bit during PSTOP pin is high.	POR-Reset
D[3:2]	IIN_RATIO[1:0]	R/W	10	I_{IN_LIM} Setting Ratio. 00 = not allowed. 01 = 6× 10 = 3× (default) 11 = not allowed Set these bits during PSTOP pin is high.	POR-Reset
D[1]	VOUT_RATIO	R/W	0	Ratio Setting for VOUT Voltage Monitor. 0 = 12.5× (default) 1 = 5× Use the equation below to calculate the battery voltage monitored through ADC. VOUT = (4 × VOUT_FB_VALUE[7:0] + VOUT_FB_VALUE2[1:0] + 1) × VOUT_RATIO × 2mV VOUT_FB_VALUE[7:0] and VOUT_FB_VALUE2[1:0] are ADC register values. Set this bit to 1 for high accuracy at 1S and 2S battery applications. Set this bit during PSTOP pin is high.	POR-Reset
D[0]	VIN_RATIO	R/W	0	Ratio Setting for VIN voltage, and VIN Voltage Monitor. 0 = 12.5× (default) 1 = 5× Use the equation below to calculate the battery voltage monitored through ADC. VIN = (4 × VIN_FB_VALUE[7:0] + VIN_FB_VALUE2[1:0] + 1) × VIN_RATIO × 2mV VIN_FB_VALUE[7:0] and VIN_FB_VALUE2[1:0] are ADC register values. Set this bit to 1 for high accuracy at V_{IN} < 10.24V. Set this bit during PSTOP pin is high.	POR-Reset

REGISTER MAP (continued)

REG0x09: CTRL0_SET Register Address [reset = 0x04]

BITS	BIT NAME	TYPE	DEFAULT	DESCRIPTION	RESET BY
D[7]	EN_OTG	R/W	0	Enable OTG Operation. 0 = IC works in charging mode (default) 1 = IC works in discharging mode	POR-Reset
D[6]	RESERVED	R/W	0	Internal use. Don't overwrite this bit.	
D[5]	SCP_RESTART	R/W	0	Discharging Mode Output SCP (V_{IN} < 1V) Restart Setting. 0 = Enable SCP restart (default) 1 = Disable SCP restart Set this bit during PSTOP pin is high.	POR-Reset
D[4]	VINREG_RATIO	R/W	0	V_{INREG} Setting Ratio. 0 = 100× (default) 1 = 40× Set this bit to 1 for V_{IN} < 10.24V.	POR-Reset
D[3:2]	FREQ_SET[1:0]	R/W	01	Switching Frequency Setting. 00 = 150kHz 01 = 300kHz (default) 10 = 300kHz 11 = 450kHz Set these bits during PSTOP pin is high.	POR-Reset
D[1:0]	DT_SET[1:0]	R/W	00	Switching Dead Time Setting. 00 = 20ns (default) 01 = 40ns 10 = 60ns 11 = 80ns Set these bits during PSTOP pin is high.	POR-Reset

REG0x0A: CTRL1_SET Register Address [reset = 0x01]

BITS	BIT NAME	TYPE	DEFAULT	DESCRIPTION	RESET BY
D[7]	ICHAR_SEL	R/W	0	Charging Current Selection. 0 = I_{IN} as charging current, the trickle charging current and termination current will be based on I_{IN} (default) 1 = I_{OUT} as charging current, the trickle charging current and termination current will be based on I_{OUT} Set this bit during PSTOP pin is high.	POR-Reset
D[6]	DIS_TRICKLE	R/W	0	Trickle Charge Control. 0 = Enable trickle charge phase (default) 1 = Disable trickle charge phase Set this bit during PSTOP pin is high.	POR-Reset
D[5]	DIS_TERM	R/W	0	Charging Termination Control. 0 = Enable auto-termination (default) 1 = Disable auto-termination Set this bit during PSTOP pin is high.	POR-Reset
D[4]	FB_SEL	R/W	0	VIN Voltage FB Setting. Only valid in discharging mode. 0 = Internal V_{IN} setting, VIN output voltage is set by VIN_RATIO bit and VINREF_I_SET bits (default) 1 = External V_{IN} setting, VIN output voltage is set by resistor divider at FB pin Set this bit during PSTOP pin is high.	POR-Reset
D[3]	TRICKLE_SET	R/W	0	VOUT Threshold Setting for Trickle Charge Phase. 0 = 70% of VOUT voltage setting (default) 1 = 60% of VOUT voltage setting Set this bit during PSTOP pin is high.	POR-Reset
D[2]	DIS_OVP	R/W	0	OVP Protection Setting for Discharging/Charging Mode. 0 = Enable OVP protection (default) 1 = Disable OVP protection	POR-Reset
D[1:0]	RESERVED	R/W	01	Internal use. Don't overwrite this bit.	

REGISTER MAP (continued)

REG0x0B: CTRL2_SET Register Address [reset = 0x01]

BITS	BIT NAME	TYPE	DEFAULT	DESCRIPTION	RESET BY
D[7]	RESERVED	R/W	0	Internal use. Don't overwrite this bit.	
D[6]	VCC_I_LIM_SET	R/W	0	V_{CC} Current Limit Setting. 0 = 160mA (default) 1 = V_{CC} limit is changed with V_{OUT} or V_{IN} (When it is higher than 13V). Set this bit during PSTOP pin is high.	POR-Reset
D[5:4]	RESERVED	R/W	00	Internal use. Don't overwrite this bit.	
D[3]	FACTORY	R/W	0	Factory Setting Bit. MCU shall write this bit to 1 after power up.	POR-Reset
D[2]	EN_DITHER	R/W	0	Enable Switching Frequency Dithering Function at USBDV2/DITHER Pin. 0 = Disable frequency dithering function, USBDV2/DITHER pin is used for PMOS gate control (default) 1 = Enable frequency dithering function, USBDV2/DITHER pin is used for frequency dithering Set this bit during PSTOP pin is high.	POR-Reset
D[1:0]	SLEW_SET[1:0]	R/W	01	Slew Rate Setting for V_{IN} Dynamic Change in Discharging Mode. 00 = 1mV/μs 01 = 2mV/μs (default) 10 = 4mV/μs 11 = 8mV/μs Set these bits during PSTOP pin is high.	POR-Reset

REG0x0C: CTRL3_SET Register Address [reset = 0x02]

BITS	BIT NAME	TYPE	DEFAULT	DESCRIPTION	RESET BY
D[7]	EN_USBDV2	R/W	0	USBDV2 Control. 0 = USBDV2 outputs logic high to turn off PMOS (default) 1 = USBDV2 outputs logic low to turn on PMOS	POR-Reset
D[6]	EN_USBDV1	R/W	0	USBDV1 Control. 0 = Open-drain output (default) 1 = Logic low output	POR-Reset
D[5]	AD_START	R/W	0	ADC Control. 0 = Stop ADC conversion (default) 1 = Start ADC conversion, MCU can monitor the values of voltage or current through ADC registers	POR-Reset
D[4]	ILIM_BW_SEL	R/W	0	I_{LIM} Loop Bandwidth Setting. 0 = 5kHz (default) 1 = 1.25kHz Set this bit during PSTOP pin is high.	POR-Reset
D[3]	LOOP_SET	R/W	0	Loop Response Control. 0 = Normal loop response (default) 1 = Improve the loop response Set this bit during PSTOP pin is high.	POR-Reset
D[2]	DIS_ShortFoldBack	R/W	0	I_{IN} and I_{OUT} Current Fold-Back Setting for VIN Short-Circuit Condition. Only valid in discharging mode. 0 = I_{IN} and I_{OUT} current limit value are fold-back to 20% and 10% of setting value respectively when VIN short-circuit happens (default) 1 = Disable fold-back	POR-Reset
D[1]	EOC_SET	R/W	1	Current Threshold Setting for End of Charging (EOC) Detection. 0 = 1/25 of charging current 1 = 1/10 of charging current (default) Set this bit during PSTOP pin is high.	POR-Reset
D[0]	EN_PFM	R/W	0	PFM Control Under Light Load Condition. Only for discharging mode. 0 = Disable PFM mode (PWM mode enabled) (default) 1 = Enable PFM mode	POR-Reset

REGISTER MAP (continued)

REG0x0D: VIN_FB_VALUE Register Address [reset = 0x00]

BITS	BIT NAME	TYPE	DEFAULT	DESCRIPTION	RESET BY
D[7:0]	VIN_FB_VALUE[7:0]	R	00000000	The High 8-Bit of the ADC Monitor of VIN Voltage (total 10-bit). VIN voltage is calculated as: V_{IN} = (4 × VIN_FB_VALUE[7:0] + VIN_FB_VALUE2[1:0] + 1) × VIN_RATIO × 2mV VIN_FB_VALUE[7:0] range: 0 to 255 00000000 = 0 (default) 00000001 = 1 00000010 = 2 …… 11111111 = 255	POR-Reset

REG0x0E: VIN_FB_VALUE2 Register Address [reset = 0x00]

BITS	BIT NAME	TYPE	DEFAULT	DESCRIPTION	RESET BY
D[7:6]	VIN_FB_VALUE2[1:0]	R	00	The low 2-bit of the ADC monitor of VIN voltage (total 10-bit). VIN voltage is calculated as: V_{IN} = (4 × VIN_FB_VALUE[7:0] + VIN_FB_VALUE2[1:0] + 1) × VIN_RATIO × 2mV VIN_FB_VALUE2[1:0] range: 0 to 3 00 = 0 (default) 01 = 1 10 = 2 11 = 3	POR-Reset
D[5:0]	RESERVED	R	000000	Internal use. Don't overwrite this bit.	

REG0x0F: VOUT_FB_VALUE Register Address [reset = 0x00]

BITS	BIT NAME	TYPE	DEFAULT	DESCRIPTION	RESET BY
D[7:0]	VOUT_FB_VALUE[7:0]	R	00000000	The High 8-Bit of the ADC Monitor of VOUT Voltage (total 10-bit). VOUT voltage is calculated as: V_{OUT} = (4 × VOUT_FB_VALUE[7:0] + VOUT_FB_VALUE2[1:0] + 1) × VOUT_RATIO × 2mV VOUT_FB_VALUE[7:0] range: 0 to 255 00000000 = 0 (default) 00000001 = 1 00000010 = 2 …… 11111111 = 255	POR-Reset

REG0x10: VOUT_FB_VALUE2 Register Address [reset = 0x00]

BITS	BIT NAME	TYPE	DEFAULT	DESCRIPTION	RESET BY
D[7:6]	VOUT_FB_VALUE2[1:0]	R	00	The Low 2-Bit of the ADC Monitor of VOUT Voltage (total 10-bit). VOUT voltage is calculated as: V_{OUT} = (4 × VOUT_FB_VALUE[7:0] + VOUT_FB_VALUE2[1:0] + 1) × VOUT_RATIO × 2mV VOUT_FB_VALUE2[1:0] range: 0 to 3 00 = 0 (default) 01 = 1 10 = 2 11 = 3	POR-Reset
D[5:0]	RESERVED	R	000000	Internal use. Don't overwrite this bit.	

REGISTER MAP (continued)

REG0x11: IIN_VALUE Register Address [reset = 0x00]

BITS	BIT NAME	TYPE	DEFAULT	DESCRIPTION	RESET BY
D[7:0]	IIN_VALUE[7:0]	R	00000000	The High 8-bit of the ADC Monitor of I_{IN} Current (total 10-bit). I_{IN} current is calculated as: I_{IN} (A) = (4 × IIN_VALUE[7:0] + IIN_VALUE2[1:0] + 1) × 2/1200 × IIN_RATIO × 10mΩ/R_{S1} IIN_VALUE[7:0] range: 0 to 255 00000000 = 0 (default) 00000001 = 1 00000010 = 2 …… 11111111 = 255	POR-Reset

REG0x12: IIN_VALUE2 Register Address [reset = 0x00]

BITS	BIT NAME	TYPE	DEFAULT	DESCRIPTION	RESET BY
D[7:6]	IIN_VALUE2[1:0]	R	00	The Low 2-Bit of the ADC Monitor of I_{IN} Current (total 10-bit). I_{IN} current is calculated as: I_{IN} (A) = (4 × IIN_VALUE[7:0] + IIN_VALUE2[1:0] + 1) × 2/1200 × IIN_RATIO × 10mΩ/R_{S1} IIN_VALUE2[1:0] range: 0 to 3 00 = 0 (default) 01 = 1 10 = 2 11 = 3	POR-Reset
D[5:0]	RESERVED	R	000000	Internal use. Don't overwrite this bit.	

REG0x13: IOUT_VALUE Register Address [reset = 0x00]

BITS	BIT NAME	TYPE	DEFAULT	DESCRIPTION	RESET BY
D[7:0]	IOUT_VALUE[7:0]	R	00000000	The High 8-Bit of the ADC Monitor of I_{OUT} Current (total 10-bit). I_{OUT} current is calculated as: I_{OUT} (A) = (4 × IOUT_VALUE[7:0] + IOUT_VALUE2[1:0] + 1) × 2/1200 × IOUT_RATIO × 10mΩ/R_{S2} IOUT_VALUE[7:0] range: 0 to 255 00000000 = 0 (default) 00000001 = 1 00000010 = 2 …… 11111111 = 255	POR-Reset

REG0x14: IOUT_VALUE2 Register Address [reset = 0x00]

BITS	BIT NAME	TYPE	DEFAULT	DESCRIPTION	RESET BY
D[7:6]	IOUT_VALUE2[1:0]	R	00	The Low 2-Bit of the ADC Monitor of I_{OUT} Current (total 10-bit). I_{OUT} current is calculated as: I_{OUT} (A) = (4 × IOUT_VALUE[7:0] + IOUT_VALUE2[1:0] + 1) × 2/1200 × IOUT_RATIO × 10mΩ/R_{S2} IOUT_VALUE2[1:0] range: 0 to 3 00 = 0 (default) 01 = 1 10 = 2 11 = 3	POR-Reset
D[5:0]	RESERVED	R	000000	Internal use. Don't overwrite this bit.	

REGISTER MAP (continued)

REG0x15: ADC_VALUE Register Address [reset = 0x00]

BITS	BIT NAME	TYPE	DEFAULT	DESCRIPTION	RESET BY
D[7:0]	ADC_VALUE[7:0]	R	00000000	The High 8-Bit of the ADC Monitor of ADC Voltage (total 10-bit). ADC voltage is calculated as: V_{ADC} = (4 × ADC_VALUE[7:0] + ADC_VALUE2[1:0] + 1) × 2mV ADC_VALUE[7:0] range: 0 to 255 00000000 = 0 (default) 00000001 = 1 00000010 = 2 …… 11111111 = 255	POR-Reset

REG0x16: ADC_VALUE2 Register Address [reset = 0x00]

BITS	BIT NAME	TYPE	DEFAULT	DESCRIPTION	RESET BY
D[7:6]	ADC_VALUE2[1:0]	R	00	The Low 2-bit of the ADC Monitor of ADC Voltage (total 10-bit). ADC voltage is calculated as: V_{ADC} = (4 × ADC_VALUE[7:0] + ADC_VALUE2[1:0] + 1) × 2mV ADC_VALUE2[1:0] range: 0 to 3 00 = 0 (default) 01 = 1 10 = 2 11 = 3	POR-Reset
D[5:0]	RESERVED	R	000000	Internal use. Don't overwrite this bit.	

REG0x17: STATUS Register Address [reset = 0x00]

BITS	BIT NAME	TYPE	DEFAULT	DESCRIPTION	RESET BY
D[7]	RESERVED	R	0	Internal use. Don't overwrite this bit.	
D[6]	AC_OK	R	0	1 = AC adapter is inserted	POR-Reset
D[5]	USBDET1	RC	0	1 = USB-A load insert is detected at USBDET1 pin	POR-Reset or Read-Reset
D[4]	RESERVED	R	0	Internal use. Don't overwrite this bit.	
D[3]	VIN_SHORT	R	0	1 = VIN short-circuit fault happens in discharging mode	POR-Reset
D[2]	OTP	R	0	1 = OTP fault happens	POR-Reset
D[1]	EOC	R	0	1 = EOC conditions are satisfied	POR-Reset
D[0]	RESERVED	R	0	Internal use. Don't overwrite this bit.	

REG0x19: MASK Register Address [reset = 0x00]

BITS	BIT NAME	TYPE	DEFAULT	DESCRIPTION	RESET BY
D[7]	RESERVED	R/W	0	Internal use. Don't overwrite this bit.	
D[6]	AC_OK_Mask	R/W	0	1 = Interrupt is disabled	POR-Reset
D[5]	USBDET1_Mask	R/W	0	1 = Interrupt is disabled	POR-Reset
D[4]	RESERVED	R/W	0	Internal use. Don't overwrite this bit.	
D[3]	VIN_SHORT_Mask	R/W	0	1 = Interrupt is disabled	POR-Reset
D[2]	OTP_Mask	R/W	0	1 = Interrupt is disabled	POR-Reset
D[1]	EOC_Mask	R/W	0	1 = Interrupt is disabled	POR-Reset
D[0]	RESERVED	R/W	0	Internal use. Write this bit to 1 after power up.	

REGISTER MAP (continued)

REG0x20: RATIO_SET Register Address [reset = 0x00]

BITS	BIT NAME	TYPE	DEFAULT	DESCRIPTION	RESET BY
D[7]	CSEL2	R/W	0	Add Battery Cell Selection Bit. It could be set up to 8S battery. 0 = REG0x00 D[4:3] (default) 1 = REG0x00 D[4:3] + 4S battery, for ≥ 5S battery. Set this bit during PSTOP pin is high.	POR-Reset
D[6]	VOUT_RATIO2	R/W	0	Add 1-bit Ratio Setting for VOUT Voltage Monitor and Setting. 0 = REG0x08 D[1] (default) 1 = 18.75x Use the equation below to calculate the battery voltage monitored through ADC. VOUT = (4 × VOUT_FB_VALUE[7:0] + VOUT_FB_VALUE2[1:0] + 1) × VOUT_RATIO2 × 2mV VOUT_FB_VALUE[7:0] and VOUT_FB_VALUE2[1:0] are ADC register values. For 6S to 8S battery applications (V_{OUT} > 25.6V), set this bit to 1. Set this bit during PSTOP pin is high.	POR-Reset
D[5]	VIN_RATIO2	R/W	0	Add 1-bit ratio Setting for VIN Voltage Monitor and Setting. 0 = REG0x08 D[0] (default) 1 = 18.75x Use the equation below to calculate the battery voltage monitored through ADC. VIN = (4 × VIN_FB_VALUE[7:0] + VIN_FB_VALUE2[1:0] + 1) × VIN_RATIO2 × 2mV VIN_FB_VALUE[7:0] and VIN_FB_VALUE2[1:0] are ADC register values. For VIN > 25.6V, set this bit to 1. Set this bit during PSTOP pin is high.	POR-Reset
D[4]	VCELL_SET2	R/W	0	Add Battery Voltage Setting per Cell. Only valid for internal VOUT voltage setting, 25mV/step. (REG0x00 D[2:0] + REG0x20 D[4]) 0001 = 3.65V 0011 = 4.05V 0000 = 4.1V 0101 = 4.175V 0010 = 4.2V (default) 0111 = 4.225V 0100 = 4.25V 0110 = 4.3V 1001 = 4.325V 1000 = 4.35V 1011 = 4.375V 1010 = 4.4V 1101 = 4.425V 1100 = 4.45V 1110 = 4.5V 1111 = 4.55V Set this bit during PSTOP pin is high.	POR-Reset
D[3]	VINREG_RATIO2	R/W	0	Program V_{INREG} Ratio Setting. 0 = REG0x09 D[4] (default) 1 = 150x Set this bit during PSTOP pin is high.	POR-Reset
D[2]	PEAK_OCP_SET	R/W	0	For Peak Current Protection Setting. 0 = Enable peak current limit (default) 1 = Disable peak current limit Set this bit during PSTOP pin is high.	POR-Reset
D[1]	IVP_SEL	R/W	0	IVP Threshold at VIN Pin Setting 0 = 40V (default) 1 = 30V Set this bit during PSTOP pin is high.	POR-Reset
D[0]	EN_IVP	R/W	0	IVP Function at VIN Pin Setting 0 = Disable (default) 1 = Enable Set this bit during PSTOP pin is high.	POR-Reset

APPLICATION INFORMATION

Capacitor Selection

The switching frequency of the chip ranges from 150kHz to 450kHz. Given the excellent high-frequency filtering performance and low equivalent series resistance (ESR) of MLCC ceramic capacitors, the use of X5R or X7R grade capacitors with a capacitance of 60μF or higher is recommended. In addition, the voltage rating of these capacitors should exceed the operating voltage by a suitable safety margin. For instance, a capacitor with a minimum voltage rating of 16V should be selected for a maximum operating voltage (V_{IN}/V_{OUT}) of 12V; for a sufficient safety margin, a 25V-rated capacitor is recommended instead.

High-capacitance polymer or tantalum capacitors can be used for both input and output, but their voltage rating must exceed the maximum operating voltage by an adequate margin. However, these capacitors do not offer the same high-frequency performance as ceramic capacitors. For this reason, it is advisable to place at least a 10μF ceramic capacitor in parallel to reduce high-frequency ripple.

Inductor Selection

A 2.2μH to 10μH inductor is recommended for loop stability.

The peak inductor current in discharging mode is calculated as follows:

When $V_{IN} \geq V_{OUT}$,

$$I_{L\_PEAK} = I_{OUT} + \frac{V_{OUT} \times (V_{IN} - V_{OUT} \times \eta)}{2 \times f_{SW} \times L \times V_{IN}} \quad (5)$$

When $V_{IN} < V_{OUT}$,

$$I_{L\_PEAK} = I_{IN} + \frac{V_{IN} \times (V_{OUT} - V_{IN})}{2 \times f_{SW} \times L \times V_{OUT} \times \eta} \quad (6)$$

Where I_{OUT} is the battery current on the VOUT side, and is calculated as follows:

$$I_{OUT} = \frac{V_{IN} \times I_{IN}}{V_{OUT} \times \eta} \quad (7)$$

η represents the power conversion efficiency. A value of 90% is recommended for calculation purposes. f_{SW} denotes the switching frequency. And L refers to the inductor value.

The peak inductor current in charging mode is calculated as follows:

When $V_{IN} \geq V_{OUT}$,

$$I_{L\_PEAK} = I_{OUT} + \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{2 \times f_{SW} \times L \times V_{IN} \times \eta} \quad (8)$$

When $V_{IN} < V_{OUT}$,

$$I_{L\_PEAK} = I_{IN} + \frac{V_{IN} \times (V_{OUT} - V_{IN} \times \eta)}{2 \times f_{SW} \times L \times V_{OUT}} \quad (9)$$

Where, I_{OUT} is the battery current on the VOUT side, and is calculated as follows:

$$I_{OUT} = \frac{V_{IN} \times I_{IN} \times \eta}{V_{OUT}} \quad (10)$$

η represents the power conversion efficiency. A value of 90% is recommended for calculation purposes. f_{SW} denotes the switching frequency. And L refers to the inductor value.

When selecting an inductor, saturation current of the component must exceed peak inductor current by a sufficient margin, with a 20% margin recommended. Rated current of inductors must be higher than battery current.

DC resistance (DCR) of inductors contributes to conduction losses in switching regulators, thus making low-DCR inductors a recommended option, especially for high-power applications. Conduction loss of inductors can be approximated by the following formula:

$$P_{L\_DC} = I_L^2 \times DCR \quad (11)$$

I_L represents the average value of inductor current, and it equals to I_{OUT} or I_{IN}.

In addition to DC power loss, inductors generate AC winding loss and core loss, both correlated with peak current of inductors. Generally, higher peak current results in increased AC winding and core loss. Users are advised to consult inductor manufacturers for selecting components with low ESR at high frequencies and minimal core loss.

Current Sense Resistor

R_{S1} and R_{S2} are current sense resistors. A 10mΩ should be used for R_{S1} to sense I_{IN} current, while R_{S2} (for IOUT current sensing) can use either 5mΩ or 10mΩ resistors. The 10mΩ resistor offers higher battery current limit accuracy, while 5mΩ resistor provides higher efficiency. Resistors with 1% or better accuracy and a low temperature coefficient are recommended.

APPLICATION INFORMATION (continued)

Note that for alternative resistor values, please contact the factory for support.

Power rating and temperature coefficient of resistors should be taken into account. Power dissipation can be approximated by the formula $P = I^2R$, where I represents the maximum current passing through a resistor. Power rating of resistors must exceed this calculated value.

Resistor values typically vary with increasing temperature, with the degree of variation determined by the temperature coefficient. For applications requiring high current limit accuracy, select resistors with the lowest possible temperature coefficient.

Current-Sense Filter Resistor Selection

It is recommended to add an RC filter network (2.2Ω + 22nF + 2.2Ω) between the CC+/ISNS+ and CC-/ISNS- pins, and place the filter as close to the chip as possible. For Buck mode applications with high input voltage and low output current — especially at 50% duty cycle — the external filter resistance may be increased (e.g., to 20Ω) to improve negative current sensing performance.

MOSFET Selection

The V_{DS} rating of all MOSFETs should exceed the maximum operating voltage by a sufficient margin, preferably more than 10V higher. For instance, a MOSFET with a minimum V_{DS} rating of 30V is recommended for a 20V maximum operating voltage, and a 40V V_{DS} rating for a 24V maximum operating voltage.

V_{GS} voltage rating of MOSFETs should exceed 8V. During operation, PCB parasitic parameters can induce transient overshoots that may cause V_{GS} voltage of MOSFETs to exceed VDRV voltage. A 10V V_{GS} rating is therefore recommended to ensure sufficient margin.

Drain current (I_D) of MOSFETs should exceed maximum battery current by a sufficient margin.

To ensure sufficient current handling capability in relatively high-temperature environments, consider the current rating at T_A = +70℃ or T_C = +100℃. Additionally, the power dissipation rating (PD) should be considered — higher PD is preferable for most applications. Ensure that power consumption of MOSFETs does not exceed the PD rating of the device.

On-resistance ($R_{DS(ON)}$) and input capacitance (C_{ISS}) of MOSFETs directly impact power efficiency. Typically, MOSFETs with lower $R_{DS(ON)}$ feature higher C_{ISS}. $R_{DS(ON)}$ is associated with conduction loss — higher $R_{DS(ON)}$ leads to greater conduction loss, resulting in lower efficiency and increased thermal dissipation. C_{ISS} affects MOSFET switching times; longer switching times increase switching loss and reduce efficiency. Select an appropriate MOSFET based on the tradeoff between $R_{DS(ON)}$ and C_{ISS}.

If a MOSFET with high C_{ISS} is selected, switching time will be prolonged; the dead time should therefore be adjusted to prevent simultaneous turn-on of the high-side and low-side MOSFETs.

Driver Resistor and SW Snubber Circuit

For EMI debugging purposes, series resistors (0603 package) are recommended to be added to the gate drive signals — HG1, LG1, LG2 and HG2 to the MOSFET gates — with RC snubber circuits (0603 package) also implemented at each SWx node. This configuration adjusts MOSFET switching times and suppresses switching overshoot, as illustrated below.

Gate drive resistors should be placed in close proximity to the MOSFETs. Begin with 0Ω resistors, in the event of significant switching overshoot, increase the resistor value to reduce switching speed. The resistor value is ideally kept below 10Ω. As switching speed decreases, the default dead time may be insufficient to suppress overshoot in the power MOSFETs. Where a resistor value above 10Ω is required, users should increase the dead time accordingly.

RC snubber circuits at the SWx nodes also serve to absorb high-frequency voltage spikes at these nodes, thereby enhancing EMC performance. RC components may be left unpopulated initially; their values can be adjusted to optimize EMC performance as required. A typical starting value for snubber components is 2.2Ω in series with 1nF. For further EMC enhancement, reduce the resistance value (e.g., to 1Ω or lower) and increase the capacitance value (e.g., to 2.2nF or higher).

APPLICATION INFORMATION (continued)

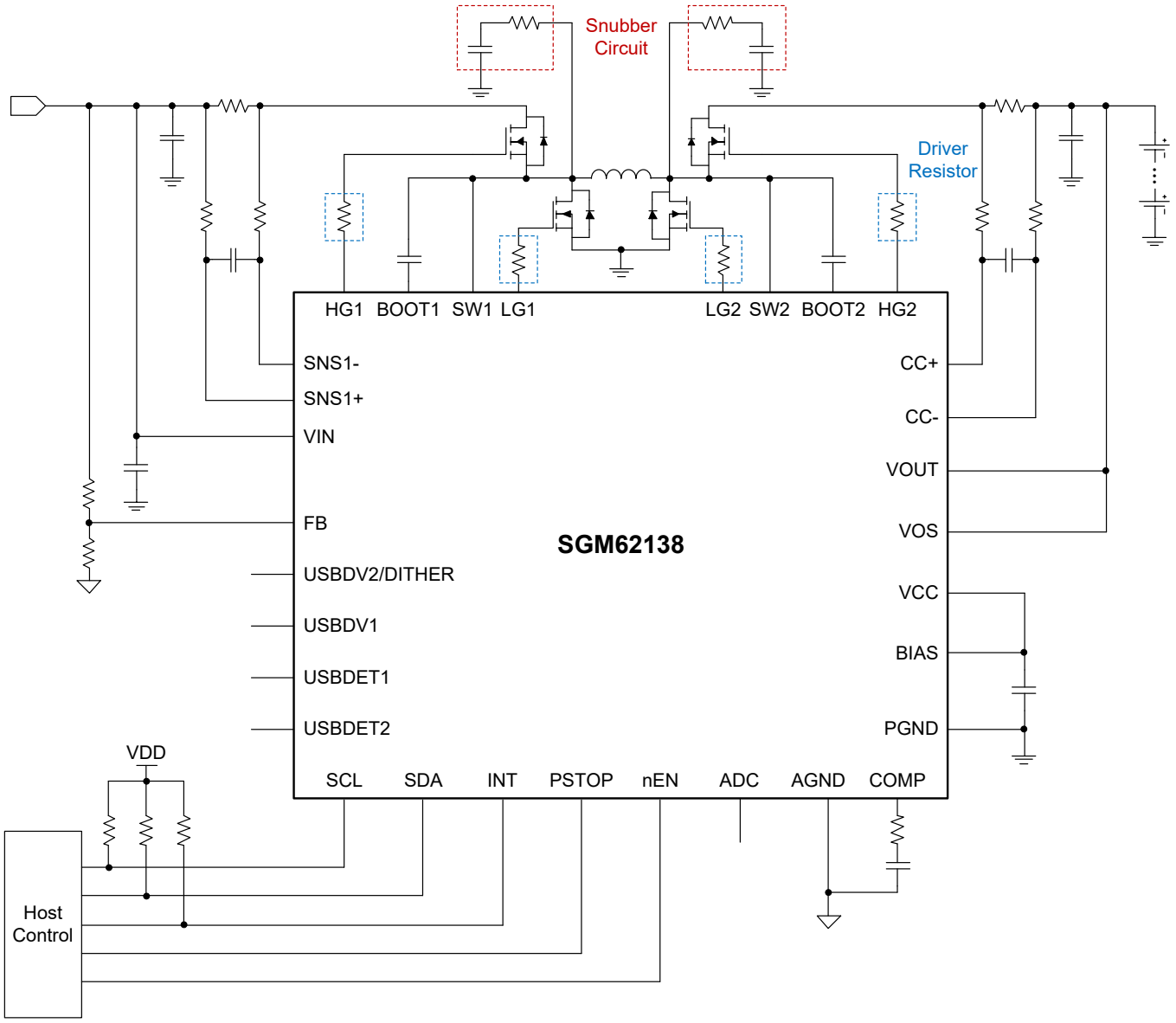


Figure 17. Driver Resistor and Snubber Circuit

LAYOUT GUIDE

1. The 1μF capacitors connected to the VIN/VOUT/VCC/BIAS pins should be placed close to the chip, with their ground connection to the ground pins as short as possible.

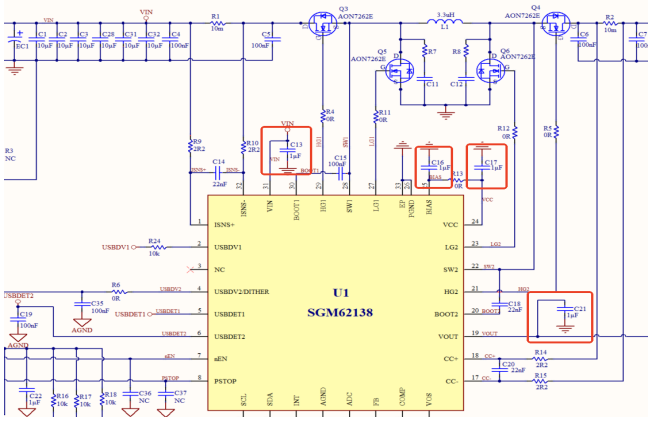


Figure 18. Component(s) on Schematic

Layout Example: Place the four capacitors close to the chip on the top layer. Connect the capacitors to their respective pins on the same layer, and route their ground connections directly.

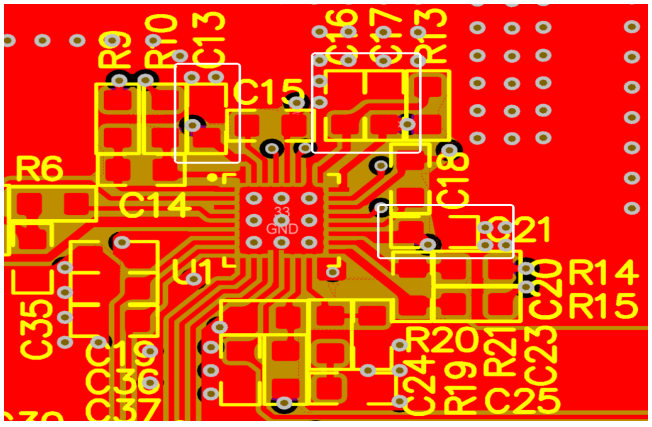


Figure 19. Top Layer View

2. Place the IIN current sense resistor, MOSFETs, and bulk capacitor on the VIN side together as close as possible. The low-side MOSFET and bulk capacitors should be positioned very close to the PGND pins. Add a 100nF capacitor between the current sense resistor and high-side MOSFET, connecting it to PGND. This helps suppress high-frequency noise and should be placed very close to the MOSFET and PGND pins.

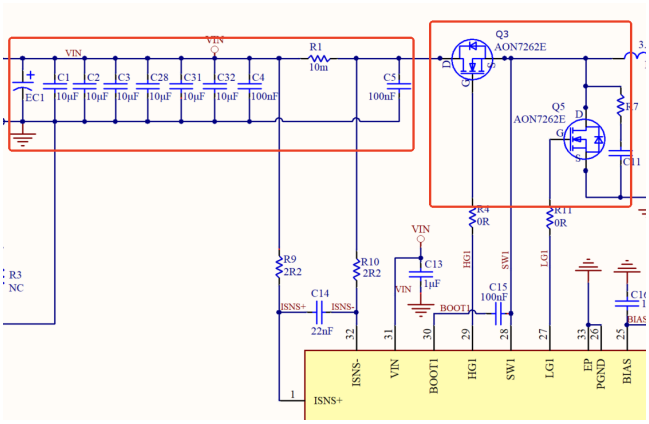


Figure 20. Component(s) on Schematic

Layout Example: Place all these components as a single group on the top layer. The VIN and PGND power traces should be routed as wide as possible. The low-side MOSFET, 100nF capacitor, and bulk capacitors should connect to the PGND pins via ground pours on both the top and bottom layers.

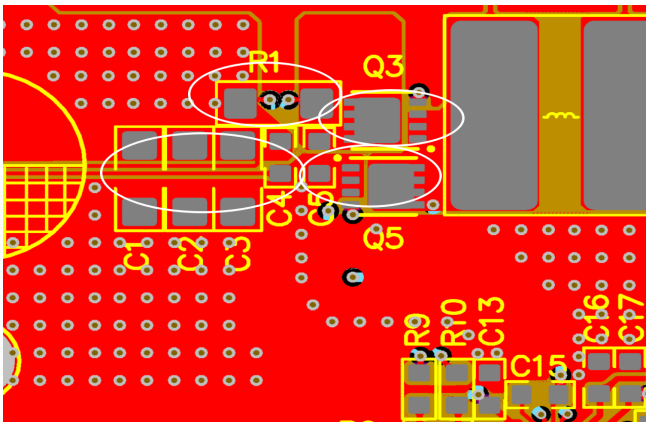


Figure 21. Top Layer View

LAYOUT GUIDE (continued)

3. Place the IOUT current sense resistor, MOSFETs, and bulk capacitor on the VOUT side together as close as possible. The low-side MOSFET and bulk capacitors should be positioned very close to the PGND pins. Add a 100nF capacitor between the current sense resistor and high-side MOSFET, connecting it to PGND. This helps suppress high-frequency noise and should be placed very close to the MOSFET and PGND pins.

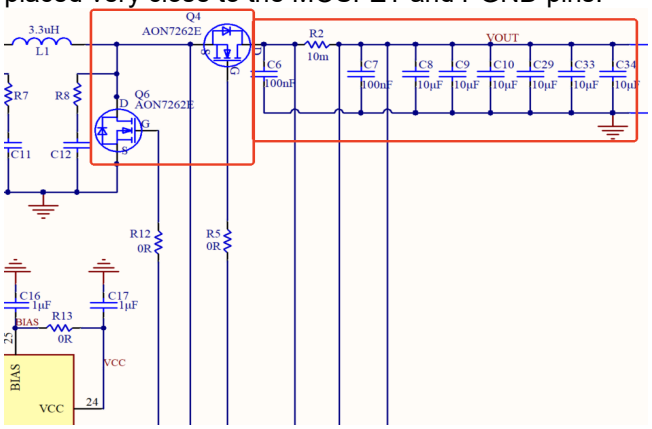


Figure 22. Component(s) on Schematic

Layout Example: Place all these components as a single group on the top layer. The VOUT and PGND power traces should be routed as wide as possible. The low-side MOSFET, 100nF capacitor, and bulk capacitors should connect to the PGND pins via ground pours on both the top and bottom layers.

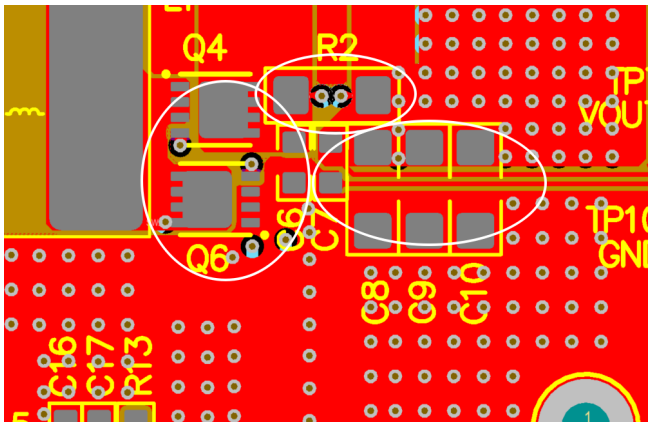


Figure 23. Top Layer View

4. The driver signals (LG1/HG1/SW1/SW2/LG2/HG2) shown below should be routed with wide traces (≥ 15mil). Driver resistors should be placed close to the MOSFETs. HGx and SWx traces should be routed in parallel and close together, while LGx traces should be routed in parallel with PGND traces (≥ 15mil) or placed close to PGND pours. A wide PGND-filled gap should be maintained between LGx and HGx, and sufficient spacing should be kept between LGx and SWx to prevent interference.

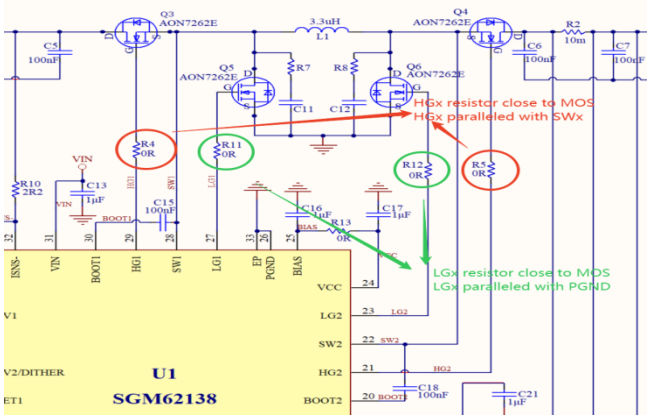


Figure 24. Component(s) on Schematic

5. The current sense traces should connect to the current sense resistor pads using the Kelvin sensing method as shown below. They should be routed in parallel (differential routing), with a filter added near the IC for each current sense path.

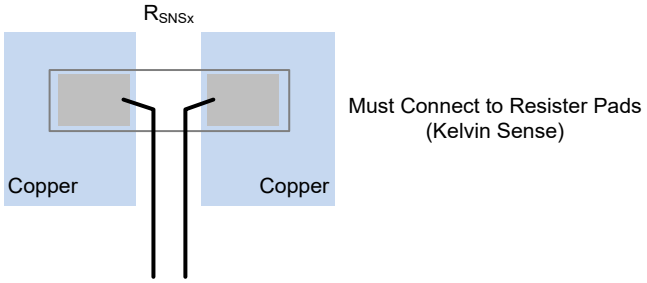


Figure 25. Current sense (Kelvin Sense)

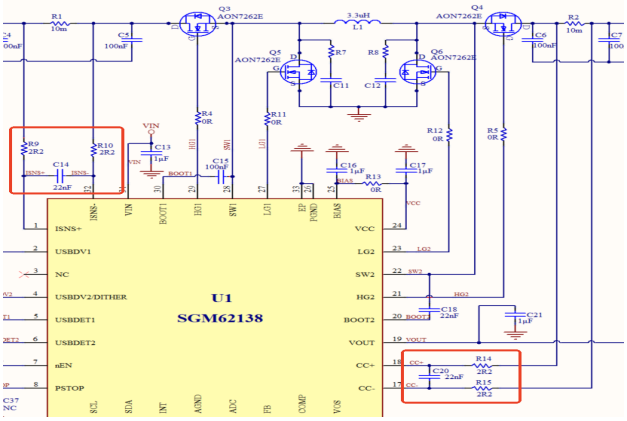


Figure 26. Component(s) on Schematic

LAYOUT GUIDE (continued)

Layout Example: Current-sense resistors R_1 and R_2 should be placed close to the power MOSFETs, so they may be located some distance away from the chip. The sense filter should be located near the chip. The traces can be routed on another layer (3rd layer in this example) but must be routed in parallel (differentially), kept well away from switching signals, and isolated with PGND pours.

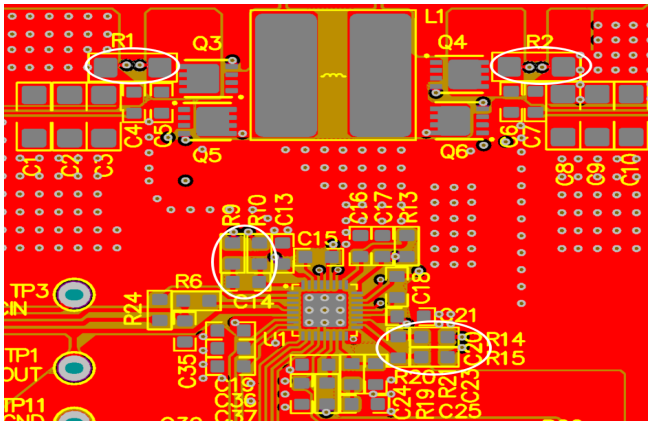


Figure 27. Top Layer View

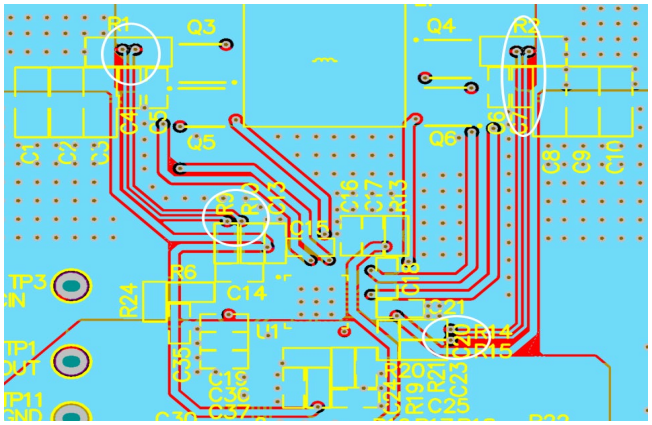


Figure 28. Middle-2 Layer View

6. Analog signal components (e.g., FB resistor dividers, COMP pin components, etc.) should be placed in close proximity to the chip and connected directly to the AGND (analog ground) pin. Next, the AGND pin and all PGNDs should be tied together at the PGND pad located beneath the chip. To boost thermal dissipation, vias should be added to the PGND pad.

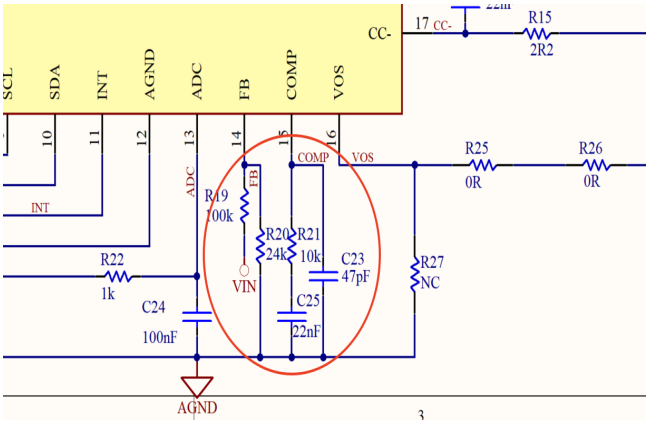


Figure 29. Component(s) on Schematic

Layout Example: Analog components should be placed close to the chip, with AGND connected to PGND at the PGND pad.

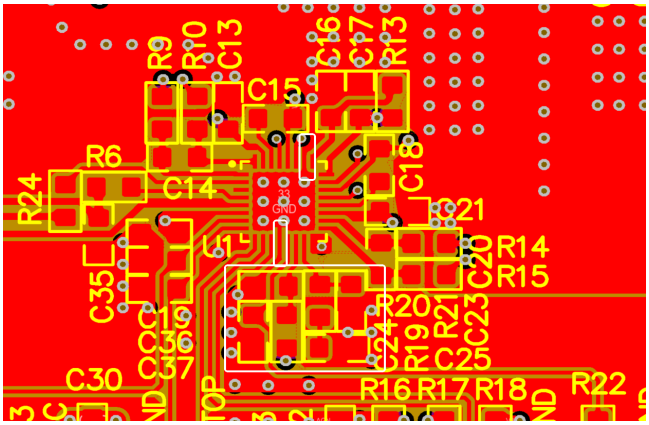


Figure 30. Top Layer View

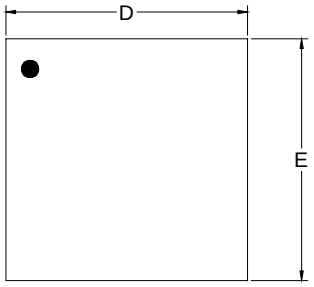
REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

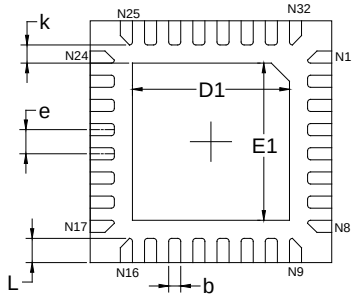
Changes from Original to REV.A (MAY 2026)	Page
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

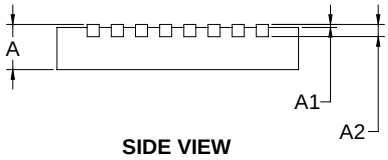
TQFN-4×4-32L



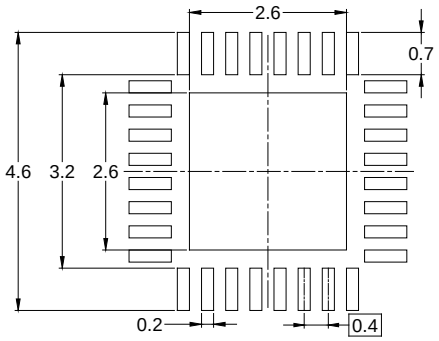
TOP VIEW



BOTTOM VIEW



SIDE VIEW



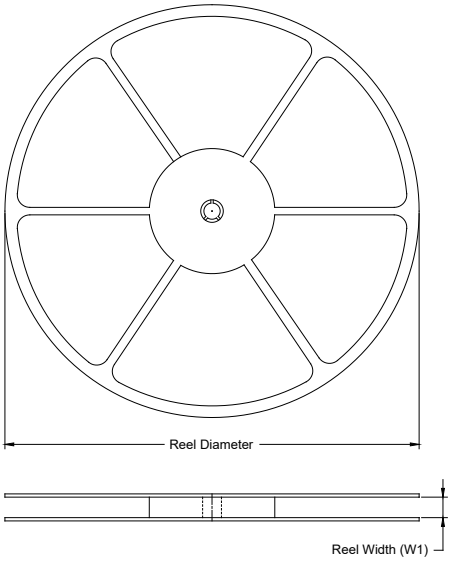
RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A2	0.203 REF		0.008 REF	
D	3.900	4.100	0.154	0.161
D1	2.500	2.700	0.098	0.106
E	3.900	4.100	0.154	0.161
E1	2.500	2.700	0.098	0.106
k	0.300 REF		0.012 REF	
b	0.150	0.250	0.006	0.010
L	0.300	0.500	0.012	0.020
e	0.400 BSC		0.016 BSC	

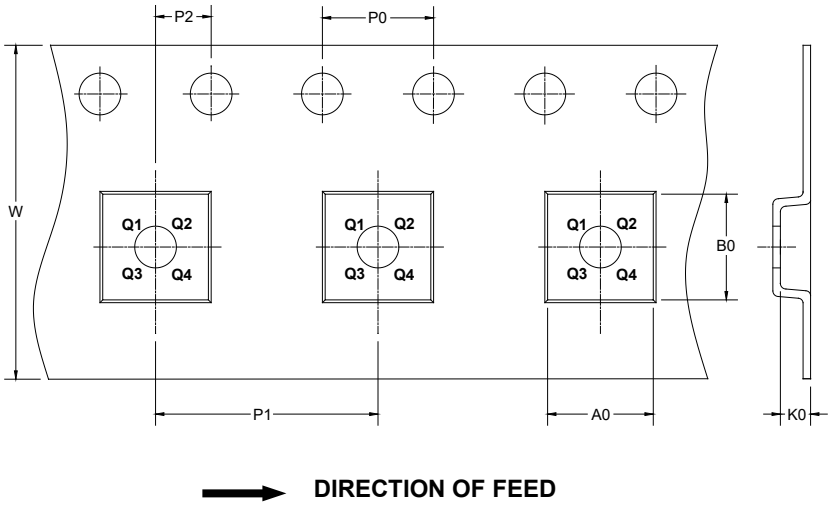
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



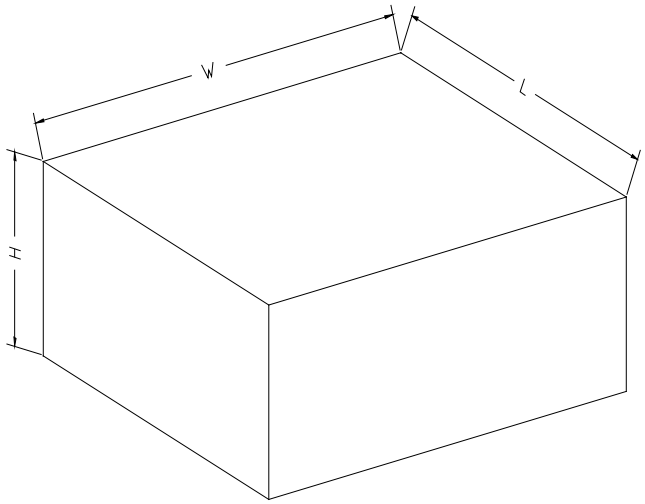
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TQFN-4×4-32L	13″	12.4	4.30	4.30	1.10	4.0	8.0	2.0	12.0	Q2

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002