SGM41526A/SGM41527A
1.6MHz Synchronous Li-Ion and Li-Polymer Stand-Alone Battery Chargers with Automatic Power Path Selector

FEATURES

- 4A Synchronous 1.6MHz PWM Charger
  - Cycle-by-Cycle Current Limit
  - Integrated 24V Switching MOSFETs
  - Integrated Bootstrap Diode
  - Digital Soft-Start
- Up to 95.2% Charge Efficiency
- 30V Absolute Maximum Input Voltage Rating with Adjustable Over-Voltage Threshold
- 4.5V to 22V Input Operating Voltage Range
- Automatic Power Path Selector (Battery/Adapter)
- Dynamic Power Management (DPM)
- Battery Charge Voltage
  - SGM41526A: Select 2-, 3-, or 4-Cell with 4.2V/Cell
  - SGM41527A: Adjustable Charge Voltage
- 18μA Battery Current (No Adapter)
- 1.3mA Input Current (Charge Disabled)
- High Accuracy
  - ±0.4% Charge Voltage Regulation
  - ±5% Charge Current Regulation
  - ±4% Input Current Regulation
- Safety
  - Thermal Regulation (Current Limit for T_J = +120℃)
  - Thermal Shutdown
  - Battery Thermistor Sense Hot/Cold Charge Suspend
  - Input Under-Voltage Lockout (UVLO)
  - Input Over-Voltage (ACOV) Protection

APPLICATIONS

Tablet PCs
Portable Terminals and Printers
Portable Medical Equipment
Battery Backup Systems

TYPICAL APPLICATION

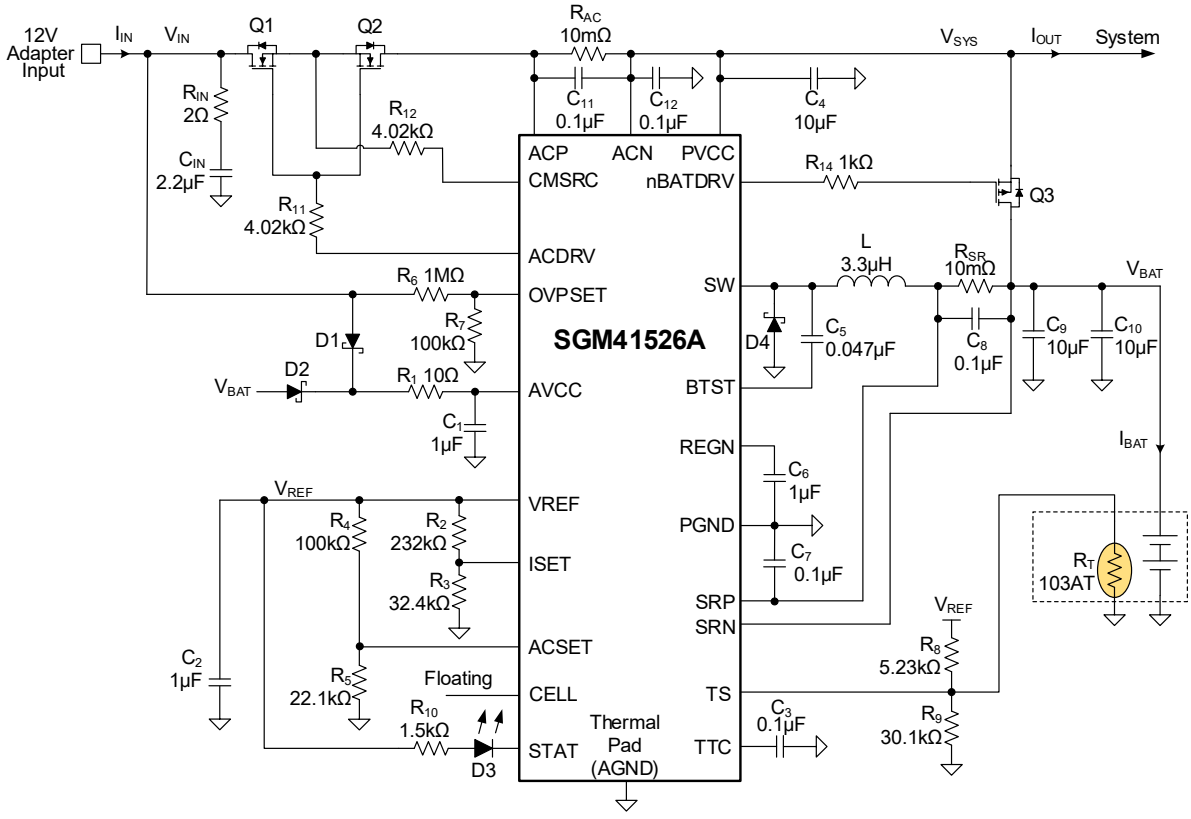


Figure 1. SGM41526A Typical Application Circuit (with a 2-Cell Battery)

GENERAL DESCRIPTION

The SGM41526A and SGM41527A are stand-alone Li-Ion and Li-polymer battery chargers. The PWM switches are integrated inside and they can automatically select the power path. They also include gate drivers for external power path selector MOSFETs. The synchronous PWM controller runs at a fixed frequency (1.6MHz) and is capable of providing accurate regulation of charge voltage, charge current and input current. They are capable of providing continuous battery pack temperature monitoring in which the charge is only allowed when the temperature is within the desired range. The SGM41526A can charge 2-, 3- or 4-cell (selected by CELL pin); while the SGM41527A has an adjustable charge voltage for up to 4 cells. In the SGM41527A, the FB pin is used for charge voltage regulation (feedback) using an internal 2.1V reference and comparator.

Typically, a full battery charging cycle has three consequent phases: pre-conditioning, constant current and constant voltage. The charge current is small during the pre-conditioning phase in which battery is heavily depleted. When the battery voltage exceeds a threshold voltage, the charge current increases to its maximum (fast charge current) until the battery voltage reaches its regulation level. Then the voltage is regulated and charge current drops. The starting phase is determined by the initial battery voltage. In constant voltage condition, the charge current drops automatically. When it decreases below 10% of the fast charge value, charging is terminated. A programmable safety charge timer is provided to prevent prolonged charging if it is not naturally terminated for any reason. When the battery voltage falls below recharge threshold, charge cycle is automatically started (or restarted).

If the input voltage falls below the battery voltage, the device enters sleep mode. In sleep mode, the quiescent current is very low.

The SGM41526A and SGM41527A use dynamic power management (DPM) to prevent overload of the input source (AC adaptor). With DPM, the output charge current is reduced if the input power limit is reached. The input current is sensed and controlled by a precision current-sense amplifier to limit the input power.

Gate driver outputs are provided for power path selection that can be achieved by three external switches. Two N-type back-to-back MOSFETs (Q1, Q2) are used as input pair (adapter power in and reverse blocking control) along with a P-type (Q3) that is used to control the battery connection to the system bus. The system is powered from adapter by Q1 and Q2 on if a qualified adapter is present. Otherwise, the system is connected to the battery by Q3. And with power path control, the battery cannot feed back to the input.

The SGM41526A and SGM41527A can charge the battery from a DC source with a voltage up to 22V. This range covers common adapter voltages and the car battery voltage. The qualified adapter range is adjustable by OVPSET pin. If the input voltage is out of the range, Q1 and Q2 will not be turned on.

For 1-cell applications (only applicable to SGM41527A), when the battery is not removable, the design can be simplified by direct connection of the battery to the system. Therefore, when the input source is overloaded, the battery can help power the system automatically.

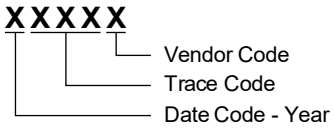
The SGM41526A and SGM41527A are available in a Green TQFN-5.5×3.5-24L package. It can operate over an ambient temperature range of -40℃ to +85℃.

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM41526A	TQFN-5.5×3.5-24L	-40℃ to +85℃	SGM41526AYTQQ24G/TR	SGM41526A YTQQ XXXXX	Tape and Reel, 3000
SGM41527A	TQFN-5.5×3.5-24L	-40℃ to +85℃	SGM41527AYTQQ24G/TR	SGM41527A YTQQ XXXXX	Tape and Reel, 3000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

AGND Referenced Voltages
- PVCC ..... -0.3V to 24V
- AVCC, ACP, ACN, ACDRV, CMSRC, STAT ..... -0.3V to 30V
- BTST ..... -0.3V to 30V
- nBATDRV, SRP, SRN ..... -0.3V to 24V
- SW ..... -2V to 24V
- FB (SGM41527A) ..... -0.3V to 24V
- CELL (SGM41526A), OVPSET, REGN, TS, TTC ..... -0.3V to 7V
- VREF, ISET, ACSET ..... -0.3V to 3.6V
- PGND ..... -0.3V to 0.3V

Differential Voltages

SRP-SRN, ACP-ACN ..... -0.5V to 0.5V

Package Thermal Resistance
- TQFN-5.5×3.5-24L, θ_{JA} ..... 30.2℃/W
- TQFN-5.5×3.5-24L, θ_{JB} ..... 6.9℃/W
- TQFN-5.5×3.5-24L, $\theta_{JC\ (TOP)}$ ..... 20℃/W
- TQFN-5.5×3.5-24L, $\theta_{JC\ (BOT)}$ ..... 2.3℃/W

Junction Temperature ..... +150℃

Storage Temperature Range ..... -65℃ to +150℃

Lead Temperature (Soldering, 10s) ..... +260℃

ESD Susceptibility

HBM 2000V

CDM 1000V

RECOMMENDED OPERATING CONDITIONS

Input Voltage Range, V_{IN} ..... 4.5V to 22V

Output Voltage, V_{BAT} ..... 18V (MAX)

Output Current Range (R_{SR} = 10mΩ), I_{OUT} ..... 0.6A to 4A

Maximum Differential Voltage

SRP-SRN, ACP-ACN ..... -200mV to 200mV

Operating Temperature Range ..... -40℃ to +85℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

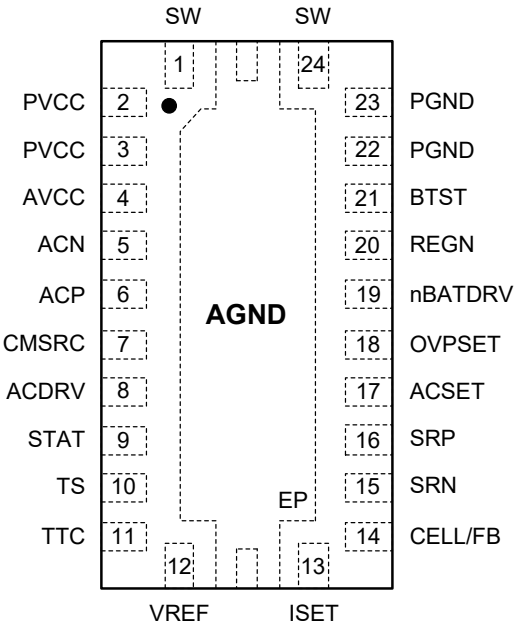
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

(TOP VIEW)



TQFN-5.5×3.5-24L

PIN DESCRIPTION

PIN	NAME	TYPE	FUNCTION
1, 24	SW	P	Switching Node. Connect SW pin to the output inductor and also to a bootstrap capacitor from BTST pin.
2, 3	PVCC	P	Charger Input Voltage. Decouple with at least 10μF ceramic capacitor from PVCC pin to PGND as close to IC as possible.
4	AVCC	P	IC Supply Power. Place an RC filter (10Ω-1μF) with ceramic capacitor from input power to AVCC pin to AGND and place capacitor close to the IC. For 5V input, a minimum 5Ω resistor is recommended. The device under-voltage lockout (UVLO) is sensed on AVCC pin (typically 3.3V rising with 0.21V hysteresis).
5	ACN	I	Input Current Sense Resistor Negative Input. Connect a 100nF ceramic capacitor from ACN to ACP for differential-mode filtering. Connect a 100nF ceramic capacitor from ACN to AGND for common-mode filtering.
6	ACP	I/P	Input Current Sense Resistor Positive Input. Connect a 100nF ceramic capacitor from ACN to ACP for differential-mode filtering. Connect an optional 100nF ceramic capacitor from ACP to AGND for common-mode filtering.
7	CMSRC	O	Common Source of the ACFET and RBFET. Connect with a 4.02kΩ resistor to the common source of the input MOSFET ACFET (Q1) and RBFET (Q2) to control the turn-on speed and limit inrush current. An external minimum 500kΩ resistor between ACDRV pin and CMSRC pin is essential.
8	ACDRV	O	Gate Driver Output for Input Switches. A 4.02kΩ resistor is placed to the common gate of the external N-channel ACFET and RBFET power MOSFETs. Connect both FETs as common source. It has break-before-make logic with respect to the nBATDRV and acts asymmetrical, allowing quick turn-off and slow turn-on.
9	STAT	O	Open-Drain Charge Status Output Pin with 10kΩ External Pull-Up to the Power Rail. It can be connected to LED to show the charging status or it can directly communicate with the host. The STAT pin acts as follows: During charge: low (LED ON). Charge completed, charger in sleep mode or charge disabled: high (LED OFF). Charge suspend (in response to a fault): 1Hz, including battery detection, charge suspend, input over-voltage, battery over-voltage, and timer fault. (LED BLINKS).

PIN DESCRIPTION (continued)

PIN	NAME	TYPE	FUNCTION
10	TS	I	Temperature Sense Voltage Input. Connect to a negative temperature coefficient (NTC) thermistor that can sense the battery temperature. The actual hot and cold temperature can be set by a resistor divider from VREF to TS to AGND. It is recommended to use a 103AT type thermistor for battery pack temperature sensing.
11	TTC	I	Safety Timer (Fast Charge) and Termination Control. Pre-charge timer is fixed inside the device (30min typically). Fast charge safety timer is determined by the capacitor from this pin to AGND (5.6min/nF). Safety timer is disabled by pulling this pin low or high, but charge termination is disabled only when it is pulled low. The safety timer can be reset by charge termination (charge termination, charge disabled, input over-voltage protection, battery over-voltage protection, charge suspend, battery absent, etc.).
12	VREF	P	3.3V Voltage Reference Output Internally Powered from AVCC Pin. Connect a 1μF ceramic capacitor to AGND as close to IC as possible. It is usually connected to the resistor divider of ISET, ACSET and TS pins. It can also be connected to STAT and CELL pins as pull-up rail.
13	ISET	I	Program Pin for Charge Current Settings. The voltage on this pin and the charge shunt resistor R_{SR} determine the fast charge current. V_{ISET} voltage can be set by a resistor divider (VREF-ISET-AGND). $$I_{CHG} = \frac{V_{ISET}}{20 \times R_{SR}}$$ The pre-charge and termination currents are equal and determined by I_{CHG} as a ratio of 10%. The charger disables when ISET voltage is pulled below 30mV and enables if it exceeds 120mV.
14	CELL (SGM41526A)	I	Cell Selection Pin for SGM41526A. Set it low for 4-cell battery, floating for 2-cell, and set it high for 3-cell battery. Cell voltage regulation is fixed at 4.2V per cell.
	FB (SGM41527A)		Feedback Pin for Regulating the Charge Voltage in SGM41527A in the Constant-Voltage Mode. A resistor divider from battery terminal (V_{BAT}) to FB (V_{FB}) to AGND sets the charge voltage. And the internal voltage reference is 2.1V.
15	SRN	I	Charge Current Sense Resistor, Negative Input. A shunt resistor is connected between SRN pin and SRP pin to sense charge current. Connect a 100nF ceramic capacitor between SRN pin and SRP pin for differential-mode filtering. Connect an optional 100nF capacitor between SRN and AGND for common-mode filtering.
16	SRP	I/P	Charge Current Sense Resistor, Positive Input. Connect a 100nF ceramic capacitor between SRN pin and SRP pin for differential-mode filtering. Connect another 100nF ceramic capacitor between SRP pin and AGND for common-mode filtering.
17	ACSET	I	Program Pin to Set Input Current Limit for Dynamic Power Management. A voltage divider from VREF to ACSET to AGND can be used to set this parameter along with the input shunt resistor R_{AC}: $$I_{DPM} = \frac{V_{ACSET}}{20 \times R_{AC}}$$
18	OVPSET	I	Program Pin for Input Over-Voltage Detection. The input voltage can be sensed by a resistor voltage divider from input to OVPSET to AGND so that the ACOV and ACUV can be realized by setting proper resistor. An input over-voltage (ACOV) is detected if OVPSET voltage exceeds the internal 1.6V reference. A voltage below 0.494V indicates an input under-voltage (ACUV). If either of the two cases happens, both of the ACFET and RBFET will be turned off. If it is in charging process, the charge will terminate. Then the LED that is connected to STAT pin will blink at 1Hz to indicate a fault.
19	nBATDRV	O	Gate Driver Output for External P-Type Power MOSFET (Battery Discharge Path). Use a 1kΩ resistor to connect this pin to the gate of the BATFET (Q3) to control the turn-on speed. The source of the BATFET connects to the system and the drain connects to the battery positive terminal. In order to decrease inrush current, the internal gate driver is designed with quick turn-off and slow turn-on functions. This gate driver has break-before-make logic with respect to the ACDRV gate driver (input switch).
20	REGN	P	5V Internal Supply for the PWM Low-side Switch Driver. Decouple with a 1μF ceramic capacitor from REGN pin to PGND pin close to the IC. Anode of integrated bootstrap diode is connected to this pin.
21	BTST	P	High-side Power MOSFET Driver Power Supply. Connect a 47nF bootstrap capacitor from SW to BTST.
22, 23	PGND	P	Device Power Ground. On the PCB layout, connect this pin directly to ground points of the input and output capacitors of the charger. PGND connects to AGND only through in one point on thermal pad under the IC.
EP	AGND	P	Exposed Pad Beneath the IC. Always solder thermal pad to the board. Use vias to transfer heat to the back side and other layers of PCB. Thermal pad acts as AGND and only connects to PGND at one single point.

NOTE:
1. I = Input, O = Output, P = Power.

ELECTRICAL CHARACTERISTICS

(T_J = -40℃ to +85℃, 4.5V ≤ V_{PVCC}, V_{AVCC} ≤ 22V (referred to AGND), typical values at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Conditions						
AVCC Input Voltage Operating Range during Charging	V_{AVCC_OP}		4.5		22	V
Quiescent Currents						
Battery Discharge Current (Sum of Currents into AVCC, PVCC, ACP, ACN)	I_{BAT}	V_{AVCC} > V_{UVLO}, V_{SRN} > V_{AVCC} (Sleep), T_J = 0℃ to +85℃		7.4	15	μA
		BTST, SW, SRP, SRN, V_{AVCC} > V_{UVLO}, V_{AVCC} > V_{SRN}, V_{ISET} < 30mV, V_{BAT} = 12.6V, charge disabled		18	30	
		BTST, SW, SRP, SRN, V_{AVCC} > V_{UVLO}, V_{AVCC} > V_{SRN}, V_{ISET} > 120mV, V_{BAT} = 12.6V, charge done		18	30	
Adapter Supply Current (Sum of Currents into AVCC, ACP, ACN)	I_{AC}	V_{AVCC} > V_{UVLO}, V_{AVCC} > V_{SRN}, V_{ISET} < 30mV, V_{BAT} = 12.6V, charge disabled		1.3	2.0	mA
		V_{AVCC} > V_{UVLO}, V_{AVCC} > V_{SRN}, V_{ISET} > 120mV, charge enabled, no switching		1.4	2.0	
		V_{AVCC} > V_{UVLO}, V_{AVCC} > V_{SRN}, V_{ISET} > 120mV, charge enabled, switching		15 (1)		
Charge Voltage Regulation						
SRN Regulation Voltage (SGM41526A)	V_{BAT_REG}	CELL floating, 2-cell, measured on SRN		8.4		V
		CELL to VREF, 3-cell, measured on SRN		12.6		
		CELL to AGND, 4-cell, measured on SRN		16.8		
SRN Regulation Voltage (SGM41527A)	V_{FB_REG}	Measure on FB		2.1		V
Charge Voltage Regulation Initial Accuracy			-0.4		0.4	%
Current Regulation - Fast Charge						
ISET Voltage Range	V_{ISET}	R_{SENSE} = 10mΩ	0.12		0.8	V
Charge Current Set Factor (Amps of Charge Current per Volt on ISET Pin)	K_{ISET}	R_{SENSE} = 10mΩ		5		A/V
Charge Current Regulation Initial Accuracy (with Schottky Diode on SW)		$V_{SRP-SRN}$ = 40mV	39.0	41.0	43.1	mV
		$V_{SRP-SRN}$ = 20mV	19.1	20.7	22.4	
		$V_{SRP-SRN}$ = 5mV	3.8	5.4	7.1	
Charge Disable Threshold	V_{ISET_CD}	V_{ISET} falling	30	50		mV
Charge Enable Threshold	V_{ISET_CE}	V_{ISET} rising		100	120	mV
Leakage Current into ISET	I_{ISET}	V_{ISET} = 2V			100	nA
Input Current Regulation						
Input DPM Current Set Factor (Amps of Input Current per Voltage on ACSET)	K_{DPM}	R_{SENSE} = 10mΩ		5		A/V
Input DPM Current Regulation Initial Accuracy (with Schottky Diode on SW)		$V_{ACP-ACN}$ = 80mV	78.3	81.6	84.8	mV
		$V_{ACP-ACN}$ = 40mV	37.3	41.0	44.7	
		$V_{ACP-ACN}$ = 20mV	17.6	20.7	23.8	
		$V_{ACP-ACN}$ = 5mV	4.2	5.5	6.9	
		$V_{ACP-ACN}$ = 2.5mV	1.5	3.0	4.5	
Leakage Current into ACSET Pin	I_{ACSET}	V_{ACSET} = 2V			100	nA

ELECTRICAL CHARACTERISTICS (continued)

(T_J = -40℃ to +85℃, 4.5V ≤ V_{PVCC}, V_{AVCC} ≤ 22V (referred to AGND), typical values at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Current Regulation - Pre-Charge							
Pre-Charge Current Set Factor	$K_{IPRECHG}$	Percentage of fast charge current			10 (2)		%
Pre-Charge Current Regulation Initial Accuracy		$V_{SRP-SRN}$ = 4mV		3.4	4.6	5.7	mV
		$V_{SRP-SRN}$ = 2mV		1.3	2.5	3.8	
Charge Termination							
Termination Current Set Factor	K_{TERM}	Percentage of fast charge current			10 (2)		%
Termination Current Regulation Initial Accuracy		$V_{SRP-SRN}$ = 4mV		2.9	3.9	4.8	mV
		$V_{SRP-SRN}$ = 2mV		0.9	1.8	2.7	
Deglitch Time for Termination (Both Edges)	t_{TERM_DEG}				100		ms
Termination Qualification Time	t_{QUAL}	V_{SRN} > V_{RECH} and I_{CHG} < I_{TERM}			250		ms
Termination Qualification Current	I_{QUAL}	Discharge current once termination is detected			2		mA
Input Under-Voltage Lockout Comparator (UVLO)							
AC Under-Voltage Rising Threshold	V_{UVLO}	Measure on AVCC		2.9	3.3	3.8	V
AC Under-Voltage Hysteresis, Falling	V_{UVLO_HYS}	Measure on AVCC			210		mV
Sleep Comparator (Reverse Discharging Protection)							
Sleep Mode Threshold	V_{SLEEP}	V_{AVCC} - V_{SRN} falling			90	280	mV
Sleep Mode Hysteresis	V_{SLEEP_HYS}	V_{AVCC} - V_{SRN} rising			210		mV
Sleep Deglitch to Disable Charge	$t_{SLEEP\_FALL\_CD}$	V_{AVCC} - V_{SRN} falling			1		ms
Sleep Deglitch to Turn Off Input FETs	$t_{SLEEP\_FALL\_FETOFF}$	V_{AVCC} - V_{SRN} falling			5		ms
Deglitch to Enter Sleep Mode, Disable VREF and Enter Low Quiescent Mode	t_{SLEEP_FALL}	V_{AVCC} - V_{SRN} falling			100		ms
Deglitch to Exit SLEEP Mode, and Enable VREF	t_{SLEEP_PWRUP}	V_{AVCC} - V_{SRN} rising			30		ms
ACN-SRN Comparator							
Threshold to Turn On BATFET	$V_{ACN-SRN}$	$V_{ACN-SRN}$ falling			180	400	mV
Hysteresis to Turn Off BATFET	$V_{ACN-SRN\_HYS}$	$V_{ACN-SRN}$ rising			110		mV
Deglitch to Turn On BATFET	$t_{BATFETOFF\_DEG}$	$V_{ACN-SRN}$ falling			2		ms
Deglitch to Turn Off BATFET	$t_{BATFETON\_DEG}$	$V_{ACN-SRN}$ rising			50		μs
Battery LOWV Comparator							
Pre-Charge to Fast Charge Transition	V_{LOWV}	Measure on SRN (SGM41526A)	CELL floating, 2-cell	5.7	5.8	6.1	V
			CELL to VREF, 3-cell	8.4	8.7	9.1	
			CELL to AGND, 4-cell	11.1	11.7	12.2	
		Measure on FB (SGM41527A)		1.42	1.46	1.50	
Fast Charge to Pre-Charge Hysteresis	V_{LOWV_HYS}	Measure on SRN (SGM41526A)	CELL floating, 2-cell		400		mV
			CELL to VREF, 3-cell		600		
			CELL to AGND, 4-cell		800		
		Measure on FB (SGM41527A)			100		
V_{LOWV} Rising Deglitch	$t_{PRE2FAS}$	Delay to start fast charge current			25		ms
V_{LOWV} Falling Deglitch	$t_{FAST2PRE}$	Delay to start pre-charge current			25		ms

ELECTRICAL CHARACTERISTICS (continued)

(T_J = -40℃ to +85℃, 4.5V ≤ V_{PVCC}, V_{AVCC} ≤ 22V (referred to AGND), typical values at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Recharge Comparator							
Recharge Threshold, below Regulation Voltage Limit, V_{BAT_REG} - V_{SRN} (SGM41526A), or V_{FB_REG} - V_{FB} (SGM41527A)	V_{RECHG}	Measure on SRN (SGM41526A)	CELL floating, 2-cell	110	200	290	mV
			CELL to VREF, 3-cell	190	300	430	
			CELL to AGND, 4-cell	280	400	540	
		Measure on FB (SGM41527A)		50	70	90	
V_{RECHG} Rising Deglitch	$t_{RECH\_RISE\_DEG}$	V_{FB} decreasing below V_{RECHG}			10		ms
V_{RECHG} Falling Deglitch	$t_{RECH\_FALL\_DEG}$	V_{FB} increasing above V_{RECHG}			10		ms
Battery Over-Voltage Comparator							
Over-Voltage Rising Threshold	V_{OV_RISE}	As percentage of V_{BAT_REG} (SGM41526A) or V_{FB_REG} (SGM41527A)			104		%
Over-Voltage Falling Threshold	V_{OV_FALL}	As percentage of V_{SRN} (SGM41526A) or V_{FB_REG} (SGM41527A)			102		%
Input Over-Voltage Comparator (ACOV)							
AC Over-Voltage Rising Threshold to Turn Off ACFET	V_{ACOV}	OVPSET rising		1.53	1.6	1.69	V
AC Over-Voltage Falling Hysteresis	V_{ACOV_HYS}	OVPSET falling			40		mV
AC Over-Voltage Rising Deglitch to Turn Off ACFET and Disable Charge	$t_{ACOV\_RISE\_DEG}$	OVPSET rising			1		μs
AC Over-Voltage Falling Deglitch to Turn On ACFET	$t_{ACOV\_FALL\_DEG}$	OVPSET falling			30		ms
Input Under-Voltage Comparator (ACUV)							
AC Under-Voltage Falling Threshold to Turn Off ACFET	V_{ACUV}	OVPSET falling		0.44	0.494	0.55	V
AC Under-Voltage Rising Hysteresis	V_{ACUV_HYS}	OVPSET rising			80		mV
AC Under-Voltage Falling Deglitch to Turn Off ACFET and Disable Charge	$t_{ACOV\_FALL\_DEG}$	OVPSET falling			1		μs
AC Under-Voltage Rising Deglitch to Turn On ACFET	$t_{ACOV\_RISE\_DEG}$	OVPSET rising			30		ms
Thermal Regulation							
Junction Temperature Regulation Accuracy	T_{A_REG}	V_{ISET} > 120mV, charging			120		℃
Thermal Shutdown Comparator							
Thermal Shutdown Rising Temperature	T_{SHUT}	Temperature rising			150		℃
Thermal Shutdown Hysteresis	T_{SHUT_HYS}	Temperature falling			20		℃
Thermal Shutdown Rising Deglitch	$T_{SHUT\_RISE\_DEG}$	Temperature rising			100		μs
Thermal Shutdown Falling Deglitch	$T_{SHUT\_FALL\_DEG}$	Temperature falling			10		ms
Thermistor Comparator							
Cold Temperature Threshold, TS Pin Voltage Rising Threshold	V_{LTF}	Charger suspends charge, as percentage of V_{VREF}		72.1	73.6	75.2	%
Cold Temperature Hysteresis, TS Pin Voltage Falling	V_{LTF_HYS}	As percentage of V_{VREF}			0.68	1.45	%
Hot Temperature TS Pin Voltage Rising Threshold	V_{HTF}	As percentage of V_{VREF}		45.8	47.3	48.8	%
Cut-Off Temperature TS Pin Voltage Falling Threshold	V_{TCO}	As percentage of V_{VREF}		43.2	44.6	45.7	%
Deglitch Time for Temperature out of Range Detection	$t_{TS\_CHG\_SUS}$	V_{TS} > V_{LTF}, or V_{TS} < V_{TCO}, or V_{TS} < V_{HTF}			20		ms
Deglitch Time for Temperature in Valid Range Detection	$t_{TS\_CHG\_RESUME}$	V_{TS} < V_{LTF} - V_{LTF_HYS} or V_{TS} > V_{TCO}, or V_{TS} > V_{HTF}			400		ms

ELECTRICAL CHARACTERISTICS (continued)

(T_J = -40℃ to +85℃, 4.5V ≤ V_{PVCC}, V_{AVCC} ≤ 22V (referred to AGND), typical values at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Charge Over-Current Comparator (Cycle-by-Cycle)						
Charge Over-Current Rising Threshold, V_{SRP} > 2.2V	V_{OCP_CHRG}	Current as percentage of fast charge current		180		%
Charge Over-Current Limit Min, V_{SRP} < 2.2V	V_{OCP_MIN}	Measure $V_{SRP-SRN}$		46		mV
Charge Over-Current Limit Max, V_{SRP} > 2.2V	V_{OCP_MAX}	Measure $V_{SRP-SRN}$		77		mV
HSFET Over-Current Comparator (Cycle-by-Cycle)						
Current Limit on HSFET	I_{OCP_HSFET}	Measure on HSFET		10		A
Charge Under-Current Comparator (Cycle-by-Cycle)						
Charge Under-Current Falling Threshold	V_{UCP}	Measure on $V_{SRP-SRN}$	1	5	12	mV
Battery Short Comparator						
Battery Short Falling Threshold	V_{BATSHT}	Measure on SRN		2		V
Battery Short Rising Hysteresis	V_{BATSHT_HYS}	Measure on SRN		200		mV
Deglitch on Both Edges	t_{BATSHT_DEG}			1		μs
Charge Current during BAT_SHORT	V_{BATSHT}	Percentage of fast charge current		10 (2)		%
VREF Regulator						
VREF Regulator Voltage	V_{VREF_REG}	V_{AVCC} > V_{UVLO}, no load	3.24	3.3	3.36	V
VREF Current Limit	I_{VREF_LIM}	V_{VREF} = 0V, V_{AVCC} > V_{UVLO}	20		80	mA
REGN Regulator						
REGN Regulator Voltage	V_{REGN_REG}	V_{AVCC} > 10V, V_{ISET} > 120mV	4.8	5.0	5.2	V
REGN Current Limit	I_{REGN_LIM}	V_{REGN} = 0V, V_{AVCC} > 10V, V_{ISET} > 120mV	20		100	mA
TTC Input						
Pre-Charge Safety Timer	$t_{PRECHRG}$	Pre-charge time before fault occurs		1800		s
Fast Charge Timer Range	$t_{FASTCHRG}$	T_{CHG} = C_{TTC} × K_{TTC}	1		10	hr
Fast Charge Timer Accuracy			-10		10	%
Timer Multiplier	K_{TTC}			5.6		min/nF
TTC Low Threshold	V_{TTC_LOW}	TTC falling		0.33		V
TTC Source/Sink Current	I_{TTC}		45	50	55	μA
TTC Oscillator High Threshold	$V_{TTC\_OSC\_HI}$			1.5		V
TTC Oscillator Low Threshold	$V_{TTC\_OSC\_LO}$			1.0		V
Battery Switch (BATFET) Driver						
BATFET Turn-Off Resistance	$R_{DS\_BAT\_OFF}$	V_{AVCC} > 5V			200	Ω
BATFET Turn-On Resistance	$R_{DS\_BAT\_ON}$	V_{AVCC} > 5V			10	kΩ
BATFET Drive Voltage	V_{BATDRV_REG}	V_{BATDRV_REG} = V_{ACN} - V_{BATDRV} when V_{AVCC} > 5V and BATFET is on	5.1		6.4	V
BATFET Power-Up Delay to Turn Off BATFET after Adapter is Detected	t_{BATFET_DEG}			30		ms
AC Switch (ACFET) Driver						
ACDRV Charge Pump Current Limit	I_{ACFET}	V_{ACDRV} - V_{CMSRC} = 5V		160		μA
Gate Drive Voltage on ACFET	V_{ACDRV_REG}	V_{ACDRV} - V_{CMSRC} when V_{AVCC} > V_{UVLO}	5.4	5.6		V
Maximum Load between ACDRV and CMSRC	R_{ACDRV_LOAD}		20			kΩ

ELECTRICAL CHARACTERISTICS (continued)

(T_J = -40℃ to +85℃, 4.5V ≤ V_{PVCC}, V_{AVCC} ≤ 22V (referred to AGND), typical values at T_J = +25℃, unless otherwise noted.)

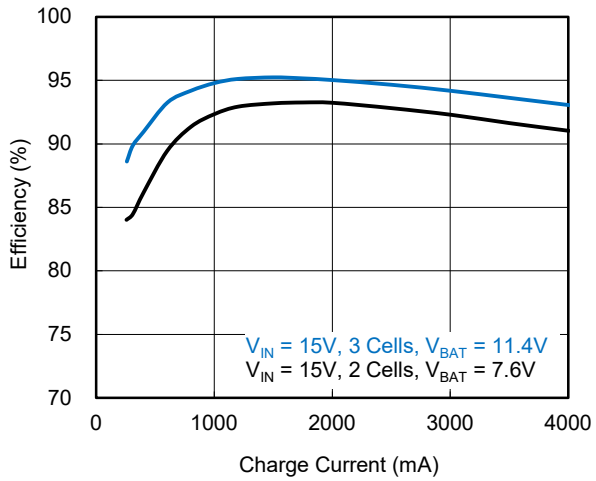
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
AC/BAT Switch Driver Timing						
Driver Dead Time	t_{DRV_DEAD}	Dead time when switching between ACFET and BATFET		10		μs
Battery Detection						
Wake Timer	t_{WAKE}	Max time charge is enabled		500		ms
Wake Current	I_{WAKE}	R_{SENSE} = 10mΩ	100	250	400	mA
Discharge Timer	t_{DISCH}	Max time discharge current is applied		1		s
Discharge Current	I_{DISCH}			9.5		mA
Fault Current after a Time-Out Fault	I_{FAULT}			2		mA
Wake Threshold with Respect to V_{REG} to Detect Absent during Wake	V_{WAKE}	Measure on SRN (SGM41526A)		100		mV/cell
Discharge Threshold to Detect Battery Absent during Discharge	V_{DISCH}	Measure on SRN (SGM41526A)		2.9		V/cell
Internal PWM						
PWM Switching Frequency	f_{SW}		1200	1600	1800	kHz
Driver Dead Time (1)	t_{SW_DEAD}	Dead time when switching between LSFET and HSFET no load		30		ns
High-side MOSFET On-Resistance	R_{DS_HI}	V_{BTST} - V_{SW} = 4.5V		29	55	mΩ
Low-side MOSFET On-Resistance	R_{DS_LO}			33	65	mΩ
Bootstrap Refresh Comparator Threshold Voltage	$V_{BTST\_REFRESH}$	V_{BTST} - V_{SW} when low-side refresh pulse is requested, V_{AVCC} = 4.5V	2.8			V
		V_{BTST} - V_{SW} when low-side refresh pulse is requested, V_{AVCC} > 6V	2.8			
Internal Soft-Start (8 Steps to Regulation Current I_{CHG})						
Soft-Start Steps	SS_STEP			8		step
Soft-Start Step Time	t_{SS_STEP}			1.6	3	ms
Charger Section Power-Up Sequencing						
Delay from ISET above 120mV to Start Charging Battery	t_{CE_DELAY}			1.5		s
Integrated BTST Diode						
Forward Bias Voltage	V_F	I_F = 120mA at +25℃		0.85		V
Reverse Breakdown Voltage	V_R	I_R = 2μA at +25℃	21			V
Logic IO Pin Characteristics (STAT, CELL)						
STAT Output Low Saturation Voltage	V_{OUT_LO}	Sink current = 5mA			0.6	V
CELL Pin Input Low Threshold, 4-Cell (SGM41526A)	V_{CELL_LO}	CELL pin voltage falling edge		0.3		V
CELL Pin Input Mid Threshold, 2-Cell (SGM41526A)	V_{CELL_MID}	CELL pin middle level voltage	0.7		2.5	V
CELL Pin Input High Threshold, 3-Cell	V_{CELL_HI}	CELL pin voltage rising edge		2.7		V

NOTES:

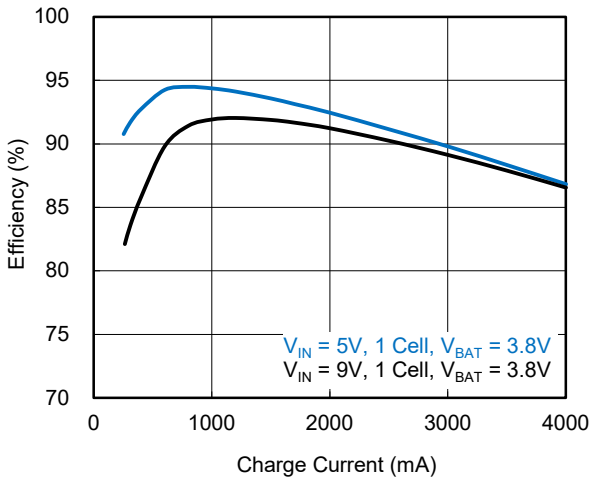
1. Specified by design.
2. The minimum current is 250mA on 10mΩ sense resistor.

TYPICAL PERFORMANCE CHARACTERISTICS

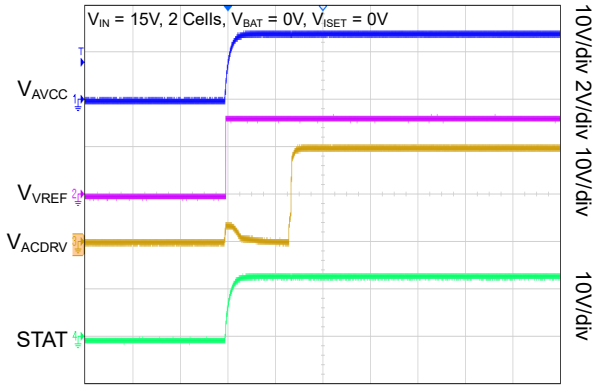
Efficiency vs. Charge Current



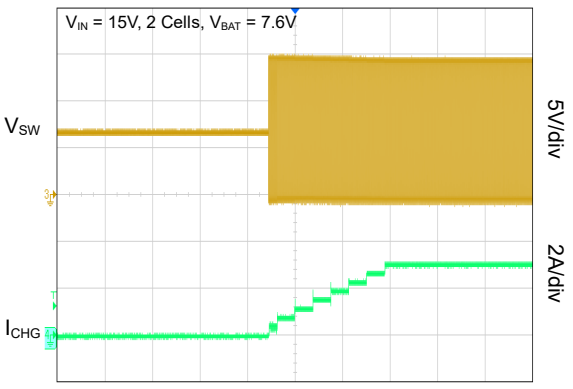
Efficiency vs. Charge Current



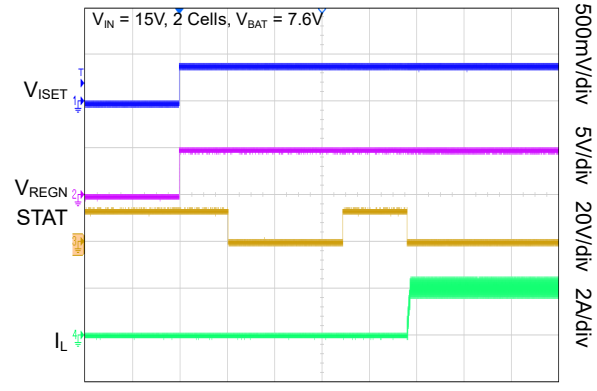
Power-Up



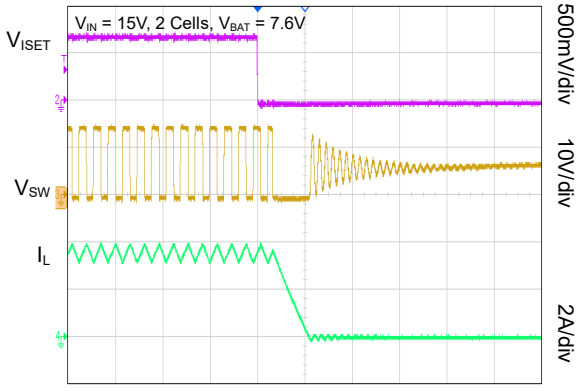
Current Soft-Start



Charge Enable by ISET

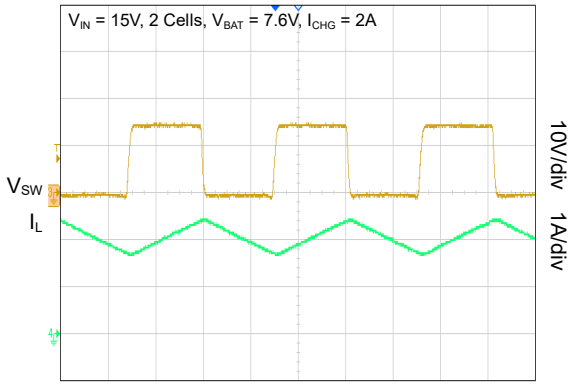


Charge Disable by ISET



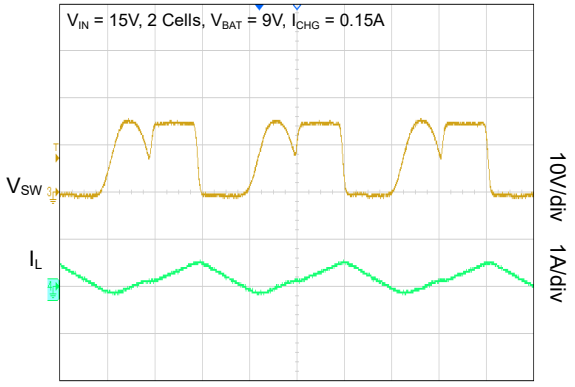
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Continuous Conduction Mode Switching



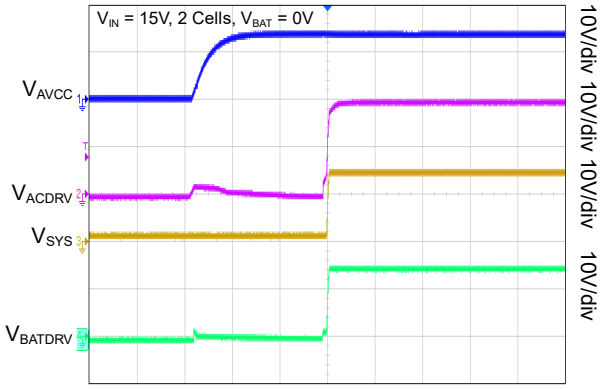
Time (200ns/div)

Discontinuous Conduction Mode Switching



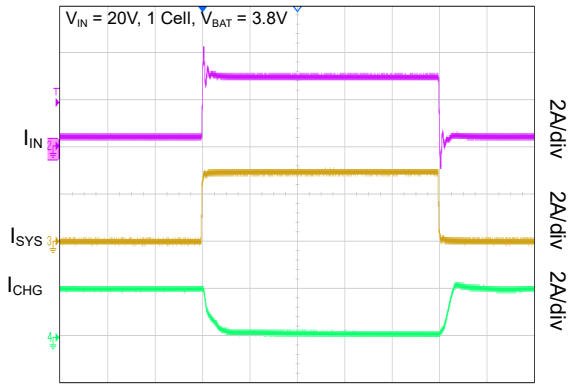
Time (200ns/div)

BATFET to ACFET Transition During Power-Up



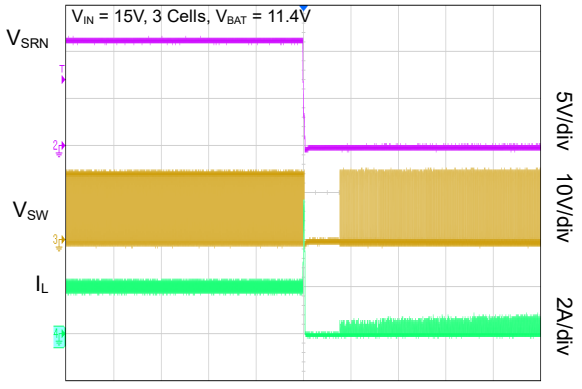
Time (10ms/div)

System Load Transient (Input Current DPM)



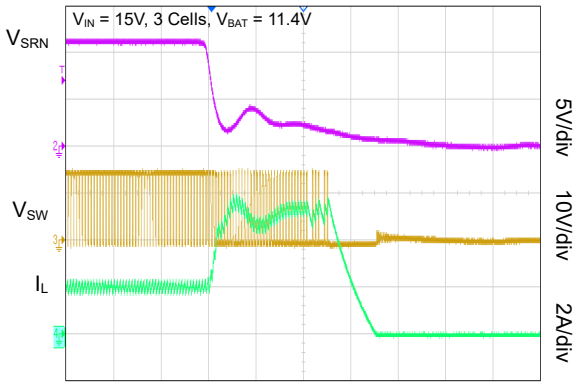
Time (100μs/div)

Battery-to-Ground Short Protection



Time (2ms/div)

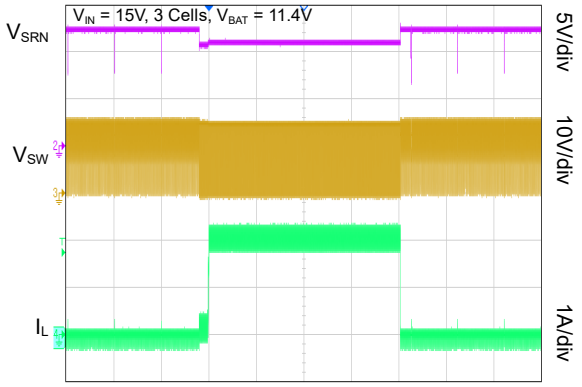
Battery-to-Ground Short Transition



Time (10μs/div)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Battery Insertion and Removal



Time (500ms/div)

FUNCTIONAL BLOCK DIAGRAM

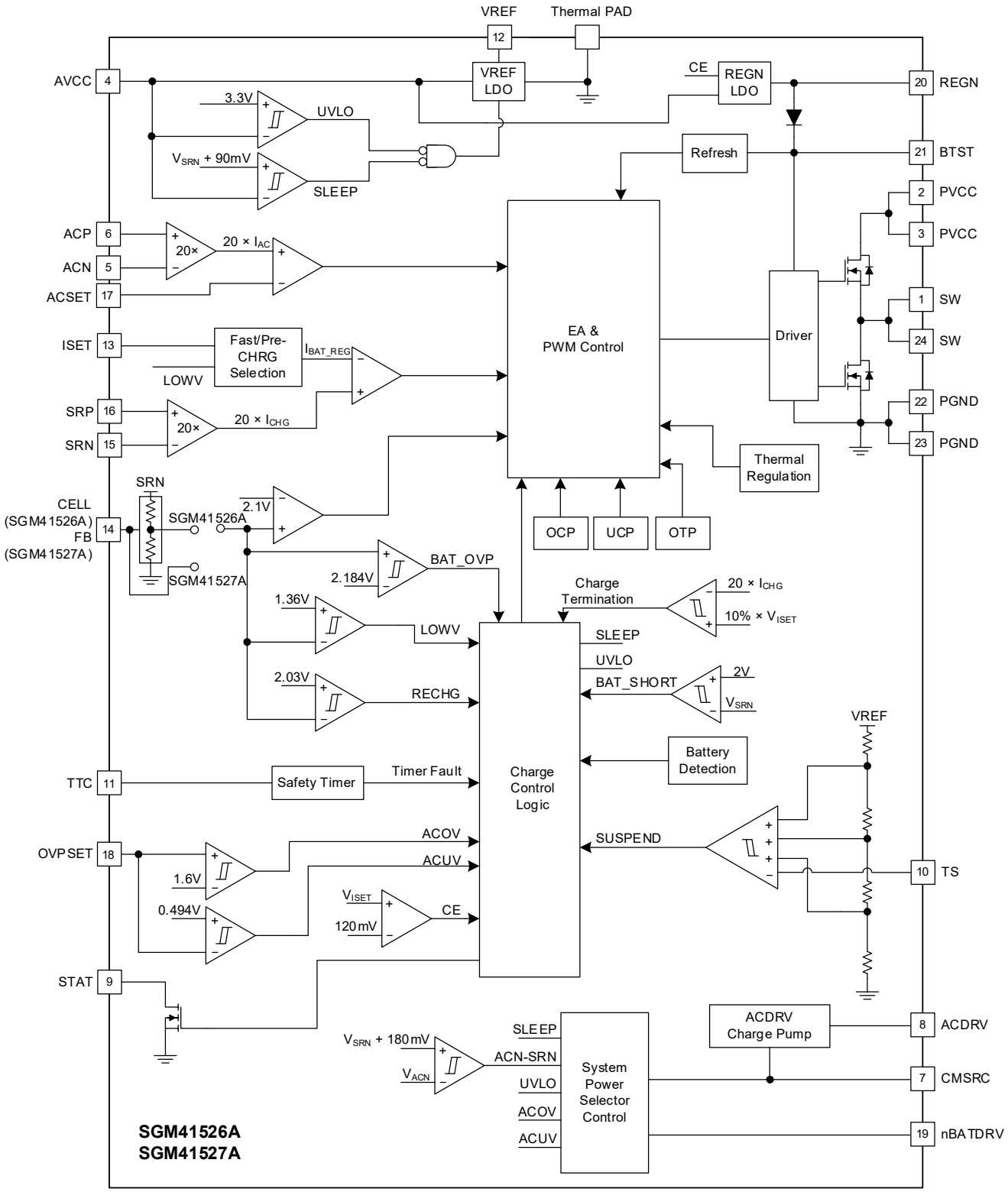


Figure 2. Functional Block Diagram

DETAILED DESCRIPTION

The SGM41526A and SGM41527A are Li-Ion and Li-polymer fixed-frequency synchronous PWM battery chargers with integrated switching power MOSFETs. Using external switches, power path management is provided along with accurate regulation of the input current, charge current and battery voltage. The internal block diagram is given in Figure 2.

Battery Voltage Regulation

An accurate PWM voltage regulator is used for charge voltage regulation. For the SGM41526A, the number of battery cells depends on the CELL pin. Two (CELL = floating), three (CELL = VREF) or four (CELL = AGND) cells can be connected in series with a fixed nominal voltage of 4.2V per cell. Table 1 shows the charge regulation voltage in each case.

Table 1. Defining Number of Battery Cells for SGM41526A

CELL Pin Voltage	Charge Regulation Voltage
Floating	8.4V (2 Cells)
VREF	12.6V (3 Cells)
AGND	16.8V (4 Cells)

For the SGM41527A, the regulation voltage is adjustable. The FB voltage is compared to an internal 2.1V voltage reference like a conventional voltage regulator. The regulation voltage can be adjusted by using an external resistor divider on the battery voltage (output voltage). Connect the center point of the resistor divider to the FB pin. The battery regulation voltage (V_{BAT}) in the SGM41527A is calculated by Equation 1:

$$V_{BAT} = 2.1V \times \left(1 + \frac{R_1}{R_2}\right) \quad (1)$$

where

• R_1 is connected between the battery positive terminal and FB.

• R_2 is connected between FB and AGND.

Battery Current Regulation

The maximum charging current for fast charge is set by the ISET input. Connect battery current sense resistor (R_{SR}) between SRP and SRN. The equation for charge current is given by:

$$I_{CHG} = \frac{V_{ISET}}{20 \times R_{SR}} \quad (2)$$

The maximum of the full-scale SRP-SRN differential voltage is 40mV, and it determines the maximum charge current selected by ISET. The maximum valid input voltage of ISET is 0.8V. For example, with a 10mΩ sense resistor, the maximum adjustable charge current is 4A, and with a 20mΩ resistor, it is 2A. If V_{ISET} = 0.5V and R_{SR} = 10mΩ, the fast charge current is I_{CHG} = 2.5A.

Pulling the ISET voltage down to ground (below 30mV) disables the charger. To enable the charger, the ISET voltage should exceed 120mV. The minimum charge current is limited by the 120mV threshold level. For example, when R_{SR} = 10mΩ, the minimum fast charge current is no less than 600mA.

As a protective feature, if the device junction temperature exceeds +120℃, the charge current folds back and is internally reduced to keep the junction temperature below +120℃.

Pre-Charge Phase

If the battery voltage is lower than V_{LOWV} when the device is powered up, the charge will start with a small pre-charge current to safely recover the battery from deep discharge state. If the battery voltage still does not exceed the V_{LOWV} threshold after 30 minutes, charging will stop, and fault status will be declared by the status pins. V_{LOWV} is typically 2.9V/cell for SGM41526A and 1.46V on FB pin for SGM41527A. The pre-charge current is determined by the fast charge current as a ratio of 10%:

$$I_{PRECHARGE} = \frac{V_{ISET}}{200 \times R_{SR}} \quad (3)$$

The deglitch time of fast charge and pre-charge transition is 25ms.

Typical Charge Cycle

Figure 3 shows a complete charge cycle profile (battery voltage and current versus time) with all the three phases followed by a typical discharge and auto recharge. The charge is started assuming that the battery is in a deep discharge state (low battery voltage). After termination and stopping the charge, the battery is normally discharged by system loads. When the voltage falls below the recharge threshold, another cycle is initiated from fast charge, to bring the battery back to the full charge state. A new charging cycle begins when any of the following conditions is met:

• The SRN pin voltage falls below the recharge threshold (V_{RECH}).

• A power-on-reset (POR).

• Disable and enable charge by pulling ISET pin below 30mV and then above 120mV, respectively.

Depending on the battery voltage, the charge is started with the proper phase. Charge sequence details will be explained in the next sections.

DETAILED DESCRIPTION (continued)

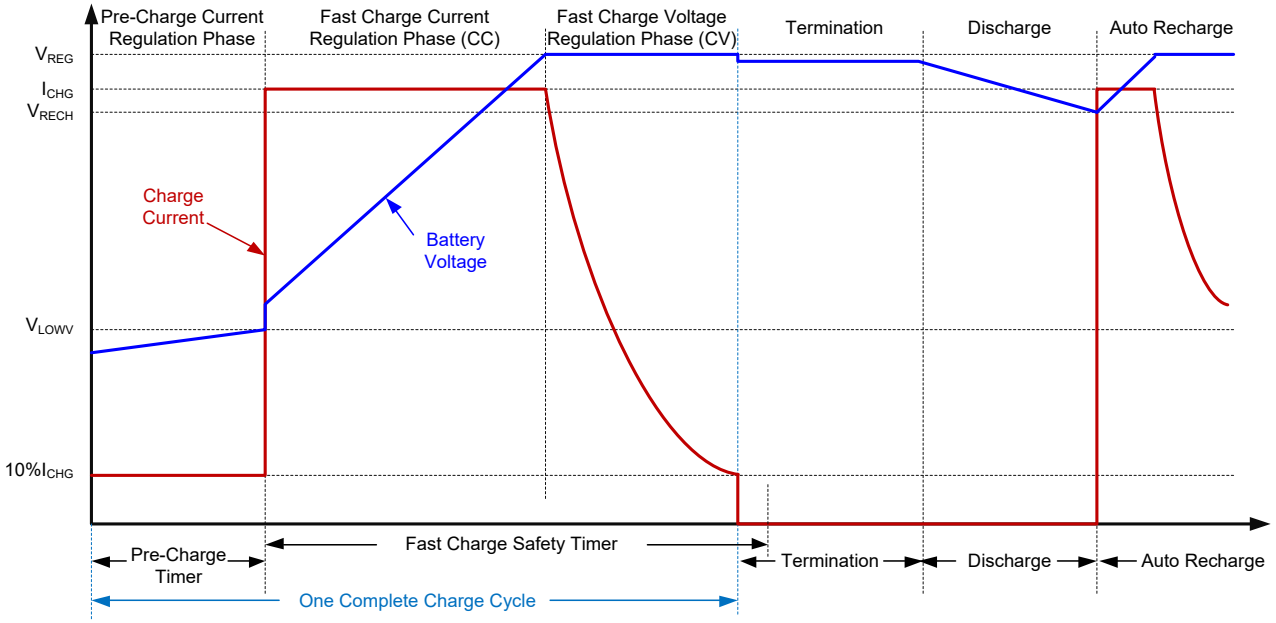


Figure 3. Typical Charge and Discharge Profile

Regulation of the Input Current

The input current is used to power the system and to charge the battery. System current may vary from zero to maximum load. With dynamic power management (DPM) capability, the adapter does not need to be designed for maximum power demand for both charge and system at the same time. Otherwise it will lead to a bulky AC adapter and relatively higher cost. With DPM, the charge current is reduced when the system has high demand for power, such that the input current is regulated to a predefined maximum. Therefore, the AC adapter can be designed for lower power that results in smaller adapter size and cost.

Input current regulation level of DPM is programmed by the voltage on ACSET pin and the input shunt resistor R_{AC}, as given in Equation 4:

$$I_{DPM} = \frac{V_{ACSET}}{20 \times R_{AC}} \quad (4)$$

The sense voltage across R_{AC} (typically 10mΩ) is sent to ACP and ACN pins. The regulation accuracy can be improved with larger sense resistor but at the cost of lower efficiency.

Termination, Recharge and Timers

In the constant voltage charging phase, the device also detects the charging current and battery voltage. The charge cycle will be terminated if the battery is fully charged that is detected when charge voltage exceeds recharge threshold (V_{RECH}) and charge current falls below termination current threshold (I_{TERM}). Charge voltage is sensed on the SRN pin of the SGM41526A and on the FB pin of the SGM41527A. Recharge voltage threshold (V_{RECH}) is a little bit lower than the regulation voltage and the termination current threshold (I_{TERM}) is equal to 10% of the programmed fast charge current as given in Equation 5:

$$I_{TERM} = \frac{V_{ISET}}{200 \times R_{SR}} \quad (5)$$

For battery safety, prolonged charging must be avoided, so time limits are considered for charge phases. For pre-charge phase, a fixed 30-minute safety timer is employed. For the fast charge phase, an adjustable timer is used. This timer can be programmed by a capacitor (C_{TTC}) connected between the TTC and AGND pins based on Equation 6:

$$t_{TTC}\ (min) = C_{TTC}\ (nF) \times K_{TTC}\ (min/nF) \quad (6)$$

where K_{TTC} is a constant typically equal to 5.6min/nF.

Connecting TCC pin to AGND disables both termination and fast charge timers. Connecting TCC pin to VREF disables the safety timer only and termination timer remains functioning.

DETAILED DESCRIPTION (continued)

Device Power-Up

The device power pin (AVCC) can be supplied by the battery or the adapter. If AVCC voltage falls below UVLO threshold, the device remains disabled. If AVCC voltage exceeds UVLO threshold, the device is enabled and another comparator (charger sleep comparator) checks the AVCC voltage to identify the power source. If the adapter is detected and the AVCC voltage exceeds the SRN voltage (battery voltage), the charger exits the sleep mode and can be enabled for charging. If the AVCC voltage is lower than SRN, the charger enters the low quiescent current sleep mode to minimize power taken from the battery. In the sleep mode, the STAT pin goes to high-impedance state and VREF output is turned off.

AVCC Input Under-Voltage Lockout (UVLO)

Usually the system cannot properly operate if AVCC voltage is too low (under-voltage). Therefore the device is enabled until AVCC voltage exceeds a minimum level (UVLO). All circuits on the IC are disabled if AVCC falls below UVLO threshold, regardless of the source of power.

Input Over-Voltage/Under-Voltage Protection

The SGM41526A and SGM41527A provide over-voltage (OV) and under-voltage (UV) protections to avoid system damage due to high or low input supply voltage. The input is qualified if input voltage is within the UV and OV window. The ACOV and ACUV comparators monitor the OVPSET voltage. If it exceeds 1.6V (for OV) or falls below 0.494V (for UV), the charge will be disabled and both input switches (Q1 and Q2) will be turned off to disconnect the system from the power supply. A resistor divider from input source can be used to define the input qualification window. Unlike UVLO that acts on AVCC (powered from input supply or battery), the OV and UV protections act only on the input power supply.

Charge Enable and Disable

If all following conditions are fulfilled, a charge will be started:

- V_{ISET} > 120mV (enable charge).
- V_{AVCC} > V_{UVLO} (device not in UVLO).
- V_{AVCC} > V_{SRN} (charger not in sleep mode).
- 0.494V < V_{OVPSET} < 1.6V (qualified power input).
- Not in Thermal Shutdown (T_{SHUT}).
- No TS fault (battery temperature not too hot or cold).
- Detect battery presence.
- ACFET is turned on.
- TTC or pre-charge timers are not expired.
- REGN and VREF pins are at their normal voltage levels without overloading.

The device remains charging until the battery is fully charged (normal termination), unless the charge is disabled when V_{ISET} < 30mV or when any of the above conditions is not fulfilled during the charge.

Power Path Selection

The SGM41526A and SGM41527A can automatically select the input adapter or battery as power source for the system. By default, the system is powered from the battery during device power-up or in sleep mode. The device can exit sleep mode if a qualified adapter is plugged in. Then the BATFET is turned off and the back-to-back MOSFET pair on the power input is turned on with a protective break-before-make logic so that system is connected to adaptor. The ACFET turns on after 10μs dead time when BATFET is turned off, so that it avoids direct input to battery short that can cause over-current through the selector switches.

Both gates of the back-to-back MOSFET pair on the power input are driven by the ACDRV pin. The sources are connected together to the CMSRC pin (Figure 1). The drain of the RBFET (Q2) is connected to the ACP pin. Q2 is for reverse discharge protection to avoid current flow from the battery to the input source. Low $R_{DS(ON)}$ switches are recommended for Q1 and Q2 to minimize conduction losses and heat generation. ACFET (Q1) can control the connection of adapter to system and battery. This switch also limits the inrush current rise/fall rate (di/dt) when input adapter is connected to the system by controlling the turn-on time.

The BATFET (P-channel, Q3) controls the connection of battery and system. Its gate is driven by nBATDRV pin and its source is connected to system.

The ACFET remains off, as long as a qualified voltage is not detected, by applying zero gate-source voltage. ACFET separates the adapter from system.

If the device is not in UVLO and system voltage is at most 0.18V above the battery, the BATFET remains on by applying -5.9V to the gate-source through the nBATDRV pin (gate voltage clamps to ground if the system voltage is less than 5.9V). The conditions can be represented as:

- V_{AVCC} > V_{UVLO} (not in UVLO).
- V_{ACN} < V_{SRN} + 180mV.

The source pin of the BATFET is connected to the system, ACN pin and PVCC.

DETAILED DESCRIPTION (continued)

If the input voltage is qualified and AVCC voltage is at least 0.21V above SRN (battery), the device can exit the sleep mode and transfer the system from battery to adapter. With the break-before-make logic, there is a 10μs dead time between input MOSFET pair and BATFET. At first the BATFET is turned off to disconnect battery from system by pulling up the nBATDRV voltage to ACN pin. Then the ACFET is turned on with a 5.6V gate drive voltage between the ACDRV and CMSRC pins, which is provided by an internal charge pump. The conditions for connecting the adapter to the system can be represented as follows:

• V_{ACUV} < V_{OVPSET} < $V_{ACOV.}$
• V_{AVCC} > V_{SRN} + 210mV.

When any of above conditions is no longer valid, ACFET is turned off and the device enters the sleep mode. BATFET remains off until the system voltage falls close to SRN (battery voltage). Then the BATFET turns on and connects the battery and system. An internal regulator drives nBATDRV pin to ACN - 5.9V to turn on BATFET.

Asymmetrical gate driving is used for fast turn-off and slow turn-on of the ACFET and BATFET. This will allow smooth transitions and soft connection of the system to the supply line. Turn-on delay can be increased by adding capacitance between the gate and source of the switches.

Charge Converter

The charge converter in SGM41526A/7A is a 1.6MHz PWM step-down regulator. The fixed switching frequency makes the filter design simple under all input/output or temperature conditions. Pulse skipping occurs if the duty cycle is approximately 97%. A type III compensation network is designed inside so that the use of low ESR ceramic capacitors on the output is allowed. The compensated error amplifier output is compared with 1.6MHz sawtooth ramp voltage to generate PWM wave. The sawtooth amplitude is proportionally adjusted to the AVCC voltage (input feedforward) to compensate the impact of the input voltage variations on the loop gain and simplify the loop compensation.

Internal Charge Current Soft-Start

The charge current automatically soft starts when fast charge mode begins to limit the stress on the converter components due to the current overshoots. During the soft-start, a total of 8 current levels are available for the programmed regulation current with an evenly spaced step. Each step lasts almost 1.6ms, for a typical soft-tart rise time of 12.8ms. This function is designed inside the device and no external components are required.

Charge Over-Current Protection

The high-side MOSFET current in the converter is always monitored by a sense FET and if it exceeds the MOSFET current limit (typically 10A), the high-side MOSFET is turned off until the next cycle.

There is another over-current protection for charge current. When it exceeds 180% of the programmed value, the high-side MOSFET is also turned off until the current falls below the threshold.

Charge Negative Current Protection

When the battery is charged, the inductor current reduces and may become negative. This negative current means that the battery feeds energy to input through converter (it is called Boost effect). The Boost effect can cause over-voltage on the input circuit and AVCC, which can damage the input components, device itself and the system. To prevent the boosting and negative charge current, the low-side switch should be turned off before the current drops to zero. The device senses the charge current by the voltage of the SRP-SRN, and if it falls below 5mV, the low-side switch is turned off for the rest of the switching cycle. This leads to discontinuous conduction mode (DCM) operation of the converter. Keeping low-side switch off limits the charging of bootstrap capacitor that feeds the high-side switch gate driver. A comparator always checks the high-side driver supply voltage, and if it falls below 2.8V the low-side switch is turned on for a short period to refresh and recharge the bootstrap capacitor voltage. This protection overrides the negative charge current protection.

DETAILED DESCRIPTION (continued)

Battery Detection

Battery presence detection is important and specially needed for the applications with removable batteries. The SGM41526A and SGM41527A use a reliable detection method for battery absence, battery insertion and battery removal. This detection procedure runs during power-up or when the battery voltage is lower than the recharge threshold. A low voltage on SRN pin (that connects to battery) can be detected due to battery discharge or battery removal. The detection process is designed such that the large capacitors on the charger output are not detected as battery. The detection flow chart is given in Figure 4.

Battery detection starts by applying a 9.5mA sink current though the SRN pin to the battery at power-up or when the SRN voltage falls below recharge threshold. If the battery voltage does not fall below the battery LOWV threshold in 1s, the battery is detected as present so the 9.5mA sink is turned off and the charge starts. During the 1s period, the 9.5mA discharge current is disabled as long as the battery voltage falls below battery LOWV threshold. Then the converter generates a small charge current to charge the SRN pin. The charge current is 250mA typically with 10mΩ sense resistor. Now, if 0.5s timer times out and the battery voltage exceeds the recharge threshold, the detection is no-battery and the process will restart from beginning to detect insertion of the battery. If after the 0.5s period, the voltage does not exceed the recharge voltage threshold, the battery is detected as present and the proper charging phase will start.

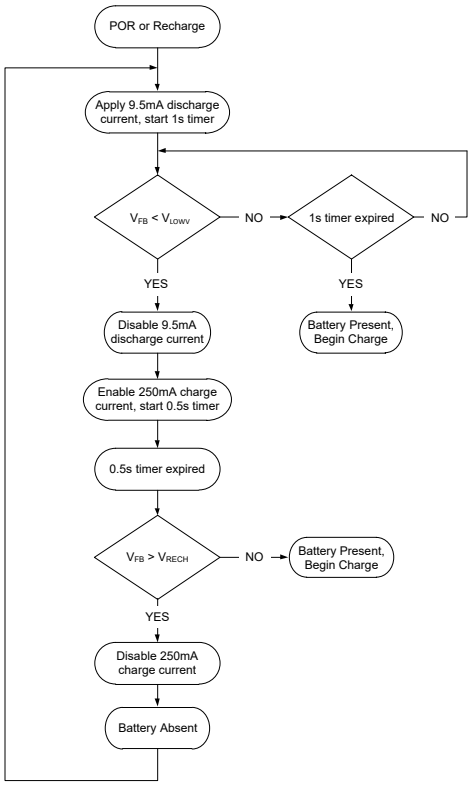


Figure 4. SGM41526A and SGM41527A Battery Detection Flow Chart

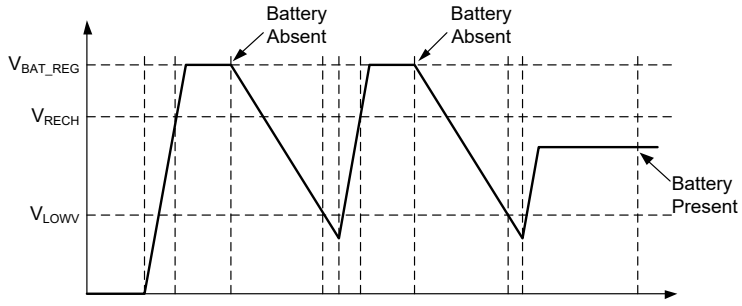


Figure 5. Timing of the Battery Insertion Detection

DETAILED DESCRIPTION (continued)

Note that the total output capacitance that appears parallel to the battery should not be too large such that with the applied sink or charge currents and timing the no-battery voltage changes fast and passes the detection thresholds within 1s or 0.5s periods. Equations 7 and 8 can be used to calculate the maximum output capacitances:

$$C_{MAX} = \frac{I_{DISCH} \times t_{DISCH}}{(4.1V - 2.9V) \times N_{Cell}} \text{ (for SGM41526A)} \quad (7)$$

$$C_{MAX} = \frac{I_{DISCH} \times t_{DISCH}}{(2.03V - 1.46V) \times \left(1 + \frac{R_1}{R_2}\right)} \text{ (for SGM41527A)} \quad (8)$$

where

C_{MAX} = maximum output capacitance.

I_{DISCH} = discharge current.

t_{DISCH} = discharge time.

N_{Cell} = number of cells in the battery.

R_1 and R_2: FB pin feedback resistors from the battery.

Example:

For a 3-cell Li+ charger (12.6V battery voltage regulation), with R_1 = 500kΩ, R_2 = 100kΩ, I_{DISCH} = 9.5mA and t_{DISCH} = 1s, the maximum allowed capacitance is:

$$C_{MAX} = \frac{9.5mA \times 1s}{0.57V \times \left(1 + \frac{500k\Omega}{100k\Omega}\right)} = 2.8mF \quad (9)$$

Therefore, the total capacitance on the battery node should be less than 2800μF.

Battery Short Protection

During charge, if the battery voltage sensed on the SRN pin falls below 2V threshold, the battery is considered in short condition. The charge will quickly stop for a 1ms period followed by a soft-start toward the pre-charge current level to prevent over-current and saturation of the inductor. In battery short condition, the charger operates in nonsynchronous mode.

Battery Over-Voltage Protection

Battery voltage is continuously monitored for over-voltage protection. If the sensed voltage exceeds 104% of the regulation voltage, the converter high-side switch remains off. This protection reacts in one cycle. The over-voltage may occur due to a battery disconnection or load removal. The stored energy in the output capacitors is discharged by sinking a total of 6mA current through SRP and SRN pins to AGND. The charge will be disabled if the over-voltage condition is not cleared for more than 30ms.

Battery Temperature Qualification

Battery temperature is continuously monitored by measuring the voltage between the TS pin and AGND that is sensed by a NTC (negative temperature coefficient) thermistor attached to the battery pack. A resistor divider from VREF is used to adjust the temperature limits. The voltage of TS pin is compared with internal thresholds and charge process will not begin until the TS pin voltage (which indicates battery temperature) is within the V_{LTF} to V_{HTF} window. If during charge the battery get too hot or too cold and temperature goes out of the allowed range, the charge will suspend by turning off PWM switches. The charge resumes automatically if the temperature returns to the allowed window.

Figure 6 illustrates the temperature qualification function and the thresholds for the charge initiation, suspension and recovery.

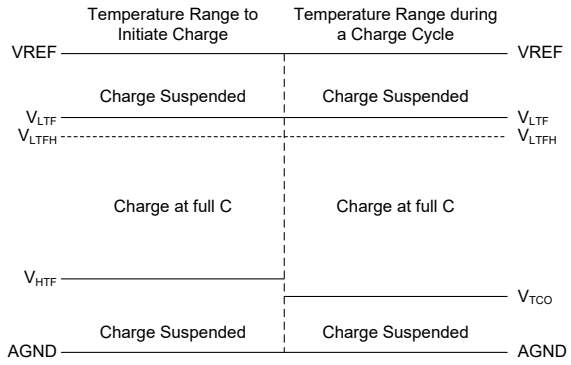


Figure 6. Battery Temperature Qualification Function and Thresholds on the Sensed TS Pin Voltage

The TS pin resistor divider (Figure 7) can be calculated based on the hot and cold temperature levels recommended for the battery by Equation 10 and Equation 11:

$$R_{T2} = \frac{V_{VREF} \times R_{THCOLD} \times R_{THHOT} \times \left(\frac{1}{V_{LTF}} - \frac{1}{V_{TCO}}\right)}{R_{THHOT} \times \left(\frac{V_{VREF}}{V_{TCO}} - 1\right) - R_{THCOLD} \times \left(\frac{V_{VREF}}{V_{LTF}} - 1\right)} \quad (10)$$

$$R_{T1} = \frac{\frac{V_{VREF}}{V_{LTF}} - 1}{\frac{1}{R_{T2}} + \frac{1}{R_{THCOLD}}} \quad (11)$$

DETAILED DESCRIPTION (continued)

Using a 103AT type NTC thermistor in the battery pack and selecting T_{COLD} = 0℃ and T_{HOT} = 45℃ range for Li-Ion or Li-polymer battery, and recalling the NTC resistances at temperature limits from datasheet:

R_{THCOLD} = 27.28kΩ (103AT NTC resistance at 0℃)
R_{THHOT} = 4.911kΩ (103AT NTC resistance at 45℃)

The resistors can be calculated as:

R_{T1} = 5.29kΩ
R_{T2} = 32.12kΩ

The actual temperature range can be calculated based on the selected standard resistor values and NTC actual characteristics.

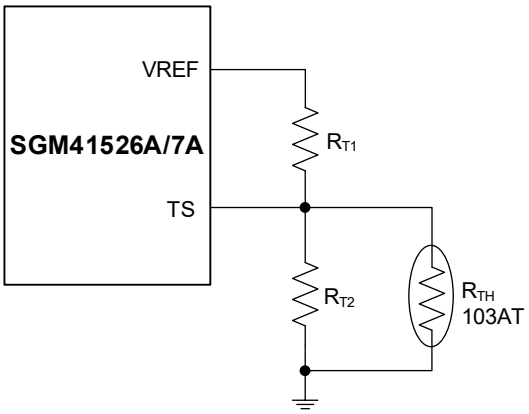


Figure 7. Battery Pack Temperature Sensing Network

MOSFET and Inductor Protection in Short Circuit Condition

The SGM41526A and SGM41527A provide cycle-by-cycle short circuit protection by monitoring the voltage drop across $R_{DS(ON)}$ of the MOSFETs. If a short is detected, the charger will be latched off, which means the Buck converter is disabled but the ACFET will not be turned off, and system is still connected to the adaptor. Latch-off state can only be removed by unplugging and re-plugging the input power (adapter). The LED connected to STAT pin blinks at this condition.

Thermal Regulation and Shutdown

The low thermal impedance of the TQFN package provides good cooling for the silicon. When the junction temperature exceeds +120℃, the thermal regulation is triggered. Then the device will decrease charge current to reduce internal heat generation. Moreover, if the junction temperature exceeds the shutdown level (T_{SHUT} = +150℃), charger is turned off and will not resume until T_J falls below +130℃.

Recovery from Timer Fault

If a charge timer fault occurs, the device recovery process will depend on the battery voltage as follows.

Case 1: If V_{BAT} exceeds the recharge threshold when the time-out fault occurs, the charge will be suspended firstly. When the battery voltage falls below recharge threshold, the battery detection begins again, and then the timer fault is cleared. The fault will also clear by a power-on-reset (POR) or by pulling the ISET voltage below 30mV.

Case 2: If V_{BAT} falls below the recharge threshold when the timer fault occurs, a small charge current is applied to detect the battery removal at first. The small charge current is not removed until V_{BAT} exceeds the recharge threshold. Then the small charge current is disabled. The rest of recovery process is as explained in case 1.

Design of the Inductor, Capacitor and Sense Resistor

For the charger internal compensation, the best stability is achieved if the LC filter resonant frequency (f_O) given in Equation 12 is approximately between 15kHz and 25kHz:

$$f_O = \frac{1}{2\pi\sqrt{LC}} \quad (12)$$

Some typical LC values for various charge currents are given in Table 2.

Table 2. LC Typical Values vs. Designed Charge Current

Charge Current	1A	2A	3A	4A
Output Inductor L	6.8μH	3.3μH	3.3μH	2.2μH
Output Capacitor C	10μF	20μF	20μF	30μF

STAT Charge Status Output

STAT is an open-drain output that indicates the charger status as explained in Table 3. This pin can be used for driving LEDs or informing the host about charge status.

Table 3. STAT Output Pin States

Charge State	STAT Transistor
Charge in Progress (including Recharging)	ON
Charge Completed, Sleep Mode, Charge Disabled	OFF
Charge Suspend, Input Over-Voltage, Battery Over-Voltage, Timer Fault, Battery Absent	BLINK

DETAILED DESCRIPTION (continued)

Device Functional Modes

The SGM41526A and SGM41527A are stand-alone switching chargers and power path selectors. They operate from a qualified adapter or DC supply system. This device is capable of providing dynamic power management (DPM mode) to reduce the input loading by sharing the load with the battery on the peak system demands. Because of DPM capability, the adaptor size and power rating can be reduced effectively for the systems with highly dynamic loads.

The gate drive pins for power path selector switches (ACDRV and CMSRC) control the input NMOS pair, ACFET (Q1) and RBFET (Q2). The nBATDRV pin controls the gate of the battery connection PMOS switch (Q3). If the input (adapter) is qualified, system will be connected to the input by turning Q1 and Q2 on. Otherwise, Q3 will be turned on then the system is powered from battery. Moreover, the battery cannot feed back to the input with power path selection control.

DPM capability is included in the SGM41526A and SGM41527A to limit maximum power taken from the input (adapter) by reducing the charge current when the system power demand is high. Input current is accurately sensed to monitor power usage. Without DPM, the adapter must be designed to provide maximum charge power plus maximum system power. However, with DPM, the adapter can be designed for significantly lower power rating that reduces the size and cost of the adapter.

The SGM41526A and SGM41527A can operate independently. However, some pin settings can be adjusted by an external controller (like ISET or ACSET). This allows the implementation of ″battery learn mode″ for applications with dynamic charging conditions.

Figure 8 shows the typical efficiency of a 4A charger for a 2-cell application.

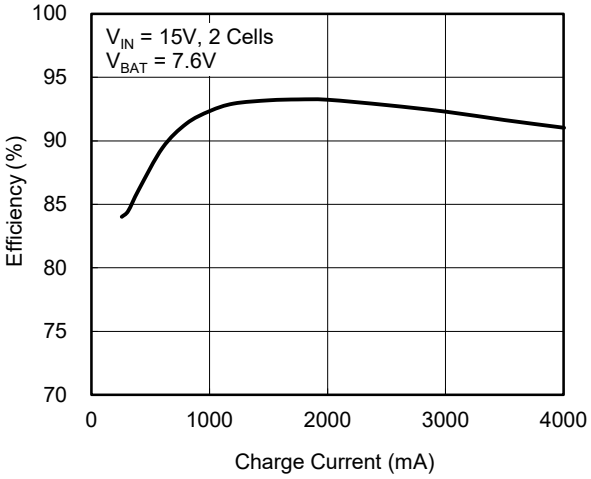


Figure 8. Typical Charge Efficiency

APPLICATION INFORMATION

SGM41526A and SGM41527A can be used in portable applications with up to 4-cell Li-Ion or Li-polymer batteries. The SGM41526A accurately regulates the battery voltage at a fixed 4.2V/cell value (minimum 2 cells) and with low leakage from battery. Number of cells is programmable by CELL pin. For the applications that need custom battery regulation voltage or use only one cell, the SGM41527A can be used. In this variant, the battery regulation voltage is adjustable through the FB pin similar to a conventional voltage regulator. Figure 9 shows a typical application circuit of the SGM41526A with a 2-cell battery (8.4V).

For power input, an adapter or power supply from 4.5V to 22V is needed generally. The minimum voltage range depends on the number of battery cells. Typically, the adapter current rating should be 500mA and higher.

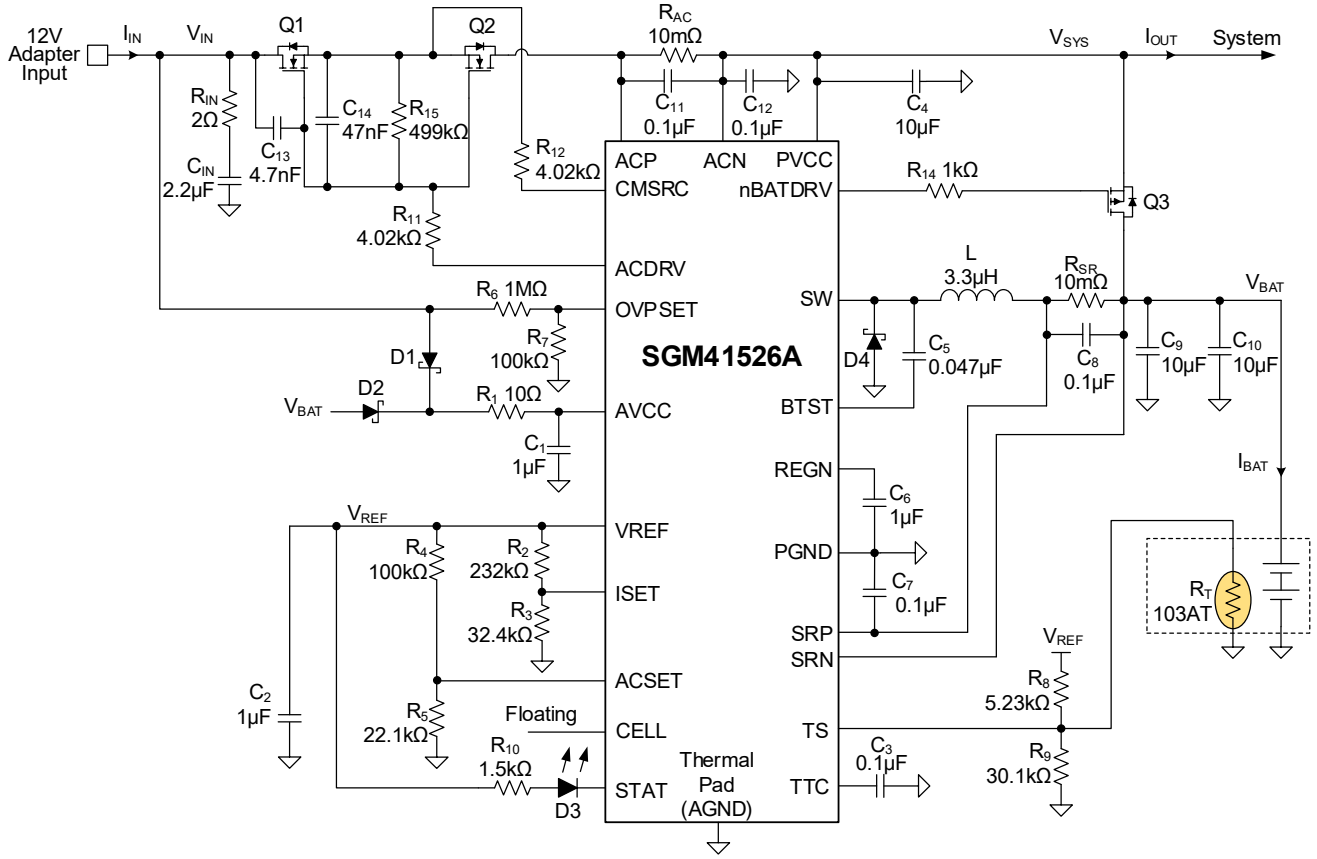
Design Requirements

As an example to explain the design procedure, suppose that a charger is needed with the parameters listed in Table 4.

Table 4. Design Requirements

Parameter	Example Value
Input Voltage Range	4.5V to 22V
Input Current DPM Limit	600mA (MIN)
Battery Voltage	18V (MAX)
Charge Current	4A (MAX)

The maximum battery voltage shows that a 4-cell battery is considered in the design.



NOTE: 12V input, 2-cell battery 8.4V, 2A charge current, 0.2A pre-charge/termination current, 3A DPM current, 17.6V input OVP, 0℃ to 45℃ TS.

Figure 9. Typical SGM41526A Schematic for a 2-Cell Battery Application

APPLICATION INFORMATION (continued)

Inductor Selection

Small inductors and capacitors can be used in this design due to the high switching frequency of the device (f_{SW} = 1.6MHz). The inductor should not saturate at the highest current that occurs at maximum charge current plus half peak value of the ripple current as given in Equation 13:

$$I_{SAT} \geq I_{CHG} + (1/2)I_{RIPPLE} \quad (13)$$

where I_{CHG} is the charging current, and I_{RIPPLE} is the ripple current magnitude (peak-to-peak of the AC component).

Except for light loads, the inductor current is continuous and the I_{RIPPLE} is determined by the following equation:

$$I_{RIPPLE} = \frac{V_{IN} \times D(1-D)}{f_S \times L} \quad (14)$$

where V_{IN} is the input voltage, D = V_{OUT}/V_{IN} is duty cycle, and L is the inductance value.

Usually the highest ripple current is generated when duty cycle is equal to or near 0.5. Inductor current ripple is typically chosen to be 20% to 40% of the full load DC current to get a reasonable compromise between inductor size and AC losses. Higher ripple results in smaller inductor but with lower efficiency. The highest input voltage and charge current ranges should be considered for inductor design. Consider 30% ripple for this design ($I_{RIPPLE} \leq 0.3I_{CHG}$):

$$0.3 \times 4A \geq \frac{22V \times 0.5 \times (1-0.5)}{1.6MHz \times L} \quad (15)$$

Or L ≥ 2.9μH.

The initial tolerance of the commercial inductors is usually quite large (typically 10% - 20% and in some cases as high as 30%). The inductance also drops with higher currents (typically in the order of 20% at maximum current). Therefore, a good margin must be considered for selection of the inductor value by consideration of the initial tolerance, thermal and maximum current drops from the inductor datasheet. For this example, a 3.3μH inductor is considered.

L = 3.3μH (nominal value of the inductor)

The minimum inductor saturation current from Equation 13 is:

$$I_{SAT} \geq 4A + \left(\frac{1}{2}\right) \times 0.3 \times 4A \rightarrow I_{SAT} \geq 4.6A$$

Inductor core type and form factor can be designed based on the required size, loss, magnetic noise coupling, cost, stock availability and reliability considerations.

Input Path Capacitors

The input capacitors carry two types of AC currents: (1) the converter switching ripple currents and (2) the high frequency (HF) transient currents of the switching. High frequency decoupling capacitors are necessary to prevent voltage ringing due to HF currents. Usually some bulk capacitance is needed to avoid large input rail voltage ripples. Typically, a ceramic capacitor placed close to the switching leg (PVCC and PGND) is sufficient to circulate the switching frequency and high frequency AC currents. This capacitor needs to have low ESR and ESL. The capacitor self-resonance frequency should be selected well above switching frequency. Otherwise, it will not be able to bypass HF switching transient currents and large ringing noise may be seen on the PVCC. A combination of smaller size and larger size capacitors may be used for better noise suppression. Stable ceramic capacitors such as X5R or X7R are recommended. All capacitors should be able to carry the peak RMS current of the ripples. Input capacitor ripple current (I_{CIN}) can be calculated from Equation 16:

$$I_{CIN} = I_{CHG} \times \sqrt{D \times (1-D)} \quad (16)$$

The highest ripple occurs at D = 0.5 and the worst case RMS ripple current is $0.5I_{CHG}$ (2A for this example).

Due to the capacitance drop at higher DC voltage bias and aging, a good margin should be considered for selection of the capacitor voltage rating. For a 20V maximum input, a 25V capacitor works. However, a 35V or higher voltage capacitor is recommended. For a high current (3A ~ 4A) charger, a minimum of 20μF input capacitance is recommended. For lower currents (1A or less), 10μF capacitance is sufficient.

Output Capacitor Selection

Applying a charge current with high ripple will deteriorate the battery lifetime and generate extra loss and heat. Therefore, it is important to bypass the inductor ripple using output capacitors and to keep the voltage ripple low, allowing only the DC current to flow and charge the battery. The output capacitors should have enough RMS current rating to carry the worst-case current ripples. The output RMS current (I_{COUT}) can be calculated as:

$$I_{COUT} = \frac{I_{RIPPLE}}{2 \times \sqrt{3}} \approx 0.29 \times I_{RIPPLE} \quad (17)$$

The output ripple is given by Equation 18:

$$\Delta V_O = \frac{V_{OUT}}{8LCf_S^2}\left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (18)$$

APPLICATION INFORMATION (continued)

The ripple can be reduced by decreasing the cut-off frequency of the LC filter ($f_r = \frac{1}{2\pi\sqrt{LC}}$). The SGM41526A and SGM41527A internal loop compensator is designed for a cut-off frequency of 15kHz to 25kHz. Therefore, in order to achieve good loop stability, select the output capacitor such that LC filter cut-off frequency is in the specified range. Stable ceramic capacitors (like X5R or X7R) are recommended with enough margin for the rated voltage (25V or higher). Selecting C_{OUT} = 20μF (two parallel 10μF) will result in f_r = 19.6kHz with the selected L = 3.3μH inductor.

Input Filter Design

Most portable applications must be able to handle hot adapter plug-in and removal. The parasitic line inductance of the adapter and the input capacitors of the charger form a second-order LC circuit that may create a transient over-voltage on the AVCC and damage the device. So careful design of the input filter with proper damping is important to assure the voltage peaks are well below the device limit. A common method is using a high ESR electrolytic input capacitor to damp the over-voltage spike. A TVS Zener diode with high current capability may also be used on the AVCC pin to clamp the transient peaks. If a more flexible and compact solution is needed, the input filter shown in Figure 10 can be used. In this network, R_iC_i filter damps the hot-plug oscillations and limits the over-voltage spikes to a safe level. D_1 provides reverse voltage protection if a reverse polarity adapter is mistakenly connected or when the battery is also feeding AVCC. C_a is the decoupling capacitor of the AVCC that is placed right beside the AVCC and AGND pins. R_aC_a filter provides more damping and reduction of the dv/dt and magnitude of voltage spike. R_a also serves as a current limiter. C_a is typically less than the C_i, so R_i dominates in the total equivalent ESR for damping of hot plug-in spikes. R_i and R_a should have sufficient package size and power rating to dissipate inrush current losses without overheating. A final test is recommended to assure all requirements are satisfied in the worst conditions and to make the necessary adjustments.

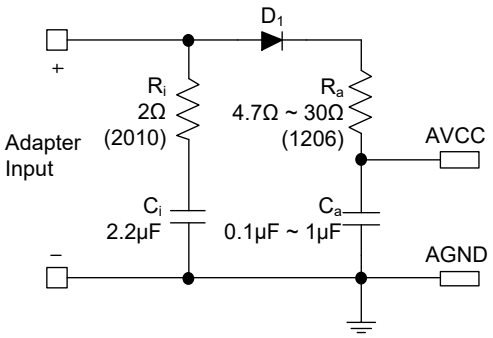


Figure 10. Input Filter

Selecting Input Switch Pair (ACFET and RBFET)

Low $R_{DS(ON)}$, N-type MOSFETs are used for ACFET(Q1) and RBFET(Q2) as shown in Figure 11. Due to the relatively large amount of capacitance on the system power rail, PVCC and charger output, a large inrush current can flow in the switches if it is not managed properly. Slow turn-on of Q1 can reduce the inrush current. MOSFETs with relatively large drain-gate and gate-source parasitic capacitances (C_{GD} and C_{GS}) have slower turn-on time. External capacitors may be used if Q1 turn-on is not slow enough. As an example, external C_{GD} = 4.7nF and C_{GS} = 47nF can be used across Q1. Current and power rating of these switches should be selected with good margin compared to the maximum current from the adapter.

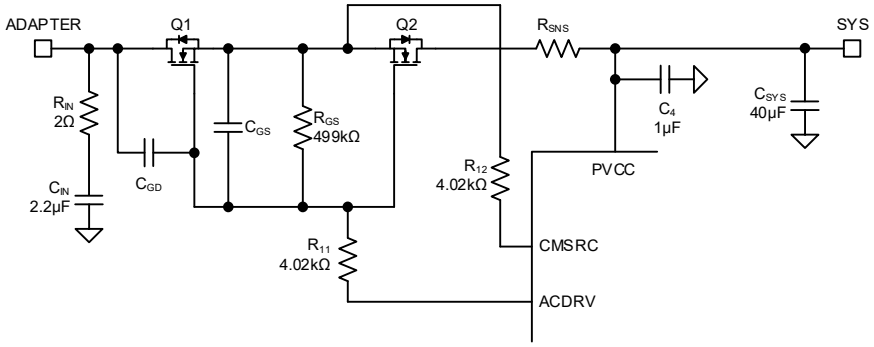
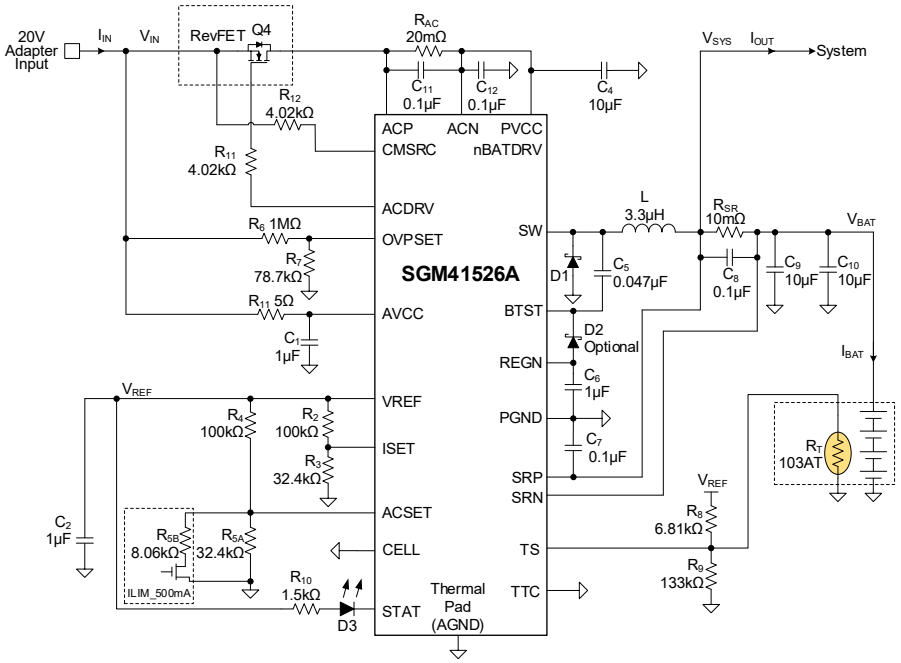


Figure 11. External Capacitors to Slowdown Q1 Turn-On and Limit Inrush Current

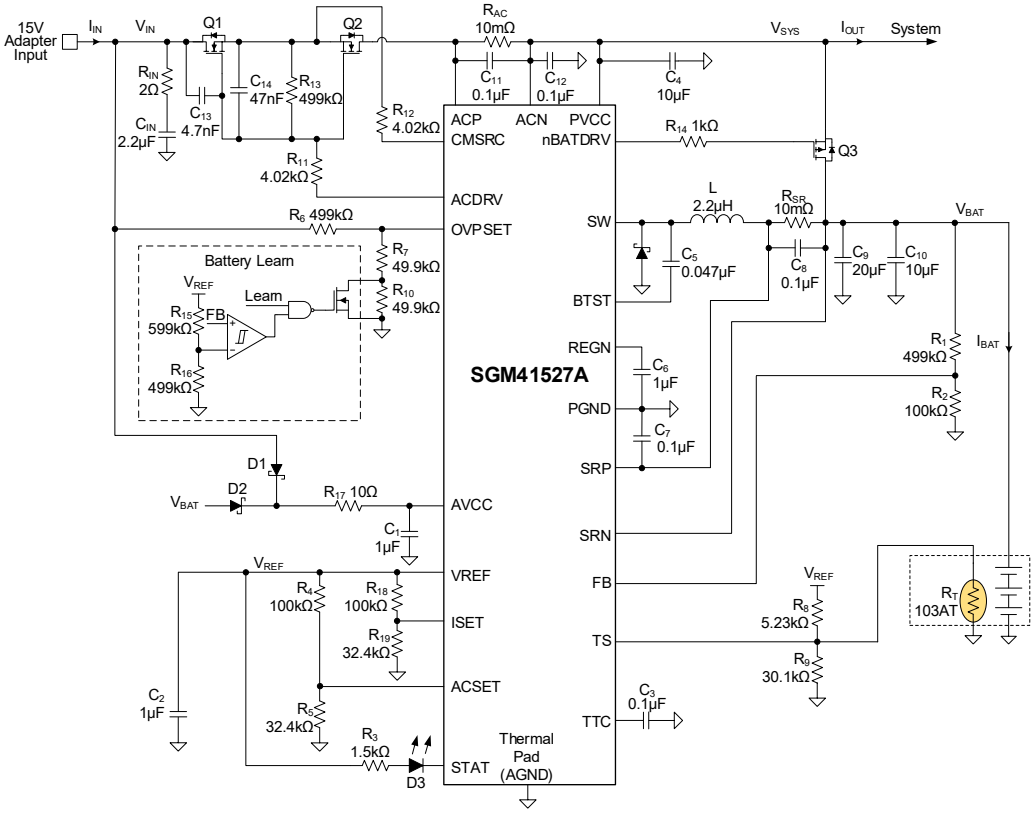
APPLICATION INFORMATION (continued)

Design Examples



NOTE: Adapter input 20V OVP 22V, up to 4A charge current, 0.4A pre-charge current, 2A adapter current or 500mA USB current, 5℃ to 40℃ TS, system connected before sense resistor.

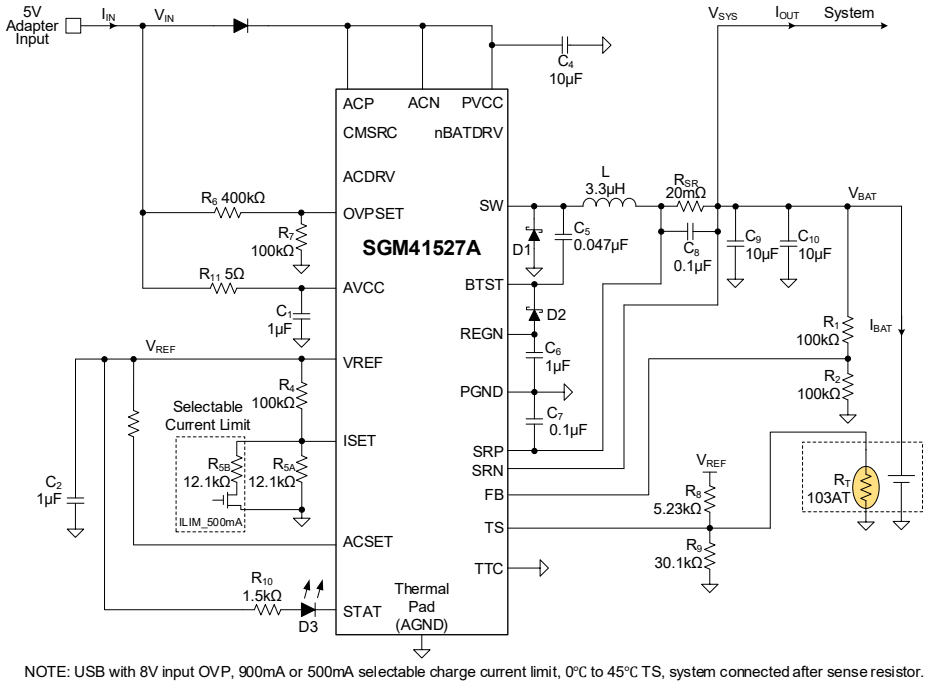
Figure 12. Typical Application Schematic with 4-Cell Unremovable Battery (OVP 20V)



NOTE: 15V input, 3-cell battery 12.6V, 4A charge current, 0.4A precharge/termination current, 4A DPM current, 0℃ to 45℃ TS.

Figure 13. A Typical 3-Cell Application Schematic with Battery Learn Function

APPLICATION INFORMATION (continued)



NOTE: USB with 8V input OVP, 900mA or 500mA selectable charge current limit, 0℃ to 45℃ TS, system connected after sense resistor.

Figure 14. Typical Application Schematic with Single-Cell Unremovable Battery

Layout Guidelines

A good PCB layout is critical for proper operation of the switching circuits. A list of important considerations for SGM41526A and SGM41527A layout design are provided here:

1. The switching node (SW) creates very high frequency noises several times higher than f_{SW} (1.6MHz) due to sharp rise and fall times of the voltage and current in the switches. To reduce the ringing issues and noise generation, it is important to minimize impedance and loop area of the AC current paths. A graphical guideline for the current loops and their frequency content is provided in Figure 15.

2. Input and other decoupling capacitors must be placed as close to the device pin and ground as possible with the shortest copper trace and on the same layer of PCB.

3. Surface area of the SW node should be minimized to reduce capacitive HF noise coupling. Use a short and wide track connection to the inductor on the same layer of PCB. Keep sensitive and high impedance traces away from switching node and trace.

4. Place the charge current-sense resistor right next to the inductor and use the same layer of PCB for routing them to the device amplifier input while keeping them close together and away from high current paths.

Figure 16 shows the proper Kelvin connection of shunt resistors for accurate current sensing. Use decoupling capacitors at the point of connection to the device (between sense traces and between one of them and AGND).

5. Output capacitors should be placed right next to the sense resistor.

6. Keep input and output capacitor ground returns tied together and on the same layer before connecting them to the device PGND. Having all of them connected in a small geometric area right beside the device is highly recommended.

7. Keep AGND separated from PGND and connect them only in a single point under the device body and connect it to the thermal pad. Use AGND copper pour only under the device. A 0Ω resistor can be used for single point connection of AGND and PGND. Make connections to AGND with star geometry.

8. For proper cooling of the device, use several thermal vias connecting the thermal pad pour to the GND plane on the opposite side and other layers of the PCB. Use enough solder for thermal pad connections. Open via holes allow solder to penetrate to the other side and provide low thermal resistance. Apply solder to the opposite side thermal ground for better connection to the vias and better thermal cooling. Thermal ground should not be connected to PGND planes.

9. Remember that vias add some parasitic impedance (resistive/inductive) to the trace. So, it is generally recommended to avoid vias in the sensitive or high frequency paths.

APPLICATION INFORMATION (continued)

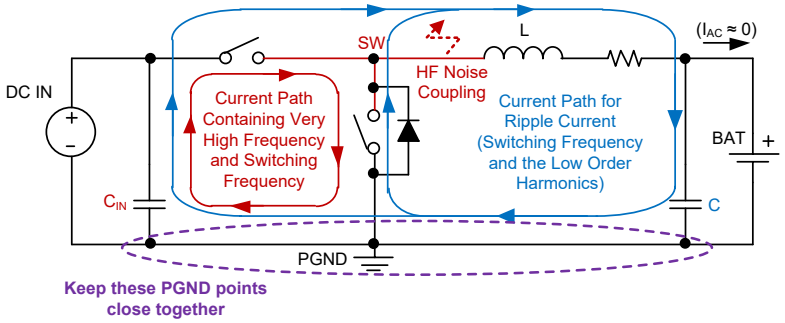


Figure 15. Graphical Representation of the Switching and Transient Current Loops, and Capacitive Noise Coupling from SW Node

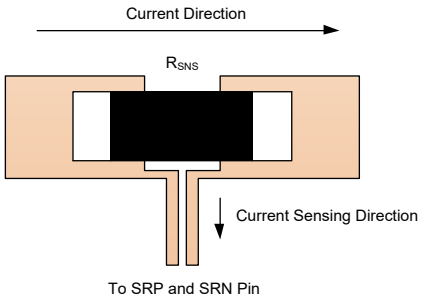


Figure 16. Sensing Resistor PCB Layout

REVISION HISTORY

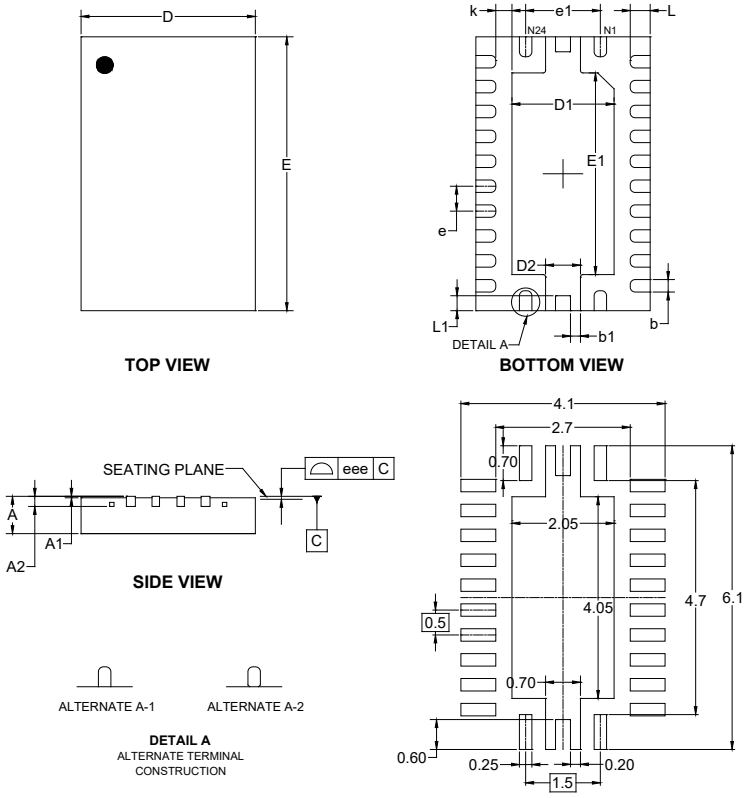
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

January 2026 – REV.A to REV.A.1	**Page**
Corrected Figure 1	1

Changes from Original to REV.A (JULY 2025)	**Page**
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

TQFN-5.5×3.5-24L

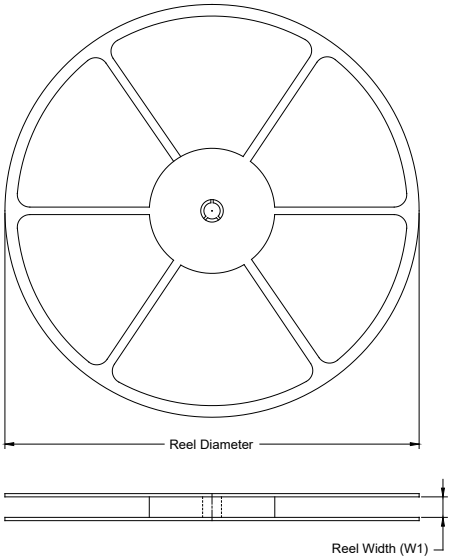


Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	0.700	-	0.800
A1	0.000	-	0.050
A2		0.203 REF	
b	0.200	-	0.300
b1	0.150	-	0.250
D	3.400	-	3.600
D1	1.950	-	2.150
D2	0.600	-	0.800
E	5.400	-	5.600
E1	3.950	-	4.150
e		0.500 BSC	
e1		1.500 BSC	
k		0.325 REF	
L	0.300	-	0.500
L1	0.200	-	0.400
eee		0.080	

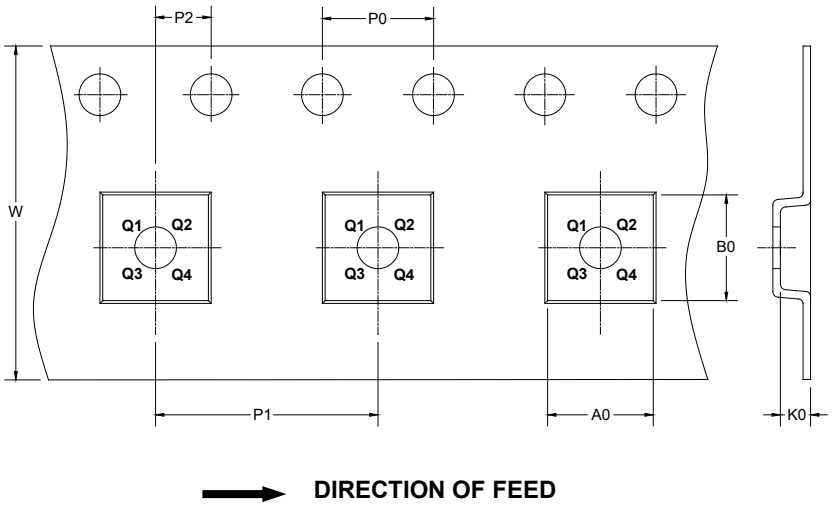
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



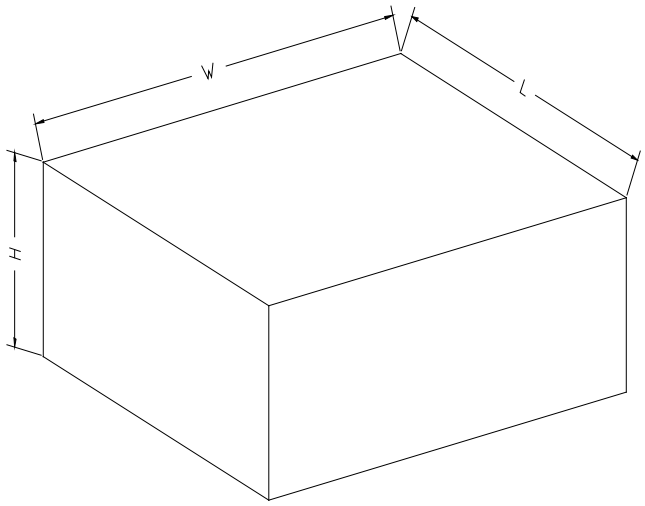
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TQFN-5.5×3.5-24L	13″	12.4	3.80	5.80	1.00	4.0	8.0	2.0	12.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002