

GENERAL DESCRIPTION

The SGM2222 is an ultra-low noise, ultra-high PSRR and low dropout voltage linear regulator for noise-sensitive applications such as RF power supply. It is capable of supplying 200mA output current with typical dropout voltage V_{DROP} of 260mV. The operating input voltage range is from 2V to 20V and output voltage range is from 0V to $(V_{IN} - V_{DROP})$. It requires an output capacitor with an effective capacitance of 2.2 μ F or larger to ensure stability.

The SGM2222 uses a high-precision 100 μ A current source as the reference and a high performance buffer with unit gain for output voltage. Therefore, the SGM2222 supports parallel connection for better noise performance as well as output current capability. And its PSRR, bandwidth, transient response and noise performance are basically not affected by the output voltage.

The SGM2222 opens multiple programmable pins for users to program the current limit, Enable/UVLO threshold, and Power-Good threshold on demand. It also supports fast start-up function. In addition, the SGM2222 integrates the reverse voltage protection, the reverse current protection, the internal current limit protection with foldback and thermal overload protection.

The SGM2222 is available in Green MSOP-10 (Exposed Pad) and TDFN-3 \times 3-10L packages. It operates over an operating temperature range of -40 $^{\circ}$ C to +125 $^{\circ}$ C.

APPLICATIONS

- Radio Frequency (RF) Power Supply
- Power Noise Sensitive Equipment
- Precision Measuring Instruments
- Medical Equipment
- Precision Power Supply
- Filter for Switching Power Supply
- High Speed/High-Precision ADC/DAC

FEATURES

- **Wide Input Voltage Range: 2V to 20V**
- **Enable Pin Accept Voltages Higher than the Supply Voltage and up to 20V**
- **Output Voltage Range: 0V to $(V_{IN} - V_{DROP})$**
- **SET Pin Current Accuracy: $\pm 1\%$ at +25 $^{\circ}$ C**
- **Output Current: 200mA**
- **Low Dropout Voltage: 260mV (TYP)**
- **Ultra-Low RMS Noise: 0.9 μ V_{RMS} (10Hz to 100kHz)**
- **Ultra-Low Spot Noise: 2.6nV/ $\sqrt{\text{Hz}}$ at 10kHz**
- **Ultra-High PSRR: 83dB (TYP) at 1MHz**
- **Optimizable Noise and PSRR through a Single Capacitor**
- **Programmable Output Voltage through a Single Resistor**
- **Programmable Current Limit**
- **Programmable Power Good Threshold**
- **Fast Start-Up Function**
- **Programmable Enable/UVLO Threshold**
- **Parallelable for Better Noise Performance and Current Capability**
- **Current Limit Foldback Protection**
- **Reverse Voltage and Reverse Current Protection**
- **-40 $^{\circ}$ C to +125 $^{\circ}$ C Operating Temperature Range**
- **Available in Green MSOP-10 (Exposed Pad) and TDFN-3 \times 3-10L Packages**

TYPICAL APPLICATION

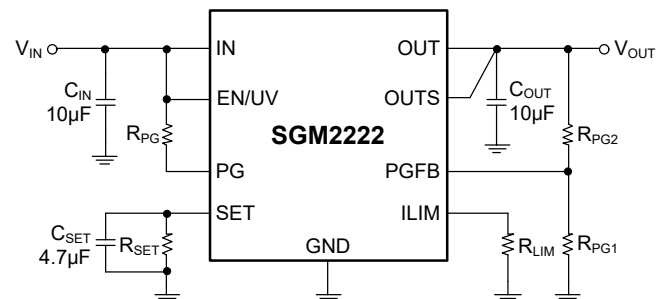


Figure 1. Typical Application Circuit

PACKAGE/ORDERING INFORMATION

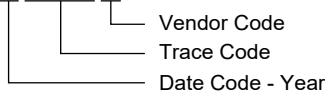
MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM2222	MSOP-10 (Exposed Pad)	-40°C to +125°C	SGM2222XPMS10G/TR	SGM2222 XPMS10 XXXXX	Tape and Reel, 4000
SGM2222	TDFN-3×3-10L	-40°C to +125°C	SGM2222XTD10G/TR	SGM 2222D XXXXX	Tape and Reel, 4000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.

MSOP-10 (Exposed Pad)/TDFN-3×3-10L

XXXXX



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

IN, EN/UV, PGFB to GND.....	±22V
PG, SET, ILIM, OUT, OUTS to GND	-0.3V to 22V
IN to EN/UV	±22V
IN to OUT.....	±22V
IN to OUTS	±22V
OUT to OUTS	±22V
Package Thermal Resistance	
MSOP-10 (Exposed Pad), θ_{JA}	40.1°C/W
MSOP-10 (Exposed Pad), θ_{JB}	16.4°C/W
MSOP-10 (Exposed Pad), $\theta_{JC(TOP)}$	45.2°C/W
MSOP-10 (Exposed Pad), $\theta_{JC(BOT)}$	1.5°C/W
TDFN-3×3-10L, θ_{JA}	37.1°C/W
TDFN-3×3-10L, θ_{JB}	13.5°C/W
TDFN-3×3-10L, $\theta_{JC(TOP)}$	41.4°C/W
TDFN-3×3-10L, $\theta_{JC(BOT)}$	1.1°C/W
Junction Temperature.....	+150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 10s).....	+260°C
ESD Susceptibility ⁽¹⁾⁽²⁾	
HBM.....	±5000V
CDM	±1000V

NOTES:

1. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.
2. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

RECOMMENDED OPERATING CONDITIONS

Input Voltage Range.....	2V to 20V
Enable Input Voltage Range.....	0V to 20V
Input Effective Capacitance, C_{IN}	2.2µF (MIN)
Output Effective Capacitance, C_{OUT}	2.2µF to 200µF
Operating Junction Temperature Range	-40°C to +125°C

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

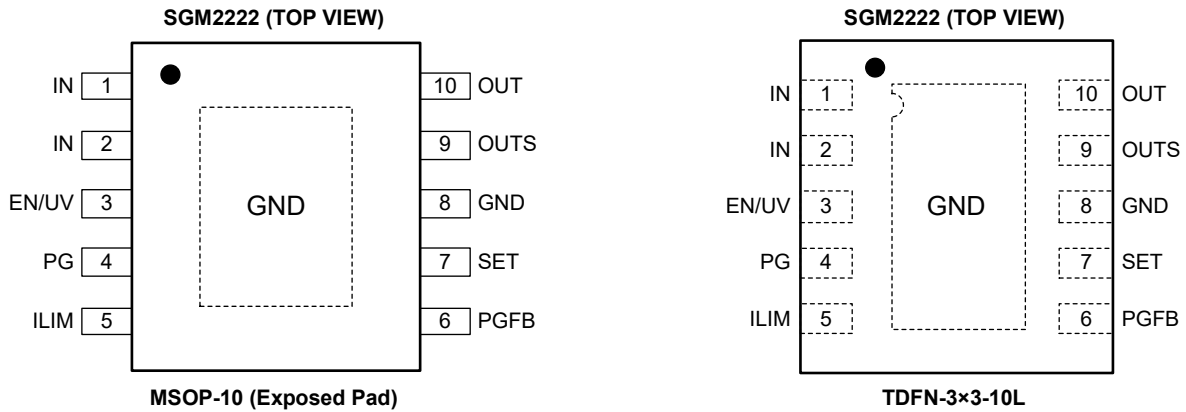
ESD SENSITIVITY CAUTION

This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATIONS



PIN DESCRIPTION

PIN	NAME	FUNCTION
1, 2	IN	Input Voltage Pin. It is recommended to use a 4.7µF or larger ceramic capacitor from IN pin to ground to get good power supply decoupling. The SGM2222 has reverse voltage protection function, which means that even if the GND, OUT or OUTS voltage is higher than the IN voltage, the SGM2222 can remain undamaged. Moreover, the SGM2222 also has reverse current protection to prevent current flow from the output to the input.
3	EN/UV	Enable and Input Supply Under-voltage Lockout (UVLO) Threshold $V_{EN/UV}$ Set Pin. Drive the EN/UV pin low to turn off the SGM2222 and the output will be pulled low by a 1.6mA current. Drive the EN/UV pin high to turn on the SGM2222. Driving the EN pin with a voltage higher than the IN voltage is allowed. The EN/UV pin programs the $V_{EN/UV}$ by adding a resistive divider between IN, EN/UV and GND pins. $V_{EN/UV} = 1.23V (TYP) \times (1 + R_{EN2} / R_{EN1})$, where R_{EN1} is the resistor between the EN/UV pin and the GND pin, and R_{EN2} is the resistor between the IN pin and the EN/UV pin. The EN/UV pin cannot float. Connect it to the IN pin if not used.
4	PG	Power-Good Indicator Output Pin. An open-drain, active-high output that indicates the OUT pin status. The PG voltage is low when the PGFB voltage is below 300mV (TYP). Additionally, the PG voltage is also pulled low when the SGM2222 is in disabled, thermal shutdown or UVLO. The PG pin can float if not in use.
5	ILIM	Current limit Setting Pin. The ILIM pin programs the external current limit threshold I_{EXT_LIMIT} by adding a resistor R_{LIMIT} between ILIM and GND pins. $I_{EXT_LIMIT} = 125mA \times k\Omega / R_{LIMIT}$, where $125mA \times k\Omega$ is the programming scale factor. The ILIM pin can be used as a current monitoring pin, as the current sourced from it is proportional to the output current in a ratio of approximately 1:400. The ILIM pin cannot float. Connect it to the GND pin if not used.
6	PGFB	Power Good Feedback Pin. The PGFB pin programs the power good threshold V_{PGFB} by adding a resistive divider between OUT, PGFB and GND pins. $V_{PGFB} = 300mV (TYP) \times (1 + R_{PG2} / R_{PG1})$, where R_{PG1} is the resistor between the PGFB pin and the GND pin, and R_{PG2} is the resistor between the OUT pin and the PGFB pin. The fast start-up function is active when the PGFB voltage is below 300mV (TYP). The PGFB pin cannot float. Connect it to the IN pin if not used.
7	SET	Output Voltage Setting Pin. The SET pin programs the output voltage V_{OUT} by adding a resistor R_{SET} between SET and GND pins. $V_{OUT} = R_{SET} \times I_{SET}$, where $I_{SET} = 100\mu A (TYP)$. A capacitor C_{SET} between SET and GND pins can improve PSRR, transient response and noise performance, but it will increase start-up time.
8	GND	Ground Pin.
9	OUTS	Output Sense Pin. The OUTS pin supports the Kelvin sense connection at the output. To achieve the expected transient response, phase/gain margin, and PSRR performance, Kelvin connect OUTS pin directly to the OUT side of out capacitor C_{OUT} , while connect the GND sides of the C_{SET} and C_{OUT} directly. And reduce the distance between the GND sides of C_{IN} and C_{OUT} . In addition, the direct connection of the OUTS pin and the OUT pin does not affect the normal function of the regulator.
10	OUT	Output Pin. It is recommended to use a ceramic capacitor with effective capacitance in the range of 2.2µF to 200µF to ensure stability. This ceramic capacitor should be placed as close as possible to OUT pin.
Exposed Pad	GND	Exposed Pad. Connect it to GND internally. Connect it to a large ground plane to maximize thermal performance. This pad is not an electrical connection point.

FUNCTIONAL BLOCK DIAGRAM

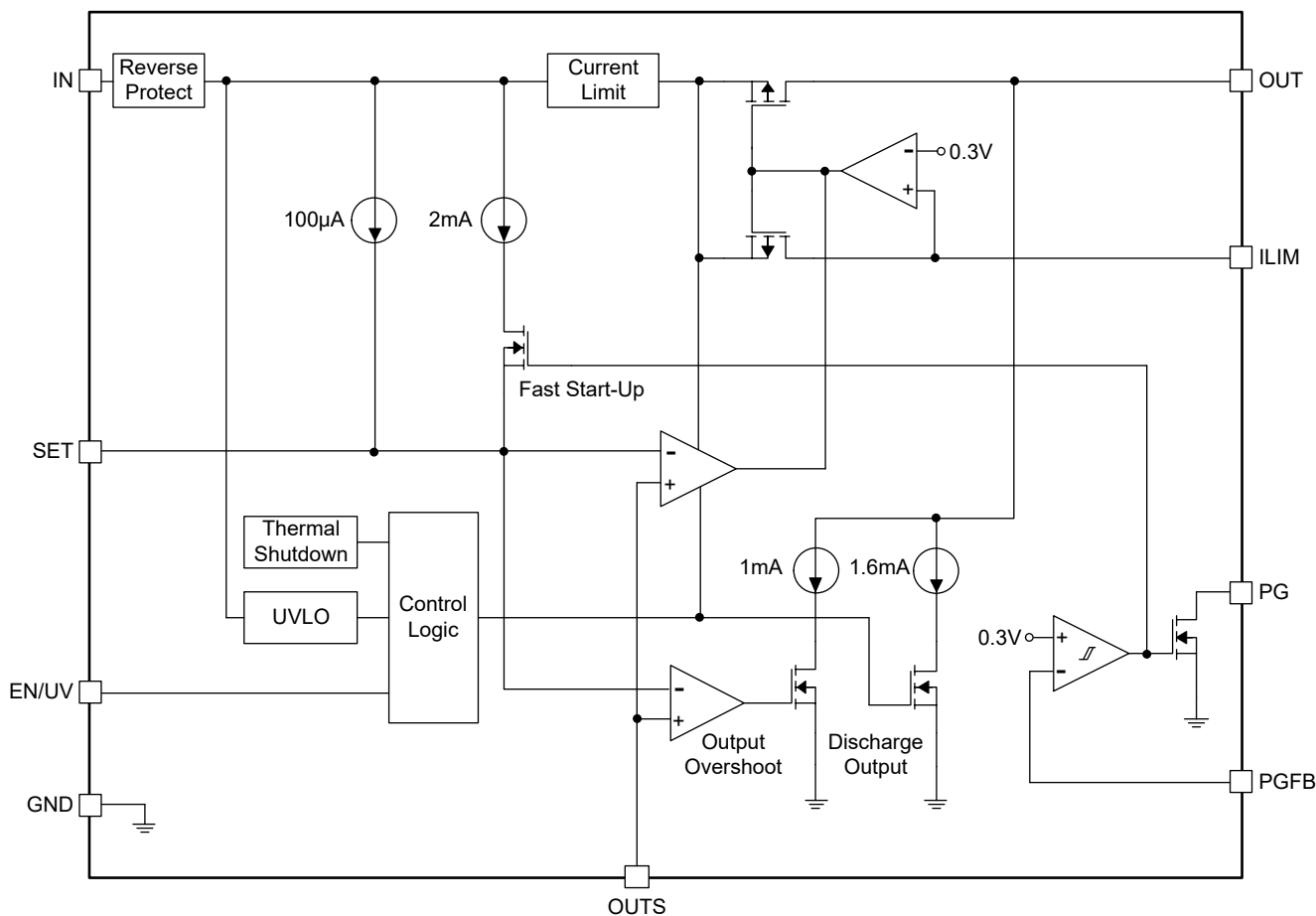


Figure 2. Block Diagram

ELECTRICAL CHARACTERISTICS

($C_{IN} = 4.7\mu\text{F}$, $C_{OUT} = 4.7\mu\text{F}$, OUTS pin connects directly to the OUT pin. $T_J = -40^\circ\text{C}$ to $+125^\circ\text{C}$, typical values are at $T_J = +25^\circ\text{C}$, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	
Input Supply Voltage Range	V_{IN}		2		20	V	
Output Voltage Range	V_{OUT}		0		$V_{IN} - V_{DROP}$	V	
Input Supply UVLO	V_{UVLO}	IN rising		1.78	2	V	
Input Supply UVLO Hysteresis	V_{HYS}	V_{UVLO} hysteresis		40		mV	
SET Pin Current	I_{SET}	$V_{IN} = 2\text{V}$, $V_{OUT(NOM)} = 1.2\text{V}$, $I_{OUT} = 1\text{mA}$, $T_J = +25^\circ\text{C}$	99	100	101	μA	
		$2\text{V} < V_{IN} < 20\text{V}$, $0\text{V} < V_{OUT(NOM)} < 18\text{V}$, $1\text{mA} < I_{OUT} < 200\text{mA}$ ⁽¹⁾	98	100	102	μA	
Fast Start-Up Set Pin Current	I_{SET_FAST}	$V_{PGFB} = 290\text{mV}$, $V_{IN} = 2.8\text{V}$, $V_{SET} = 1.2\text{V}$		2		mA	
Output Offset Voltage	V_{OS} ($V_{OUT} - V_{SET}$)	$V_{IN} = 2\text{V}$, $V_{OUT(NOM)} = 1.2\text{V}$, $I_{OUT} = 1\text{mA}$, $T_J = +25^\circ\text{C}$	-1		1	mV	
		$2\text{V} < V_{IN} < 20\text{V}$, $0\text{V} < V_{OUT(NOM)} < 18\text{V}$, $1\text{mA} < I_{OUT} < 200\text{mA}$ ⁽¹⁾	-1.8		1.8		
Line Regulation	$\Delta I_{SET}/\Delta V_{IN}$	$V_{IN} = 2\text{V}$ to 20V , $V_{OUT(NOM)} = 1.2\text{V}$, $I_{OUT} = 1\text{mA}$		1	5	nA/V	
Line Regulation	$\Delta V_{OS}/\Delta V_{IN}$	$V_{IN} = 2\text{V}$ to 20V , $V_{OUT(NOM)} = 1.2\text{V}$, $I_{OUT} = 1\text{mA}$		0.35	3	$\mu\text{V}/\text{V}$	
Load Regulation	ΔI_{SET_LOAD}	$V_{IN} = 2\text{V}$, $V_{OUT(NOM)} = 1.2\text{V}$, $I_{OUT} = 1\text{mA}$ to 200mA		3.5	150	nA	
Load Regulation	ΔV_{OS_LOAD}	$V_{IN} = 2\text{V}$, $V_{OUT(NOM)} = 1.2\text{V}$, $I_{OUT} = 1\text{mA}$ to 200mA		0.01	0.5	mV	
Change in I_{SET} with V_{SET}	ΔI_{SET_VSET}	$V_{IN} = 20\text{V}$, $I_{OUT} = 1\text{mA}$	$V_{SET} = 1.2\text{V}$ to 18V	5	100	nA	
			$V_{SET} = 0\text{V}$ to 1.2V	120	1000	nA	
Change in V_{OS} with V_{SET}	ΔV_{OS_VSET}	$V_{IN} = 20\text{V}$, $I_{OUT} = 1\text{mA}$	$V_{SET} = 1.2\text{V}$ to 18V	0.03	0.2	mV	
			$V_{SET} = 0\text{V}$ to 1.2V	0.04	0.5	mV	
Dropout Voltage	V_{DROP}	$V_{IN} = V_{OUT(NOM)}$, $R_{SET} = 33\text{k}\Omega$	$I_{OUT} = 1\text{mA}$	195	240	mV	
			$I_{OUT} = 50\text{mA}$	200	260	mV	
			$I_{OUT} = 150\text{mA}$	200	270	mV	
			$I_{OUT} = 200\text{mA}$	260	420	mV	
Internal Current Limit ⁽²⁾	I_{LIMIT}	$V_{OUT} = 0\text{V}$, $R_{LIMIT} = 0\Omega$	$V_{IN} = 5\text{V}$	200	275	350	mA
			$V_{IN} = 13\text{V}$	200	285	370	
			$V_{IN} = 20\text{V}$	90	150	220	
Programmable Current Limit	I_{LIMIT_EXT}	Programming Scale Factor: $2\text{V} < V_{IN} < 20\text{V}$		125		$\text{mA} \times \text{k}\Omega$	
		$V_{IN} = 2\text{V}$, $V_{OUT} = 0\text{V}$, $R_{LIMIT} = 0.625\text{k}\Omega$	170	200	230	mA	
		$V_{IN} = 2\text{V}$, $V_{OUT} = 0\text{V}$, $R_{LIMIT} = 2.5\text{k}\Omega$	40	50	60		
GND Pin Current	I_{GND}	$V_{IN} = V_{OUT(NOM)} + 1\text{V}$	$I_{OUT} = 0\text{mA}$	2	3.5	mA	
			$I_{OUT} = 200\text{mA}$	5.5	7		
Shutdown Current	I_{SHDN}	$V_{EN/UV} = 0\text{V}$, $V_{IN} = 20\text{V}$		2.8	20	μA	
Reverse Input Current	$I_{REV-INPUT}$	$V_{IN} = -20\text{V}$, $V_{EN/UV} = 0\text{V}$, $V_{OUT} = 0\text{V}$, $V_{SET} = 0\text{V}$		0.2	20	μA	
Reverse Output Current	$I_{REV-OUTPUT}$	$V_{IN} = 0\text{V}$, $V_{EN/UV} = 0\text{V}$, $V_{OUT} = 20\text{V}$, SET = open		8	35	μA	
EN/UV Pin Threshold	$V_{EN/UV}$	EN/UV rising, $V_{IN} = 2\text{V}$	1	1.23	1.35	V	
EN/UV Pin Hysteresis	$\Delta V_{EN/UV}$	$V_{EN/UV}$ hysteresis, $V_{IN} = 2\text{V}$		180		mV	
EN/UV Pin Current	$I_{EN/UV}$	$V_{EN/UV} = 0\text{V}$, $V_{IN} = 20\text{V}$	-150	3		nA	
		$V_{EN/UV} = 1.24\text{V}$, $V_{IN} = 20\text{V}$		1	3	μA	
		$V_{EN/UV} = 20\text{V}$, $V_{IN} = 0\text{V}$		6.5	30	μA	

ELECTRICAL CHARACTERISTICS (continued)

($C_{IN} = 4.7\mu\text{F}$, $C_{OUT} = 4.7\mu\text{F}$, OUTS pin connects directly to the OUT pin. $T_J = -40^\circ\text{C}$ to $+125^\circ\text{C}$, typical values are at $T_J = +25^\circ\text{C}$, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Start-Up Time	t_{STR}	$V_{IN} = 6\text{V}$, $V_{OUT(NOM)} = 5\text{V}$, $I_{OUT} = 200\text{mA}$, from assertion of $V_{EN/UV}$ to $V_{OUT} = 90\% \times V_{OUT(NOM)}$	$C_{SET} = 0.47\mu\text{F}$, $V_{PGFB} = 6\text{V}$	72		ms
			$C_{SET} = 4.7\mu\text{F}$, $V_{PGFB} = 6\text{V}$	720		
			$C_{SET} = 4.7\mu\text{F}$, $R_{PG1} = 50\text{k}\Omega$, $R_{PG2} = 700\text{k}\Omega$ (with fast start-up to $90\% \times V_{OUT}$)	13		
PGFB Trip Point	V_{PGFB}	PGFB rising	282	300	318	mV
PGFB Hysteresis	ΔV_{PGFB}	PGFB hysteresis		45		mV
PGFB Pin Current	I_{PGFB}	$V_{IN} = 2\text{V}$, $V_{PGFB} = 300\text{mV}$		2	500	nA
PG Output Low Voltage	$V_{PG(LO)}$	$I_{PG} = 100\mu\text{A}$, $V_{PGFB} = 0\text{V}$		30	100	mV
PG Leakage Current	$I_{PG(LKG)}$	$V_{PG} = 20\text{V}$, $V_{PGFB} = V_{IN}$		0.05	1.5	μA
Minimum Load Required	$I_{OUT(MIN)}$	$V_{OUT} < 1\text{V}$	10			μA
Discharge Current	I_{DISC}	$V_{OUT} = 3.3\text{V}$, $V_{IN} = 20\text{V}$, $V_{EN/UV} = 0\text{V}$		1.6		mA
Power Supply Rejection Ratio	PSRR	$V_{IN} = 5\text{V}$, $V_{OUT(NOM)} = 3.3\text{V}$, $I_{OUT} = 50\text{mA}$, $C_{OUT} = 10\mu\text{F}$, $C_{SET} = 4.7\mu\text{F}$	$f = 120\text{Hz}$	120		dB
			$f = 10\text{kHz}$	107		
			$f = 100\text{kHz}$	87		
			$f = 1\text{MHz}$	83		
Output Voltage Noise	e_n	$I_{OUT} = 200\text{mA}$, $V_{OUT(NOM)} = 3.3\text{V}$, $C_{SET} = 4.7\mu\text{F}$, $f = 10\text{Hz}$ to 100kHz		0.9		μV_{RMS}
Thermal Shutdown Temperature	T_{SHDN}	T_J rising		165		$^\circ\text{C}$
Thermal Shutdown Hysteresis	ΔT_{SHDN}	Hysteresis		20		$^\circ\text{C}$

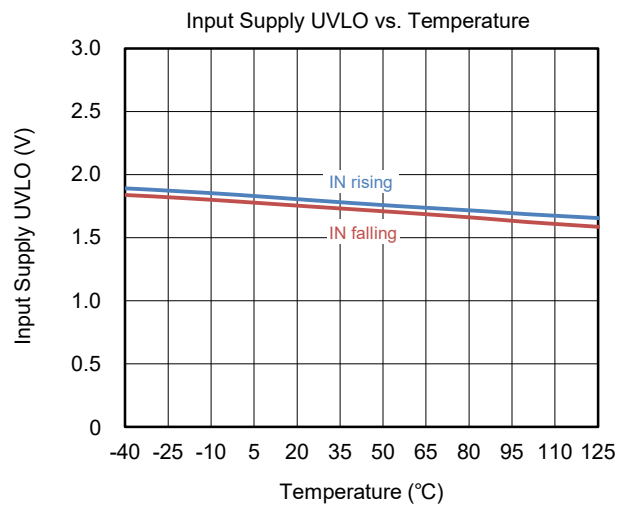
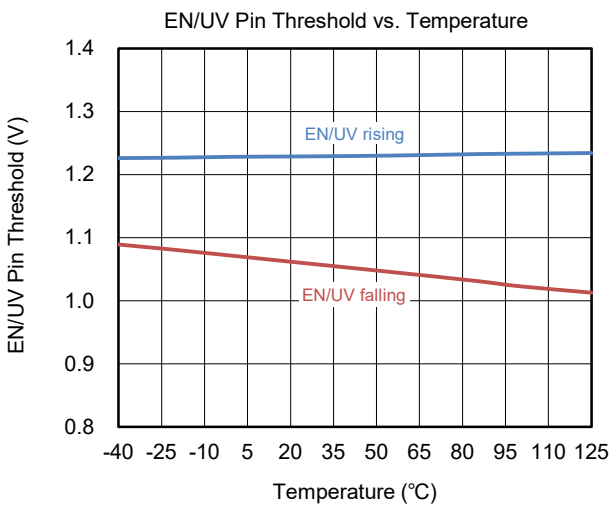
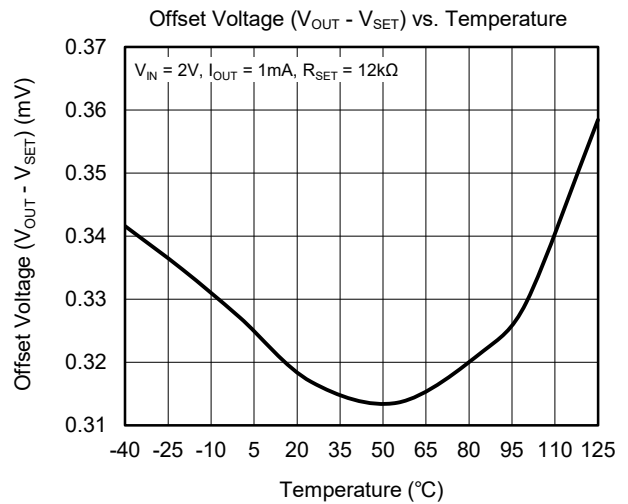
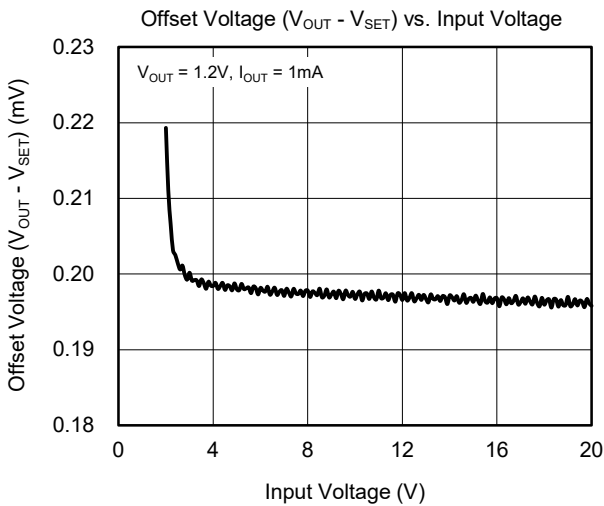
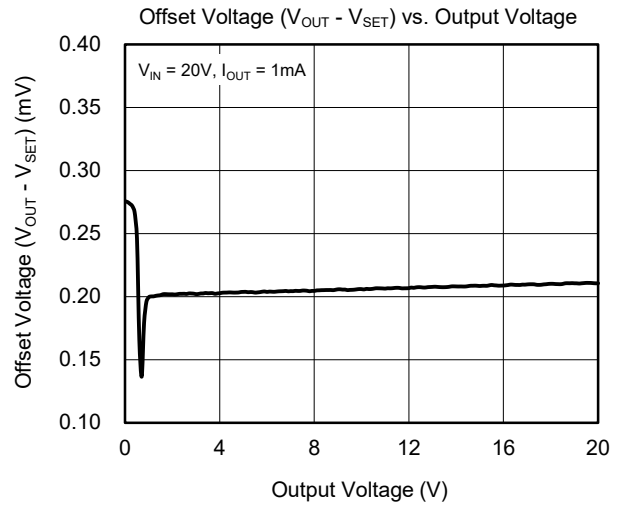
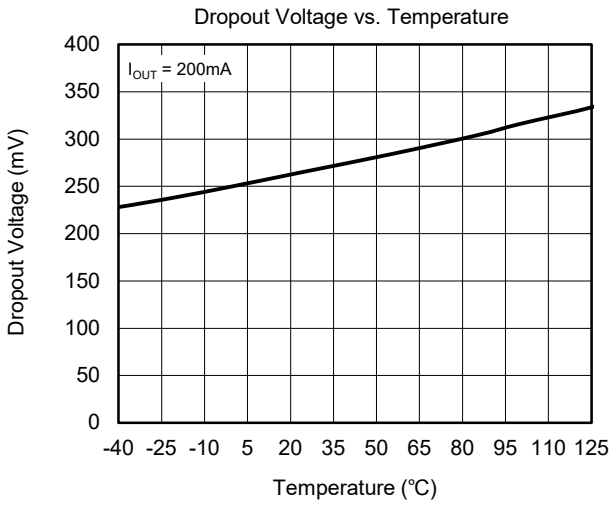
NOTES:

1. The SGM2222 integrates the current limit foldback function. When $(V_{IN} - V_{OUT}) > 13\text{V}$, the output current is restricted to protect the regulator. If at maximum output current during operation, the input voltage range must be limited. If the maximum input voltage is reached in operation, restrict the output current range.

2. The internal current limit includes the current limit foldback.

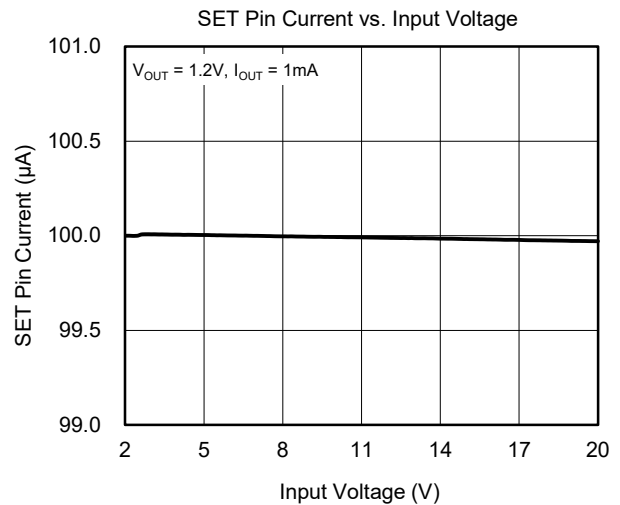
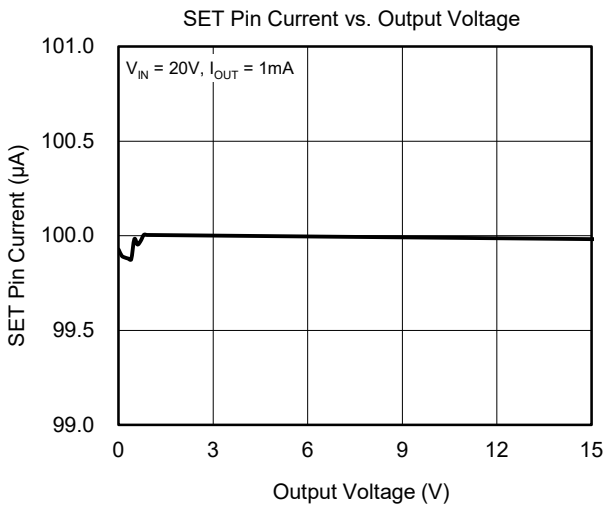
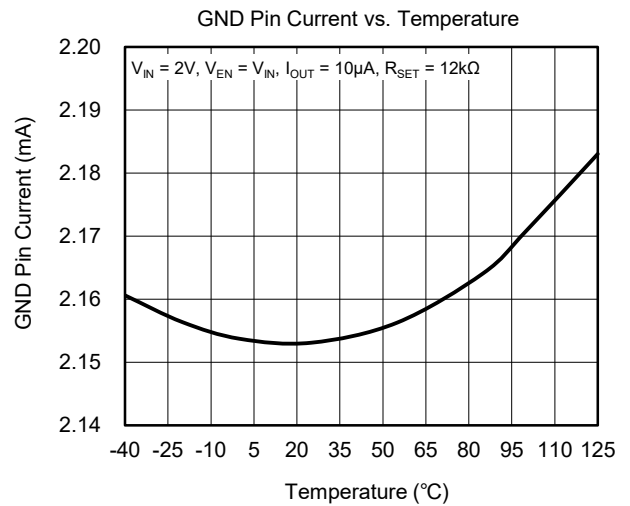
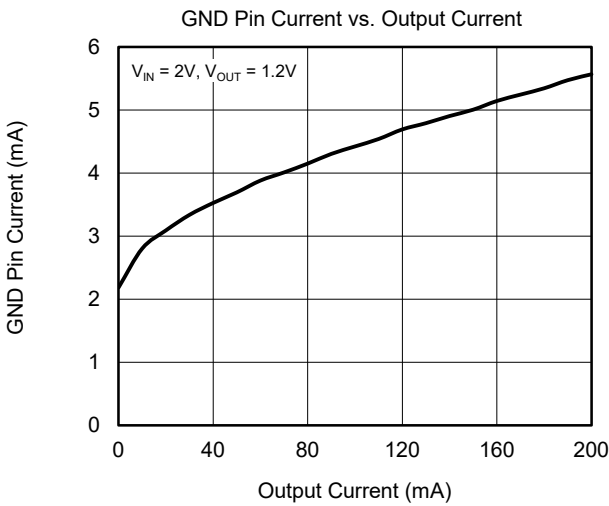
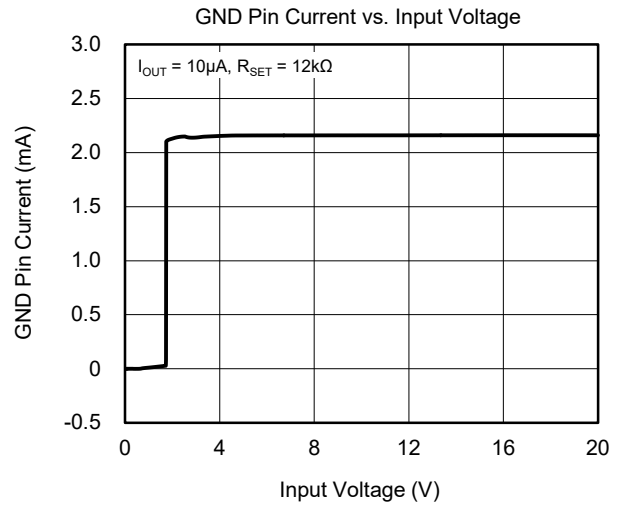
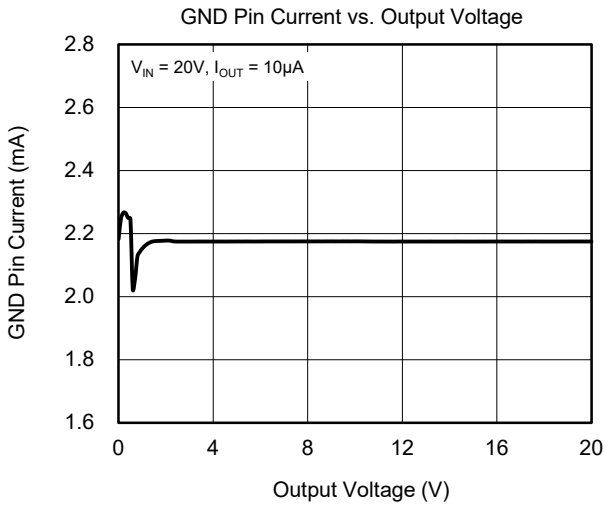
TYPICAL PERFORMANCE CHARACTERISTICS

$T_J = +25^\circ\text{C}$, $C_{OUT} = 4.7\mu\text{F}$, $R_{SET} = 33\text{k}\Omega$, unless otherwise noted.



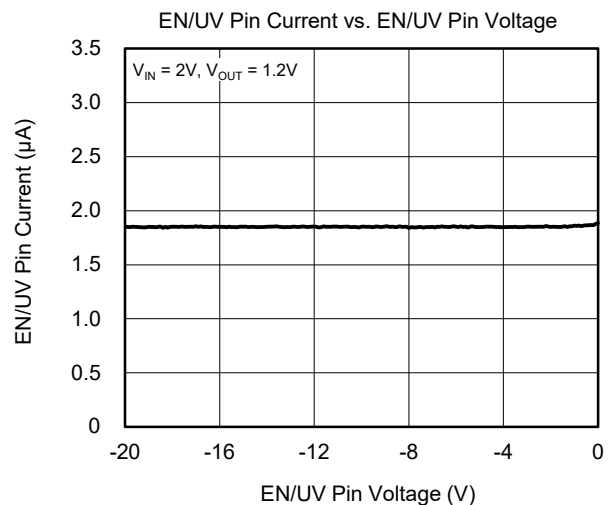
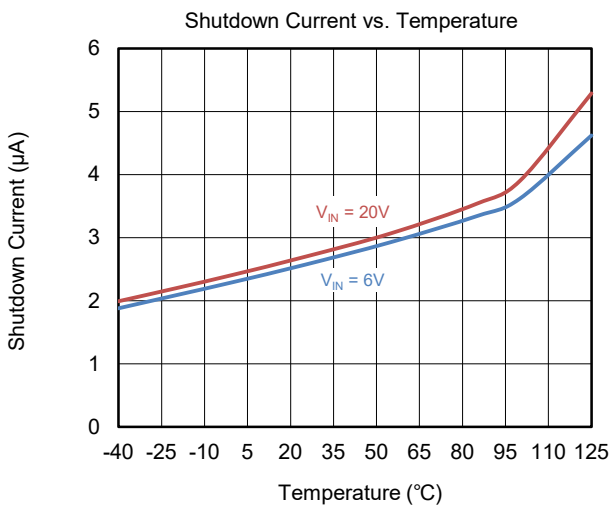
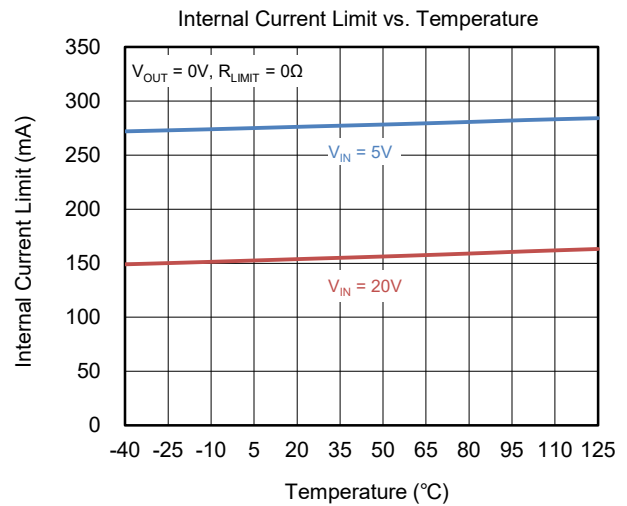
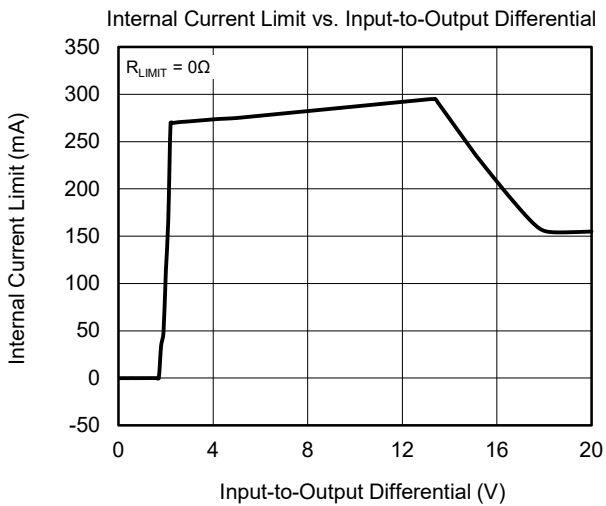
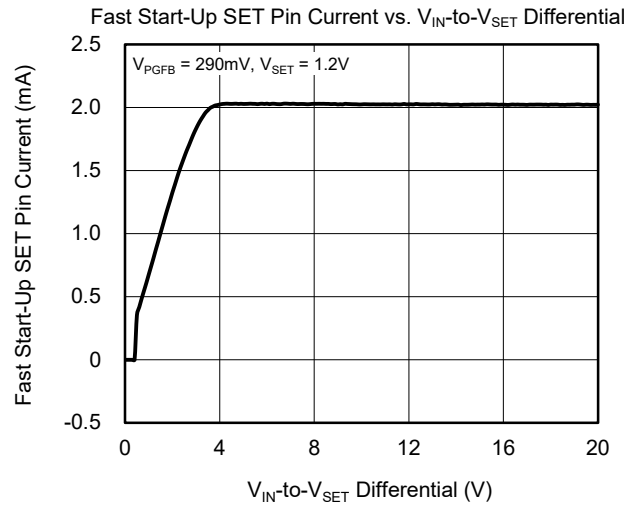
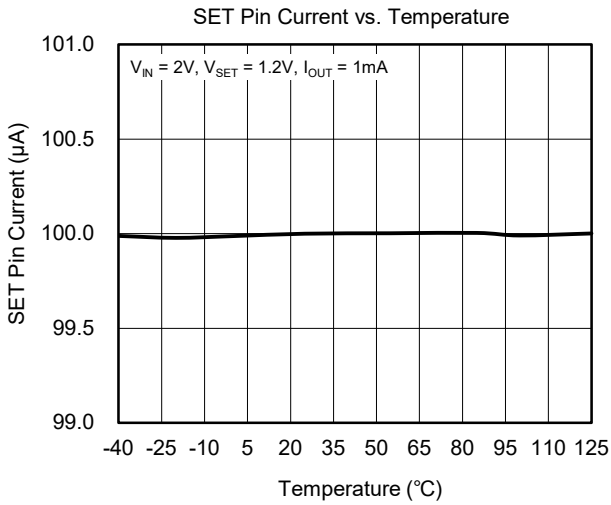
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

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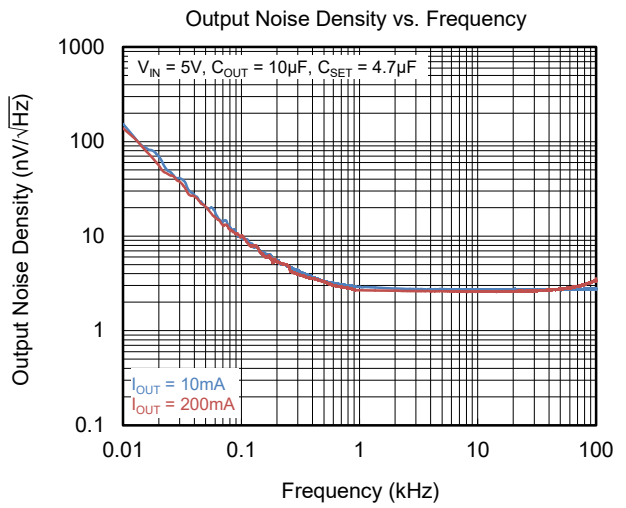
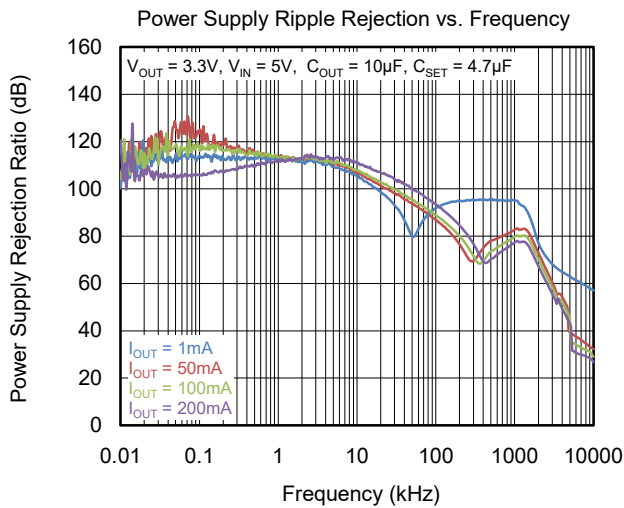
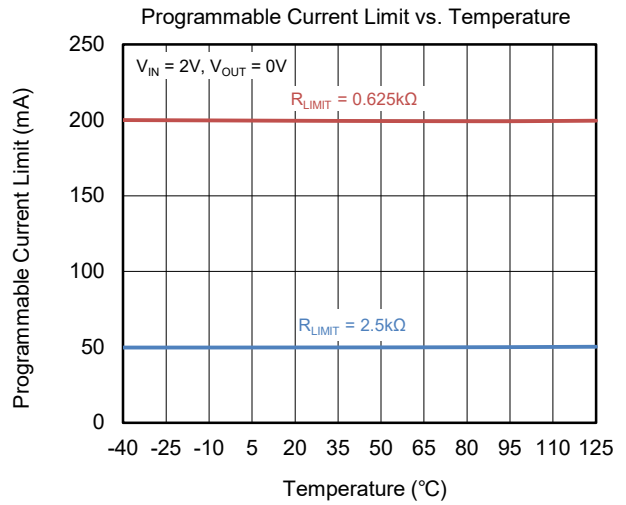
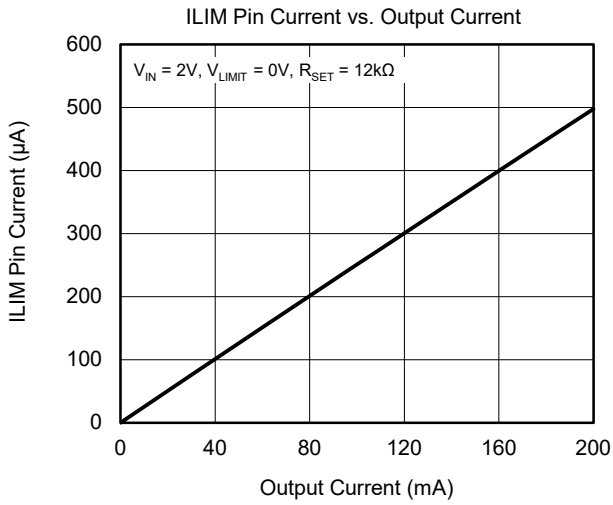
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_J = +25°C, C_{OUT} = 4.7µF, R_{SET} = 33kΩ, unless otherwise noted.

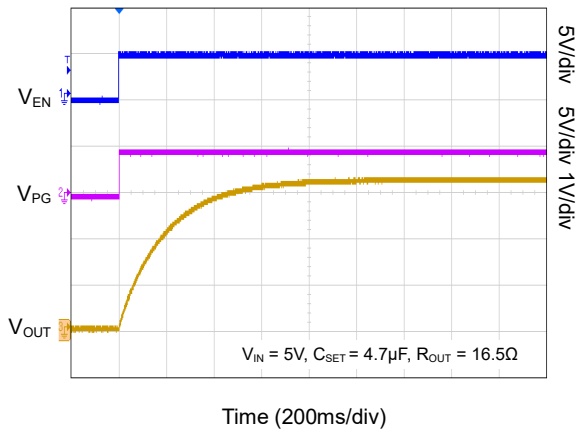


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

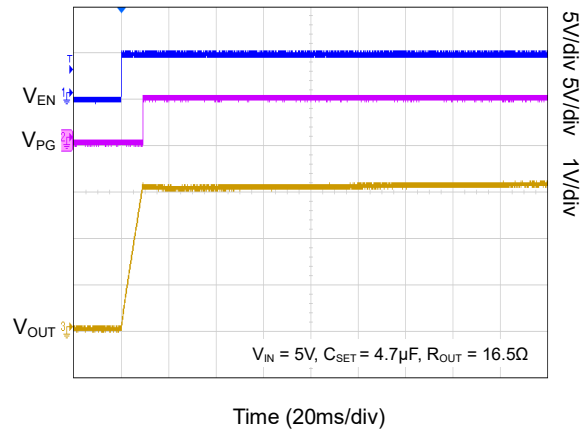
$T_J = +25^\circ\text{C}$, $C_{OUT} = 4.7\mu\text{F}$, $R_{SET} = 33\text{k}\Omega$, unless otherwise noted.



Start-Up Time without Fast Start-Up Circuitry for Large C_{SET}

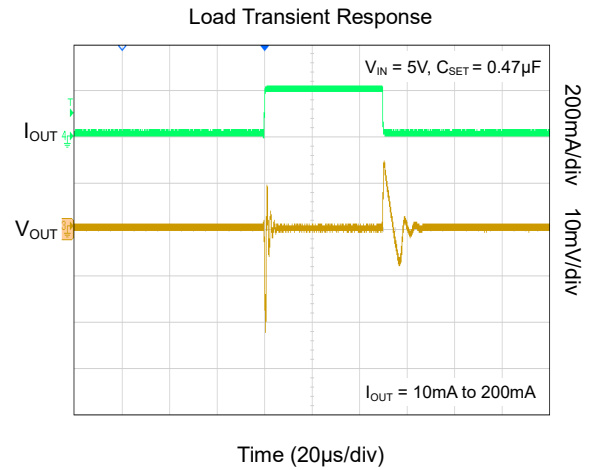
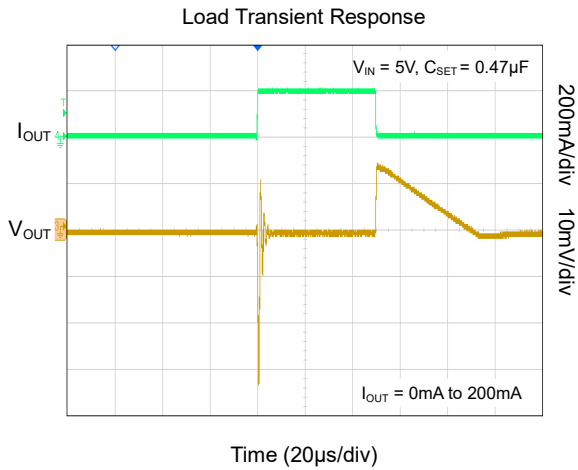
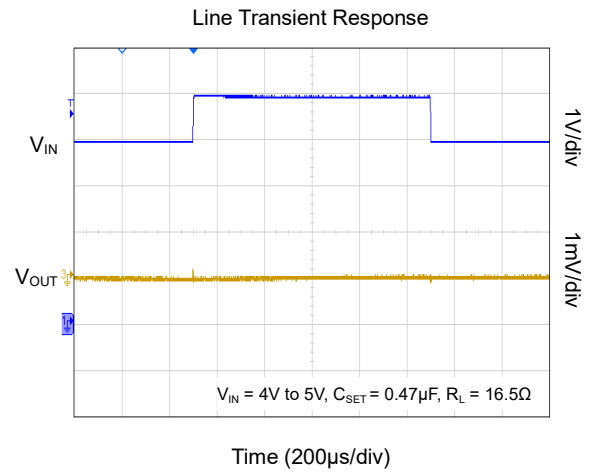
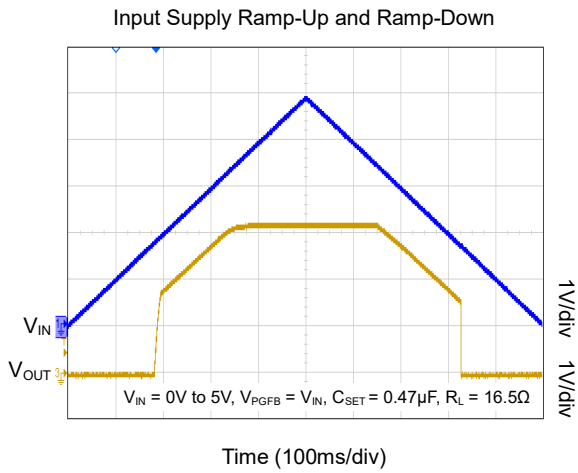


Start-Up Time with Fast Start-Up Circuitry for Large C_{SET}



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_J = +25°C, C_{OUT} = 4.7µF, R_{SET} = 33kΩ, unless otherwise noted.



APPLICATION INFORMATION

The SGM2222 is an ultra-low noise, ultra-high PSRR and low dropout LDO and provides 200mA output current. Multiple SGM2222s in parallel can further reduce noise and increase output current capability. The high performance makes the SGM2222 useful in a variety of applications.

The SGM2222 allows users to program the current limit, Enable/UVLO threshold and Power-Good threshold on demand. It also supports fast start-up operation. Moreover, the SGM2222 provides protection functions for output overload, output short-circuit condition and overheating. These features make the device a reliable solution to solve many challenging problems in the generation of clean and accurate power supply.

Input Capacitor Selection (C_{IN})

The input decoupling capacitor should be placed as close as possible to the IN pin to ensure the device stability. 4.7 μ F or larger X7R or X5R ceramic capacitor is selected to get good dynamic performance.

When V_{IN} is required to provide large current instantaneously, a large effective input capacitor is required. Multiple input capacitors can limit the input tracking inductance. Adding more input capacitors is available to restrict the ringing and to keep it below the device absolute maximum ratings. For C_{OUT} with larger capacitance, it is recommended to choose the larger capacitance C_{IN} .

Output Capacitor Selection (C_{OUT})

A minimum 4.7 μ F output capacitor is required to maintain the stability of the LDO, and the output capacitor should be placed as close as possible to the OUT pin. In addition, in order to obtain the best transient performance, it is recommended to use X7R or X5R ceramic capacitor as the output capacitor. Ceramic capacitor has low equivalent series resistance (ESR), excellent temperature and DC bias characteristics. However, it cannot be ignored that the effective capacitance of ceramic capacitor is affected by temperature, DC bias and package size.

For example, Figure 3 shows the capacitance and DC bias and temperature characteristics of 0805, 10V, 10 μ F \pm 10%, X7R capacitor. Therefore, it is necessary to evaluate whether the effective capacitance of the output capacitor can meet the stability requirements of

the LDO in practical applications. In general, a capacitor in higher voltage rating and a larger package exhibits better stability, and the effective capacitance can be obtained from the manufacturer datasheet.

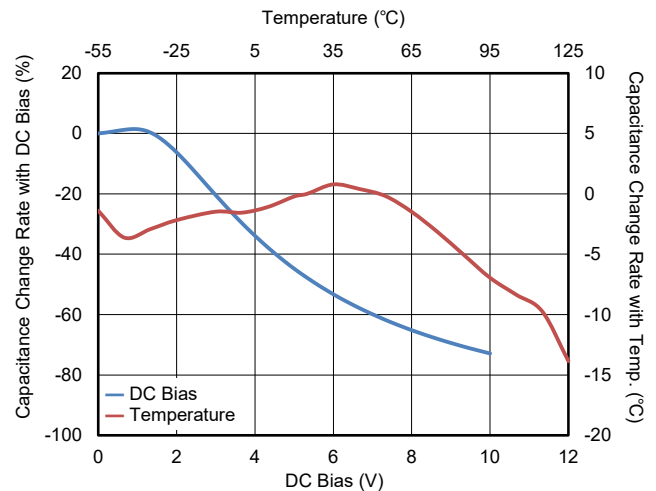


Figure 3. Capacitance vs. DC Bias and Temperature Characteristics

Additionally, C_{OUT} with larger capacitance and lower ESR will help increase the high frequency PSRR and improve the load transient response.

Enable/UVLO

The SGM2222 has an EN/UV pin which has both enable and under-voltage lockout (UVLO) threshold $V_{EN/UV}$ setting function. The EN/UV pin enable threshold is 1.23V (TYP) with 180mV of hysteresis. When the EN/UV pin is pulled to high, the SGM2222 is enabled. When the EN/UV pin is pulled to low, the SGM2222 is disabled and the quiescent current drops to 2.8 μ A (TYP).

If $V_{EN/UV}$ needs to be adjusted, add a resistive voltage divider between the IN, EN/UV and GND pins. The $V_{EN/UV}$ calculation formula is as follow:

$$V_{EN/UV} = 1.23V \times \left(1 + \frac{R_{EN2}}{R_{EN1}}\right) + I_{EN/UV} \times R_{EN2} \quad (1)$$

where R_{EN1} is the resistor between the EN/UV pin and the GND pin, and R_{EN2} is the resistor between the IN pin and the EN/UV pin. The EN/UV pin current ($I_{EN/UV}$) can be omitted if R_{EN1} is below 100k Ω . If this function is not used, the EN/UV pin can also be directly pulled to IN pin.

APPLICATION INFORMATION (continued)

SET Pin Configuration

The SET pin is used to configure the output voltage of the SGM2222 through an external resistor R_{SET} when the regulator operates normally, for detailed configuration details, refer to the Output Voltage section below.

Usually, when the SET pin is in use, an additional bypass capacitor C_{SET} needs to be added to improve output noise, PSRR and transient performance. It should be noted that the C_{SET} must maintain low leakage current to avoid causing significant output voltage errors.

Output Voltage

As shown in Figure 4, the SGM2222 internally integrates a $100\mu\text{A}$ precision current source as the reference, which is connected to the inverting input of the error amplifier. The reference voltage V_{REF} can be set by adding a resistor R_{SET} between the SET pin and ground. Calculate the value for V_{REF} using the following equation:

$$V_{REF} = 100\mu\text{A} \times R_{SET} \quad (2)$$

The error amplifier is a high performance rail-to-rail buffer with unit-gain that can produce an output voltage V_{OUT} with a low output impedance characteristic whose amplitude is equal to the V_{REF} 's. The SGM2222 allows output voltages to vary from 0V to $(V_{IN} - V_{DROP})$. A PMOS-based input pair is active for outputs from 0V to 0.6V and an NPN-based input pair handles outputs above 1.2V to provide optimal performance, with a seamless transition between the two pairs from 0.6V and 1.2V output.

Since the error amplifier always operates with unity gain, the loop gain, frequency response and bandwidth of the SGM2222 are independent of the magnitude of the output voltage, which means that PSRR, transient response and noise performance are basically unaffected by the output voltage. The noise can be further reduced by a factor of \sqrt{N} by connecting N SGM2222s in parallel. In addition, paralleling multiple

SGM2222s can also achieve higher output current. Specific implementation: connect all SET pins directly together and all IN pins directly together. The OUT pins are connected through ballast resistors (or appropriate PCB trace resistors) to equalize the current among each parallel SGM2222.

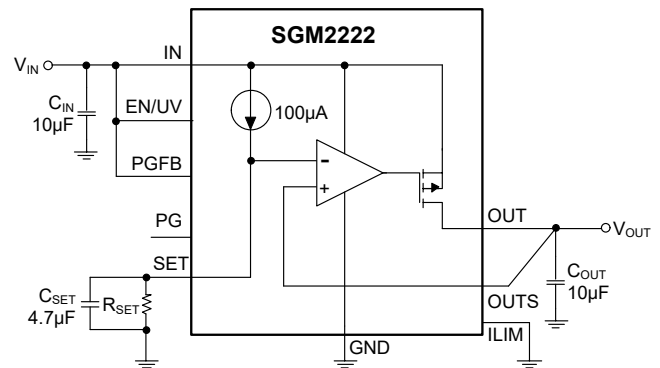


Figure 4. Basic Adjustable Regulator

The SET pin is a high-impedance node, which may cause unwanted signal coupling to the SET pin and affect the stability of the regulator. Adding a capacitor C_{SET} from the SET pin to ground can solve this problem. It should be noted that in high vibration environments, C_{SET} capacitors need to be carefully selected, ceramic capacitors with the piezoelectric response may not be suitable. However, the SET pin is tolerant of high ESR and ESL, so non-piezoelectric-responsive capacitors such as tantalum or electrolytic can be used. To ensure precision output voltage, R_{SET} should be a precision resistor. In addition, although the current reference inside the SGM2222 is highly accurate, any leakage path at the SET pin will cause the output voltage to shift.

The SGM2222 allows using an external voltage reference to eliminate the tolerance of the reference current and resistance, resulting in a more accurate voltage output. The external voltage reference is connected to the SGM2222 via the SET pin and the external reference should have the ability to sink $100\mu\text{A}$ current.

APPLICATION INFORMATION (continued)

Output Sensing

The direct connection of the OUTS pin and the OUT pin does not affect the normal function of the regulator. However, to achieve the expected transient response, phase/gain margin and PSRR performance, the SGM2222 recommends a Kelvin connection in the PCB layout. The OUTS pin and the GND side of the SET pin resistor support this Kelvin connection. As shown in Figure 5, the OUTS pin is directly connected to the OUT side of C_{OUT} by Kelvin connection, while connect the GND sides of the C_{SET} and C_{OUT} directly. In addition, placing the GND sides of C_{IN} and C_{OUT} reasonably close together is also beneficial for performance.

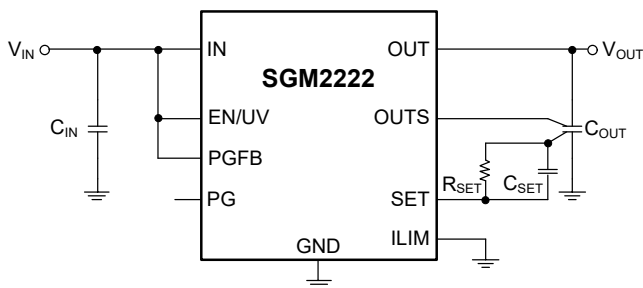


Figure 5. A Kelvin Connection

Soft Start-Up

The SET pin bypass capacitor C_{SET} not only limits inrush current but also soft-starts the output. The soft start-up function of the SGM2222 can be achieved by adding R_{SET} and C_{SET} when the PGFB pin is pulled to IN pin or OUT pin for input voltages above 300mV. The rough calculation formula for the 0% to 90% of nominal V_{OUT} soft start time is as follow:

$$t_{SS} \approx 2.3 \times R_{SET} \times C_{SET} \quad (3)$$

Fast Start-Up

The SGM2222 can obtain the lower noise and high PSRR performance by adding a bypass capacitor C_{SET} to the SET pin in application. To prevent the increase of the start-up time caused by the C_{SET} , the SGM2222 has designed a fast start-up function circuit. During normal operation of the SGM2222, if the PGFB pin voltage is

below 300mV, the fast start-up function is active. The current of the SET pin will increase to 2mA in order to quickly establish the SET pin and OUT pin voltage during start-up. If the PGFB pin is pulled to IN pin or PGFB pin voltage V_{PGFB} is above 300mV, the fast start-up function and Power-Good are disabled.

Power-Good Indicate

The SGM2222 has a PG pin which supports open-drain output and it is used to indicate whether the power supply is good or not based on the input voltage of PGFB pin. Once the PGFB pin voltage is higher than 300mV, the PG pin will become high impedance. In addition, the power-good comparator is designed with a hysteresis voltage of 40mV.

According to the design of SGM2222, the power good threshold V_{PGFB} can be configured through a resistive divider between OUT, PGFB and GND pins. The detailed calculation formula is as follow:

$$V_{PGFB} = 0.3V \times \left(1 + \frac{R_{PG2}}{R_{PG1}}\right) + I_{PGFB} \times R_{PG2} \quad (4)$$

where R_{PG1} is the resistor between the PGFB pin and the GND pin, and R_{PG2} is the resistor between the OUT pin and the PGFB pin. It is necessary to consider the PGFB pin current (I_{PGFB}) from the Electrical Characteristics table when configuring the voltage divider resistor network. However, if R_{PG1} is below 30k Ω , the I_{PGFB} may be omitted. When the output voltage is lower than V_{PGFB} , the PG pin open-drain engages and pulls the PG pin close to GND pin. When the output voltage is higher than V_{PGFB} , the PG pin is indicated as high impedance. Connecting the PG pin to an external power supply via a pull-up resistor enables any downstream device to receive a power-good valid logic signal for sequencing. The resistance of the pull-up resistor is recommended to be 200k Ω . The PG output is pulled down when the SGM2222 is in one of the following states, including disabled, thermal shutdown and UVLO. If the power-good indicator function is not used, float the PG pin.

DETAILED DESCRIPTION (continued)

Programmable Current Limit

The voltage limit threshold of the ILIM pin is 300mV. The maximum current sourced from the ILIM pin can be set by connecting a resistor R_{LIMIT} between the ILIM pin and GND pin, thereby programming the external current limit I_{EXT_LIMIT} of the SGM2222. The I_{LIMIT_EXT} can be calculated using a programming scale factor of 125mA × kΩ as follows:

$$I_{LIMIT_EXT} = 125mA \times k\Omega / R_{LIMIT} \quad (5)$$

When the dropout voltage between input and output exceeds 13V, the foldback circuit of the SGM2222 reduces the internal current limit. Under this condition, the internal current limit may become more restrictive than the externally programmed value to ensure the SGM2222 remains within its Safe Operating Area (SOA).

The current flowing out of the ILIM pin is proportional to the output current at a ratio of approximately 1:400. Therefore, the ILIM pin can also be used as a current monitoring pin, with the voltage across R_{LIMIT} varying from 0V to 300mV. In addition, if external current limiting and current monitoring functions are not used, the ILIM pin can be connected to GND pin.

Output Overshoot Control

The SGM2222 is internally designed with an output overshoot control circuit as shown in the Functional Block Diagram. This function is mainly designed to reduce the output overshoot when the output current suddenly changes from heavy load to light or no load. If no this feature, when the output current jumps from full load to no load, the output will present overshoot

because the output capacitor does not have a fast discharge path. The SGM2222 designs this feature and when the OUTS pin voltage is higher than the SET pin voltage, the output overshoot control circuit will be turned on and a current absorber of nearly 1mA will discharge the output capacitor until the output returns to normal voltage. When the OUTS pin voltage is lower than the SET pin voltage, the output overshoot control circuit will be turned off.

Thermal Overload Protection

The SGM2222 is designed with power limit protection, and the thermal overload protection limits the junction temperature to be lower than +165°C. Under the extreme conditions of high ambient temperature or power dissipation, when the junction temperature is above +165°C, the output is turned off and reduces the output current to 0mA. When the junction temperature falls below +145°C, the output is turned on again and the output current is restored to the nominal value. For reliable operation, device power dissipation must be externally limited so that the junction temperature do not exceed +125°C.

Input Reverse Protection

In addition to current limit and thermal overload protection, the SGM2222 is also designed with reverse input voltage protection. This feature allows the IN to GND pins and the IN and OUT pins to withstand a maximum voltage of -20V without large reverse current. It should be noted that the reverse voltage cannot exceed the specification range according to Absolute Maximum Ratings.

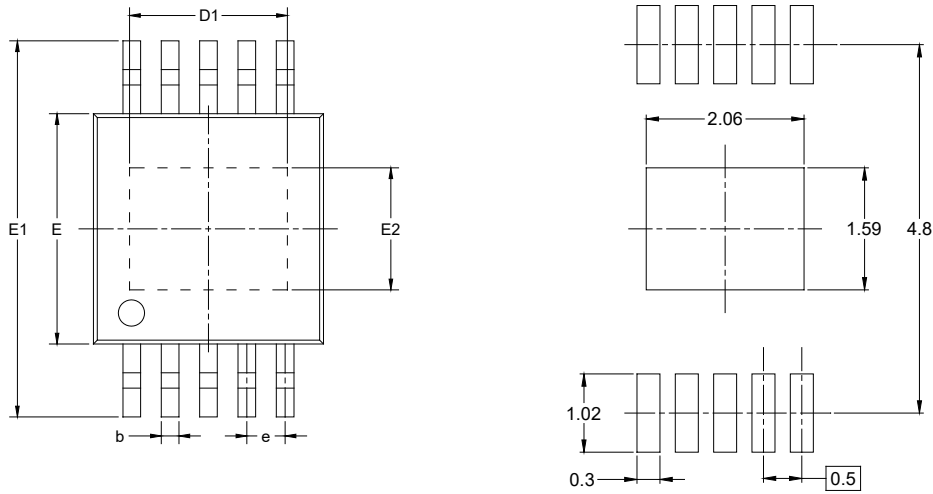
REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

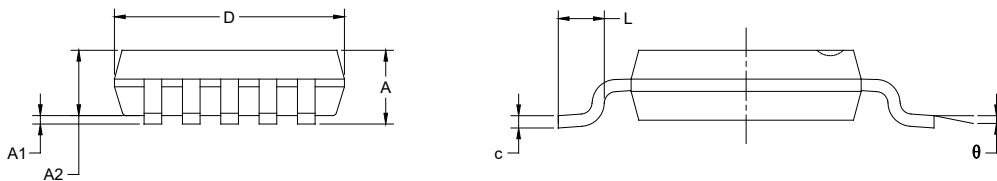
Changes from Original to REV.A (NOVEMBER 2025)	Page
Changed from product preview to production data.....	All

PACKAGE OUTLINE DIMENSIONS

MSOP-10 (Exposed Pad)



RECOMMENDED LAND PATTERN (Unit: mm)



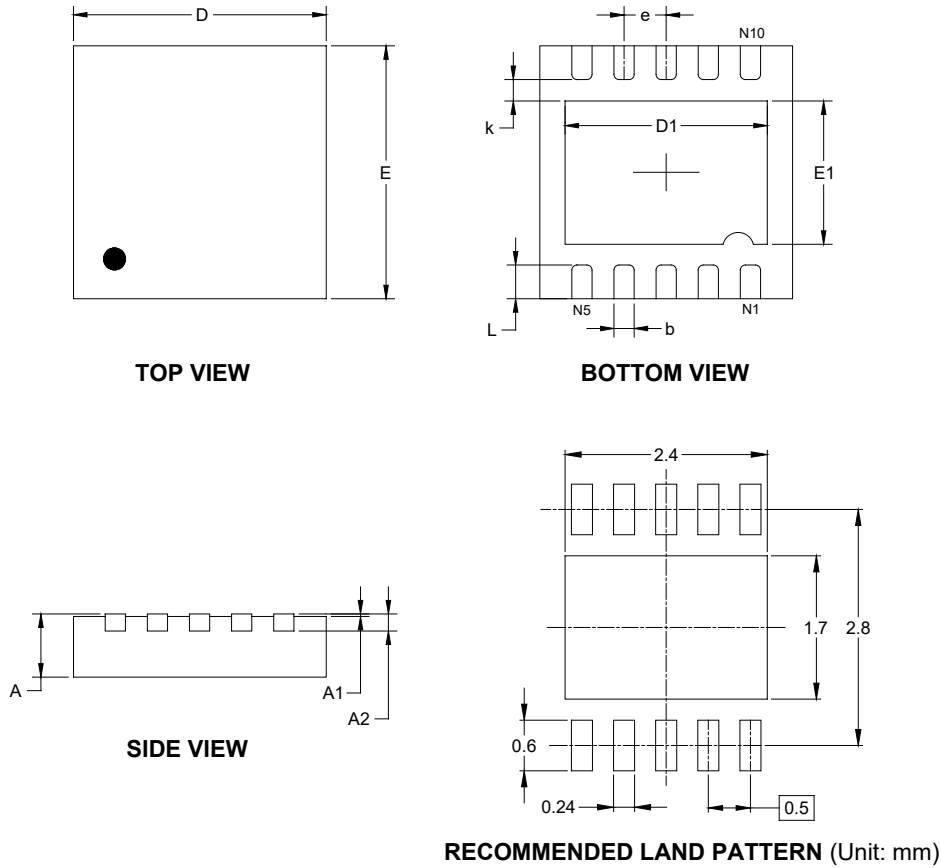
Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	0.820	-	1.100
A1	0.020	-	0.150
A2	0.750	-	0.950
b	0.170	-	0.280
c	0.080	-	0.230
D	2.900	-	3.100
D1	1.700	-	2.416
E	2.900	-	3.100
E1	4.750	-	5.050
E2	1.450	-	1.730
e	0.500 BSC		
L	0.400	-	0.800
θ	0°	-	8°

NOTES:

1. Body dimensions do not include mode flash or protrusion.
2. This drawing is subject to change without notice.

PACKAGE OUTLINE DIMENSIONS

TDFN-3×3-10L

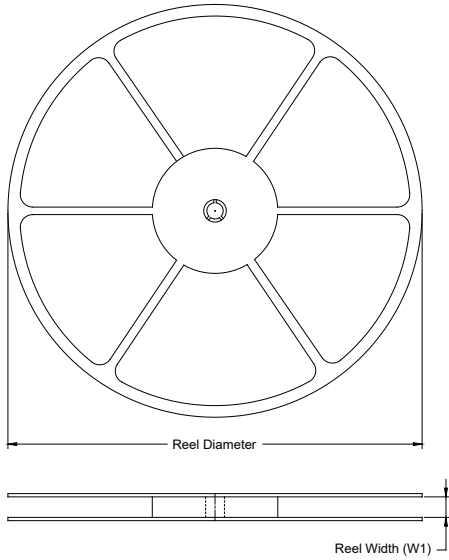


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A2	0.203 REF		0.008 REF	
D	2.900	3.100	0.114	0.122
D1	2.300	2.600	0.091	0.103
E	2.900	3.100	0.114	0.122
E1	1.500	1.800	0.059	0.071
k	0.200 MIN		0.008 MIN	
b	0.180	0.300	0.007	0.012
e	0.500 TYP		0.020 TYP	
L	0.300	0.500	0.012	0.020

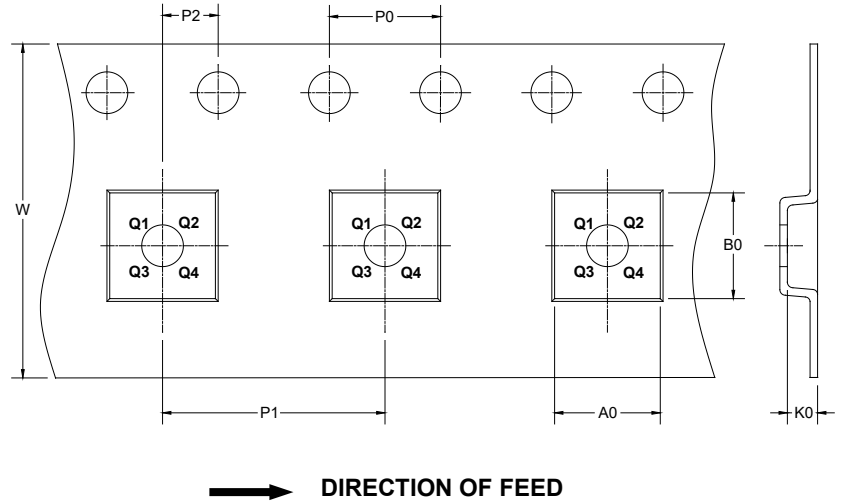
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

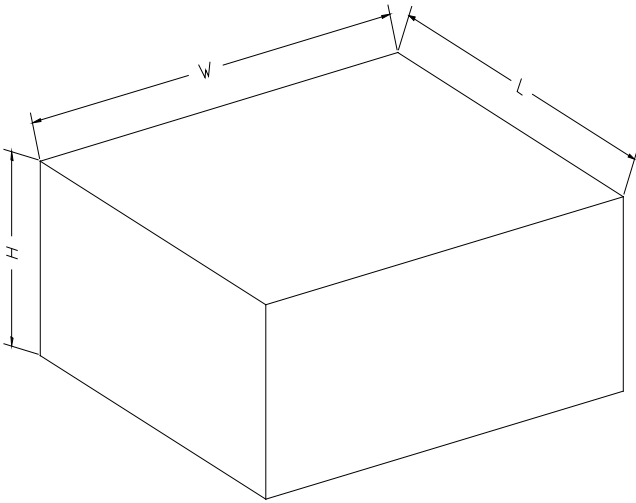
KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
MSOP-10 (Exposed Pad)	13"	12.4	5.20	3.30	1.50	4.0	8.0	2.0	12.0	Q1
TDFN-3×3-10L	13"	12.4	3.35	3.35	1.13	4.0	8.0	2.0	12.0	Q1

DD0001

PACKAGE INFORMATION

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13"	386	280	370	5

DD0002