SGM42330/SGM42331
5V to 60V, Three-Phase Brushless DC Motor Pre-Drivers

GENERAL DESCRIPTION

The SGM42330/1 family is a three-phase BLDC gate driver. It is designed to drive three half-bridges composed of six N-channel power MOSFETs, and supports an input voltage range of 5V to 60V.

These devices generate the gate drive voltages using an internal charge pump and enhance the high-side MOSFETs using a bootstrap circuit. Even if the output works at 100% duty cycle, the internal trickle-charge circuit can maintain enough high-side gate driver voltage.

For SGM42330, the ENx and PWMx control inputs are provided for each half-bridge. For SGM42331, the HSx (high-side control inputs) and LSx (low-side control inputs) are provided for each half-bridge.

The device has multiple protection functions, including programmable short-circuit protection (SCP), over-current protection (OCP), under-voltage lockout (UVLO), adjustable dead-time control, and thermal shutdown (TSD).

The SGM42330/1 is available in Green TSSOP-28 (Exposed Pad) and TQFN-4×4-28BL packages.

APPLICATIONS

Three-Phase Brushless DC Motors and Permanent Magnet Synchronous Motors
Power Drills
Impact Drivers
E-Bike

FEATURES

- **5V to 60V Wide Input Voltage Range**
- **Charge Pump Gate Drive Supply**
- **Bootstrap High-side Driver with Trickle-Charge Circuit Supports 100% Duty Cycle Operation**
- **Low-Power Sleep Mode**
- **Adjustable Short-Circuit Protection**
- **Over-Current Protection**
- **Control Inputs**
  - **SGM42330: ENx and PWMx**
  - **SGM42331: HSx and LSx**
- **Adjustable Dead-Time Control to Prevent Shoot-Through**
- **Thermal Shutdown and UVLO Protection**
- **Fault Indication Output**
- **Thermally Enhanced Surface-Mount Package**
- **Available in Green TSSOP-28 (Exposed Pad) and TQFN-4×4-28BL Packages**

TYPICAL APPLICATION

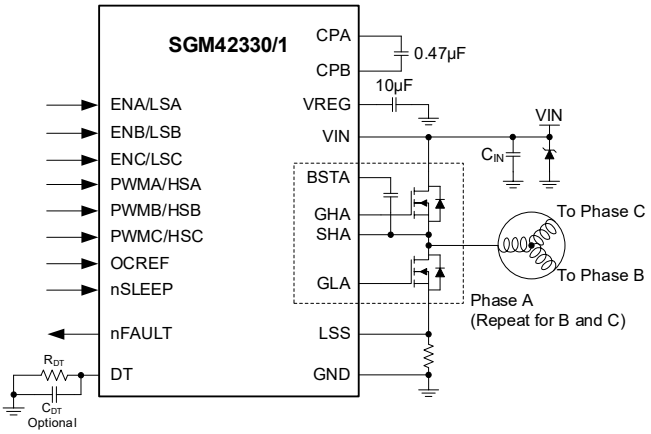


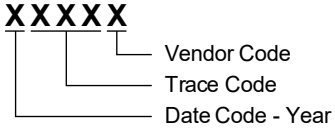
Figure 1. SGM42330/1 Typical Application Circuit

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM42330	TSSOP-28 (Exposed Pad)	-40℃ to +125℃	SGM42330XPTS28G/TR	SGM42330 XPTS28 XXXXX	Tape and Reel, 4000
	TQFN-4×4-28BL	-40℃ to +125℃	SGM42330XTSX28G/TR	SGM42330 XTSX28 XXXXX	Tape and Reel, 3000
SGM42331	TSSOP-28 (Exposed Pad)	-40℃ to +125℃	SGM42331XPTS28G/TR	SGM42331 XPTS28 XXXXX	Tape and Reel, 4000
	TQFN-4×4-28BL	-40℃ to +125℃	SGM42331XTSX28G/TR	SGM42331 XTSX28 XXXXX	Tape and Reel, 3000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines “Green” to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Input Voltage, V_{IN} ..... -0.3V to 62V
CPA ..... -0.3V to 60V
CPB ..... -0.3V to 13V
VREG ..... -0.3V to 13V
BSTA/B/C ..... -0.3V to 70V
GHA/B/C ..... -0.3V to 70V
GHA/B/C (Transient, 2μs) ..... -8V to 70V
SHA/B/C ..... -0.3V to 62V
SHA/B/C (Transient, 2μs) ..... -8V to 62V
GLA/B/C ..... -0.3V to 13V
LSS ..... -0.3V to 1V
All Other Pins to AGND ..... -0.3V to 6V
Package Thermal Resistance
TSSOP-28 (Exposed Pad), θ_{JA} ..... 31.3℃/W
TSSOP-28 (Exposed Pad), θ_{JB} ..... 12.1℃/W
TSSOP-28 (Exposed Pad), $\theta_{JC\ (TOP)}$ ..... 20.1℃/W
TSSOP-28 (Exposed Pad), $\theta_{JC\ (BOT)}$ ..... 1.7℃/W
TQFN-4×4-28BL, θ_{JA} ..... 33.5℃/W
TQFN-4×4-28BL, θ_{JB} ..... 10.8℃/W
TQFN-4×4-28BL, $\theta_{JC\ (TOP)}$ ..... 24.6℃/W
TQFN-4×4-28BL, $\theta_{JC\ (BOT)}$ ..... 1.7℃/W
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility (1) (2)
HBM ..... ±3000V
CDM ..... ±1500V

NOTES:

1. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.

2. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

RECOMMENDED OPERATING CONDITIONS

Input Voltage, V_{IN} ..... 5V to 60V
OCREF Voltage, V_{OC} ..... 0.125V to 2.4V (1)
Operating Ambient Temperature Range ..... -40℃ to +125℃
Operating Junction Temperature Range ..... -40℃ to +150℃

NOTE: 1. When V_{IN} is below 6.5V, the recommended operating range for OCREF is 0.125V to 1.8V.

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

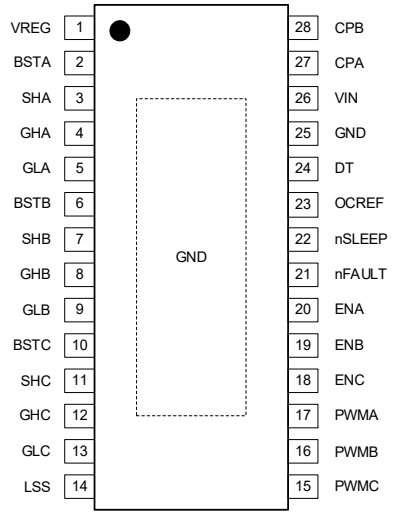
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

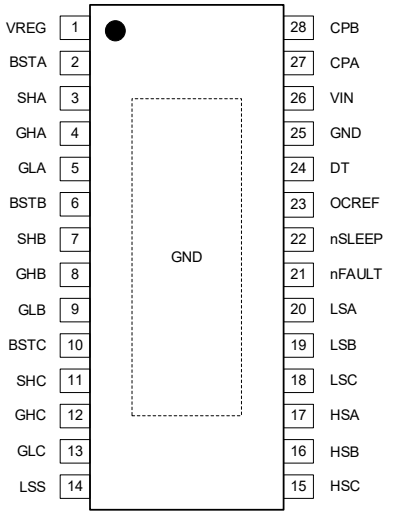
PIN CONFIGURATIONS

SGM42330 (TOP VIEW)



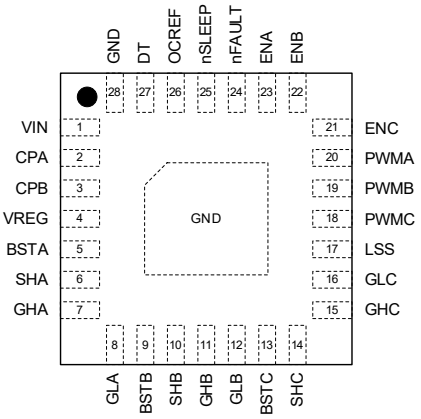
TSSOP-28 (Exposed Pad)

SGM42331 (TOP VIEW)



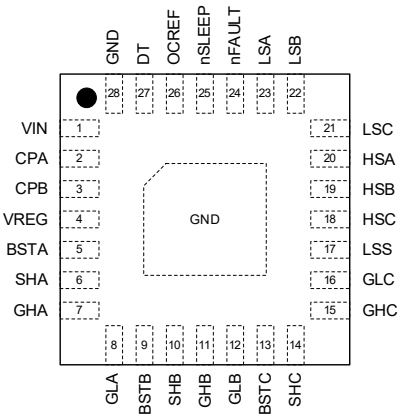
TSSOP-28 (Exposed Pad)

SGM42330 (TOP VIEW)



TQFN-4×4-28BL

SGM42331 (TOP VIEW)



TQFN-4×4-28BL

PIN DESCRIPTION

PIN		NAME	FUNCTION
TSSOP-28 (Exposed Pad)	TQFN-4×4-28BL		
26	1	VIN	Input Supply Voltage. Bypass to GND with a ceramic capacitor. May require additional bulk capacitance.
27	2	CPA	Charge Pump Switching Node. Connect a ceramic capacitor between CPA and CPB pins.
28	3	CPB	
1	4	VREG	Gate Drive Supply Output. Connect a ceramic capacitor between VREG and GND.

PIN DESCRIPTION (continued)

PIN		NAME	FUNCTION
TSSOP-28 (Exposed Pad)	TQFN-4×4-28BL		
2	5	BSTA	Phase A Bootstrap. Connect a ceramic capacitor between BSTA and SHA.
3	6	SHA	Phase A High-side Source Connection.
4	7	GHA	Phase A High-side Gate Drive.
5	8	GLA	Phase A Low-side Gate Drive.
6	9	BSTB	Phase B Bootstrap. Connect a ceramic capacitor between BSTB and SHB.
7	10	SHB	Phase B High-side Source Connection.
8	11	GHB	Phase B High-side Gate Drive.
9	12	GLB	Phase B Low-side Gate Drive.
10	13	BSTC	Phase C Bootstrap. Connect a ceramic capacitor between BSTC and SHC.
11	14	SHC	Phase C High-side Source Connection.
12	15	GHC	Phase C High-side Gate Drive.
13	16	GLC	Phase C Low-side Gate Drive.
14	17	LSS	Low-side Source Connection.
15	18	PWMC	SGM42330 Only. Phase C PWM Input. Logic high pulls half-bridge high, logic low pulls half-bridge low and no effect when ENC is low. Internal pull-down.
		HSC	SGM42331 Only. Phase C High-side FET Enable Input.
16	19	PWMB	SGM42330 Only. Phase B PWM Input. Logic high pulls half-bridge high, logic low pulls half-bridge low and no effect when ENB is low. Internal pull-down.
		HSB	SGM42331 Only. Phase B High-side FET Enable Input.
17	20	PWMA	SGM42330 Only. Phase A PWM Input. Logic high pulls half-bridge high, logic low pulls half-bridge low and no effect when ENA is low. Internal pull-down.
		HSA	SGM42331 Only. Phase A High-side FET Enable Input.
18	21	ENC	SGM42330 Only. Phase C Enable Pin. Logic high enables the half-bridge channel. Internal pull-down.
		LSC	SGM42331 Only. Phase C Low-side FET Enable Input.
19	22	ENB	SGM42330 Only. Phase B Enable Pin. Logic high enables the half-bridge channel. Internal pull-down.
		LSB	SGM42331 Only. Phase B Low-side FET Enable Input.
20	23	ENA	SGM42330 Only. Phase A Enable Pin. Logic high enables the half-bridge channel. Internal pull-down.
		LSA	SGM42331 Only. Phase A Low-side FET Enable Input.
21	24	nFAULT	Fault Indication. Open-drain output. This pin is pulled logic low during a fault condition and requires an external pull-up resistor to 3.3V to 5.0V.
22	25	nSLEEP	Sleep Mode Input. Apply high to enable internal pull-down, and low to enter into the low power sleep mode.
23	26	OCREF	Over-Current Protection Reference Voltage Input.
24	27	DT	Dead Time Setting. Connect a resistor between DT and GND to set the dead time.
25	28	GND	Ground.
Exposed Pad	Exposed Pad	GND	Ground.

ELECTRICAL CHARACTERISTICS

(V_{IN} = 24V, T_J = -40℃ to +125℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Power Supply							
Input Supply Voltage	V_{IN}			5		60	V
Quiescent Current	I_Q	nSLEEP = 1, gate not switching	R_{DT} = 200kΩ, SGM42330		0.9	2	mA
			R_{DT} = 10kΩ, SGM42331		0.9	2	
	I_{nSLEEP}	nSLEEP = 0				1	μA
Control Logic							
Input Logic Low Threshold	V_{IL}			0.8			V
Input Logic High Threshold	V_{IH}					2.1	V
Logic Input Current	I_{IN_H}	V_{IH} = 5V		-20		20	μA
	I_{IN_L}	V_{IL} = 0.8V		-20		20	μA
nSLEEP Pull-Down Resistance	$R_{SLEEP-PD}$				1.5		MΩ
Internal Pull-Down Resistance	R_{PD}	All logic inputs except nSLEEP			860		kΩ
nFAULT Output (Open-Drain Output)							
Output Low Voltage	V_{OL}	I_O = 5mA				0.5	V
Output High Leakage Current	I_{OH}	V_O = 3.3V				1	μA
Protection Circuits							
UVLO Rising Threshold	V_{IN_RISE}			3.6	4.2	4.7	V
UVLO Hysteresis	V_{IN_HYS}				190		mV
VREG Rising Threshold	V_{REG_RISE}			6.7	7.4	8.1	V
VREG Hysteresis	V_{REG_HYS}				0.5	1	V
Short-Circuit Threshold Accuracy (MOSFET V_{DS})	V_{SC}	T_J = +25℃	V_{OC} = 1V	0.8	1	1.2	V
			V_{OC} = 2.4V	2.18	2.4	2.62	
OCP Deglitch Time	t_{OC}				3		μs
SLEEP Wakeup Time	t_{nSLEEP}				1.3		ms
LSS OCP Threshold	V_{LSS_OCP}			0.4	0.5	0.6	V
Thermal Shutdown	T_{SD}				165		℃
Gate Drive							
Bootstrap Diode Forward Voltage	V_{FBOOT}	I_D = 10mA			0.9	1.1	V
		I_D = 100mA			1.1	1.3	V
VREG Output Voltage	V_{REG}	V_{IN} = 5.5V to 60V, T_J = -40℃ to +125℃		10	11.5	12.8	V
		V_{IN} = 5V, T_J = -40℃ to +125℃		9			
Maximum Source Current	I_{OSO}	Guaranteed by design, not tested in production			1		A
Maximum Sink Current	I_{OSI}	Guaranteed by design, not tested in production			1.2		A
Gate Drive Pull-Up Resistance	R_{UP}	$I_{GH/LX}$ = -100mA, V_{REG} = 11.5V			4		Ω
HS Gate Drive Pull-Down Resistance	R_{HS-DN}	V_{REG} = 11.5V	I_{GHx} = 100mA	0.4		3.5	Ω
LS Gate Drive Pull-Down Resistance	R_{LS-DN}		I_{GLx} = 100mA	0.4		4	
LS Passive Pull-Down Resistance	R_{LS-PDN}				560		kΩ
LS Automatic Turn-On Time	t_{LS}	At power-up			0.53		μs
Charge Pump Frequency	f_{CP}				108		kHz

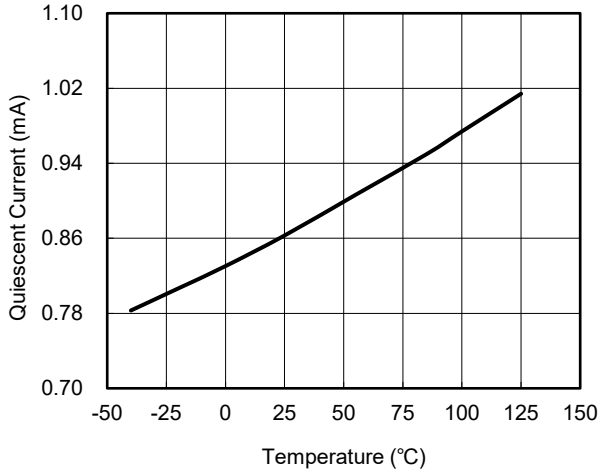
ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 24V, T_J = -40℃ to +125℃, unless otherwise noted.)

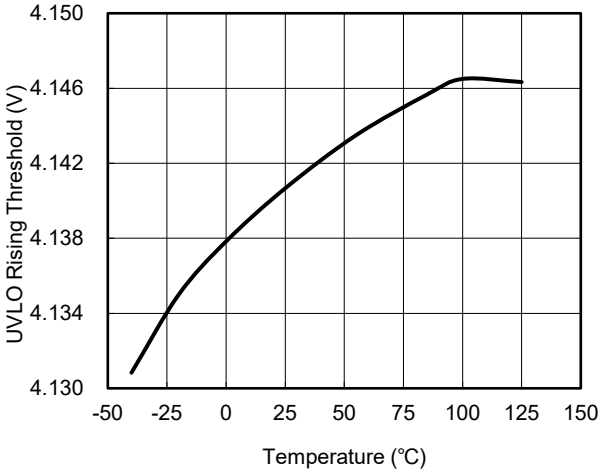
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Dead Time for SGM42330						
Dead Time	t_{DEAD}	DT open		6		μs
		R_{DT} = 200kΩ		0.74		μs
		DT tied to GND		100		ns
Dead Time for SGM42331						
Dead Time	t_{DEAD}	R_{DT} = 10kΩ		0.7		μs
		DT tied to GND		100		μs

TYPICAL PERFORMANCE CHARACTERISTICS

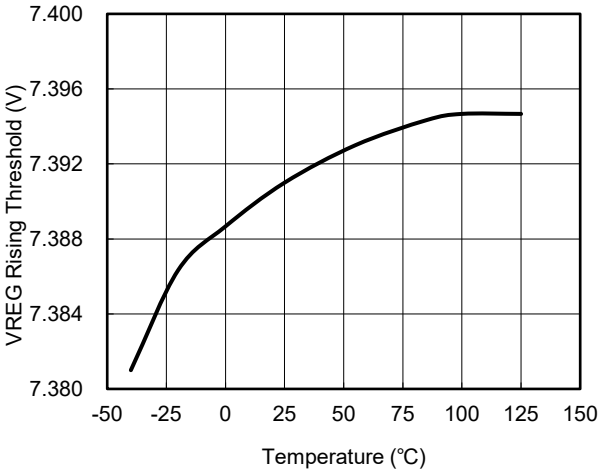
Quiescent Current vs. Temperature



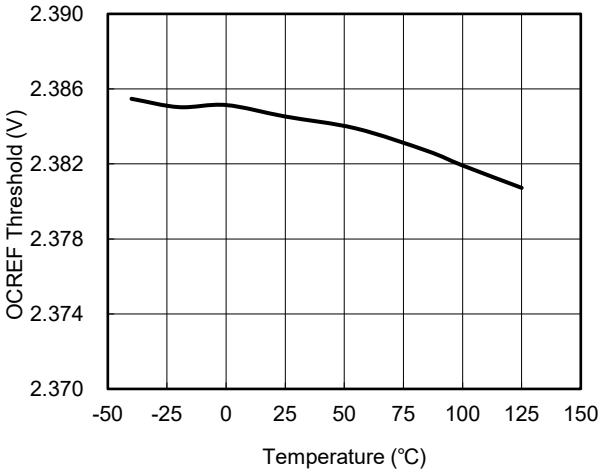
UVLO Rising Threshold vs. Temperature



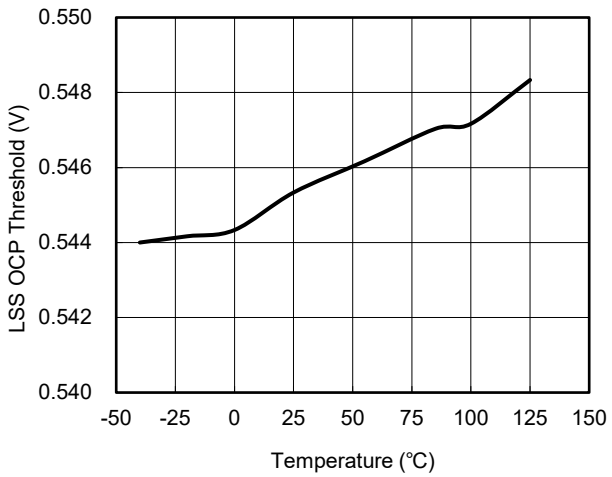
VREG Rising Threshold vs. Temperature



OCREF Threshold vs. Temperature



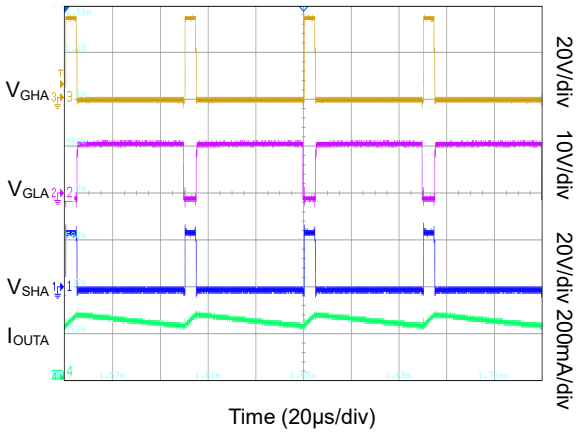
LSS OCP Threshold vs. Temperature



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

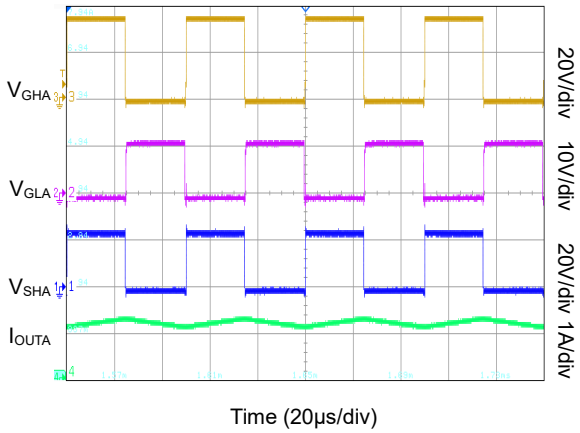
V_{IN} = 24V, V_{OCREF} = 0.5V, R_{DT} = 200kΩ, ENA = ENC = H, PWMC = L, f_{PWMA} = 20kHz, T_A = +25℃, resistor + inductor load: 5Ω + 1mH/phase with star connection, unless otherwise noted.

Steady State (Duty = 10%)



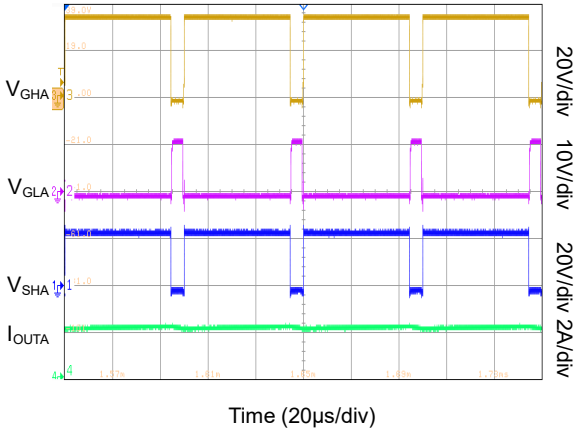
Time (20μs/div)

Steady State (Duty = 50%)



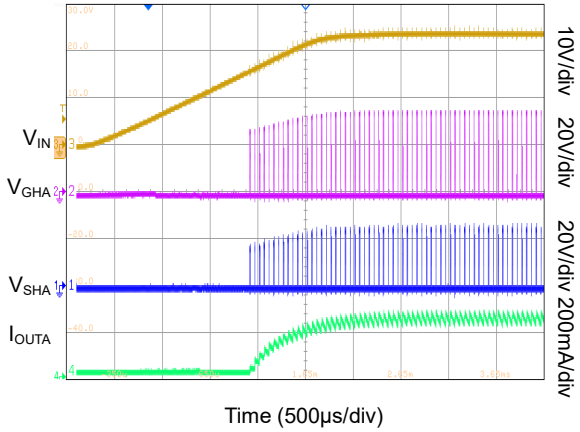
Time (20μs/div)

Steady State (Duty = 90%)



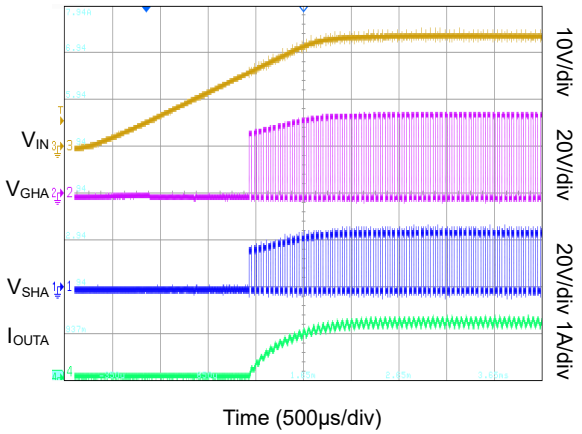
Time (20μs/div)

Power Ramp Up (Duty = 10%)



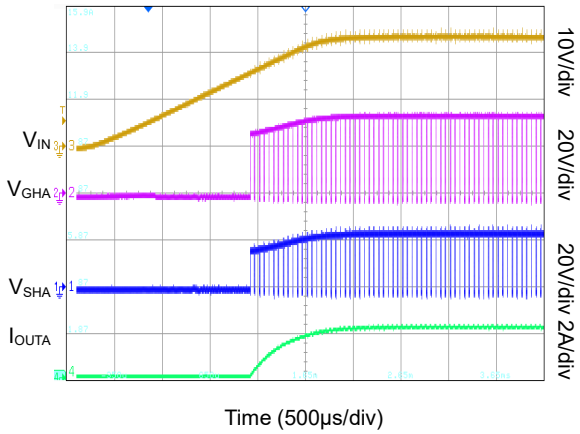
Time (500μs/div)

Power Ramp Up (Duty = 50%)



Time (500μs/div)

Power Ramp Up (Duty = 90%)

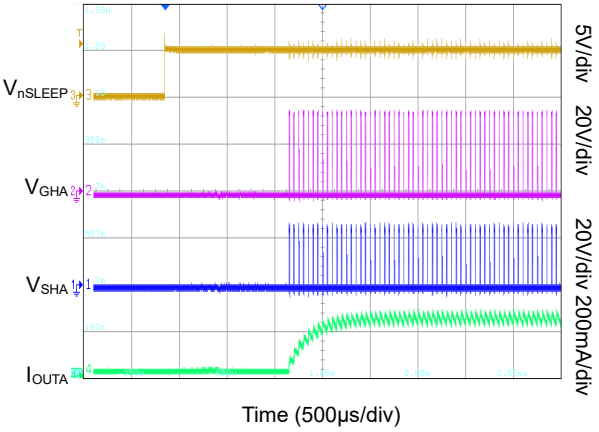


Time (500μs/div)

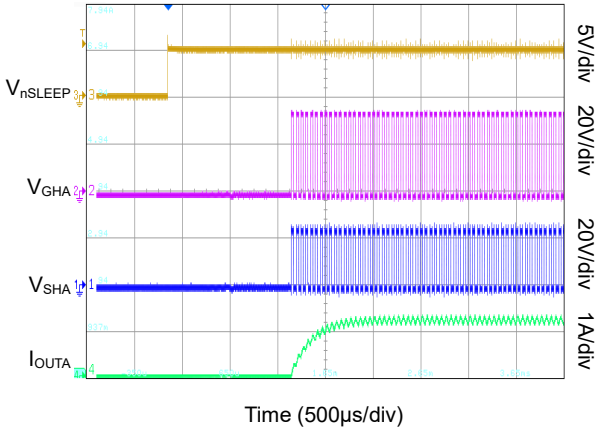
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

V_{IN} = 24V, V_{OCREF} = 0.5V, R_{DT} = 200kΩ, ENA = ENC = H, PWMC = L, f_{PWMA} = 20kHz, T_A = +25℃, resistor + inductor load: 5Ω + 1mH/phase with star connection, unless otherwise noted.

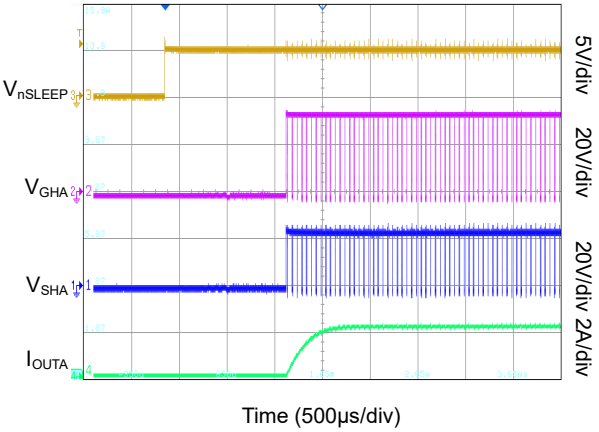
nSLEEP Recovery (Duty = 10%)



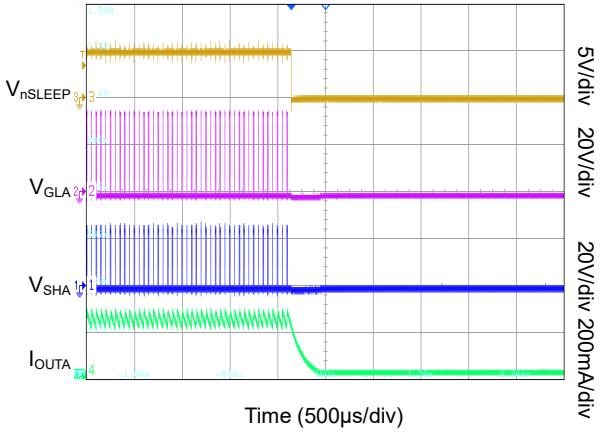
nSLEEP Recovery (Duty = 50%)



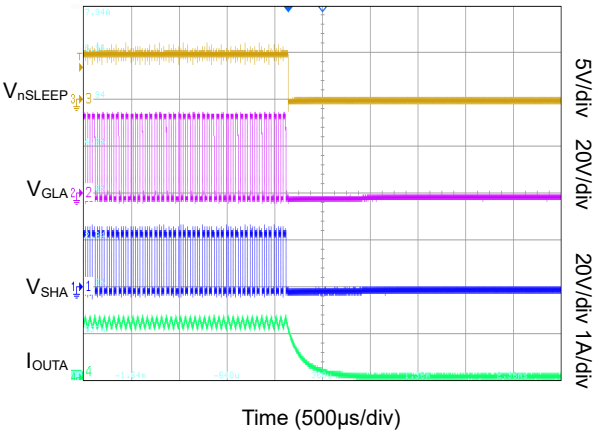
nSLEEP Recovery (Duty = 90%)



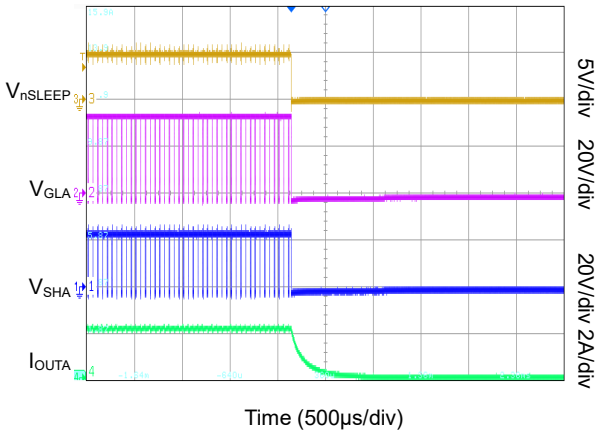
SLEEP Entry (Duty = 10%)



SLEEP Entry (Duty = 50%)



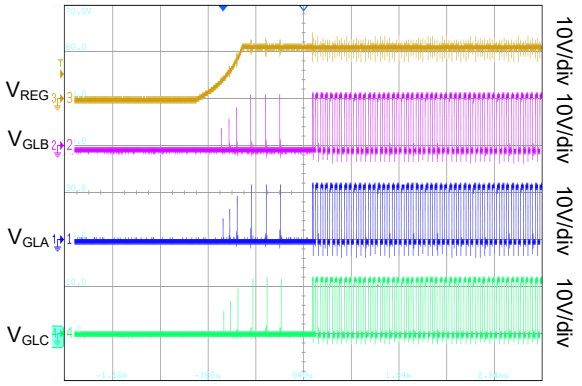
SLEEP Entry (Duty = 90%)



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

V_{IN} = 24V, V_{OCREF} = 0.5V, R_{DT} = 200kΩ, ENA = ENB = ENC = H, f_{PWMA} = f_{PWMB} = f_{PWMC} = 20kHz, T_A = +25℃, no load.

VREG Startup (Duty = 50%)



Time (500μs/div)

FUNCTIONAL BLOCK DIAGRAM

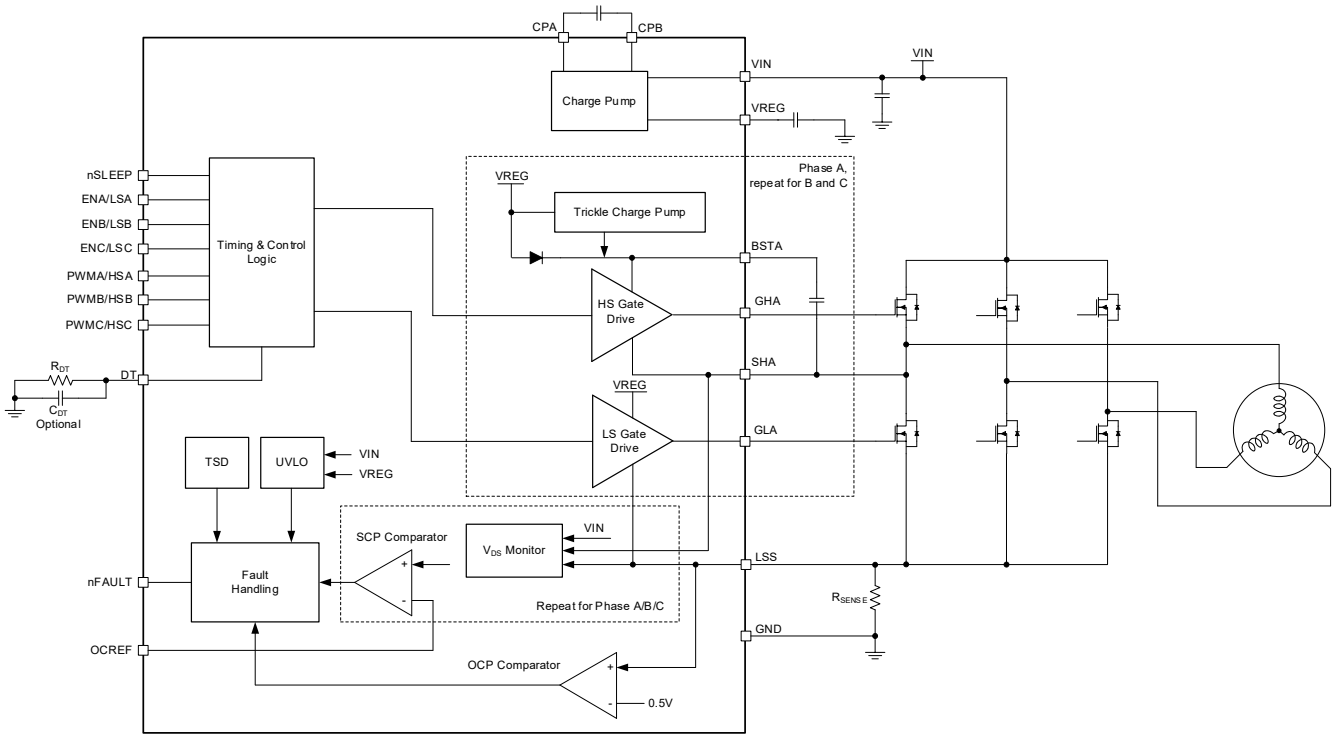


Figure 2. SGM42330/1 Block Diagram

DETAILED DESCRIPTION

The SGM42330/1 family is a gate driver for three-phase BLDC motors, designed to drive six N-channel power MOSFETs. The gate drive supports peak gate drive currents up to 1A source and 1.2A sink and can operate from 5V to 60V. The devices generate the gate drive voltages using an internal charge pump and enhance the high-side MOSFETs using a bootstrap circuit. The SGM42330/1 includes a sleep mode that disables active operation and reduces supply current to below 1μA.

The SGM42330/1 provides multiple protection functions, including programmable short-circuit protection (SCP), over-current protection (OCP), under-voltage lockout (UVLO), adjustable dead-time control, and thermal shutdown (TSD).

Power-Up Sequence

The power-up sequence begins when voltage is applied to the VIN pin, requiring V_{IN} to be above the UVLO rising threshold (V_{IN_RISE}).

Following the onset of power-up, the VREG supply is activated. The device becomes functional only after V_{REG} rises above VREG rising threshold (V_{REG_RISE}).

The power-up sequence takes approximately 1ms to 2ms, after which the SGM42330/1 begins to respond to logic inputs and drives the outputs.

Gate Drive Power Supplies

The gate drive power supplies are derived from VIN. An internal regulated charge pump doubler circuit generates approximately 11.5V at the VREG pin, and this voltage serves as the low-side gate drive supply. External capacitors are required between the CPA and CPB pins, and from the VREG pin to ground.

A bootstrap capacitor, in conjunction with an internal "trickle" charge pump, produces the high-side gate drive. The bootstrap capacitors are charged to the VREG voltage during low-side MOSFET conduction. This charge is subsequently utilized to drive the high-side MOSFET gate when it turns on.

An internal trickle charge pump delivers a small current (approximately 35μA) to compensate for leakages that would otherwise discharge the bootstrap capacitors, thereby keeping them charged and enabling 100% duty cycle operation.

Low-side Automatic Turn-on

To ensure proper high-side gate driving after power-up, the low-side gate drive is activated for several pulses (t_{LS}) during the power-up sequence to charge the bootstrap capacitor, raising the BSTx to SHx voltage to an appropriate level.

Sleep Mode (nSLEEP Input)

Pulling nSLEEP low puts the device into a low-power mode, with a maximum current of no more than 1μA. While nSLEEP is active low, all inputs are ignored. An internal pull-down is present on nSLEEP, thus, driving it high is required to enable device operation.

Exiting sleep mode causes the power-up process described above to repeat.

Input Logic

The SGM42330 uses ENx and PWMx as input pins to drive the corresponding half-bridge. With ENx low, neither the high-side nor the low-side gate drive output is enabled. Only when ENx is high does the corresponding gate drive output follow PWMx, with dead time inserted between switching transitions. The dead time is set by the R_{DT} resistor. Refer to Table 1 for the logic truth table of SGM42330.

Table 1: Input Logic Truth Table of SGM42330

ENx	PWMx	SHx
H	H	VIN
H	L	GND
L	x	Hi-Z

The SGM42331 provides HSx (high-side gate driver control inputs) and LSx (low-side gate driver control inputs) for each half-bridge. To prevent shoot-through between the high-side and low-side MOSFETs, dead time is inserted when HSx and LSx switch. The dead time is configured by R_{DT}. When both HSx and LSx are high, neither the high-side nor the low-side gate drive is turned on. (See Table 2).

Table 2: Input Logic Truth Table of SGM42331

LSx	HSx	SHx
H	H	Hi-Z
H	L	GND
L	H	VIN
L	L	Hi-Z

DETAILED DESCRIPTION (continued)

nFAULT

Upon the occurrence of VREG UVLO, OCP, SCP, or TSD, nFAULT is asserted low and latched. Once the fault condition is cleared and the device is re-powered, nFAULT is released high. nFAULT is configured as an open-drain output.

Short-Circuit Protection (V_{DS} Sensing)

V_{DS} sensing circuitry is implemented in the SGM42330/1 for the purpose of protecting the power stage from high-current damage. The VDS voltage of each of the six MOSFETs is monitored. If the corresponding gate drive signal is active and the VDS voltage of that MOSFET rises above the voltage present on the OCREF pin, a short circuit is detected.

Upon detection of a short-circuit event, the SGM42330/1 disables all gate drives and enters a latched state. nFAULT is asserted low as well. Normal operation is restored only after all fault conditions are cleared and the device is re-powered.

Short circuit protection can be disabled by connecting a 100kΩ resistor between VREG and OCREF.

Over-Current Protection (OCP)

The SGM42330/1 provides over-current protection by sensing the current in a low-side shunt resistor connected between the LSS and ground. Upon detection of the LSS voltage exceeding the LSS OCP threshold voltage (V_{LSS_OCP}), the device enters over-current protection. Once in this state, nFAULT of the SGM42330/1 is asserted low, and the device enters a latched state in which all outputs are disabled until a restart is performed via nSLEEP or VIN UVLO.

The OCP current level is set by the shunt resistor value. When OCP is not needed, LSS may be tied directly to ground. Alternatively, over-current protection can be disabled by connecting a 100kΩ resistor between VREG and OCREF. Note that this also disables the SCP function.

Short-Circuit and OCP Deglitch Time

Current spikes often occur during MOSFET switching. To avoid erroneously triggering SCP, filtering out these spikes is essential. An internal fixed OCP deglitch time (t_{OC}) filters out these spikes when the MOSFETs switch.

Dead Time Adjustment

To prevent shoot-through in any phase of the bridge, a dead time (t_{DEAD}) must be inserted after a high-side or low-side turn-off and before the next complementary turn-on event. For all three phases, the dead time is determined by a single dead time resistor (R_{DT}) connected between DT and ground. The dead time calculation formula for the SGM42330 is given in Equation 1, and the SGM42331 calculation formula is given in Equation 2.

$$t_{DEAD}\ (ns) = 3.2 \times R_{DT}\ (k\Omega) + 100ns \quad (1)$$

$$t_{DEAD}\ (ns) = 60 \times R_{DT}\ (k\Omega) + 100ns \quad (2)$$

An internal minimum dead time (100ns) is applied if DT is directly grounded. When the R_{DT} of SGM42330 is open, the dead time is approximately 6μs.

To reduce the impact of GND noise, a capacitor C_{DT} (TYP 100pF) can optionally be connected in parallel with the R_{DT} resistor, thereby improving dead time accuracy.

UVLO Protection

When the VIN voltage falls below the UVLO threshold (V_{IN_RISE}), all device circuitry is disabled, and the internal logic is reset. If the VIN voltage rises above the UVLO threshold, the power-up sequence is executed.

When the VREG voltage drop below the V_{REG} rising threshold after power-up, a VREG_UVLO fault is triggered. nFAULT is asserted low and remains latched until a reset is performed via nSLEEP or VIN re-power.

Thermal Shutdown

If the die temperature exceeds the thermal shutdown threshold (T_{SD}), the device enters thermal shutdown. nFAULT is pulled low and remains latched until the temperature decreases and nSLEEP is asserted or VIN is re-powered.

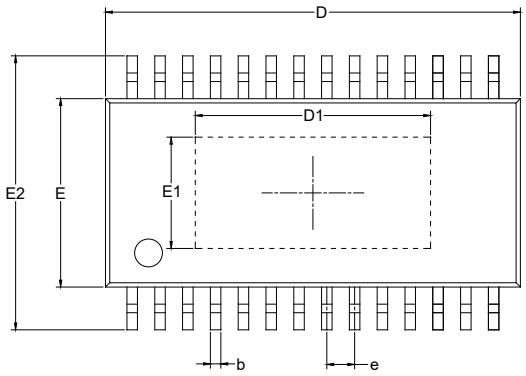
REVISION HISTORY

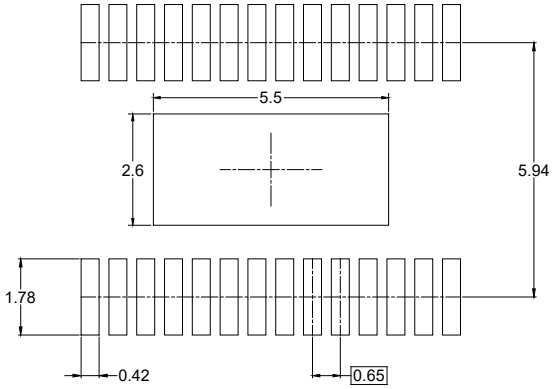
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original to REV.A (NOVEMBER 2026)	Page
Changed from product preview to production data	All

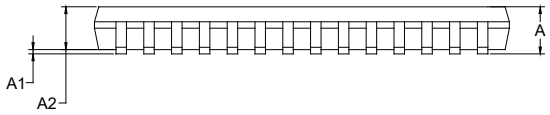
PACKAGE OUTLINE DIMENSIONS

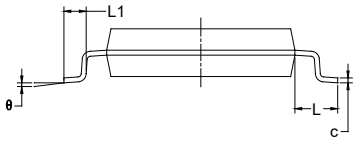
TSSOP-28 (Exposed Pad)





RECOMMENDED LAND PATTERN (Unit: mm)





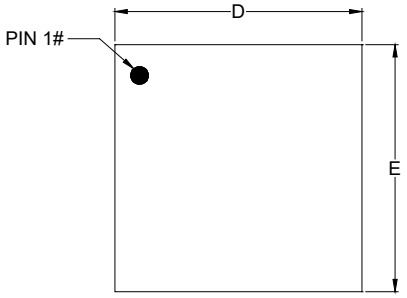
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A		1.200		0.047
A1	0.050	0.150	0.002	0.006
A2	0.800	1.050	0.031	0.041
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
D	9.600	9.800	0.378	0.386
D1	5.300	5.700	0.209	0.224
E	4.300	4.500	0.169	0.177
E1	2.400	2.800	0.094	0.110
E2	6.200	6.600	0.244	0.260
e	0.650 BSC		0.026 BSC	
L	1.000 BSC		0.039 BSC	
L1	0.450	0.750	0.018	0.030
θ	0°	8°	0°	8°

NOTES:

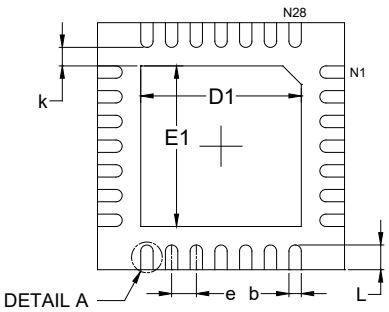
1. Body dimensions do not include mode flash or protrusion.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-153.

PACKAGE OUTLINE DIMENSIONS

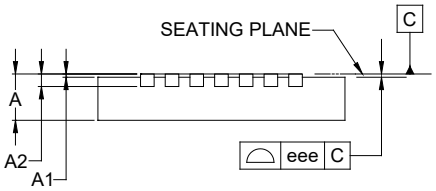
TQFN-4×4-28BL



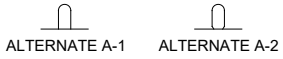
TOP VIEW



BOTTOM VIEW

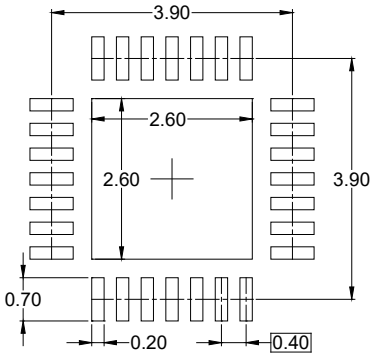


SIDE VIEW



DETAIL A

ALTERNATE TERMINAL CONSTRUCTION



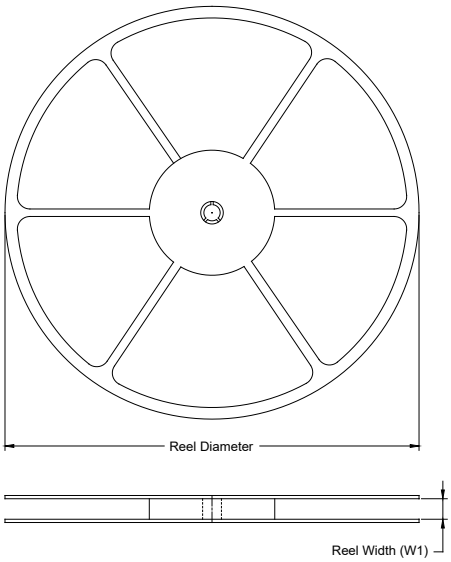
RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	0.700	-	0.800
A1	0.000	-	0.050
A2		0.203 REF	
b	0.150	-	0.250
D	3.900	-	4.100
E	3.900	-	4.100
D1	2.500	-	2.700
E1	2.500	-	2.700
e		0.400 BSC	
k		0.300 REF	
L	0.300	-	0.500
eee		0.080	

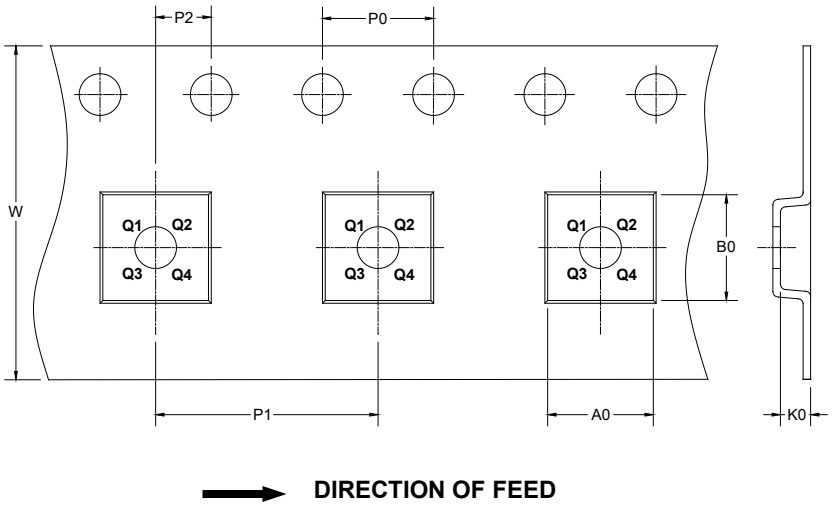
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



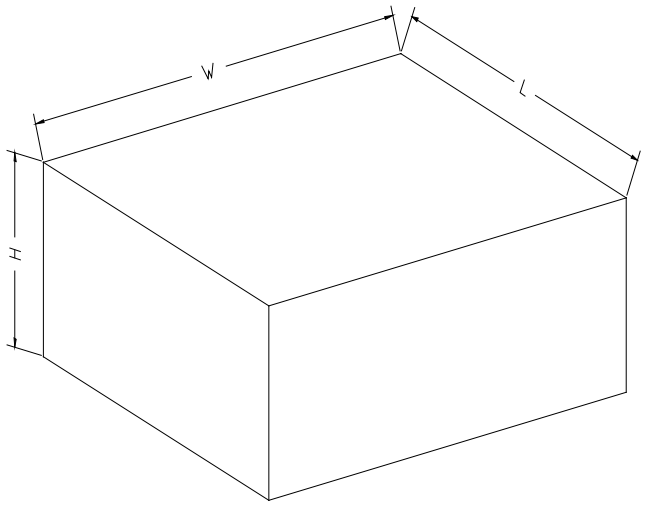
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TSSOP-28 (Exposed Pad)	13"	16.4	6.80	10.25	1.60	4.0	8.0	2.0	16.0	Q1
TQFN-4×4-28BL	13"	12.4	4.30	4.30	1.10	4.0	8.0	2.0	12.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002